# United States District Court

**EASTERN DISTRICT OF TEXAS**
**TYLER DIVISION**

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|---|---|---|
| **CONVERSANT INTELECTUAL PROPERTY MANAGEMENT INC., et al.** | § | **CIVIL ACTION 6:12-cv-847 (LEAD CASE)** |
| **v.** | § | |
| **XILINX, INC.** | § | |
| **CONVERSANT INTELECTUAL PROPERTY MANAGEMENT INC., et al.** | § | |
| **v.** | § | **CIVIL ACTION 6:12-cv-848** |
| **STMICROELECTRONICS, INC.** | § | |

## MEMORANDUM OPINION AND ORDER

This claim construction order construes the disputed claim terms of United States Patents No. 5,577,230, 5,968,036, 7,051,306, 7,945,885, 7,996,811. Plaintiff filed an opening brief (Doc. No. 115), Defendant filed a response (Doc. No. 118), and Plaintiff filed a reply (Doc. No. 118).[1] On November 5, 2014, the Court held a claim construction hearing and heard argument. For the reasons that follow, the Court adopts the constructions set forth herein.

[1] References to docket numbers herein are to Civil Action No. 6:12-CV-847 unless otherwise indicated.

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## BACKGROUND

This is a patent infringement suit. Plaintiff has brought suit alleging infringement of United States Patents No. 5,577,230 ("the '230 Patent"), 5,968,036 ("the '036 Patent"), 7,051,306 ("the '306 Patent"), 7,945,885 ("the '885 Patent"), and 7,996,811 ("the '811 Patent"). STMicroelectronics, Inc. is the only remaining Defendant.

United States Magistrate Judge Keith F. Giblin of this Court previously construed various terms in the patents-in-suit in *MOSAID Technologies, Inc. v. Freescale Semiconductor, Inc.*, No. 6:11-CV-173 ("*Freescale*"), Doc. No. 252, 2013 WL 1819769 (E.D. Tex. Apr. 29, 2013) ("*Freescale Order*"). Judge Giblin also entered a Report and Recommendation recommending denial of a motion for summary judgment of indefiniteness as to Claim 8 of the '230 Patent. No. 6:11-CV-173, Doc. No. 251 (E.D. Tex. Apr. 29, 2013) ("*Freescale MSJ R&R*").

Both sides in *Freescale* moved for reconsideration, but all of the parties settled shortly after the completion of briefing on those motions. *See* No. 6:11-cv-173, Doc. Nos. 255, 256, 260, 262, 265, 267 (briefing); *see also* Doc. No. 270, 6/17/2013 Order for Closing Documents.

## LEGAL PRINCIPLES

Claim construction is a matter of law. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995). The purpose of claim construction is to resolve the meanings and technical scope of claim terms. *U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997). When the parties dispute the scope of a claim term, "it is the court's duty to resolve it." *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008).

The claims of a patent define the scope of the invention. *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1324 (Fed. Cir. 2002). They provide the "metes and bounds" of the patentee's right to exclude. *Corning Glass Works v. Sumitomo Elec. U.S.A., Inc.*, 868 F.2d 1251,

1257 (Fed. Cir. 1989). Accordingly, claim construction begins with and "remain[s] centered on the claim language itself." *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1116 (Fed. Cir. 2004).

Claim terms are normally given their "ordinary and customary meaning." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Id.*

The best guide for defining a disputed term is a patent's intrinsic evidence. *Teleflex*, 299 F.3d at 1325. Intrinsic evidence includes the patent's specification and the prosecution history. *Id.*

The claims are part of the specification. *Markman*, 52 F.3d at 979. The context in which a term is used in the claims instructs the term's construction. *Phillips*, 415 F.3d at 1314; *see also Abtox, Inc. v. Exitron Corp.*, 122 F.3d 1019, 1023 (Fed. Cir. 1997) ("[T]he language of the claim frames and ultimately resolves all issues of claim interpretation."). "Differences among claims can also be a useful guide in understanding the meaning of particular claim terms." *Phillips*, 415 F.3d at 1314.

In addition to the claims, the specification's written description is an important consideration during the claim construction process. *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). The written description provides further context for claim terms and may reflect a patentee's intent to limit the scope of the claims. *Watts v. XL Sys., Inc.*, 232 F.3d 877, 882 (Fed. Cir. 2000). But care must be taken to avoid unnecessarily reading limitations from the specification into the claims. *Teleflex*, 299 F.3d at 1326; *see also Raytheon Co. v. Roper Corp.*, 724 F.2d 951, 957 (Fed. Cir. 1983) ("That claims are interpreted in light of

the specification does not mean that everything expressed in the specification must be read into all the claims."). "[P]articular embodiments appearing in the written description will not be used to limit claim language that has broader effect." *Innova/Pure Water*, 381 F.3d at 1117; *see also Phillips*, 415 F.3d at 1323 ("[A]lthough the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments.").

The prosecution history is also part of the intrinsic evidence. *Phillips*, 415 F.3d at 1317. It "consists of the complete record of the proceedings before the PTO and includes the prior art cited during the examination of the patent." *Id.* Statements made during the prosecution of the patent may limit the scope of the claims. *Teleflex*, 299 F.3d at 1326.

Finally, the Court may rely on extrinsic evidence to aid with understanding the meaning of claim terms. *Markman*, 52 F.3d at 981. Extrinsic evidence includes "all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises." *Id.* at 980. Extrinsic evidence is generally less useful, *Phillips*, 415 F.3d at 1317, and it should not be relied on when it contradicts the intrinsic evidence. *Markman*, 52 F.3d at 981.

Prior claim construction proceedings involving the same patents-in-suit are "entitled to reasoned deference under the broad principals of *stare decisis* and the goals articulated by the Supreme Court in *Markman*, even though *stare decisis* may not be applicable *per se*." *Maurice Mitchell Innovations, LP v. Intel Corp.*, No. 2:04-CV-450, 2006 WL 1751779, at *4 (E.D. Tex. June 21, 2006). The Court nonetheless conducts an independent evaluation during claim construction proceedings. *See, e.g., Texas Instruments, Inc. v. Linear Techs. Corp.*, 182 F. Supp. 2d 580, 589-90 (E.D. Tex. 2002); *Burns, Morris & Stewart Ltd. P'ship v. Masonite Int'l Corp.*,

401 F. Supp. 2d 692, 697 (E.D. Tex. 2005); *Negotiated Data Solutions, Inc. v. Apple, Inc.*, No. 2:11-CV-390, 2012 WL 6494240, at *5 (E.D. Tex. Dec. 13, 2012).

**JUDICIAL ESTOPPEL**

Defendant argues that judicial estoppel bars Plaintiff from "re-litigat[ing] positions that it presented and lost before Judge Giblin." Resp. Br. at 1. Plaintiff replies that neither waiver nor judicial estoppel is applicable here. Reply Br. at 2-4.

"[W]here a party assumes a certain position in a legal proceeding, and succeeds in maintaining that position, he may not thereafter, simply because his interests have changed, assume a contrary position, especially if it be to the prejudice of the party who has acquiesced in the position formerly taken by him." *New Hampshire v. Maine*, 532 U.S. 742, 749 (2001) (quoting *Davis v. Wakelee*, 156 U.S. 680, 689 (1895)); *see Hall v. GE Plastic PTE Ltd.*, 327 F.3d 391, 396 (5th Cir. 2003) ("Judicial estoppel prevents a party from asserting a position in a legal proceeding that is contrary to a position previously taken in the same or some earlier proceeding.") (citation and internal quotation marks omitted). The doctrine of judicial estoppel is governed by regional circuit law. *See, e.g,, Source Search Techs., LLC v. LendingTree, LLC*, 588 F.3d 1063, 1071 (Fed. Cir. 2009).

In evaluating the doctrine, the Court of Appeals for the Fifth Circuit looks primarily to three factors: whether "(1) the party against whom judicial estoppel is sought has asserted a legal position which is plainly inconsistent with a prior position; (2) a court accepted the prior position; and (3) the party did not act inadvertently." *Love v. Tyson Foods, Inc.*, 677 F.3d 258, 261 (5th Cir. 2012); *see Hall*, 327 F.3d at 398, 399-400.

"Adoption does not require a formal judgment; rather, it only requires that the first court has adopted the position urged by the party, either as a preliminary matter or as part of a final

disposition." *In re Superior Crewboats, Inc.*, 374 F.3d 330, 335 (5th Cir. 2004) (citations and internal quotation marks omitted); *see Hall*, 327 F.3d at 398-99 (the "judicial acceptance" requirement does not mean the party must have prevailed on the merits).

"Because the doctrine [of judicial estoppel] is intended to protect the judicial system, rather than the litigants, detrimental reliance by the opponent of the party against whom the doctrine is applied is not necessary." *Id.* at 261. Further, "[b]ecause the rule is intended to prevent improper use of judicial machinery, judicial estoppel is an equitable doctrine invoked by a court at its discretion." *New Hampshire*, 532 U.S. at 750 (citations and internal quotation marks omitted); *see Hall*, 327 F.3d at 396 (quoting *New Hampshire*).

As a threshold matter, Defendant has failed to demonstrate that waiver or judicial estoppel should apply *in the present case* based on any decision by Plaintiff to refrain from objecting to an adverse finding by the judge in *Freescale*. *Cf. Lava Trading, Inc. v. Sonic Trading Mgmt., LLC*, 445 F.3d 1348, 1353 (Fed. Cir. 2006) ("judicial estoppel does not normally apply on appeal to prevent a party from altering an unsuccessful position before the trial court").

As to constructions that were proposed by Plaintiff and adopted in *Freescale*, some authorities caution against allowing a party to abandon a position that was successfully advanced earlier in the same case or a prior case. *See Fitness Quest, Inc. v. Monti*, 330 F. App'x 904, 914 (Fed. Cir. 2009) ("Judicial estoppel can apply to claim construction arguments."); *Mondis Tech. Ltd. v. Chimei Innolux Corp.*, 822 F. Supp. 2d 639, 650 n.14 (E.D. Tex. 2011) (Ward, J.) (". . . InnoLux is judicially estopped from agreeing to a claim construction position, which this Court accepted in its claim construction order, and then urging a different position merely weeks before trial.").

Nonetheless, the evolving nature of claim construction tends to weigh against prohibiting a party from changing its position, even after that position has been adopted by a court. *See SanDisk Corp. v. Memorex Prods., Inc.*, 415 F.3d 1278, 1291 (Fed. Cir. 2005) ("the equities do not favor applying judicial estoppel to prevent claim construction arguments from evolving after preliminary injunction"); *see Jack Guttman, Inc. v. Kopykake Enters., Inc.*, 302 F.3d 1352, 1361 (Fed. Cir. 2002) ("District courts may engage in a rolling claim construction, in which the court revisits and alters its interpretation of the terms as its understanding of the technology evolves.").

Further, review of each of the presently proposed constructions is necessary to determine whether Plaintiff prevailed earlier *and* whether Plaintiff is now proposing a construction that is "plainly inconsistent" with the prior construction. *See Love*, 677 F.3d at 261; *see also LSI Indus., Inc. v. ImagePoint, Inc.*, 279 F. App'x 964 (Fed. Cir. 2008) ("The district court's application of judicial estoppel was misplaced, however, primarily because MDI never prevailed on any argument that these terms were drafted in means-plus-function format."); *Paltalk Holdings, Inc. v. Microsoft Corp.*, No. 2:06-CV-367, 2008 WL 4830571 (E.D. Tex. July 29, 2008) (Folsom, J.) ("PalTalk is not strictly limited to the claim construction positions taken by HearMe [(PalTalk's predecessor-in-interest)], as long as the positions advanced by PalTalk are not 'clearly inconsistent' with those of HearMe in the previous litigation.") (citing *SanDisk*, 415 F.3d at 1290-91).

Based on this framework of legal principles, the Court evaluates the doctrine of judicial estoppel for each term as to which Defendant has asserted the doctrine, as discussed below.

## CONSTRUCTION OF AGREED TERMS

The parties have submitted the following agreed-upon constructions, which the Court hereby adopts:

| Term | Claims | Agreed Construction |
|---|---|---|
| "simultaneously stored" | '230 Patent, Claim 1 | "both contained" |
| "interrupt" | '036 Patent, Claim 1 | "a signal indicating that an event has occurred that requires attention, or that a peripheral is ready to send or receive data" |
| "back biasing" | '811 Patent, Claim 14 | "biasing of the body of a device independently of the source by applying a voltage" |
| "selecting a frequency" | '306 Patent, Claim 16 | "choosing a frequency of operation for the power island" |
| "determine a target power level" | '306 Patent, Claim 16 | "determine a desired, calculated, or specified power consumption for a power island" |
| "based on needs and operation of the integrated circuit" | '306 Patent, Claim 16 | "based on future operational needs and current operating status of the integrated circuit" |
| "first memory means for storing program instructions and data" | '230 Patent, Claim 1 | Function: storing program instructions and data.<br><br>Structure: memory systems, including RAM, ROM, PROM, EPROM, FLASH, EEPROM, and RAM, and equivalents thereof. |
| "second memory means, for storing program instructions and data" | '230 Patent, Claim 1 | Function: storing program instructions and data.<br><br>Structure: memory systems, including RAM, ROM, PROM, EPROM, FLASH, EEPROM, and RAM, and equivalents thereof. |
| "means for requesting transfers of data between the processor and the first memory means and the processor and the second memory means" | '230 Patent, Claim 1 | Function: requesting transfers of data between the processor and the first memory means and the processor and the second memory means.<br><br>Structure: data read/write unit 52 of Figure 3, as referenced at 4:17-24, and equivalents thereof. |

| | | |
|---|---|---|
| "means for requesting fetches of program instructions from the first and second memory means" | '230 Patent, Claim 1 | Function is: requesting fetches of program instructions from the first and second memory means.<br><br>Structure is: Program Fetch Unit 50, and equivalents thereof. |
| "means for arbitrating which of the first and second memory bus interfaces a particular program instruction fetch or data transfer is to take place" | '230 Patent, Claim 1 | Function: arbitrating which of the first and second memory bus interfaces a particular program instruction fetch or data transfer is to take place.<br><br>Structure: arbitration unit 54 in Figure 4 including control process 56 implementing the truth table of Figure 5 and the flowchart of Figure 6 and bus controllers 58, 60, and equivalents thereof. |

Joint Claim Construction and Prehearing Statement, Doc. No. 102 at 2-3.

**CONSTRUCTION OF DISPUTED TERMS IN U.S. PATENT NO. 5,577,230**

The '230 Patent, titled "Apparatus and Method for Computer Processing Using an Enhanced Harvard Architecture Utilizing Dual Memory Buses and the Arbitration for Data/Instruction Fetch," issued on November 19, 1996, from an application filed on August 10, 1994. The Abstract of the '230 Patent states:

> This arbitration unit includes a request controller and two bus controllers. The request controller monitors the instruction fetch or data requests and causes the two bus controllers to implement an instruction fetch or data transfer through one of the two memory interfaces based upon a preassigned priority. Based upon at least one address bit or a control bit contained on a memory management translation table, the request controller identifies which of the memory interfaces to utilize to fetch or transfer data. Preferably, one of the storage areas is random-access memory and the other is read-only memory containing program instructions and read-only data.

**A. "request controller"**

| **Plaintiff's Proposed Construction** | **Defendant's Proposed Construction** |
|---|---|
| "Request controller" is to be given its plain and customary meaning, which is "a processor configured to control a request." | "A portion of the arbitration unit 54 in Figure 4 including control process 56 that implements the truth table of Figure 5 and the flowchart of Figure 6 or equivalents." |

*Freescale* found no construction necessary. *See Freescale Order* at 9-10.

Prior to the hearing, Plaintiff cited *Freescale* and argued that Defendant's proposal sought "to impose a claim limitation from the specification's description of an embodiment." Open. Br. at 6. Defendant responded that adopting Plaintiff's interpretation "would cause claim 2 to be broader than claim 1," which "cannot be correct." Resp. Br. at 4.

But the parties resolved their dispute at the hearing after Plaintiff represented that it would not argue that a request controller can be found outside of the arbitration means structure. Tr. Markman Hr'g 67-68. Accordingly, no further construction is necessary. *See U.S. Surgical*, 103 F.3d at 1568 ("Claim construction is a matter of resolution of disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims, for use in the determination of infringement. It is not an obligatory exercise in redundancy.").

The Court therefore hereby construes **"request controller"** to have its **plain meaning**.

**B. "[wherein the preassigned priority is] dynamic"**

| **Plaintiff's Proposed Construction** | **Defendant's Proposed Construction** |
|---|---|
| "Dynamic" should be construed as: "Not fixed; subject to change." | "Wherein the preassigned priority is dynamic" should be construed as: "Capable of changing the priority of requests while the system is in operation." |

*Freescale* did not address this disputed term.

(1) The Parties' Positions

Plaintiff argues that Defendant's proposal is taken from "a description of *one* embodiment of the invention." Open. Br. at 7. Plaintiff also submits that because "[t]he meaning of 'preassigned priority' is clear and apparent from the Claim language itself," "[t]he Court need not repeat or restate clear language in issuing a *Markman* claim construction order." *Id.* at 7 n.2.

Defendant responds that "[t]he dispute centers on [Plaintiff's] attempt to read 'dynamic' so broadly as to include reprogramming or modifying a system when it is turned off rather than requiring the ability for the priority to change while the system is on." Resp. Br. at 6. Defendant submits that the specification discloses a "dynamic" system in which "the system would adjust the priority as operating conditions unfold." *Id.* at 7. Defendant also argues that "nothing in the specification or file history supports [Plaintiff's] overbroad construction that 'dynamic' should include any change made at any time, even when the system is off to be reworked or reprogrammed." *Id.* Further, Defendant urges, "[f]or all parts of the claim's phrase to make sense and have meaning, a priority that is 'preassigned' before the system begins running must be subject to change after operation commences." *Id.*

Plaintiff replies that "Defendant overlooks the fact that the statement it cites explains these two ways [that the preassigned priority could be made dynamic rather than being static] are merely '[e]xamples of dynamic preassigned priorities.'" Reply Br. at 4 (quoting '230 Patent at 5:34). Plaintiff further explains:

> The system gives priority to interrupts based on a criteria that is "preassigned." If the system allows the user to change that preassigned criteria, then the preassigned criteria is "dynamic." It is not established in the system as a "constant" (*See* '230 Patent, 5:33) – the user can change it. Plaintiff's construction is entirely consistent with the specification.

*Id.* at 5.

(2) Analysis

Although Plaintiff proposes that only "dynamic" should be construed, the parties' briefing demonstrates a dispute as to the entire term "wherein the preassigned priority is dynamic," and the Court has a duty to resolve that dispute. *See O2 Micro*, 521 F.3d at 1362.

Claim 3 of the '230 Patent recites:

> 3. The apparatus according to claim 2, wherein the preassigned priority is dynamic.

Claims 1 and 2, from which Claim 3 depends, do not shed any light on the meaning of a "preassigned priority" being "dynamic."

The specification discloses:

> [W]hen a simultaneous request is made for both program instruction and data on the same bus, as in the affirmative response to step 660 (Events 7, 9, 13 and 15), then the control process 56 (step 670) selects a source based on the *preassigned priority* of the truth table in FIG. 5, i.e., either the program fetch unit 50 or data read/write unit 52 and initiates the selected access (steps 670, 690) giving that source priority on the bus in conflict. The control process incorporates *preassigned priority* which may be based upon the needs of the particular application. *The "preassigned priority" may be constant, e.g. static or it may be dynamic. Examples of dynamic preassigned priorities are that priority could be given to the request most frequently made on the bus in conflict or to the most recent past request on the bus in conflict.*

'230 Patent at 5:24-37 (emphasis added); *see id.* at Fig. 5.

The specification thus explains that the constituent term "preassigned" refers to rules that have been arranged in advance of a particular bus request. *See id.* at 5:24-37. Further, as Defendant argues, the rules can be changed during operation of the system based on events that occur during operation. *See id.* at 5:32-37. Although Plaintiff urges that such a reading improperly imports limitations from a preferred embodiment, interpretation of the terms "preassigned" and "dynamic" in light of the specification is necessary to give meaning to all of the words in the claim. *See, e.g., Digital-Vending Servs. Int'l, LLC v. Univ. of Phoenix, Inc.*, 672

F.3d 1270, 1275 (Fed. Cir. 2012) ("[C]laims are interpreted with an eye toward giving effect to all terms in the claim.") (quoting *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 950 (Fed. Cir. 2006)). Plaintiff's proposal, by contrast, would be vastly overbroad by encompassing a change by any mechanism at any time.

The Court therefore hereby construes **"wherein the preassigned priority is dynamic"** to mean **"wherein the system is capable of changing the rules for prioritizing requests while the system is in operation."**

**C. "instruction data"**

| **Plaintiff's Proposed Construction** | **Defendant's Proposed Construction** |
|---|---|
| Plain and ordinary meaning | "The output of self-modifying code written to memory and subsequently executable by the processor." |

Defendant here proposes the construction that the parties agreed upon in *Freescale*. *See Freescale Order* at 13.

(1) The Parties' Positions

Plaintiff argues that from the language of Claim 8, "it is apparent that the instruction data comes from self-modifying code." Open. Br. at 9. Plaintiff further argues that Claim 8 does not require that the instruction data be "written to memory" and does not limit execution to the processor. *Id.*

Defendant responds that judicial estoppel applies because Plaintiff "*agreed* to the construction Judge Giblin adopted, and which [Defendant] now proposes." Resp. Br. at 8.

Defendant also responds that Plaintiff's proposal is contrary to the claims and the specification and is also contrary to the construction that Plaintiff agreed to in *Freescale*. *Id.* at 8-10. As to the claim language, Defendant argues that Claim 8 "requires that the 'instruction

data' of 'self-modifying code' be included within the 'program instructions' described in claim 1," which are recited as being stored in the first and second memory means. *Id.* at 9. Further, Defendant submits, "Claim 8 requires that the instruction data be "executable as a program instruction.'" *Id.* As to the specification, Defendant urges that "[t]he requirements of memory and a processor are not optional features of one potential embodiment--they are essential aspects of the claimed invention's architecture and thus every embodiment." *Id.*

Plaintiff replies that "Plaintiff's position is that 'instruction data' requires no construction; a position not 'plainly inconsistent' with its agreement in *Freescale* to a compromised construction of the term." Reply Br. at 5 (quoting *Love*, 677 F.3d at 261). Plaintiff also submits:

> Defendant cites the specification's reference to a microprocessor in its architecture that makes "requests for memory accesses to either of the buses" and that is "able to modify program memory using data accesses." [Doc. 118 at 9-10]. These statements do not equate to a limitation that "the processor" execute "instruction data."

*Id.* at 5 (square brackets in original).

<u>(2) Analysis</u>

Even assuming that Plaintiff's proposal of "plain and ordinary meaning" is inconsistent with the construction agreed upon in *Freescale*, because the *Freescale* construction was agreed upon the Court declines to apply judicial estoppel. *See New Hampshire*, 532 U.S. at 750 ("Because the rule is intended to prevent improper use of judicial machinery, judicial estoppel is an equitable doctrine invoked by a court at its discretion.") (citations and internal quotation marks omitted); *see Hall*, 327 F.3d at 396.

The disputed term appears in Claim 8 of the '230 Patent, which depends from Claim 1. Claims 1 and 8 of the '230 Patent recite (emphasis added):

> 1. Apparatus for interfacing computer memory using an enhanced Harvard architecture, which comprises:
>
> a) first memory means for storing program instructions and data;
>
> b) second memory means, for storing program instructions and data, such that program instructions and data may be simultaneously stored in at least one of said first or said second memory means; and
>
> c) a processor coupled to the first and second memory means by respective first and second interface buses, the processor including:
>
> means for requesting fetches of program instructions from the first and second memory means;
>
> means for requesting transfers of data between the processor and the first memory means and the processor and the second memory means; and
>
> means for arbitrating which of the first and second memory bus interfaces a particular program instruction fetch or data transfer is to take place.
>
> * * *
>
> 8. The apparatus according to claim 1, wherein at least a portion of the program instructions may include self-modifying code which generates *instruction data*, which *instruction data* in turn is executable as a program instruction.

The specification discloses:

> The present invention solves the problem of determining over which bus a particular transaction must be made by utilizing a novel on-chip arbitration unit which services the microprocessor's requests for memory accesses to either of the buses, made by an instruction fetch unit or a data read/write unit.

*Id.* at 2:62-67.

Claim 8 recites that instruction data is "executable as a program instruction" but does not refer to a processor. Defendant makes a series of inferences to support its proposal that instruction data is "written to memory" and is "executable by the processor."

First, Defendant infers that because the instruction data is generated by self-modifying code that is part of "program instructions," the "instruction data" is "program instructions." That instruction data is generated by program instructions, however, does not demonstrate that instruction data *is* program instructions. Likewise, that "instruction data . . . is executable as a

program instruction," as recited in Claim 8, does not establish that instruction data *is* a program instruction.

Second, Defendant infers that instruction data must be stored in the first "memory means for storing program instructions and data" or the "second memory means, for storing program instructions and data," which is where "program instructions" are stored. Defendant has failed to support this inference with any evidence. Again, that instruction data is generated by program instructions does not demonstrate that instruction data *is* program instructions.

Third, Defendant infers that because the "processor" is "coupled to the first and second memory means," the program instructions stored therein, including the instruction data, must be executable by the processor. Defendant has failed to support this inference with any evidence. Indeed, Claim 1 does not recite the processor executing program instructions, let alone instruction data. Instead, the processor is recited as including means for requesting fetches of program instructions, requesting transfers of data, and arbitrating requests.

Because Defendant's proposal is based on unsupported inferences, Defendant's proposed construction is hereby expressly rejected. No further construction is necessary. *See U.S. Surgical*, 103 F.3d at 1568.

The Court therefore hereby construes **"instruction data"** to have its **plain meaning**.

**D. "may include self-modifying code"**

| **Plaintiff's Proposed Construction** | **Defendant's Proposed Construction** |
|---|---|
| "Adapted to support the coexistence of self-modifying code with data and program memory." | "The stored program instructions recited in Claim 1 include self-modifying code." |

*Freescale* found:

> The court rejects Plaintiffs' suggestion that the claim [(Claim 8)] should be construed to mean "capable of supporting self-modifying code," because it would

> re-write Claim 8. Claim 8 is not directed to a capability of the apparatus to support self-modifying code; rather, Claim 8 is directed toward imposing a further limitation on the stored program instructions recited in Claim 1. Although Plaintiffs' proposal is incorrect, so is Defendants' argument that Claim 8 does not present a narrowing limitation to Claim 1.
>
> In view of the specification, the court concludes that the POSITA [(person of ordinary skill in the art)] would understand the phrase "may include self-modifying code" in Claim 8 to mean that the stored program instructions recited in Claim 1 include self-modifying code.

*Freescale MSJ R&R* at 6.

(1) The Parties' Positions

Plaintiff submits that whereas Defendant's proposal rewrites "may" to "shall," Plaintiff's proposal is consistent with the claim language, as well as the specification, which "teaches that the system 'supports' self-modifying code (i.e., it 'may' include it), not that the system 'must' include self-modifying code." Open. Br. at 9-10 (citing '230 Patent at 2:38-42).

Defendant responds that Plaintiff "is again attempting to relitigate a construction it lost before Judge Giblin and did not seek to have [the presiding district judge] review in the *Freescale* case." Resp. Br. at 10.

Defendant also argues that here as in *Freescale*, the Court should find that "a capability construction cannot be correct, because the suggested capability is already inherent in claim 1 from which claim 8 depends." *Id.* at 11.

Plaintiff replies that the capability proposed by Defendant is *not* inherent in claim 1. Reply Br. at 6 (citing *Johnson Worldwide Assocs., Inc. v. Zebco, Inc.*, 175 F.3d 985, 992 (Fed. Cir. 1999) ("[M]ere inferences drawn from the description of an embodiment of the invention cannot serve to limit claim terms.")). Plaintiff further contends that *Freescale* improperly rewrote "may" as "shall." Reply Br. at 6 (citing *Terlep v. Brinkman Corp.*, 418 F.3d 1379, 1382 (Fed. Cir. 2005) ("The construction of claims is simply a way of elaborating the normally terse claim

language in order to understand and explain, but not to change, the scope of the claims." (citation and internal quotation marks omitted)).

(2) Analysis

As a threshold matter, although *Freescale* agreed with Plaintiff that Claim 8 is not indefinite, *Freescale* "reject[ed] Plaintiffs' suggestion that the claim should be construed to mean "capable of supporting self-modifying code." *Freescale MSJ R&R* at 6. Because *Freescale* rejected the interpretation proposed by Plaintiff in that case, judicial estoppel does not apply. *Love*, 677 F.3d at 261 (considering whether the "court accepted the prior position"). Further, Defendant has failed to demonstrate that waiver or judicial estoppel should apply in the present cases based on any decision by Plaintiff to refrain from objecting to an adverse finding by the magistrate judge in *Freescale*. *Cf. Lava Trading*, 445 F.3d at 1353 ("judicial estoppel does not normally apply on appeal to prevent a party from altering an unsuccessful position before the trial court").

Claim 8 of the '230 Patent recites (emphasis added):

> 8. The apparatus according to claim 1, wherein at least *a portion* of the program instructions *may include self-modifying code* which generates instruction data, which instruction data in turn is executable as a program instruction.

Defendant's proposal that "[]the stored program instructions recited in Claim 1 include self-modifying code" is too narrow because Claim 8 refers to "at least a portion of the program instructions," not necessarily all of the program instructions.

As to supporting the "coexistence of self-modifying code with data and program memory," as Plaintiff has proposed, the Background of the Invention states:

> [A] need exists for a computer system architecture for use in mobile or portable computing and high performance system applications, which provides the advantages of the dual bus interface of conventional Harvard architecture while *supporting read-only data and self-modifying code* wherein both instructions and

> data may be stored in each of two memory storage areas connected to the microprocessor by independent buses.

'230 Patent at 2:28-35 (emphasis added). The Summary of the Invention then states: "The present invention provides apparatus and methods for computer processing using an enhanced Harvard architecture for a computer system which *supports read-only data coexisting with program memory and self-modifying code*." *Id.* at 2:39-42 (emphasis added).

Further, Plaintiff urges that its proposal of "adapted to support" is not vague but rather is supported by precedent. Open. Br. at 10 (citing *Power-One, Inc. v. Artesyn Techs., Inc.*, 599 F.3d 1343, 1348 (Fed. Cir. 2010) ("[T]he terms 'adapted to' and 'near' are not facially vague or subjective. Claims using relative terms such as 'near' or 'adapted to' are insolubly ambiguous only if they provide no guidance to those skilled in the art as to the scope of that requirement.")).

On balance, the Court gives "reasoned deference" to the findings in *Freescale*, in particular as to the finding that "Claim 8 is directed toward imposing a further limitation on the stored program instructions recited in Claim 1." *Freescale MSJ R&R* at 6; *Maurice Mitchell Innovations*, 2006 WL 1751779, at *4. Nonetheless, this limitation applies to "at least a portion" of the program instructions, not necessarily all of the program instructions recited in Claim 1.

The Court therefore hereby construes **"may include self-modifying code"** to mean **"at least a portion of the program instructions include self-modifying code."**

**CONSTRUCTION OF DISPUTED TERMS IN U.S. PATENT NO. 5,958,036**

The '036 Patent, titled "Circuit for Arbitrating Interrupts with Programmable Priority Levels," issued on September 28, 1999, from an application filed September 8, 1997. The Abstract of the '036 Patent states:

> Apparatus for arbitrating the selection of an interrupt for servicing from a plurality of interrupts in which a priority level for each of the plurality of interrupts is programmed in a first register and each of the interrupts which is to

> be evaluated for selection for servicing is set as pending in a second register. Only a pending interrupt having a priority level above a pre-set current interrupt priority level is selected for servicing and where multiple pending interrupts of the same priority level occur, the one with the highest order bit position in the second register is used.

**A. "first register having a plurality of interrupts each being programmed at one of a plurality of priority levels" and "second register in which a state is set for certain of said plurality of interrupts to be in a pending state"**

| **"first register having a plurality of interrupts each being programmed at one of a plurality of priority levels"** | |
|---|---|
| **Plaintiff's Proposed Construction** | **Defendant's Proposed Construction** |
| "A *first* storage area divided into a series of memory fields, each corresponding to an interrupt and programmed to indicate one of multiple priority levels." | "A storage area divided into a series of memory fields, each corresponding to an interrupt and programmed to indicate one of multiple priority levels." |
| **"second register in which a state is set for certain of said plurality of interrupts to be in a pending state"** | |
| **Plaintiff's Proposed Construction** | **Defendant's Proposed Construction** |
| "A *second* storage area divided into a series of memory fields, each indicating whether the corresponding interrupt in the first register is pending." | "A storage area divided into a series of memory fields, each indicating whether the corresponding interrupt in the first register is pending." |

*Freescale* "conclude[d] that the proper construction of this ["first register . . ."] term is 'a storage area divided into a series of memory fields, each corresponding to an interrupt and programmed to indicate one of multiple priority levels.'" *Freescale Order* at 27.

Prior to the hearing, Plaintiff argued that "[t]he Claim's language explicitly identifies two distinct registers." Open. Br. at 12. Defendant responded that Plaintiff's proposals of "first" and "second" were "potentially misleading because they would suggest to the jury that two completely distinct registers are required to meet the claims." Resp. Br. At 12.

At the hearing, Plaintiff clarified that it does not intend to argue that two registers must be physically separate circuitry. Tr. Markman Hr'g 27-28, Nov. 5, 2014. Instead, Plaintiff represented that it only intended to argue that there are "two different types of functions that are being performed" in Claim 1. *Id.* at 27. Because Defendant indicated that its only concern in briefing this term was that Plaintiff would argue physical separateness, the parties agreed they had resolved their dispute on this term. *Id.* at 28.

The Court accordingly hereby construes the terms as set forth in the following chart:

| Term | Construction |
|---|---|
| **"first register having a plurality of interrupts each being programmed at one of a plurality of priority levels"** | **"a storage area divided into a series of memory fields, each corresponding to an interrupt and programmed to indicate one of multiple priority levels"** |
| **"second register in which a state is set for certain of said plurality of interrupts to be in a pending state"** | **"a storage area divided into a series of memory fields, each indicating whether the corresponding interrupt in the first register is pending"** |

**B. "an arbitration circuit responsive to the data in said first and second registers"**

| **Plaintiff's Proposed Construction** | **Defendant's Proposed Construction** |
|---|---|
| "A circuit that identifies pending interrupts from the second register and decodes the priority of interrupts from the first register. The circuit is 'responsive' to register data in the sense that it operates based on the programmed priority levels of the first register and the settings in the second register for pending interrupt requests." | No construction is necessary. |

*Freescale* found no construction necessary:

> The claim language is complete in itself to set forth the functional capability that is defining of the "arbitration circuit." The circuit is "responsive" to register data in the sense that it operates based on the programmed priority levels of the first register and the settings in the second register for pending interrupt requests. The

> parties' dispute is resolved by rejecting both constructions. Both Plaintiffs' and Defendants' constructions are inconsistent with the specification and the claim language. As an addition[al] note, both parties appear to consider that the term "arbitration" need not be construed as neither includes anything about it in their respective constructions.

*Freescale Order* at 30.[2]

(1) The Parties' Positions

Plaintiff submits that its proposed construction incorporates the findings in *Freescale* and is supported by the specification, in particular Figures 2A and 2B. Open. Br. at 13. Plaintiff concludes that "[i]n order to select an interrupt, the circuit must necessarily identify which interrupts are pending by examining the second register, which contains that information." *Id.*

Alternatively, Plaintiff submits:

> The Freescale Order determined that the decoding is performed by a "mask decoder," rather than the arbitration circuit. If the Court interprets the '036 Patent similarly, the Court can simply remove the phrase "and decodes the priority of interrupts from the first register" from Plaintiff's proposed construction, and the construction will still assist the jury by explaining the arbitration circuit's responsiveness.

*Id.* at 13 n.4.

Defendant responds that "[y]et again, [Plaintiff] is advancing a construction that Judge Giblin considered and rejected in *Freescale* and [Plaintiff] did not ask [the presiding district judge] to review." Resp. Br. at 13.

Defendant also argues that "[i]t is the mask decoder . . ., not the arbitration circuit . . ., that performs the identifying and decoding functions that [Plaintiff] seeks to require from the 'arbitration circuit.'" *Id.* at 14 (citing '036 Patent at 3:44-60). "Nowhere in the specification,"

---

[2] In *Freescale*, Plaintiff proposed: "a circuit that identifies pending interrupts from the second register and decodes the priority of interrupts from the first register." *Freescale Order* at 28. The defendants proposed: "a circuit that identifies pending interrupts from the data in the second register and decodes the priority of such pending interrupts using the data in the first register." *Id.*

Defendant argues, "does the arbitration circuit identify and decode interrupts." *Id.* As to Plaintiff's alternative proposal, Defendant responds that both decoding and identifying are features of the mask decoder, not the arbitration circuit. *Id.* Defendant concludes that "[Plaintiff] has proposed a self-contradictory construction that includes both language that was rejected by Judge Giblin, and Judge Giblin's reasoning for rejecting that language." *Id.* at 15.

Plaintiff replies that "[t]o select an interrupt, the circuit inherently must examine the second register to determine which interrupts are pending." Reply Br. at 7.

(2) Analysis

As a threshold matter, Defendant has failed to demonstrate that waiver or judicial estoppel should apply in the present cases based on any decision by Plaintiff to refrain from objecting to an adverse finding by the magistrate judge in *Freescale*. *Cf. Lava Trading*, 445 F.3d at 1353 ("judicial estoppel does not normally apply on appeal to prevent a party from altering an unsuccessful position before the trial court").

Claim 1 of the '036 Patent recites (emphasis added):

> 1. Apparatus operating with a plurality of interrupts in which a pending interrupt is to be selected for servicing on a priority level basis, comprising:
>
> a first register having a plurality of interrupts each being programmed at one of a plurality of priority levels;
>
> a second register in which a state is set for certain of said plurality of interrupts to be in a pending state so as to be evaluated for selection for servicing; and
>
> *an arbitration circuit responsive to the data in said first and second registers* programmed to select and pass for servicing one interrupt of a pending state having a predetermined one or more of said plurality of priority levels.

The specification discloses a register that stores information in a series of bits that indicate whether corresponding interrupts are pending:

> In the present invention, when an interrupt request occurs for one of a plurality of devices, a corresponding assigned bit is set in a register (INS) and the interrupt is then considered to be pending.

’036 Patent at 1:39-42; *see id.* at Fig. 2B. The specification also discloses a register that stores priorities:

> The interrupt specification requires the circuit to first evaluate each interrupt against its programmed priority level, and then to arbitrate competing interrupts by accounting for priority level and bit position in the INS register.

*Id.* at 1:62-65; *see id.* at Fig. 2A; *see also id.* at 2:50-64, 3:3-5, 3:44-45 (“A mask decoder 30 is used to mask, or decode, the priority of each pending interrupt (set to logic 1 in INS 25).”).

Further, the specification discloses an arbitrator circuit that passes interrupts based on a priority level:

> The priority arbitrator circuit 50 receives an input on the respective lines 49-1, 49-2 and 49-3 from each of the LBDs 40-1, 40-2 and 40-3 having a pending interrupt. The arbitrator 50 is pre-set with a current interrupt priority level (CIPL) instruction on line 48 by the application program to establish the priority level of the interrupt that is to be passed to be serviced. That is, it might be decided by a program instruction provided to arbitrator 50 to honor and service only interrupts whose priority level is greater than 2. This illustrative example is shown in FIG. 1.
>
> The arbitrator 50 essentially is a unit that has three AND gates, each gate corresponding to a priority level. The AND gate, or gates, which are to effect passage of interrupts above a priority level as set on CIPL line 48 are enabled.

*Id.* at 7:34-47.

Plaintiff’s proposal of “[a] circuit that identifies pending interrupts from the second register and decodes the priority of interrupts from the first register,” however, is contrary to the findings in *Freescale*:

> The claim language itself defines the functional capability of the arbitration circuit (i.e., select and pass an interrupt for servicing). The circuitry for doing so is Interrupt Priority Arbitration circuit 50 together with decision select circuit 60. What Plaintiffs’ construction advances is different functionality than specified in the claim. The identification of interrupts in the second register and the decoding of the priority of the interrupts is the function of mask decoder 30. Plaintiffs misread the claim language and their proposed construction is rejected.

*Freescale Order* at 29.

On balance, the Court gives "reasoned deference" to the findings in *Freescale*. *See id.* at 29-30; *Maurice Mitchell Innovations*, 2006 WL 1751779, at *4. The latter portion of Plaintiff's proposed construction is substantially supported by the above-quoted disclosures and will assist the finder of fact.

The Court therefore hereby construes **"an arbitration circuit responsive to the data in said first and second registers"** to mean **"a circuit that operates based on the programmed priority levels of the first register and the settings in the second register for pending interrupt requests."**

**C. "register"**

| **Plaintiff's Proposed Construction** | **Defendant's Proposed Construction** |
|---|---|
| "A temporary storage unit." | "A storage area divided into a series of memory fields." |

*Freescale* did not address this disputed term apart from constructions of larger disputed terms.

<u>(1) The Parties' Positions</u>

Plaintiff argues that "register" need not be construed apart from the constructions of other disputed terms that include the term "register." Open. Br. at 14. Alternatively, Plaintiff proposes "if the Court construes 'register' separately, it should incorporate the temporary nature of the storage, which is implicit throughout the specification." *Id.* (citing '036 Patent at 2:41-4:30 & Figs. 1-2C).

Defendant responds: "Once again, [Plaintiff] seeks to alter a construction it persuaded Judge Giblin to adopt. At that time, [Plaintiff] did not advocate a construction of register that

added a requirement of 'temporary' storage and has no basis for reversing course now." Resp. Br. at 15.

Defendant also argues that "[a]lthough registers often do store information temporarily, there is nothing inherent in the concept of a register as used in the art, or in the '036 patent, that prevents a register from serving as a permanent repository if the circuit designer so chooses." *Id.*

Plaintiff replies that judicial estoppel does not apply because "Plaintiff has stated, as it did in *Freescale*, that 'the term 'register' is already being construed within the context of 'first register' and 'second register' and does not need separate construction.'" Reply Br. at 8.

(2) Analysis

As a threshold matter, Defendant has failed to demonstrate that Plaintiff's proposal of referring to "temporary" storage is "plainly inconsistent" with Plaintiff's positions in *Freescale*. *See Love*, 677 F.3d at 261.

Nonetheless, neither the two columns of the specification cited by Plaintiff. nor anything else in the '036 Patent warrants limiting the term "register" to being a "temporary" storage unit.

The Court therefore hereby construes **"register"** to have its **plain meaning** apart from the constructions of other disputed terms in which "register" appears, addressed above.

**CONSTRUCTION OF DISPUTED TERMS IN U.S. PATENTS NO. 7,051,306, 7,945,885, AND 7,996,811**

The '306 Patent, titled "Managing Power on Integrated Circuits Using Power Islands," issued on May 23, 2006, and bears an earliest priority date of May 7, 2003. The Abstract of the '306 Patent states:

> Systems and methods manage power in an integrated circuit using power islands. The integrated circuit includes a plurality of power islands where power consumption is independently controlled within each of the power islands. A power manager determines a target power level for one of the power islands. The power manager then determines an action to change a consumption power level of

> the one of the power islands to the target power level. The power manager performs the action to change the consumption power level of the one of the power islands to the target power level.

The ’885 Patent and the ’811 Patent are both titled “Power Managers for an Integrated Circuit.” The ‘885 Patent issued on May 17, 2011. The ’811 Patent issued on August 9, 2011. Both the ’885 Patent and the ’811 Patent bear an earliest priority date of May 7, 2003. The Abstracts of the ’885 Patent and the ’811 Patent are the same and state:

> A system for an integrated circuit comprising a plurality of power islands includes a first power manager and a second power manager. The first power manager manages a first power consumption for the integrated circuit based on needs and operation of the integrated circuit. The second power manager communicates with the first power manager and manages a second power consumption for one of the power islands.

The ’885 Patent is a continuation of United States Patent No. 7,415,680 (“the ’680 Patent”), which in turn is a continuation of the ’306 Patent. The ‘811 Patent is a continuation of a continuation of the ’680 Patent.

**A. “power island(s)”**

| **Plaintiff’s Proposed Construction** | **Defendant’s Proposed Construction** |
|---|---|
| “A section of the integrated circuit with independently controllable voltage and independently controllable frequency to two or more non-zero frequencies.” | “A section of an integrated circuit where power consumption is controlled by independently varying its operating voltage and its frequency of operation.” |

*Freescale* found:

> Plaintiffs’ construction incorrectly includes reference to “non-zero frequency,” which is superfluous to an understanding of the term “power island.” Plaintiffs are correct, however, that both voltage control and frequency control are contemplated by the term when read in view of the intrinsic evidence.
>
> The court therefore construes this term as: “a section of an integrated circuit where power consumption is controlled by independently varying its operating voltage and its frequency of operation.”

*Freescale Order* at 44.

Before the hearing, Plaintiff argued that the *Freescale* construction should be modified so as to refer to "two or more non-zero frequencies" because "a jury may not share the Court's understanding of a zero frequency signal" as being "a DC signal, which is not time-variant, and actually not a frequency signal at all." Open. Br. at 15 (quoting *Freescale Order* at 43).

At the hearing, Defendant agreed that it would not argue that turning the power off, resulting in a zero frequency, is a frequency of operation. Tr. Markman Hr'g 54, Nov. 5, 2014. With that agreement, both Parties represented that they had no issue with the *Freescale* construction. *Id.*

The Court therefore substantially adopts the *Freescale* construction but modifies it to clarify that power consumption could be controlled by varying voltage *or* frequency (or both), which appears to have been the understanding in *Freescale*. *See Freescale Order* at 43-44.

The Court accordingly hereby construes **"power island"** to mean **"a section of an integrated circuit where power consumption is controlled by independently varying its operating voltage or its frequency of operation (or both)."**

**B. "power manager"**

| **Plaintiff's Proposed Construction** | **Defendant's Proposed Construction** |
|---|---|
| "Any system, circuitry or device configured to control power." | "Circuitry, device, or system configured to determine a target power level of a power island, determine an action to change the target power level, and perform an action to change the consumption power level to the target power level." |

*Freescale* found:

> Defendants are correct that the specification gives a specific definition of the "power manager." *See, e.g.,* '306 patent at 4:18-28. The court will construe these terms ["power manager" and "power manager to control the power consumptions"] to mean: []"circuitry, device, or system configured to determine a target power level of a power island, determine an action to change the target

> power level, and perform an action to change the consumption power level to the target power level."

*Freescale Order* at 46.

(1) The Parties' Positions

Plaintiff argues that *Freescale* erred because "[i]n this case, there is no clearly definitional language and, contrary to law, the construction Defendant proffers chooses one of multiple disclosed embodiments while excluding others." Open. Br. at 17. Plaintiff argues that disclosures concerning coordination between Master Power Managers ("MPMs"), Intermediate Power Managers ("IPMs"), and Slave Power Managers ("SPMs") would be "illogical if each power manager is separately working" as Defendant has proposed. *Id.* at 18. Plaintiff urges that "adding limitations from the specification will not aid the jury's understanding because the relevant features of the power manager in each claim are already clearly stated in the claims." *Id.* at 19. Plaintiff concludes:

> Defendant's proffered construction would improperly restrict all of the claimed power managers to one of the several embodiments claimed. Defendant['s] intention is to define "power manager" to include all of the "power manager" limitations from Claim 16 of the '306 patent. When Defendant['s] definition is actually applied to Claim 16, the term becomes redundant and makes no sense; when applied to the other patents, the definition improperly takes the limitations of Claim 16 and shoe-horns them into every other claim.

Open. Br. at 20.

Defendant responds that *Freescale* adopted the "explicit definition" of "power manager" in the specification. Resp. Br. at 17. Defendant also argues this definition of "power manager" is consistent with the disclosures concerning MPMs, IPMs, and SPMs, "which may be used together to implement the claimed power manager." *Id.* at 17-18. Further, Defendant argues, Plaintiff's argument regarding applying Defendant's proposal to Claim 16 "seeks to elevate form over substance." *Id.* at 19. Finally, Defendant urges that "[t]he definition of 'power manager'

was established in the ’306 patent, and [Plaintiff’] cannot retroactively broaden or undo that definition using the claims of related patents that were not drafted until years after the ’306 patent had issued,” particularly given that “the later filed patents each share the same specification as the ’306 patent, including the definition of ‘power manager.’” *Id.* at 20.

Plaintiff replies that “the specification’s statement that a system ‘may’ combine an MPM, an IPM and an SPM does not support Defendant’s proposal that would require *each* of these power managers to contain the complete functionality its construction describes.” Reply Br. at 9. Plaintiff also submits that “[t]he specific functionality of a ‘power manager’ within the claims varies between the claims.” *Id.*

(2) Analysis

The specification discloses:

> *The power manager 120 is any circuitry, device, or system configured to (1) determine a target power level for one of the power islands* 112, 114, 116, and 118 where power consumption is independently controlled within each of the power islands 112, 114, 116, and 118, *(2) determine action to change a consumption power level of the one of the power islands* 112, 114, 116, and 118 *to the target power level*, and *(3) perform the action to change the consumption power level of the one of the power islands* 112, 114, 116, and 118 *to the target power level*. The power manager 120 can dynamically change the power consumption of the power islands 112, 114, 116, and 118 based on the needs and operation of the integrated circuit 110. The target power level is a desired, calculated, or specified power consumption of the power islands 112, 114, 116, and 118. *Some examples of the power manager 120 are the slave power manager (SPM), the intermediate power manager (IPM), and the master power manager (MPM), which are described in further detail below. The power manager 120 may be a hierarchy or group of power managers 120.* Although FIG. 1 depicts the power manager 120 as being located outside the integrated circuit 110, other embodiments may have the power manager 120 located in the integrated circuit 110. In other embodiments, the power manager 120 may be distributed among multiple power managers that are on or off the integrated circuit 110 or integrated with a CPU.

’306 Patent at 4:18-44 (emphasis added). The Summary of the Invention similarly states:

> A power manager determines a target power level for one of the power islands. The power manager then determines an action to change a consumption power level of the one of the power islands to the target power level. The power manager performs the action to change the consumption power level of the one of the power islands to the target power level.

*Id.* at 2:24-30.

On one hand, a patentee may define a term in the specification. *See Sinorgchem Co., Shandong v. Int'l Trade Commc'n*, 511 F.3d 1132, 1136 (Fed. Cir. 2007) (noting that "the word 'is' . . . may signify that a patentee is serving as its own lexicographer") (citation and internal quotation marks omitted); *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1117 (Fed. Cir. 2004) ("All that is required is that the patent applicant set out the different meaning in the specification in a manner sufficient to give one of ordinary skill in the art notice of the change from ordinary meaning."); *see also Cell & Network Selection LLC v. AT&T Inc.*, 6:13-CV-403, 2014 WL 3671029, at *2 (E.D. Tex. July 23, 2014) (holding that the specification defined "paging channel" by disclosing: "The paging channel is an encoded, interleaved, spread, and modulated spread spectrum signal that is used by mobile stations operating within the coverage area of the base station. The base station uses the paging channel to transmit system overhead information and mobile station specific messages.").

On the other hand, these disclosures concern the operation of a "power manager" rather than a definition of one. Such a reading is reinforced by the claims, some of which recite the limitations proposed by Defendant but others of which do not. Claim 16 of the '306 Patent recites (emphasis added):

> 16. A system for an integrated circuit comprising a plurality of power islands where power consumption is independently controlled within each of the power islands, the system comprising:
>
> power control circuitry configured to control power for one of the power islands; and

a *power manager* configured to *determine a target power level* for the one of the power islands based on needs and operation of the integrated circuit, *determine at least one of actions to change a power consumption level* of the one of the power islands to the target power level, and *perform the at least one of the actions to change the power consumption level* of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands.

Claim 8 of the ’885 Patent recites (emphasis added):

8. An integrated circuit comprising:

an integrated circuit chip;

a plurality of power islands disposed on the integrated circuit chip having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;

one or more power consumption signals indicating one or more of the power consumptions;

a *power manager* disposed on the integrated circuit chip and coupled to each of the power islands configured to monitor the one or more power consumption signals, the *power manager* being configured to *individually control each of the power consumptions*, and the *power manager* being configured to *change power consumption in at least one of the power islands* in response to a power consumption change request.

Claim 1 of the ’811 Patent recite (emphasis added):

1. A system comprising:

an integrated circuit;

a plurality of power islands of the integrated circuit having associated power consumptions, each of the power consumptions adapted to be independently controlled; and

a *power manager* to control the power consumptions;

at least one of the power islands adapted to have the *power manager* control its associated power consumption by a) the at least one of the power islands being configured to have one of plural threshold voltages of variable threshold transistors selected, and b) the system being configured to perform, during operation, an action on the at least one of the power islands, the action including changing a frequency of operation or changing a supply voltage.

Thus, as Plaintiff has argued:

It is . . . not enough that the only embodiments, or all of the embodiments, contain a particular limitation. We do not read limitations from the specification into claims; we do not redefine words. Only the patentee can do that. To constitute disclaimer, there must be a clear and unmistakable disclaimer.

*Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1366-67; *see also Phillips*, 415 F.3d at 1323.

On balance, the patentee discussed particular features that a "power manager" could have, such as the "power manager 120" illustrated in Figure 1, but the patentee did *not* set forth that disclosure as a disclaimer or a clear lexicography. *See Thorner*, 669 F.3d at 1365 ("To act as its own lexicographer, a patentee must 'clearly set forth a definition of the disputed claim term' other than its plain and ordinary meaning.") (quoting *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002)).

The Court therefore hereby construes **"power manager"** to mean **"any system, circuitry, or device configured to control power."**

**C. "power consumption signals indicating one or more of the power consumptions"**

| **Plaintiff's Proposed Construction** | **Defendant's Proposed Construction** |
|---|---|
| No construction is necessary because the term is clear in the context of the claim language. | "A power consumption signal will indicate the power consumption level associated with a particular power island." |

*Freescale* found no construction necessary and stated as follows, in full, as to this disputed term:

> Plaintiffs contend that no construction is necessary, because the term is clear in the context of the claim language.
>
> Defendants propose: "a signal containing information from which the power consumed by a particular power island can be determined." Defendants contend that there is an unstated dispute as to whether the term requires power consumption to be indicated for a particular power island, or for an entire chip. Defendants believe their proposal follows from the claim language itself, but want to have conformation of their reading of the claim expressed in a construction.
>
> Defendants are correct in their reading of the claim language. Further, Plaintiffs do not appear to dispute that power consumption is in regard to a particular power island. Claim 8 recites a plurality of power islands having associated power consumptions. Thus, a power consumption signal will indicate the power

> consumption associated with a particular power island. However, Defendants' construction is overly limiting in requiring that the signal contain information from which power consumed can be determined.
>
> The court concludes that no construction of this term is necessary.

*Freescale Order* at 47-48.

(1) The Parties' Positions

Plaintiff argues that "Defendant's proposed construction would not assist the jury's understanding; to the contrary, it essentially rearranges the wording to make it more confusing." Open. Br. at 21.

Defendant responds that its proposal adopts the description of this term in *Freescale* and "clarifies for the jury that the power consumption signals are associated with particular power islands." Resp. Br. at 21. "Without the benefit of [Defendant's] construction," Defendant argues, "the jury may mistakenly believe that this limitation could be met by a single power consumption signal for the entire chip or some other region of the IC that is not a power island." *Id.* at 22.

Plaintiff replies that "Defendant's construction copies a statement from Judge Giblin's Order, while missing the point that Judge Giblin found the term does not require construction." Reply Br. at 10.

(2) Analysis

Claims 1 and 8 of the '885 Patent recite (emphasis added):

> 1. An integrated circuit comprising:
> an integrated circuit chip;
> *a plurality of power islands* disposed on the integrated circuit chip *having associated power consumptions*, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;
> one or more *power consumption signals indicating one or more of the power consumptions*;

> a power management processor disposed on the integrated circuit chip and coupled to each of the power islands configured to monitor the one or more power consumption signals, the power management processor being dedicated to execute power management software to individually control each of the power consumptions, and the power management processor being configured to change power consumption in at least one of the power islands in response to a power consumption change request.
>
> * * *
>
> 8. An integrated circuit comprising:
>
> an integrated circuit chip;
>
> *a plurality of power islands* disposed on the integrated circuit chip *having associated power consumptions*, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;
>
> one or more *power consumption signals indicating one or more of the power consumptions*;
>
> a power manager disposed on the integrated circuit chip and coupled to each of the power islands configured to monitor the one or more power consumption signals, the power manager being configured to individually control each of the power consumptions, and the power manager being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

On balance, Defendant's proposed construction would tend to confuse rather than clarify the scope of the claims, particularly as to Defendant's proposal of referring to a "power consumption level." Defendant's proposed construction is therefore hereby expressly rejected.

Nonetheless, the Court adopts the finding in *Freescale* that each power consumption signal indicates power consumption associated with a particular power island rather than, for example, multiple power islands or an entire chip. *See Freescale Order* at 47-48.

The Court accordingly hereby construes **"power consumption signals indicating one or more of the power consumptions"** to have its **plain meaning**. The Court further hereby directs that at trial the parties cannot present any arguments inconsistent with the above-discussed finding in *Freescale* that a power consumption signal is associated with a particular power island rather than multiple power islands or an entire chip.

**D. "power manager to control the power consumptions"**

| **Plaintiff's Proposed Construction** | **Defendant's Proposed Construction** |
|---|---|
| "See '306 Patent, Claim 16. Per the context of the claim, the power manager controls the power consumptions associated with the integrated circuit of the claim." | "Circuitry, device, or system configured to determine a target power level of a power island, determine an action to change the target power level, and perform an action to change the consumption power level to the target power level." |

*Freescale* addressed this term together with the term "power manager," addressed above. *See Freescale Order* at 45-46.

(1) The Parties' Positions

Plaintiff argues:

> Claims 1 and 17 of the '811 Patent use "power manager" broadly, consistent with its use within the specifications, and then describe the power manager's function within the Claim. Thus, a broad construction of the term at issue is appropriate. Defendant's construction suffers from the same flaw as its proposed construction of "power manager" – it improperly imports a description of the "power manager" in one embodiment of the '306 Patent into claims that use broader language.

Open. Br. at 21.

Defendant responds that Plaintiff's proposal "is erroneous and confusing, because it would tie the power consumptions to the 'integrated circuit,' instead of the power islands, as is clear in the claims at issue." Resp. Br. at 22. Defendant further argues:

> The Court should give force to the patentee's explicit definition of "power manager" as Judge Giblin correctly did in the *Freescale* case, and reject [Plaintiff's] confused proposal cross-referencing the '306 patent and erroneously tying the power consumptions to the whole integrated circuit rather than to the individual power islands.

*Id.*

Plaintiff replies that "[i]dentical constructions" for this disputed term and for "power manager" "would render the language 'to control the power consumptions' superfluous, contrary

to rules of construction." Reply Br. at 10 (citing *Frans Nooren Afdichtingssystemen B.V. v. Stopaq Amcorr Inc.*, 744 F.3d 715, 722 (Fed. Cir. 2014) ("It is the usual (though not invariable) rule that, in patent claims as elsewhere, the construction of a clause as a whole requires construction of the parts, with meaning to be given to each part so as to avoid rendering any part superfluous.")). Further, Plaintiff argues, "injecting Defendant's construction of 'power manager' into this term creates unnecessary redundancy." *Id.*

(2) Analysis

Claims 1 and 17 of the '811 Patent recite (emphasis added):

1. A system comprising:
an integrated circuit;
a plurality of power islands of the integrated circuit having associated power consumptions, each of the power consumptions adapted to be independently controlled; and
a *power manager to control the power consumptions*;
at least one of the power islands adapted to have the power manager control its associated power consumption by a) the at least one of the power islands being configured to have one of plural threshold voltages of variable threshold transistors selected, and b) the system being configured to perform, during operation, an action on the at least one of the power islands, the action including changing a frequency of operation or changing a supply voltage.

* * *

17. A system comprising:
an integrated circuit;
a plurality of power islands of the integrated circuit having associated power consumptions, each of the power consumptions adapted to be independently controlled;
*a power manager to control the power consumptions*; and
an internal regulator, the system being configured to have a supply voltage provided by the internal regulator, and
at least one of the power islands adapted to have the power manager control its associated power consumption in that the system is configured to have:
a supply voltage to the at least one of the power islands changed, and
a frequency of operation of the at least one of the power islands changed.

On balance, this disputed term requires no construction apart from the constituent term "power manager," which is addressed above. In other words, the phrase "to control the power consumptions" does not alter the meaning of "power manager" but rather merely sets forth a relationship between the power manager and other limitations recited in the claims.

The Court therefore hereby construes **"power manager to control the power consumptions"** to have its **plain meaning** apart from the Court's construction of "power manager," above.

**E. "each of the power consumptions adapted to be independently controlled"**

| **Plaintiff's Proposed Construction** | **Defendant's Proposed Construction** |
|---|---|
| No construction is necessary. | No construction is necessary. |

Plaintiff previously proposed: "The power consumption of each of the power islands of the claim are each capable of being controlled free of the control exercised by other power islands." Joint Claim Construction and Prehearing Statement, Ex. A at 6.

In its opening brief, Plaintiff states: "Plaintiff initially sought construction of the term to clarify for the jury that each power island's power consumption can be controlled free of the control of other power islands. * * * However, upon further analysis, Plaintiff agrees with Defendant that the term is sufficiently clear such that construction is unnecessary." Open. Br. at 22. Defendant's response brief notes Plaintiff's agreement. Resp. Br. at 23. The parties' September 26, 2014 Joint Claim Construction Chart also notes the parties' agreement that no construction is necessary. Doc. No. 122-1 at 10. The Court therefore does not address this term.

## CONCLUSION

The Court hereby **ADOPTS** the above claim constructions for the patents-in-suit. For ease of reference, the Court's claim interpretations are set forth in a table in Appendix A.

So ORDERED and SIGNED this 9th day of January, 2015.

K. Nicole Mitchell

K. NICOLE MITCHELL
UNITED STATES MAGISTRATE JUDGE

**APPENDIX A**

| **Claim Term** | **Court's Construction** |
|---|---|
| "request controller" | plain meaning |
| "wherein the preassigned priority is dynamic" | "wherein the system is capable of changing the rules for prioritizing requests while the system is in operation" |
| "instruction data" | plain meaning |
| "may include self-modifying code" | "at least a portion of the program instructions include self-modifying code" |
| "first register having a plurality of interrupts each being programmed at one of a plurality of priority levels" | "a storage area divided into a series of memory fields, each corresponding to an interrupt and programmed to indicate one of multiple priority levels" |
| "second register in which a state is set for certain of said plurality of interrupts to be in a pending state" | "a storage area divided into a series of memory fields, each indicating whether the corresponding interrupt in the first register is pending" |
| "an arbitration circuit responsive to the data in said first and second registers" | "a circuit that operates based on the programmed priority levels of the first register and the settings in the second register for pending interrupt requests" |
| "register" | plain meaning |
| "power island" | "a section of an integrated circuit where power consumption is controlled by independently varying its operating voltage or its frequency of operation (or both)" |
| "power manager" | "any system, circuitry, or device configured to control power" |
| "power consumption signals indicating one or more of the power consumptions" | plain meaning |
| "power manager to control the power consumptions" | plain meaning |