

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Barry A. Hoberman, *et al.*
U.S. Patent No.: 8,854,077 Attorney Docket No.: 44508-0023IP3
Issue Date: October 7, 2014
Appl. Serial No.: 13/569,613
Filing Date: August 8, 2012
Title: LOW LEAKAGE AND DATA RETENTION CIRCUITRY

DECLARATION OF PAUL MIN, Ph.D.

I, Paul Min, Ph.D., of St. Louis, Missouri, declare that:

I. ASSIGNMENT

1. I have been retained as a technical expert by counsel on behalf of MediaTek Inc. and MediaTek USA Inc. (collectively “Petitioner” or “MediaTek”). I understand that MediaTek is requesting that the Patent Trial and Appeal Board (“PTAB” or “Board”) institute *Inter Partes* Review (“IPR”) of U.S. Patent No. 8,854,077 (“the ’077 Patent”) (MTK-1001).

2. I have been asked to provide my independent analysis of the ’077 Patent in light of the prior art cited below.

3. I am not currently an employee of MediaTek. I received no compensation for this declaration beyond my normal hourly compensation based on my time actually spent preparing these opinions and analyzing the ’077 Patent, the prior art cited below, and the issues related thereto, and I will not receive any added compensation based on the outcome of any IPR or other proceeding involving the ’077 Patent.

II. QUALIFICATIONS

4. A summary of my background and qualifications as a technical expert for this case is provided below. A complete listing of my qualifications and background are detailed in my curriculum vitae (“CV”), which is attached hereto as Appendix A. Among other things, my CV includes a list of my issued patents and publications. My curriculum vitae also includes information about my expert witness experience, with case numbers where available.

5. I received a B.S. degree in Electrical Engineering in 1982, an M.S. degree in Electrical Engineering in 1984, and a Ph.D. degree in Electrical Engineering in 1987 from the University of Michigan in Ann Arbor. I received several academic honors, including my B.S. degree with honors, a best graduate student award and a best teaching assistant award during my M.S. study, and a best paper award from a major international conference for reporting results from my Ph.D. thesis.

6. After receiving my Ph.D., I worked at Bellcore in New Jersey from August 1987 until August 1990. At Bellcore, I was a member of the team responsible for evolving the public switched telephone network (PSTN) into a multi-services voice and data network that incorporated packet switches, optical technologies, and wireless technologies.

7. In September 1990, I joined the faculty at Washington University in St. Louis. In July 1996, I was promoted to an Associate Professor of Electrical Engineering with tenure. I am currently a Senior Professor of Electrical and

Systems Engineering at Washington University in St. Louis. I have served as the Chair of the Graduate Curriculum (2000-2002) and the Chair of the Undergraduate Curriculum (2011-2014) for the Electrical and Systems Engineering department.

8. At Washington University, I have conducted research in communication, computing, and related electronic hardware and software. I have received several grants from the U.S. Federal Agencies, including the National Science Foundation and the Defense Advanced Research Project Agency, the Air Force Office of Scientific Research, and numerous contracts from companies and organizations around the world.

9. As a faculty member at Washington University, I taught a number of courses in electronics, communication, and computing at both the undergraduate and graduate levels. For example, I have taught courses including electronic circuits, communication theory, data networks, transmission and multiplexing, and signaling and control of communication networks. I have supervised numerous graduate students, many of whom received a doctoral degree under my guidance.

10. In addition to my responsibilities as a university faculty member, I founded two companies. In May 1997, I founded MinMax Technologies, Inc., a fabless semiconductor company that developed switch fabric integrated circuit chips for the Internet. In March 1999, I founded Erlang Technology, Inc., a fabless semiconductor company that focused on the design and development of

integrated circuit chips and software for the Internet. One of Erlang's products received a best product of the year award in 2004 from a major trade journal for the electronics industry. In these companies, I have designed a number of circuits and software applications for the Internet and wireless communication networks. Specifically related to the technology at issue in the '077 patent, many of the integrated circuit chips my companies developed were notoriously power-hungry (as many specialized communication chips do), requiring us to incorporate various power control mechanisms to assure the proper functioning of these chips.

11. Outside my own start-up companies, I have also served in various technology and business advisor roles for other companies and organizations around the world. I was the main technical author for one of two winning proposals to the Korean government for CDMA wireless service licenses (1996). I was responsible for designing a commercial scale IS-95 CDMA cellular network, which I understand to be one of the earliest such networks deployed in the world. I worked with numerous engineers and scientists around the world to implement this commercial-scale cellular network before IS-95 CDMA was widely accepted and deployed. This provided me with extensive insight into various components of CDMA technology, which extensively use various transmission and switching technologies. I have also been involved in a semiconductor company that specializes in semiconductor memories such as flash EEPROMs as a board member and as a technical advisor (2007-2011).

12. I am a member of and have been actively involved in a number of professional organizations. For example, I have served as the Chair of the Saint Louis Section of the IEEE with more than 3,000 members (2014), and a member of the Eta Kappa Nu Honor Society for electrical engineers. I have also been an Ambassador of the McDonnell International Scholars Academy (2007-2013).

13. I am a named inventor on eleven U.S. patents. I have extensively published technical papers in international conferences and journals, technical memoranda and reports, and given a number of seminars and invited talks. I have organized several international conferences and served as an international journal editor.

14. I have also served as an expert in certain legal proceedings. A list of cases in which I have testified at trial, hearing, or by deposition is provided in my curriculum vitae (Appendix A). Over the past several years, I have been retained by patent owners as well as patent challengers in various IPR proceedings.

III. LEGAL PRINCIPLES

15. In forming my analysis and conclusions expressed in this declaration, I have applied the legal principles described in the following paragraphs, which were provided to me by counsel for the Petitioner.

A. Anticipation

16. It is my understanding that invalidation by “anticipation” exists only if a single alleged prior art reference discloses each and every limitation of the claim at issue, either expressly or inherently. In other words, every limitation of

the claim must appear in a single prior art reference for the reference to anticipate that claim. I also understand that all elements of the claim must be disclosed in the reference as they are arranged in the claim. I also understand that to be considered anticipatory, the prior art reference must be enabling and must describe the patentee's claimed invention sufficiently to have placed it in the possession of a person of ordinary skill in the field of invention. Under the principles of inherency, I understand that if the prior art necessarily functions in accordance with or includes the claimed limitations, it anticipates.

17. I have been informed that a claim is invalid if the claimed invention was known or used by others in the U.S., or was patented or published anywhere, before the Applicant's invention. I further have been informed that a claim is invalid if the invention was patented or published anywhere, or was in public use, on sale, or offered for sale in this country, more than one year prior to the filing date of the patent application (critical date). I have also been informed that a claim is invalid if an invention described by that claim was described in a U.S. patent granted on an application for a patent (or in a published application for a U.S. patent) that was filed by another in the U.S. before the date of invention for such a claim.

18. I understand that a dependent claim contains all of the limitations of the independent claim from which it depends. Thus, to establish anticipation, every limitation set forth in a dependent claim as well as the independent claim from which it depends must be found in an anticipatory reference.

B. Obviousness

19. I have been informed that a patent claim is invalid as “obvious” in light of one or more prior art references if it would have been obvious to a person of ordinary skill in the art at the time of the alleged invention (“POSITA”), taking into account (1) the scope and content of the prior art, (2) the differences between the prior art and the claims, (3) the level of ordinary skill in the art, and (4) any so called “secondary considerations” of non-obviousness, which include: (i) “long felt need” for the claimed invention, (ii) commercial success attributable to the claimed invention, (iii) unexpected results of the claimed invention, and (iv) “copying” of the claimed invention by others. I understand that a patent cannot be properly granted for subject matter that would have been obvious to a POSITA at the time of the alleged invention, and that a patent claim directed to such obvious subject matter is invalid under 35 U.S.C. § 103. It is also my current understanding that in assessing the obviousness of claimed subject matter one should evaluate obviousness over the prior art from the perspective of a POSITA at the time the invention was made (and not from the perspective of either a layman or a genius in that art).

20. While I do not know the exact date that the alleged invention claimed in the '077 Patent was made, I do know that the '077 Patent was filed on August 8, 2012 and claims priority through a series of continuations to an earliest provisional application filed on February 19, 2004. MTK-1001, Cover Page. I also understand that Patent Owner MOSAID Technologies Inc. (“Patent Owner”

or “MOSAID”) asserts that the ’077 Patent claims are entitled to an invention date at least as early as December 11, 2003. MTK-1021. For purposes of my analysis here, I have applied a date of December 11, 2003 as the date of the alleged invention in my obviousness analysis, although in many cases the same analysis would hold true even if the date of the alleged invention occurred earlier or later than December 11, 2003, especially given the earlier publication or filing dates of the cited prior art references.

21. I have been informed that a claim can be obvious in light of a single prior art reference or multiple prior art references. To be obvious in light of a single prior art reference or multiple prior art references, there must be a reason that would have prompted a POSITA to modify the single prior art reference, or combine two or more references, in a manner that provides the elements of the claimed invention. This reason may come from a teaching, suggestion, or motivation to combine, or may come from the reference(s) themselves, the knowledge or “common sense” of a POSITA, or from the nature of the problem to be solved, and this reason may be explicit or implicit from the prior art as a whole. I have been informed that, under the law, the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand it is improper to rely on hindsight in making the obviousness determination.

C. Claim Construction

22. I understand that, for purposes of my analysis in this IPR proceeding, the terms appearing in the patent claims should be interpreted according to their “ordinary and customary meaning.” In determining the ordinary and customary meaning, the words of a claim are first given their plain meaning that those words would have had to a POSITA. I understand that the structure of the claims, the specification, and the file history also may be used to better construe a claim insofar as the plain meaning of the claims cannot be understood. Moreover, treatises and dictionaries may be used, albeit under limited circumstances, to determine the meaning attributed by a person of ordinary skill in the art to a claim term at the time of filing. I have followed this approach in my analysis, and for all of the claim terms considered in this declaration, I have applied the plain and ordinary meaning of those terms.

23. I also understand that the words of the claims should be interpreted as they would have been interpreted by a POSITA at the time the alleged invention was made (not today). Because I do not know at what date the alleged invention was made, I have used the date of December 11, 2003 for the reasons explained in Paragraph 20 above. However, the plain meanings/interpretations that I employed in my analysis below would have also been correct if the date of invention was anywhere within the late 1990s to early 2000s.

IV. PERSON OF ORDINARY SKILL IN THE ART

24. Based on my knowledge and experience in the field and my review of the '077 Patent and its file history, and my first-hand knowledge of undergraduate electrical engineering curricula at the time of the '077 Patent's alleged priority date of December 2003, I believe a person of ordinary skill in the art ("POSITA") at the time of the earliest possible priority date of the '077 Patent would have had at least a bachelor of science degree in electrical engineering, computer engineering, computer science, or a related field, and at least two years of experience in the research, design, development, or testing of electronic circuits or components, or software for controlling electronic circuits or components, or the equivalent, with additional education substituting for experience and vice versa. I understand that a person of ordinary skill in the art is not a specific, real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

V. MATERIALS CONSIDERED

25. My analyses set forth in this declaration are based on my experience in the field of high performance circuit design, in particular, power management of such circuitries. Based on my above-described experience in the field, I believe that I am considered to be an expert in the field. Also, based on my experience, I understand and know of the capabilities of persons of ordinary skill in this field during the late 1990s to early 2000s and specifically during the time before the earliest possible priority date for the '077 Patent (December 11, 2003).

For example, I taught classes as part of the Electrical Engineering curricula, personally designed and implemented a number of circuitries that required active power management, and worked closely with many persons of such skill level in the field during that time frame.

26. As part of my independent analysis for this declaration, I have considered the following: the background knowledge/technologies that were commonly known to persons of ordinary skill in this field during the time before the earlier possible priority date for the '077 Patent; my own knowledge and experiences gained from my work experience in the field of high performance circuit design generally; my experience in teaching and advising others in such subjects; and my experience in working with others involved in the field of high performance circuit design or similar fields. In addition, I have analyzed the following publications and materials:

- U.S. Patent No. 8,854,077 to Hoberman, *et al.* (“the '077 Patent”) (MTK-1001) and its accompanying Prosecution History (MTK-1002);
- U.S. Patent Publication No. 2003/0025130 to Takahashi, *et al.* (“Takahashi”) (MTK-1004);
- U.S. Patent Publication No. 2003/0102904 to Mizuno, *et al.* (“Mizuno”) (MTK-1005);
- U.S. Patent No. 7,091,766 to Ko, *et al.* (“Ko”) (MTK-1006);
- U.S. Patent No. 5,440,520 to Schutz, *et al.* (“Schutz”) (MTK-1007);

- Alan C. Dixon, *et al.*, *A Practical Approach to Digital Electronics*, 2000 (MTK-1008);
- John D. Carpinelli, *Computer Systems Organization and Architecture*, 2001 (MTK-1009);
- U.S. Patent No. 6,141,762 to Nicol, *et al.* (“Nicol”) (MTK-1010);
- U.S. Patent No. 6,087,813 to Tobita (“Tobita”) (MTK-1011);
- U.S. Patent No. 6,809,538 to Borkar (“Borkar”) (MTK-1012);
- U.S. Patent No. 6,518,826 to Zhang (“Zhang”) (MTK-1013);
- U.S. Patent No. 7,042,274 to Hazucha, *et al.* (“Hazucha”) (MTK-1014);
- Modern Dictionary of Electronics, Seventh Edition, 1999 (MTK-1015);
- Dictionary of Science and Technology, 2003 (MTK-1016);
- Adel S. Sedra, *et al.*, *Microelectronic Circuits*, 1998 (“Sedra”) (MTK-1017);
- U.S. Patent No. 6,791,361 to Alon, *et al.* (“Alon”) (MTK-1018);
- Excerpts from MOSAID Technologies Inc.’s Disclosure of Asserted Claims and Infringement Contentions in Case No. 2:23-CV-00129, Dated July 6, 2023 (MTK-1021)
- The Declaration of June A. Munford (MTK-1024)
- Claim Construction Order in Mosaid Technologies Inc. v. Freescale Semiconductor, Inc., Case No. 6:11-cv-00173 (E.D. Tex. April 29, 2013) (MTK-1025)

- Claim Construction Order in Conversant Intellectual Property Management Inc., et al. v. Xilinx, Inc., Case No. 6:12-cv-00847 (E.D. Tex. January 9, 2015) (MTK-1026)

27. Although for the sake of brevity this Declaration refers to selected portions of the cited references, it should be understood that one of ordinary skill in the art would have viewed the references cited herein in their entirety, and in combination with other references cited herein or cited within the references themselves. The references used in this Declaration, therefore, should be viewed as being incorporated herein in their entirety.

VI. BACKGROUND INFORMATION

A. Background of the Technology

28. In order to aid the understanding of the opinions I provide in the declaration, I now provide a brief background of the technology at issue. In doing so, I will refer to a popular undergraduate textbook entitled “Microelectronic Circuits,” Fourth Edition by Adel S. Sedra and Kenneth C. Smith 1998 (“Sedra”) (MTK-1017). Personally, I have taught an undergraduate course at Washington University in St. Louis referred to as ESE 232 Introduction to Electronic Circuits using various editions of Sedra as the main textbook. In what follows, I will quote various excerpts from the fourth edition of Sedra, which is the latest edition of Sedra prior to the asserted time of the invention for the ’077 Patent (*i.e.*, the 2003 time frame). Other materials are also cited below to provide an appropriate background of the technology.

1. Power Consumption in Integrated Circuits

29. At around the asserted time of the invention for the '077 Patent, a vast majority of the Very Large Scale Integration (VLSI) circuits were based on the Complementary Metal-Oxide-Semiconductor (CMOS) technology. MTK-1017, 1-4 (“Since the early 1980s, CMOS (complementary MOS) technology has almost completely dominated the SLSI scene.”).

30. Appendix A of Sedra illustrates a high-level overview of the VLSI processes. *Id.*, A-4 to A-13. In particular, at the end of the placing various components of the VLSI circuits, certain areas of the circuitry can be grouped together as part of the layout process as shown in the figure below.

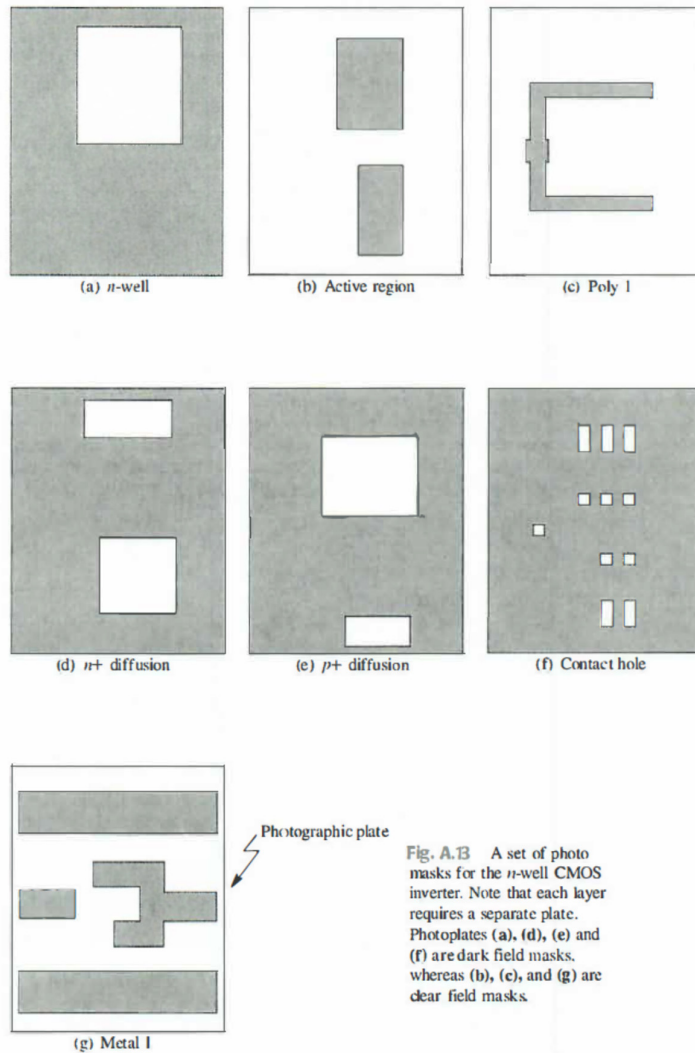


Fig. A-13 A set of photo masks for the n -well CMOS inverter. Note that each layer requires a separate plate. Photoplates (a), (d), (e) and (f) are dark field masks, whereas (b), (c), and (g) are clear field masks.

MTK-1017, FIG. A-13.

31. Particular portions of the VLSI area are noted as the active region (FIG. A-13(b) above), where the active components (such as the transistors and diodes) are placed to implement the functions designed to be performed by the VLSI circuitry. As shown in the figure, there are multiple, distinct and separate active regions in a circuitry. For example, if the circuitry were a central processing unit (CPU), one active region may correspond to the Arithmetic Logic Unit (ALU), another active region may be a Static Random Access Memory

(SRAM), yet another may be an interface module, and so on. While these active regions together implement the overall required functions of the CPU, by in large, they operate independently with different levels of requirements such as the clock speed and power consumption level.

32. In the context of the '077 Patent, “[a] power island is any section, delineation, partition, or division of an integrated circuit where power consumption is controlled within the section, delineation, partition, or division. In some embodiments, the power islands are delineated based on geographic factors of the integrated circuit. In some embodiments, the power islands are delineated based on functional IP units of the integrated circuit 200.” MTK-1001, 3:65-4:5.

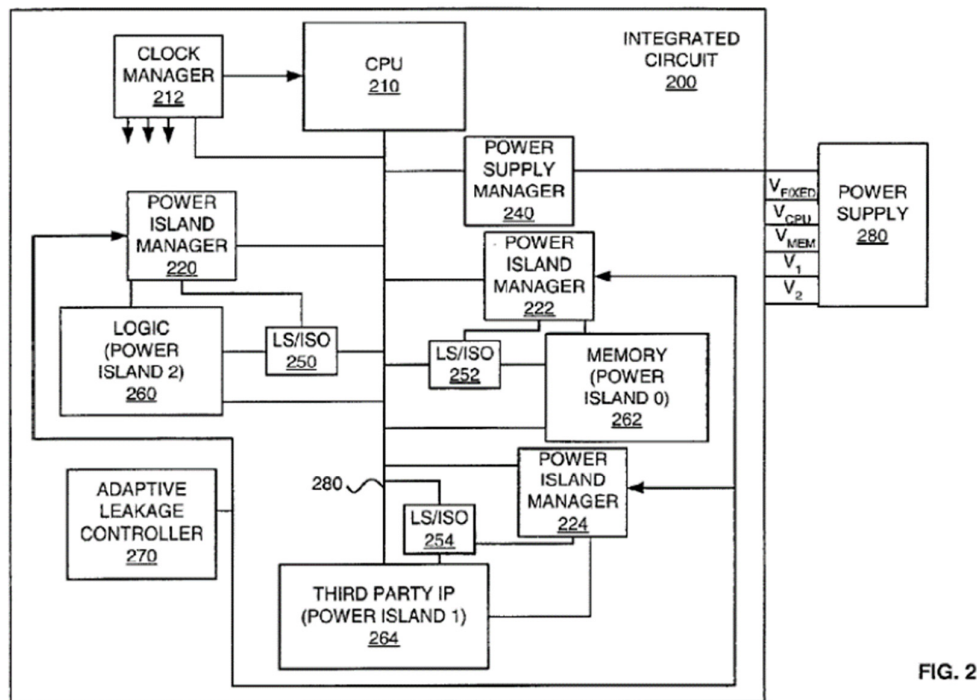


FIG. 2

MTK-1001, FIG. 2.

33. In comparison, power islands 260, 262, and 264 of FIG. 2 of the '077 Patent may belong to various active regions in FIG. A-13 of Sedra. The '077 Patent states that “[t]he power island managers 220, 222, and 224 are any circuitry, device, or system configured to provide control signals to a power island to control power within the power island, the power island managers 220, 222, and 224 can dynamically change the power consumption of the power islands based on the needs and operation of the integrated circuit 200. The power island managers 220, 222, 224 may select a clock, change clock frequency, or modify the voltage within the power island to control the power consumption of the power island.” MTK-1001, 4:11-20.

34. Many Application Specific Integrated Circuits (ASIC) have extremely high levels of complexity and performance requirements. For example, switch fabric chips I personally designed over the past 30+ years required a very number of input/output pins (in excess of one thousand), a high power consumption level (tens of watts), and a very high clock frequency (multiple gigabits per second). In addition, the resulting chip designs required a large surface dimension (multiple square inches), comprising many distinct active regions. For these types of chips, it is necessary to manage the power consumption tightly, optimizing the power consumption levels separately for each different active region.

35. The following figure from Sedra shows a high-level construct of the basic structure of a CMOS logic gate, which is the main building block of the VLSI circuitry designs.

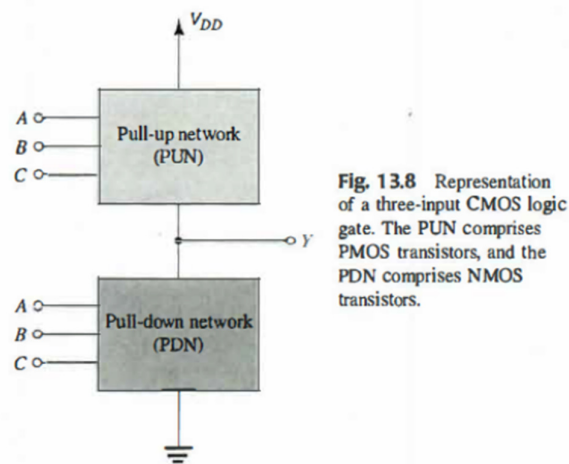


Fig. 13.8 Representation of a three-input CMOS logic gate. The PUN comprises PMOS transistors, and the PDN comprises NMOS transistors.

MTK-1017, 1059.

36. Sedra states that “[a] CMOS logic circuit is in effect an extension, or a generalization, of the CMOS inverter: The inverter consists of an NMOS pull-down transistor, and a PMOS pull-up transistor, operated by the input voltage in a complementary fashion. The CMOS logic gate consists of two networks: the pull-down network (PDN) constructed of NMOS transistors, and the pull-up network (PUN) constructed of PMOS transistors (see Fig. 13.8).”

MTK-1017, 1058.

37. Sedra further states that “for the three-input gate represented in Fig. 13.8, the PDN will conduct for all input combinations that require a low output ($Y = 0$) and will then pull the output node down to ground, causing a zero voltage to appear at the output, $v_y = 0$. Simultaneously, the PUN will be off, and no direct

dc path will exist between V_{DD} and ground. On the other hand, all input combinations that call for a high output ($Y = 1$) will cause the PUN to conduct, and the PUN will then pull the output node up to V_{DD} , establishing an output voltage $v_y = V_{DD}$. Simultaneously, the PDN will be cut off, and again, no dc current path between V_{DD} and ground will exist in the circuit.” MTK-1017, 1058-1059. In other words, at both at the low output state, *i.e.*, $Y = 0$ and the high output state $Y = 1$, either the PUN or the PDN is turned off and there is no dc path between V_{DD} and ground exists in the circuit. As both the PDN and the PUN must conduct at the same time for the current to flow, there is no dc current flowing between V_{DD} and ground at both at the low output state, *i.e.*, $Y = 0$ and the high output state $Y = 1$.

38. The following is a figure from Sedra showing the voltage transfer characteristics of a CMOS inverter.

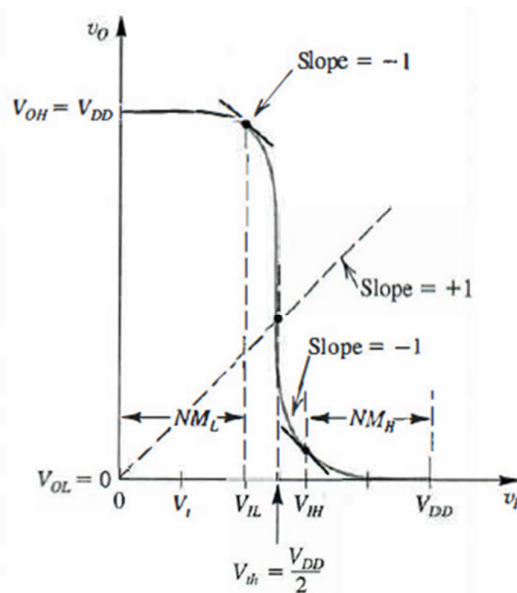


Fig. 13.5 The voltage transfer characteristic (VTC) of the CMOS inverter when Q_N and Q_P are matched.

MTK-1017, 1051.

39. The PMOS transistor (noted as Q_P in the figure above) corresponds to the PDN in FIG. 13.8 of Sedra and the NMOS transistor (noted as Q_N in the figure above) corresponds to the PUN in FIG. 13.8 of Sedra. v_O in the figure above corresponds to Y in FIG. 13.8 of Sedra. In this way, V_{OH} (output high) corresponds to $Y = 1$ and V_{OL} corresponds to $Y = 0$. As explained above, at $Y = 1$ and $Y = 0$, there is no current path through the PUN and the PDN. In order for the current to pass through the PUN and the PDN, both the PUN and the PDN must be on at the same time, which happens during the transition period from/to $Y = 1$ to/from $Y = 0$. The transition period corresponds to the portion of the graph shown in the above figure when $v_I = V_{OL}$ and $v_I = V_{OL}$ along the horizontal axis when v_O transitions from/to V_{OH} to/from V_{OL} along the vertical axis. In digital design, this transition period is referred to as the switching time.

40. Since the CMOS gates only consume power during the transition period, the power consumed by the CMOS gates are mostly dynamic in nature. MTK-1017, 1056 (“The negligible static power dissipation of CMOS has been a significant factor in motivating its replacing NMOS as the technology of choice in implementing high-density VLSI circuits.”).

41. Sedra explains that “[t]he dynamic power dissipated in the CMOS inverter is given by Eq. (13.4), which we repeat here as $P_D = fCV_{DD}^2$ (13.20) where f is the frequency at which the gate is switched.” MTK-1017, 1056. Setting aside the various capacitance, C , associated with the CMOS gate, the power consumed by a CMOS gate is proportional to the switching frequency f

and to the square of the supplied voltage V_{DD} . Since digital circuits including the CMOS gates are clocked, the switching frequency f is related to the clocking frequency of the circuit. This is the reason why the management of the power is performed by changing the clock frequency and/or the supplied power level.

2. Leakage Currents in Integrated Circuits

42. The '077 Patent states that “[m]ost integrated circuits have a design goal to reduce the overall power consumption. The total power consumed by an integrated circuit includes dynamic power consumption and standby leakage current consumption. The challenge in designing an integrated circuit is to reduce the dynamic power and leakage power, while maintaining performance and cost goals for the integrated circuit. In complementary metal oxide semiconductors (CMOS), various types of leakage occur such as pn junction reverse-bias current, subthreshold leakage, oxide tunneling current, gate current due to hot-carrier injection, gate-induced drain leakage, and channel punch through current. When the threshold voltage for a CMOS transistor is reduced for higher performance, the leakage power is significant in the total power consumption of the CMOS circuit.” MTK-1001, 1:33-47. This excerpt from the '077 Patent explains that in addition to the current necessary for the CMOS circuits to operate during the transition period, *i.e.*, the dynamic current, there is an additional type of current, *i.e.*, the leakage currents, which are generated by the non-ideal behavior of the CMOS circuits such as the “pn junction reverse-bias current, subthreshold

leakage, oxide tunneling current, gate current due to hot-carrier injection, gate-induced drain leakage, and channel punch through current.” *Id.*

43. To explain these non-ideal behaviors of the CMOS circuits, I again refer to Sedra. Sedra states that “[o]ur study of the physical operation of the pn junction and of the basic concepts of semiconductor physics is intended to provide a foundation for understanding not only the characteristics of junction diodes but also those of the bipolar junction transistor, studied in the next chapter, and field-effect transistors, studied in Chapter 5.” MTK-1017, 123.

44. To explain how the diodes work, Sedra first introduces an ideal model for the diodes. Sedra states that “[t]he ideal diode may be considered the most fundamental nonlinear circuit element.” MTK-1017, 123.

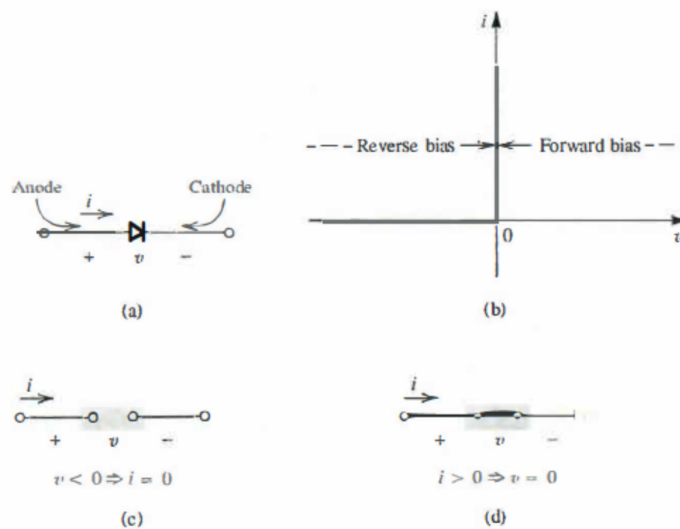


Fig. 3.1 The ideal diode: (a) diode circuit symbol; (b) i - v characteristic; (c) equivalent circuit in the reverse direction; (d) equivalent circuit in the forward direction.

MTK-1017, FIG. 3.1.

45. In describing FIG. 3.1 above, Sedra states that “[t]he terminal characteristic of the ideal diode can be interpreted as follows: If a negative voltage [relative to the reference direction indicated in FIG. 3.1 (a)] is applied to the diode, no current flows and the diode behaves as an open circuit [FIG. 3.1(c)]. Diodes operated in this mode are said to be reverse-biased, or operated in the reverse direction. An ideal diode has zero current when operated in the reverse direction and is said to be cut off. On the other hand, if a positive current [relative to the reference direction indicated in FIG. 3.J(a)] is applied to the ideal diode, zero voltage drop appears across the diode. In other words, the ideal diode behaves as a short circuit in the forward direction [FIG. 3.J (d)]; it passes any current with zero voltage drop. A forward-conducting diode is said to be turned on, or simply, on.” MTK-1017, 124.

46. The excerpt from Sedra above is saying that the ideal diode has two distinct states of operation: (1) The cut-off state where there is no current flowing across the diode and (2) the turned-on state where the diode conducts in forward direction (*i.e.*, from the positive terminal, anode, to the negative terminal, cathode).

47. In practice, however, ideal diodes do not exist. Sedra states that “[i]n this section we study the characteristics of real diodes – specifically, semiconductor junction diodes made of silicon.” MTK-1017, 131.

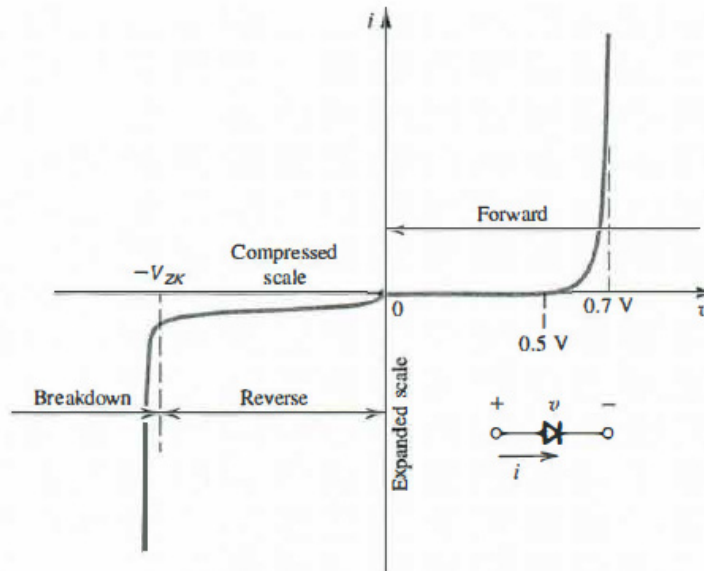


Fig. 3.8 The diode i - v relationship with some scales expanded and others compressed in order to reveal details.

MTK-1017, FIG. 3.8.

48. With regard to the figure above, Sedra explains:

As indicated, the characteristic curve consists of three distinct regions:

1. The forward-bias region, determined by $v > 0$ [,]
2. The reverse-bias region, determined by $v < 0$ [,]
3. The breakdown region, determined by $v < -V_{ZK}$.

MTK-1017, 132.

49. In comparison to the characteristics of the ideal diodes shown in FIG. 3.1 of Sedra, FIG. 3.8 above, which describes the characteristics of the “real diode,” shows non-zero current flowing in the region $v < 0$, which was referred to as the “cut-off” for the ideal diode where no current was flowing. This

phenomenon is what the '077 described as the “pn junction reverse-bias current,” a significant type of the leakage current. MTK-1001, 1:40-44.

50. Sedra explains that “[t]he reverse-bias region of operation is entered when the diode voltage v is made negative” and that “real diodes exhibit reverse currents that, though quite small, are much larger than I_S . For instance, a small-signal diode whose I_S is of the order of 10^{-14} to 10^{-15} A could show a reverse current of the order of 1 nA” (*i.e.*, 10^{-9} A, up to a million times larger than I_S). MTK-1017, 136. Sedra further explains that “[a] good part of the reverse current is due to leakage effects. These leakage currents are proportional to the junction area, just as I_S is. Their dependence on temperature, however, is different from that of I_S .” *Id.*, 136.

51. To be sure, there are types of leakage current such as the “subthreshold leakage, oxide tunneling current, gate current due to hot-carrier injection, gate-induced drain leakage, and channel punch through current,” as described by the '077 Patent. MTK-1001, 1:40-44. These types of leakage current are all related to the non-ideal characteristics of the semiconductors, *e.g.*, transistors and diodes, and correspond to the undesired occurrences of current flow.

52. For example, the on/off characteristic of the ideal diode at $v = 0$ shown in Fig. 3.1 of Sedra above is to be contrasted with the on/off characteristic of the realistic diode shown in Fig. 3.8. For the realistic diode, the current through the diode is non-zero between $v = 0.5V$ and $v = 0.7V$. That is to say that the

realistic diode conducts a certain amount of current, albeit small, below $v = 0.7V$, which is the threshold voltage for the realistic diode to turn on. This phenomenon is referred to as the subthreshold leakage, by which the CMOS circuits start consuming power before the PUN and the PDN change their respective logical states in earnest.

53. Yet another non-ideal characteristic of CMOS transistors is the oxide tunneling current described in the '077 Patent. In a CMOS transistor, the gate terminal is isolated from the substrate through oxide. Through repeated operation of the transistor (e.g., turning on and off numerous times in a typical lifetime of the transistor), the oxide that isolates the gate from the transistor substrate can erode and some small amount of current will flow through the oxide. This oxide tunneling current is another example of power consumption by the CMOS transistor due to leakage current.

3. Integrated Circuit Power Islands

54. As described above, the '077 Patent states “[a] power island is any section, delineation, partition, or division of an integrated circuit where power consumption is controlled within the section, delineation, partition, or division. In some embodiments, the power islands are delineated based on geographic factors of the integrated circuit. In some embodiments, the power islands are delineated based on functional IP units of the integrated circuit 200.” MTK-1001, 3:65-4:5.

55. As I have also explained, during the VLSI design process, certain areas of the circuitry can be grouped together as part of the layout process as shown in Fig. A.13 of Sedra.

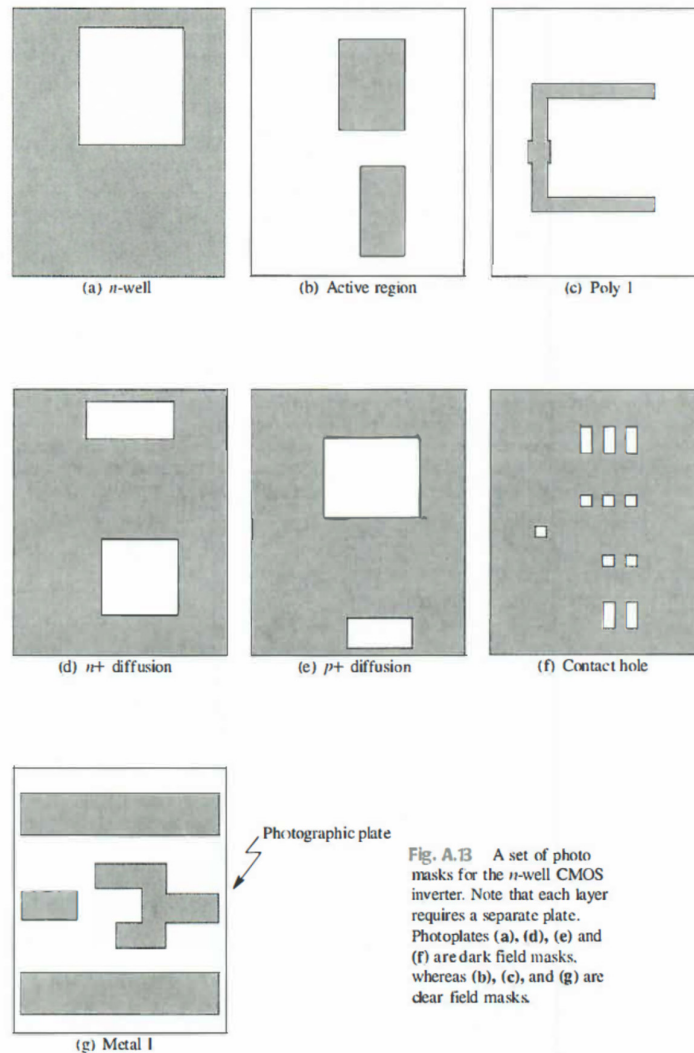


Fig. A.13 A set of photo masks for the n -well CMOS inverter. Note that each layer requires a separate plate. Photoplates (a), (d), (e) and (f) are dark field masks, whereas (b), (c), and (g) are clear field masks.

MTK-1017, FIG. A.13.

56. The figure above from Sedra shows separate active regions in a circuit, which may correspond, for example, to the “Memory (Power Island 0) 262,” “Third Party IP (Power Island 1) 264,” and “Logic (Power Island 2) 260,” in Figure 2 of the ’077 Patent shown below. While these active regions together

implement the overall required functions of the integrated circuit chip, by in large, they operate independently with different levels of requirements, such as different clock speeds and power consumption levels.

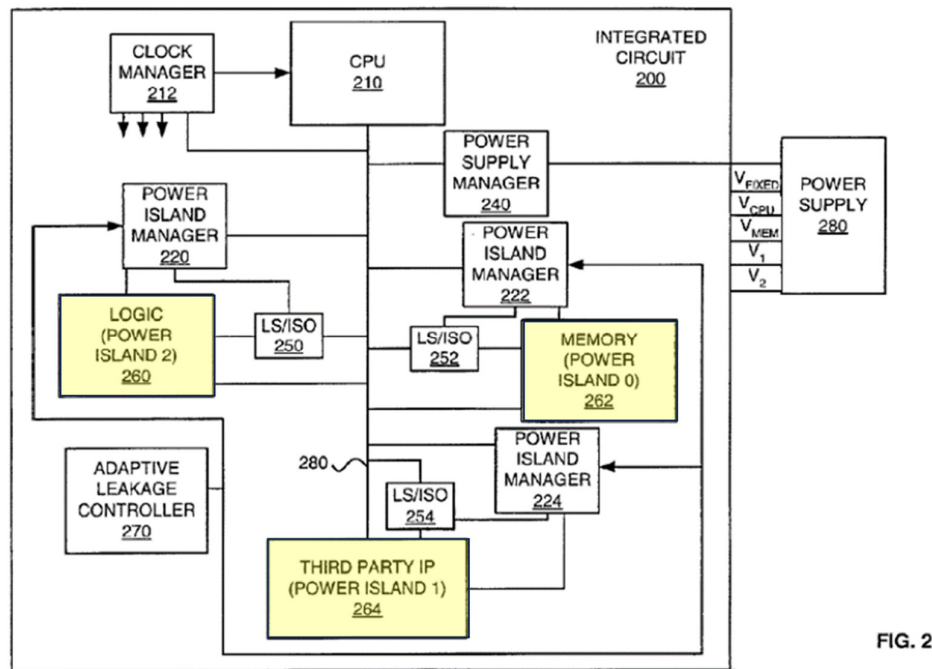


FIG. 2

MTK-1001, FIG. 2 (annotated).

57. As explained in the '077 Patent, “[t]he power island managers 220, 222, and 224 are any circuitry, device, or system configured to provide control signals to a power island to control power within the power island, the power island managers 220, 222, and 224 can dynamically change the power consumption of the power islands based on the needs and operation of the integrated circuit 200. The power island managers 220, 222, 224 may select a clock, change clock frequency, or modify the voltage within the power island to control the power consumption of the power island.” MTK-1001, 4:11-20.

4. Sleep Transistors and Standby Modes

58. The '077 Patent describes the operation of CMOS circuits as having a dynamic mode and a standby mode. MTK-1001, 1:33-39 (“Most integrated circuits have a design goal to reduce the overall power consumption. The total power consumed by an integrated circuit includes *dynamic power consumption and standby leakage current consumption*. The challenge in designing an integrated circuit is to reduce the dynamic power and leakage power, while maintaining performance and cost goals for the integrated circuit.”) (emphasis added).

59. As explained above, most of the power consumed by the CMOS circuits is attributed to the dynamic mode, *i.e.*, while the circuits change state from logic high to logic low or *vice versa* and consume what the '077 Patent refers to as “dynamic power consumption.” *Id.* As I have also explained, even when the circuits are not changing their states dynamically, the circuits still consume certain amounts of power, which the '077 Patent refers to as “standby leakage current consumption.” *Id.*

60. The '077 Patent states that “[a]nother technique for reducing leakage is a sleep transistor. FIG. 1 depicts prior art circuitry including a sleep transistor. For NMOS sleep transistors, one or more NMOS transistors are added to logic gates in series with the cell transistors to VSS. The NMOS sleep transistors act as a switch to turn on and off the logic gate.” MTK-1001, 2:9-14.

61. The following Figure 1 of the '077 Patent depicts a sleep transistor, with certain annotations added for illustration. As the '077 Patent acknowledges, sleep transistors such as these were well known in the art before the '077 Patent as a means of placing circuits into a standby or active modes.

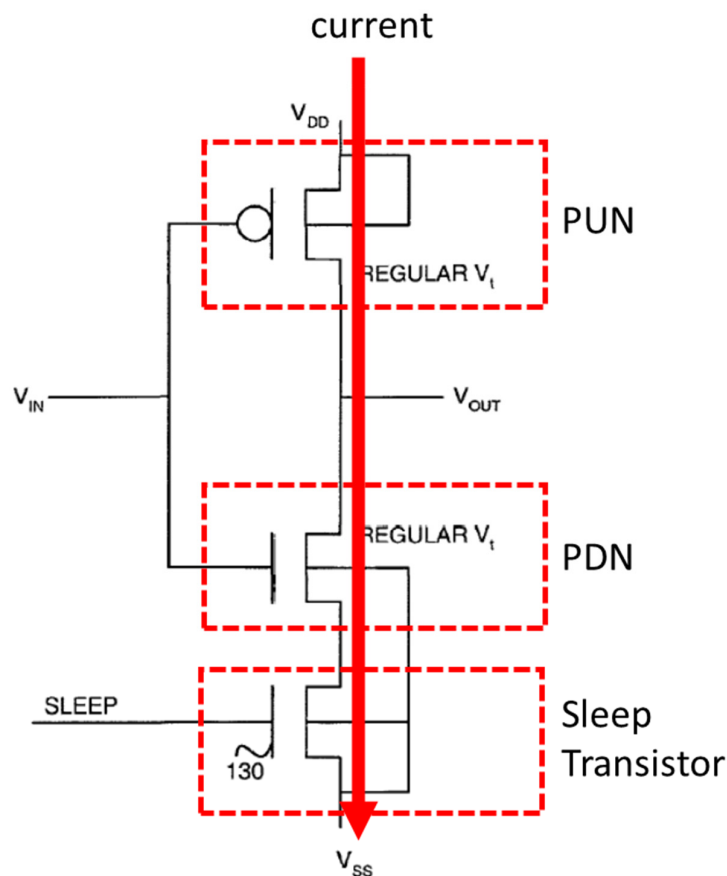


FIG. 1
PRIOR ART

MTK-1001, FIG. 1 (annotated).

62. In the figure above, the transistor shown at the top of the stack corresponds to the pull up network (PUN) and the transistor shown in the middle of the stack is the pull down network (PDN). The transistor shown at the bottom of the stack is the sleep transistor. As explained above, without the sleep

transistor in the stack, there is certain amount of the “standby leakage current consumption” when the PUN and the PUN are in the standby mode, *i.e.*, not switching their respective states from “high to low” or “low to high.” If the sleep transistor is added, however, it is possible to control the flow of current from top to bottom shown as shown in the annotated figure above, by switching off the path of the current by turning off the sleep transistor.

63. While sleep transistors add to the complexity of the circuit, when there are millions or billions of CMOS logic gates in the circuit, even a small amount of “standby leakage current consumption” by each gate can result in a large amount of total leakage current. The total leakage current can become a significant issue when controlling the power consumption is critical, for example, in mobile devices.

B. Overview of the '077 Patent

64. The '077 Patent is titled “Low Leakage and Data Retention Circuitry” and relates generally to reducing power consumption in integrated circuits. MTK-1001, Title, Abstract, 1:29-39.

65. As the '077 Patent explains, an integrated circuit’s total power consumption includes the power consumed while the integrated circuit is operating—referred to by the '077 Patent as “dynamic power consumption”—and the power consumed while the integrated circuit is not operating—referred to by the '077 Patent as “standby leakage current consumption.” MTK-1001, 1:34-36. As its name implies, the power consumed while the integrated circuit is

not operating is due to leakage current, which is the current flowing through the integrated circuit even while it is a standby state and not performing its designed function. MTK-1001, 1:40-47.

66. The '077 Patent acknowledges, and I agree, that methods of reducing leakage current were well-known prior to the '077 Patent. MTK-1001, 1:48-2:20; *see* Section VI.A. For example, the use of so-called sleep transistors placed in series between a circuit and its supply voltage (*e.g.*, sleep transistor 130 between V_{DD} and V_{SS} as depicted in FIG. 1) can act as a switch to control whether the circuit is in an operational or standby state. MTK-1001, 2:9-20. When the sleep transistor is turned on, the circuit is connected to its supply voltage and is placed into an operational state. On the other hand, when the sleep transistor is turned off, the circuit is disconnected from its source voltage and enters a low-power standby (*i.e.*, sleep) mode.

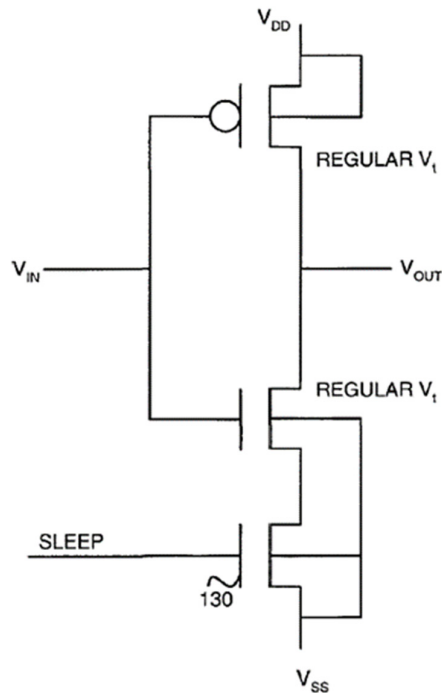


FIG. 1
PRIOR ART

MTK-1001, FIG. 1.

67. Another common solution for controlling power consumption in integrated circuits is to divide the integrated circuit into distinct power regions—often referred to as power islands—whose power consumptions can be controlled independently. MTK-1001, 3:49-55, 3:65-4:10 (“A power island is any section, delineation, partition, or division of an integrated circuit where power consumption is controlled within the section, delineation, partition, or division.”). As the ’077 Patent explains, an integrated circuit can have multiple power islands, and sleep transistors can be used to control the power consumed by those individual power islands. *See* MTK-1001, FIG. 2.

68. The '077 Patent discloses such a technique with respect to Figure 2.

MTK-1001, 3:49-4:27.

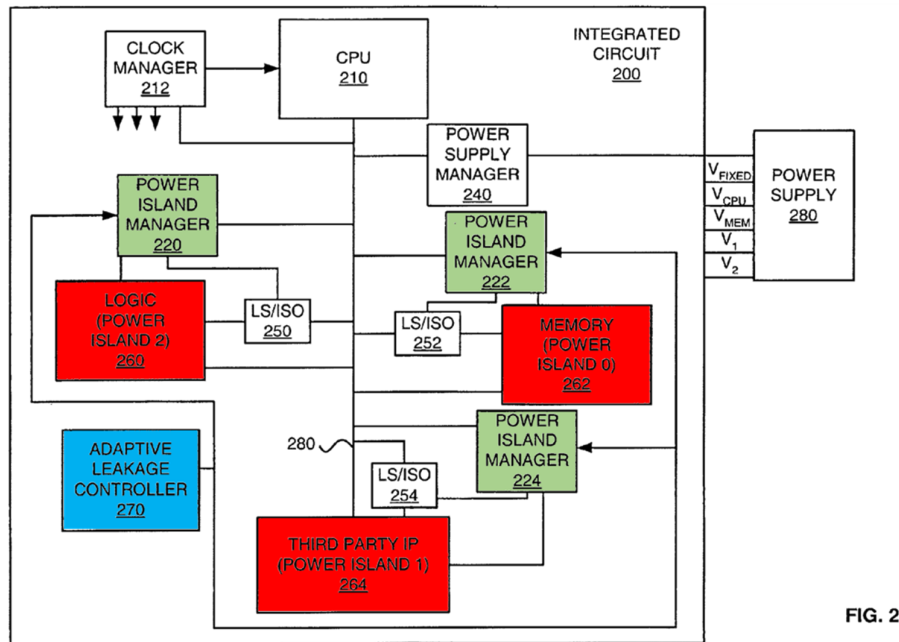


FIG. 2

MTK-1001, FIG. 2 (annotated).

69. Specifically, in the integrated circuit embodiment of Figure 2, the power islands 260, 262, 264 (in red) have associated low leakage circuitry such as sleep transistors. MTK-1001, 3:49-55, 3:65-4:10. As also shown in Figure 2, “the power islands are delineated based on geographic factors of the integrated circuit” or “based on functional IP units of the integrated circuit 200,” such as “memory 262, logic 260, and third party IP 264.” *Id.*, 3:65-4:10.

70. Each of the power islands is connected to a power island manager 220, 222, 224 (in green) that provides control signals to the power island to control its power consumption. MTK-1001, 3:49-55, 4:11-20. The '077 Patent

explains that “[t]he power island managers ... are any circuitry, device, or system configured to provide control signals to a power island to control power within the power island.” *Id.*, 4:11-20. For example, a power island manager “may select a clock, change clock frequency, or modify the voltage within the power island to control the power consumption of the power island.” *Id.*

71. The '077 Patent's technique also uses an adaptive leakage controller (in blue) that provides control signals to the power island managers. MTK-1001, 4:21-39. The '077 Patent explains that the adaptive leakage controller provides control signals so that the power island managers “provide the optimum voltage to be applied to sleep transistors in the power islands.” *Id.* For example, in an “exemplary embodiment,” the control signals can “compensate for process and temperature variation.” *Id.*; *see also id.*, 3:65-4:10. In this way, the voltages applied to the power islands are optimized to reduce leakage currents while the power islands are in standby (*i.e.*, sleep) mode. By reducing power consumption during standby, overall power consumption of the integrated circuit can be reduced. MTK-1001, 4:21-5:7.

72. Generally, the claims of the '077 Patent are directed to the use of power islands in conjunction with an adaptive leakage controller, power island manager, and low leakage sleep circuits. As demonstrated below, the disclosed technique, including each of these elements, were known in the prior art, such that all of the claims of the '077 Patent are rendered obvious. While the '077 Patent also discloses embodiments relating to data retention in integrated circuits

during standby mode, neither data retention nor data retention circuitry is recited by the claims. Therefore, I do not provide an overview of those portions of the '077 Patent here. *See, e.g.*, MTK-1001, FIGS. 3 (depicting a “data retention state machine 330”), 5, 6, 7A-7C, 8A-8B, 9-12 (collectively referred to as describing the unclaimed “Low Leakage Data Retention Circuitry”).

C. Prosecution History of the '077 Patent

73. U.S. Patent Application No. 13/569,613 (“the '613 Application”), which ultimately resulted in the '077 Patent, was filed on August 8, 2012. MTK-1001, Cover. The '613 Application claimed priority through a series of continuations to U.S. Provisional Patent Application No. 60/546,574 with a priority date of February 19, 2004. MTK-1002, 98-100. After filing the '613 Application, the Applicant filed a Preliminary Amendment on October 16, 2012 that cancelled originally-filed claims 1-63 and added new claims 64-81. *Id.*, 84-88. The Patent Office subsequently allowed the '077 Patent claims on January 24, 2014 without issuing a rejection. *Id.*, 157-164 (Notice of Allowance), *see also id.*, 263-267 (June 6, 2014 Second Notice of Allowance). The '077 Patent issued on October 7, 2014. MTK-1001, Cover.

D. Interpretation of the '077 Patent Claims

74. I understand that, for purposes of my analysis in this IPR proceeding, the terms appearing in the patent claims should be interpreted according to what is referred to as the “*Phillips*” standard. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. § 42.100. I further understand that the words of the

claims should be given their plain meaning unless that meaning is inconsistent with the patent specification or the patent's history of examination before the Patent Office. I also understand that the words of the claims should be interpreted as they would have been interpreted by a POSITA at the time of the invention (not today). Without further information on what date the invention as claimed was made, I have used the earliest possible priority date of the '077 Patent as the point in time for claim interpretation purposes. Patent Owner asserts that date was December 11, 2003. However, my interpretation of the words of the claims would be the same if the earliest possible priority date of the '077 Patent was anywhere within the late 1990s to early 2000s.

VII. OVERVIEW OF CONCLUSIONS FORMED

75. I have reviewed the Petition for IPR of the '077 Patent, and agree with the analysis contained therein. In summary, it is my opinion that each and every limitation of each and every challenged claim, whether taken alone or in combination, would have been at least obvious to one of ordinary skill in the art at the time of the alleged invention in view of the prior art cited in the Petition and further explained in this declaration. To summarize my conclusions:

- Based upon my knowledge and experience and my review of the prior art listed at Section V above, I believe that claims 1-18 of the '077 Patent are rendered obvious by Takahashi.

- Based upon my knowledge and experience and my review of the prior art listed at Section V above, I believe that claims 3 and 12 of the '077 Patent are rendered obvious by Takahashi in view of Ko.
- Based upon my knowledge and experience and my review of the prior art listed at Section V above, I believe that claims 5 and 14 of the '077 Patent are rendered obvious by Takahashi in view of Schutz.
- Based upon my knowledge and experience and my review of the prior art listed at Section V above, I believe that claims 1-18 of the '077 Patent are rendered obvious by Mizuno.
- Based upon my knowledge and experience and my review of the prior art listed at Section V above, I believe that claims 3 and 12 of the '077 Patent are rendered obvious by Mizuno in view of Ko.

VIII. ANALYSIS OF THE PRIOR ART

A. Analysis of Takahashi with Respect to Claims 1-18

76. For the reasons articulated in detail below, and based on my review of the '077 Patent and the Takahashi reference, it is my opinion that a POSITA would have readily understood that Takahashi renders obvious all elements of claims 1-18 of the '077 Patent.

1. Overview of Takahashi

77. Takahashi is titled “Suppressing the Leakage Current in an Integrated Circuit.” MTK-1004, Title. Takahashi explains that the Field of the Invention is “a semiconductor integrated circuit, for example, a semiconductor

integrated circuit by which power consumption can be reduced by suppressing leakage current.” *Id.*, [0001]. Takahashi acknowledges that power consumption in integrated circuits, including that due to leakage currents during standby, was a common problem in the art at the time.

In recent years, as semiconductor integrated circuit technology has progressed, mobile communication terminals, compact solid-state audio players, and portable semiconductor devices, such as laptop personal computers, have become pervasive. Since a necessary power is supplied to these semiconductor devices, it is absolutely essential to reduce the power consumption in order to allow them to operate for a long time.

In the case of a semiconductor integrated circuit, voltage reduction is one effective method for achieving low power consumption. Thus, semiconductor integrated circuits having a source voltage of 1.0 V or lower have been prototyped and have already been brought to the commercial stage. When the source voltage drops and becomes close to threshold voltage V_{th} of a MOS transistor, a drop in its operating speed becomes a problem. In order to maintain the operating speed of a semiconductor integrated circuit with a low source voltage, a transistor with a threshold voltage lower than that of a normal transistor is needed. However, along with a decrease in the threshold voltage of the transistor is an increase in leakage current results. Thus, while in a standby status, that is, when not operating, the increase in power consumption due to leakage current reaches a level which cannot be ignored, so that reduction of power consumption, the primary objective of reducing the voltage, can no longer be realized.

MTK-1004, [0002]-[0003].

78. Thus, Takahashi's "invention was created in light of such a situation, and its objective is to present a semiconductor integrated circuit by which the leakage current during standby can be suppressed while maintaining the reliability of the gate oxide film, the circuit area can be minimized, and defects can be detected reliably." *Id.*, [0016].

79. Takahashi describes "a first embodiment of a semiconductor integrated circuit" for reducing leakage current during standby with reference to Figures 1-5. MTK-1004, [0047]-[0053]. As shown in Figure 1, the "device 200" includes a "logic circuit 10 having a CMOS structure, switching circuit 20 for supplying an operating current to logic circuit 10, voltage regulator 40 capable of supplying variable and multiple voltages, and control circuit 30 for controlling voltage regulator 40." MTK-1004, [0048].

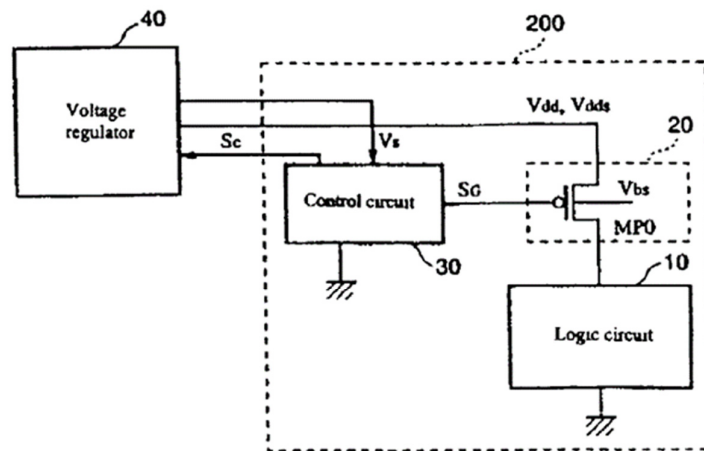


FIG. 1

MTK-1004, FIG. 1.

80. Takahashi explains that its “switching circuit 20” acts as a sleep transistor to place the “logic circuit 10” into an operational state or a standby state.

Switching circuit 20 supplies an operating current to logic circuit 10 during operation and suppresses the leakage current of the low threshold voltage transistor of logic circuit 10 during standby. As shown in FIG. 4, in switching circuit 20, the source of transistor MP0 is connected to source voltage V_{dd} supply line, and its drain is connected to node N1. In other words, node N1 is a virtual source voltage supply terminal of logic circuit 10. When transistor MP0 is conductive (on), source voltage V_{dd} is applied to node N1, and a driving current is supplied to logic circuit 10. On the other hand, when transistor MP0 is off (off), supply of current to logic circuit 10 is cut off. Thus, generation of a leakage current at logic circuit 10 is suppressed.

MTK-1004, [0052].

81. Takahashi further explains the control signals provided to the “switching circuit 20” to reduce leakage current in the “logic circuit 10.” *Id.*, [0053]-[0054]. As explained below, by adjusting the levels of the control signals provided to the “switching circuit 20,” the transistor MP0 can be placed into a low impedance state during operation of the “logic circuit 10” and into a “super cut-off status” during standby to reduce leakage current in the “logic circuit 10.”

Control signal S_G of different levels is applied to the gate of transistor MP0 during operation and during standby, respectively. Transistor MP0 is turned on or off according to the level of said control signal S_G . Furthermore, different levels are applied during operation and during standby, respectively, for the source voltage at the source of transistor MP0. In the prior art, the source voltage is kept at the same value

during operation and during standby. However, in the case of the semiconductor integrated circuit of the present embodiment, source voltages V_{dd} and V_{dds} are switched depending on the condition of logic circuit 10. For example, during operation, source voltage V_{dd} is set to nominal operating voltage V_{ddN} of the transistor. During standby, the source voltage is set to value V_{ddL} , for example, $V_{ddL}=V_{ddN}-0.3$ V, slightly lower than V_{ddN} . As a result, the gate-source voltage of switching transistor MP0 acquires the opposite sign to that of the voltage during normal use in order to realize a super cut-off status.

MTK-1004, [0053].

82. A related embodiment shown in Figures 11-17 of Takahashi adds a “fusing circuit 202” to the “device 200” as shown below. MTK-1004, [0045], [0097]-[0117]. The “fusing circuit 202” supplies “control data DAT” to the “voltage regulator 100” such that the levels of the control signals generated by the “voltage regulator 100” are dependent upon both the “control data and status control signal S_c from device 200.” *Id.*, [0098].

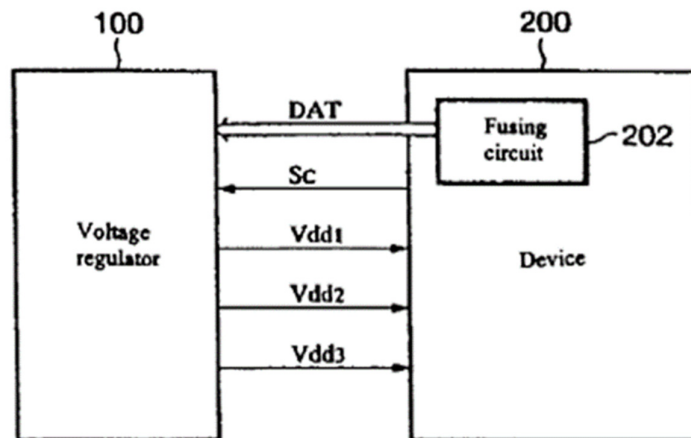


FIG. 11

MTK-1004, FIG. 11.

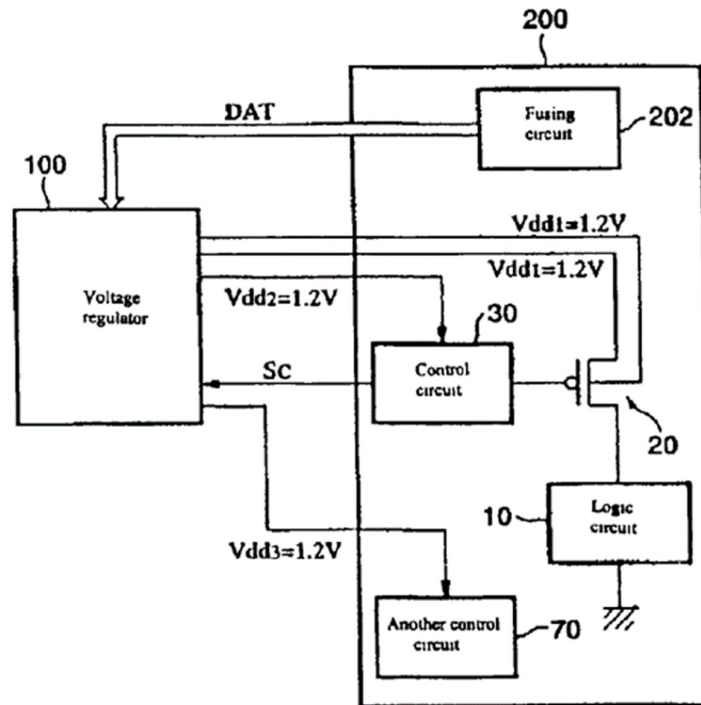


FIG. 16

MTK-1004, FIG. 16.

As shown in the figure, the semiconductor integrated circuit of the present embodiment is configured with voltage regulator 100 and device 200. Device 200 is provided with fusing circuit 202. Multiple-bit control data DAT are output by said fusing circuit 202. Upon receiving control data DAT from fusing circuit 202, voltage regulator 100 controls the level of voltage to be supplied to device 200 according to said control data and status control signal SC from device 200. In the case of the example in FIG. 11, multiple different levels of voltages V_{dd1} , V_{dd2} , and V_{dd3} are supplied from voltage regulator 100 to device 200.

MTK-1004, [0098].

83. Takahashi explains that the control data DAT is “based on the process requirements of device 200 during operation (Active mode) and during standby (Sleep mode).” *Id.*, [0110]. “Because voltage regulator 100 generates

source voltages V_{dd1} , V_{dd2} , and V_{dd3} using optimum values under the respective preset conditions according to control data DAT and control signal S_C indicating the operating status of device 200, and outputs them into device 200, optimum source voltages in accordance with the process requirements of the circuit elements constituting the device can be supplied, and the effect of variations in the production process can be reduced.” *Id.*, [0117]; *see also id.*, [0123]. The components and operation of the “device 200” in the embodiment of Figures 11-17 otherwise remain largely the same as in the embodiment of Figures 1-5.

84. In addition, Takahashi discloses a related embodiment with respect to Figure 10 that employs its invention for a “circuit capable of performing I_{ddq} measurement.” *Id.*, [0087]. “As shown in the figure, said measuring circuit is configured with local circuits, such as a scan-pass circuit comprising multiple flip-flops (FF), memories, a logic circuit, and a peripheral circuit, and a switching circuit for supplying a driving current to each respective local circuit.” *Id.*

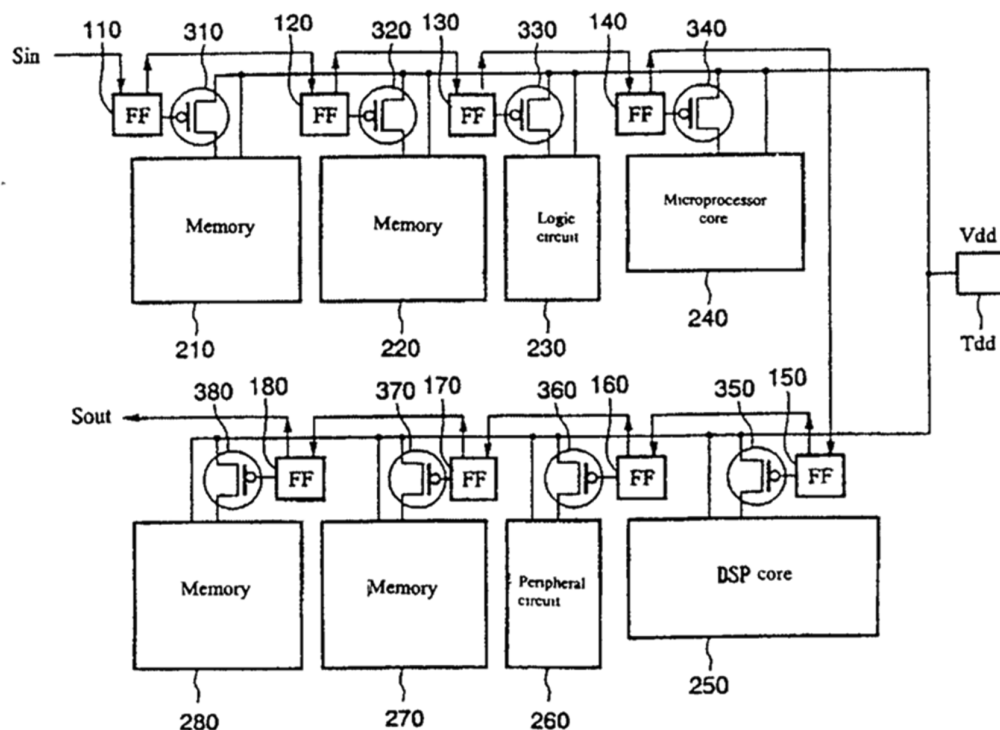


FIG. 10

MTK-1004, FIG. 10.

85. Like its other embodiments, Takahashi's Figure 10 includes a "switching circuit ... configured with pMOS transistors 310, 320, ..., and 380." *Id.*, [0090]. The pMOS transistors "are turned on/off ... in order to supply a driving current to a prescribed functional circuit when in the on status" and turn off the driving current when in the off status so that "occurrence of a leakage current in the functional circuit can be suppressed." *Id.* Using this mechanism, the circuit can measure the power consumption of a given power island both during operation and when in standby.

For example, when the test pattern is designed appropriately, data [logic] 0 is stored into flipflop 130, and data [logic] 1 is stored into all the other flip-flops.

Under said condition, transistor 330 is on, and the other transistors are all off. Thus, driving current is supplied to logic circuit 230, and logic circuit 230 becomes operational. On the other hand, because no driving current is supplied to any functional circuits other than logic circuit 230, these functional circuits are all in the standby status. Furthermore, in a functional circuit in the standby status, because the transistor constituting the switching circuit is turned off to cut off the leakage current path, occurrence of a leakage current can be suppressed.

At this time, the current supplied from source voltage V_{dd} supply terminal T_{dd} is supplied to logic circuit 230 which is in the operating status. Thus, power consumption of logic circuit 230 during the operation can be measured by measuring the current input from terminal T_{dd} .

As described above, in a semiconductor integrated circuit comprising multiple functional circuits, power consumption of the respective functional circuits during the operation can be measured using the measuring circuit of the present example by designing a test pattern to be input into the scan-pass circuit appropriately. In addition, power consumption due to leakage current at each functional circuit during standby can also be measured based on the same principle.

MTK-1004, [0092]-[0094].

2. Claim 1

(a) Element 1[p]

86. The preamble of claim 1 recites “A method carried out in an integrated circuit that includes an adaptive leakage controller, a power manager and a plurality of power islands, the method comprising.” Takahashi discloses and renders obvious the preamble of claim 1.

87. Takahashi pertains to methods carried out in an integrated circuit. MTK-1004, Abstract, [0001]. For example, the embodiments disclosed in Figures 1-5 and 11-17 of Takahashi are each described as a “semiconductor integrated circuit.” *Id.*, [0047] (“FIG. 1 is a circuit diagram showing a first embodiment of a semiconductor integrated circuit pertaining to the present invention.”), [0097] (“FIG. 11 is a diagram showing a fourth embodiment of a semiconductor integrated circuit pertaining to the present invention.”).

88. Takahashi’s integrated circuits include a “logic circuit 10 having a CMOS structure” that “is a functional circuit for performing a logic operation.” MTK-1004, [0045], [0048], [0078]. Takahashi provides specific examples of the types of functional circuits included in the “logic circuit 10.”

As shown in FIG. 4, logic circuit 10 is a CMOS inverter configured with pMOS transistor MP1 and NMOS transistor MN1. Furthermore, logic circuit 10 is not limited to said [configuration], and it may consist of other kinds of logic circuits, such as an AND circuit, a NAND circuit, or an OR circuit. Furthermore, the pMOS transistor and the nMOS transistor constituting logic circuit 10 are so-called low threshold voltage MOS transistors having a threshold voltage, or an absolute value of threshold voltage, lower than that of a normal transistor.

MTK-1004, [0050].

89. In my opinion, a POSITA would have understood and found it obvious that Takahashi’s “logic circuit 10” is a power island.

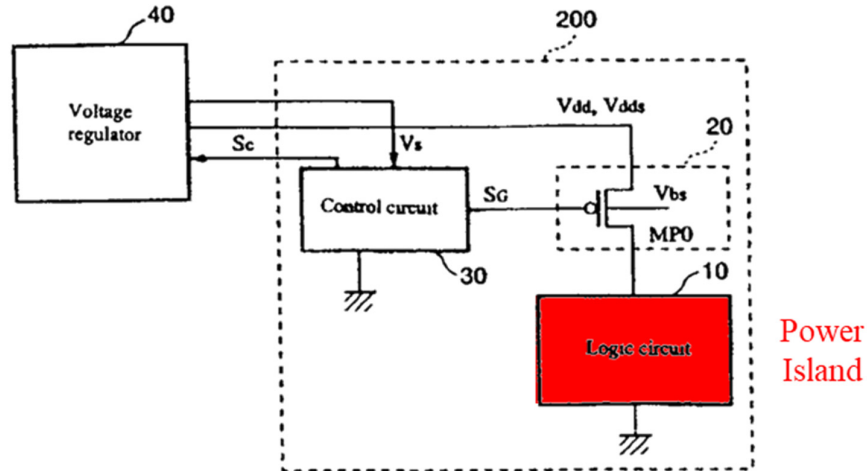


FIG. 1

MTK-1004, FIG. 1 (annotated).

The '077 Patent describes a power island as any “section, delineation, partition, or division of an integrated circuit where power consumption is controlled within the section, delineation, partition, or division.” *Id.*, 3:65-4:1. Takahashi’s “logic circuit 10” is a portion of the integrated circuit device where the power consumption is controlled within the portion of the integrated circuit. Specifically, power consumption within the “logic circuit 10” is controlled by the “[s]witching circuit 20 [that] supplies an operating current to logic circuit 10 during operation and suppresses the leakage current of the low threshold voltage transistor of logic circuit 10 during standby.” *Id.*, [0052]. That is, when the “switching circuit 20” is on, the “logic circuit 10” receives a voltage V_{dd} to place the “logic circuit 10” into operational mode, and when off, the “logic circuit 10” receives a lower voltage that places the “logic circuit 10” into a low-power standby state. *Id.*

90. Similarly, the “device 200” of Figures 11-17 includes the “logic circuit 10” and further includes “another control circuit 70” for “Wake up logic.” MTK-1004, [0110]-[0116], FIGS. 14-17.

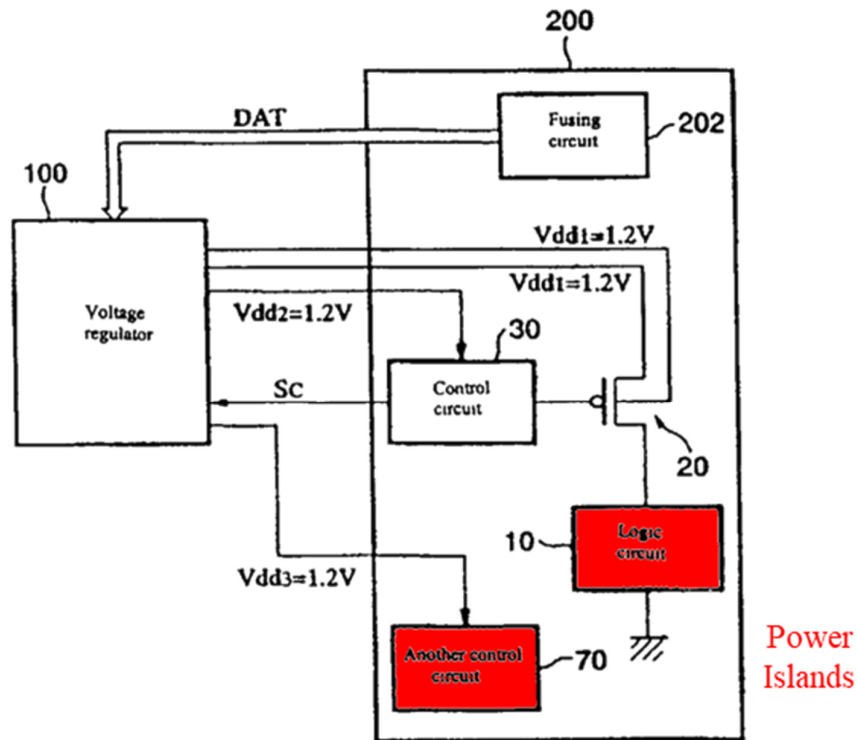


FIG. 16

MTK-1004, FIG. 16 (annotated).

91. In my opinion, a POSITA would have understood that the “control circuit 70” for “Wake up logic” is another power island because power consumption is controlled within the block 70. Specifically, “source voltage V_{dd3} ” varies between 1.2V and 0.7V based on whether the “Wake up logic” is in an operational or standby state. *Id.*; see also MTK-1001, 3:65-4:1. Power consumption by the “Wake up logic” power island is reduced when in the standby

state. Thus, Takahashi's integrated circuit "device 200" comprises a plurality of power islands, including at least the "logic circuit 10" and "control circuit 70."

92. Further, it is my opinion that a POSITA would have found it obvious for Takahashi's integrated circuit to include multiple power islands. The embodiments of Figures 1-5 and 11-17 that I discuss above disclose controlling the power consumption of individual circuit blocks, such as "logic circuit 10" and "control circuit 70" that are each a power island. Based on Takahashi's disclosure, a POSITA also would have found it obvious for these integrated circuits to include additional power islands.

93. Takahashi's integrated circuit of Figure 10 provides such an example. Figure 10 depicts a related embodiment for a "circuit capable of performing I_{ddq} measurement," *i.e.*, for measuring current through the various power islands in the circuit. MTK-1004, [0087]-[0095]. As shown below, the circuit of Figure 10 includes multiple power islands, including a "logic circuit 230," "[m]emories 210, 220, 270, and 280, ... microprocessor core 240, DSP core 250, and peripheral circuit 260." *Id.*, [0089].

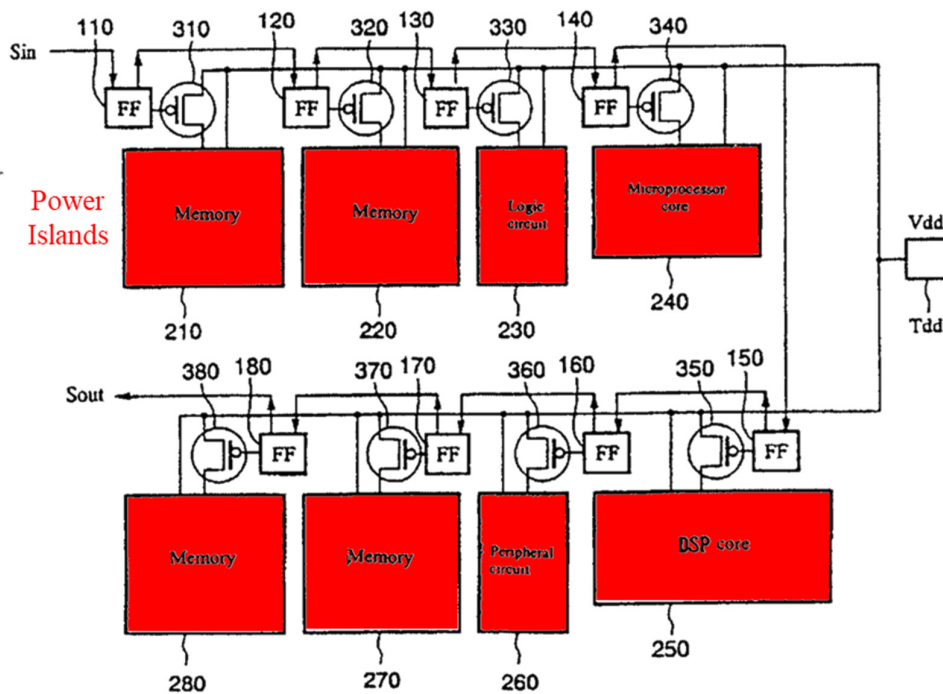


FIG. 10

MTK-1004, FIG. 10 (annotated).

94. Takahashi explains that power consumption within the power islands of Figure 10 uses the same mechanism as in the embodiments shown in Figures 1-5 and 11-17. Specifically, just as the power consumption within the integrated circuits of Figures 1-5 and 11-17 is controlled by the “switching circuit 20 ... with pMOS transistor MP0,” the power consumption within each of the functional circuits 210-280 in Figure 10 is controlled by the “switching circuit ... with pMOS transistors 310, 320, ... , and 380.” *Id.*, [0090].

The switching circuit is configured with pMOS transistors 310, 320, ... , and 380. These transistors are turned on/off according to the data held in respective flip-flops 110, 120, ... , and 180 in order to supply a driving current to a prescribed functional circuit when in the on status. Because the current supply path to said

functional circuit is cut off when in the on status, occurrence of a leakage current in the functional circuit can be suppressed.

MTK-1004, [0090].

95. In my opinion, a POSITA would have found it obvious to incorporate additional power islands like those shown in Figure 10 into the embodiments of Figures 1-5 and 11-17. Indeed, the embodiment of Figures 11-17 expressly contemplates having “another control circuit 70” that may be, for example, “Wake up logic.” Including additional power islands in the integrated circuit would provide additional functionality in the integrated circuit device (*e.g.*, memory or digital signal processing (DSP)). A POSITA would have understood and been motivated to control power consumption within these additional power islands using the mechanism shown in the embodiments of Figures 1-5, 10, and 11-17 to reduce the overall power consumption of the device, and would have understood how to do so using the “voltage regulator 10” and additional “switching circuits” as shown in these embodiments.

96. In my opinion, Takahashi also discloses and renders obvious the claimed “power manager.” Specifically, Takahashi’s integrated circuits include a “voltage regulator” that “controls the level of voltage to be supplied to device 200.” MTK-1004, [0098]. A POSITA would have understood and found obvious that Takahashi’s “voltage regulator” is a “power manager” because it controls power within the power islands, *e.g.*, the “logic circuit 10” and “control circuit 70.” *See* MTK-1001, 4:11-14.

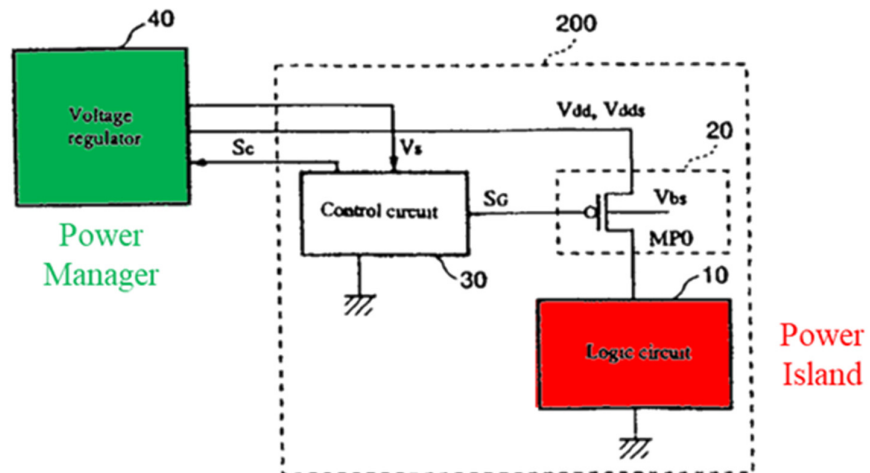


FIG. 1

MTK-1004, FIG. 1 (annotated).

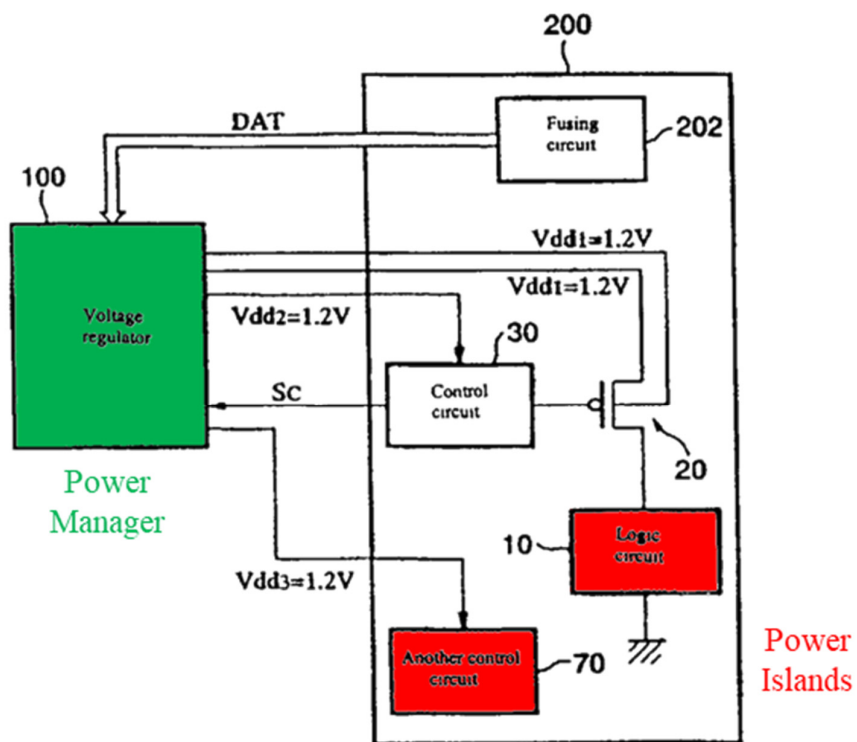


FIG. 16

MTK-1004, FIG. 16 (annotated).

97. For example, Takahashi explains that the “voltage regulator 40” in the embodiment of Figures 1-5 provides different voltage levels in order to control power within the “logic circuit 10.” Specifically, during operation of the “logic circuit 10,” the “voltage regulator 40” provides signals V_{dd} , V_{dds} to provide power to the “logic circuit 10.” MTK-1004, [0053]. On the other hand, when the “logic circuit 10” is in standby, “voltage regulator 40” lowers the voltage to achieve a “super cut-off status” in the “switching circuit 20” that achieves lower leakage current and reduced power consumption.

Furthermore, different levels are applied during operation and during standby, respectively, for the source voltage at the source of transistor MP0. In the prior art, the source voltage is kept at the same value during operation and during standby. However, in the case of the semiconductor integrated circuit of the present embodiment, source voltages V_{dd} and V_{dds} are switched depending on the condition of logic circuit 10. For example, during operation, source voltage V_{dd} is set to nominal operating voltage V_{ddN} of the transistor. During standby, the source voltage is set to value V_{ddL} , for example, $V_{ddL}=V_{ddN}-0.3V$, slightly lower than V_{ddN} . As a result, the gate-source voltage of switching transistor MP0 acquires the opposite sign to that of the voltage during normal use in order to realize a super cut-off status.

MTK-1004, [0053].

98. Similarly, in the embodiment of Figures 11-17, the “voltage regulator 100” provides different voltage signals to control the power within the “logic circuit 10” and “control circuit 70” during “Active” and “Sleep” modes. *Id.*, [0110]-[0117], FIGS. 14-17. During “Active mode,” the “voltage regulator

100” provides voltage signals (V_{dd1} , V_{dd2} , V_{dd3}) to power up the “logic circuit 10” and “control circuit 70.” *Id.* On the other hand, during “Sleep mode,” the “voltage regulator 100” lowers the voltage signals to put the “logic circuit 10” and “control circuit 70” to sleep. *Id.*

Active Mode	Bit 2	Bit 1	Bit 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0	0	0	1.2V	1.2V	1.20V	Weak
Fuse prog-1	0	0	1	1.15V	1.15V	1.15V	NTPW,NWPT
Fuse prog-2	0	1	0	1.05V	1.05V	1.05V	TYPC,NSPW,NWPS
Fuse prog-3	0	1	1	0.95V	0.95V	0.95V	NSPT,NTPS
Fuse prog-4	1	0	0	0.85V	0.85V	0.85V	Strong

FIG. 14

Sleep Mode	Bit 2	Bit 1	Bit 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0	0	0	0.7V	1.0V	0.7V	Weak
Fuse prog-1	0	0	1	0.7V	1.0V	0.7V	NTPW,NWPT
Fuse prog-2	0	1	0	0.7V	1.0V	0.7V	TYPC,NSPW,NWPS
Fuse prog-3	0	1	1	0.7V	1.0V	0.7V	NSPT,NTPS
Fuse prog-4	1	0	0	0.7V	1.0V	0.7V	Strong

FIG. 15

MTK-1004, FIGS. 14-15 (annotated).

99. Therefore, in my opinion a POSITA would have understood and found obvious that Takahashi’s “voltage regulator” is a power manager. While the ’077 Patent does not describe a “power manager” in its written description, the ’077 Patent does briefly describe a “power island manager.”

The power island managers 220, 222, and 224 are any circuitry, device, or system configured to provide control signals to a power island to control power within the power island. The power island managers 220, 222, and 224 can dynamically change the power

consumption of the power islands based on the needs and operation of the integrated circuit 200. The power island managers 220, 222, 224 may select a clock, change clock frequency, or modify the voltage within the power island to control the power consumption of the power island.

MTK-1001, 4:11-20; *see also id.*, 3:49-55.

100. Like the '077 Patent's "power island manager" that "control[s] power within the power island," Takahashi's "voltage regulator" controls power within the "logic circuit 10" and "control circuit 70." *See id.* The '077 Patent states that the "power island managers ... may select a clock, change clock frequency, or modify the voltage within the power island to control the power consumption of the power island." *Id.* As explained above, Takahashi's "voltage regulator" likewise modifies the voltage within the power island (*e.g.*, "logic circuit 10") to control the power consumption of the power island during active and standby states. MTK-1004, [0052]-[0053].

101. In my opinion, Takahashi also discloses and renders obvious that its integrated circuit includes an "adaptive leakage controller" as required by Claim 1 of the '077 Patent. Specifically, Takahashi's integrated circuit includes a "control circuit 30" that controls the "voltage regulator." MTK-1004, [0048].

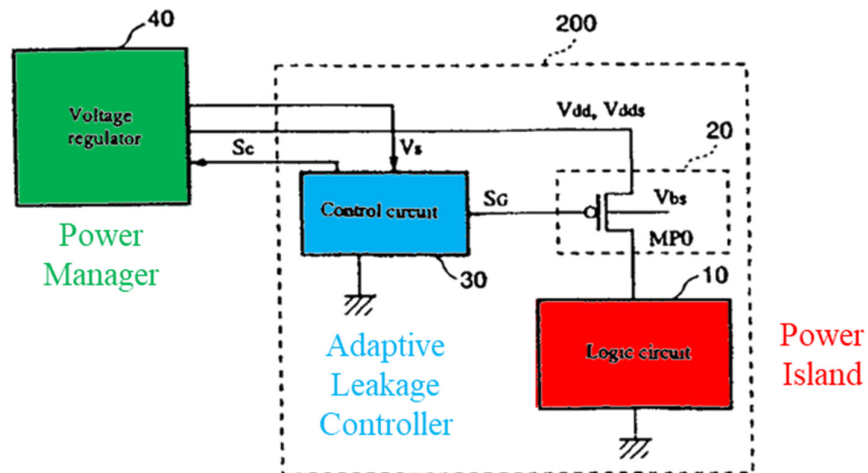


FIG. 1

MTK-1004, FIG. 1 (annotated).

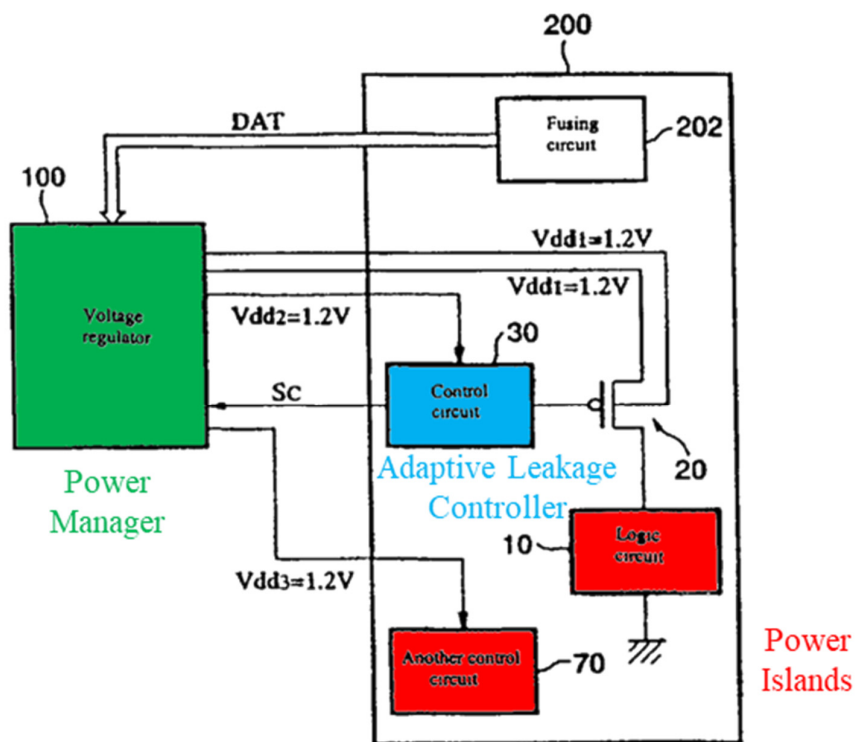


FIG. 16

MTK-1004, FIG. 16 (annotated).

102. Takahashi explains that the adaptive leakage controller “control circuit 30 ... generates control signal S_C as the operating status of device 200 changes and outputs it into voltage regulator 100” (“voltage regulator 40” in Figures 1-5) such that “voltage regulator 100 generates source voltages V_{dd1} , V_{dd2} , and V_{dd3} using optimum values under the respective preset conditions according to control data DAT and control signal S_C indicating the operating status of device 200, and outputs them into device 200.” MTK-1004, [0116]-[0117]. The “control circuit 30” also generates a “[c]ontrol signal S_G of different levels [that] is applied to the gate of transistor MP0 during operation and during standby” such that “[t]ransistor MP0 is turned on or off according to the level of said control signal S_G .” *Id.*, [0053].

103. Thus, the “control circuit 30” controls the amount of leakage in the “device 200.” Specifically, based on the control signals S_C and S_G , “the switching circuit can be turned on during operation to supply driving current to the logic circuit, and the switching circuit can be turned off to suppress the occurrence of leakage current in low threshold voltage transistors in the logic circuit” during standby. *Id.*, [0117]-[0118]. Takahashi further explains that the “switching transistor MP0” of the “switching circuit 20” is placed into a “super cut-off status” during standby to further reduce the leakage current. *Id.*, [0053], [0118]; *see also id.*, [0010], [0058], [0062], [0073], [0085], [0116]. To do so, during standby the “source voltage is set to value V_{ddL} , for example, $V_{ddL}=V_{ddN}-0.3V$ ” such that the “gate-source voltage of switching transistor MP0 acquires the

opposite sign to that of the voltage during normal use.” *Id.*, [0053]. The “drain current I_D can be further suppressed in addition to the super cut-off effect by controlling bulk bias voltage V_{bs} to be high.” *Id.*, [0058]; *see also id.*, [0118].

104. Thus, in my opinion a POSITA would have understood and found obvious that Takahashi’s “control circuit 30” is an adaptive leakage controller that provides control signals for optimizing the voltages applied to the “switching circuit 20” and power islands of the “device 200.” MTK-1001, 4:21-23. By optimizing the voltages applied to the “switching circuit 20” and power islands of the “device 200” based on the operation state of the “device 200,” the “control circuit 30” adaptively controls leakage within the “device 200” to reduce power consumption.

105. Though not recited by the claims, the ’077 Patent explains with respect to its Figure 2 that the “adaptive leakage controller (ALC) 270 ... provides control signals to compensate for process and temperature variation to provide the optimum voltage to be applied to sleep transistors in the power islands.” MTK-1001, 4:21-27; *see also id.*, 4:28-39.

106. To the extent such functionality is required of the claimed “adaptive leakage controller,” Takahashi renders obvious this element to a POSITA. Takahashi’s embodiment of Figures 11-17 includes a “fusing circuit 202” that provides “control data DAT” indicating the “effect of variations in the production process” on the “driving capability” of the transistors in “device 200.” *See* MTK-1004, [0098], [0104], [0110]-[0111], [0117]. “Because voltage regulator 100

generates source voltages V_{dd1} , V_{dd2} , and V_{dd3} using optimum values under the respective preset conditions according to control data DAT and control signal S_C indicating the operating status of device 200, and outputs them into device 200, optimum source voltages in accordance with the process requirements of the circuit elements constituting the device can be supplied, and the effect of variations in the production process can be reduced.” *Id.*, [0117]. In my opinion, a POSITA would have found it obvious for the “control circuit 30” to provide the “control data DAT” to the “voltage regulator 100” (*e.g.*, by integrating the “fusing circuit 202” into the “control circuit 30”). By doing so, the control signals from the “control circuit 30” would also optimize the variable voltages output by the “voltage regulator 100” based on process variation.

107. Further, it is my opinion that it would have been obvious for the control signals from “control circuit 30” to also account for temperature variation. It was well-known at the time of the ’077 Patent that transistor performance is dependent both on process variation and temperature variation. *See, e.g.*, MTK-1010, 1:37-2:14 (“Thus, it is known that varying supply voltage to a chip can improve performance by eliminating unexpected variability in the supply voltage, and by accounting for process and operating temperature variations.”); MTK-1011, 12:18-21 (“the temperature dependency and any variation caused in manufacturing can be cancelled”); MTK-1012, 2:34-43, FIG. 2 (“leakage power in an integrated circuit increases exponentially as a function of temperature”); MTK-1013, 1:19-30 (“a sub threshold leakage of a metal-oxide semiconductor

field effect transistor (MOSFET) may be increased up to ten times when the temperature is raised from room temperature to 100° Celsius”); MTK-1014, 4:14-23 (“In some embodiments, the line regulation provided by the first feedback loop may filter input noise and compensate for process and temperature variations.”). For example, Sedra explains that the “[s]tudy of semiconductor physics shows that at an absolute temperature T (in Kelvins), the intrinsic concentration n_i (that is, the number of free electrons and holes per cubic centimeter) can be found from $n_i^2 = BT^3 e^{-E_G/kT}$ (3.6) where B is a material-dependent parameter = 5.4×10^{31} for silicon, E_G is a parameter known as the bandgap energy = 1.12 electron volts (eV) for silicon, and k is Boltzmann's constant = 8.62×10^{-5} eV/K.” MTK-1017, 139. In this excerpt, Sedra clearly explains that the number of free electrons, n_i , depends on, among other things, the temperature and the material, which in turn determines the conductivity of the semiconductors (*e.g.*, diodes) and their on/off characteristics. Thus, in addition to sending control signals indicating the status of the “device 200” and process variation, it would have been obvious for the “control circuit 30” to send control signals that also indicate temperature variation. By doing so, the voltages provided to Takahashi’s “switching circuit 20” and power islands would be further optimized to reduce leakage during standby.

108. Thus, even if claim 1 of the ’077 Patent is construed to require that the “adaptive leakage controller” has the features of the “ALC 270” of Figure 2 of the ’077 Patent, Takahashi discloses and renders obvious that element.

109. Further, I understand that the terms “power island” and “power manager” have been construed in prior litigations involving a patent describing a similar subject matter, U.S. Patent No. 7,051,306. *See* MTK-1025 43-44 (construing “power island” as “section of an integrated circuit where power consumption is controlled by independently varying its operating voltage and its frequency of operation”); 44-46 (construing “power manager” as “circuitry, device, or system configured to determine a target power level of a power island, determine an action to change the target power level, and perform an action to change the consumption power level to the target power level”); MTK-1026 28-29 (clarifying meaning of prior construction of “power island” as “a section of an integrated circuit where power consumption is controlled by independently varying its operating voltage or its frequency of operation (or both)”); 29-34 (construing “power manager” as “any system, circuitry, or device configured to control power”). In my opinion, no construction is necessary for the purposes of this proceeding because plain and ordinary meaning suffices. And while the prior constructions involved a different patent and different claims, Takahashi’s disclosures, in light of a POSITA’s knowledge, would also render these terms obvious under the prior constructions for the reasons discussed above with respect to element 1[p]. *See also* MTK-1001, 4:11-20; *see also id.*, 3:49-55; MTK-1005, [0121]; MTK-1006, 1:21-38.

110. Thus, to the extent the preamble of claim 1 of the '077 Patent is limiting, it is my opinion that Takahashi discloses and renders obvious the preamble of claim 1.

(b) Element 1[a]

111. Element 1[a] recites “receiving, at the power manager, a control signal from the adaptive leakage controller.” In my opinion, Takahashi discloses and renders obvious element 1[a].

112. As I explained with respect to the preamble of claim 1, it is my opinion that Takahashi discloses and otherwise renders obvious a power manager and adaptive leakage controller. Specifically, it is my opinion that in the related embodiments of Figures 1-5 and 11-17, Takahashi’s “voltage regulator” (labelled “40” in Figures 1-5 and “100” in Figures 11-17) discloses and renders obvious a power manager, and Takahashi’s “control circuit 30” discloses and renders obvious an adaptive leakage controller.

113. As shown below, Takahashi discloses that the adaptive leakage controller (*i.e.*, the “control circuit 30”) sends a “control signal S_c ” to the power manager (*i.e.*, the “voltage regulator”). MTK-1004, [0116]-[0117].

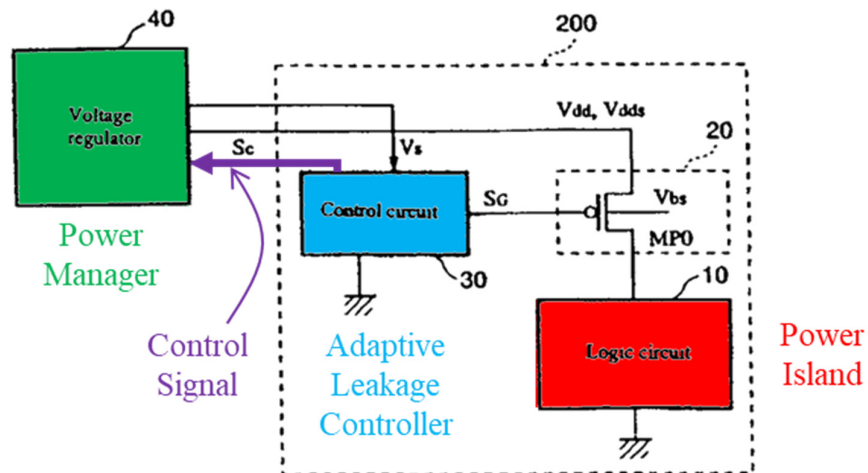


FIG. 1

MTK-1004, FIG. 1 (annotated).

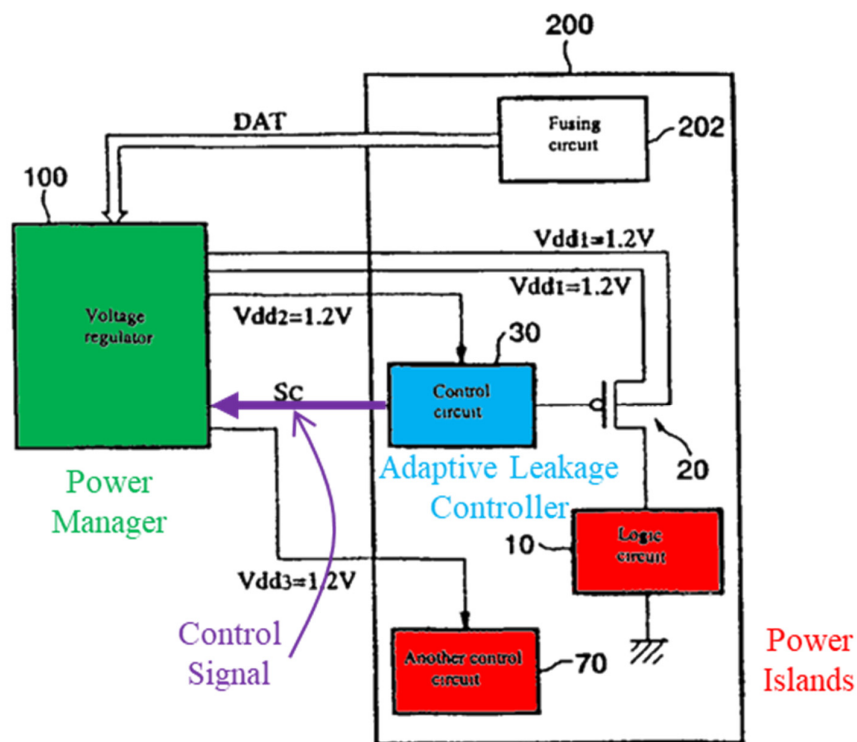


FIG. 16

MTK-1004, FIG. 16 (annotated).

114. Takahashi's "control signal S_C " indicates the "operating status of device 200," including the "logic circuit 10." MTK-1004, [0116]. Specifically, Takahashi's "control signal S_C " is provided to the "voltage regulator" to indicate whether the "device 200" is in "operation (Active mode)" or "standby (Sleep mode)." *Id.*, [0109]-[0110]. Takahashi's "[v]oltage regulator 100 generates different levels of source voltages during operation and during standby according to said control data DAT and status control signal S_C and supplies them to device 200." MTK-1004, [0111]; *see also id.*, [0098], FIG. 1. For example, in Figures 11-17, based on the "control signal S_C " the "[v]oltage regulator 100 controls the levels of source voltages V_{dd1} , V_{dd2} , and V_{dd3} supplied to device 200 using predetermined optimum values according to control signal S_C indicating control data DAT and the operating condition of the device." *Id.*, [0109].

115. Thus, in my opinion a POSITA would find that Takahashi discloses and renders obvious "receiving, at the power manager, a control signal from the adaptive leakage controller."

(c) Element 1[b]

116. Element 1[b] recites "employing the power manager to dynamically change power consumptions of the plurality of power islands, the employing the power manager to dynamically change power consumptions including: generating a variable voltage based on the control signal; and providing the variable voltage to at least one of low leakage sleep circuits of the integrated circuit." In my opinion, Takahashi discloses and renders obvious element 1[b].

117. As explained with respect to elements 1[p] and 1[a], it is my opinion that Takahashi discloses and otherwise renders obvious a plurality of power islands and a power manager. Specifically, it is my opinion that Takahashi's "logic circuit 10" and "control circuit 70" are each a power island. It also would have been obvious to a POSITA to include multiple other power islands in Takahashi's integrated circuit to provide additional functionalities as shown, for example, in Figure 10 (*e.g.*, to add memory or digital signal processing (DSP) to the "device 200). Further, Takahashi's "control circuit 30" discloses and renders obvious a power manager.

118. Turning to element 1[b], it is my opinion that Takahashi discloses that its power manager (*i.e.*, "voltage regulator") "generat[es] a variable voltage based on the control signal" as required by claim 1. As shown below, Takahashi's "voltage regulator" generates a variable voltage " V_{dd} " (in Figures 1-5) or " V_{ddl} " (in Figures 11-17) based on the "control signal S_c " received from the "control circuit 30" (adaptive leakage controller).

119. For instance, Takahashi explains that the “source voltage V_{dd} ” generated by the “voltage regulator 40” in Figures 1-5 is set to “different levels ... during operation and during standby.” MTK-1004, [0053]. As shown in Figure 1 above and described in more detail with respect to Figures 11-17, the “control signal S_c ” notifies the “voltage regulator 40” of the status of the “logic circuit 10.”

Control signal S_G of different levels is applied to the gate of transistor MP0 during operation and during standby, respectively. Transistor MP0 is turned on or off according to the level of said control signal S_G . Furthermore, different levels are applied during operation and during standby, respectively, for the source voltage at the source of transistor MP0. In the prior art, the source voltage is kept at the same value during operation and during standby. ***However, in the case of the semiconductor integrated circuit of the present embodiment, source voltages V_{dd} and V_{dds} are switched depending on the condition of logic circuit 10.*** For example, during operation, source voltage V_{dd} is set to nominal operating voltage V_{ddN} of the transistor. During standby, the source voltage is set to value V_{ddL} , for example, $V_{ddL} = V_{ddN} - 0.3V$, slightly lower than V_{ddN} . As a result, the gate-source voltage of switching transistor MP0 acquires the opposite sign to that of the voltage during normal use in order to realize a super cut-off status.

MTK-1004, [0053] (emphasis added).

120. With respect to Figures 11-17, Takahashi explains that “multiple different levels of voltages V_{dd1} , V_{dd2} , and V_{dd3} are supplied from voltage regulator 100 to device 200” based on the “status control signal S_c ” received from the “control circuit 30.” *Id.*, [0098]. For example, Figures 16 and 17 of Takahashi

depict an example of the voltage signals output by the “voltage regulator 100” during operation and standby. When the “control signal Sc ” indicates that the “device 200” is in operation, “source voltage[] V_{dd1} ... [is] 1.2V as shown” in Figure 16, and when the “control signal Sc ” indicates that the “device 200” is in standby, “source voltage V_{dd1} generated by voltage regulator 100 ... is 0.7V” as shown in Figure 17. *Id.*, [0109], [0111]-[0115], FIGS. 14-15.

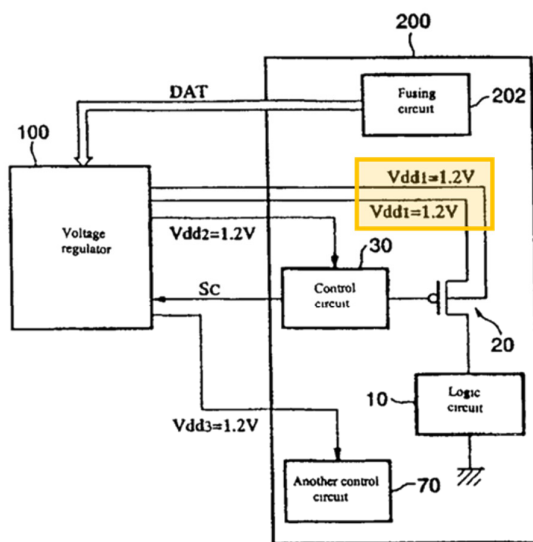


FIG. 16

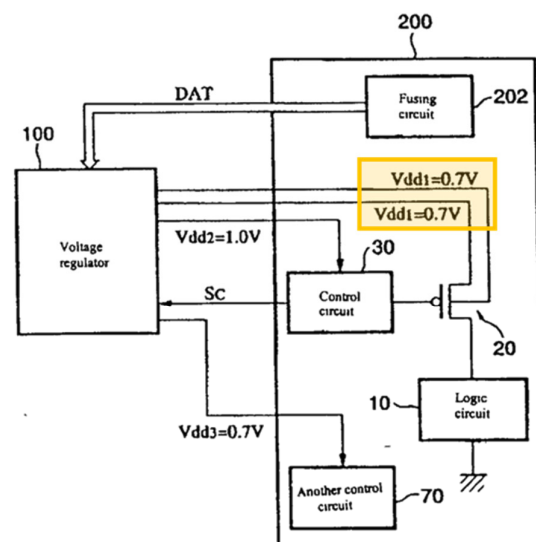


FIG. 17

MTK-1004, FIGS. 16-17 (annotated).

121. Takahashi further discloses and renders obvious “providing the variable voltage to at least one of low leakage sleep circuits of the integrated circuit.” Specifically, as shown in the related embodiments of Figures 1-5 and 11-17, Takahashi’s “voltage regulator 100” provides the variable voltage to the “switching circuit 20.” *Id.*, Abstract, [0051]-[0052], [0113]-[0116].¹

¹ In addition to the “source voltage V_{dd1} ,” Figures 14-15 of Takahashi also explain that “source voltage V_{dd2} ” is provided to the “SW Tr Gate,” which a

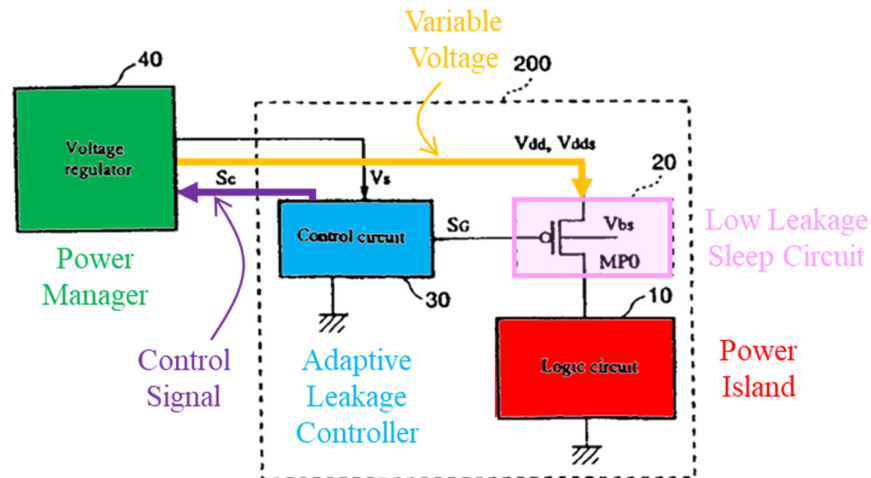


FIG. 1

MTK-1005, FIG. 1 (annotated).

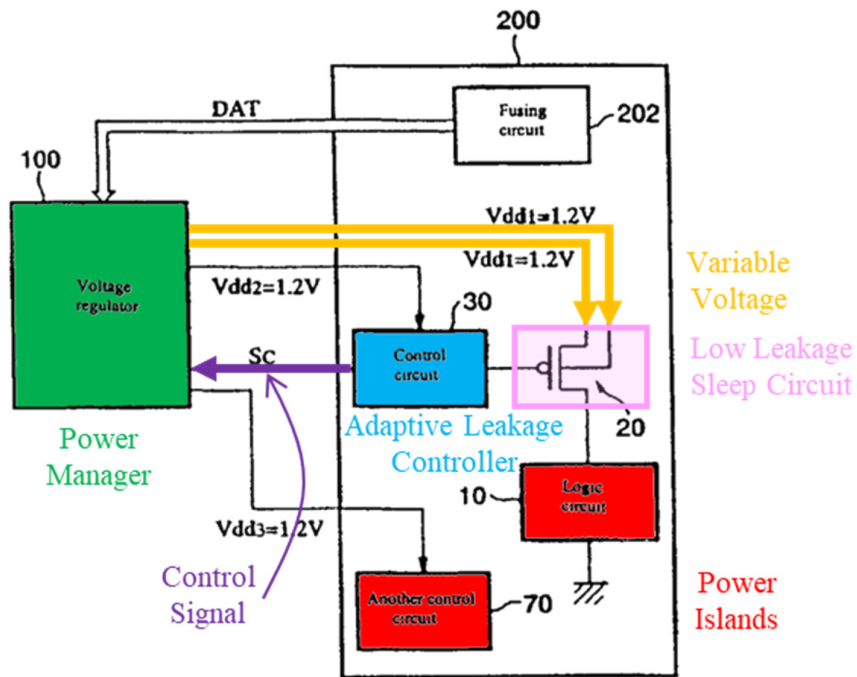


FIG. 16

POSITA would understand refers to the gate of “transistor MP0” in the “switching circuit 20.” Thus, “ V_{dd2} ” is another variable voltage that is generated by the power manager (*i.e.*, “voltage regulator”) based on the “control signal S_C .” MTK-1004, FIGS. 14-15.

MTK-1004, FIG. 16 (annotated).

122. In my opinion, the “switching circuit 20” is a low leakage sleep circuit because it reduces leakage during standby (sleep) mode. Takahashi explains that the “switching circuit 20 is configured with pMOS transistor MP0” that “supplies an operating current to logic circuit 10 during operation and suppresses the leakage current of the low threshold voltage transistor of logic circuit 10 during standby.” *Id.*, [0051]-[0053]. Specifically, “[w]hen transistor MP0 is conductive (on), source voltage V_{dd} is applied to node N1, and a driving current is supplied to logic circuit 10. On the other hand, when transistor MP0 is off (off), supply of current to logic circuit 10 is cut off. Thus, generation of a leakage current at logic circuit 10 is suppressed.” *Id.*, [0052].

123. While the '077 Patent does not use the term “low leakage sleep circuit” in its specification, the '077 Patent does disclose a “technique for reducing leakage [using] a sleep transistor” that “act[s] as a switch to turn on and off the logic gate.” MTK-1001, 2:9-20; *see also id.*, Abstract, 2:45-50, 4:21-5:7, 7:12-17. Specifically, “the sleep transistor 130 is turned on (gate to VDD) during normal cell operation. When the cell is idle, the sleep transistor 130 is turned off (gate tied to VSS) to reduce the leakage current of the cell.” *Id.*, 2:9-20; *see also id.*, 7:8-17 (“FIGS. 5, 6, 7A-C, and 8A-8B disclose one embodiment for low leakage, data retention circuitry. In this embodiment, in sleep mode, the circuit parts of a flip-flop that do not require data retention are coupled to ground through a sleep transistor. The gate of the sleep transistor is coupled to a sleep signal that

can be driven to a negative voltage such as $-0.3V$. Thus, the leakage in these circuit parts of the flip-flop is eliminated (reduced). When not in a sleep state, the sleep transistor has a gate value equal to or greater than the VDD supply, which effectively grounds the circuit.”). Takahashi’s “switching circuit 20” comprising the “transistor MP0” operates in this same way to provide an operational voltage to the “logic circuit 10” during “Active mode” and reduce leakage during “Sleep mode.” *See* MTK-1004, [0052], [0110].

124. While Figures 1-5 and 11-17 depict circuits with a single “switching circuit 20,” in my opinion a POSITA would have found it obvious for Takahashi’s integrated circuits to including multiple “switching circuits.” For example, Figure 10 of Takahashi depicts an embodiment with multiple “functional circuits” 210-280 that are each a power island, where power to each “functional circuit” is controlled by the “pMOS transistors” 310-380. MTK-1004, [0090]-[0091], [0094].

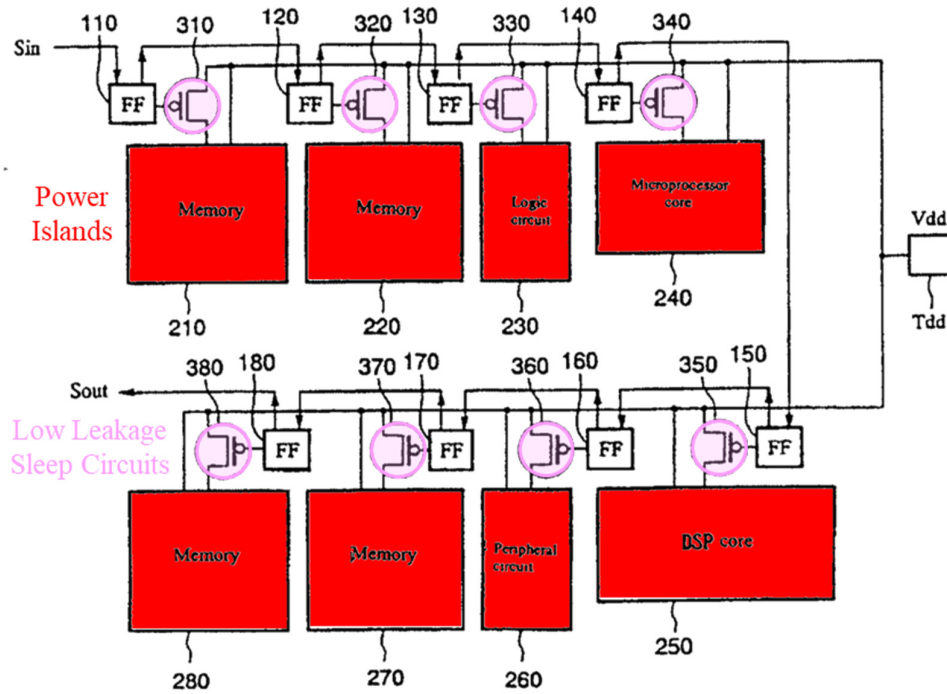


FIG. 10

MTK-1004, FIG. 10 (annotated).

Memories 210, 220, 270, and 280, logic circuit 230, microprocessor core 240, DSP core 250, and peripheral circuit 260 are functional circuits to be operated using source voltage V_{dd} .

The switching circuit is configured with pMOS transistors 310, 320, ... , and 380. These transistors are turned on/off according to the data held in respective flip-flops 110, 120, ... , and 180 in order to supply a driving current to a prescribed functional circuit when in the on status. Because the current supply path to said functional circuit is cut off when in the on status, occurrence of a leakage current in the functional circuit can be suppressed.

MTK-1004, [0089]-[0090].

125. In my opinion, a POSITA would have found it obvious to apply this structure to Takahashi's related embodiments in Figures 1-5 and 11-17. For

example, a POSITA would have understood that the “device 200” could include another “switching circuit 20” with an associated “logic circuit 10” as I show in the modified version of Figure 16 below.

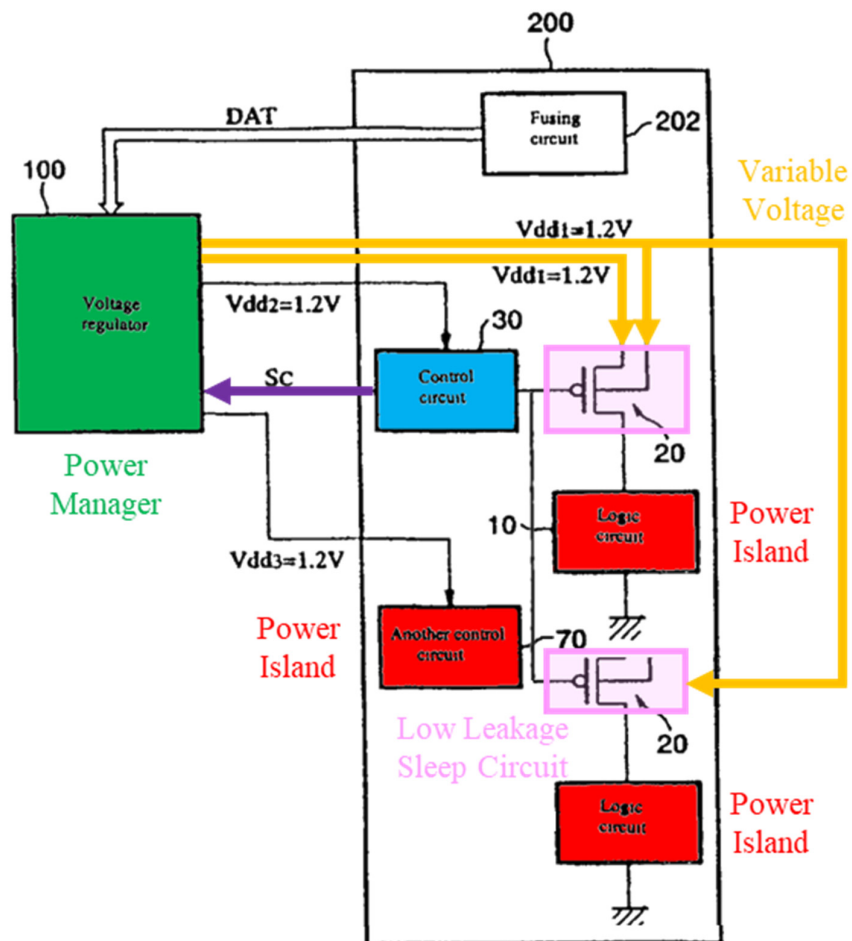


FIG. 16

MTK-1004, FIG. 16 (modified and annotated).

126. A POSITA would have understood that a “device 200” can include more than one “logic circuit 10” (or other type of functional circuit, *e.g.*, a memory as in Figure 10), and would have been motivated to provide a “switching

circuit 20” for each “logic circuit 10” to obtain the same leakage and power reduction benefits that I described above.

127. Other similar modifications to Takahashi’s embodiments of Figures 1-5 and 11-17 would also have been obvious. For example, a POSITA would have understood and found it obvious to include a “switching circuit 20” before the other “control circuit 70” so that leakage in the “control circuit 70” can be reduced when the “Wake up logic” is in standby. In another example, a POSITA would have understood and found it obvious to include multiple “control circuits 30,” each with its own “logic circuit 10” (or other type of functional circuit). Doing so would enable the device to provide power and reduce the leakage of the additional “logic circuit 10” (or other type of functional circuit) independently from the “logic circuit 10” shown in Figures 1-5 and 11-17.

128. As such, Takahashi’s integrated circuit “employ[s] the power manager to dynamically change power consumptions of the plurality of power islands” as required by claim 1. Specifically, as discussed above, Takahashi employs the “voltage regulator” (*i.e.*, power manager) to dynamically change the power consumptions of the power islands, including “logic circuit 10” and “control circuit 70.” As shown in Figures 11-17, for example, Takahashi’s “voltage regulator 100” provides the variable voltage “ V_{dd1} ” to the “switching circuit 20.” During an active mode, “ V_{dd1} ” is set to an operational voltage (*e.g.*, 1.2V as shown in Figure 16) to power the “logic circuit 10” power island. MTK-1004, [0112]-[0113]. Then, during standby, the variable voltage “ V_{dd1} ” is

reduced (*e.g.*, to 0.7V as shown in Figure 17) to reduce leakage current and therefore power consumption by the “logic circuit 10.” *Id.*, [0114]-[0116]. The “voltage regulator 100” similarly changes the varying voltage “V_{dd3}” to the other power island “control circuit 70,” to power the “Wake up logic” of “control circuit 70” during operation and reduce its power consumption during standby. *Id.*, [0110]-[0117], FIGS.14-17.

129. Thus, it is my opinion that Takahashi discloses and renders obvious element 1[b]. Because Takahashi discloses or renders obvious each element of claim 1 of the '077 Patent, it is my opinion that Takahashi renders obvious claim 1.

3. Claim 2

130. Claim 2 recites “[t]he method as claimed in claim 1 further comprising putting to sleep and taking out of sleep, at different times, at least one of the power islands.” In my opinion, Takahashi renders obvious claim 2 of the '077 Patent.

131. As I discussed at element 1[b] above, Takahashi’s power islands, including “logic circuit 10” and “control circuit 70,” are put into “standby (Sleep mode)” or “operation (Active mode)” at different times to reduce power consumption due to leakage currents when they are inactive. MTK-1004, [0110]. For example, Takahashi explains that the “switching circuit 20” that includes “transistor MP0” “supplies an operating current to logic circuit 10 during operation and suppresses the leakage current of the low threshold voltage

transistor of logic circuit 10 during standby.” *Id.*, [0052]-[0053]. “When transistor MP0 is conductive (on), source voltage V_{dd} is applied to node N1, and a driving current is supplied to logic circuit 10. On the other hand, when transistor MP0 is off (off), supply of current to logic circuit 10 is cut off” such that “generation of a leakage current at logic circuit 10 is suppressed.” *Id.*, [0052]; *see also id.*, [0098], [0112]-[0116] (describing the same functionality in Figures 11-17). Thus, the power island “logic circuit 10” is put to sleep and taken out of sleep at different times. Similarly, Takahashi discloses that the voltage “ V_{dd3} ” provided to another power island “control circuit 70” is varied to place the “Wake up logic” of “control circuit 70” into active or sleep modes at different times. MTK-1004, [0098]-[0100], [0110]-[0117].

132. A POSITA would also have understood that putting Takahashi’s power islands into “standby (Sleep mode)” or “operation (Active mode)” discloses the claimed “putting to sleep and taking out of sleep.” The ’077 Patent describes “sleep states” as those in which a circuit is not operational but has “low leakage.” *See* MTK-1001, Abstract, 2:37-50, 7:8-28. Thus, the ’077 Patent and Takahashi both refer to a “sleep” state as one in which a portion of the integrated circuit is not operational and has a reduced leakage. Other references from the same timeframe similarly describe such states as “sleep states.” *See, e.g.*, MTK-1018, 1:37-45 (“Leakage power consumption has become a major design concern for sub-micron transistors especially in low power applications, e.g., portable computers. For example, in portable computers with battery operation, leakage

power consumption may shorten the life of the battery. Consequently, techniques have been developed to mitigate leakage power consumption such as during the power saving mode of operation commonly referred to as ‘sleep mode’ or ‘sleep state.’”).

133. While not expressly recited by claim 2, to the extent that claim 2 requires putting power islands into sleep and out of sleep at different times from other power islands, it is my opinion that Takahashi renders obvious claim 2.² Specifically, a POSITA would have found it obvious to selectively place the “logic circuit 10” or “control circuit 70” power islands into standby (sleep) or operational (active) states at different times from other power islands, as Takahashi discusses with respect to Figure 10.

² In my opinion, the plain meaning of claim 2 does not require putting at least one power island to sleep and taking it out of sleep at different times *from other power islands*.

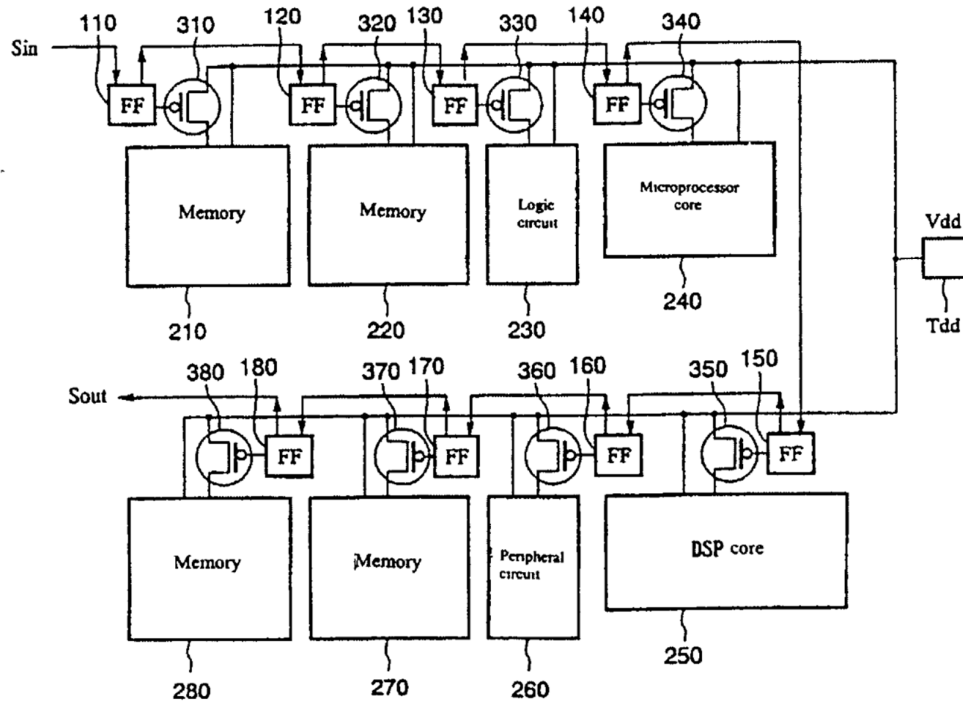


FIG. 10

MTK-1004, FIG. 10.

Memories 210, 220, 270, and 280, logic circuit 230, microprocessor core 240, DSP core 250, and peripheral circuit 260 are functional circuits to be operated using source voltage Vdd.

The switching circuit is configured with pMOS transistors 310, 320, ... , and 380. These transistors are turned on/off according to the data held in respective flip-flops 110, 120, ... , and 180 in order to supply a driving current to a prescribed functional circuit when in the on status. Because the current supply path to said functional circuit is cut off when in the on status, occurrence of a leakage current in the functional circuit can be suppressed.

MTK-1004, [0089]-[0090]; *see generally* [0087]-[0095] (“[I]n the semiconductor integrated circuit shown in FIG. 10, supply of driving current to the respective

functional circuits can be controlled individually by controlling the on/off status of the respective transistors constituting the switching circuit.”).

134. In my opinion, a POSITA would have been motivated to selectively place individual power islands into sleep or operational states because doing so would further reduce power consumption of the “device 200.” That is, a POSITA would have understood that putting unused power islands to sleep even while other power islands in the “device 200” are operational would reduce the overall power consumption of the “device 200.”

135. Further, in my opinion a POSITA would have known how to implement such a feature, as shown in Figure 10 of Takahashi, in the integrated circuit embodiments of Figures 1-5 and 11-17. For example, a POSITA would have understood that additional “switching circuits 20” could be added for the other power islands in Takahashi’s “device 200,” *e.g.*, adding a “switching circuit 20” for the “control circuit 70” power island. A POSITA also would have understood how to control the on/off operation of those additional “switching circuits 20” using the “control circuit 30” (*e.g.*, where the “control circuit 30” provides additional “control signals S_G ” for the additional “switching circuits 20”) or additional control circuits like the “control circuit 30.” Such modifications would have been well within the skill of a POSITA and would be simple modifications that a POSITA could perform with a reasonable expectation of success. Further, such a modification would provide the predictable result of putting unused power islands to sleep even while other power islands in the

“device 200” are active, thereby reducing power consumption of the “device 200” overall.

136. Thus, in my opinion Takahashi renders obvious claim 2 of the '077 Patent.

4. Claim 3

137. Claim 3 recites “[t]he method as claimed in claim 2 wherein the power manager employs a state machine to control the putting to sleep and the taking out of sleep.” In my opinion, Takahashi renders obvious claim 3 of the '077 Patent.

138. As I explained with respect to element 1[p] above, Takahashi’s “voltage regulator” discloses and renders obvious a power manager. A POSITA would have further understood and found obvious that Takahashi’s “voltage regulator” employs a state machine to control putting power islands (*e.g.*, the “logic circuit 10” and “control circuit 70”) to sleep and taking them out of sleep.

139. Specifically, Takahashi discloses that the “voltage regulator 100” of Figures 11-17 determines optimum “source voltages” for putting power islands into standby and operational states based on the “control data DAT” and “control signal S_C.” MTK-1004, [0098]-[0117]. With respect to Figures 13-15, Takahashi explains that the “control data DAT” is set “according to the driving capabilities of the pMOS transistor and the nMOS transistor constituting device 200.” *Id.*, [0100]. For instance, in Figure 13 the “levels of source voltage V_{dd} supplied to device 200 vary,” from V_{dd}=1.2V when the pMOS and nMOS transistors have

weak driving capabilities, to $V_{dd}=0.85V$ when the pMOS and nMOS transistors have strong driving capabilities. *Id.*, [0107]-[0108].

P-MOS	NWPS Vdd=1. 05V	NTPS Vdd=0. 95V	Strong Vdd=0. 85V	Strong corner
	NWPT Vdd=1. 15V	Typical Vdd=1. 05V	NSPT Vdd=0. 95V	
	Weak Vdd=1. 2V	NTPW Vdd=1. 15V	NSPW Vdd=1. 05V	
Weak corner				N-MOS

FIG. 13

MTK-1004, FIG. 13.

Takahashi further explains that the “control signal S_C indicat[es] the operating condition of device 200,” *i.e.*, whether the device is in “operation (Active mode)” or “standby (Sleep mode).” *Id.*, [0109]-[0110], [0117]; *see also id.*, [0004], [0072]-[0073] (changing the values of similar “control signals S_{C1} and S_{C2} ” based on the operating status of the device), FIG. 18.

140. “FIGS. 14 and 15 show the voltage levels of source voltages V_{dd1} , V_{dd2} , and V_{dd3} generated by voltage regulator 100 according to the values of the respective bits of control data DAT set based on the process requirements of device 200 during operation (Active mode) and during standby (Sleep mode) and said control data.” *Id.*, [0110].

<u>Active</u> Mode	Bit 2	Bit 1	Bit 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0	0	0	1.2V	1.2V	1.20V	Weak
Fuse prog-1	0	0	1	1.15V	1.15V	1.15V	NTPW,NWPT
Fuse prog-2	0	1	0	1.05V	1.05V	1.05V	TYPC,NSPW,NWPS
Fuse prog-3	0	1	1	0.95V	0.95V	0.95V	NSPT,NTPS
Fuse prog-4	1	0	0	0.85V	0.85V	0.85V	Strong

FIG. 14

<u>Sleep</u> Mode	Bit 2	Bit 1	Bit 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0	0	0	0.7V	1.0V	0.7V	Weak
Fuse prog-1	0	0	1	0.7V	1.0V	0.7V	NTPW,NWPT
Fuse prog-2	0	1	0	0.7V	1.0V	0.7V	TYPC,NSPW,NWPS
Fuse prog-3	0	1	1	0.7V	1.0V	0.7V	NSPT,NTPS
Fuse prog-4	1	0	0	0.7V	1.0V	0.7V	Strong

FIG. 15

MTK-1004, FIGS. 14-15.

141. To put the power islands (e.g., “logic circuit 10” and “control circuit 70”) to sleep or take them out of sleep, “[v]oltage regulator 100 generates different levels of source voltages during operation and during standby according to said control data DAT and status control signal S_C and supplies them to device 200.” *Id.*, [0111].

142. As shown in Figures 14 and 15 of Takahashi, the same values of “DAT” data bits can result in different values for the outputs of voltage regulator 40. In other words, depending on whether the device is in the active or sleep state as indicated by the “control signal S_C,” the same “DAT” data bits result in different outputs of voltage regulator 40. In fact, as shown in Figures 14 and 15, voltage regulator 40 has 6 distinct states: 5 states for the active mode (5 rows in Figure 14) and one state for the sleep mode (because all 5 rows in Figure 15 have

the same voltage outputs). This clearly shows that voltage regulator 40 of Takahashi operates depending on the mode of the device (*i.e.*, whether the device is in the active mode or in the sleep mode), and only when the device is in the active mode, the three data bits can control the voltage regulator to output different voltages.

143. A POSITA would have therefore understood that Takahashi's "voltage regulator" employs a state machine. *See, e.g.*, MTK-1001, 6:19-21, 6:38-55; MTK-1008 (defining "state machine" as a "circuit containing several different states reachable from each other, with state changes happening synchronously"). For example, the 2001 textbook *Computer Systems Organization & Architecture* from John D. Carpinelli (MTK-1009) describes state machines in which "[i]nputs to the state machine are combined with the current state of the machine to determine the new state, or next state of the machine. Depending on the type of machine, outputs are generated based on either the state of the machine, or the state of the machine and the machine inputs." MTK-1009 at 51. In Takahashi, the "voltage regulator 100" of Figures 11-17 (and similarly, "voltage regulator 40" of Figures 1-5) determines its operable state (the different outputs for V_{dd1} , V_{dd2} , and V_{dd3}) based on the inputs "control data DAT and status control signal Sc ."

144. Based on the explanations above, in my opinion, a POSITA would have understood and found obvious that Takahashi's "voltage regulator" employs a state machine to control putting at least one power island to sleep (*i.e.*, "standby

state” or “Sleep mode”) and taking it out of sleep (*i.e.*, “operational state” or “Active mode”).

5. Claim 4

145. Claim 4 recites “[t]he method as claimed in claim 1 wherein the variable voltage is an optimum voltage.” In my opinion, Takahashi renders obvious claim 4 of the ’077 Patent.

146. As I explained with respect to element 1[b] above, Takahashi discloses and renders obvious a power manager that generates a variable voltage. For example, in the embodiment of Figures 1-5, Takahashi’s “voltage regulator 40” is a power manager that generates a variable “source voltage V_{dd} .” Likewise, in the embodiment of Figures 11-17 the “voltage regulator 100” is power manager that generates variable voltages including “source voltage V_{dd1} .”

147. Takahashi further discloses that the variable “source voltage” generated by the “voltage regulator” is set to “optimum values under the respective preset conditions according to control data DAT and control signal S_C indicating the operating status of device 200.” MTK-1004, [0117]; *see also id.*, [0099]-[0100], [0107], [0109]-[0111], [0123], FIGS. 13-15. Takahashi optimizes the variable “source voltage” based on the process variation indicated by “control data DAT” so that “the effect of variations in the production process can be reduced” and the “occurrence of leakage current is suppressed.” *Id.*, Abstract, [0109], [0116]-[0118], [0123]. Similarly, the voltage is optimized based on the

operating state indicated by “control signal S_C ” to reduce the leakage current during standby. *See, e.g., id.*, [0055]-[0057], Fig. 2.

148. Thus, in my opinion, a POSITA would have understood and found obvious that Takahashi’s variable voltage (*e.g.*, “ V_{dd} ” or “ V_{ddl} ”) is an optimum voltage.³

6. Claim 5

149. Claim 5 recites “[t]he method as claimed in claim 4 wherein the optimum voltage is dependent upon both process variation and temperature variation.” In my opinion, Takahashi renders obvious claim 5 of the ’077 Patent.

150. As I explained at element 1[b] and claim 4 above, the variable voltage outputs from Takahashi’s “voltage regulator” (*e.g.*, labelled “ V_{dd} ” in Figures 1-5 and “ V_{ddl} ” in Figures 11-17) are optimized for the operating state and performance of the integrated circuit device. In my view, a POSITA would have found it obvious in view of Takahashi to optimize the variable voltage outputs depending on both process variation and temperature variation.

151. As I explained with respect to Claim 4, Takahashi discloses optimizing the “source voltage” based on process variation so that “the effect of

³ It is my understanding that claim 4 does not require that the “variable voltage” is optimized based on temperature and/or process variations. This understanding comports with the claims in part because claim 5 separately recites that the “variable voltage” is optimized “dependent upon both process variation and temperature variation.” However, to the extent that the “variable voltage” of claim 4 must be optimized based on temperature and/or process variations, in my opinion Takahashi renders obvious claim 4 for the reasons stated here with respect to claim 4 and below with respect to claim 5.

variations in the production process can be reduced.” MTK-1004, [0117]; *see also id.* at [0099]-[0100], [0107], [0109]-[0111], [0123], FIGS. 13-17. That is, the voltage outputs from the “voltage regulator” are optimized based on the process used to fabricate the transistors in the device, including the “transistor MP0” in the “switching circuit 20,” to increase the “current driving capability” during operation and reduce leakage during standby. *See id.* at Abstract.

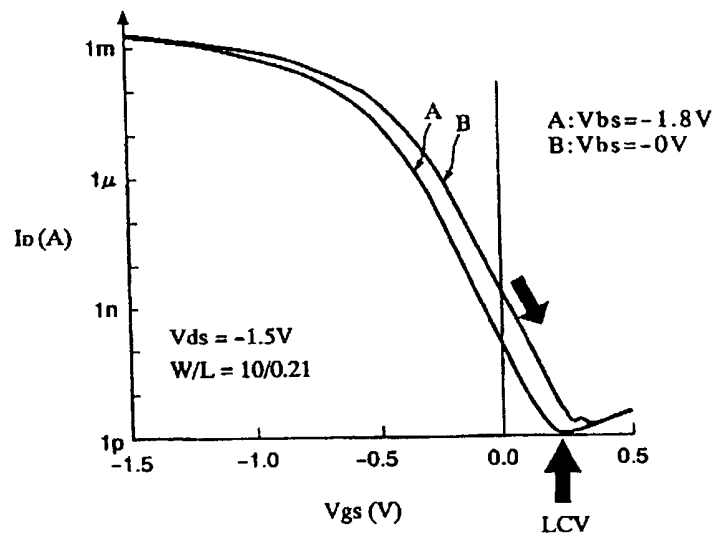


FIG. 2

MTK-1004, FIG. 2.

FIG. 2 is a graph showing the relationship between drain current I_D of pMOS transistor MP0 and gate-source voltage V_{gs} . In said graph, drain-source voltage V_{ds} of transistor MP0 is -1.5 V, for example. In addition, assume that channel width W of transistor MP0 is $10\mu\text{m}$, and channel length L is $0.21\mu\text{m}$.

As shown in FIG. 2, the drain current of the transistor changes in accordance with gate-source voltage V_{gs} . When gate-source voltage V_{gs} is of a specific value, for example, when V_{gs} is approximately 0.2 V, in FIG. 2, the drain current of transistor MP0 has a very low value. That is, a leakage current valley (LCV) is present. The

gate-source voltage at this time will be referred to as V_{gsV} hereinafter.

As described above, drain current I_D of transistor MP0 can be further reduced during standby bringing gate-source voltage V_{gs} up to V_{gsV} by controlling control signal S_G that is applied to the gate of transistor MP0 during standby. Thus, leakage current of logic circuit 10 can be reduced drastically. For example, when $V_{gs}=V_{gsV}$, drain current I_D of the transistor is reduced to approximately {fraction (1/700)} of that when gate-source voltage V_{gs} is 0 V.

Furthermore, the drain current can be further reduced by applying a voltage higher than the voltage applied to the source of transistor MP0 to its channel region during standby.

MTK-1004, [0054]-[0057]; *see also id.* at [0050].

152. A POSITA would have found it obvious to further optimize Takahashi's "source voltage" based on temperature variation to further reduce "leakage current" and improve device performance. Indeed, it was well-known at the time of the '077 Patent that transistor performance is dependent both on process variation and temperature variation. *See, e.g.*, MTK-1010, 1:37-2:14 ("Thus, it is known that varying supply voltage to a chip can improve performance by eliminating unexpected variability in the supply voltage, and by accounting for process and operating temperature variations."); MTK-1011, 12:18-21 ("the temperature dependency and any variation caused in manufacturing can be cancelled"); MTK-1012, 2:34-43, FIG. 2 ("leakage power in an integrated circuit increases exponentially as a function of temperature"); MTK-1013, 1:19-30 ("a sub threshold leakage of a metal-oxide semiconductor

field effect transistor (MOSFET) may be increased up to ten times when the temperature is raised from room temperature to 100° Celsius”); MTK-1014, 4:14-23 (“In some embodiments, the line regulation provided by the first feedback loop may filter input noise and compensate for process and temperature variations.”).

153. Thus, in my opinion, it would have been obvious to optimize the variable voltages generated by the power manager (*e.g.*, the “source voltage V_{dd} ” generated by “voltage regulator 40” or “source voltage V_{ddl} ” generated by “voltage regulator 100”) based on temperature variation in addition to process variation to (1) improve performance of the pMOS and nMOS transistors in the “switching circuit 20” and power islands (*e.g.*, “logic circuit 10”) and (2) further reduce power consumption due to leakage current during standby. A POSITA would have readily implemented these optimizations with predictable results and a reasonable expectation of success. For example, a POSITA would have been capable of adding a temperature sensor to Takahashi’s integrated circuit device and configuring the “voltage regulator” to optimize its “source voltage” outputs based on temperature in addition to the process variation indicated by “control data DAT” and “status control signal S_c .” MTK-1004, [0098]-[0117], FIGS. 11-17.

154. It is therefore my opinion that Takahashi renders obvious claim 5 of the ’077 Patent.

7. Claim 6

155. Claim 6 recites “[t]he method as claimed in claim 4 wherein the optimum voltage is generated by a sleep generator.” In my opinion, Takahashi renders obvious claim 6 of the ’077 Patent.

156. As I discussed above at elements 1[p] and 1[b] and claim 4, Takahashi’s “voltage regulator” discloses and renders obvious a power manager that generates an optimized variable voltage. Specifically, Takahashi’s “voltage regulator” is a power manager that generates an optimized variable voltage (*e.g.*, “V_{dd}” in Figures 1-5 and “V_{ddl}” in Figures 11-17) based on, among other things, whether the power island is in an operating state (“Active mode”) or standby state (“Sleep mode”). MTK-1004, [0110].

157. Specifically, during “standby (Sleep mode)”, Takahashi’s “voltage regulator” generates an optimum “source voltage” and provides it to the “switching circuit 20” to limit leakage current. *Id.*; *see* Claim 4. Figure 15, for example, provides exemplary values for the “source voltages V_{dd1}, V_{dd2}, and V_{dd3}” generated by the “voltage regulator 100” during “Sleep mode.”

Sleep Mode	Bit 2	Bit 1	Bit 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0	0	0	0.7V	1.0V	0.7V	Weak
Fuse prog-1	0	0	1	0.7V	1.0V	0.7V	NTPW,NWPT
Fuse prog-2	0	1	0	0.7V	1.0V	0.7V	TYPC,NSPW,NWPS
Fuse prog-3	0	1	1	0.7V	1.0V	0.7V	NSPT,NTPS
Fuse prog-4	1	0	0	0.7V	1.0V	0.7V	Strong

FIG. 15

MTK-1004, FIG. 15 (annotated).

158. Takahashi also discloses that the variable voltages provided during “Sleep mode” can be optimized to place the “switching circuit 20” transistor “MP0” into “super cut-off status” so that “leakage current during standby can be suppressed.” MTK-1004, [0009]-[0010].

Control signal S_G of different levels is applied to the gate of transistor MP0 during operation and during standby, respectively. Transistor MP0 is turned on or off according to the level of said control signal S_G . Furthermore, different levels are applied during operation and during standby, respectively, for the source voltage at the source of transistor MP0. In the prior art, the source voltage is kept at the same value during operation and during standby. However, in the case of the semiconductor integrated circuit of the present embodiment, source voltages V_{dd} and V_{dds} are switched depending on the condition of logic circuit 10. For example, during operation, source voltage V_{dd} is set to nominal operating voltage V_{ddN} of the transistor. During standby, the source voltage is set to value V_{ddL} , for example, $V_{ddL} = V_{ddN} - 0.3V$, slightly lower than V_{ddN} . As a result, the gate-source voltage of switching transistor MP0 acquires the opposite sign to that of the voltage during normal use in order to realize a super cut-off status.

MTK-1004, [0053]; *see also id.* at [0058], [0062], [0073], [0085], [0116]-[0118].

159. As I explained in my analysis of claim 4, Takahashi’s “[v]oltage regulator 100 generates different levels of source voltages ... during standby” so that “switching circuit 20 is in the super cut-off status during standby, and the occurrence of leakage current at logic circuit 10 is suppressed.” MTK-1004, [0111], [0116]. That is, Takahashi’s “voltage regulator” includes a voltage generation element for generating optimal voltages for putting the power islands

into “Sleep mode” and reducing leakage current. *See id.* While the ’077 Patent describes the “sleep generator” only briefly, a POSITA would have understood based on Takahashi’s disclosures that the voltage generation element of Takahashi’s “voltage regulator” is the claimed sleep generator. *See* MTK-1001, 5:8-67, FIGS. 3-4.

160. It is therefore my opinion that a POSITA would have understood and found obvious that Takahashi’s “voltage regulator” includes a sleep generator for generating the optimum voltage.

8. Claim 7

161. Claim 7 recites “[t]he method as claimed in claim 1 wherein the control signal is a digital signal.” In my opinion, Takahashi renders obvious claim 7 of the ’077 Patent.

162. As I explained at element 1[a] above, the “control signal Sc” is a control signal provided to the “voltage regulator” that is a power manager. Specifically, Takahashi’s “control circuit 30” transmits the “control signal Sc indicating the operating status of device 200,” *i.e.*, whether the device 200 is operating or in standby. MTK-1004, [0116]-[0117]. Takahashi’s “voltage regulator” receives the “control signal Sc” and generates “different levels of source voltages ... according to said control data DAT and status control signal Sc.” *Id.*, [0111]; *see also id.*, [0098].

163. In my opinion, a POSITA would have understood that Takahashi’s “control signal Sc” is a digital signal, and otherwise would have found it obvious

to use a digital signal for the “control signal S_C .” Takahashi explains that the “control signal S_C ” indicates one of two states of the “device 200”—either that it is in “operation (Active mode)” or “standby (Sleep mode).” Thus, the “control signal S_C ” is a binary signal. MTK-1004, Abstract, [0098], [0110]-[0111], [0116]-[0117]. For example, Takahashi’s related embodiments in Figures 6-7 and 8-9 include similar “control signals S_{C1} and S_{C2} ” that are sent to a “voltage switching circuit 50 [that is] provided in place of the volage regulator.” *Id.*, [0065], [0069]-[0074]. Like the “control signal S_C ,” the “control signals S_{C1} and S_{C2} ” take one of two values—either “the level of source voltage V_{ddN} ” or “ground potential GND.” *Id.* A POSITA would have understood that the binary “control signals S_{C1} and S_{C2} ” are digital signals, and similarly would have understood that Takahashi’s “control signal S_C ” that takes one of two values also is a digital signal. *See* MTK-1015 (defining “digital signal” as “[a]n electrical signal with two states—on or off, high or low, positive or negative—such as could be obtained from a telegraph key or two-position toggle switch”); MTK-1016 (defining “digital signal” as “an electric signal that has only a number of possible states, as opposed to an analog signal which is continuously variable”).

164. Moreover, Takahashi explains that the “control data DAT” provided to the “voltage regulator” is a digital signal with a specific “number of bits.” MTK-1004, [0098], [0101], [0104], [0109]-[0111], FIGS. 14-15. In my opinion, a POSITA would have found it obvious to use digital signals for both the “control data DAT” and “control signal S_C .” Such an implementation would be preferable

so that the “voltage regulator” selects the “source voltage” levels based solely on digital inputs, rather than on a mix of digital and analog inputs.

165. Further, all electrical signals fall into one of two categories—either they are digital or analog. As one of only two options, it would have been obvious to a POSITA for Takahashi’s “control signal S_c ” to be a digital signal.

166. Thus, in my opinion Takahashi discloses and renders obvious that the “control signal S_c ” is a digital signal.

9. Claim 8

167. Claim 8 recites “[t]he method as claimed in claim 1 wherein the at least one of the low leakage sleep circuits is connected in series to a source of a supply voltage and to a logic gate or storage cell of one of the power islands.” In my opinion, Takahashi renders obvious claim 8 of the ’077 Patent.

168. As I explained at element 1[b] above, it is my opinion that Takahashi’s “switching circuit 20” including the transistor “MP0” discloses and render obvious the claimed low leakage sleep circuit. It is also my opinion, as explained with respect to element 1[p], that Takahashi’s “logic circuit 10” discloses and renders obvious a power island.

169. As shown in the embodiments of Figures 1-5 and 11-17, Takahashi’s “switching circuit 20” is connected in series between the “voltage regulator” and “logic circuit 10.” MTK-1004, Abstract (“Switching circuit 20 is provided between logic circuit 10 and source voltage V_{dd} supply terminal.”). Takahashi’s “voltage regulator” regulates a system power supply (not shown) to generate the

“source voltages” that are provided to the “switching circuit 20.” MTK-1004, [0053], [0098]. Specifically, the “voltage regulator” provides the “switching circuit 20” with “source voltages V_{dd} and V_{dds} ” in the embodiment of Figures 1-5 and “ V_{ddl} ” in the embodiment of Figures 11-17. *Id.*⁴

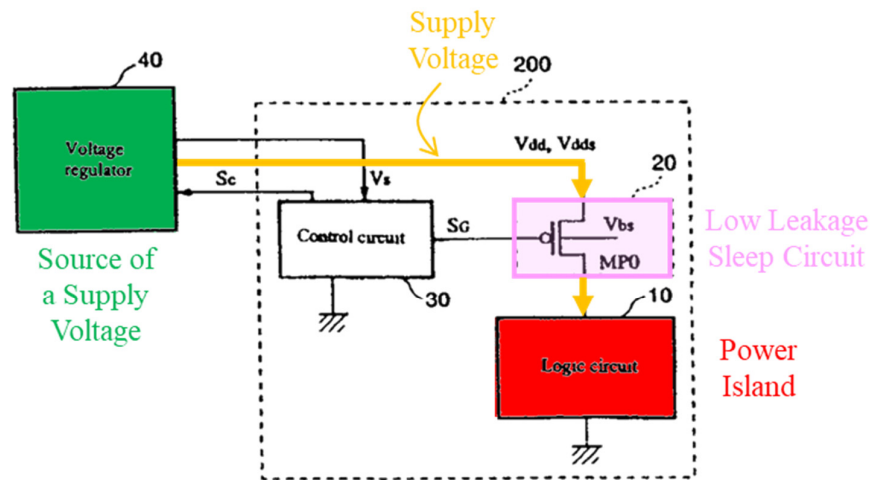


FIG. 1

MTK-1004, FIG. 1 (annotated).

⁴ Claim 9 of the '077 Patent further recites that the “at least one of the low leakage sleep circuits modifies the supply voltage to one of the power islands,” indicating that the “supply voltage” includes the entire voltage path from the source to the power island, including both the paths before and after the claimed low leakage sleep circuit.

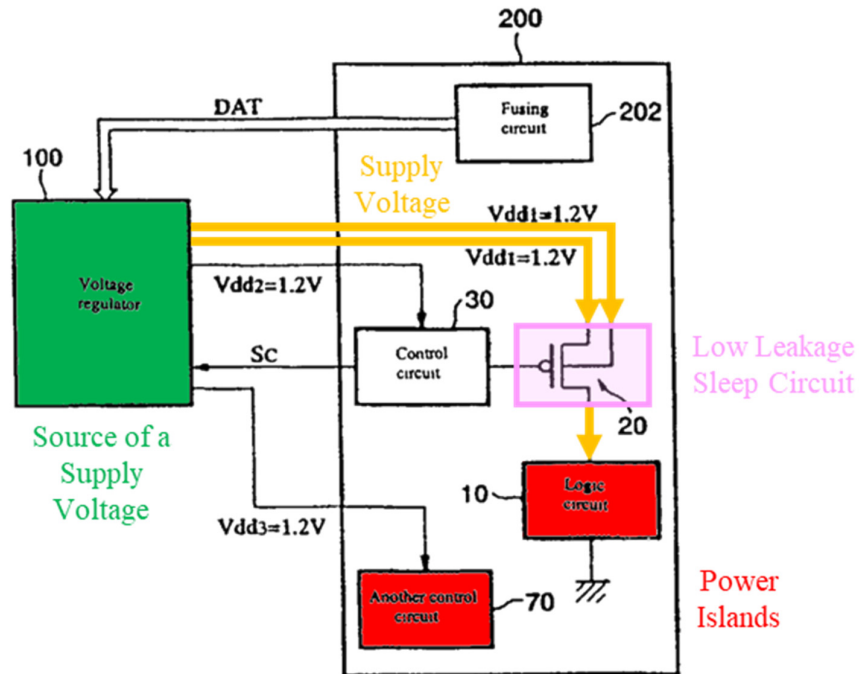


FIG. 16

MTK-1005, FIG. 16 (annotated).

170. As shown in Figure 1, “the source of transistor MP0” in the “switching circuit 20” “is connected to source voltage V_{dd} supply line, and its drain is connected to ... a virtual source voltage supply terminal of logic circuit 10. When transistor MP0 is conductive (on), source voltage V_{dd} is applied to node N1, and a driving current is supplied to logic circuit 10. On the other hand, when transistor MP0 is off (off), supply of current to logic circuit 10 is cut off.” MTK-1004, [0052]; *see also id.*, [0112]-[0116]. Thus, the “switching circuit 20” including “transistor MP0” is in series between the supply voltage and the power island.

171. Takahashi also discloses and renders obvious that the power islands such as “logic circuit 10” include a logic gate or storage cell. Takahashi discloses

that the “logic circuit 10 [has] a CMOS structure” that may include “a CMOS inverter configured with pMOS transistor MP1 and NMOS transistor MN1,” and/or “may consist of other kinds of logic circuits, such as an AND circuit, a NAND circuit, or an OR circuit.” MTK-1004, [0048], [0050]. Similarly, the related embodiment of Figure 10 discloses power islands including “[m]emories 210, 220, 270, and 280, logic circuit 230, microprocessor core 240, DSP core 250, and peripheral circuit 260 [that] are functional circuits to be operated using source voltage V_{dd} .” *Id.*, [0089]; FIG. 10.

172. Thus, in my opinion, a POSITA would understand that Takahashi’s “switching circuit 20” including the transistor “MP0” is connected in series to a source of a supply voltage and to a logic gate or storage cell of one of the power islands. It is therefore my opinion that Takahashi renders obvious claim 8.

10. Claim 9

173. Claim 9 recites “[t]he method as claimed in claim 8 wherein the at least one of the low leakage sleep circuits modifies the supply voltage to the one of the power islands during a sleep mode.” In my opinion, Takahashi renders obvious claim 9 of the ’077 Patent.

174. As I explained at elements 1[p] and 1[b], it is my opinion that each “switching circuit 20” including a “transistor MP0” is a low leakage sleep circuit and that the “logic circuit 10” is one of a plurality of power islands. Further, as I explained at claim 2, Takahashi’s power islands are put either into “operation (Active mode)” or “standby (Sleep mode).”

175. Takahashi discloses that the “switching circuit 20” lowers the supply voltage to the “logic circuit 10” during a “standby (Sleep mode).” MTK-1004, [0110]. Specifically, during “operation (Active mode),” the “switching circuit 20” having “transistor MP0” is “conductive (on) [such that] source voltage V_{dd} is applied to node N1, and a driving current is supplied to logic circuit 10.” MTK-1004, [0052], [0110]; *see also id.*, [0112]-[0116], FIGS. 14, 16. After transitioning to “Sleep mode,” the source voltage is lowered such that “transistor MP0 is off (off) [and] supply of current to logic circuit 10 is cut off.” *Id.*, [0052]; *see also id.*, [0112]-[0116], FIGS. 2-3, 14-17. Thus, Takahashi discloses that the “switching circuit 20” modifies the supply voltage provided to the “logic circuit 10” from an operating voltage (*e.g.*, as shown in Figures 14 and 16, when the “transistor MP0” is on) to a lower voltage during “standby (Sleep mode)” (*e.g.*, to a lower voltage when “transistor MP0” is off). *Id.*, [0110]-[0111].

176. Thus, it is my opinion that Takahashi discloses and renders obvious modifying the supply voltage to one of the power islands during a sleep mode.

11. Claim 10

(a) Element 10[p]

177. The preamble of claim 10 recites “[a] method carried out in an integrated circuit that includes an adaptive leakage controller, a power manager, a plurality of power islands and a plurality of low leakage sleep circuits, the method comprising.” Takahashi discloses and renders obvious the preamble of

claim 10 of the '077 Patent for at least the reasons discussed above with respect to element 1[p], the discussion of which I incorporate herein by reference.

(b) Element 10[a]

178. Element 10[a] recites “receiving, at the power manager, a control signal from the adaptive leakage controller.” Takahashi discloses and renders obvious element 10[a] for at least the reasons discussed above with respect to element 1[a], the discussion of which I incorporate herein by reference.

(c) Element 10[b]

179. Element 10[b] recites “employing the power manager to dynamically change power consumptions of the plurality of power islands, the employing the power manager to dynamically change power consumptions including: generating a variable voltage based on the control signal; and providing the variable voltage to the plurality of low leakage sleep circuits.” Takahashi discloses and renders obvious element 10[b] for at least the reasons discussed above with respect to element 1[b], the discussion of which I incorporate herein by reference.

(d) Element 10[c]

180. Element 10[c] recites “wherein each of low leakage sleep circuits is associated with leakage reduction of a respective one of the plurality of power islands.” In my opinion, Takahashi discloses and renders obvious element 10[c].

181. As I explained with respect to element 1[p] above, Takahashi’s “logic circuit 10” is a power island and the “switching circuit 20” is a low leakage

sleep circuit. Further, as explained at element 1[b], a POSITA would have found it obvious to include multiple instances of the “switching circuit 20” in the embodiments of Figures 1-5 and 11-17 of Takahashi.

182. Takahashi discloses that the “switching circuit 20” of the related embodiments of Figures 1-5 and 11-17 “suppresses the leakage current of the ... logic circuit 10 during standby.” MTK-1004, [0052]; *see also id.*, [0054]-[0059], [0062], [0116], [0118]. Similarly, Figure 10 of Takahashi discloses an embodiment in which the “switching circuit 20” includes “pMOS transistors 310, 320, ... , and 380” that can be turned off so that the “occurrence of a leakage current in the [respective] functional circuit can be suppressed.” *Id.*, [0090].

For example, when the test pattern is designed appropriately, data [logic] 0 is stored into flipflop 130, and data [logic] 1 is stored into all the other flip-flops. Under said condition, transistor 330 is on, and the other transistors are all off. Thus, driving current is supplied to logic circuit 230, and logic circuit 230 becomes operational. On the other hand, because no driving current is supplied to any functional circuits other than logic circuit 230, these functional circuits are all in the standby status. Furthermore, in a functional circuit in the standby status, because the transistor constituting the switching circuit is turned off to cut off the leakage current path, occurrence of a leakage current can be suppressed.

MTK-1004, [0092].

183. Thus, Takahashi discloses to a POSITA, and otherwise renders it obvious, that each “switching circuit 20” in Takahashi’s integrated circuit has an

associated leakage reduction for a respective “logic circuit 10” or other power island.

184. Thus, in my opinion, Takahashi discloses and renders obvious that each “switching circuit 20” is a low leakage sleep circuit associated with a leakage reduction of a respective one of the plurality of power islands.

12. Claim 11

185. Claim 11 recites “[t]he method as claimed in claim 10 further comprising putting to sleep and taking out of sleep, at different times, at least one of the power islands.” Takahashi renders obvious claim 11 for at least the reasons discussed above with respect to claim 2 and claim 10, the discussion of which is incorporated herein by reference.

13. Claim 12

186. Claim 12 recites “[t]he method as claimed in claim 11 wherein the power manager employs a state machine to control the putting to sleep and the taking out of sleep.” Takahashi renders obvious claim 12 for at least the reasons discussed above with respect to claim 3, claim 10, and claim 11, the discussion of which is incorporated herein by reference.

14. Claim 13

187. Claim 13 recites “[t]he method as claimed in claim 10 wherein the variable voltage is an optimum voltage.” Takahashi renders obvious claim 13 for at least the reasons discussed above with respect to claim 4 and claim 10, the discussion of which is incorporated herein by reference.

15. Claim 14

188. Claim 14 recites “[t]he method as claimed in claim 13 wherein the optimum voltage is dependent upon both process variation and temperature variation.” Takahashi renders obvious claim 14 for at least the reasons discussed above with respect to claim 5, claim 10, and claim 13, the discussion of which is incorporated herein by reference.

16. Claim 15

189. Claim 15 recites “[t]he method as claimed in claim 13 wherein the optimum voltage is generated by a sleep generator.” Takahashi renders obvious claim 15 for at least the reasons discussed above with respect to claim 6, claim 10, and claim 13, the discussion of which is incorporated herein by reference.

17. Claim 16

190. Claim 16 recites “[t]he method as claimed in claim 10 wherein the control signal is a digital signal.” Takahashi renders obvious claim 16 for at least the reasons discussed above with respect to claim 7 and claim 10, the discussion of which is incorporated herein by reference.

18. Claim 17

191. Claim 17 recites “[t]he method as claimed in claim 10 wherein at least one of the low leakage sleep circuits is connected in series to a source of a supply voltage and to a logic gate or storage cell of an associated one of the power islands.” Takahashi renders obvious claim 17 for at least the reasons discussed

above with respect to claim 8 and claim 10, the discussion of which is incorporated herein by reference.

19. Claim 18

192. Claim 18 recites “[t]he method as claimed in claim 17 wherein the at least one of the low leakage sleep circuits modifies the supply voltage to the associated one of the power islands during a sleep mode.” Takahashi renders obvious claim 18 for at least the reasons discussed above with respect to claim 9, claim 10, and claim 17, the discussion of which is incorporated herein by reference.

B. Analysis of Takahashi in View of Ko with Respect to Claims 3 and 12

193. For the reasons articulated in detail below, and based on my review of the '077 Patent, and the Mizuno and Ko references, it is my opinion that a POSITA would have readily understood that the combination of Mizuno and Ko renders obvious claims 3 and 12 of the '077 Patent.

1. Overview of Ko

194. Ko is titled “Retention System for System-Transparent State Retention.” MTK-1006, Title. Ko explains that the Field of the Invention “relates generally to digital integrated circuits and, more particularly, to reducing leakage current in power-saving standby modes of digital integrated circuit operation.” *Id.*, 1:14-17. Ko explains that leakage current was a well-known problem in the industry at the time.

The demand for higher clock-rates and lower power supply voltages in digital integrated circuits such as CMOS circuits results in rapidly increasing levels of standby leakage current (i.e., the current consumed by a CMOS circuit when the clock is not active). As an example, multi-million gate I.C.s operating in the Gigahertz region with supply voltages below 1.5V can have standby leakage of 100mA or higher. This level of leakage current represents a significant problem for portable (battery operated) applications. This problem is conventionally addressed by introducing products that feature state-retentive, low-leakage standby modes.

MTK-1006, 1:21-38.

195. Ko also discusses known solutions for implementing low-power standby modes that reduce power consumption due to leakage currents while also retaining necessary data. Specifically, Ko explains that known solutions for implementing “low-leakage standby modes” with data retention would use “state retention flip-flops [to] store the status of operation of the circuit ... in latches with low leakage current during power-down phase.” *Id.*, 1:39-56. “The retention latch (called a shadow latch hence forth) is formed with thick-oxide (low leakage) transistors and is powered by a separate permanent power supply to retain data in power-down or retention mode.” *Id.* To retain data in the shadow latches during standby, Ko explained that conventional approaches had “two [power] supplies, a permanent supply for retention and a virtual supply for conventional logic power.” *Id.*, 1:57-2:2.

196. However, Ko acknowledges that “[t]his architecture has limitations” because “[b]oth supplies must be present for normal operation,” which

“introduces a physical design overhead of routing an additional power rail to all the registers.” *Id.* Ko also explains that “[s]ome disadvantages of such a scheme are: the additional circuitry required for such a shadow latch implementation is magnified at chip level when a large number of retention flip-flops are required; generation of additional control signals required to drive the flip-flop in and out of retention mode not only increase the flip-flop area, but also pose routing problems at block level; and additional shadow latch and control circuitry can load the speed-critical path of the flip-flop worsening the propagation delay of the flip-flop.” *Id.*, 1:39-56.

197. Thus, Ko developed a system and method of implementing “low-leakage standby modes” with data retention “which avoid the aforementioned disadvantages of conventional approaches.” *Id.*, 2:3-5. Figure 1 of Ko illustrates such a system. Specifically, Figure 1 depicts a power switching arrangement in which “a suitable transistor is provided as a header switch for selectively (in response to the signal UP/DN) connecting and disconnecting the module level power supply VDD to and from the chip level (permanent) power supply VCC.” *Id.*, 2:63-3:6. Ko’s system also includes a “separate power supply VRETAIN” for powering the “shadow latches” that “retain[] data while power is removed” from the functional circuitry in the “logic block.” MTK-1006, 2:63-3:34.

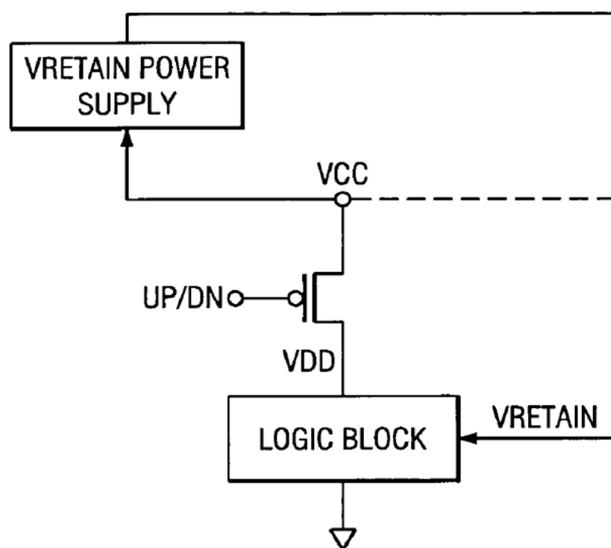


FIG. 1

MTK-1006, FIG. 1.

198. Ko explains that this basic structure can be applied to systems with multiple logic blocks that can be powered-down (*i.e.*, put into standby) independently of other logic blocks. MTK-1006, 9:51-63, FIG. 11. For example, Figure 4 depicts an example where Ko’s power switching arrangement is used in a “wireless communication apparatus,” *e.g.*, a mobile phone. MTK-1006, 7:20-50, 7:64-8:2.

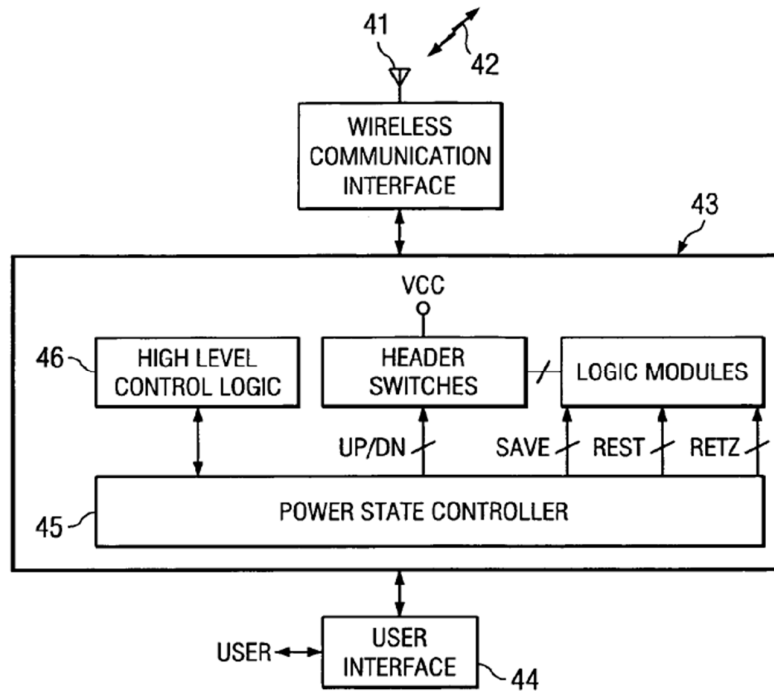


FIG. 4

MTK-1006, FIG. 4.

199. Ko explains that the “wireless communication apparatus” has a “data processing apparatus 43 [that] can perform data processing operations related to the communications on air interface 42.” MTK-1006, 7:20-31. The “data processing apparatus 43” includes “header switches” and “a plurality of logic modules ... for performing data processing operations.” *Id.*, 7:32-50. “The data processing apparatus 43 further includes a power state controller 45 which, in some embodiments, utilizes state machines to provide appropriate control signals to the header switches and logic modules.” *Id.*

200. Specifically, “the power state controller provides control signals UP/DN to the respective header switches, and provides control signals REST, RETZ ... and SAVE for distribution to each of the logic modules.” *Id.* As

explained above, the UP/DN control signal in particular is used to turn the header switches on and off so that the logic modules are connected or disconnected from the power supply VCC. *Id.*, 2:63-3:6, 7:32-50. The other signals “REST, RETZ ... and SAVE” are used for data retention during standby modes. For example, Figure 5 of Ko “is a timing diagram which illustrates the timing relationship of the control signals produced by the power state controller 45.” *Id.*, 7:51-53.

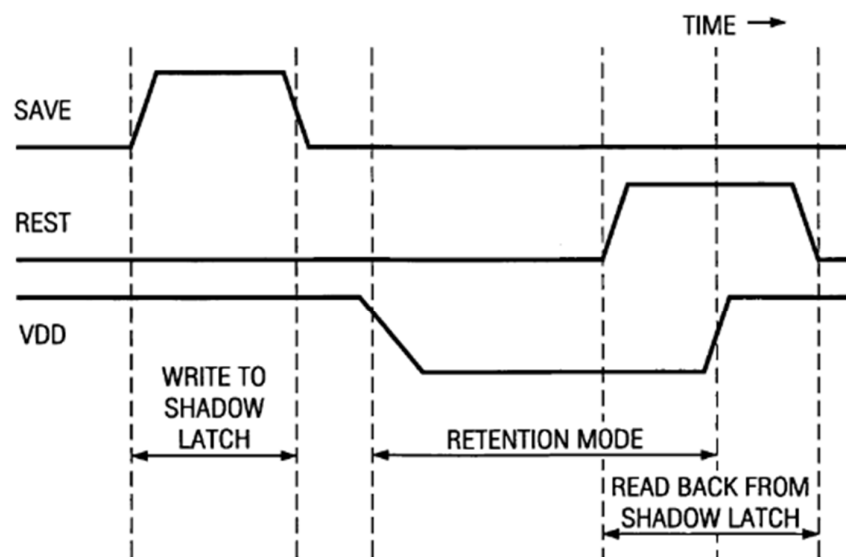


FIG. 5

MTK-1006, FIG. 5.

201. Ko explains that “the VDD waveform of FIG. 5 generally timewise corresponds to activation (VDD on) and inactivation (VDD off) of the UP/DN signal of FIG. 4.” MTK-1006, 7:53-55. The other signals including the “SAVE” signal and “REST” (*i.e.*, “restore”) signal are used to retain data when transitioning between operational and low-power standby states.

2. Combination of Takahashi and Ko

202. In my opinion, a POSITA would have been motivated to combine Takahashi with Ko.

203. As an initial matter, a POSITA would have been motivated to combine Takahashi and Ko because both are assigned to Texas Instruments Inc. and directed to technologies in the same field of endeavor. *Id.* Specifically, both Takahashi and Ko relate to reducing power consumption in integrated circuits, and in particular, reducing power consumption due to leakage currents, which is of particular concern in portable device applications. MTK-1004, Title, Abstract, [0001] (“The present invention pertains to a semiconductor integrated circuit, for example, a semiconductor integrated circuit by which power consumption can be reduced by suppressing leakage current.”), [0002] (discussing the invention’s application to “mobile communication terminals, compact solid-state audio players, and portable semiconductor devices, such as laptop personal computers”); MTK-1006, 1:14-17 (“The invention relates generally to digital integrated circuits and, more particularly, to reducing leakage current in power-saving standby modes of digital integrated circuit operation.”), 3:7-34, 7:20-50 (describing a “wireless communication apparatus according to the invention”), 9:2-4, 9:42-50. As I explained above, the ’077 Patent is in this same field of endeavor in that it is also concerned with reducing power consumption due to leakage currents. *See* MTK-1001, Title, Abstract, 1:29-39.

204. A POSITA also would have been motivated to combine Takahashi and Ko because both address the same known power consumption problem, and

do so in the same way. Specifically, both Takahashi and Ko reduce overall power consumption by putting circuit blocks of an integrated circuit into a low-power standby mode when not in use. *See, e.g.*, MTK-1004, [0017], [0052]-[0053], [0094]-[0095]; MTK-1006, 1:20-56, 2:63-3:6. Furthermore, Takahashi and Ko both use MOS transistors as switches to limit power to the circuit block when in standby, and to provide an operational power supply to the circuit block when it is in use.

In FIG. 1, switching circuit 20 is configured with pMOS transistor MP0. Transistor MP0 has a threshold voltage either equal to or higher than that of the low threshold transistor constituting the logic circuit, and said threshold voltage is -0.2V , for example.

Switching circuit 20 supplies an operating current to logic circuit 10 during operation and suppresses the leakage current of the low threshold voltage transistor of logic circuit 10 during standby. As shown in FIG. 4, in switching circuit 20, the source of transistor MP0 is connected to source voltage V_{dd} supply line, and its drain is connected to node N1. In other words, node N1 is a virtual source voltage supply terminal of logic circuit 10. When transistor MP0 is conductive (on), source voltage V_{dd} is applied to node N1, and a driving current is supplied to logic circuit 10. On the other hand, when transistor MP0 is off (off), supply of current to logic circuit 10 is cut off. Thus, generation of a leakage current at logic circuit 10 is suppressed.

MTK-1004, [0051]-[0052].

FIG. 1 diagrammatically illustrates a power switching arrangement according to exemplary embodiments of the invention. As shown in FIG. 1, a suitable transistor is provided as a header switch for selectively (in response to the signal UP/DN) connecting and disconnecting the module level power supply VDD to

and from the chip level (permanent) power supply VCC. The module level power supply VDD provides operating power for a logic module that includes state retention registers according to the invention. VDD is connected to VCC when UP/DN is activated, and is disconnected from VCC when UP/DN is inactivated.

MTK-1006, 2:63-3:6.

205. Takahashi and Ko also both teach modifying the voltages applied to the MOS switches and the circuit blocks in the integrated circuit during operation and standby to limit power consumption due to leakage currents. MTK-1004, [0052], [0112]-[0116]; MTK-1006, 4:1-24, 7:32-55.

206. In my opinion, these similarities between Takahashi and Ko—along with their common ownership by Texas Instruments Inc.—would have motivated a POSITA to employ Ko’s state machine with Takahashi’s “voltage regulator.”⁵ Doing so would have improved Takahashi’s ability to reduce power consumption in its integrated circuit device, including power consumption due to leakage currents.

207. For example, in the embodiment of Figures 11-17, Takahashi discloses that the “[v]oltage regulator 100 controls the levels of source voltages V_{dd1} , V_{dd2} , and V_{dd3} supplied to device 200 using predetermined optimum values according to control signal S_C indicating control data DAT and the operating

⁵ As I explained in my analysis of claim 3 above, it is my opinion that Takahashi by itself discloses and renders obvious employing a state machine. However, to the extent that Takahashi alone fails to render claim 3 obvious, it is my opinion that Takahashi in combination with Ko renders obvious employing a state machine as recited by claim 3.

condition of the device.” MTK-1004, [0109]. When the “status control signal S_C ” indicates that the “device 200” is operational, the “voltage regulator 100” outputs voltages as shown in Figures 14 and 16. *Id.*, [0112]-[0117]. On the other hand, when the “status control signal S_C ” indicates that the “device 200” is in standby, the “voltage regulator 100” outputs the reduced voltages shown in Figures 15 and 17. *Id.*

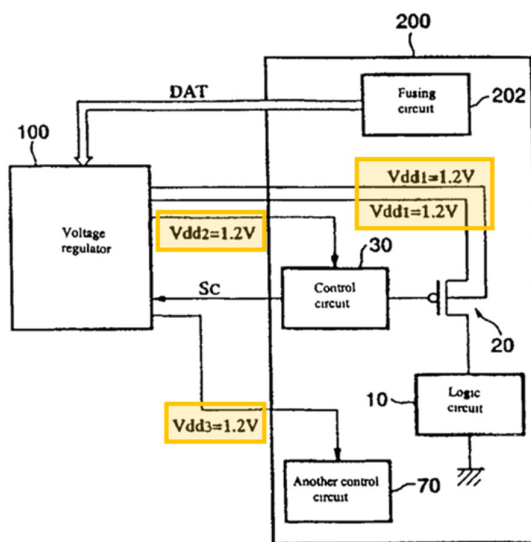


FIG. 16

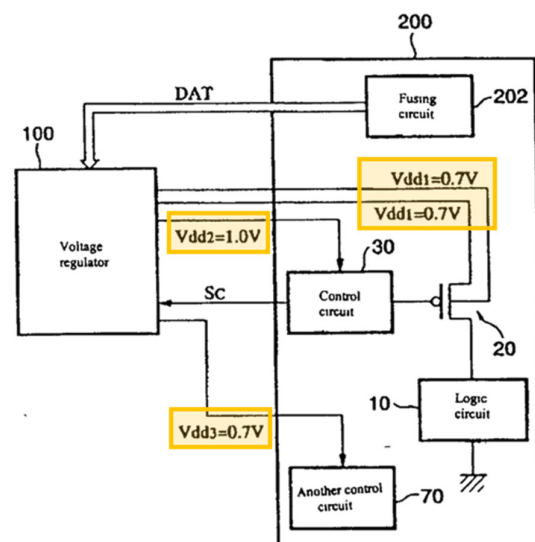


FIG. 17

MTK-1004, FIGS. 16-17 (annotated).

208. To the extent that Takahashi’s “voltage regulator” does not itself disclose or render obvious employing a state machine to change the output states of the “source voltages” (e.g., “ V_{dd1} , V_{dd2} , and V_{dd3} ”), it would have been obvious to do so in view of Ko. Moreover, a POSITA would have understood that not all of the circuits in Takahashi’s “device 200” require power at all times, even when the “device 200” itself is operating. For example, in the embodiment of Figures 11-17, “source voltage V_{dd3} ” is provided to “another control circuit 70” that has

“Wake up logic.” MTK-1004, [0112]-[0117], FIGS. 14-17. In my opinion, a POSITA would have understood (as its name suggests) that the “Wake up logic” is only operated while the “device 200” is returning to the operational state from the “standby (Sleep mode).” Thus, a POSITA would have understood that the “Wake up logic” can be returned to a standby state after it completes its “wake up” function. In Takahashi, however, even after the “Wake up logic” completes its function, the “voltage regulator” in Takahashi continues to provide it with an operational “source voltage V_{dd3} .” Thus, while Takahashi’s system addresses power consumption and reduces leakage current, a POSITA would have understood that it was capable of improvement to further reduce overall power consumption. MTK-1004, [0110]-[0117].

209. Additionally, as I explained in my analysis of elements 1[p] and 1[b] above, a POSITA would have found it obvious for Takahashi’s “device 200” to include additional power islands, such as other memories, logic circuits, microprocessor cores, DSP cores, or peripheral circuits as shown in Takahashi’s Figure 10. MTK-1004, [0087]-[0095]. Like the “Wake up logic” above, a POSITA would have understood that some power islands could be powered down during operation of the “device 200” to conserve power. For example, a POSITA would have understood that certain processor or DSP cores could be put into a standby state when not in use, and that peripheral circuits are often able to be powered down when they are inactive.

210. A POSITA would have understood that Ko provides the capability to selectively power down specific circuits within the device that is absent from Takahashi. MTK-1006, 2:63-3:6, 7:20-50. For example, Ko discloses a “wireless communication apparatus” having “a plurality of logic modules that include logic for performing data processing operations.” MTK-1006, 7:32-50. To conserve power in Ko’s device, a “power state controller 45 ... utilizes state machines” to power down “logic modules” when they are not in use. *Id.*, 2:63-3:6, 7:32-50, 9:42-50 (“Referring again to FIG. 4, in some applications, it may be desirable to power-down one or more of the logic modules independently of the remaining logic modules, in order to reduce current consumption.”).

FIG. 4 diagrammatically illustrates pertinent portions of exemplary embodiments of a wireless communication apparatus according to the invention. The wireless communication apparatus of FIG. 4 includes an antenna structure 41 for permitting communication via an air interface 42. A data processing apparatus 43 can perform data processing operations related to the communications on air interface 42. A wireless communication interface can utilize conventional techniques to interface the data processing apparatus 43 to the antenna structure 41. A user interface 44 can use conventional techniques to interface the data processing apparatus 43 to a user of the wireless communication apparatus.

The data processing apparatus 43 includes a plurality of logic modules that include logic for performing data processing operations, and state retention registers for storing data associated with the data processing operations. These registers are constructed from corresponding pluralities of state retention flip-flops, for example the state retention flip-flops illustrated in FIGS. 2, 3 and 8–10. The data processing apparatus 43

further includes a power state controller 45 which, in some embodiments, utilizes state machines to provide appropriate control signals to the header switches and logic modules. As shown in FIG. 4, the power state controller provides control signals UP/DN to the respective header switches, and provides control signals REST, RETZ (described hereinbelow) and SAVE for distribution to each of the logic modules. The power state controller 45 activates these control signals appropriately to implement the exemplary operations described above with respect to FIGS. 2, 3 and 8–10.

MTK-1006, 7:20-50.

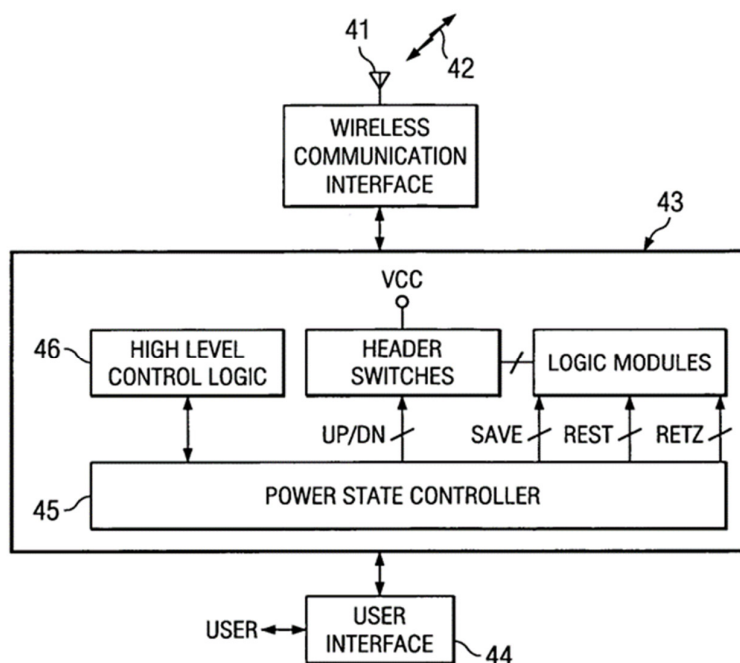


FIG. 4

MTK-1006, FIG. 4.

211. Because Takahashi and Ko are commonly owned references that provide a similar solution (*i.e.*, the use of MOS switches to place power islands into standby modes) to a similar problem (*i.e.*, power consumption, and in particular power consumption due to leakage currents), a POSITA would have

been motivated to combine the two references to further reduce the power consumption in Takahashi's system. Specifically, a POSITA would have naturally looked to employ Ko's "state machine" in Takahashi's "voltage regulator" to selectively power down circuits in Takahashi's "device 200." By selectively putting certain circuits into "standby (Sleep mode)," overall power consumption of the device is reduced, thereby addressing the problem of extending battery life in mobile devices. MTK-1004, [0002]; MTK-1006, 1:21-31.

212. In my opinion, a POSITA would have readily implemented Ko's "state machine" with Takahashi's "voltage regulator" to control the power state of individual circuits with a reasonable expectation of success. At the time of the '077 Patent, the use of state machines already was a well-known solution for efficiently controlling an integrated circuit. As such, a POSITA would have needed only routine electrical and computer engineering principles to employ a state machine with Takahashi's "voltage regulator." As just one example, a POSITA would have understood how to use Ko's "state machine" to set the individual "source voltages V_{dd1} , V_{dd2} , and V_{dd3} " to the appropriate levels for an operational or standby state depending on whether the respective circuits powered by those "source voltages" were in use. Doing so would require the same level of programming as in Ko, where "state machines" are used to "provide appropriate control signals to the header switches and logic modules" to put them into operational or standby states. MTK-1006, 7:38-43. Combining Ko with

Takahashi in this way would predictably reduce the overall power consumption of Takahashi's "device 200," by reducing the power consumption of individual circuits that are put into "standby (Sleep mode)" even while other circuits in the "device 200" remain operational.

213. Therefore, it is my opinion that a POSITA would have been motivated to combine Takahashi with Ko and would been capable of doing so with a reasonable expectation of success.

3. Claim 3

214. Claim 3 recites "[t]he method as claimed in claim 2 wherein the power manager employs a state machine to control the putting to sleep and the taking out of sleep." In my opinion, to the extent that Takahashi alone does not render obvious claim 3, the combination of Takahashi and Ko renders obvious claim 3.

215. Ko discloses a "power switching arrangement" in which "a suitable transistor is provided as a header switch for selectively (in response to the signal UP/DN) connecting and disconnecting the module level power supply VDD to and from the chip level (permanent) power supply VCC." MTK-1006, 2:63-3:6.

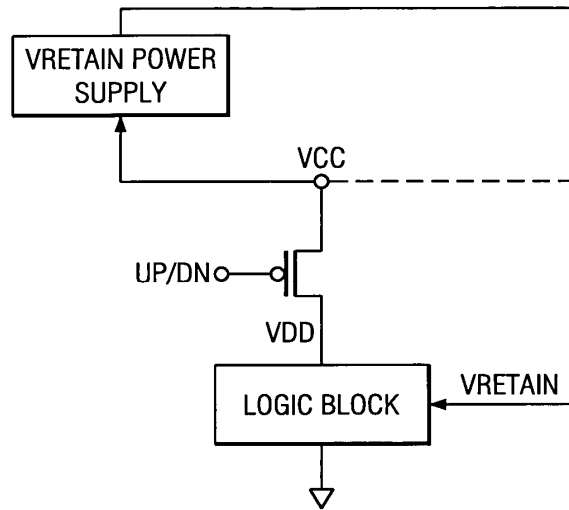


FIG. 1

MTK-1006, FIG. 1.

216. Notably, Ko’s use of a “header switch” is similar, as shown below, to Takahashi’s use of the “switching circuit 20” to connect and disconnect power from its “logic circuit 10.” See MTK-1004, [0051]-[0053].

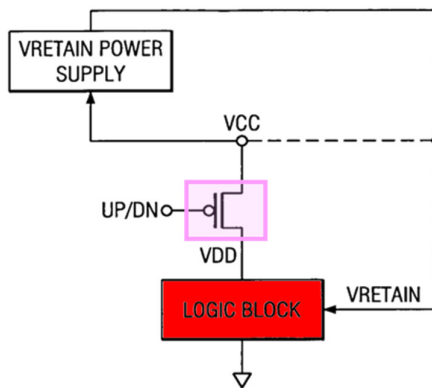


FIG. 1

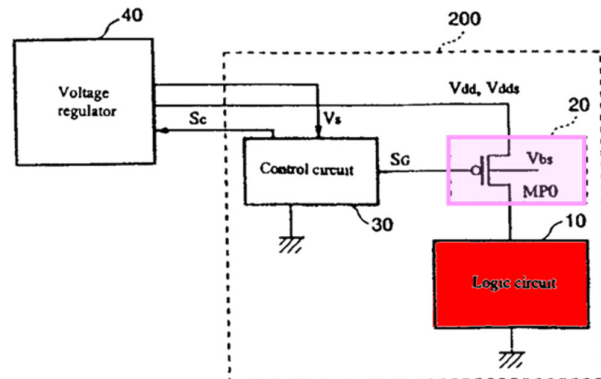


FIG. 1

MTK-1006, FIG. 1 (annotated, left); MTK-1004, FIG. 1 (annotated, right).

217. Ko discloses that its power switching technique can be applied to “a wireless communication apparatus” having multiple logic modules, so that it may

“power-down one or more of the logic modules independently of the remaining logic modules, in order to reduce current consumption.” *Id.*, 7:20-50, 9:42-63, FIG. 4. To do so, Ko’s “wireless communication apparatus” includes a “power state controller 45” that “utilizes state machines to provide appropriate control signals to the header switches and logic modules.” *Id.*, 7:38-42. “The power state controller 45 activates these control signals appropriately” so that the logic modules in use receive power while unused logic modules are put into a low-power standby mode. *Id.*, 7:32-50. Ko shows the “power state controller 45” in Figure 4, below. There, the “power state controller provides control signals UP/DN to the respective header switches” to connect and disconnect the logic modules from the system power “VCC.” *Id.*, 7:42-47; *see also id.*, FIG. 1.

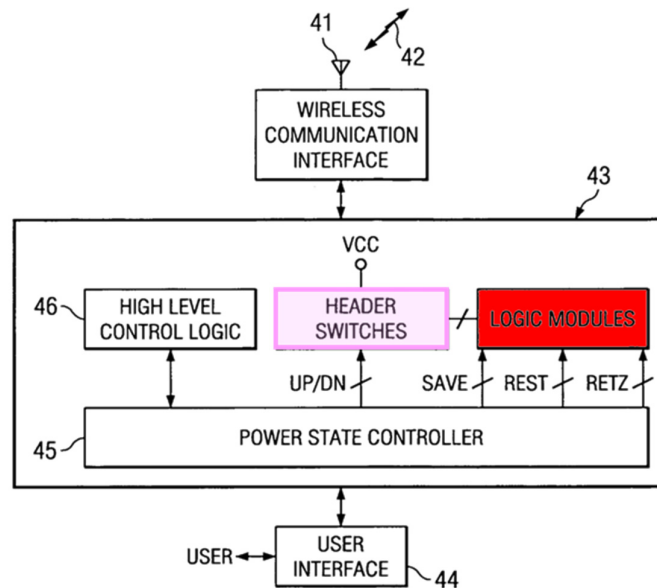


FIG. 4

MTK-1006, FIG. 4 (annotated).

218. Based on Ko's teachings, a POSITA would have found it obvious to employ a state machine in Takahashi's "voltage regulator." Doing so would enable Takahashi's system to conserve additional power by putting individual circuits in the "device 200" into standby when not in use, even while other circuits in the "device 200" remain operational. For instance, Takahashi's "voltage regulator 100" would employ Ko's "state machine" to provide "source voltage V_{dd3} " at 1.2V to the "Wake up logic" of "control circuit 70" when the "device 200" is coming out of standby, and to lower "source voltage V_{dd3} " to the standby level of 0.7V once it has completed its "Wake up" function, even while other circuits in the "device 200" remain operational. MTK-1004, [0110]-[0117], FIGS. 14-17.

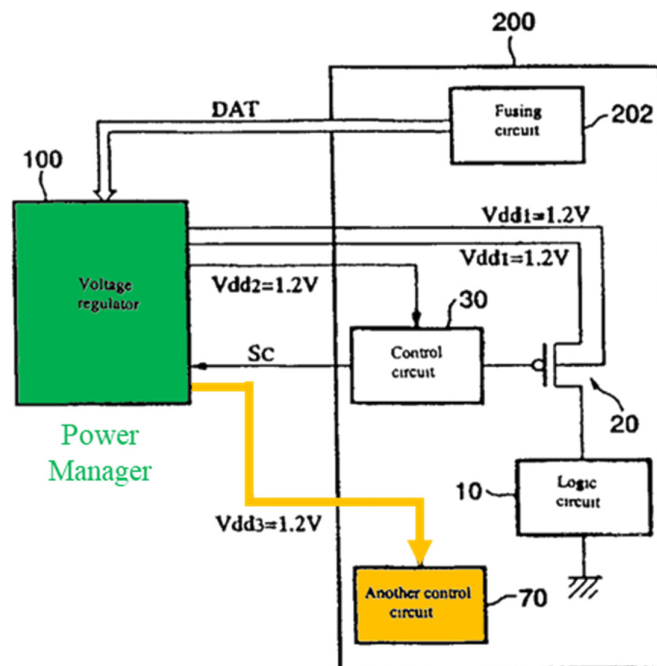


FIG. 16

MTK-1004, FIG. 16 (annotated).

Active Mode	Bit 2	Bit 1	Bit 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0	0	0	1.2V	1.2V	1.20V	Weak
Fuse prog-1	0	0	1	1.15V	1.15V	1.15V	NTPW,NWPT
Fuse prog-2	0	1	0	1.05V	1.05V	1.05V	TYPC,NSPW,NWPS
Fuse prog-3	0	1	1	0.95V	0.95V	0.95V	NSPT,NTPS
Fuse prog-4	1	0	0	0.85V	0.85V	0.85V	Strong

FIG. 14

Sleep Mode	Bit 2	Bit 1	Bit 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0	0	0	0.7V	1.0V	0.7V	Weak
Fuse prog-1	0	0	1	0.7V	1.0V	0.7V	NTPW,NWPT
Fuse prog-2	0	1	0	0.7V	1.0V	0.7V	TYPC,NSPW,NWPS
Fuse prog-3	0	1	1	0.7V	1.0V	0.7V	NSPT,NTPS
Fuse prog-4	1	0	0	0.7V	1.0V	0.7V	Strong

FIG. 15

MTK-1004, FIGS. 14-15 (annotated).

219. In my opinion, a POSITA would have had a reasonable expectation of success in combining Ko with Takahashi in this way. As discussed above, it would have required a simple modification of Takahashi's "voltage regulator" to employ Ko's "state machine" for controlling the putting to sleep and taking out of sleep of the "logic circuit 10," "control circuit 70," and other power islands. Employing Ko's "state machine" in this way would have required merely routine electrical or computer programming knowledge and was a task well within the skill of a POSITA. *Id.*

220. Additionally, integrating Ko's "state machine" to power-down unused circuits while other circuits of the "device 200" remain in operation would have had the predictable effect of reducing the overall power consumption of the "device 200." Thus, incorporating Ko's "state machine" with Takahashi's

“voltage regulator” would improve Takahashi’s ability to “reduce the power consumption in order to allow [mobile communication terminals] to operate for a long time.” MTK-1004, [0002].

221. It is therefore my opinion that the combination of Takahashi and Ko renders obvious claim 3.

4. Claim 12

222. Claim 12 recites “The method as claimed in claim 11 wherein the power manager employs a state machine to control the putting to sleep and the taking out of sleep.” To the extent that Takahashi alone does not render obvious claim 12, the combination of Takahashi and Ko renders obvious claim 12 for at least the reasons discussed above with respect to claim 3, the discussion of which is incorporated herein by reference.

C. Analysis of Takahashi in View of Schutz with Respect to Claims 5 and 14

223. For the reasons articulated in detail below, and based on my review of the ’077 Patent, and the Takahashi and Schutz references, it is my opinion that a POSITA would have readily understood that the combination of Takahashi and Schutz renders obvious claims 5 and 14 of the ’077 Patent.

1. Overview of Schutz

224. Schutz is titled “Integrated Circuit Device that Selects Its Own Supply Voltage by controlling a Power Supply.” Schutz defines the Field of the Invention as “supplying electrical power to circuits, and more specifically to integrated circuit devices that select their own supply voltage by controlling a

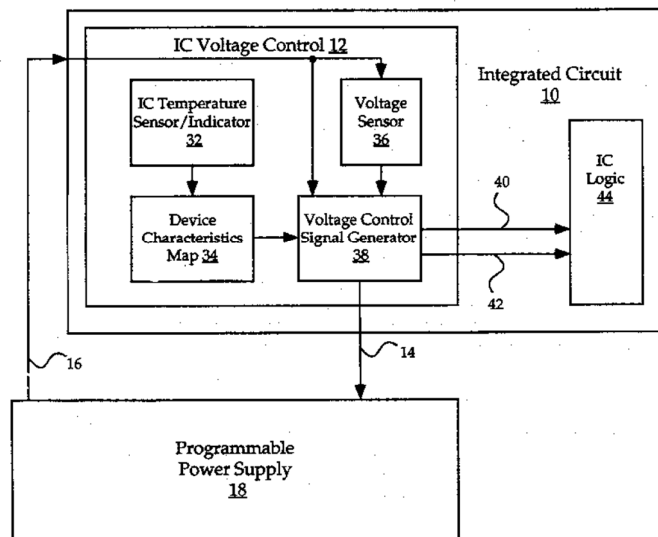
separate power supply.” MTK-1007, 1:7-11. Schutz issued in 1995 to Intel Corporation.

225. Schutz explains that its “invention addresses two problems associated with the operational voltage (i.e., the power supply voltage) of today’s microprocessors and other integrated circuit devices (ICs).” *Id.*, 1:7-36. First, Schutz states that its invention addresses problems associated with reducing the operational voltage of integrated circuits. Schutz explains that while “the operational voltages of today’s microprocessors are progressively being decreased in order to optimize performance and reduce power consumption,” doing so “poses problems for both computer system manufacturers and microprocessor manufacturers” that have to build their systems to operate with lower voltages. *Id.*, 1:16-26, 1:37-2:7. Second, Schutz states that its invention addresses problems associated with meeting device performance requirements in the presence of temperature and other variations. Schutz explains that “[h]aving to guarantee microprocessor operation over a full range of supply voltages and temperatures unduly limits the upper frequency specification because only certain supply voltage and temperature combinations exhibit slower performance.” *Id.*, 1:26-36, 2:8-42.

226. To address these challenges, Schutz developed an “integrated circuit device 10 [that] selects the supply voltage 16 based on a plurality of predetermined operational voltages and the temperature of integrated circuit

device 10.” *Id.*, Abstract, 6:31-35. Schutz depicts an example of this system in Figure 2.

Figure 2



MTK-1007, FIG. 2.

227. The “integrated circuit 10” of Figure 2 has an “IC voltage control circuit 12 [that] includes an IC temperature sensor circuit 32, a device characteristics map 34, a voltage sensor circuit 36, and a voltage control signal generator 38.” *Id.*, 6:37-41. “The device characteristics map 34 stores predetermined operational characteristics of integrated circuit device 10,” which are determined “as part of the manufacturing process ... or during final testing of the integrated circuit device.” *Id.*, 6:64-66, 7:1-5, 7:24-37.

The predetermined operational voltages may be programmed into the device characteristics map 34 either as part of the manufacturing process (such as where the map 34 comprises ROM memory cells) or during final testing of the integrated circuit device (such as where the map 34 comprises EPROM,

EEPROM, or FLASH memory cells). One advantage of programming after final test is that the predetermined operational voltages can be selected to optimize the speed of the particular device. For example, if during final testing a particular device were determined to run slow at low voltage and high temperature the corresponding predetermined operational voltage could be set high to improve performance at that temperature.

MTK-1007, 7:24-37.

228. Schutz further explains how the “IC voltage control 12” adapts the voltage for the integrated circuit. Specifically, the “IC temperature sensor 32” detects the temperature and provides a “digital temperature value” to the “device characteristics map 34.” *Id.*, 38-45. “In response to the digital temperature value generated by the IC temperature sensor 32, device characteristics map 34 provides the corresponding operational voltage value to the voltage control signal generator 38.” *Id.* “The voltage control signal generator 38 generates the voltage control signals 14 according to the predetermined operational voltage value indicated by map 34,” in response to which the “programmable power supply 18” generates the “supply voltage 16.” *Id.*, 7:42-45. Schutz further explains that “[i]n a closed-loop design, the voltage control signal generator 38 also receives the supply voltage 16 as a feedback signal, and adjusts, or fine tunes, the voltage control signals according to the actual supply voltage 16 sensed.” *Id.*, 7:46-50. In this way, Schutz’s “integrated circuit device 10” achieves a reliable operation speed for the “integrated circuit device 10” and reduces power consumption regardless of manufacturing variations and temperature changes. *Id.*, 1:13-2:45.

2. Combination of Takahashi and Schutz

229. In my opinion, a POSITA would have been motivated to combine Takahashi and Schutz.

230. Takahashi and Schutz are both directed to the same field of endeavor, namely, optimizing power to integrated circuits, including to reduce power consumption. *See* MTK-1004, [0001] (“The present invention pertains to a semiconductor integrated circuit, for example, a semiconductor integrated circuit by which power consumption can be reduced by suppressing leakage current.”), [0002] (discussing applications to “mobile communication terminals, compact solid-state audio players, and portable semiconductor devices, such as laptop personal computers”), [0017]; MTK-1007, Title, Abstract, 1:7-10 (“The present invention relates generally to supplying electrical power to circuits”), 1:13-2:45 (discussing the benefits of “reduced power consumption” including to “increase battery life of laptop and notebook computers.”). As I explained above, the ’077 Patent is in the same field of endeavor in that it is also concerned with optimizing power to integrated circuits and reducing overall power consumption, including that due to leakage currents. *See* MTK-1001, Abstract, 1:29-39; 2:37-50.

231. A POSITA also would have been motivated to combine Takahashi and Schutz because both address the same known problem of providing optimum voltages to an integrated circuit, and do so in similar ways. As shown below, Takahashi and Schutz employ a similar device structure in which an integrated

circuit provides control signals to a voltage regulator or supply, which optimizes the power provided to the integrated circuit.

Figure 2

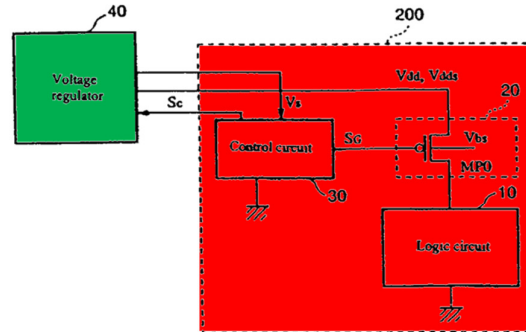
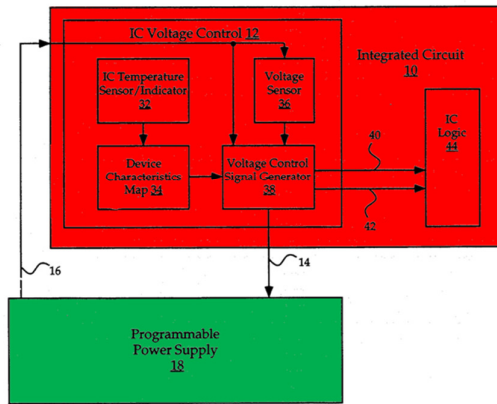


FIG. 1

MTK-1007, FIG. 2 (annotated, left); MTK-1004, FIG. 1 (annotated, right)

232. As I discussed above, Takahashi discloses optimizing “source voltages” supplied to the “logic circuit 10” and other power islands “according to the driving capabilities of the transistors” in the circuit and the operating status of the device. *See* MTK-1004, [0099]-[0100]. Schutz takes a similar approach to optimizing the voltages provided to its “integrated circuit device 10.” Specifically, Schutz “optimize[s] the high speed or high frequency performance” of the device by adjusting its “supply voltage 16” depending on temperature and the device’s “manufacturing process,” “intended use,” and “performance characteristics.” *See* MTK-1007, Abstract, 5:14-18, 7:5-8.

233. Takahashi and Schutz determine these optimal voltages in the same way—by testing the devices during manufacturing to determine their

characteristics, then programming the devices based on the results of the device testing. MTK-1004, [0098]-[0109]; MTK-1007, 5:14-34, 6:64-7:37.

In order to instruct voltage regulator 100 of 5 different levels of source voltage, 3-bit control data DAT are needed. Here, assume, for example, that control data DAT comprise 3 bits of data D2, D1, and D0. After the production process for device 200 is completed, it is measured using a test circuit in order to extrapolate the driving capabilities of the pMOS transistor and the NMOS transistor constituting device 200 according to the result of the measurement, so that the condition of device 200 under the process requirements shown in FIG. 13 can be determined. Because fusing circuit 202 can be programmed to set the respective fuses to desired conditions according to the condition of device 200, control data DAT in accordance with the condition of device 200 are output by fusing circuit 202. Voltage regulator 100 controls the levels of source voltages V_{dd1} , V_{dd2} , and V_{dd3} supplied to device 200 using predetermined optimum values according to control signal SC indicating control data DAT and the operating condition of the device.

MTK-1004, [0109]; *see generally id.*, [0098]-[0100], [0109]-[0117].

The predetermined operational voltages may be programmed into the device characteristics map 34 either as part of the manufacturing process (such as where the map 34 comprises ROM memory cells) or during final testing of the integrated circuit device (such as where the map 34 comprises EPROM, EEPROM, or FLASH memory cells). One advantage of programming after final test is that the predetermined operational voltages can be selected to optimize the speed of the particular device. For example, if during final testing a particular device were determined to run slow at low voltage and high temperature the corresponding predetermined operational voltage could be set high to improve performance at that temperature.

In response to the digital temperature value generated by the IC temperature sensor 32, device characteristics map 34 provides the corresponding predetermined operational voltage value to the voltage control signal generator 38. The voltage control signal generator 38 generates the voltage control signals 14 according to the predetermined operational voltage value indicated by map 34.

MTK-1007, 7:24-37; *see generally id.*, 4:55-5:18, 6:64-7:45, 8:12-28, FIG. 3.

234. During operation, Takahashi and Schutz use this programming to determine the optimum supply voltages for their respective integrated circuits. Specifically, Takahashi's "voltage regulator 100" receives "control data DAT" stored in "fusing circuit 202," and "generates source voltages V_{dd1} , V_{dd2} , and V_{dd3} using optimum values ... according to control data DAT and control signal SC indicating the operating status of device 200, and outputs them into device 200." MTK-1004, [0098], [0117]. Similarly, Schutz's "IC voltage control circuit 12" "selects one of the predetermined operational voltages stored in the device" that is the "optimized operational voltage for the measured device temperature," such that the optimal voltage is then "generated by the programmable power supply" and provided to the integrated circuit device. MTK-1007, 8:11-28.

235. A POSITA would therefore understand that both Takahashi and Schutz reduce "the effect of variations in the production process" by powering their devices using "optimum source voltages in accordance with the process requirements of the circuit elements constituting the device." MTK-1004, [0117]; MTK-1007, 7:5-37 ("[t]he device characteristics map 34 stores predetermined

operational characteristics of integrated circuit device 10” such that “[t]he predetermined operational voltages may be chosen to optimize the high speed or high frequency performance of integrated circuit device 10 at a given temperature”), 8:12-19.

236. In my opinion, these similarities between Takahashi and Schutz would have motivated a POSITA to implement Schutz’s teachings of voltage optimization into Takahashi’s system, to further improve Takahashi’s ability to optimize the voltages provided to “device 200.”⁶

237. As discussed above, Takahashi’s integrated circuit of Figures 11-17 programs “control data DAT” into the “fusing circuit 202” to account for the “driving capabilities of the pMOS transistor and the nMOS transistor [that] vary due to variations during the production process.” MTK-1004, [0099]. During operation, the “voltage regulator 100” generates the “source voltages V_{dd1} , V_{dd2} , and V_{dd3} ” for “device 200” based on the “control signal S_c ” that indicates the operating state of the device and the “control data DAT” that indicates the transistor characteristics. *Id.*, [0098]-[0117], [0123]. In this way, Takahashi can optimize the “source voltages” to reduce the effects of process variation and

⁶ As I explained in my analysis of claim 5 above, it is my opinion that Takahashi by itself renders obvious the features of claim 5. However, to the extent that Takahashi alone fails to render claim 5 obvious, it is my opinion that Takahashi in combination with Schutz renders obvious optimizing a voltage based on process and temperature variations as recited by Claim 5.

improve device performance, including reducing power consumption due to leakage currents.

238. However, at the time of the '077 Patent a POSITA would have understood that the optimum voltages to provides the “device 200” also depends on other factors. As I explained at claim 5 above, it was well-known at the time that transistor performance is dependent on both process variation and temperature variation. *See* Section VIII.C.6 (citing references describing transistor performance dependence on process and temperature variations). Thus, even though Takahashi optimizes the “source voltages V_{dd1} , V_{dd2} , and V_{dd3} ” for process variation, those voltages may not be the most optimal voltages for the “device 200.” MTK-1004, [0117]. In my opinion, A POSITA would have therefore understood that the device performance could be further improved by optimizing the voltages generated by the “voltage regulator 100” to account for temperature variations in addition to process variations. To implement such improvements, a POSITA naturally would have looked to references such as Schutz, which issued in 1995 to Intel Corporation, a well-known company in the field.

239. Schutz provides one solution for optimizing the voltages provided to an “integrated circuit device” to account for temperature variations in addition to process variations.

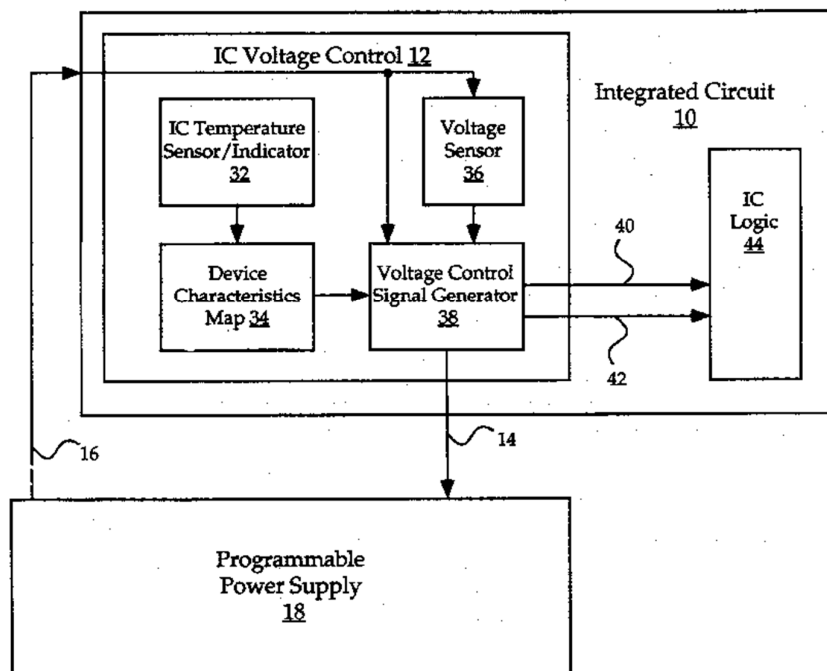
The specification describes an integrated circuit device that selects its own supply voltage by controlling a programmable power supply. The programmable

power supply provides a supply voltage in response to one or more voltage control signals generated by the integrated circuit device. The integrated circuit device includes a voltage control circuit for generating the voltage control signals according to one or more predetermined operational voltages programmed into the integrated circuit device such that the supply voltage is substantially equal to a selected one of the predetermined operational voltages. The integrated circuit device may include a temperature sensor to allow selection of the predetermined operational voltage according to device temperature to avoid speed-limiting voltage and temperature combinations.

MTK-1007, Abstract; *see also id.*, 8:13-19 (explaining that the “optimized operational voltage” may be based on the “measured device temperature” and “other factors including ... manufacturing characteristics or the intended application of the device”).

240. As Schutz explains with respect to Figure 2, an “IC temperature sensor 32 senses the temperature of the device 10 and indicates that temperature to the device characteristics map 34.” MTK-1007, 6:50-52. “In response to the digital temperature value generated by the IC temperature sensor 32, device characteristics map 34 provides the corresponding predetermined operational voltage value to the voltage control signal generator 38.” *Id.*, 7:38-42. Then, “voltage control signal generator 38 generates the voltage control signals 14 according to the predetermined operational voltage value indicated by map 34” and provides the control signals to the “programmable voltage generator 18” to generate the optimal “supply voltage 16” for the “integrated circuit device 10.” *Id.*, 7:38-45; *see also id.*, 4:14-18, 8:20-28.

Figure 2



MTK-1007, FIG. 2.

241. In my opinion, because Takahashi and Schutz provide similar solutions to a similar problem within the same field, a POSITA would have been motivated to combine the two references to further optimize the “source voltages” in Takahashi’s system. For example, a POSITA would have been motivated to modify Takahashi’s “voltage regulator 100” to employ Schutz’s “IC temperature sensor” in addition to the “fusing circuit 202.” A POSITA would have understood that such a modification would have enabled Takahashi’s “voltage regulator 100” to further optimize the “source voltages” based on temperature variation in addition to process variation.

242. Further, a POSITA would have readily implemented a temperature sensor into Takahashi's system to further optimize the voltages provided to the "device 200" with predictable results. Temperature sensors were well known in the art, such that a POSITA would have been able to implement a temperature sensor in Takahashi's system using only routine electrical and computer engineering principles. A POSITA also would have known how to modify Takahashi's "voltage regulator 100" to select optimum values for the "source voltages" provided to "device 200" based on temperature in addition to the "control data DAT and status control signal S_C." MTK-1004, [0111]. For example, a POSITA would have known that the available output states for Takahashi's "voltage regulator 100" (e.g., as shown in Figures 13-15 of Takahashi) could be augmented with additional states that account for variations in temperature. The similarity between Takahashi's implementation of these output states and Schutz's implementation of these output states would have made such a modification straightforward for a POSITA to implement.

TABLE 2

predetermined operational voltage	programmed value
+5.0	000
-5.0	001
12.0	010
3.3	011
2.5	100
1.8	101
1.5	110
1.2	111

TABLE 3

0-20° C.	3.0 V	40-50° C.	3.3 V
10-20° C.	3.1 V	50-60° C.	3.4 V
20-30° C.	3.2 V	60-70° C.	3.5 V
30-40° C.	3.2 V	70-80° C.	3.6 V

Active Mode	BitBitBit 2 1 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0 0 0	1.2V	1.2V	1.20V	Weak
Fuse prog-1	0 0 1	1.15V	1.15V	1.15V	NTPW,NWPT
Fuse prog-2	0 1 0	1.05V	1.05V	1.05V	TYP,NSPW,NWPS
Fuse prog-3	0 1 1	0.95V	0.95V	0.95V	NSPT,NTPS
Fuse prog-4	1 0 0	0.85V	0.85V	0.85V	Strong

FIG. 14

Sleep Mode	BitBitBit 2 1 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0 0 0	0.7V	1.0V	0.7V	Weak
Fuse prog-1	0 0 1	0.7V	1.0V	0.7V	NTPW,NWPT
Fuse prog-2	0 1 0	0.7V	1.0V	0.7V	TYP,NSPW,NWPS
Fuse prog-3	0 1 1	0.7V	1.0V	0.7V	NSPT,NTPS
Fuse prog-4	1 0 0	0.7V	1.0V	0.7V	Strong

FIG. 15

MTK-1007, Tables 2-3 (left); MTK-1004, FIGS. 14-15 (right).

In my opinion, such a combination of Schutz with Takahashi would predictably optimize the voltages provided to the “device 200” to account for temperature variations in addition to process variations, thereby further improving the performance and power consumption in Takahashi’s “device 200.”

243. Therefore, it is my opinion that a POSITA would have been motivated to combine Takahashi with Schutz and would have been capable of doing so with a reasonable expectation of success.

3. Claim 5

244. Claim 5 recites “[t]he method as claimed in claim 4 wherein the optimum voltage is dependent upon both process variation and temperature variation.” In my opinion, to the extent that Takahashi alone does not render obvious claim 5, the combination of Takahashi and Schutz renders obvious claim 5.

245. As I discussed at element 1[p] and claim 5 of Section VIII.A above, Takahashi discloses a power manager (*i.e.*, the “voltage regulator”) that generates optimal voltages for the “device 200” based on the operating state of the device and the performance characteristics of the transistors in the device. *See* MTK-1004, [0117] (“Because voltage regulator 100 generates source voltages V_{dd1} , V_{dd2} , and V_{dd3} using optimum values under the respective preset conditions according to control data DAT and control signal S_C indicating the operating status of device 200, and outputs them into device 200, optimum source voltages

in accordance with the process requirements of the circuit elements constituting the device can be supplied, and the effect of variations in the production process can be reduced.”).

246. In the same technical field, Schutz discloses an “IC voltage control circuit 12” that generates an optimum operational voltage for the “integrated circuit 10” “based on the temperature of the device” and “device characteristics.” MTK-1007, 6:64-7:37. As I explained above, Schutz does so using an “IC temperature sensor 32” that detects the temperature of the integrated circuit device and a “voltage control signal generator 38” that selects an “optimized operational voltage” for the device based on the measured temperature and a “device characteristics map 34.” *Id.*, 6:50-7:37, 8:12-18.

247. In my opinion, a POSITA would have found it obvious to modify Takahashi’s “voltage regulator” in view of Schutz, to generate “source voltages” that are optimized based upon both process variation and temperature variation. For instance, it would have been obvious for the “voltage regulator 100” of Figures 11-17 to receive a temperature signal from a temperature sensor like Schutz’s “IC temperature sensor 32” in addition to the “control data DAT” that indicates the “effect of variations in the production process” and the “status control signal S_C .” MTK-1004, [0098], [0111], [0117], FIGS. 13-17. Based on these inputs, Takahashi’s “voltage regulator 100” would generate optimum “source voltages V_{dd1} , V_{dd2} , and V_{dd3} ” that account for process and temperature variations along with the operating status of the device. *Id.*

248. As I discussed above, the combined Takahashi-Schutz system would select the optimum values for the “source voltages V_{dd1} , V_{dd2} , and V_{dd3} ” from a set of states like those depicted in Figures 14-15 of Takahashi, simply modified to account for temperature variation in addition to the operational mode and transistor characteristics of the “device 200.” MTK-1004, [0110]-[0111]; MTK-1007, 4:55-5:27, 6:64-7:23.

249. In my opinion, a POSITA would have had a reasonable expectation of success in combining Schutz and Takahashi in this way, because the combination would only require (1) the integration of Schutz’s “IC temperature sensor 32” into Takahashi’s system, and (2) minor updates to the programming of the “voltage regulator,” to select its voltage outputs based on temperature in addition to the “control data DAT and status control signal S_c .” MTK-1004, [0111]. Integrating Schutz’s “IC temperature sensor 32” into Takahashi’s system would have required merely routine electrical or computer programming knowledge and was a task well within the skill of a POSITA. Selecting the “voltage regulator’s” voltage outputs based on temperature variation in addition to process variation enables further optimization of those voltages for the “device 200.” A POSITA would have reasonably expected that such improvements would further improve the performance of the “device 200,” including its ability to reduce power consumption due to leakage currents. For example, optimizing the “source voltages” based on both temperature and process variation would ensure that the “pMOS transistor MP0 constituting switching circuit 20 is in the

super cut-off status during standby” such that “the occurrence of leakage current at logic circuit 10 is suppressed.” *Id.*, [0116].

250. It is therefore my opinion that the combination of Takahashi and Schutz renders obvious claim 5.

4. Claim 14

251. Claim 14 recites “[t]he method as claimed in claim 13 wherein the optimum voltage is dependent upon both process variation and temperature variation.” To the extent that Takahashi does not render obvious claim 14, the combination of Takahashi and Schutz renders obvious claim 14 for at least the reasons discussed above with respect to claim 5, the discussion of which is incorporated by reference.

D. Analysis of Mizuno with Respect to Claims 1-18

252. For the reasons articulated in detail below, and based on my review of the '077 Patent and the Mizuno reference, it is my opinion that a POSITA would have readily understood that Mizuno renders obvious all elements of claims 1-18 of the '077 Patent.

1. Overview of Mizuno

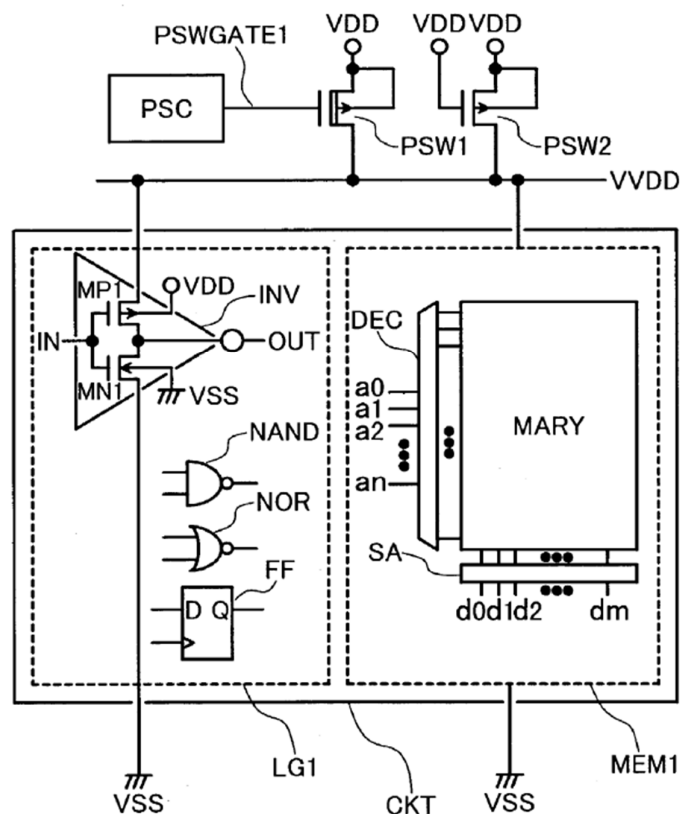
253. Mizuno is titled “Semiconductor Integrated Circuit Device.” MTK-1005, Title. Mizuno explains that the Field of the Invention is “a semiconductor integrated circuit device with excellent high speed and low power operation characteristics.” *Id.*, [0001]. Mizuno explains that “[a]s the chip manufacturing process progresses towards making smaller and finer chip circuitry, the different

leakage currents within the chip, including the subthreshold leakage current, gate tunneling leakage current and GIDL (Gate-Induced Drain Leakage) current increase.” *Id.*, [0002]. “These leakage currents increase the electrical current consumption of the chip.” *Id.* Mizuno proposes systems and methods to address these leakage currents by reducing the overall power consumption of a device during standby modes that are caused by leakage currents. *See id.*, [0003]-[0009]. In particular, Mizuno’s “invention ... is capable of reducing the different types of leakage current (subthreshold leakage current, GIDL current, gate tunneling current, etc.) while the circuit block is in standby state while still maintain the information stored in the information retention circuits within the circuit block. The present invention also allows high speed circuit block operation while the circuit block is in the operation state.” *Id.*, [0009].

254. To achieve this, Mizuno couples a “leakage current control circuit” to a “circuit block CKT” in the integrated circuit. *Id.*, Abstract, [0008]-[0009], [0053]. Mizuno discloses several related embodiments with this structure.

255. Figures 1-30 depict a first embodiment of Mizuno’s integrated circuit device. MTK-1005, [0052]-[0107].

FIG.1



MTK-1005, FIG. 1.

FIG. 1 is a circuit diagram showing the basic structure of the invention. In the figure, CKT denotes the circuit block, PSW1 denotes the power switch, VDD denotes a power supply voltage for example with a voltage of 1.0 volts, VVDD denotes the virtual power line, VSS denotes the ground with a voltage of 0 volts, and PSC denotes the power switch controller. A circuit block CKT as shown for example in FIG. 1 contains a logic circuit LG1 composed of an inverter INV, a NAND circuit NAND, a NOR circuit NOR and a flip-flop circuit FF; and a memory MEM1 composed of a memory cell array MARY, word decoder DEC and sensing amplifier SA, etc. The circuit block CKT may also be comprised only of a logic circuit LG1 or a memory MEM1. One characteristic feature is it (circuit block) contains information retention circuits such as the flip-flop FF of the logic circuit LG1 and the

memory cell array MARY. Here, the information retention circuits are circuits with volatile information retention functions and that information is determined by the CMOS logic.

The power switch controller PSC controls the on and off operation of the power switch PSW1 connected between the power supply VDD and the virtual power line VVDD. The power switch controller PSC also controls the current flow in the power supply VDD and the virtual power line VVDD. A current source is also connected between the power supply VDD and the virtual power line VVDD, and limits the current flowing to the virtual power line VVDD from the power supply VDD. The circuit block CKT is connected between the virtual power line VVDD and the ground VSS and the virtual power line VVDD is equivalent to an actual power line in the circuit block CKT. In other words, the current supplied to the circuit block during operation is mainly supplied from the power switch PSW1; and the current supplied to the circuit block during standby operation is mainly supplied to the current source PSW2. Though not shown in FIG. 1, the voltage of the power supply VDD is the circuit block C operating voltage and is supplied from a stable power supply circuit.

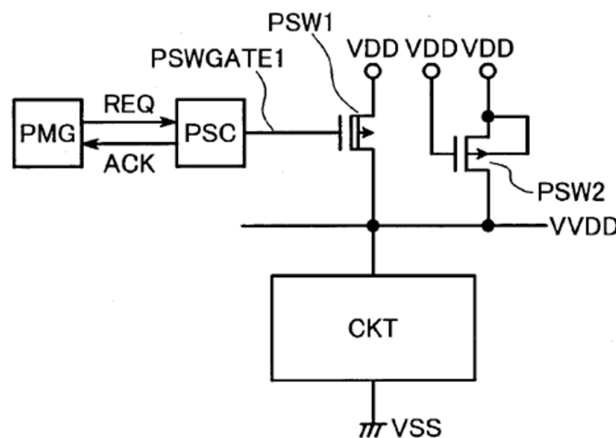
MTK-1005, [0053]-[0054].

256. Thus, Mizuno discloses a system in which the power switch controller turns the power switch PSW1 on or off to control power consumption within the circuit block CKT. Specifically, “the gate signal PSWGATE1 of power switch PSW1 is driven to low level by the power switch controller PSC and the power switch PSW1 turns on. In this state, power is supplied to the circuit block CKT by way of the power switch PSW1 so that the virtual power line VVDD reaches VDD potential and the circuit block CKT is operable (in

operating state).” *Id.*, [0055]. On the other hand, when “the gate signal PSWGATE1 of power switch PSW1 is driven to high level by the power switch controller PSC,” the “power switch PSW1 turns off.” *Id.* As a result, “[t]he voltage (or voltage potential of virtual power line VVDD gradually discharges” and “[t]he leakage current flowing to circuit block CKT ... that was initially large ... also gradually becomes a smaller value.” *Id.*

257. Figures 22-30 of Mizuno provide additional detail about the power switch controller PSC. MTK-1005, [0092]-[0107].

FIG.22



MTK-1005, FIG. 22.

FIG. 22 is a structure of the interface for the power switch controller PSC. The power switch controller PSC that controls the power switch PSW1 and current source PSW2 implements control by means of a power controlling circuit PMG. This allows designing the circuit block CKT low-leak mechanism separately from the power controlling circuit PMG that reduces power consumption in the chip overall. A handshake between the power controlling circuit PMG and the power switch controller PSC by means of the request line

REQ and response line ACK controls the on/off operation of the power switch PSW1 and controls the state of the circuit block. Here, setting the request line REQ to high level turns on the power switch PSW1 and controls the circuit block CKT in the operation state. After the power switch PSW1 turns fully on and the virtual power line VVDD is charged to the voltage potential of power supply VDD, when the response line ACK reaches high level, the external section of the power switch controller (power controlling circuit PMG) is notified that the circuit block CKT has switched to the operation state. Conversely, when the request line REQ is set to low level, the power switch PSW1 turns off and the circuit block is controlled to the standby state. When the power switch PSW1 turns fully off, and the response line ACK switches to low level, the external section of the power switch controller is notified that the circuit block CKT has switched to the standby state.

Id., [0093].

258. In Figures 23-30, Mizuno discloses various structures for the power switch controller capable of providing this functionality. For example, Figures 23 and 24 of Mizuno describe one possible structure for the power switch controller that enables the power switch controller to generate an appropriate voltage for the signal PSWGATE1 based on the control signal REQ received from the power controlling circuit PMG.

FIG.23

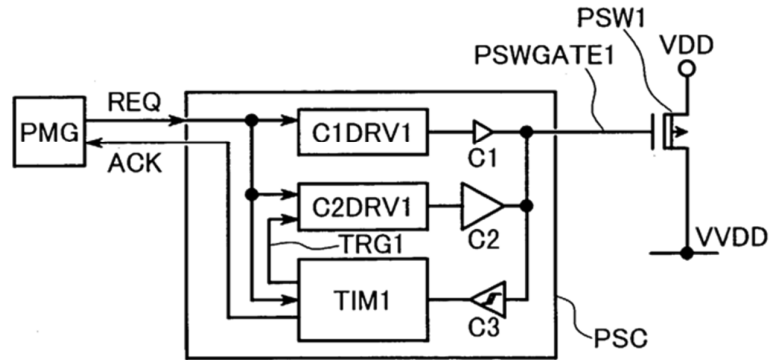
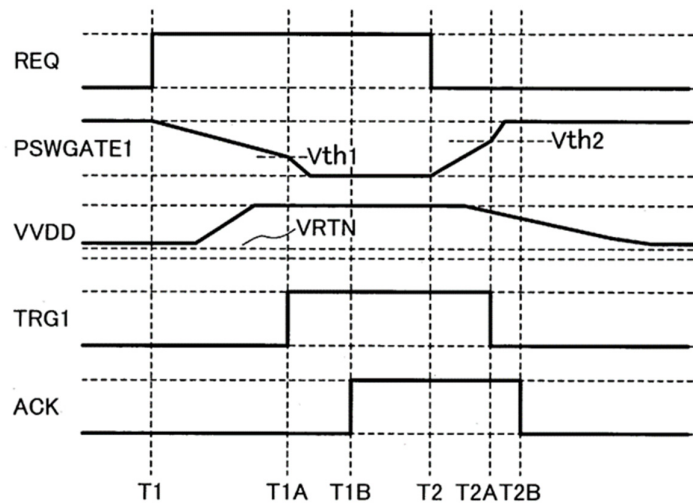


FIG.24



MTK-1005, FIGS. 23-24

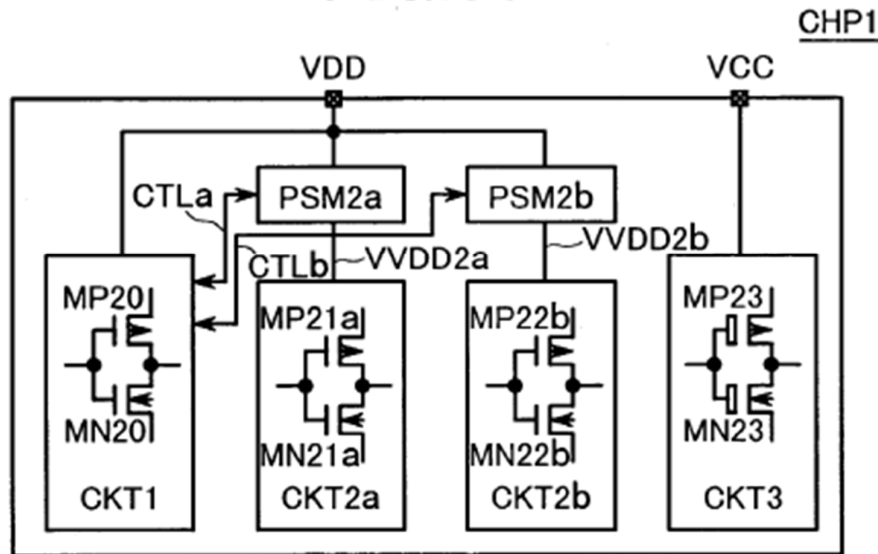
FIG. 23 is a more detailed structure of the power switch controller PSC. In the figure, C1 is a drive circuit (hereafter described as a driving circuit with high impedance) for the gate signal PSWGATE1 having small drive performance. Also in the figure, C2 is a drive circuit (hereafter described as a driving circuit with low impedance) for the gate signal PSWGATE1 having drive performance larger than C1. Also in the figure, C3 is a voltage potential detector for the gate signal PSWGATE1, C1DRV is a control circuit for C1, C2DRV is a control circuit for C2 and TM1 is a timer.

FIG. 24 is a timing chart for the operation in FIG. 23. When operation has shifted from standby to the operation state and the request line REQ reaches high level, first of all the gate signal PSWGATE1 is driven to high impedance by C1 by way of the C1DRV control circuit for C1. The potential detector C3 detects that the gate signal PSWGATE1 was driven to a level (V_{th1}) at time T1A, and TRG1 is driven to high level by the timer TIM1. The gate signal PSWGATE1 is in this way driven to a low impedance by C2 by way of the C2DRV control circuit for C2. The timer TM1 measures the time TA from time T1 to T1A, and after a time TB established using the specific relation (for example {fraction (1/2)}) with time TA, (time T1B in the example in FIG. 24) the response line ACK is driven to high level. There are no particular restrictions on the timer characteristics (relation between time TA and time TB) however the gate signal PSWGATE1 is driven completely to low level at time T1B. Also the virtual power line VVDD may be fully charged up to the voltage potential of VDD.

MTK-1005, [0095]-[0096].

259. Mizuno discloses a related embodiment with respect to Figures 35-40. MTK-1005, [0120]-[0134] (“Of course, the various adaptations and specific examples disclosed for the first embodiment are also applicable to the leakage current reduction circuit of the third embodiment.”). The embodiment of Figures 35-40 extends the embodiment of Figures 1-30 to control the leakage currents through multiple circuits in a device using “multiple leakage control circuits [PSM2a, PSM2b].” *Id.*, [0122]. Mizuno explains that “[b]y establishing multiple leakage control circuits as in FIG. 35, and controlling the leakage current of circuits grouped in multiple circuits integrated on the chip, the leakage current of the overall chip can be efficiently reduced.” *Id.*

FIG.35



MTK-1005, FIG. 35.

260. In the example of FIG. 35, for instance, PSM2a controls power provided to the circuit block CKT2a and PSM2b controls power provided to the circuit block CKT2b. *Id.*, [0121]. By powering the circuit blocks CKT2a, CKT2b only when necessary, overall power consumption of the chip can be reduced, even where other circuit blocks CKT1 and CKT3 require power at all times. *Id.*

2. Claim 1

(a) Element 1[p]

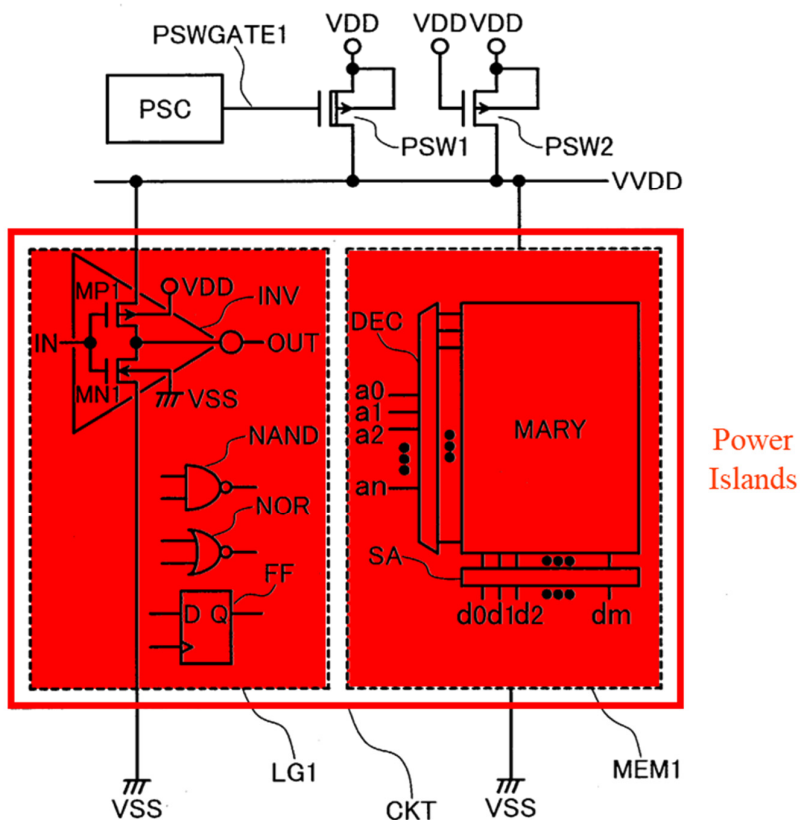
261. The preamble of claim 1 recites “[a] method carried out in an integrated circuit that includes an adaptive leakage controller, a power manager and a plurality of power islands, the method comprising.” Mizuno discloses and renders obvious the preamble of claim 1.

262. Mizuno is titled “Semiconductor Integrated Circuit Device” and relates to methods carried out in “a semiconductor integrated circuit device with

excellent high speed and low power operation characteristics.” MTK-1005, Title, [0001]. For example, both of the related embodiments of Figures 1-30 and 35-40 are integrated circuit devices. *See generally id.*, FIGS. 1-30, 35-40.

263. Mizuno’s integrated circuit device comprises a plurality of power islands. For example, as shown in Figure 1, Mizuno’s integrated circuit includes a “circuit block CKT ... contain[ing] a logic circuit LG1 composed of an inverter INV, a NAND circuit NAND, a NOR circuit NOR and a flip-flop circuit FF; and a memory MEM1 composed of a memory cell array MARY, word decoder DEC and sensing amplifier SA, etc.” MTK-1005, [0053].

FIG.1



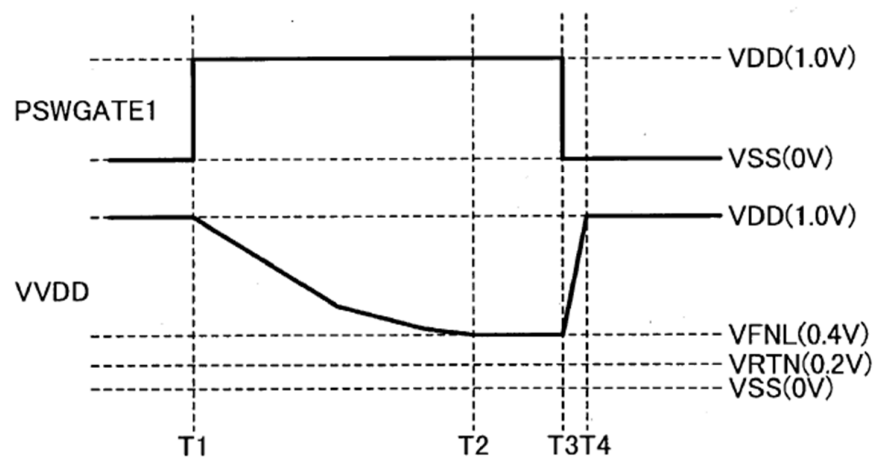
MTK-1005, FIG. 1

264. In my opinion, a POSITA would have understood and otherwise found it obvious that Mizuno's "logic circuit LG1" and "memory MEM1," both individually and collectively, are power islands. The '077 Patent describes a power island as any "section, delineation, partition, or division of an integrated circuit where power consumption is controlled within the section, delineation, partition, or division." *Id.*, 3:65-4:1. Mizuno's circuit block CKT, including the logic circuit LG1 and memory MEM1, are individually and collectively portions

of an integrated circuit device where the power consumption is controlled within the portion of the integrated circuit. *See* MTK-1005, [0054].

265. Specifically, when the circuit block CKT is in an “operating state,” “power is supplied to the circuit block CKT by way of the power switch PSW1 so that the virtual power line VVDD reaches VDD potential and the circuit block CKT is operable.” *Id.*, [0055]. On the other hand, when the circuit block CKT is in “standby,” the “power switch PSW1 turns off” and the “voltage (or voltage potential) of virtual power line VVDD gradually discharges due to the current leakage from virtual power line VVDD of circuit block CKT to ground VSS.” *Id.*, [0054]-[0055]. This process is shown in Figure 2 of Mizuno.

FIG.2

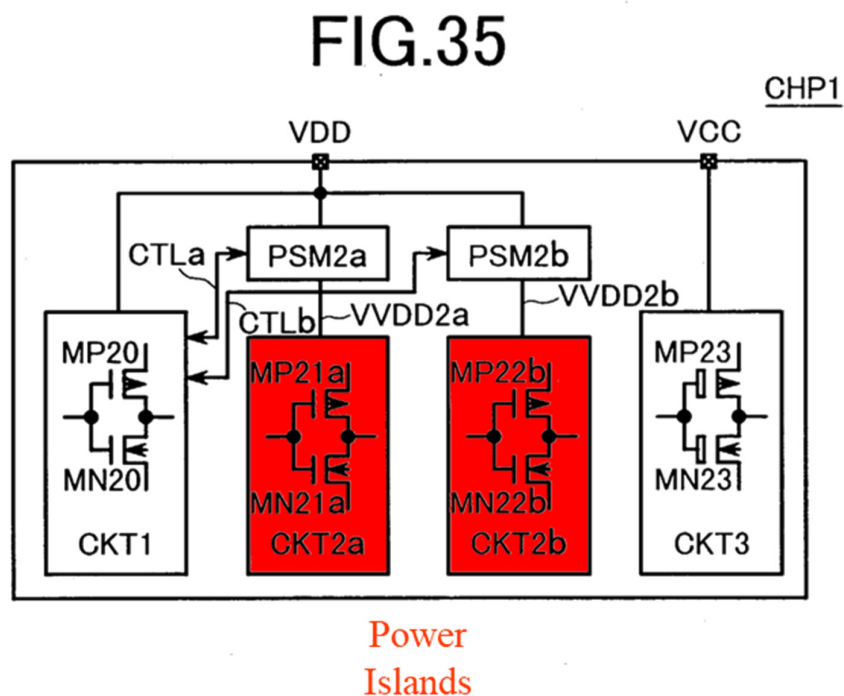


MTK-1005, FIG. 2.

266. Mizuno explains that “[a]s the voltage of the virtual power line VVDD becomes lower ... [t]he leakage current flowing to circuit block CKT ... also gradually becomes a smaller value.” *Id.*, [0055]. As a result, “power

consumption due to leakage current in the standby state can be greatly reduced.”
Id., [0087].

267. Mizuno’s other embodiments also depict an integrated circuit with a plurality of power islands. In the related embodiment of Figures 35-40, for example, Mizuno’s integrated circuit has multiple “circuit blocks” CKT1, CKT2a, CKT2b, CKT3 that are each a power island.



MTK-1005, FIG. 35.

268. Mizuno describes that each of these circuits blocks is a different portion of the chip CHP1 with a different function.

FIG. 35 is a block circuit diagram of the chip CHP1 structure of the present invention. Most of the signal wiring and power supply grounds have been omitted from the drawing for simplicity. The circuit block CKT1 is a circuit block supplied with power directly

from a power supply VDD and not by way of the leakage reduction circuit of the present invention. Circuit blocks CKT2a and CKT2b are circuit blocks supplied with power from the power supply VDD by way of the leakage reduction circuits PSM2a and PSM2b of the present invention. The circuit block CKT3 is a circuit block is supplied with power directly from a power supply VCC different from the power supply VDD and not by way of the leakage Reduction circuit of the present invention. ... The circuit block CKT1 in FIG. 35 is a circuit requiring that power be constantly applied. These for example are circuits to control the leakage reduction circuits PSM2a and PSM2b, real time clocks (RTC), interrupt handling circuits, a DRAM refresh circuit, a memory, etc. The circuit block CKT3 is an I/O circuit.

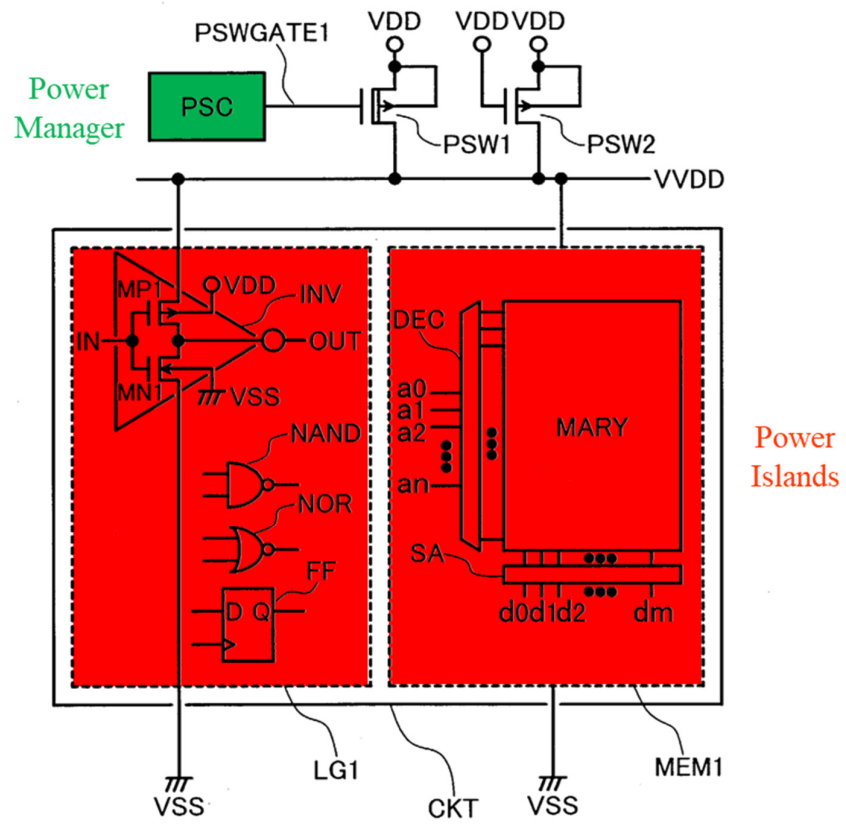
MTK-1005, [0121].

269. Power consumption is controlled within each of these portions of the chip CHP1. For example, power consumption within each of the circuits CKT2a and CKT2b is controlled by the “leakage reduction circuits PSM2a and PSM2b” that operate similarly to the leakage reduction circuitry in the embodiment of Figures 1-30. *See* MTK-1005, [0125]-[0128] (The structure of FIG. 38 can also utilize the method for applying the voltage VFNL to the virtual power line VVDD during standby as in the structure in FIG. 17. The PSW2 of FIG. 38 is not required in this case. Two types of control methods may be used in this case. In the first method, the VDD voltage is applied to VREF during operation as described above, and the power supply voltage VDD is applied to the virtual power line VVDD2a. During standby the VFNL ($<VDD$) voltage is applied to VREF, and the voltage VFNL is supplied to the virtual power line VVDD2a. The voltage

source VFNLGEN was required by the structure of FIG. 17, however this structure (FIG. 38) has the advantage of being able to use an operational amplifier OPAMP and power switch PSW1 instead.”), [0130] (“Of course the various adaptations and specific examples disclosed for the first embodiment are also applicable to the leakage current reduction circuit of the third embodiment.”), FIG. 38. Thus, it is my opinion that Mizuno discloses and renders obvious to a POSITA an integrated circuit that includes multiple power islands. For instance, based on the embodiment of Figures 35-40, a POSITA would have found it obvious for the integrated circuit of Figures 1-30 to include multiple power islands (*e.g.*, multiple circuit blocks “CKT”) whose power consumption is individually controlled.

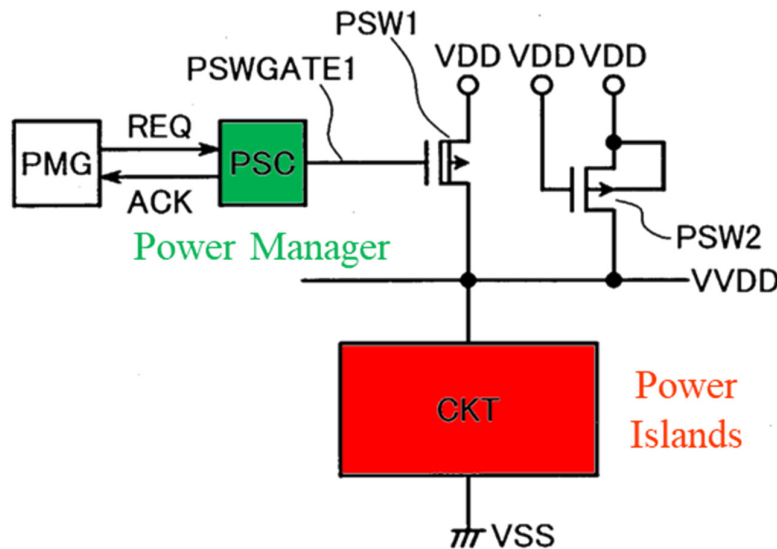
270. In my opinion, Mizuno also discloses and renders obvious that the integrated circuit includes a “power manager.” Specifically, Mizuno’s integrated circuit device has a “power switch controller PSC” for controlling the power consumption of the power islands. MTK-1005, [0054], [0093]. Examples of Mizuno’s power switch controller PSC are shown in Figures 1 and 22, which I have annotated below.

FIG.1



MTK-1005, FIG. 1 (annotated).

FIG.22



MTK-1005, FIG. 22 (annotated).

271. Mizuno explains that the “power switch controller PSC controls the on and off operation of the power switch PSW1 connected between the power supply VDD and the virtual power line VVDD” that “is equivalent to an actual power line in the circuit block CKT.” MTK-1005, [0054].

The power switch controller PSC controls the on and off operation of the power switch PSW1 connected between the power supply VDD and the virtual power line VVDD. The power switch controller PSC also controls the current flow in the power supply VDD and the virtual power line VVDD. A current source is also connected between the power supply VDD and the virtual power line VVDD, and limits the current flowing to the virtual power line VVDD from the power supply VDD. The circuit block CKT is connected between the virtual power line VVDD and the ground VSS and the virtual power line VVDD is equivalent to an actual power line in the circuit block

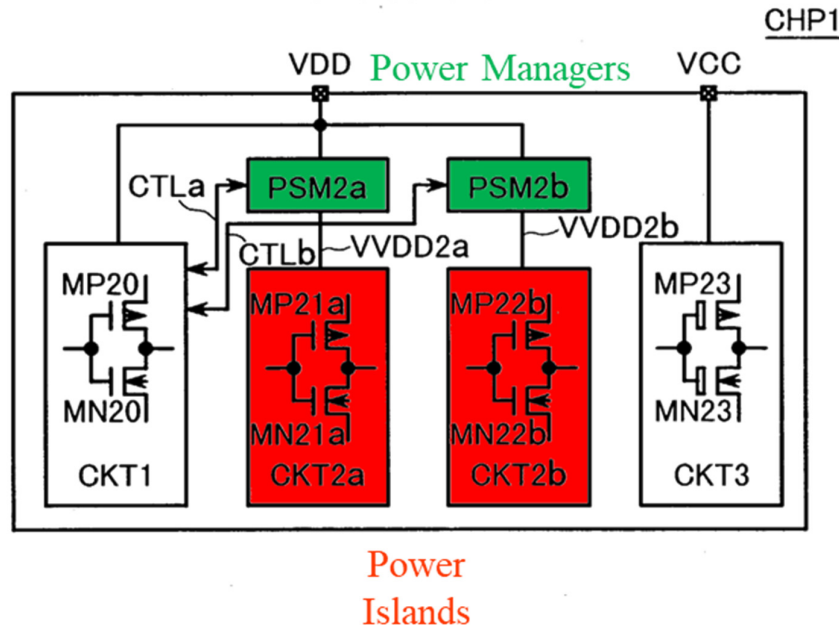
CKT. In other words, the current supplied to the circuit block during operation is mainly supplied from the power switch PS1; and the current supplied to the circuit block during standby operation is mainly supplied to the current source PSW2. Though not shown in FIG. 1, the voltage of the power supply VDD is the circuit block C operating voltage and is supplied from a stable power supply circuit.

Id., [0054].

272. Mizuno explains that “[g]enerally, the smaller the voltage of the virtual power line VVDD, the smaller the value $I_{off}(CKT)$ becomes.” *Id.*, [0059]. Thus, “the size of the respective leakage currents ... during standby in the circuit block are determined by the current source PSW2” and “is smaller than the leakage current flowing in the circuit block CKT during operation.” *Id.*, [0059].

273. Similarly, Mizuno’s integrated circuit in the related embodiment of Figures 35-40 includes “leakage reduction circuits PSM2a and PSM2b” that are used to control power consumption of the “[c]ircuit blocks CKT2a and CKT2b.” *Id.*, [0121].

FIG.35



MTK-1005, FIG. 35 (annotated).

FIG. 35 is a block circuit diagram of the chip CHP1 structure of the present invention. Most of the signal wiring and power supply grounds have been omitted from the drawing for simplicity. The circuit block CKT1 is a circuit block supplied with power directly from a power supply VDD and not by way of the leakage reduction circuit of the present invention. Circuit blocks CKT2a and CKT2b are circuit blocks supplied with power from the power supply VDD by way of the leakage reduction circuits PSM2a and PSM2b of the present invention. The circuit block CKT3 is a circuit block is supplied with power directly from a power supply VCC different from the power supply VDD and not by way of the leakage Reduction circuit of the present invention. ... In the same figure, CTLa, CTLb are leakage control lines of the leakage reduction circuit of the present invention and equivalent to the request line REQ and response line ACK of FIG. 22. The circuit block CKT1 in FIG. 35 is a circuit requiring that power be constantly applied. These for example are circuits to control the leakage reduction circuits PSM2a and PSM2b, real time clocks

(RTC), interrupt handling circuits, a DRAM refresh circuit, a memory, etc.

Id., [0121].

274. In my opinion, a POSITA would have understood and found obvious that Mizuno’s “power switch controller PSC” (and the corresponding portions of the “leakage reduction circuits PSM2a and PSM2b”) is a power manager. While the ’077 Patent does not describe a “power manager” in its written description, the ’077 Patent does briefly describe a “power island manager.”

The power island managers 220, 222, and 224 are any circuitry, device, or system configured to provide control signals to a power island to control power within the power island. The power island managers 220, 222, and 224 can dynamically change the power consumption of the power islands based on the needs and operation of the integrated circuit 200. The power island managers 220, 222, 224 may select a clock, change clock frequency, or modify the voltage within the power island to control the power consumption of the power island.

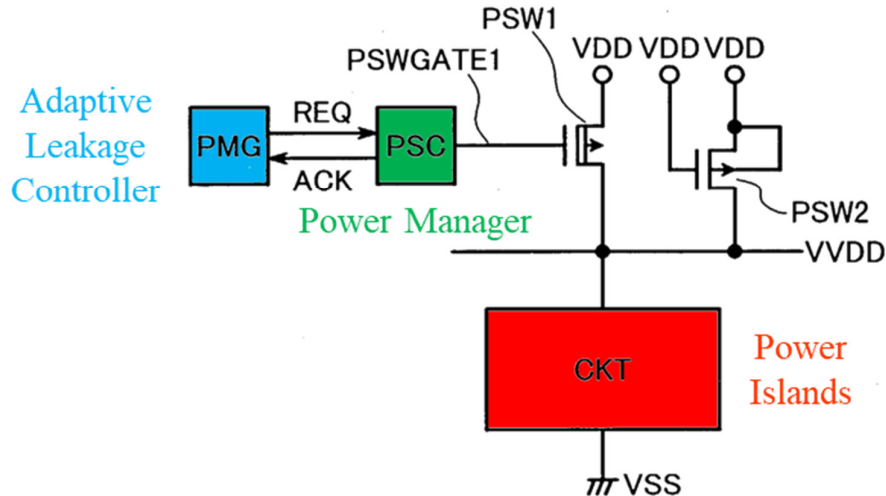
MTK-1001, 4:11-20; *see also id.*, 3:49-55.

275. Like the ’077 Patent’s “power island manager” that “control[s] power within the power island,” Mizuno’s “power switch controller” (and “leakage reduction circuits” that each include a “power switch controller”) controls the power within the “circuit block CKT.” *See id.* Specifically, Mizuno’s “power switch controller” provides the control signal PSWGATE1 that is a variable voltage. Based on the PSWGATE1 signal, voltage within the “circuit block CKT” power island is modified to control the power consumption of the

“circuit block CKT” (e.g., to increase power consumption during operation by providing a higher voltage and current and decreasing power consumption during standby by providing a lower voltage and current). See MTK-1005, [0054]-[0055], [0093].

276. In my opinion, Mizuno also discloses that its integrated circuit includes an “adaptive leakage controller” as required by Claim 1 of the ’077 Patent. Specifically, Mizuno explains that its integrated circuit device includes a “power controlling circuit PMG that reduces power consumption in the chip overall.” MTK-1005, [0093].

FIG.22



MTK-1005, FIG. 22 (annotated).

277. Mizuno explains that the “power controlling circuit PMG” controls the “power switch controller PSC by means of the request line REQ and response

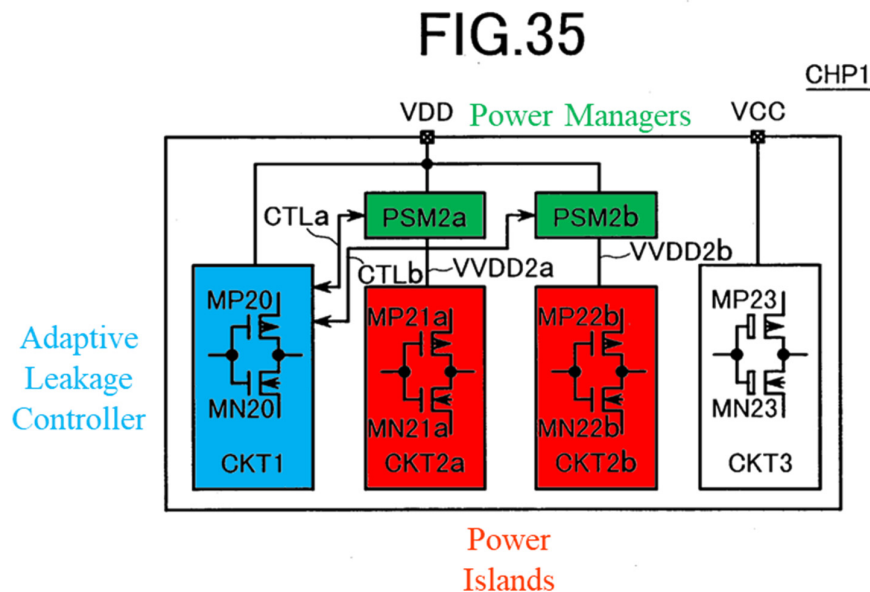
line ACK.” MTK-1005, [0093]. Mizuno provides additional explanation of the “power controlling circuit PMG” with respect to Figure 22.

FIG. 22 is a structure of the interface for the power switch controller PSC. The power switch controller PSC that controls the power switch PSW1 and current source PSW2 implements control by means of a power controlling circuit PMG. This allows designing the circuit block CKT low-leak mechanism separately from the power controlling circuit PMG that reduces power consumption in the chip overall. A handshake between the power controlling circuit PMG and the power switch controller PSC by means of the request line REQ and response line ACK controls the on/off operation of the power switch PSW1 and controls the state of the circuit block. Here, setting the request line REQ to high level turns on the power switch PSW1 and controls the circuit block CKT in the operation state. After the power switch PSW1 turns fully on and the virtual power line VVDD is charged to the voltage potential of power supply VDD, when the response line ACK reaches high level, the external section of the power switch controller (power controlling circuit PMG) is notified that the circuit block CKT has switched to the operation state. Conversely, when the request line REQ is set to low level, the power switch PSW1 turns off and the circuit block is controlled to the standby state. When the power switch PSW1 turns fully off, and the response line ACK switches to low level, the external section of the power switch controller is notified that the circuit block CKT has switched to the standby state.

Id., [0093].

278. Similarly, with respect to the embodiment of Figures 35-40, the “circuit block CKT1” is an “adaptive leakage controller” that provides control signals over “leakage control lines” CTLa, CTLb to the “leakage reduction

circuits PSM2a and PSM2b” to control change the leakage of the “[c]ircuit blocks CKT2a and CKT2b.” *Id.*, [0121].



MTK-1005, FIG. 35 (annotated).

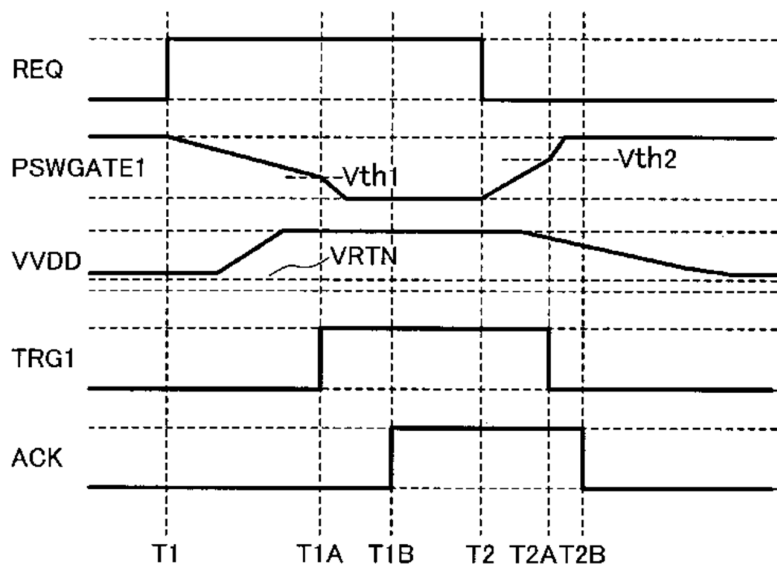
FIG. 35 is a block circuit diagram of the chip CHP1 structure of the present invention. Most of the signal wiring and power supply grounds have been omitted from the drawing for simplicity. The circuit block CKT1 is a circuit block supplied with power directly from a power supply VDD and not by way of the leakage reduction circuit of the present invention. Circuit blocks CKT2a and CKT2b are circuit blocks supplied with power from the power supply VDD by way of the leakage reduction circuits PSM2a and PSM2b of the present invention. The circuit block CKT3 is a circuit block is supplied with power directly from a power supply VCC different from the power supply VDD and not by way of the leakage Reduction circuit of the present invention. ... In the same figure, CTLa, CTLb are leakage control lines of the leakage reduction circuit of the present invention and equivalent to the request line REQ and response line ACK of FIG. 22. The circuit block CKT1 in FIG. 35 is a circuit requiring that power be constantly applied.

These for example are circuits to control the leakage reduction circuits PSM2a and PSM2b, real time clocks (RTC), interrupt handling circuits, a DRAM refresh circuit, a memory, etc.

Id., [0121].

279. Thus, the “power controlling circuit PMG” provides the “circuit block CKT” an operating voltage VDD through “power switch PSW1” when in an active mode and provides a lower voltage through “current source PSW2 [that] functions as a leak current limited circuit for circuit block CKT” when in standby (*i.e.*, sleep) mode. MTK-1005, [0057]. For example, in Figure 24, when Mizuno’s “power controlling circuit PMG” sets “REQ” to a high level, the voltage “VVDD” to the “circuit block CKT” is increased to VDD and the current in the “circuit block CKT” reaches its operational current. MTK-1005, [0096]; *see also Id.*, [0066], FIG. 5. On the other hand, when the “power controlling circuit PMG” sets “REQ” to a low level, the voltage “VVDD” decreases to “VRTN” and the leakage current through “circuit block CKT,” which Mizuno refers to as “I_{off}(CKT),” likewise decreases. *Id.*, [0097]-[0098]; *see also id.*, [0055]-[0057], [0065]-[0066].

FIG.24



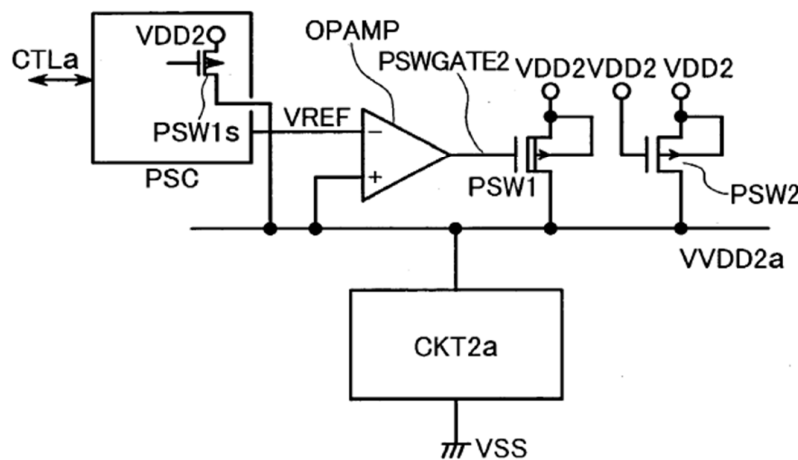
MTK-1005, FIG. 24

280. Thus, a POSITA would have understood and found obvious that Mizuno’s “power controlling circuit PMG” (and the corresponding “circuit block CKT1” for “control[ing] the leakage reduction circuits PSM2a and PSM2b” in Figures 35-40) is an adaptive leakage controller that provides a control signal REQ to optimize the voltage to the “circuit block CKT” to reduce power consumption due to leakage currents. MTK-1001, 4:21-23.

281. Though not recited by the claims, the ’077 Patent explains with respect to its Figure 2 that the “adaptive leakage controller (ALC) 270 ... provides control signals to compensate for process and temperature variation to provide the optimum voltage to be applied to sleep transistors in the power islands.” MTK-1001, 4:21-27; *see also id.*, 4:28-39.

282. To the extent such functionality is required of the claimed “adaptive leakage controller,” Mizuno discloses and renders obvious this element to a POSITA. With respect to the embodiment of Figures 35-40 of Mizuno, Figure 37 depicts a structure having a “voltage regulator circuit” VDC in addition to the leakage reduction circuits PSM2a and PSM2b. MTK-1005, [0124]-[0126]. Figure 38 provides additional detail when the “voltage regulator VDC and leak regulator circuit PSM2a or PSM2b components in the example in FIG. 37 [are] combined together.” *Id.*, [0125].

FIG.38



MTK-1005, FIG. 38.

The voltage regulator VDC and leak regulator circuit PSM2a or PSM2b components in the example in FIG. 37 can be combined together. That structure is shown in FIG. 38. In the figure, PSW2 is the current source, OPAMP is the operational amplifier and VREF is the reference voltage. During operation, a voltage VDD can be supplied to the virtual power line VVDD2a by applying voltage VDD to VREF. To turn the power

switch PSW1 off, VREF may be set to a sufficiently low voltage (for example below 0 volts). The power switch PSW1 has smaller drive power than the power switch PSW1. This is utilized for reducing noise during the shift from the standby state to operation state. The operating method is the same as the operating method relating to FIG. 27. Even here, there are no particular restrictions on the threshold voltage or gate dielectric thickness of the power switch PSW1, however an optimal selection should be made according to the voltage of VDD.

MTK-1005, [0125].

283. Here, the control signal CTLa from the CKT1 is provided to the “power switch controller PSC.” *See id.*, FIGS. 37-38. Based on the control signal CTLa, the voltages provided to the “power switch PSW1,” including the voltages VREF and VVDD2a, are optimized. *Id.*, [0126]-[0128]. Specifically, the voltages can be optimized to account for the operating state of the device and “variations (non-uniformities) in chip manufacture or information on environmental fluctuations, and the characteristics (or properties) of the circuit block CKT2a or CKT2b that changed due to these variations or fluctuation can be corrected.” *Id.*, [0126]; *see also id.*, [0128] (discussing corrections for “temperature and process conditions, etc.”). A POSITA would have understood and found obvious that such information would be provided via the “leakage control lines” like CTLa. Mizuno describes this process in further detail with respect to Figure 38.

The voltage regulator circuit can monitor the virtual power line VVDD2a or VVDD2b voltages and may regulate voltage by applying the desired VDD voltage

to the virtual power line even if the current consumption is large in circuit blocks CKT2a and CKT2b. When the circuit path from the power supply terminal of the chip to the circuit within the circuit block has a high impedance, a so-called IR drop occurs due to current consumption of the circuit block CKT2a or CKT2b. This IR drop can be prevented by the above described formula. The virtual power line VVDD2a or VVDD2b voltages can also be changed based on the information on variations (non-uniformities) in chip manufacture or information on environmental fluctuations, and the characteristics (or properties) of the circuit block CKT2a or CKT2b that changed due to these variations or fluctuation can be corrected.

The structure of FIG. 38 can also utilize the method for applying the voltage VFNL to the virtual power line VVDD during standby as in the structure in FIG. 17. The PSW2 of FIG. 38 is not required in this case. Two types of control methods may be used in this case. In the first method, the VDD voltage is applied to VREF during operation as described above, and the power supply voltage VDD is applied to the virtual power line VVDD2a. During standby the VFNL ($<VDD$) voltage is applied to VREF, and the voltage VFNL is supplied to the virtual power line VVDD2a. The voltage source VFNLGEN was required by the structure of FIG. 17, however this structure (FIG. 38) has the advantage of being able to use an operational amplifier OPAMP and power switch PSW1 instead. In the second method, besides the operational amplifier OPAMP and power switch PSW1, the voltage source VFNLGEN is installed on the virtual power line VVDD2a. During operation, a voltage VDD is applied to VREF as described above, and a voltage VDD is supplied to the virtual power line VVDD2a. During standby, 0 volts is applied to VREF, and the voltage VFNL is supplied to the virtual power line VVDD2a from the voltage source VFNLGEN.

Either method has the advantage that the virtual power line VVDD2a voltage during standby can be made a voltage close to VRTN by directly applying VFNL to

the virtual power line VVDD2a during standby state. The value of the directly applied VFNL voltage can also be directly controlled according to the voltage of power supply VDD, the temperature and process conditions, etc.

MTK-1005, [0126]-[0128].

284. Thus, even if claim 1 of the '077 Patent is construed to require that the “adaptive leakage controller” has the features of the “ALC 270” of Figure 2 of the '077 Patent, Mizuno discloses and renders obvious that element.

285. As noted above in my discussion of Takahashi, “power island” and “power manager” have been construed in prior litigations involving a patent describing similar subject matter, U.S. Patent No. 7,051,306. *See* MTK-1025 43-44, 44-46; MTK-1026 28-29, 29-34. In my opinion, no construction is necessary for the purposes of this proceeding because plain and ordinary meaning suffices. And while the prior constructions involved a different patent and different claims, Mizuno’s disclosures, in light of a POSITA’s knowledge, would also render these terms obvious under the prior constructions for the reasons discussed above with respect to element 1[p]. *See also* MTK-1001, 4:11-20; *see also id.*, 3:49-55; MTK-1005, [0121]; MTK-1006, 1:21-38.

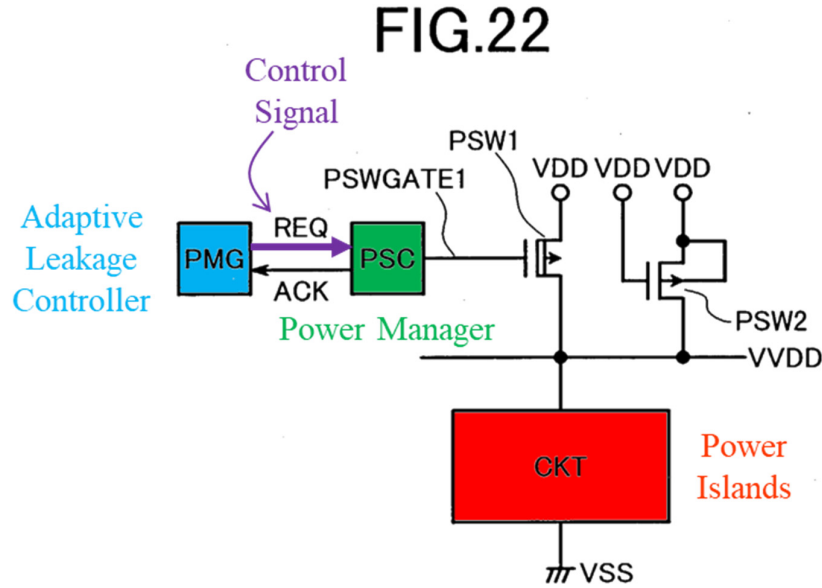
286. Therefore, to the extent the preamble of claim 1 of the '077 Patent is limiting, it is my opinion that Mizuno discloses and renders obvious the preamble of claim 1.

(b) Element 1[a]

287. Element 1[a] recites “receiving, at the power manager, a control signal from the adaptive leakage controller.” In my opinion, Mizuno discloses and renders obvious element 1[a].

288. As I explained with respect to the preamble of claim 1, it is my opinion that Mizuno discloses and otherwise renders obvious a power manager and adaptive leakage controller. Specifically, it is my opinion that in the embodiment of Figures 1-30, Mizuno’s “power switch controller PSC” discloses and renders obvious a power manager, and Mizuno’s “power controlling circuit PMG” discloses and renders obvious an adaptive leakage controller. Similarly, in the related embodiment of Figures 35-40, power managers are included in “leakage reduction circuits PSM2a and PSM2b,” which are in communication with a “circuit block CKT1” that “control[s] the leakage reduction circuits PSM2a and PSM2b.” *See* MTK-1005, [0121], [0131] (“Of course the various adaptations and specific examples disclosed for the first embodiment are also applicable to the leakage current reduction circuit of the third embodiment.”); element 1[p].

289. Mizuno’s “power switch controller PSC” that is a power manager receives a control signal “REQ” from the “power controlling circuit PMG” That is an adaptive leakage controller. MTK-1005, [0093]. As Mizuno explains, the control signal “REQ” controls the “power switch controller PSC” to set the voltage “PSWGATE1” either high or low. *Id.* In turn, the “power switch PSW1” is turned on or off to place the “circuit block CKT” into an active or standby state. *Id.*



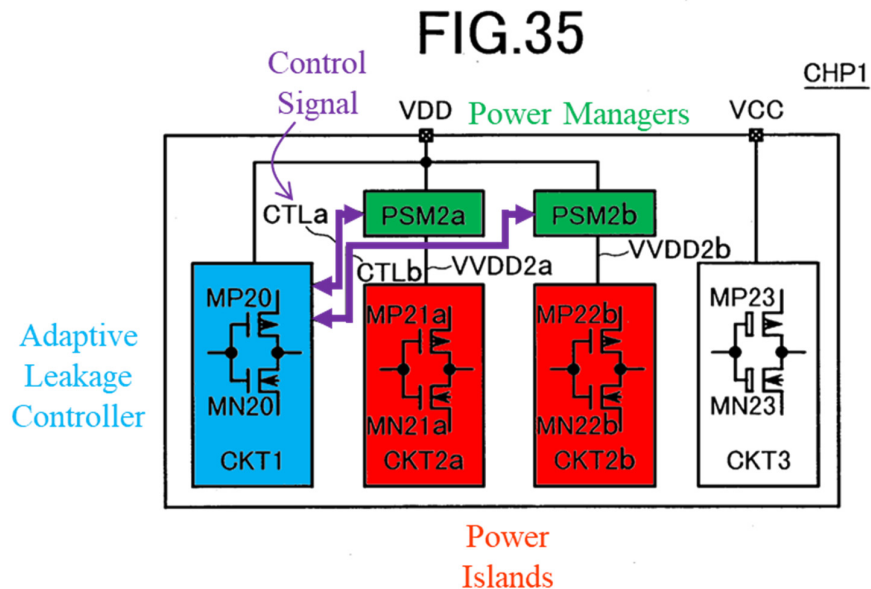
MTK-1005, FIG. 22 (annotated).

FIG. 22 is a structure of the interface for the power switch controller PSC. The power switch controller PSC that controls the power switch PSW1 and current source PSW2 implements control by means of a power controlling circuit PMG. This allows designing the circuit block CKT low-leak mechanism separately from the power controlling circuit PMG that reduces power consumption in the chip overall. A handshake between the power controlling circuit PMG and the power switch controller PSC by means of the request line REQ and response line ACK controls the on/off operation of the power switch PSW1 and controls the state of the circuit block. Here, setting the request line REQ to high level turns on the power switch PSW1 and controls the circuit block CKT in the operation state. After the power switch PSW1 turns fully on and the virtual power line VVDD is charged to the voltage potential of power supply VDD, when the response line ACK reaches high level, the external section of the power switch controller (power controlling circuit PMG) is notified that the circuit block CKT has switched to the operation state. Conversely, when the request line REQ is set to low level, the power switch PSW1 turns off and the circuit block is controlled to the

standby state. When the power switch PSW1 turns fully off, and the response line ACK switches to low level, the external section of the power switch controller is notified that the circuit block CKT has switched to the standby state.

MTK-1005, [0093].

290. The related embodiment of Figures 35-40 shows a similar control signal. There, the “circuit block CKT1” sends control signals “CTLa, CLTb” to the “leakage reduction circuits PSM2a and PSM2b.” *Id.*, [0121].



MTK-1005, FIG. 35 (annotated).

291. Mizuno explains that “CTLa, CTLb are leakage control lines of the leakage reduction circuit of the present invention and equivalent to the request line REQ and response line ACK of FIG. 22.” *Id.* As explained at element 1[p], the “circuit block CKT1” includes circuits for, *inter alia*, “control[ling] the leakage reduction circuits PSM2a and PSM2b.” *Id.* Thus, it is my opinion that a POSITA would understand and find obvious that in the embodiment of Figures 35-40, “leakage reduction circuits PSM2a and PSM2b” in green include power managers and the “circuit block CKT1” in blue is an adaptive leakage controller that provides a control signal to the power managers. *See id.*, [0125] (“The voltage regulator VDC and leak regulator circuit PSM2a or PSM2b components

in the example in FIG. 37 can be combined together ... as shown in FIG. 38), FIG. 38 (depicting a “power switch controller PSC”).

292. It is therefore my opinion that a POSITA would find that Mizuno discloses and renders obvious “receiving, at the power manager, a control signal from the adaptive leakage controller.”

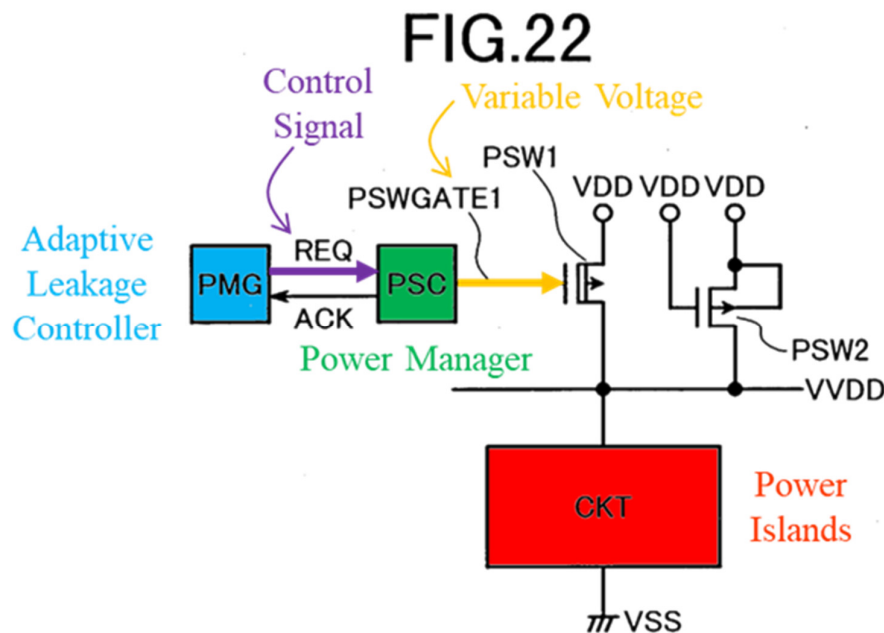
(c) Element 1[b]

293. Element 1[b] recites “employing the power manager to dynamically change power consumptions of the plurality of power islands, the employing the power manager to dynamically change power consumptions including: generating a variable voltage based on the control signal; and providing the variable voltage to at least one of low leakage sleep circuits of the integrated circuit.” In my opinion, Mizuno discloses and renders obvious element 1[b].

294. As explained with respect to elements 1[p] and 1[a], it is my opinion that Mizuno discloses and otherwise renders obvious a plurality of power islands and a power manager. Specifically, it is my opinion that in the embodiment of Figures 1-30, the circuit block CKT, and the “logic circuit LG1” and “memory MEM1” within the circuit block CKT, individually and collectively disclose and render obvious a plurality of power islands. Further, Mizuno’s “power switch controller PSC” discloses and renders obvious a power manager. In the related embodiment of Figures 35-40, each of the “leakage reduction circuits PSM2a and PSM2b” include a power manager (“power switch controller PSC”) for controlling power consumption within the power islands “[c]ircuit blocks CKT2a

and CKT2b.” See MTK-1005, [0121], [0131] (“Of course the various adaptations and specific examples disclosed for the first embodiment are also applicable to the leakage current reduction circuit of the third embodiment.”); elements 1[p], 1[a].

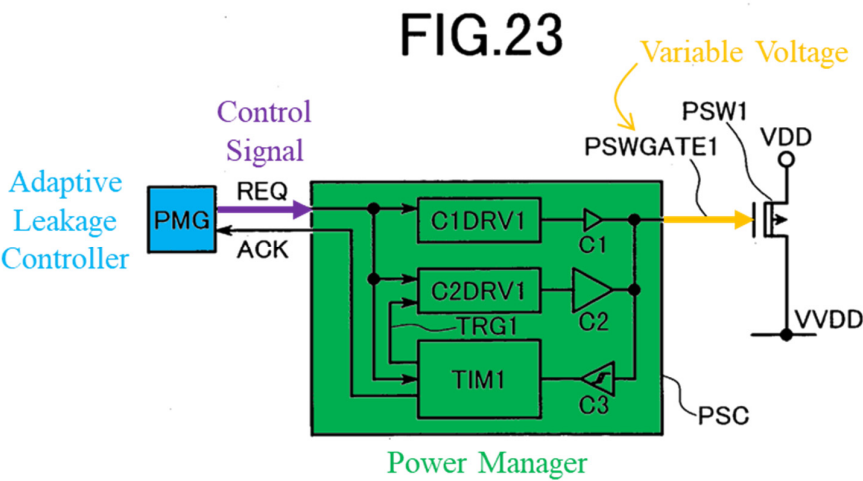
295. Turning to element 1[b], it is my opinion that Mizuno discloses that its “power switch controller PSC” (*i.e.*, power manager) “generat[es] a variable voltage based on the control signal” as required by claim 1. Specifically, the “power switch controller PSC” generates a variable voltage “PSWGATE1” based on the control signal “REQ” received from the “power controlling circuit PMG” that is an adaptive leakage controller.



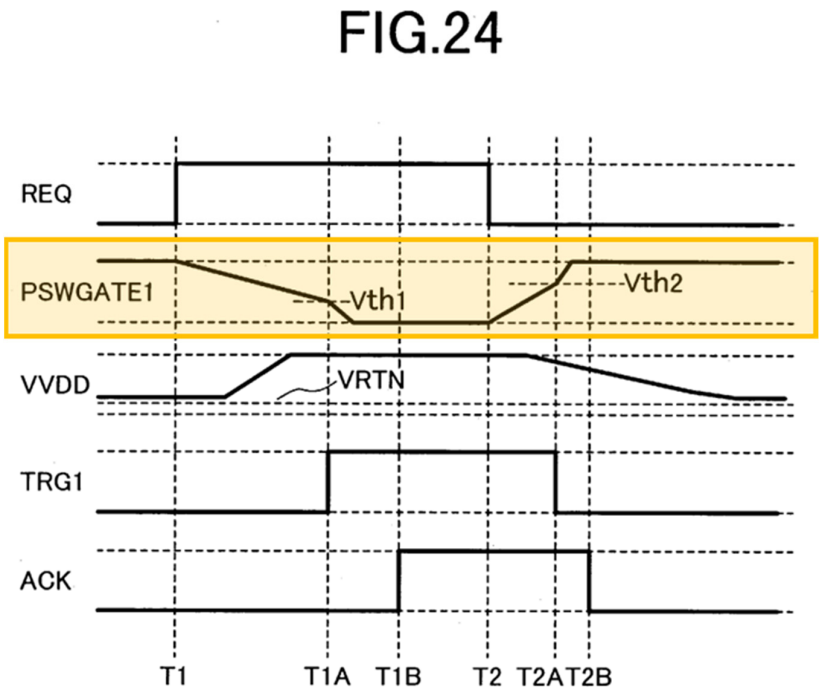
MTK-1005, FIG. 22 (annotated).

296. Figures 23-24 of Mizuno depict one example of the variable voltage “PSWGATE1.” There, in response to the control signal “REQ,” the “drive

circuits” C1DRV1 and C2DRV2 of the “power switch controller PSC” generate the voltage “PSWGATE1” that varies over time as shown in Figure 24. MTK-1005, [0095]-[0099].



MTK-1005, FIG. 23 (annotated).



MTK-1005, FIG. 24 (annotated).

FIG. 24 is a timing chart for the operation in FIG. 23. When operation has shifted from standby to the operation state and the request line REQ reaches high level, first of all the gate signal PSWGATE 1 is driven to high impedance by C1 by way of the C1DRV control circuit for C1. The potential detector C3 detects that the gate signal PSWGATE1 was driven to a level (V_{th1}) at time T1A, and TRG1 is driven to high level by the timer TIM1. The gate signal PSWGATE1 is in this way driven to a low impedance by C2 by way of the C2DRV control circuit for C2. The timer TM1 measures the time T_A from time T1 to T1A, and after a time T_B established using the specific relation (for example $\{\text{fraction } (1/2)\}$) with time T_A , (time T1B in the example in FIG. 24) the response line ACK is driven to high level. There are no particular restrictions on the timer characteristics (relation between time T_A and time T_B) however the gate signal PSWGATE1 is driven completely to low level at time T1B. Also the virtual power line VVDD may be fully charged up to the voltage potential of VDD.

MTK-1005, [0096].

297. The related embodiment of Figures 35-40 likewise shows that the variable voltage is generated in response to the control signal. As shown below, the “power switch controller PSC” receives the control signal “CTLa” that is “equivalent to the request line REQ and response line ACK” from the “circuit block CKT1.” *Id.*, [0121]. In response, the “power switch controller PSC” provides variable voltage VREF that results in the variable voltage PSWGATE2 that is provided to the “power switch PSW1.” *Id.*, [0125], [0127]. Similarly, the “power switch controller PSC” provides a variable voltage to VVDD2a based on the control signal “CTLa.” *Id.*

Variable
Voltages

CTLa

Control
Signal

VDD2O

PSW1s

PSC

OPAMP

PSWGATE2

VREF

VDD2

VDD2

VDD2

PSW1

PSW2

VVDD2a

CKT2a

VSS

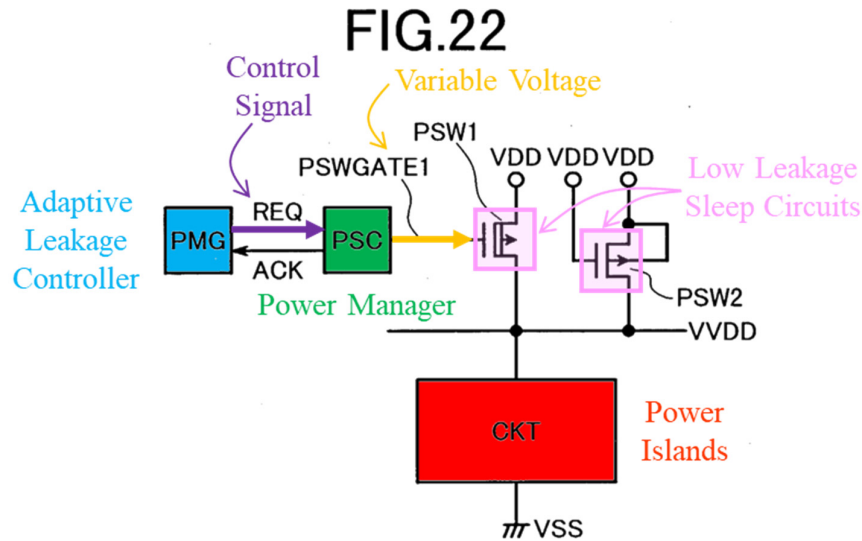
The voltage regulator VDC and leak regulator circuit PSM2a or PSM2b components in the example in FIG. 37 can be combined together. That structure is shown in FIG. 38. In the figure, PSW2 is the current source, OPAMP is the operational amplifier and VREF is the reference voltage. During operation, a voltage VDD can be supplied to the virtual power line VVDD2a by applying voltage VDD to VREF. To turn the power switch PSW1 off, VREF may be set to a sufficiently low voltage (for example below 0 volts). The power switch PSW1 has smaller drive power than the power switch PSW1. This is utilized for reducing noise during the shift from the standby state to operation state. The operating method is the same as the operating method relating to FIG. 27. Even here, there are no particular restrictions on the threshold voltage or gate dielectric thickness of the power switch PSW1, however an optimal selection should be made according to the voltage of VDD.

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The structure of FIG. 38 can also utilize the method for applying the voltage VFNL to the virtual power line VVDD during standby as in the structure in FIG. 17. The PSW2 of FIG. 38 is not required in this case. Two types of control methods may be used in this case. In the first method, the VDD voltage is applied to VREF during operation as described above, and the power supply voltage VDD is applied to the virtual power line VVDD2a. During standby the VFNL ($<VDD$) voltage is applied to VREF, and the voltage VFNL is supplied to the virtual power line VVDD2a. The voltage source VFNLGEN was required by the structure of FIG. 17, however this structure (FIG. 38) has the advantage of being able to use an operational amplifier OPAMP and power switch PSW1 instead. In the second method, besides the operational amplifier OPAMP and power switch PSW1, the voltage source VFNLGEN is installed on the virtual power line VVDD2a. During operation, a voltage VDD is applied to VREF as described above, and a voltage VDD is supplied to the virtual power line VVDD2a. During standby, 0 volts is applied to VREF, and the voltage VFNL is supplied to the virtual power line VVDD2a from the voltage source VFNLGEN.

Id., [0127].

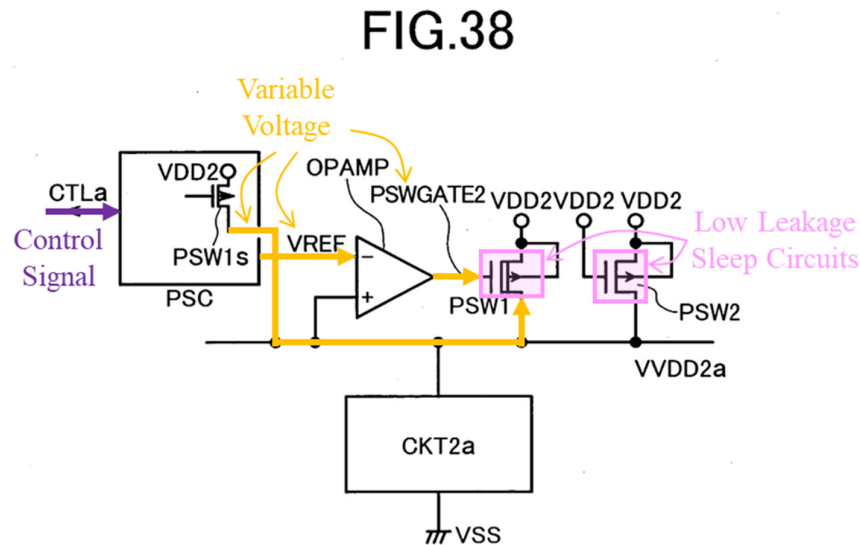
298. Mizuno further discloses and renders obvious “providing the variable voltage to at least one of low leakage sleep circuits of the integrated circuit.” Specifically, as shown in the embodiment of Figures 1-30, Mizuno’s “power switch controller PSC” provides the variable voltage “PSWGATE1” to the “power switch PSW1.” MTK-1005, [0054]-[0055].



MTK-1005, FIG. 22 (annotated).

299. Mizuno explains that when “PSWGATE1 of power switch PSW1 is driven to a low level by the power switch controller PSC ... the power switch PSW1 turns on. In this state, power is supplied to the circuit block CKT by way of the power switch PSW1 so that the virtual power line VVDD reaches VDD potential and the circuit block CKT is operable (in operating state).” *Id.*, [0055]. To put the “circuit block CKT” into standby mode, “the gate signal PSWGATE1 ... is driven to high level by the power switch controller PSC and the power switch PSW1 turns off.” *Id.*, [0055]. As a result, “the voltage of the virtual power line VVDD becomes lower.” *Id.* Thus, “the current supplied to the circuit block during standby operation is mainly supplied [by] the current source PSW2.” *Id.*, [0054]; *see also id.*, [0096]-[0098].

300. Similarly, in the embodiment of Figures 35-40, the variable voltage VREF output by the “power switch controller PSC” is provided to the “power switch PSW1” through the OPAMP, as is the variable voltage VVDD2a.



MTK-1005, FIG. 38 (annotated).

301. As with the related embodiment of Figures 1-30, the variable voltage provided to the “power switch PSW1” turns the “power switch PSW1” on and off depending on the voltage level. *Id.*, [0125]-[0127]. For example, “the VDD voltage is applied to VREF during operation as described above, and the power supply voltage VDD is applied to the virtual power line VVDD2a. During standby the VFNL (<VDD) voltage is applied to VREF, and the voltage VFNL is supplied to the virtual power line VVDD2a.” *Id.*, [0127]; *see also id.*, [0125] (“During operation, a voltage VDD can be supplied to the virtual power line VVDD2a by applying voltage VDD to VREF. To turn the power switch PSW1 off, VREF may be set to a sufficiently low voltage (for example below 0 volts).”).

302. In my opinion, the “power switch PSW1” and “current source PSW2” are each a low leakage sleep circuit. Mizuno explains that the leakage current through “power switch PSW1” during standby is substantially less than the current through “current source PSW2” (*i.e.*, “ $I_{\text{off}}(\text{PSW1}) \ll I_{\text{off}}(\text{PSW2})$ ”). *Id.*, [0057], [0085], [0093]. Specifically, as Mizuno places its “circuit block CKT” into standby (*i.e.*, sleep) mode, “[t]he leakage current flowing to circuit block CKT is listed as $I_{\text{off}}(\text{CKT})$ that was initially large (at time T1) also gradually becomes a smaller value (period from time T1 to T2).” *Id.*, [0055]. As such, the “current source PSW2 functions as a leak current limiter circuit for circuit block CKT.” *Id.*, [0057]. Moreover, by using multiple “leakage reduction circuits PSM2a and PSM2b” as in the embodiment of Figures 35-40, Mizuno “control[s] the leakage current of circuits grouped in multiple circuits integrated onto the chip, the leakage current of the overall chip can be efficiently reduced.” *Id.*, [0122].

303. Thus, a POSITA would have understood and found obvious that Mizuno’s “power switch PSW1” and “current source PSW2,” (like the “leakage reduction circuits PSM2a and PSM2b” in Figures 35-40) are low leakage sleep circuits that reduce leakage in the integrated circuit during standby. Indeed, while the ’077 Patent does not use the term “low leakage sleep circuit” in its specification, the ’077 Patent does disclose a “technique for reducing leakage [using] a sleep transistor” that “act[s] as a switch to turn on and off the logic gate.” MTK-1001, 2:9-20; *see also id.*, Abstract, 2:45-50, 4:21-5:7, 7:12-17.

Specifically, “the sleep transistor 130 is turned on (gate to VDD) during normal cell operation. When the cell is idle, the sleep transistor 130 is turned off (gate tied to VSS) to reduce the leakage current of the cell.” *Id.*, 2:9-20; *see also id.*, 7:8-17 (“FIGS. 5, 6, 7A-C, and 8A-8B disclose one embodiment for low leakage, data retention circuitry. In this embodiment, in sleep mode, the circuit parts of a flip-flop that do not require data retention are coupled to ground through a sleep transistor. The gate of the sleep transistor is coupled to a sleep signal that can be driven to a negative voltage such as $-0.3V$. Thus, the leakage in these circuit parts of the flip-flop is eliminated (reduced). When not in a sleep state, the sleep transistor has a gate value equal to or greater than the VDD supply, which effectively grounds the circuit.”). Mizuno’s “power switch PSW1” and “current source PSW2” (like the “leakage reduction circuits PSM2a and PSM2b”) operate in this same way to provide an operational voltage to the “circuit block CKT” during operation and reduce leakage current during standby.

304. As such, Mizuno’s integrated circuit “employ[s] the power manager to dynamically change power consumptions of the plurality of power islands” as required by claim 1. Specifically, as discussed above, Mizuno employs the “power switch controller PSC” to dynamically change the power consumption of the “circuit block CKT” during operational and standby states. *See, e.g.*, MTK-1005, [0087]-[0088] (“[t]he present invention is characterized in that power consumption due to leakage current in the circuit block during the standby state can be greatly reduced”), [0093], [0122]. For example, in the embodiment of

Figures 1-30, the voltage “VVDD” provided to the “logic circuit LG1” and “memory MEM1” power islands of the “circuit block CKT” during standby is drastically reduced from “VDD (1.0V)” to “VFNL (0.4V).” *Id.*, [0055]. As a result, the leakage current through the “circuit block CKT” (called “Ioff(CKT)”) also becomes a smaller value. *Id.*, [0055]; *see also id.*, [0060] (“the smaller the voltage of the virtual power line VVDD, the smaller the value Ioff(CKT) becomes”). Mizuno explains that, as a result of reducing the leakage current Ioff(CKT), “power consumption due to leakage current in the circuit block during the standby state can be greatly reduced.” *Id.*, [0087]; *see also id.*, Abstract. Mizuno discusses the same advantage with respect to the embodiment of Figures 35-40. There, the “leakage control circuits PSM2a and PSM2b” (which each include a “power switch controller PSC”) are configured to “control[] the leakage current of circuits grouped in multiple circuits integrated onto the chip,” such that “the leakage current of the overall chip can be efficiently reduced.” *Id.*, [0122].

305. Thus, it is my opinion that Mizuno discloses and renders obvious element 1[b]. Because Mizuno discloses or renders obvious each element of claim 1 of the '077 Patent, it is my opinion that Mizuno renders obvious claim 1.

3. Claim 2

306. Claim 2 recites “[t]he method as claimed in claim 1 further comprising putting to sleep and taking out of sleep, at different times, at least one of the power islands.” In my opinion, Mizuno renders obvious claim 2 of the '077 Patent.

307. As I discuss at element 1[b] above, Mizuno's "circuit blocks" (e.g., "circuit block 10" that includes "logic circuit LG1" and "memory MEM1") are put into standby and taken out of standby at different times to reduce power consumption when the "circuit blocks" are not being used. MTK-1005, [0087], [0093]. Specifically, the "power switch controller PSC" puts the "circuit blocks" (e.g., "circuit block CKT" including the "logic circuit LG1" and "memory MEM1") into standby or operational mode at different times by controlling "the on and off operation of the power switch PSW1." *Id.*, [0054]. By turning the "power switch PSW1" on and off, Mizuno controls the "current flow in the power supply VDD and the virtual power line VVDD." *Id.* Specifically, when the "power switch PSW1" turns on, the "virtual power line VVDD" is set to VDD and the "circuit block CKT" enters the operational state, *i.e.*, is "tak[en] out of sleep." Conversely, when the "power switch PSW1" turns off, the voltage at the "virtual power line VVDD" is reduced to put the "circuit block CKT" in standby mode, *i.e.*, is "put[] to sleep." *Id.*, [0054]-[0055]. A similar operation is used in the related embodiment of Figures 35-40 for the "leakage reduction circuits PSM2a and PSM2b" to put the "[c]ircuit blocks CKT2a and CKT2b" into standby and operational states. *Id.*, [0121]-[0134].

308. Moreover, I should note that Mizuno discloses two different forms of standby, both of which are sleep states. Specifically, Mizuno discloses a "standby (idle)" state that maintains "information within the information retention circuits within the circuit block," and also discloses a "deep stand-by

state” in which “information in the information retention circuit within the circuit block will be lost.” *Id.*, [0005], [0087]. As Mizuno explains, the benefit of the “deep stand-by state” is that power to the “circuit block CKT” can be reduced even further to achieve “lower power consumption than in stand-by state with data retention.” *Id.*, [0087].

The present invention is characterized in that power consumption due to leakage current in the circuit block during the standby state can be greatly reduced while still maintaining (keeping) the information within the information retention circuits within the circuit block. This standby function is here called the stand-by state with data retention. In addition to this stand-by state with data retention, the VFNL may be set to a smaller value (value of VRTN or lower) by reducing the current flowing in the current source PSW2 and reducing the voltage of the voltage source VFNLGEN (configuration in FIG. 17). The information in the information retention circuit within the circuit block will be lost in this structure, however a standby state (Called the deep stand-by state to distinguish it from the stand-by state with data retention. In these specifications, these terms are used to classify the two states.) having lower power consumption than in stand-by state with data retention can be achieved.

As one example, the structure of FIG. 18 shows an example for achieving the deep stand-by state of FIG. 14. In FIG. 18, the gate signal PSWGATE1a of the current source PSW2 is controlled by the power switch controller PSC. FIG. 19 is a timing chart showing an example of the operation in FIG. 18. In the stand-by state with data retention from time T1 to time T2, a low level is applied to the gate signal of current source PSW2 the same as the case of the structure in FIG. 14 by means of the power switch controller PSC. In the deep stand-by state from time T2 to time T3, a high level is applied to the gate signal of the current source PSW2 by the power switch controller PSC. In the deep

stand-by state, $I(\text{PSW2})$ is determined by the on current of PMOS transistor PSW2 and the VFNL is determined by the interaction between this on-current and $I_{\text{off}}(\text{CKT})$, and the condition $\text{VFNL} > \text{VRTN}$ satisfied. However, since the PMOS transistor PSW2 is off from time T2 to time T3, the value of VFNL is nearly zero (of course, a value below VRTN). Though information cannot be held in the information retention circuits during deep stand-by state, the deep stand-by state has the advantage of lower leakage current than the stand-by state with data retention. If retention of information in the information retention circuits is not required, then power consumption can be reduced even further by changing to the deep stand-by state.

MTK-1005, [0087]-[0088].

309. In my opinion, a POSITA would understand that both the “standby” and “deep standby” states are a “sleep state.” The ’077 Patent describes “sleep states” as those in which a circuit is not operational but has “low leakage.” *See* MTK-1001, Abstract, 2:37-50, 7:8-28. Further, the ’077 Patent describes a “sleep state” in which the “circuitry also retains data” as well as a “sleep state” for “circuitries that do not require data retention.” *See id.*, Abstract, 9:65-10:9. These states correspond to the “standby” and “deep standby” states of Mizuno, respectively. *See* MTK-1005, [0087]-[0088]. Other references from the same timeframe similarly describe such states as “sleep states.” *See, e.g.*, MTK-1018, 1:37-45 (“Leakage power consumption has become a major design concern for sub-micron transistors especially in low power applications, e.g., portable computers. For example, in portable computers with battery operation, leakage power consumption may shorten the life of the battery. Consequently, techniques

have been developed to mitigate leakage power consumption such as during the power saving mode of operation commonly referred to as ‘sleep mode’ or ‘sleep state.’”).

310. While not expressly recited by claim 2, to the extent that claim 2 requires putting power islands into sleep and out of sleep at different times from other power islands, it is my opinion that Mizuno renders obvious claim 2. As I discussed above at element 1[b], for example, the embodiment of Figures 35-40 includes multiple “leakage controls circuits PSM2a and PSM2b” that control “the leakage current of circuits grouped in multiple circuits integrated onto the chip.” MTK-1005, [0121]-[0122]. Mizuno explains that the “leakage control circuits PSM2a and PSM2b” are controlled by “CTLa, CTLb [that] are leakage control lines of the leakage reduction circuit of the present invention and equivalent to the request line REQ and response line ACK of FIG. 22.” *Id.*, [0122]. In my opinion, a POSITA would have understood and found obvious that the “circuit block CKT1” could place a particular circuit block (*e.g.*, one of “[c]ircuit blocks CKT2a and CKT2b”) into the standby or operational state at a different time from another using the control lines “CTLa, CTLb.” *Id.*, [0121]-[0122]. For example, when the “circuit block CKT1” sets the control line “CTLa” high and sets the control line “CTLb” low, the circuit block “CKT2a” would go to the operational state and the circuit block “CKT2b” would go into the standby state. *Id.*, [0093], [0121].

311. For these reasons, it is my opinion that Mizuno renders obvious claim 2.

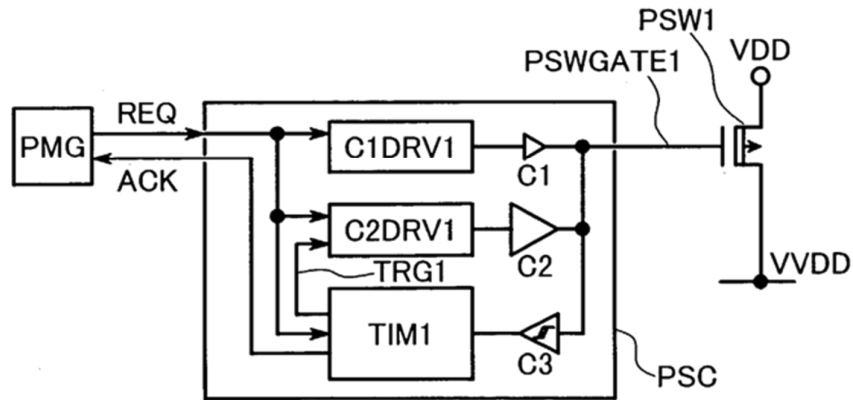
4. Claim 3

312. Claim 3 recites “[t]he method as claimed in claim 2 wherein the power manager employs a state machine to control the putting to sleep and the taking out of sleep.” In my opinion, Mizuno renders obvious claim 3 of the ’077 Patent.

313. As I explained with respect to element 1[p] above, Mizuno’s “power switch controller PSC” discloses and renders obvious a power manager. A POSITA would have further understood and found obvious that Mizuno’s “power switch controller PSC” employs a state machine to control putting a power island (*e.g.*, the “circuit block CKT” including its “logic circuit LG1” and/or “memory MEM1”) into standby (*i.e.*, “sleep”) and operational (*i.e.*, “out of sleep”) states.

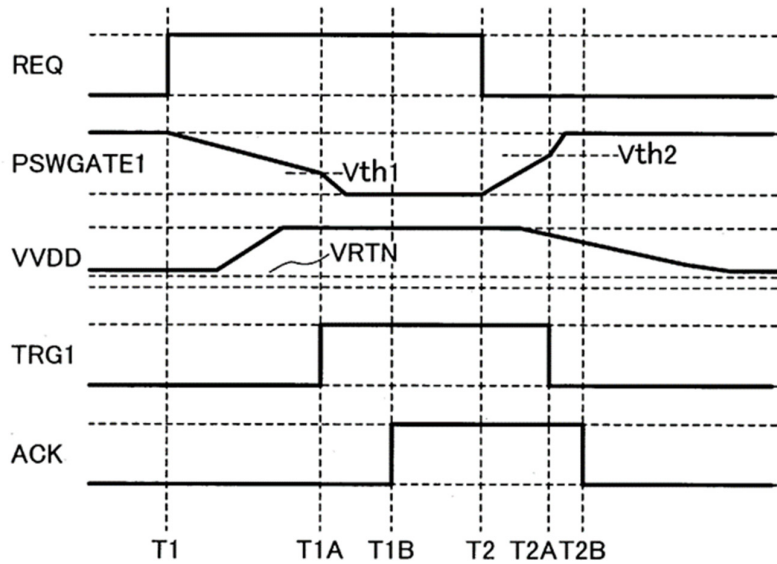
314. The embodiment of Figures 1-30 of Mizuno discloses and renders obvious the claimed state machine. With respect to Figures 23-24, for example, Mizuno explains that when the control signal “REQ reaches high level,” it initiates a “shift[] from standby to the operation state” (time T1). MTK-1005, [0096]. At this time (time T1), the “power switch controller PSC” enters a first state in which “the gate signal PSWGATE1 is driven to high impedance by C1 by way of the C1DRV control circuit.” *Id.*

FIG.23



MTK-1005, FIG. 23.

FIG.24



MTK-1005, FIG. 24.

315. This continues until “PSWGATE1” reaches a “level (V_{th1}) at time T1A,” at which point (time T1A) the “power switch controller PSC” enters a second state in which “PSWGATE1 is ... driven to a low impedance by C2 by

way of the C2DRV control circuit” and “TRG1 is driven to high level by the timer TIM1.” *Id.* After “a time TB” (at time T1B), the “power switch controller PSC” then enters a third state in which “ACK is driven to high level” and “the virtual power line VVDD may be fully charged up to the voltage potential of VDD.” *Id.*

316. Mizuno goes on to describe a similar state machine process for the “shift[] from the operation state to standby state.” *See id.*, [0097]-[0101].

When operation has shifted from the operation state to standby state, and the request line REQ reaches low level at time T2.

The gate signal PSWGATE1 is then first of all driven to high impedance by C1, by way of the C1DRV control circuit for C1. The potential detector C3 detects that the gate signal PSWGATE1 was driven to a level V_{th2} at time T2A, and TRG1 is driven to low level by the timer TIM1. The gate signal PSWGATE1 is in this way driven to a low impedance by C2 by way of the C2DRV control circuit for C2. Based on the time from time T2 to time T2A, the timer drives the response line ACK to low level after a certain time (time T2B). There are no particular restrictions on the timer characteristics (relation between time TA' from time T2B to time T2A and time TTB' from time T2A to time T2B) and even a time for example of TA'/TB' 2 is satisfactory.

MTK-1005, [0097]-[0098].

317. In related Figures 25-30, Mizuno discloses similar configurations of the “power switch controller PSC” that also utilize a state machine to control putting the power islands into standby (*i.e.*, “sleep”) and operational (*i.e.*, “taking out of sleep”) states. A POSITA would have understood and found obvious that

each of these configurations of the “power switch controller PSC” utilizes a state machine.

318. Indeed, Mizuno’s “power switch controller PSC” functions in the same way as the ’077 Patent’s claimed “state machine” that “performs the timing” when transitioning between sleep and operational states. MTK-1001, 6:19-21; *see also id.*, 6:38-55. Moreover, in my opinion a POSITA would have understood that Mizuno’s “power switch controller PSC” is a state machine as that term is understood in the art at the time of the ’077 Patent. *See, e.g.*, MTK-1008 (defining “state machine” as a “circuit containing several different states reachable from each other, with state changes happening synchronously”). For example, the 2001 textbook *Computer Systems Organization & Architecture* from John D. Carpinelli (MTK-1009) describes state machines in which “[i]nputs to the state machine are combined with the current state of the machine to determine the new state, or next state of the machine. Depending on the type of machine, outputs are generated based on either the state of the machine, or the state of the machine and the machine inputs.” MTK-1009 at 51.

319. In comparison with these definitions of the term “state machine,” In Mizuno, the outputs of the “power switch controller PSC” (*e.g.*, “PSWGATE1”) depend on the current status of the “power switch controller PSC” and its inputs (*e.g.*, in Figures 23-24, the control signal “REQ” and “potential detector C3” input measuring “PSWGATE1,” and in Figures 25-30 the additional input “SENS1” or “SENS2” measuring the “virtual voltage line VVDD”). Specifically,

the “power switch controller PSC” has distinct output states, *e.g.*, for “PSWGATE1,” to place the “circuit block CKT” into standby (“sleep”) or operational (“out of sleep”) states. Any transitions in the output state of the “power switch controller PSC” are triggered by a change (*i.e.*, either a rising edge or a falling edge) in the REQ signal issued by the “power controlling circuit PMG.” At the precise time of change in the REQ signal (T1 in Figure 24 above), the “PSWGATE1” signal starts transitioning, in turn causing the transitioning of VVDD. Specifically, as shown in Figure 24 above, PSWGATE1 reaches threshold voltage Vth1 allowing VVDD to rise and eventually reach VDD. That is to say, the “power switch controller PSC” employs a state machine with different output states for putting the “circuit block CKT” into standby (“sleep”) and operation (“taking out of sleep”) that change from one state to the other synchronously with the change in the REQ signal. This manner of operation for the “power switch controller PSC” is consistent with the commonly known definitions of the term “state machine” stated above.

320. Thus, it is my opinion that a POSITA would have understood and found obvious that Mizuno’s “power switch controller PSC” employs a state machine to control putting the “circuit block CKT” into standby (*i.e.*, “sleep”) and operational (*i.e.*, “out of sleep”) states.

5. Claim 4

321. Claim 4 recites “[t]he method as claimed in claim 1 wherein the variable voltage is an optimum voltage.” In my opinion, Mizuno renders obvious claim 4 of the ’077 Patent.

322. As I explained with respect to element 1[b] above, Mizuno discloses and renders obvious a power manager that generates a variable voltage. For example, in the embodiment of Figures 1-30, Mizuno’s “power switch controller PSC” is a power manager that generates a variable voltage PSWGATE1, and in the embodiment of Figures 35-40, the “power switch controller PSC” of the “leakage reduction circuits PSM2a and PSM2b” generates the variable voltage VREF that results in the variable voltage PSWGATE2. Further, in the embodiment of Figures 35-40, the “power switch controller PSC” generates a variable voltage provided to the “virtual power line VVDD2a.”

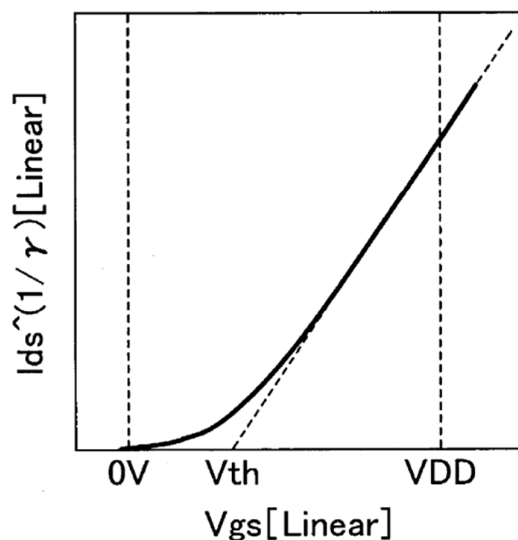
323. Mizuno further renders obvious that each of these variable voltages is an optimum voltage. In the embodiment of Figures 1-30, when “gate signal PSWGATE1 of power switch PSW1 is driven to low level by the power switch controller PSC ... the power switch PSW1 turns on. In this state, power is supplied to the circuit block CKT by way of the power switch PSW1 so that the virtual power line VVDD reaches VDD potential and the circuit block CKT is operable (in operating state).” MTK-1005, [0055]. Conversely, when “the gate signal PSWGATE1 of power switch PSW1 is driven to high level by the power switch controller PSC ... the power switch PSW1 turns off” And the “circuit block CKT” enters the standby state. *Id.* Thus, the levels of the variable voltage

PSWGATE1 (like VREF and PSWGATE2 in the embodiment of Figures 35-40) are optimized to be above or below the threshold voltage of the “power switch PSW1” transistor to turn the switch on or off. Mizuno describes how this threshold voltage is determined to optimize the value of PSWGATE1.

In these specifications, the MOS transistor threshold voltage V_{th} is the gate voltage when the MOS transistor drain current (This current does not include the subthreshold leak current.) starts to flow. This V_{th} is determined by the following widely used definitions. In a saturation region where the gate voltage V_{gs} is sufficiently large and the drain voltage V_{ds} is also sufficiently large, the drain current I_{ds} is proportional to the y power of $(V_{gs}-V_{th})$. The $1/y$ power of drain current I_{ds} therefore forms a straight line at a sufficiently large gate voltage V_{gs} as shown in FIG. 41. Therefore, the threshold voltage V_{th} can be found from a tangent of the direct line portion of the $1/y$ power of $(V_{gs}-V_{th})$ set as shown in FIG. 41. The value of y is greatly dependent on the gate length of the MOS transistor. In a long-channel MOS transistor having a gate length L_g of approximately $1\mu\text{m}$, the value of y is approximately 2. In a short-channel MOS transistor with a gate length L_g below $0.25\mu\text{m}$, the value of y is smaller than 2 and is for example a value of approximately 1.4.

MTK-1005, [0058].

FIG.41



MTK-1005, FIG. 41; *see also id.*, FIG. 3.

324. Mizuno further explains that the threshold voltage of the “power switch PSW1” depends in part upon the structure and process used to fabricate it. MTK-1005, [0090]. For example, Mizuno discusses balancing the “tradeoffs” between the “on-resistance per surface area of power switch PSW1 during operation” and the “gate tunneling leakage current” during standby. *Id.* Mizuno proposes a structure with “a thick gate dielectric film for the MOS transistors comprising the power switch PSW1 compared to the MOS transistors comprising the circuit block CKT,” because using this structure for “power switch PSW1” requires “a voltage amplitude to the gate terminal of power switch PSW1 that is larger than power supply VDD.” *Id.* Mizuno explains that such a structure for the “power switch PSW1” is advantageous because its “on-resistance during

operation can ... be reduced and a power switch with a sufficiently small leakage current during standby can be obtained.” *Id.*; *see also id.*, [0125]. Thus, to operate the “power switch PSW1,” Mizuno’s “power switch controller PSC” generates an optimum voltage that is sufficiently above or below the threshold voltage of the “power switch PSW1” to turn on the switch with limited on-resistance during operation and turn off the switch with minimal leakage current during standby. *Id.*

325. Mizuno further describes optimizing the variable voltage PSWGATE1 to achieve a reverse bias of the “power switch PSW1” to further reduce leakage current during standby. Specifically, Mizuno explains that the current during standby is dominated by the “current source PSW2,” such that “ $I_{\text{off}}(\text{PSW1}) \ll I_{\text{off}}(\text{PSW2})$ ” (*i.e.*, that the current through PSW1 is much less than the current through PSW2). *Id.*, [0057], [0079]. “The condition $I_{\text{off}}(\text{PSW1}) \ll I(\text{PSW2})$ can be satisfied by selecting device parameters for the power switch PSW1 and the current source PSW2” and “overdriv[ing] the power switch PSW1 gate signal up to $V_{\text{DD}} + a$ during standby” as shown in Figures 12 and 13. MTK-1005, [0079]. “A reverse bias voltage is in this way applied across the source-drain of power switch PSW1 and the $I_{\text{off}}(\text{PSW1})$ becomes small. This is one more method for achieving the $I_{\text{off}}(\text{PSW1}) \ll I(\text{PSW2})$ condition.” *Id.*

FIG.12

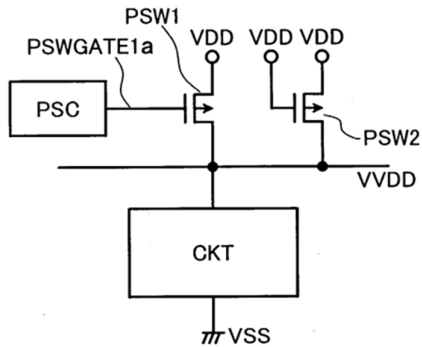
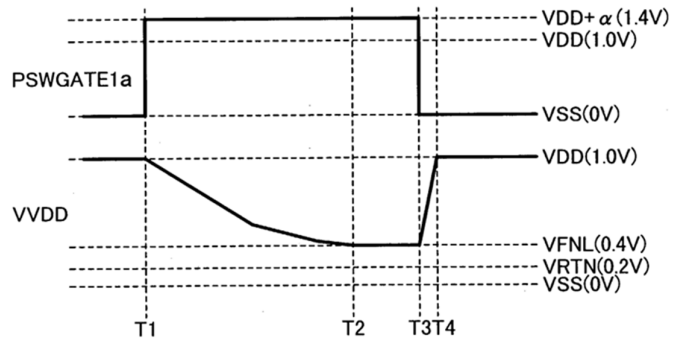


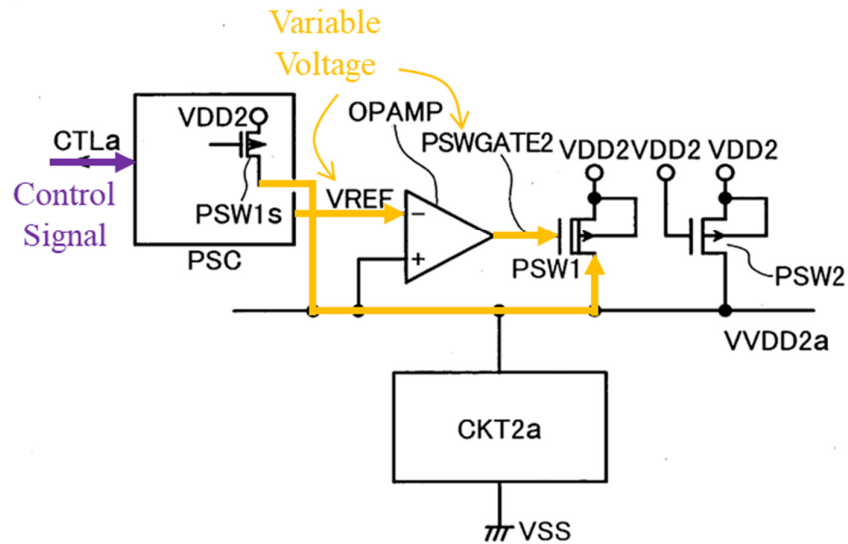
FIG.13



MTK-1005, FIGS. 12-13.

326. Likewise, in the related embodiment of Figures 35-40, the “power switch controller PSC” varies VREF and thus PSWGATE2 to optimize it for the operation of the integrated circuit. Moreover, in this embodiment, the variable voltage generated by the “power switch controller PSC” and provided to the “virtual power line VVDD2a” is optimized for the “circuit block CKT2a” that it powers.

FIG.38



MTK-1005, FIG. 38 (annotated).

The voltage regulator VDC and leak regulator circuit PSM2a or PSM2b components in the example in FIG. 37 can be combined together. That structure is shown in FIG. 38. In the figure, PSW2 is the current source, OPAMP is the operational amplifier and VREF is the reference voltage. ***During operation, a voltage VDD can be supplied to the virtual power line VVDD2a by applying voltage VDD to VREF. To turn the power switch PSW1 off, VREF may be set to a sufficiently low voltage (for example below 0 volts).*** The power switch PSW1 has smaller drive power than the power switch PSW1. This is utilized for reducing noise during the shift from the standby state to operation state. The operating method is the same as the operating method relating to FIG. 27. ***Even here, there are no particular restrictions on the threshold voltage or gate dielectric thickness of the power switch PSW1, however an optimal selection should be made according to the voltage of VDD.***

The voltage regulator circuit can monitor the virtual power line VVDD2a or VVDD2b voltages and may regulate voltage by applying the desired VDD voltage

to the virtual power line even if the current consumption is large in circuit blocks CKT2a and CKT2b. When the circuit path from the power supply terminal of the chip to the circuit within the circuit block has a high impedance, a so-called IR drop occurs due to current consumption of the circuit block CKT2a or CKT2b. This IR drop can be prevented by the above described formula. ***The virtual power line VVDD2a or VVDD2b voltages can also be changed based on the information on variations (non-uniformities) in chip manufacture or information on environmental fluctuations, and the characteristics (or properties) of the circuit block CKT2a or CKT2b that changed due to these variations or fluctuation can be corrected.***

MTK-1005, [0125]-[0126] (emphasis added).

327. Thus, in my opinion a POSITA would have understood and found obvious that Mizuno's variable voltage (*i.e.*, PSWGATE1 in Figures 1-30 and VREF that results in PSWGATE2 in Figures 35-40) is an optimum voltage.⁷

6. Claim 5

328. Claim 5 recites “[t]he method as claimed in claim 4 wherein the optimum voltage is dependent upon both process variation and temperature variation.” In my opinion, Mizuno renders obvious claim 5 of the '077 Patent.

⁷ It is my understanding that claim 4 does not require that the “variable voltage” is optimized based on temperature and/or process variations. This understanding comports with the claims in part because claim 5 separately recites that the “variable voltage” is optimized “dependent upon both process variation and temperature variation.” However, to the extent that the “variable voltage” of claim 4 must be optimized based on temperature and/or process variations, in my opinion Mizuno renders obvious claim 4 for the reasons stated here with respect to claim 4 and below with respect to claim 5.

329. As explained at element 1[b] and claim 4 above, it is my opinion that Mizuno's PSWGATE1 (in the embodiment of Figures 1-30, which is similarly referred to as VREF and PSWGATE2 in the embodiment of Figures 35-40), is a variable voltage that is optimized for the performance of the integrated circuit, *e.g.*, to reduce on-resistance during operation and reduce leakage current during standby. *See* MTK-1005, [0090]. In my view, a POSITA would have found it obvious in view of Mizuno to optimize this variable voltage depending on both process variation and temperature variation.

330. Specifically, as I discussed at claim 4 above, Mizuno optimizes the voltage PSWGATE1 for the process used to fabricate the "power switch PSW1." *See id.*, [0057], [0079], [0090], [0125]. Thus, Mizuno discloses optimizing PSWGATE1 based on variations in the process used to fabricate the transistor in the "power switch PSW1."

331. Moreover, as I discussed at claim 5 of Ground 1A based on Takahashi, it was well-known before the '077 Patent that transistor performance is dependent upon process and temperature variations. Indeed, Mizuno discloses adjusting the voltages applied to the transistors of the "circuit block CKT" to account for process and temperature variations, as shown below.

Though there are no particular restrictions on the substrate bias signal VBP and VBN voltages during operation, a low voltage may be applied to VBP (for example, VDD or a lower voltage) and a high voltage may be applied to VBN (for example VSS or a higher voltage) to achieve high speed circuit block CKT operation. *An optimal voltage may be applied to the*

substrate bias signal VBP, VBN according to the high speed operation needed in the circuit block CKT. Typical inverter INV configurations (structures) within the circuit block CKT were shown in FIG. 8 and FIG. 11. These however showed nothing more than typical CMOS logic circuits and needless to say, can be applied to various circuits containing information retention circuits such as shown in the circuit block of FIG. 1. In substrate bias control in particular, if the substrate bias voltage value applied to the MOS transistor substrate is determined according to the process, temperature and power supply voltage, then irregularities in the process and fluctuations in the temperature and power supply voltage can be compensated and VRTN made a smaller value.

MTK-1005, [0077] (emphasis added).

FIG. 17 is another example for setting the VFNL during standby. In FIG. 17, the voltage source VFNLGEN generates a VFNL of a specified voltage drop and drives the virtual power line VVDD. In the operating state, power is supplied to the circuit block by the power switch PSW1 and in standby state power is supplied to the circuit block by the voltage source VFNLGEN. During standby, the value of VFNL generated from the voltage source VFNLGEN may be a value of VRTN or more. Needless to say however, the lower the voltage, the smaller the value of leakage current that can be obtained from the circuit block CKT during standby. There are no particular restrictions on the configuration (structure) of the voltage source VFNLGEN. When the voltage source VFNLGEN is integrated onto the same chip holding the circuit block CKT, then a structure for generating a specific VFNL can be achieved for example by utilizing a voltage regulator of the known art with the power supply VDD. The voltage source VFNLGEN may also be installed outside of that chip. When directly generating VFNL from the voltage source VFNLGEN as shown in FIG. 17, a design can be achieved for making the voltage of the virtual power line VVDD close to that of VRTN. ***The output voltage VFNL of the voltage source***

VFNLGEN may also be automatically controlled according to the power supply VDD voltage, temperature and process conditions, etc.

MTK-1005, [0086] (emphasis added).

The voltage regulator circuit can monitor the virtual power line VVDD2a or VVDD2b voltages and may regulate voltage by applying the desired VDD voltage to the virtual power line even if the current consumption is large in circuit blocks CKT2a and CKT2b. When the circuit path from the power supply terminal of the chip to the circuit within the circuit block has a high impedance, a so-called IR drop occurs due to current consumption of the circuit block CKT2a or CKT2b. This IR drop can be prevented by the above described formula. ***The virtual power line VVDD2a or VVDD2b voltages can also be changed based on the information on variations (non-uniformities) in chip manufacture or information on environmental fluctuations, and the characteristics (or properties) of the circuit block CKT2a or CKT2b that changed due to these variations or fluctuation can be corrected.***

MTK-1005, [0125] (emphasis added); *see also id.*, [0064], [0076], [0080]-[0081], [0128] (describing similar voltage adjustments to account for variations in process and temperature).

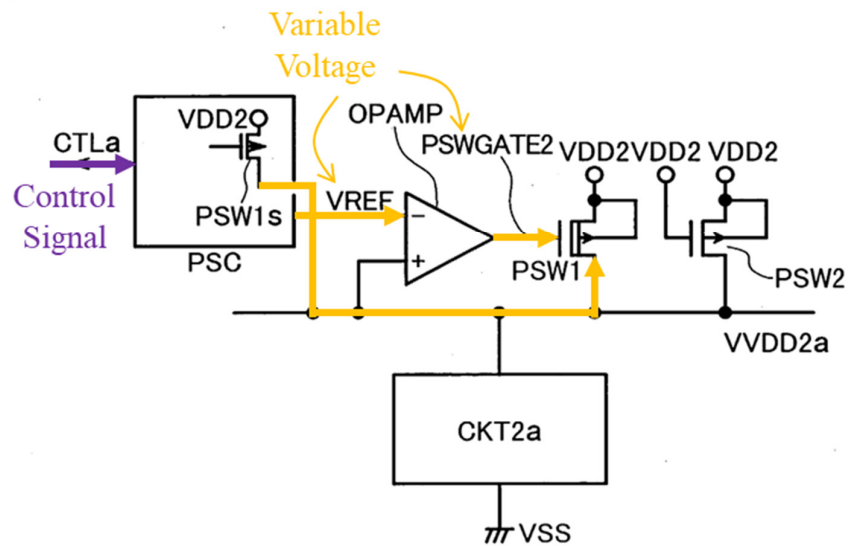
332. Mizuno also acknowledges that these variations also impact the performance of the transistors in the “power switch PSW1” and “current source PSW2.” *Id.*, [0091]. Specifically, Mizuno describes designing the structure (*e.g.*, gate length) of the transistors in “power switch PSW1” and “current source PSW2” to “allow[] lowering variations in the threshold [voltage] that occur in the process” of manufacturing those transistors. *Id.* Specifically, by making the gate lengths of the transistors in “PSW1” and “PSW2” “thicker than the gate length of

the MOS transistor comprising the circuit block CKT,” “the leakage current flow in the circuit block during standby due to process variations can also be reduced” with greater efficacy. *Id.*

333. Therefore, a POSITA would have found it obvious to apply Mizuno’s teachings to optimize the voltages applied to the “power switch PSW1” and “current source PSW2” based on process variation and temperature variation. Optimizing the variable PSWGATE1 voltage applied to the “power switch PSW1” based on process variation and temperature variation would achieve Mizuno’s stated goal of efficiently controlling the “power switch PSW1” so that “on-resistance during operation can ... be reduced and a power switch with a sufficiently small leakage current during standby can be obtained.” *Id.*, [0090].

334. Similarly, in the embodiment of Figures 35-40, the variable voltage generated by the “power switch controller PSC” and provided to the “virtual power line VVDD2a” is optimized based on “variations (non-uniformities) in chip manufacture” and “environmental fluctuations” that a POSITA would understand are process and temperature variations.

FIG.38



MTK-1005, FIG. 38 (annotated).

The voltage regulator circuit can monitor the virtual power line VVDD2a or VVDD2b voltages and may regulate voltage by applying the desired VDD voltage to the virtual power line even if the current consumption is large in circuit blocks CKT2a and CKT2b. When the circuit path from the power supply terminal of the chip to the circuit within the circuit block has a high impedance, a so-called IR drop occurs due to current consumption of the circuit block CKT2a or CKT2b. This IR drop can be prevented by the above described formula. ***The virtual power line VVDD2a or VVDD2b voltages can also be changed based on the information on variations (non-uniformities) in chip manufacture or information on environmental fluctuations, and the characteristics (or properties) of the circuit block CKT2a or CKT2b that changed due to these variations or fluctuation can be corrected.***

MTK-1005, [0126] (emphasis added).

335. It is therefore my opinion that Mizuno renders obvious claim 5 of the '077 Patent.

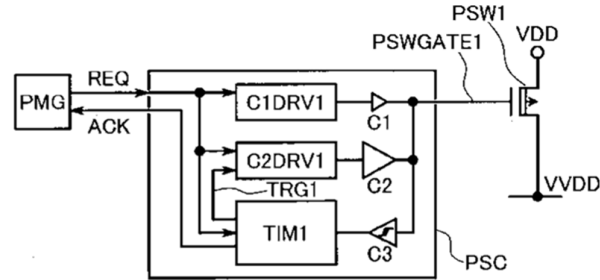
7. Claim 6

336. Claim 6 recites “[t]he method as claimed in claim 4 wherein the optimum voltage is generated by a sleep generator.” In my opinion, Mizuno renders obvious claim 6 of the ’077 Patent.

337. As I discussed above at elements 1[p] and 1[b] and claim 4, Mizuno’s “power switch controller PSC” discloses and renders obvious a power manager that generates an optimized variable voltage. In the related embodiments of Figures 1-30 and 35-40, the optimized variable voltage is PSWGATE1 (referred to as VREF that results in PSWGATE2 in Figures 35-40). Further, in the embodiment of Figures 35-40, the “power switch controller PSC” also generates a voltage for the “virtual power line VVDD2a” as shown in Figure 38.

338. Mizuno’s “power switch controller PSC” further renders obvious that the optimized variable voltage is generated by a sleep generator. For example, Figure 23 of Mizuno (and related Figures 25, 27, and 29) depicts the “power switch controller PSC” in additional detail. As Mizuno explains, during standby the “gate signal PSWGATE1” is “first of all driven to high impedance by C1, by way of the C1DRV control circuit for C1.” Once the “potential detector C3 detects that the gate signal PSWGATE1 was driven to a level V_{th2} ,” then the “PSWGATE1 is ... driven to a low impedance by C2 by way of the C2DRV control circuit for C2.” *Id.*; *see also id.*, [0095], [0103]-[0106].

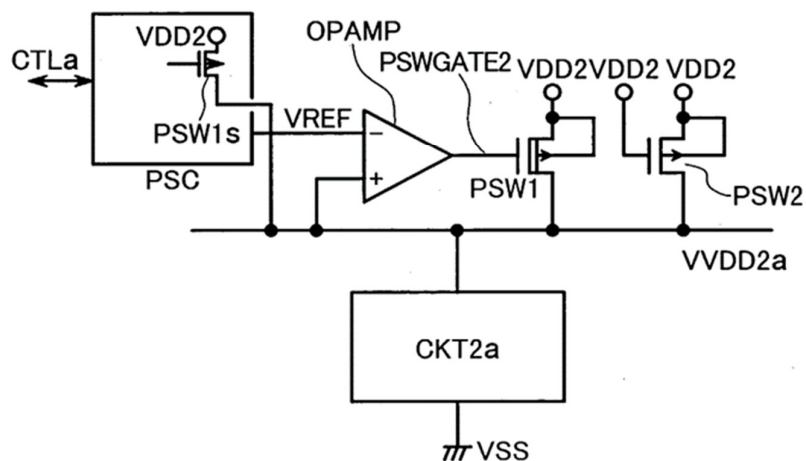
FIG.23



MTK-1005, FIG. 23.

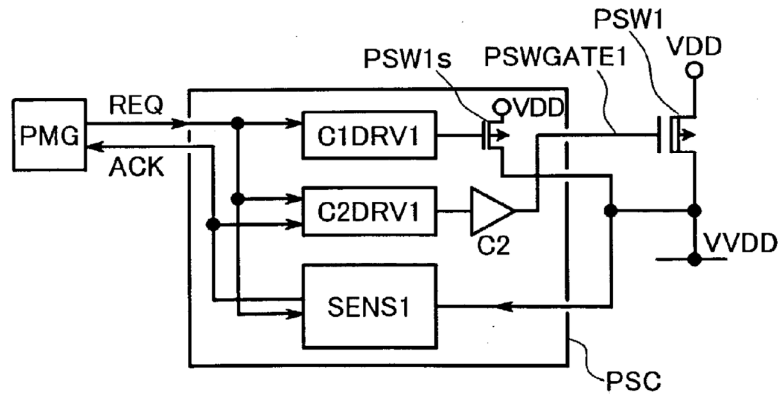
339. Similarly, in the related embodiment of Figures 35-40, Mizuno discloses that the voltage VVDD2a provided to the “power switch PSW1” is generated through the “power switch PSW1s” (e.g., VDD during an active state, or lower voltage during standby), as shown in Figure 38 and related figures 27-30.

FIG.38



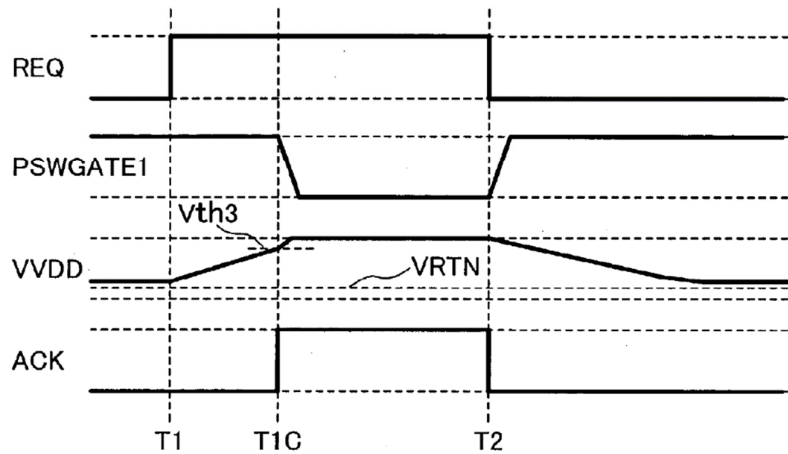
MTK-1005, FIG. 38.

FIG.27



MTK-1005, FIG. 27.

FIG.28



MTK-1005, FIG. 28; *see also* MTK-1005, FIGS. 29-30.

340. While the '077 Patent does not describe specific requirements for its “sleep generator,” it describes it as a component of the “power island manager.” *See* MTK-1001, FIG. 3, 5:8-13. Likewise, the “power switch controller PSC” includes components (*e.g.*, the drive circuits C1, C2, and/or power switch PSW1s) for generating the optimized variable voltages in Mizuno.

341. It is therefore my opinion that a POSITA would have understood and found obvious that Mizuno’s “power switch controller PSC” includes a sleep generator for generating the optimum voltage.

8. Claim 7

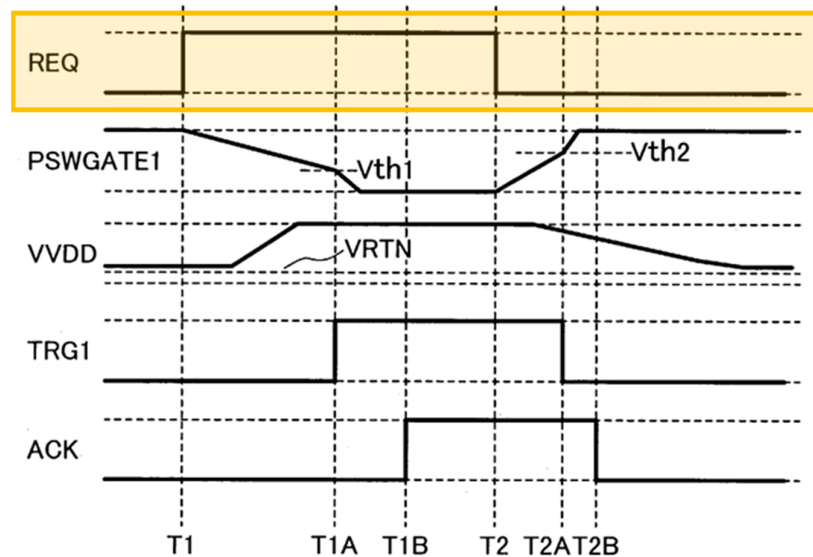
342. Claim 7 recites “[t]he method as claimed in claim 1 wherein the control signal is a digital signal.” In my opinion, Mizuno renders obvious claim 7 of the ’077 Patent.

343. As I explained at element 1[a] above, the signal “REQ” (referred to in the embodiment of Figures 35-40 as “CTL_a, CTL_b”) is a control signal provided to the “power switch controller PSC” that is a power manager. Specifically, Mizuno’s “power controlling circuit PMG” transmits the control signal “REQ” to the “power switch controller PSC” to “control[] the on/off operation of the power switch PSW1 and control[] the state of the circuit block.” MTK-1005, [0093]; *see also id.*, [0121] (“CTL_a, CTL_b are leakage control lines of the leakage reduction circuit of the present invention and equivalent to the request line REQ and response line ACK”).

344. Mizuno discloses that the “REQ” control signal is a digital control signal that takes one of two levels—either high or low. *See* MTK-1015 (defining “digital signal” as “[a]n electrical signal with two states—on or off, high or low, positive or negative—such as could be obtained from a telegraph key or two-position toggle switch”); MTK-1016 (defining “digital signal” as “an electric signal that has only a number of possible states, as opposed to an analog signal

which is continuously variable”). For example, Figure 24 of Mizuno depicts the “REQ” control signal during transitions between active and standby states. *Id.*; *see also id.*, FIGS. 26, 28, 30.

FIG.24



MTK-1005, FIG. 24 (annotated).

345. Specifically, Mizuno explains that setting “REQ” to the “high level turns on the power switch PSW1 and controls the circuit block CKT in the operation state.” *Id.* “Conversely, when the request line REQ is set to low level, the power switch PSW1 turns off and the circuit block is controlled to the standby state.” *Id.*

346. Because the “REQ” signal is a binary signal that takes only one of two levels (high or low), it is my opinion that a POSITA would have understood

that the “REQ” signal is a digital control signal, and otherwise would have found it obvious to use a digital signal for the “REQ” control signal.

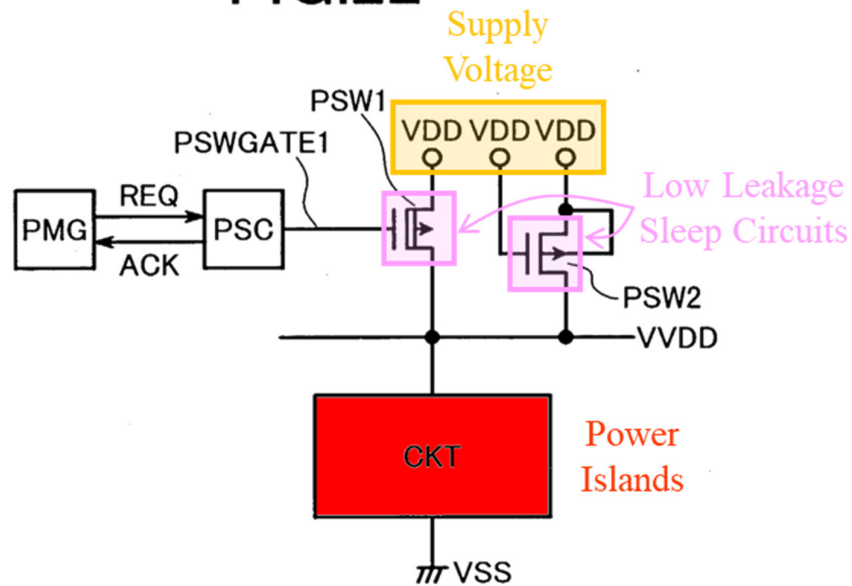
9. Claim 8

347. Claim 8 recites “[t]he method as claimed in claim 1 wherein the at least one of the low leakage sleep circuits is connected in series to a source of a supply voltage and to a logic gate or storage cell of one of the power islands.” In my opinion, Mizuno renders obvious claim 8 of the ’077 Patent.

348. As I explained at element 1[b] above, it is my opinion that Mizuno’s “power switch PSW1” and “current source PSW2” disclose and render obvious the claimed low leakage sleep circuits. It is also my opinion, as explained with respect to element 1[p], that Mizuno’s “circuit block CKT” that includes the “logic circuit LG1” and “memory MEM1” each individually and collectively disclose and render obvious a power island.

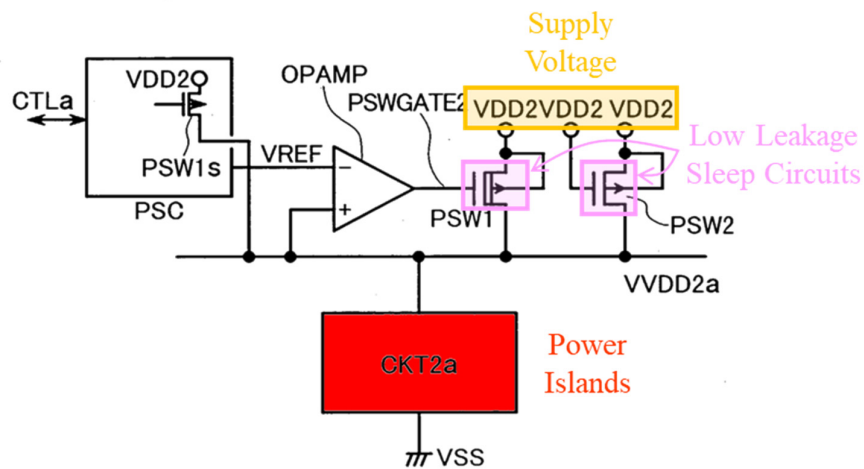
349. As shown below, Mizuno further discloses that the “power switch PSW1” and “current source PSW2” low leakage sleep circuits are connected in series to a source of the “power supply VDD” and the “circuit block CKT”

FIG.22



MTK-1005, FIG. 22 (annotated).

FIG.38

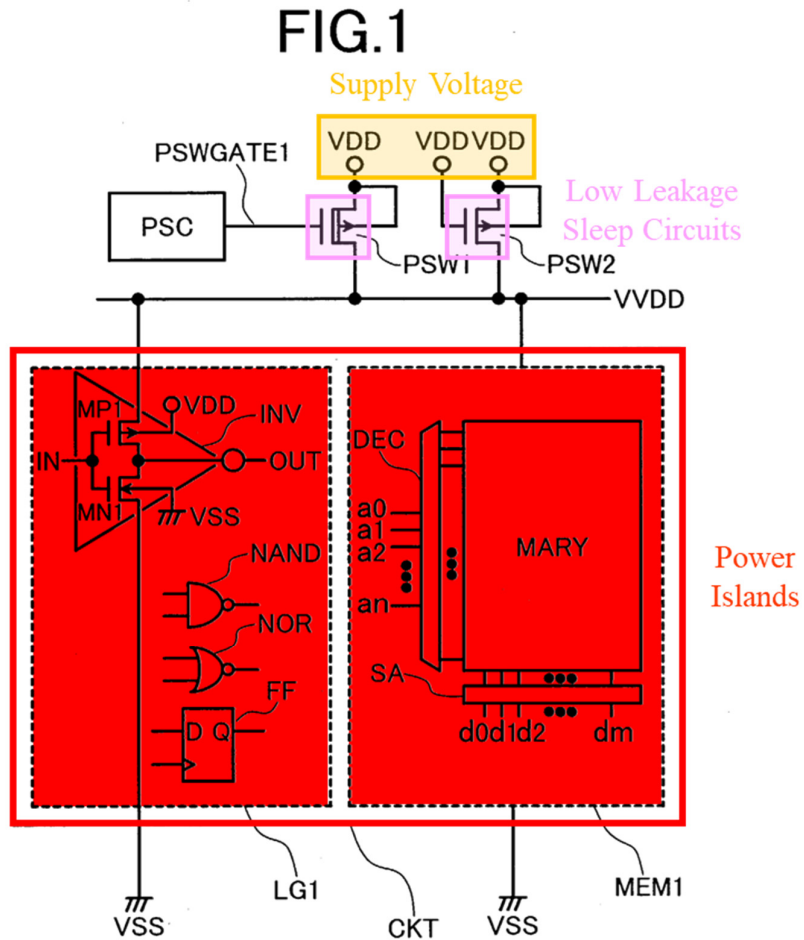


MTK-1005, FIG. 38 (annotated).

350. Regarding the “power supply VDD,” Mizuno discloses that “the voltage of the power supply VDD is the circuit block [CKT] operating voltage

and is supplied from a stable power supply circuit.” MTK-1005, [0054]; *see also id.*, [0093], [0123]. Thus, Mizuno discloses to a POSITA that the “power switch PSW1” and “current source PSW2” are connected in series between a source of a supply voltage (*i.e.*, the “stable power supply circuit” that provides VDD) and the “circuit block CKT.” *Id.*, Abstract (“n a semiconductor integrated circuit device comprising a circuit block having a first MOS transistor, and a leakage current control circuit having a second MOS transistor and a current source, a source and drain circuit of the second MOS transistor is formed between the power supply line of the circuit block and a voltage point where operating voltage is supplied.”), [0003] (“[A] power switch composed of MOS transistors having a threshold voltage with an absolute value sufficiently higher than the absolute values of threshold voltages of MOS transistors comprising the circuit block, is inserted in series with the circuit block power supply between power and ground.”), [0008], [0054] (“The power switch controller PSC controls the on and off operation of the power switch PSW 1 connected between the power supply VDD and the virtual power line VVDD.”).

351. Regarding the “circuit block CKT” that contains “a logic circuit LG1” and a “memory MEM1,” Mizuno discloses that the “logic circuit LG1” has logic gates including “an inverter INV, a NAND circuit NAND, a NOR circuit NOR and a flip-flop circuit FF,” and the “memory MEM1” includes “a memory cell array MARY.” *Id.*, [0053]. Such logic gates and storage cells are shown in Figure 1 of Mizuno, below.



352. Thus, a POSITA would understand that Mizuno’s “power switch PSW1” and “current source PSW2” are connected in series to a source of a supply voltage and to a logic gate or storage cell of one of the power islands. It is therefore my opinion that Mizuno renders obvious claim 8.

10. Claim 9

353. Claim 9 recites “[t]he method as claimed in claim 8 wherein the at least one of the low leakage sleep circuits modifies the supply voltage to the one

of the power islands during a sleep mode.” In my opinion, Mizuno renders obvious claim 9 of the ’077 Patent.

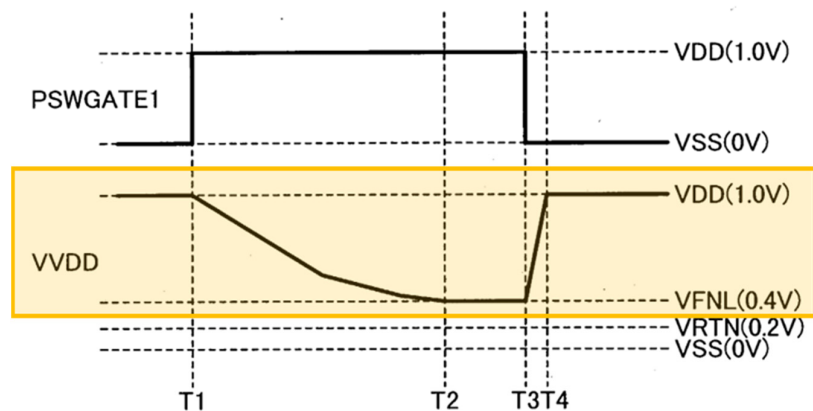
354. As I explained at elements 1[p] and 1[b], it is my opinion that the “power switch PSW1” and “current source PSW2” of Mizuno are low leakage sleep circuits and that the “circuit block CKT” that includes the “logic circuit LG1” and “memory MEM1” are each individually and collectively power islands. Further, as I explained at claim 2, Mizuno’s power islands are put into operational (*i.e.* “out of sleep”) and standby (*i.e.*, “sleep”) states.

355. Mizuno further discloses that during standby the “power switch PSW1” and “current source PSW2” cause the voltage “VVDD” supplied to the “circuit block CKT” to decrease. MTK-1005, [0054]-[0055], [0093]-[0106].⁸ Mizuno explains that the “virtual power line VVDD is equivalent to an actual power line in the circuit block CKT,” *i.e.*, the “virtual power line VVDD” is the supply voltage to the “circuit block CKT.” *Id.*, [0054]. When the “power switch PSW1” is turned on, “the virtual power line VVDD reaches VDD potential and the circuit block CKT is operable (in operating state).” *Id.*, [0055]. On the other

⁸ In the related embodiment of Figures 35-40, the “virtual power line VVDD” is referred to as “VVDD2a” and the “supply voltage VDD” is referred to as “VDD2.” *See* MTK-1005, [0125]-[0128]. The operation of the “power switch PSW1” and “current source PSW2” to control changes to the voltage provided to the “circuit block CKT” (referred to as “circuit block CKT2a” in the embodiment of Figures 35-40) is the same as in the embodiment of Figures 1-30. Thus, my opinion with respect to the embodiment of Figures 1-30 applies equally to the related embodiment of Figures 35-40. *See id.*, [0130] (“Of course the various adaptations and specific examples disclosed for the first embodiment are also applicable to the leakage current reduction circuit of the third embodiment.”).

hand, when the “power switch PSW1 turns off,” the “voltage (or voltage potential) of virtual power line VVDD gradually discharges due to the current leakage from virtual power line VVDD of circuit block CKT to ground VSS” until the “virtual power line VVDD reaches the final converging stable voltage level VFNL.” *Id.* Mizuno depicts one example of the change in the supply voltage provided to the “circuit block CKT” in Figure 2 below.

FIG.2



MTK-1005, FIG. 2 (annotated).

356. It is therefore my opinion that Mizuno’s low leakage sleep circuits, including “power switch PSW1” and “current source PSW2,” modify the supply voltage “VVDD” to the one of the power islands (individually and collectively the “logic circuit LG1” and “memory MEM1” of the “circuit block CKT”) during standby (*i.e.*, “sleep mode”). Thus, it is my opinion that Mizuno renders obvious claim 9.

11. Claim 10

(a) Element 10[p]

357. The preamble of claim 10 recites “[a] method carried out in an integrated circuit that includes an adaptive leakage controller, a power manager, a plurality of power islands and a plurality of low leakage sleep circuits, the method comprising.” Mizuno discloses and renders obvious the preamble of claim 10 of the ’077 Patent for at least the reasons discussed above with respect to element 1[p], the discussion of which I incorporate herein by reference.

(b) Element 10[a]

358. Element 10[a] recites “receiving, at the power manager, a control signal from the adaptive leakage controller.” Mizuno discloses and renders obvious element 10[a] for at least the reasons discussed above with respect to element 1[a], the discussion of which I incorporate herein by reference.

(c) Element 10[b]

359. Element 10[b] recites “employing the power manager to dynamically change power consumptions of the plurality of power islands, the employing the power manager to dynamically change power consumptions including: generating a variable voltage based on the control signal; and providing the variable voltage to the plurality of low leakage sleep circuits.” Mizuno discloses and renders obvious element 10[b] for at least the reasons discussed above with respect to element 1[b], the discussion of which I incorporate herein by reference.

(d) Element 10[c]

360. Element 10[c] recites “wherein each of low leakage sleep circuits is associated with leakage reduction of a respective one of the plurality of power islands.” In my opinion, Mizuno discloses and renders obvious element 10[c].

361. As I explained with respect to element 1[p] above, Mizuno’s “circuit block CKT” that includes “logic circuit LG1” and “memory MEM1” are each individually and collectively a “power island.” Further, as I explained with respect to element 1[b] above, Mizuno’s “power switch PSW1” and “current source PSW2” are each a low leakage sleep circuit. Similarly, in the related embodiment of Figures 35-40, each of the “leakage reduction circuits PSM2a and PSM2b” include a “power switch PSW1” and “current source PSW2” that are each a low leakage sleep circuit.

362. Each of Mizuno’s low leakage sleep circuits, including “power switch PSW1” and “current source PSW2,” is associated with a leakage reduction of a respective one of Mizuno’s power islands. Specifically, when Mizuno transitions to the standby state, the voltage “VVDD” is reduced from VDD to VFNL by the “power switch PSW1” and “current source PSW2.” MTK-1005, [0055]. As a result, the leakage current in the respective power island “I_{off}(CKT) ... also gradually becomes a smaller value.” MTK-1005, [0055].

The operation of FIG. 1 is shown next utilizing the timing chart of FIG. 2. Prior to time T1, the gate signal PSWGATE1 of power switch PSW1 is driven to low level by the power switch controller PSC and the power switch PSW1 turns on. In this state, power is supplied

to the circuit block CKT by way of the power switch PSW1 so that the virtual power line VVDD reaches VDD potential and the circuit block CKT is operable (in operating state). At time T1, the gate signal PSWGATE1 of power switch PSW1 is driven to high level by the power switch controller PSC and the power switch PSW1 turns off. The voltage (or voltage potential) of virtual power line VVDD gradually discharges due to the current leakage from virtual power line VVDD of circuit block CKT to ground VSS by the power switch PSW1 turning off. ***As the voltage of the virtual power line VVDD becomes lower, $I_{off}(CKT)$ (The leakage current flowing to circuit block CKT is listed as $I_{off}(CKT)$ that was initially large (at time T1) also gradually becomes a smaller value (period from time T1 to T2).*** The virtual power line VVDD reaches the final converging stable voltage level VFNL (period from time T2 to T3).

MTK-1005, [0055] (emphasis added).

363. Thus, “power consumption due to leakage current in the circuit block during the standby state can be greatly reduced.” *Id.*, [0087]; *see also id.*, [0059] (“In the present invention, the size of the respective leakage currents such as the gate tunneling current and subthreshold leakage current during standby in the circuit block are determined by the current source PSW2. That value is smaller than the leakage current flowing in the circuit block CKT during operation.”).

364. Similarly, in the related embodiment of Figures 35-40, the multiple “leakage reduction circuits PSM2a and PSM2b” each include low leakage sleep circuits “power switch PSW1” and “current source PSW2” associated with respective power island “[c]ircuit blocks CK2a and CKT2b.” MTK-1005, [0121].

[illegible]

365. Mizuno explains that the “[c]ircuit blocks CKT2a and CKT2b are circuit blocks supplied with power from the power supply VDD by way of the leakage reduction circuits PSM2a and PSM2b.” MTK-1005, [0121]. That is, the voltage provided to the “circuit block CKT2a” is controlled by the “leakage reduction circuit PSM2a” and the voltage provided to the “circuit block CKT2b” is controlled by the “leakage reduction circuit PSM2b.” The “power switch PSW1” and “current source PSW2” in each “leakage reduction circuit” operates the same as the “power switch PSW1” and “current source PSW2” in the related embodiment of Figures 1-30. *Id.*, [0130] (“the various adaptations and specific examples disclosed for the first embodiment are also applicable to the leakage current reduction circuit of the third embodiment”). Thus, each of the low leakage sleep circuits is associated with leakage reduction of a respective one of the “circuit blocks CKT2a, CKT2b” and “the leakage current of the overall chip can be efficiently reduced.” MTK-1005, [0122].

366. Thus, a POSITA would have understood that Mizuno discloses and renders obvious that each of its low leakage sleep circuits (*i.e.*, the “power switch PSW1” and “current source PSW2”) has an associated leakage reduction for a respective power island (“circuit block CKT”).

367. Because Mizuno discloses or renders obvious each element of claim 10 of the '077 Patent, it is my opinion that Mizuno renders obvious claim 10.

12. Claim 11

368. Claim 11 recites “[t]he method as claimed in claim 10 further comprising putting to sleep and taking out of sleep, at different times, at least one of the power islands.” Mizuno renders obvious claim 11 for at least the reasons discussed above with respect to claim 2 and claim 10, the discussion of which is incorporated herein by reference.

13. Claim 12

369. Claim 12 recites “[t]he method as claimed in claim 11 wherein the power manager employs a state machine to control the putting to sleep and the taking out of sleep.” Mizuno renders obvious claim 12 for at least the reasons discussed above with respect to claim 3, claim 10, and claim 11, the discussion of which is incorporated herein by reference.

14. Claim 13

370. Claim 13 recites “[t]he method as claimed in claim 10 wherein the variable voltage is an optimum voltage.” Mizuno renders obvious claim 13 for

at least the reasons discussed above with respect to claim 4 and claim 10, the discussion of which is incorporated herein by reference.

15. Claim 14

371. Claim 14 recites “[t]he method as claimed in claim 13 wherein the optimum voltage is dependent upon both process variation and temperature variation.” Mizuno renders obvious claim 14 for at least the reasons discussed above with respect to claim 5, claim 10, and claim 13, the discussion of which is incorporated herein by reference.

16. Claim 15

372. Claim 15 recites “[t]he method as claimed in claim 13 wherein the optimum voltage is generated by a sleep generator.” Mizuno renders obvious claim 15 for at least the reasons discussed above with respect to claim 6, claim 10, and claim 13, the discussion of which is incorporated herein by reference.

17. Claim 16

373. Claim 16 recites “[t]he method as claimed in claim 10 wherein the control signal is a digital signal.” Mizuno renders obvious claim 16 for at least the reasons discussed above with respect to claim 7 and claim 10, the discussion of which is incorporated herein by reference.

18. Claim 17

374. Claim 17 recites “[t]he method as claimed in claim 10 wherein at least one of the low leakage sleep circuits is connected in series to a source of a supply voltage and to a logic gate or storage cell of an associated one of the power

islands.” Mizuno renders obvious claim 17 for at least the reasons discussed above with respect to claim 8 and claim 10, the discussion of which is incorporated herein by reference.

19. Claim 18

375. Claim 18 recites “[t]he method as claimed in claim 17 wherein the at least one of the low leakage sleep circuits modifies the supply voltage to the associated one of the power islands during a sleep mode.” Mizuno renders obvious claim 18 for at least the reasons discussed above with respect to claim 9, claim 10, and claim 17, the discussion of which is incorporated herein by reference.

E. Analysis of Mizuno in View of Ko with Respect to Claims 3 and 12

376. For the reasons articulated in detail below, and based on my review of the '077 Patent, and the Mizuno and Ko references, it is my opinion that a POSITA would have readily understood that the combination of Mizuno and Ko renders obvious claims 3 and 12 of the '077 Patent.

1. Combination of Mizuno and Ko

377. In my opinion, a POSITA would have been motivated to combine Mizuno with Ko.

378. As an initial matter, a POSITA would have been motivated to combine Mizuno and Ko because both references are directed to solving similar problems. First, both Mizuno and Ko are concerned with reducing power consumption in integrated circuits, including power consumption resulting from

leakage currents during standby states. For example, Mizuno explains that its “invention is ... capable of reducing the different types of leakage current ... while the circuit block is in standby state” and “also allows high speed circuit block operation while the circuit block is in the operation state.” MTK-1005, [0009]; *see also id.*, [0087]-[0088], [0093], [0130]. Similarly, Ko discloses that its “invention relates generally to digital integrated circuits and, more particularly, to reducing leakage current in power-saving standby modes of digital integrated circuit operation.” MTK-1006, 1:14-17; *see also id.*, 3:7-34, 7:20-50, 9:2-4, 9:42-50.

379. Second, both Mizuno and Ko describe solutions for retaining data in integrated circuits during reduced-power standby states.

Noticing the fact that the information in the information retention circuit can still be retained even if the supply voltage when the power supply switch was off is made lower than absolute value of the MOS transistor threshold voltage, the inventors developed a structure capable of retaining information in the information retention circuit and reducing electrical power loss due to leakage (current).

MTK-1005, [0007]. *See also id.*, [0009], [0053], [0065]-[0066], [0087]-[0088] (“The present invention is characterized in that power consumption due to leakage current in the circuit block during the standby state can be greatly reduced while still maintaining (keeping) the information within the information retention circuits within the circuit block.”), [0099].

FIG. 2 diagrammatically illustrates exemplary embodiments of a flip-flop with state retention

capability for use in a state retention register according to the invention. The flip-flop of FIG. 2 is a multi-threshold CMOS (MTCMOS) flip-flop. This MTCMOS flip-flop includes normal core transistors which are used throughout the logic module and have a first gate oxide thickness, and also includes additional transistors having a thicker gate oxide (and correspondingly less leakage) than the normal core transistors. These thick gate oxide transistors are used to implement the state retention functionality of the flip-flop. The inverters connected back-to-back between the nodes N10 and N11 form a shadow latch for retaining data while power is removed from the normal functional (in this example, DQ) flip-flop circuitry. These inverters are formed with thick oxide (low leakage) transistors and are powered by a separate power supply VRETAIN, which is produced from the permanent power supply VCC (see also FIG. 1).

MTK-1006, 3:7-24; *see also id.*, Title, Abstract (“[s]tate retention registers for use in low-power standby modes of digital IC operation are provided”), 4:8-13 (describing Ko’s invention “to reduce the leakage current while the shadow latch is retaining data with the normal functional flip-flop circuitry powered-down”).

380. Notably, the ’077 Patent is directed to addressing these same problems. For example, the ’077 Patent is titled “Low Leakage and Data Retention Circuitry,” and in its “Summary of the Invention” describes “a data retention circuit” that includes a “leakage optimization circuit ... configured to simultaneously decrease leakage power in conjunction with the state retention,” as well as a “circuit ...configured to process ... input signals and retain data in a sleep state having low leakage.” MTK-1001, Title, 2:24-50; *see also id.*, Abstract, 1:20-39, 3:49-55.

381. A POSITA also would have been motivated to combine Mizuno and Ko because they address the same known problems in similar ways. As I have explained, Mizuno and Ko both reduce overall power consumption in integrated circuits by placing portions of an integrated circuit into low-power standby states when they are inactive, so that only the active portions of the integrated circuit are receiving full power. *See* MTK-1005, [0054]-[0055], [0093], [0121]-[0122]; MTK-1006, 1:20-56, 2:63-3:6, 7:20-50.

382. To place portions of the integrated circuit into operational or standby states, Mizuno and Ko both utilize MOS transistors. Mizuno refers to these transistors as, for example, “power switch PSW1,” while Mizuno refers to them as “header switches.” *Id.*

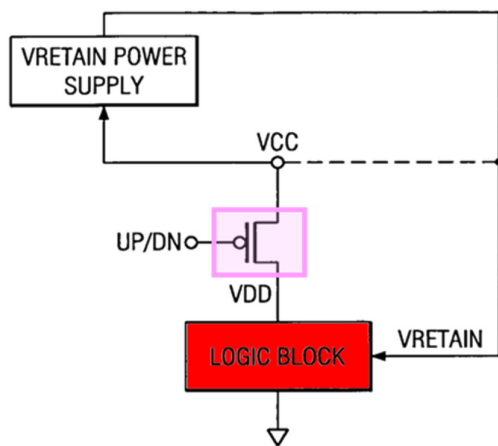


FIG. 1

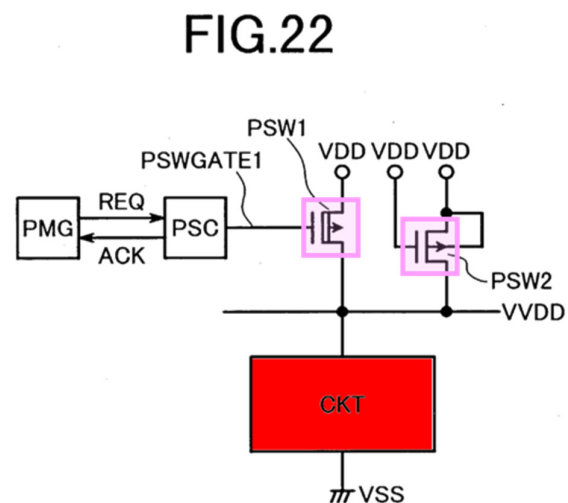


FIG. 22

MTK-1006, FIG. 1 (annotated) (left); MTK-1005, FIG. 22 (annotated) (right).

383. In both references, the transistors are used to connect or disconnect the portions of the integrated circuit from their operational voltage supply, thereby placing the circuit blocks into operational or standby states, respectively.

Id. That is, Mizuno and Ko both teach modifying the voltages applied to the switching circuits to turn them on or off, thereby changing the voltage provided to the portions of the integrated circuit depending on whether they are in operational or standby states. *Id.* Changing the voltages to the portions of the integrated circuit (*i.e.*, specific circuit blocks) during operational and standby states reduces overall power consumption in the system, including that due to leakage currents. *Id.*

384. Mizuno and Ko also propose similar methods of achieving data retention during low-power standby states. Specifically, Mizuno and Ko both do so by optimizing the voltage applied to the portions of the integrated circuit that are in standby so as to reduce power consumption while still maintaining the data stored in the retention circuitry. MTK-1005, [0003], [0065], [0087], [0099]; MTK-1006, Abstract, 3:21-24. Mizuno explains that during standby, “[a]s shown in FIG. 2 in the present invention, in order to retain information stored within the information holding circuit within the circuit block CKT, the voltage value VFNL of the virtual power line VVDD can be a voltage higher than voltage VRTN which is the minimum voltage capable of retaining information stored within the information holding circuit.” MTK-1005, [0065]. Similarly, Ko’s integrated circuit includes a “separate power supply VRETAIN” set to a level capable of powering data retention “shadow latches” during a “low-power standby mode.” MTK-1006, Abstract, 3:21-24.

385. Based on their similarities, it is my opinion that a POSITA developing Mizuno's system would have been motivated to look to Ko, and would have been capable of integrating the teachings of each with a reasonable expectation of success.

386. Specifically, the similarities between Mizuno and Ko would have led a POSITA to employ Ko's implementation of a state machine with Mizuno's "power switch controller PSC." Mizuno puts a "circuit block CKT" into standby or operational mode using its "power switch PSW1" that controls whether the "circuit block CKT" receives an operating voltage VDD. MTK-1005, [0055], [0093]-[0107]. The "power switch PSW1" is controlled by a "power switch controller PSC" that generates a variable voltage "PSWGATE1" that controls the on or off status of the "power switch PSW1." *Id.* Mizuno explains that the "power switch controller PSC" employs specific combinations of elements as shown in Figures 23-30. Two such examples, from Figures 23 and 29, are shown below.

FIG.23

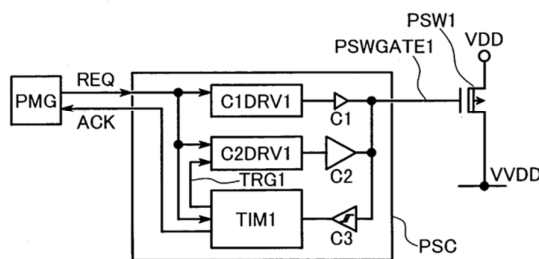
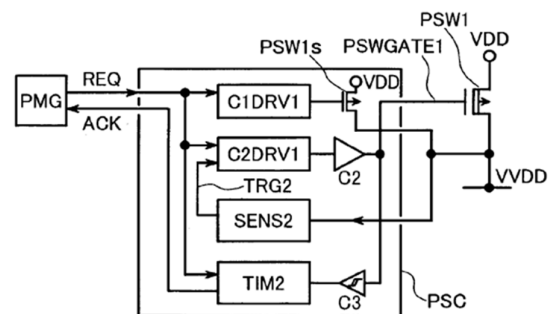


FIG.29



MTK-1005, FIGS. 23, 29.

387. As shown, Mizuno’s “power switch controller includes control circuits (e.g., “C1DRV,” “C2DRV”), drive circuits (e.g., “C1,” “C2”), a timer (e.g., “TM1”), voltage potential detectors (e.g., “C3,” “SENS1,” “SENS2”), and/or a power switch (e.g., “PSW1s”). MTK-1005, [0093]-[0107], FIGS. 22-30. Mizuno explains that these configurations are used to ensure that data is retained during the transitions between standby and operational states.

The present invention is characterized in that information is retained (held) within the information retention circuits. Of course this information must be retained when changing from the standby state to the operation state and also when changing from the operation state to the standby state. Information within the information retention circuits might be destroyed due to coupling noise from the virtual power line VVDD during the change from the standby state to the operation state. To eliminate this problem, the structure in FIG. 23 utilizes a driving circuit with high impedance C1 and a driving circuit with low impedance C2 to drive the gate signal PSWGATE1 so the slew rate is reduced. The coupling noise from the virtual power line VVDD is reduced and the information within the information retention circuits can be prevented from being destroyed.

MTK-1005, [0099]; *see also id.*, [0100].

388. While Mizuno discloses one approach to controlling the transition between standby and operational states, a POSITA would have understood that Mizuno’s solution is merely a design choice selected from among a finite number of known solutions.

389. A POSITA would have understood that Ko discloses another possible solution for putting portions of an integrated circuit into standby or

operational states. MTK-1006, 7:20-50. Specifically, Ko discloses a “power state controller 45 which, in some embodiments, utilizes state machines to provide appropriate control signals to the header switches and logic modules” to put the “logic modules” in the integrated circuit into standby or operational states. *Id.* For example, Figures 5 and 13 of Ko are timing diagrams illustrating “the timing relationships of the control signals produced by the power state controller 45” to ensure that data is not lost when putting a logic module into the “low-power standby (state retention) mode of operation” and to restore data when entering an operational mode form the standby mode. MTK-1006, 7:51-55, 11:9-29.

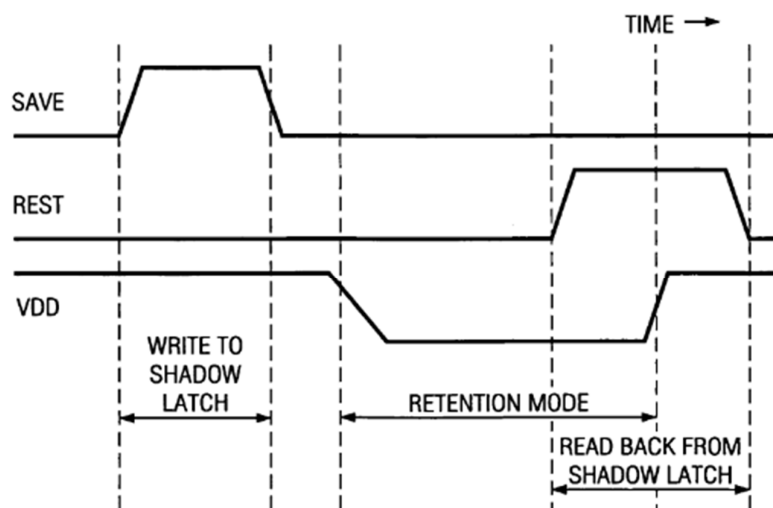
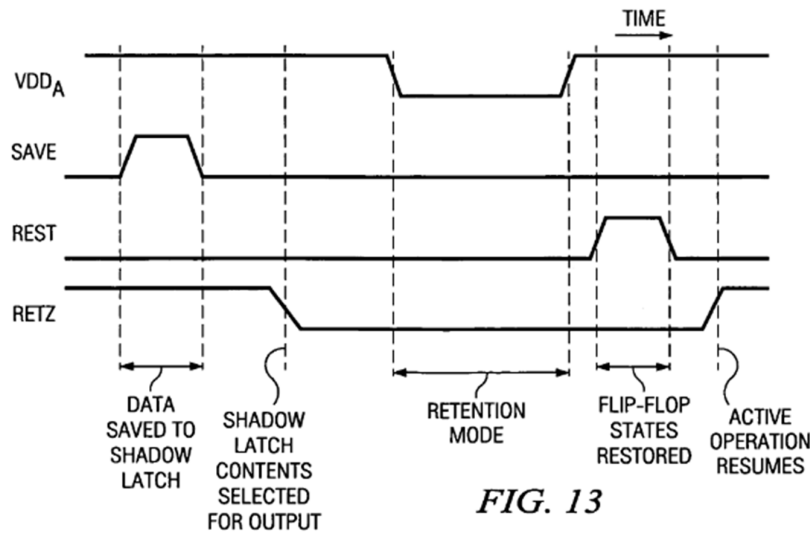


FIG. 5

MTK-1006, FIG. 5.



MTK-1006, FIG. 13.

390. Because Mizuno and Ko provide a similar solution to a similar problem within the same field of endeavor, it is my opinion that a POSITA would have naturally looked at, and been motivated to combine, Mizuno and Ko when selecting a method implementing transitions between standby and operational states. Specifically, a POSITA would have understood that Mizuno’s “power switch controller PSC” could employ Ko’s “state machines” to control the “gate signal PSWGATE1 so the slew rate is reduced” when transitioning the “circuit block CKT” between standby and operational states. In my opinion, such a substitution of one known solution for another would have been a mere design choice that was both obvious to try and would have yielded predictable results.⁹

⁹ As I explained above, it is my opinion that Mizuno alone discloses and renders obvious employing a state machine to put its power islands to sleep and take them out of sleep (*i.e.*, to transition them between standby and operating states). However, as I explain here, to the extent that Mizuno alone does not render obvious this feature, it is my opinion that Mizuno in combination with Ko renders

Moreover, doing so would have required merely routine electrical or computer programming knowledge and was a task well within the skill of a POSITA. A POSITA would have understood how to modify Mizuno's "power switch controller PSC" to use Ko's state machine, and Mizuno's integrated circuit would not be negatively impacted by that modification.

391. In my opinion, a POSITA also would have been motivated to make this substitution. First, a POSITA would have understood that a state machine requires less circuit area to implement than a circuit like that disclosed by Mizuno for its "power switch controller PSC." Indeed, Mizuno acknowledges that "surface area overhead" was a design concern. MTK-1005, [0089]. Thus, a POSITA would have been motivated to use Ko's state machine to reduce the "surface area" of the "power switch controller PSC" without losing the ability to retain data during transitions to and from the standby state. For example, in the embodiment of Figures 35-40, the separate "power switch controller[s] PSC" in the "leakage reduction circuits PSM2a and PSM2b" would be replaced by a single state machine capable, as taught by Ko, of controlling the transitions between operational or standby status of multiple power islands (*e.g.*, "circuit blocks CKT2a and CKT2b"). *See, e.g.*, MTK-1005, [0121]; MTK-1006, 7:38-42.

392. Second, a POSITA would have understood that Mizuno's analog solution to controlling the transitions between operating and standby states,

obvious employing a state machine to control such transitions as recited by claim 3.

including the change of variable voltage PSWGATE1, is susceptible to process and temperature variations. Therefore, a POSITA would have been motivated to replace Mizuno's "power switch controller PSC" design with Ko's "state machine" because a POSITA would have understood that Ko's "state machine" is a digital circuit that is less susceptible to environmental and process variations. Thus, a POSITA would have been motivated to implement Ko's "state machine" in Mizuno's integrated circuits to obtain these benefits over the circuitry employed by Mizuno's "power switch controller PSC."

393. Therefore, it is my opinion that a POSITA would have been motivated to combine Mizuno with Ko and would have been capable of doing so with a reasonable expectation of success.

2. Claim 3

394. Claim 3 recites "[t]he method as claimed in claim 2 wherein the power manager employs a state machine to control the putting to sleep and the taking out of sleep." In my opinion, to the extent that Mizuno alone does not render obvious claim 3, the combination of Mizuno and Ko renders obvious claim 3.

395. As I explained with respect to claim 3 when discussing the combination of Takahashi and Ko, Ko employs "state machines to provide appropriate control signals to the header switches and logic modules" to transition the "logic modules" between active and standby states. *See* MTK-1006, 7:20-50, 9:42-50; Section VIII.B.3.

396. In my opinion, a POSITA would have found it obvious for Mizuno's "power switch controller PSC" to employ a state machine as taught by Ko to control the putting to sleep and taking out of sleep of power islands (*e.g.*, the "circuit block CKT") in Mizuno's integrated circuit. As discussed above, a POSITA would have understood that Ko's state machine would consume less surface area than Mizuno's implementation and would be less susceptible to environmental and process variations. Thus, a POSITA would have been motivated to use Ko's state machine in lieu of Mizuno's "power switch controller PSC" circuitry (*e.g.*, as shown in Figure 23) to improve the "power switch controller PSC's" ability to place the "circuit block CKT" into an operational or standby mode without losing data. MTK-1005, [0093]-[0107].

397. A POSITA would have had a reasonable expectation of success in combining Ko with Mizuno in this way. Because the combination utilizes known methods and is well within the skill of a POSITA, replacing Mizuno's "power switch controller PSC" with Ko's "state machine" represents a simple substitution of one known element for another. Further, incorporating Ko's "state machine" would result in reduced surface area for the low leakage mechanism in Mizuno's and would reduce the temperature and process dependence in the timing of the signal PSWGATE1 used to transition Mizuno's power islands between active and standby states. *Id.* Thus, it is my opinion that a POSITA would have been motivated to modify Mizuno's power manager (*i.e.*, "power switch controller PSC") to use Ko's "state machine" to improve its ability to

transition the “circuit block CKT” power island between standby and operational states without risk of data loss. MTK-1005, [0099]-[0101].

398. It is therefore my opinion that the combination of Mizuno and Ko renders obvious claim 3.

3. Claim 12

399. Claim 12 recites “The method as claimed in claim 11 wherein the power manager employs a state machine to control the putting to sleep and the taking out of sleep.” To the extent that Mizuno alone does not render obvious claim 12, the combination of Mizuno and Ko renders obvious claim 12 for at least the reasons discussed above with respect to claim 3, the discussion of which is incorporated herein by reference.

IX. ADDITIONAL REMARKS

400. I currently hold the opinions set expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

401. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code.

Dated: March 6, 2024

By: 
Paul Min, Ph.D.
St. Louis, Missouri

APPENDIX A

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St. Louis, MO 63130

Education

<u>Year</u>	<u>College or University</u>	<u>Degree</u>
1987	The University of Michigan	Ph.D. in Electrical Engineering
1984	The University of Michigan	M.S. in Electrical Engineering
1982	The University of Michigan	B.S. in Electrical Engineering

Professional Experience

From: 1990
To: Present
Organization: Washington University, St. Louis

Summary:

2015 - Senior Professor - Department of Electrical Systems Engineering

2011 – 2014 Chair – Undergraduate Curriculum, Department of Electrical and Systems Engineering

2000 – 2002 Chair – Graduate Curriculum, Department of Electrical and Systems Engineering

2002 - 2014 Associate Professor - Department of Electrical and Systems Engineering

1997 - 2008 On leave from full-time duty at Washington University – as Presidents of MinMax Technologies and Erlang Technology.)

1996 - 2002 Associate Professor - Department of Electrical Engineering

1996 Promoted with Tenure

1990 - 1996 Assistant Professor - Department of Electrical Engineering

- Teaching Experience
- “Transmission System and Multiplexing,” Washington University, ESE 571
 - “Electrical Laboratory I,” Washington University, EE 250.
 - “Communication Theory,” Washington University, ESE 471.
 - “Reliability and Quality Control,” Washington University, ESE 405/505
 - “Signaling and Control of Communications Networks,” Washington University, ESE 572.
 - “Introduction to Electronic Circuits,” Washington University, ESE232
 - “Queueing Systems and Discrete Stochastic Processes,” Washington University, EE 536 / CS 567.
 - “Digital Computer,” Washington University, EE 260M / CS 260.
 - “Data Networks,” Washington University, EE 530.
 - “Electrical Circuit Analysis,” Washington University, ESE 230.
 - “Computer/Communications System Analysis I,” Washington University, EE 557/ CS 557.
 - “Computer/Communications System Analysis II,” Washington University, EE558 / CS 558.
 - “Digital Systems Laboratory,” Washington University, EE 455 / CS 455.

From: 1999
To: 2008
Organization: Erlang Technology, Inc., St. Louis, Missouri
Title: Founder and President
Summary: Up to 70 employees, \$40M in total capital raised from 5 VCs and 3 Corporations
Received “Product of Year” Award from Analog Zone Magazine in 2004

From: 1997
To: 1999
Organization: MinMax Technologies, Inc., St. Louis, Missouri
Title: Founder and President
Summary: Fabless semiconductor company, designing high performance switching ASICs

From: September 1987
To: August 1990
Organization: Bellcore, New Jersey
Title: Member of Technical Staff
Summary: Member of New Network Architecture Development Group

From: 1983
To: 1987

Organization: Department of Electrical Engineering, The University of Michigan
Title: Graduate Instructor
Summary: Instructor for senior level Electrical Engineering Laboratory Class. Received a Best “Best Graduate Instructor Award” from the Department of Electrical Engineering

Professional Affiliations, Achievements & Awards

- Technical Program Committee, COMCAS 2021, Tel Aviv, November 2021.
- Technical Program Committee, COMCAS 2019, Tel Aviv, November 2019.
- Technical Program Committee, COMCAS 2017, Tel Aviv, November 2017.
- Technical Program Committee, COMCAS 2015, Tel Aviv, October 2015.
- Past-Chair, Saint Louis Section of the Institute of Electrical and Electronics Engineers (IEEE), 2015.
- Member of Executive Committee, Saint Louis Section of the IEEE, 2010-2015.
- Chair, Saint Louis Section of the IEEE, 2014.
- Technical Program Committee, COMCAS 2013, Tel Aviv, October 2013.
- Vice Chair, Saint Louis Section of the IEEE, 2013
- Treasurer, Saint Louis Section of the IEEE, 2012.
- The Best Paper Award at MOBILITY 2011, October 2011, Barcelona, Spain.
- Counselor, Student Chapter of the Year, the Institute of Electrical and Electronics Engineers, 2011.
- Award of Appreciation, Saint Louis Section of the Institute of Electrical and Electronics Engineers, 2011, for contribution to various activities of the Saint Louis Section the Institute of Electrical and Electronics Engineers.
- Secretary, Saint Louis Section of the IEEE, 2010.
- Counselor, Student Chapter of the Year, the Institute of Electrical and Electronics Engineers, 2010.
- Wall Street Journal Businessmen of Year, 2003.
- American Men and Women of Science, listed in 1997.
- Member, Eta Kappa Nu (Honor Society for Electrical Engineers), inducted in 1992
- Outstanding Achievement Award, Bellcore, 1990.
- 18th ISATA Award of Technical Excellence, the best paper award at ISATA 1988.
- Rockwell Fellow, Rockwell International, 1985, 1986.
- Outstanding Graduate Student Award, the University of Michigan, 1985.
- Outstanding Teaching Award, the University of Michigan, 1984, 1986.
- Member of Honor's College, the University of Michigan, 1979, 1980.

- Honor's Convocation, the University of Michigan, 1979.
- Outstanding Freshman Award, the University of Michigan, 1979.
- Woodhaven Rotary Club Scholarship, Woodhaven Rotary Club, 1978.
- Second Place Winner, the State of Michigan Mathematics Prize Competition, 1977.
- International Program Committee, *IASTED International Conference on Communications, Internet and Information Technology (CIIT 2005)*, Cambridge, Massachusetts from October 31-November 2, 2005.
- International Program Committee, *IASTED International Conference on Communications 2003*, Scottsdale, Arizona, 2003.
- International Program Committee, *Wireless and Optical Communications 2003*, Banff, Canada, 2003.
- International Program Committee, Session Chair, *Wireless and Optical Communications 2002*, Banff, Canada, 2002.
- Invited participant, *NSF Workshop on Enhancing International Cooperation in CS/CE Research and Education*, Portland, 1997.
- Session Chair, *the 1993 Conference on Information Sciences and Systems*, Baltimore, March 1997.
- Member, Board of Editors, *Journal of Network and Systems Management*, 1996-1998.
- Program Committee, *International Symposium on Integrated Network Management*, San Diego, 1997.
- Guest Editor, *Journal of Network and Systems Management, Special Issue on Routing in Broadband Networks*, December 1995 and June 1996.
- Invited participant, *ARPA Workshop on Survivability of Large Scale Systems*, Washington D.C., 1996.
- Special Event Organizer, *International Symposium on Integrated Network Management*, Santa Barbara, 1995.
- Organizing Committee, *International Symposium on Integrated Network Management*, Santa Barbara, 1995.
- Local Arrangements Chair, *IEEE Information Theory Workshop on Information Theory Multiple Access and Queueing*, St. Louis, 1995.
- Chair, *Communications Chapter, St. Louis Section of the IEEE*, 1995.
- Participant, *IEEE Information Theory Workshop on Information Theory, Multiple Access and Queueing*, St. Louis, 1995.
- Participant, *ARPA/AFOSR Non-Linear Optics and Communication Workshop*, Denver, 1994.
- Participant, *CNRI Giga Bit Network Workshop*, Washington D.C., 1993.
- Participant, *IFIP/IEEE International Workshop on Distributed Systems*, New Jersey, 1993.
- Program Committee, *International Conference on Computer Communications and Networks*, San Diego, 1992.
- Session Chair, *ISMM International Conference*, New Orleans, 1990.
- Senior Member, *IEEE*.

- Member, *IEEE Committee on Network Operations and Management*.
- Member, *IEEE Committee on Computer Communications*.
- Registered Specialist, *Hong Kong Research Grant Council*.
- Reviewer, *IEEE Transactions on Communications*.
- Reviewer, *IEEE Transactions on Networking*.
- Reviewer, *IEEE Journal on Selected Areas in Communications*.
- Reviewer, *Journal of Network and Systems Management*.
- Reviewer, *Telecommunication Systems*.
- Reviewer, *Computers and Electrical Engineering*.
- Reviewer, *ETRI Journal*.
- Reviewer, *IEEE Transactions on Automatic Control*.
- Reviewer, *IEEE Communications*.
- Book Reviewer, *Prentice Hall*.
- Book Reviewer, *Morgan Kaufmann Publishers, Inc.*
- Book Reviewer, *Irwin Publishing Co.*

University Activities:

- Undergraduate Studies Committee, School of Engineering and Applied Science (2012 – Present)
- Faculty Advisor for IEEE Student Chapter (2009 – Present)
- Ambassador for McDonnell International Scholar Academy (2007 – 2013)
- Web Development Committee (2006 – 2008)
- University Judicial Board (1998 - 2000)
- Resource Generation Committee (1994 - 1995)
- Top 20 Committee (1992 - 1995)
- Telecommunications Committee, Chair (1991 - 1997)
- Library Planning Committee (1991 - 1992)
- Computer Engineering Committee (1990 - 1996)
- Communications Curriculum Committee (1990 - 1992)
- Resources Committee (1990 - 1992)

Patents

<u>Patent No.</u>	<u>Date</u>	<u>Title</u>
10,623,323	04/14/20	Network Devices and a Method for Signature Pattern Detection
10,284,476	05/07/19	Hierarchical Pattern Matching Devices and Methods

7,110,411	09/19/06	Method of and Apparatus for WFQ Scheduling Using a Plurality of Scheduling Queues to Provide Fairness, High Scalability, and Low Computational Complexity
7,106,738	09/12/06	Method of and Apparatus for High Speed Packet Switching Using Train Packet Queuing and Providing High Scalability
6,859,455	02/22/05	Method of and Apparatus for Building and Using Multi-Dimensional Index Trees for Multi-Dimensional Data Objects
6,614,789	09/02/03	Method of and Apparatus for Matching Strings of Different Lengths
6,359,885	3/19/02	Multi-Channel Packet Switching Apparatus Having Traffic Flow Controlling and Checking Functions
6,128,292	10/03/00	Packet Switching Apparatus with Multi-Channel and Multi-Cast Switching Functions and Packet Switching System Using the Same
5,788,161	12/13/98	Network Designer for Communication Networks
5,526,352	06/11/95	Integrable Low Complexity Multi-Channel Switch
5,440,549	08/08/95	Nonblocking Multi-Channel Switching with Multicasting Capability

Publications

- Yu, Qixiang, Luo, Z., and Min, P.S., “Intrusion Detection in Wireless Sensor Networks for Destructive Intruders.” Proceedings of the APSIPA 2015 conference. December 16-19, 2015.
- Hung, C.P., and Min, P.S., “Simple Web Application Framework.” Submitted for publication in the IEEE Transactions on Cloud Computing.
- Luo, Z., and Min, P.S., “Parallel Implementation of Energy-Based Target Localization Methods in Wireless Sensor Networks.” Proceeding of the 2014 IEEE SOUTHEASTCON.
- Yu, Q., Luo, Z., and Min, P.S., “Intrusion Detection in Wireless Sensor Networks for Destructive Intruder.” Proceeding of 2014 International Conference on Smart Computing (SMARTCOMP 2014).
- Luo, Z., and Min, P.S., “Survey of Target Localization Methods in Wireless Sensor Networks,” 19th IEEE International Conference on Networks (ICON 2013), Singapore, December 11-13, 2013.
- Hung, C.P., and Min, P.S., “Deriving and Visualizing the Lower Bounds of Information Gain for Prefetch Systems,” 19th IEEE International Conference On Networks (ICON 2013), Singapore, December 11-13, 2013.
- Hung, C.P., and Min, P.S., “Access LUT without CAM - Improved Pearson Hashing for Collision Reduction,” 19th IEEE International Conference On Networks (ICON 2013), Singapore, December 11-13, 2013.
- Luo, Z and Min, P.S., “Target Localization in Wireless Sensor Networks for Industrial Control with Selected Sensors.” International Journal of Distributed Sensor Networks, Volume 2013 (2013), Article ID 304631.
- Hung, C.P., and Min, P.S. “Performance Evaluation of Distributed Mobile Application Virtualization Services,” International Journal on Advances in Internet Technology, Vol. 5, no. 3&4, 2012, pp. 65-83.

- Hung, C.P. and Min, P.S., “Performance evaluation of distributed application virtualization services using the UMTS mobility model,” *MOBILITY 2011 The First International Conference on Mobile Services, Resources, and Users*, 23-29 Oct. 2011.
- Hung, C.P. and Min, P.S., “Service Area Optimization For Application Virtualization Using UMTS Mobility Model,” *International Conference on Internet Computing*, pp. 128-134, Las Vegas, July 18-21, 2011.
- Hung, C.P. and Min, P.S., “Application Virtualization Using UMTS Mobility Model,” *ICOMP'11*, September, 2011.
- Hung, C.P. and Min, P.S., “Infrastructure Arrangement for Application Virtualization Service,” the 9th International Information and Telecommunication Technologies Symposium, Vol.1, pp. 78-85, Rio de Janeiro, December 2010.
- Hung, C.P. and Min, P.S., “Probabilistic Approach to Network-Based Virtual Computing,” the 9th International Information and Telecommunication Technologies Symposium, Vol.1, pp. 117-124, Rio de Janeiro, December 2010.
- Shiravi, A. and Min, P. S., “On the Latency Bound of Proportional Nested-DRR with Credit Adjusting,” *2007 Workshop on High Performance Switching and Routing HPSR 2007*, July 2007.
- Shiravi, A. and Min, P. S., “LOOFA-PB: A Modified LOOFA Scheduler for Variable-Length Packet Switching,” *2007 IEEE International Conference on Communications (ICC 2007)*, Glasgow, June 2007.
- Shiravi, A., Kim, Y. G., and Min, P. S., “Congestion Prediction of Self-Similar Network through Parameter Estimation,” *Proceedings of 2006 IEEE/IFIP Network Operations & Management Symposium*, April 2006, Vancouver.
- Shiravi, A., Kim, Y. G., and Min, P. S., “Traffic Dispatching Algorithm in Three-Stage Switch,” *Proceedings of 5th International Conference on Networking*, April 2006, Mauritius.
- Shiravi, A., Kim, Y. G., and Min, P. S., “Proportional Nested Deficit Round Robin with Credit Adjusting,” *Proceedings of 2nd Int'l Conf. on Quality of Service in Heterogeneous Wired/Wireless Networks (QShine 2005)*, Orlando, August 2005.
- Shiravi, A., Kim, Y. G., and Min, P. S., “Proportional Nested Deficit Round Robin: Improving the Latency of Packet Scheduler with an $O(1)$ Complexity,” *Proceedings of International Workshop on Advanced Architectures and Algorithms for Internet Delivery and Applications (AAA-IDEA 2005)*, Orlando, June 2005
- Kim, Y. G., Shiravi, A., and Min, P. S., “Prediction-Based Routing through Least Cost Delay Constraint,” *Proceedings of IEEE IPDPS 2004*, Santa Fe, April 2004.
- Kim, Y. G. and Min, P. S., “On the Prediction of Average Queuing Delay with Self-Similar Traffic,” *Proceedings of IEEE GLOBECOM 2003*, San Francisco, December 2003.
- Hu, C., Saidi, H., Yan, P. Y., and Min, P.S., “A Protocol Independent Policier And Shaper Using Virtual Scheduling Algorithm,” *Proceedings of ICCAS 2002*.

- Hu, C., Saidi, H., and Min, P.S., “DB_WFQ: An Efficient Fair Queueing Using Binary Counter,” *Proceeding of Coins 2002*.
- Yoon, U. and Min, P.S., “Performance Analysis of Radio Link Control Mechanism in W-CDMA System”, IEEE VTC’01 Fall, October 2001, New Jersey
- Akl, B., Hegde, M.V., Naraghi-Pour, M., and Min, P.S., “Multi-Cell CDMA Network Design,” *IEEE Transaction on Vehicular Technology*, Volume 50, No. 3, pp. 711-722, May 2001.
- Yoon, U., Park, S., Min, P.S., “Performance Analysis of Multiple Rejects ARQ at RLC (Radio Link Control) for Packet Data Service in W-CDMA System,” *IEEE Globecom*, November 2000, San Francisco.
- Yoon, U., Park, S., Min, P.S., “Performance Analysis of Multiple Rejects ARQ for RLC (Radio Link Control) in the Third Generation Wireless Communication,” *WCNC*, September 2000, Chicago.
- Yoon, U., Park, S., Min, P.S., “Network Architecture and Wireless Data Service Protocol based on Mobile IP toward the Third Generation Wireless Communication,” *3G Wireless*, June 2000, San Francisco, pp. 211-215
- R.G. Akl, M.V. Hegde, M. Naraghi-Pour, P.S. Min, “Multi-Cell CDMA Network Design,” *IEEE International Conference on Communications*, June 2000.
- R.G. Akl, M.V. Hegde, M. Naraghi-Pour, P.S. Min, “CDMA Network Design to Meet Non-uniform User Demand,” *International Teletraffic Congress*, March 2000.
- R.G. Akl, M.V. Hegde, M. Naraghi-Pour, P.S. Min, “CDMA Network Design,” *IEEE Transactions on Vehicular Technology*.
- R.G. Akl, M.V. Hegde, M. Naraghi-Pour, P.S. Min, “Cell Placement in a CDMA Network,” *IEEE Wireless Communications and Networking Conference*, September 1999, Volume 2, pp. 903-907.
- R.G. Akl, M.V. Hegde, P.S. Min, “Effects of Call Arrival Rate and Mobility on Network Throughput in Multi-Cell CDMA,” *IEEE International Conference on Communications*, June 1999, Volume 3, pp. 1763-1767.
- Hegde, M.V., Schmid, O.A., Saidi, H., and Min, P.S., “Real-Time Adaptive Bandwidth Allocation for High-Speed ATM Switches,” accepted, *International Conference on Communications*, June 1999.
- Akl, B.G., Hegde, M.V., and Min, P.S., “Effects of Mobility on Network Throughput in Multicell CDMA Networks,” accepted, *International Conference on Communications*, June 1999.
- Akl, B.G., Hegde, M.V., Min, P.S., and Naraghi-Pour, M., “Flexible Allocation of Capacity in Multi-Cell CDMA Networks,” accepted, *Vehicular Technology Conference*, June 1999.
- R.G. Akl, M.V. Hegde, M. Naraghi-Pour, P.S. Min, “Flexible Allocation of Capacity in Multi-Cell CDMA Networks,” *IEEE Vehicular Technology Conference*, May 1999, Volume 2, pp. 1643-1647.

- Oh, M.S., and Min, P.S., "Reliability Analysis for One-Turn and Deflection Crossbar Architectures and Distributed Fault Recovery Scheme," *Proceedings of GLOBECOM 97*, Phoenix, November 1997.
- Kim, K.B., Yan, P.Y., Kim, K.S., Schmid, O., and Min, P.S., "A Growable ATM Switch with Embedded Multi-Channel Multicasting Property," *Proceedings of GLOBECOM 97*, pp. 222-226, Phoenix, November 1997.
- Kim, K.B., Yan, P.Y., Kim, K.S., Schmid, O., and Min, P.S., "MASCON: A Single IC Solution to ATM Multi-Channel Switching with Embedded Multicasting," *Proceedings of ISS 97*, pp. 451-458, Toronto, September 1997.
- Maunder, A.S., and Min, P.S., "Investigation of Rate Control in Routing Policies for B-ISDN Networks," *Proceedings of the 15th International Teletraffic Congress*, Washington D.C., June 1997.
- Yan, P.Y., Kim, K.B., Kim, K.S., and Min, P.S., "A Large Scale ATM Switch System Using Multi-Channel Switching Paradigm," *Proceedings of ATM Workshop*, Lisbon, Portugal, May 1997.
- Yan, P.Y., Kim, K.S., Min, P.S., and Hegde, M.V., "Multi-Channel Deflection Crossbar (MCDC): A VLSI Optimized Architecture for Multi-Channel ATM Switching," *Proceedings of IEEE INFOCOM 97*, Kobe, Japan, April 1997.
- Maunder, A., Rayes, A., and Min, P.S., "Analysis and Rate Controlling Link: Leaky Bucket with Finite Servers," *Proceedings of the 1997 Conference on Information Sciences and Systems*, Baltimore, March 1997.
- Shin, S.W., Min, P.S., and Kim, J.H., "Real Time Traffic Management System at Korean Mobile Telecom," *Proceedings of 19th Annual Pacific Telecommunications Conference*, pp. 113-121, Honolulu, Hawaii, January 1997.
- Min, P.S., Hegde, M.V., Chandra, A., and Maunder, A.S., "Analysis of Banyan Based Copy Networks with Internal Buffering," *Journal of High Speed Networks*, Volume 5, No. 3, pp. 259-275 November 1996.
- Vargas, C., Hegde, M.V., Naraghi-Pour, M., and Min, P.S., "Shadow Prices for Least Loaded Routing and Aggregated Least Busy Alternate Routing," *IEEE Transactions on Networking*, Volume 4, No. 5, pp. 796-807, October 1996.
- Shin, S.W., Kwon, S.M., and Min, P.S., "Capacity Analysis of CDMA with Nonuniform Cell Loading and Sizes," *Proceedings of the 34th Annual Allerton Conference*, October 1996.
- Hegde, M.V., Min, P.S., and Sohraby, K., "Note from Guest Editors," *Journal of Network and Systems Management*, Volume 4, No. 2, pp. 101-102, June 1996.
- Rayes, A. and Min, P.S., "Application of Shadow Price in Capacity Expansion of State Dependent Routing," *Journal of Network Systems Management*, Volume 4, No. 1, pp. 71-93, March 1996.
- Min, P.S., "PCS Revolution in the United States," *Electronics News*, No. 2277, January 22, 1996. Translated and published in Korean.

- Hegde, M.V., Min, P.S., and Sohraby, K., "Guest Editorial," *Journal of Network and Systems Management*, Volume 3, No. 4, pp. 347-349, December 1995.
- Min, P.S., Hegde, M.V., Saidi, H., and Chandra, A., "Nonblocking Copy Networks in Multi-Channel Switching," *IEEE Transactions on Networking*, Volume 3, No. 6, pp. 857-871, December 1995.
- Rayes, A. and Min, P.S., "Capacity Expansion of Least Busy Alternate Routing with Shadow Price," *Proceedings of GLOBECOM 95*, Singapore, November 1995.
- Min, P.S., Hegde, M.V., Chandra, A., and Maunder, A., "Throughput and Delay for Copy Networks with Internal Buffers," *Proceedings of the 33rd Annual Allerton Conference*, October 1995.
- Min, P.S., Hegde, M.V., Saidi, H., and Chandra, A., "Fanout Splitting in Nonblocking Copy Networks with Shared Buffering," *Proceedings of the 33rd Annual Allerton Conference*, October 1995.
- Min, P.S., Hegde, M.V., and Rayes, A., "Estimation of Exogenous Traffic Based on Link Measurements in Circuit-Switched Networks," *IEEE Transactions on Communications*, Volume 43, No. 8, pp. 2381-2390, August 1995.
- Maunder, A., Rayes, A., and Min, P.S., "Analysis of Routing Policies in Broadband Networks." Invited paper. *Canadian Journal of Electrical and Computer Engineering*, Special Issue on Planning and Designing of Broadband Networks, Volume 20, No. 3, pp. 125-136, July 1995.
- Min, P.S., Hegde, M.V., Saidi, H., and Chandra, A., "Architecture and Performance of Nonblocking Copy Networks with Multi-Channel Switching," *Proceedings of APCC 95*, pp. 531-535, Osaka, Japan, June 1995.
- Saidi, H., Min, P.S., and Hegde, M.V., "A New Structural Property of Statistical Data Fork," *IEEE Transactions on Networking*, Volume 3, No. 3, pp. 289-298, June 1995.
- Min, P.S., Saidi, H., and Hegde, M.V., "A Nonblocking Architecture for Broadband Multi-Channel Switching," *IEEE Transactions on Networking*, Volume 3, No. 2, pp. 181-198, April 1995.
- Min, P.S., Hegde, M.V., Saidi, H., and Chandra, A., "Multi-Channel Copy Networks: Architecture, Performance Model, Fairness, and Cell Sequencing," *Proceedings of IEEE INFOCOM 95*, pp. 931-938, Boston, April 1995.
- Min, P.S., Hegde, M.V., and Chandra, A., "Analysis of Packet Movements in Internally Buffered Copy Networks," *Third ORSA Telecommunications Conference*, p. 141, Boca Raton, Florida, March 1995.
- Maunder, A. and Min, P.S., "Routing for Multi-Rate Traffic with Multiple Qualities of Service," *Proceedings of the Third International Conference on Computer Communications and Networks*, pp. 104-108, San Francisco, September 1994.
- Saidi, H. and Min, P.S., "Performance Benefits of Multi-Channel Switching," *Proceedings of the 32nd Annual Allerton Conference*, pp. 583-592, September 1994.
- Min, P.S., "Book Review: 'Telecommunications Network Management into the 21st Century'," *IEEE Communications*, Volume 32, No. 7, pp. 5-8, July 1994.

- Saidi, H., Min, P.S., and Hegde, M.V., "Guaranteed Cell Sequence in Nonblocking Multi-Channel Switching," *Proceedings of IEEE INFOCOM 94*, Toronto, pp. 1420-1427, June 1994.
- Min, P.S., Hegde, M.V., Saidi, H., and Chandra, A., "Shared Buffering in Nonblocking Copy Networks," *Proceedings of the 1994 IEEE International Symposium on Information Theory*, Norway, p. 406, June 1994.
- Min, P.S., Hegde, M.V., and Rayes, A., "Real Time Traffic Estimation in Circuit-Switched Networks," *Proceedings of the 14th International Teletraffic Congress*, France, pp. 1175-1184, June 1994.
- Hegde, M.V., Min, P.S., and Rayes, A., "State Dependent Routing: Traffic Dynamics and Performance Benefits," *Journal of Network and Systems Management*, Volume 2, No. 2, pp. 125-149, June 1994.
- Saidi, H., Min, P.S., and Hegde, M.V., "Control of Packet Flow in Statistical Data Forks," *Proceedings of the 1994 International Conference on Communications*, New Orleans, pp. 415-419, May 1994.
- Saidi, H., Min, P.S., and Hegde, M.V., "Nonblocking Multi-Channel Switching in ATM Networks," *Proceedings of the 1994 International Conference on Communications*, New Orleans, pp. 701-705, May 1994.
- Maunder, A. and Min, P.S., "Analysis and Development of Routing Schemes for Multi-Rate, Multi-Point Traffic," *Proceedings of the 1994 Conference on Information Sciences and Systems*, Princeton, pp. 1041-1046, March 1994.
- Min, P.S., Hegde, M.V., and Chandra A., "Internal Buffering in Banyan-Based Copy Networks," *Proceedings of the 1994 Conference on Information Sciences and Systems*, Princeton, pp. 209-214, March 1994.
- Rayes, A. and Min, P.S., "Capacity Expansion in State Dependent Routing Schemes," *Proceedings of the 1994 Conference on Information Sciences and Systems*, Princeton, pp. 237-241, March 1994.
- Vargas, C., Hegde, M.V., Naraghi-Pour, M., and Min, P.S., "Shadow Prices for State Dependent Routing," *Proceedings of the 1994 Conference on Information Sciences and Systems*, Princeton, pp. 243-248, March 1994.
- Saidi, H., Min, P.S., and Hegde, M.V., "Non-Blocking Multi-Channel Switching." Invited paper. *Proceedings of the 31st Annual Allerton Conference*, pp. 335-344, September 1993.
- Min, P.S., Hegde, M.V., and Rayes, A., "Model Based Estimation of Exogenous Traffic," *Proceedings of the 1993 Conference on Information Sciences and Systems*, Baltimore, pp. 126-131, March 1993.
- Hegde, M.V., Min, P.S., and Rayes, A., "Performance Analysis of State Dependent Routing," *Proceedings of the 1993 Conference on Information Sciences and Systems*, pp. 695-700, Baltimore, March 1993.
- Hegde, M.V. and Min, P.S., "Telephone Networks," Magill Survey of Science Applied Science, Salem Press, pp. 2624-2630, 1992.

- Saidi, H., Min, P.S., and Hegde, M.V., "Assignment of 2^k Trunk Groups in Multi-Channel Switches Using Generalized Binary Addresses," *Proceedings of the 30th Annual Allerton Conference*, pp. 652-661, September 1992.
- Hegde, M.V. and Min, P.S., "Performance Analysis of State Dependent Routing." Invited paper. *Second ORSA Telecommunications Conference*, Boca Raton, Florida, February 1992.
- Rizzoni, R. and Min, P.S., "Detection of Sensor Failures in Automotive Engines," *IEEE Transactions on Vehicular Technology*, Volume 40, No. 2, pp. 487-500, May 1991.
- Min, P.S. and Hegde, M.V., "End-to-End Planning Models for Optimal Evolution of Telecommunications Network," *Proceedings of IEEE INFOCOM 90*, San Francisco, pp. 200-206, June 1990.
- Min, P.S., "Validation of Controller Inputs in Electronically Controlled Engines." Invited paper. *Proceedings of the 1990 American Control Conference*, pp.2887-2890, San Diego, May 1990.
- Min, P.S. and Youn, C., "Generic Equipment Models (GEM) for Consistent Planning of Telecommunications Networks," *Proceedings of the 1990 ISMM International Conference*, New Orleans, pp. 190-194, March 1990.
- Min, P.S., "Robust Application of Beard-Jones Detection Filter," *Advances in Computing and Control*, Springer-Verlag, Volume 130, pp. 162-173, 1989.
- Min, P.S. and Ribbens, W.B., "A Vector Space Solution to Incipient Sensor Failure Detection," *IEEE Transactions on Vehicular Technology*, Volume 38, No.3, pp. 148-158, August 1989.
- Min, P.S., "Robust Application of Beard-Jones Detection Filter," *Proceedings of the 1989 American Control Conference*, Pittsburgh, pp. 859-864, June 1989.
- Rizzoni, G. and Min, P.S., "Real Time Detection Filters for the On-board Diagnosis of Incipient Failures," *Proceedings of the 1989 International Symposium on Allied Technology and Automation*, pp. 1445-1466, Paper No. 89131, Florence, Italy, June 1989.
- Min, P.S., "Diagnosis of On-Board Sensors in Internal Combustion (IC) Engines," *Proceedings of the 1989 American Control Conference*, Pittsburgh, pp. 1065-1070, June 1989.
- Min, P.S., "Detection of Incipient Sensor Failures in Internal Combustion Engines," *Proceedings of the 1988 International Symposium on Allied Technology and Automation*, Paper No. 88038, Florence, Italy, June 1988.

Testimony Provided or Expected to Provide as Expert Witness

Matter: Patent Infringement for Wireless Local Area Networks
Law Firm: Quinn Emanuel Urquhard & Sullivan LLP

Case Name: Certain Audio Players and Components thereof (II). U.S.I.T.C. Inv. No. 337-TA-1330.

Testifying Expert for Google Inc.

Completed in June 2023.

(Expert reports submitted and deposed.)

Matter: Patent Infringement for Wireless Communications

Law Firm: Alston & Bird

Case Name: Atlas Global Technologies LLC v. ASUSTek Computers Inc. USDC WD TX

Civil Action No. 6:21-cv-820

Testifying Expert for ASUSTek

Completed in November 2023

(Expert report submitted.)

Matter: Patent Infringement for Wireless Communications

Law Firm: Perkins Coie

Case Name: Bell Northern Research, LLC v. HMD AMERICA, INC. et al., Case No.: 1:22-cv-22706-SCOLA/GOODMAN (S.D. Fla.)

Testifying Expert for HMD

Completed in December 2023

(Expert report submitted. Deposed.)

Matter: Patent Infringement for Wireless Communications

Law Firm: LAW OFFICES S. J. CHRISTINE YANG

Case Name: Atlas Global Technologies LLC v. ZyXEL Communications Corp. et al., U.S.D.C., W.D.T.X., Waco Div., Case No. 6:22-cv-00355 Atlas Global Technologies LLC v. D-Link Corp. U.S.D.C., W.D.T.X., Waco Div., Case No. 6:22-cv-00520

Testifying Expert for ZyXel

Retained in March 2023.

(Expert report submitted.)

Matter: Patent Infringement for Wireless Communications

Law Firm: Finnegan, Henderson, Farabow, Garrett & Dunner, LLP

Case Name: Bell Northern Research v. MeidaTek Inc.

Testifying Expert for MediaTek Inc.

Retained in August 2023.

Matter: Patent Infringement for Home Security System

Law Firm: Foley and Lardner LLP

Case Name: Alarm.com v. Vivint, Inc., AAA Arbitration Case. No. 01-22-0004-5525 and U.S.D.C. Case No. 2:23-cv-00004-JRG-RSP (E.D. Tex.),

Testifying Expert for Vivint, Inc.

Completed in 2023.

Matter: Patent Infringement for Wireless Communications and Electronics

Law Firm: Perkins Coie
Case Name: Bell Northern Research, LLC v. HMD AMERICA, INC. et al., Case No.: 1:22-cv-22706-SCOLA/GOODMAN (S.D. Fla.)
Testifying Expert for HMD
Completed in December 2023.

Matter: Patent Infringement for Network Switches
Law Firm: Charhon Callahan Robson & Garza, PLLC
Case Name: Sable Networks, Inc. and Sable IP, LLC v. CouldFlare, Inc. U.S.D.C. WD Tx
Case No. 6:21-cv-261
Testifying Expert for CloudFlare, Inc.
Completed in January 2024.
(Expert report submitted and deposited.)

Matter: Patent Infringement for Network Security
Law Firm: Fish and Richardson
Case Name: Finjan LLC v. Palo Alto Networks, Inc. – Case No. 4:14-cv-04908-PJH. USDC
ND CA, Oakland Division.
Testifying Expert for Finjan LLC.
Retained in September 2022.
(Expert report submitted and deposited.)

Matter: Patent Infringement for Network Management
Law Firm: Irell & Manella LLP
Case Name: SNMP Research, Inc. & SNMP Research International, Inc. v. Broadcom Inc.,
Brocade Communications Systems LLC, & Extreme Networks, Inc. U.S.D.C.
E.D. Tennessee at Knoxville Case No. 3:20-CV-451
Testifying Expert for SNMP Research.
Retained in May 2022.

Matter: Inter Parte Reexamination for Wireless Communications
Law Firm: Finnegan, Henderson, Farabow, Garrett & Dunner, LLP
Case Name: Patent reexamination in front of the U.S.P.T.O.
Testifying Expert for MediaTek
Retained in March 2023.

Matter: Patent Infringement for Network Switching
Law Firm: Baker Botts
Case Name: Corrigent Corp. v. Arista Networks, Inc., Case No. 1:22-cv-00497-UNA. USDC
Delaware
Testifying Expert for Arista
Retained in October 2022.

Matter: Patent Infringement for Mobile Devices
Law Firm: Fish and Richardson
Case Name: GComm v. Samsung, U.S.D.C. ED. TX. Case No.:2:22-cv-0078-JRG

Testifying Expert for Samsung
Completed in January 2024.

Matter: Patent Infringement for Wireless Networks
Law Firm: McKool Smith
Case Name: Certain Mobile Telephones, Tablet Computers with Cellular Connectivity, and Smart Watches with Cellular Connectivity, Components Thereof, and Products Containing Same. U.S.I.T.C. Inv. No. 337-TA-1299
Testifying Expert for Ericsson
Completed in July 2022.
(Expert report submitted and deposed.)

Matter: Patent Infringement for Semiconductor Manufacturing
Law Firm: Kramer Levin
Case Name: Oasis Tooling, Inc. v. Siemens Indus. Software, Inc., 1:22-cv-151 (D. Del.), Oasis Tooling, Inc. v. GlobalFoundries U.S. Inc., 1:22-cv-312 (D. Del.)
Testifying Expert for Oasis Tooling
Retained in June 2022.
(Expert reports submitted.)

Matter: Patent Infringement for Optical Networks
Law Firm: Duane Morris
Case Name: NextGen Innovations, LLC v. Infinera Corporation. U.S.D.C. ED. TX (Marshall)
Case No. 2:22-cv-00306-JRG-RSP / IPR
Testifying Expert for Infinera
Retained in April 2023.

Matter: Patent Infringement for Wireless Devices
Law Firm: King and Spalding LLP
Case Name: Intellectual Ventures, et. al. v. General Motors Company and General Company Motors, LLC, Case No. 6:21-CV-1088 pending in the Western District of Texas, Waco Division
Testifying Expert for General Motors
Completed in January 2023.
(Expert report submitted.)

Matter: Patent Infringement for Wireless Devices
Law Firm: Sterne Kessler
Case Name: Neo Wireless LLC v. Volkswagen Group of America, Inc. and Volkswagen Group of America Chattanooga Operations, LLC and related matters
Testifying Expert for Volkswagen
Completed in September 2023.
(Expert report submitted and deposed. IPR declarations submitted)

Matter: Patent Infringement for Wireless Networks
Law Firm: Covington & Burling LLP

Case Name: XR Communications, LLC v. D-Link Systems, Inc., No. 8:17-cv-00596
(Consolidated) (C.D. Cal.)
Testifying Expert for Hewlett Packard Enterprise
Completed
(Expert report submitted and deposited.)

Matter: Patent Infringement for USB Charging System
Law Firm: Orrick, Herrington & Sutcliffe LLP
Case Name: Fundamental Innovation Systems International LLC v. TCT Mobile (US), TCT
Mobile (US) Holdings, Inc., et al. U.S.D.C. Delaware No. 20-552-RGA-CJB
Testifying Expert for TCL
Completed in June 2022.
(Expert report submitted and deposited.)

Matter: Inter Parte Reexamination for Wireless Communications
Law Firm: Alston & Bird
Case Name: Patent reexamination in front of the U.S.P.T.O.
Testifying Expert for Nokia
Retained in May 2022.
(Expert report submitted.)

Matter: Patent Infringement for Network Management System
Law Firm: Morgan, Lewis & Bockius, LLP
Case Name: Certain Routers, Access Points, Controllers, Network Management Devices,
Other Networking Products, and Hardware and Software Components Thereof,
U.S.I.T.C. Inv. No. 337-TA-1227
Testifying Expert for Hewlett Packard, Netgear, and CommScope
Completed in August 2021.
(Expert report submitted, deposited, and testified during trial.)

Matter: Patent Infringement for Security Systems
Law Firm: Forley and Lardner LLP
Case Name: Certain Residential Premises Security Monitoring and Automation Control
Panels, and Components Thereof (ITC Inv. No. 337-TA-1273) and ADT LLC et
al v. Vivint, Inc., Case No. 6:21-cv-00687 (W.D. Tex.)
Testifying Expert for Vivint, Inc.
Completed in April 2022.
(Expert report submitted, deposited, and testified during trial.)

Matter: Inter Parte Reexamination for Internet Communications
Law Firm: Perkins Coie
Case Name: Patent reexamination in front of the U.S.P.T.O.
Testifying Expert for Twitter
Retained in June 2020.
(Expert report submitted.)

- Law Firm: Fisher Broyles
Case Name: Vaxcel International Co., Ltd. v. Heathco LLC, U.S.D.C. Delaware No. 20-224-LPS
Testifying Expert for Vaxcel
Retained in February 2021.
(Expert report submitted and deposed.)
- Matter: Patent Infringement for Network Communication System
Law Firm: Charhon Callahan Robson & Garza, PLLC
Case Name: Sable Networks, Inc. and Sable IP, LLC, v. ClouFlare, Inc. U.S.D.C. WDTX, Civil Action No. 6:21-cv-261
Testifying Expert for CloudFlare, Inc.,
Completed in January 2024.
- Matter: Patent Infringement for Mobile Wireless Device
Law Firm: Pearl Cohen
Case Name: In the Matter Of Certain UMTS And LTE Cellular Communications Modules And Products Containing The Same, U.S.I.T.C. Inv. No. 337-TA-1240
Testifying Expert for Telit Wireless Communication, Quectel, and Thales
Completed in March 2023.
(Expert reports submitted and deposed.)
- Matter: Transactional Taxes for Internet Application
Law Firm: Ryan Rapp & Underwood, PLC
Case Name: ADP, LLC v. Arizona Department of Revenue (TX2018-000246),
Testifying Expert for ADP, LLC.
Completed in June 2020.
(Expert report submitted.)
- Matter: Trade Secret Misappropriation in Digital Electronics
Law Firm: Goodwin Proctor LLP
Case Name: Guzik Technical Enterprises versus Keysight Technologies, Inc. Superior Court of the State of California for the County of Santa Clara, Case No.: 19CV355879
Testifying Expert for Keysight Technologies, Inc.
Retained in August 2020.
- Matter: Patent Infringement for Fiber Optic Devices
Law Firm: Cooley
Case Name: Certain High-Density Fiber Optic Equipment and Components Thereof, U.S.I.T.C. Inv. No. 337-TA-1194
Testifying Expert for AFL Communications, Panduit, FS.Com, Wirewerk, and Siemon
Completed in October 2020.
(Expert reports submitted, deposed, and testified during trial.)
- Matter: Patent Infringement for Optical Transport Networks

- Law Firm: Venerble
Case Name: Huawei Technologies Co. Ltd v Verizon Communications, Inc., et. al., 2:20-cv-0030
Testifying Expert for Verizon.
Retained in March 2020.
(IPR declarations submitted.)
- Matter: Patent Infringement for Lighting System
Law Firm: Fisher Broyles
Case Name: Vaxcel International Co., Ltd., v. Jasco Products Company, LLC., (Case No. USDC Western District of Oklahoma, 5:19-CV-00154-JD
Testifying Expert for Vaxcel.
Retained in August 2020.
- Matter: Patent Infringement for Wireless Communication
Law Firm: McDermott Will & Emery
Case Name: Bell Northern Research LLC v. ZTE. (Case No. 3:18-cv-01786 - S.D. Cal)
Testifying Expert for ZTE.
Retained in July 2019.
(IPR declarations submitted.)
- Matter: Patent Infringement for Wireless Communication
Law Firm: Jones Day
Case Name: Bell Northern Research LLC v. Kyocera Corp. (Case No. 3:18-cv-1785 - S.D. Cal)
Testifying Expert for Kyocera.
Completed in May 2019.
(Claim construction declaration submitted, and deposed.)
- Matter: Patent Infringement for Electronic Payment Systems
Law Firm: Paul Hastings
Case Name: ID Tech Corp. v. Samsung Electronics Co., Ltd., et al. (Case No. No. 8:17-cv-1748-DOC-JDE (C.D. Cal))
Testifying Expert for Samsung.
Retained in January 2019.
(Expert reports submitted, and deposed.)
- Matter: Patent Infringement for Internet Switching
Law Firm: Maynard Cooper
Case Name: Parity Networks, LLC v. Juniper Networks, Inc., Case No. 6:17-CV-00495-RWS-KNM (U.S.D.C.E.D. Tx.)
Testifying Expert for Juniper.
Retained in April 2018.
(IPR declarations submitted.)
- Matter: Patent Infringement for Internet Switching

Law Firm: Morgan Lewis
Case Name: Parity Networks, LLC v. Hewlett Packard Enterprise Company, Case No. 6:17-CV-00682 (U.S.D.C.E.D. Tx.)
Testifying Expert for Hewlett Packard Enterprise Company.
Retained in September 2018.
(IPR declarations submitted.)

Matter: Inter Parte Rexamination for Covered Business Method
Law Firm: Reed Smith LLP
Case Name: NASDAQ v. Miami International
Expert for Miami International.
Retained in February 2018.
(Expert declarations submitted, and deposited.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Quinn Emanuel
Case Name: Qualcomm v. Apple, Case No. 3:17-cv-00108-GPC-MDD (U.S.D.C.S.D. Cal.)
Testifying Expert for Qualcomm.
Completed in April 2019.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for Communication Devices
Law Firm: Venable
Case Name: Sycamore IP Holdings LLC v. Verizon Communications Inc, Case No. 2:16-cv-591-JRG-RSP (U.S.D.C. E.D. Texas)
Testifying Expert for Verizon and Level 3.
Completed in September 2017.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Alston Bird
Case Name: Huawei Technologies Co. Ltd. V. Nokia Solutions and Networks, Case No. 2:16-cv-0056-JRG-RSP (U.S.D.C. E.D. Texas)
Testifying Expert for Nokia.
Completed in December 2017.
(Expert reports submitted.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Quinn Emanuel
Case Name: Huawei Technologies Co. Ltd. V. Samsung Electronics C. Ltd, Case No. 3:16-cv-02787 (U.S.D.C. N.D. Cal)
Testifying Expert for Samsung.
Completed in March 2019.
(Expert reports submitted, and deposited.)

Matter: Arbitration for Licensing
Law Firm: Alston Bird
Case Name: Nokia v. LG Electronics, International Chamber of Commerce Arb. No. 21326
Testifying Expert for Nokia.
Completed in October 2016.
(Expert reports submitted.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Ropes and Gray
Case Name: Godo Kaisha IP Bridge 1 v. TCL Communication Technology Holdings, Case No. 15-634-SLR-SRF (U.S.D.C.S.D. Delaware.)
Testifying Expert for IP Bridge.
Completed in October 2018.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Paul Hastings
Case Name: Odyssey Wireless, Inc., v. Samsung Electronics Co., Ltd., et al, Case No. 3:15-cv-1738-H-RBB (U.S.D.C.S.D. Cal.)
Testifying Expert for Samsung.
Completed in October 2016.
(Expert reports submitted.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Greenberg Traurig
Case Name: Mobile Telecommunications Technologies LLC v. Amazon.com, Inc., 2:13-cv-883-JRG-RSP (U.S.D.C. E.D. Texas)
Testifying Expert for Amazon.
Completed in April 2015.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Mayer Brown
Case Name: Mobile Telecommunications Technologies LLC v. LG Electronics Mobilecomm U.S.A., Inc., 2:13-cv-947-JRG-RSP (U.S.D.C. E.D. Texas)
Testifying Expert for LG Electronics Mobilecomm.
Completed in February 2016.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for Semiconductor Devices
Law Firm: Mayer Brown
Case Name: Inter Parte Reexamination for U.S. Patent Nos. 6,895,520 and 6,899,332
Expert for LG Electronics.
Completed in February 2016.
(Expert declaration submitted, and deposited.)

- Matter: Patent Infringement in Vehicular Electronics
Law Firm: Gardner, Linn, Burkhardt & Flory, L.L.P
Case Name: *Magna Electronics Inc. v. TRW Automotive Holdings Corp. et al.*, Civil Action No. 1:12-cv-00654 (Western District of Michigan), and relating to the action styled *Magna Electronics Inc. v. TRW Automotive Holdings Corp. et al.*, Civil Action No. 1:13-cv-00324 (Western District of Michigan).
Testifying Expert for Magna Electronics
Completed in February 2016.
(Expert reports submitted, and deposed.)
- Matter: Patent Infringement in Electronic Circuits
Law Firm: Ropes and Gray
Case Name: Certain Devices Containing Non-Volatile Memory and Products Containing the Same (USITC Inv. Nos. 337-TA-922)
Testifying Expert for Spansion Inc.
Completed in February 2015.
(Expert reports submitted.)
- Matter: Trade Secret Misappropriation in Software Method for Cable Television Advertisement
Law Firm: Brownstein Hyatt Farber Schreck
Case Name: Cross MediaWorks v. EMT Holdings, USDC Southern District of New York, Case No. 1:14-cv-00561-VSB
Testifying Expert for Cross MediaWorks.
Completed in April 2015.
(Testified during injunction hearing.)
- Matter: Patent Infringement in Vehicular Electronics
Law Firm: Steptoe and Johnson
Case Name: Certain Vision-Based river Assistance System Cameras and Components Thereof (USITC Inv. Nos. 337-TA-899 and 907)
Testifying Expert for Magna Electronics
Completed in February 2015.
(Expert reports submitted, deposed, and testified during trial.)
- Matter: Patent Infringement for Vehicular System
Law Firm: Susman Godfrey
Case Name: Eagle Harbor Holdings, LLC, and Mediustech, LLC, v. Ford Motor Company, 3:11-cv-05503-BHS (U.S.D.C. Western District of Washington at Tacoma)
Testifying Expert for Mediustech.
Completed in March 2015.
(Expert reports submitted, deposed, and testified during trial.)
- Matter: Patent Infringement for Communication Networks
Law Firm: Davis Polk & Wardwell LLP

Case Name: Sprint Communications Company L.P., v. Comcast Cable Communications, LLC, Comcast IP Phone, LLC, and Comcast Phone of Kansas, LLC. 2:11-cv-02684-KHV-DJW (U.S.D.C. Kansas)
Testifying Expert for Comcast.
Retained in March 2012.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Communication Networks
Law Firm: Quinn Emanuel
Case Name: France Telecom S.A. v. Marvell Semiconductor, Inc., 12-Civ-4986 (S.D.N.Y.)
Testifying Expert for Marvell.
Completed in September 2014.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Wireless Image Distribution
Law Firm: Jones Day
Case Name: *Inter Partes* Review of U.S. Patent No. 8,437,797
Expert for Google Inc.
Completed in November 2014.
(Expert declaration submitted.)

Matter: Nonvolatile Semiconductor Memories
Law Firm: Jones Day
Case Name: *Inter Partes* Review of U.S. Patent Nos. 8,301,833 and 8,516,187
Expert for SanDisk.
Completed in May 2014.
(Expert declaration submitted.)

Matter: Communication Protocols for Wireless Device
Law Firm: Dorsey & Whitney, LLP
Case Name: Certain Point-To-Point Network Communication Devices and Products Containing Same (USITC Inv. No. 337-TA-892)
Testifying Expert for Toshiba
Completed in May 2014.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Wireless Networks
Law Firm: Ropes and Gray
Case Name: In the Matter of Certain Wireless Devices With 3G and/or 4G Capabilities and Components Thereof (USITC Inv. No. 337-TA-868) InterDigital Comms., Inc. v. Huawei Techs. Co., Ltd., No. 13-00008 (D. Del., filed January 2, 2013), InterDigital Comms., Inc. v. ZTE Corp., No. 13-00009 (D. Del., filed January 2, 2013), InterDigital Comms., Inc. v. Nokia Corp., No. 1:13-cv-00010 (D. Del., filed January 2, 2013), InterDigital Comms., Inc. v. Samsung Elec. Co., Ltd., No. 13-00011 (D. Del., filed January 2, 2013)
Testifying Expert for Joint Defense Group.

Completed in February 2014.
(Expert reports submitted, deposed, and testified during trials.)

Matter: Patent Infringement for Mobile Communication
Law Firm: Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P.
Case Name: Certain Digital Media Devices, Including Televisions, Blu-Ray Disc Players, Home Theater Systems, Tablets and Mobile Phones, Components Thereof and Associated Software (USITC Inv. No. 337-TA-882)
Testifying Expert for LG Electronics, Inc.
Completed in February 2014.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Wireless Networks
Law Firm: Vinson & Elkins LLP
Case Name: Wi-LAN USA, Inc. and Wi-LAN, Inc. v. Telefonaktiebolaget LM Ericsson and Ericsson, Inc. (USDC: Southern District of FL - Case #1: 12-cv-23569), Wi-LAN USA, Inc. and Wi-LAN, Inc. v. Alcatel-Lucent USA, Inc. (USDC: Southern District of FL - Case #1: 12-cv-23568-Altonaga/Simonton)
Testifying Expert for Wi-LAN.
Completed in May 2015.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Data Storage
Law Firm: Ropes and Gray, Weil Gotshal
Case Name: Summit Data Systems, LLC v. EMC Corporation., et al. 1:10-cv-00749-GMS (U.S.D.C. Delaware)
Testifying Expert for EMC Corporation and Netapp, Inc.
Completed in December 2012.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Wireless Mobile Device
Law Firm: Ashurst Australia
Case Name: Samsung v. Apple, Australian Federal Court Proceeding No. NSD 1243 of 2011
Testifying Expert for Samsung Electronics.
Completed in December 2012.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Wireless Mobile Devices
Law Firm: Quinn Emanuel
Case Name: Apple Inc. v. Samsung Electronics Co., Ltd., et al., 4:11-cv-01846-LHK (N.D. Cal.) and Samsung Electronics Co., Ltd., et al. v. Apple Inc., 4:11-cv-02079 (N.D. Cal.)
Testifying Expert for Samsung Electronics.
Completed in July 2012.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Wireless Mobile Device
Law Firm: Quinn Emanuel
Case Name: Certain Electronic Devices, Including Wireless Communication Devices, Portable Music And Data Processing Devices, And Tablet Computer, U.S.I.T.C. Inv. No. 337-TA-794
Testifying Expert for Samsung Electronics.
Completed in June 2012.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Portable Storage Device
Law Firm: White and Case
Case Name: CERTAIN UNIVERSAL SERIAL BUS (“USB”) PORTABLE STORAGE DEVICES, INCLUDING USB FLASH DRIVES AND COMPONENTS THEREOF, US International Trade Commission Investigation No. 337-TA-788
Testifying Expert Witness for Trek
Completed in May 2012.
(Expert reports submitted, and deposed.)

Matter: Copyright Infringement for Petroleum Processing Software
Law Firm: Osha Liang LLP
Case Name: Aspen Technology, Inc. v. Tekin A. Kunt and M3 Technology, Inc., Case Number: H-10-1127, US District Court, Texas, Houston Division.
Testifying Expert for M3 Technology, Inc.
Completed in May 2012.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Trade Secret Misappropriation for DC-DC converter
Law Firm: Covington & Burling, Haynes Boone
Case Name: Certain DC—DC Controllers and Products Containing Same, US International Trade Commission Investigation No. 337-TA-698
Testifying Expert for UPI.
Completed in March 2012.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Parallel Processor
Law Firm: Orrick, Herrington, & Sutcliffe. Kirkland and Ellis.
Case Name: BIAx Corporation v. Nvidia and Sony Civil Action No. 09-cv-01257-PAB-MEH
Testifying Expert for Nvidia and Sony
Completed in March 2012.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Call Center Technology
Law Firms: Duffy, Sweeney, and Scott. Foley Lardner.
Case Name: Ronald Katz Technology Licensing v. Citizens Financial Group 7-ML-1816-C RGK (FFM)
Testifying Expert Witness for Citizens Financial Group.

Completed in 2011.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Storage Area Network
Law Firm: DLA Piper
Case Name: Network Appliance, Inc., v. Sun Microsystems, Inc., Case Number: C-07-06053
EDL, US District Court, Northern District of California, San Francisco Division.
Testifying Expert for Sun Microsystems, Inc.
Completed in 2010.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Flat Panel Display Controller
Law Firm: Jones Day
Case Name: Certain Video Displays, Components Thereof, and Products Containing Same, US
International Trade Commission Investigation No. 337-TA-687
Testifying Expert for Vizio, Inc.
Completed in 2010.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Call Center Technology
Law Firms: Foley Lardner
Case Name: Ronald Katz Technology Licensing v. US Bank 7-ML-1816-C RGK (FFM)
Testifying Expert Witness for US Bank
Completed in May 2009.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for USB to VGA Converter
Law Firm: Wang Hartmann, Gibbs, & Cauley, P.C.
Case Name: Displaylink Corporation v. Magic Control Technology Corporation, Case No.
5:07-CV-01998-RMW, US District Court, Northern District of California, San
Francisco Division.
Testifying Expert for Magic Control Technology Corporation
Completed in 2009.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Flash Memory
Law Firm: Jones Day and Wilson Sansini
Case Name: Certain Flash Memory Controllers, Drives, Memory Card, and Media Players and
Products Containing Same. US International Trade Commission Investigation
No. 337-TA-619
Testifying Expert for SanDisk Corporation.
Completed in 2008.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Semiconductor Packaging
Law Firm: Jones Day

Case Name: Certain Semiconductor Chips with Minimized Chip Package Size and Products Containing the Same. US International Trade Commission Investigation No. 337-TA-605

Testifying Expert for Freescale Semiconductor

Completed in 2008.

(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Automatic Switching System

Law Firms: Jones Day, and Heller Ehrman, LLP.

Case Name: ATEN International Co., Ltd and ATEN Technology, Inc. v. Belkin Corporation, Belkin Logistics, Inc. and Emine Technology Co., Ltd. US International Trade Commission Investigation No. Ltd 337-TA-589

Testifying Expert for Belkin Corporation, Belkin Logistics, Inc., and Emine Technology Co., Ltd.

Completed in 2007.

(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Dual Mode Communication

Law Firm: Wilmer Cutler Pickering Hale and Dorr, LLP

Case Name: Broadcom Corporation v. Qualcomm Incorporated SACV05-467-JVS (RNBx)

Testifying Expert Witness for Broadcom Corporation

Completed in 2007.

(Expert reports submitted, deposed, and testified during trial.)