

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Barry A. Hoberman, *et al.*
U.S. Patent No.: 8,854,077 Attorney Docket No.: 44508-0023IP3
Issue Date: October 7, 2014
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Filing Date: August 8, 2012
Title: LOW LEAKAGE AND DATA RETENTION CIRCUITRY

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**PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT
NO. 8,854,077 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42**

TABLE OF CONTENTS

I.	REQUIREMENTS FOR IPR.....	1
A.	Grounds for Standing	1
B.	Challenge and Relief Requested	1
II.	THE '077 PATENT	2
A.	Brief Description	2
B.	Summary of the Prosecution History	5
C.	Level of Ordinary Skill in the Art	5
D.	Claim Construction.....	6
III.	THE CHALLENGED CLAIMS ARE UNPATENTABLE.....	6
A.	GROUND 1A—CLAIMS 1-18 ARE OBVIOUS OVER TAKAHASHI	6
1.	Overview of Takahashi	6
2.	Claim 1	10
3.	Claim 2	29
4.	Claim 3	31
5.	Claim 4	33
6.	Claim 5	33
7.	Claim 6	34
8.	Claim 7	35
9.	Claim 8	37
10.	Claim 9	39
11.	Claim 10	39
12.	Claim 11	40
13.	Claim 12	40
14.	Claim 13	40
15.	Claim 14	40
16.	Claim 15	40
17.	Claim 16	40
18.	Claim 17	41

19. Claim 18	41
B. GROUND 1B—CLAIMS 3 AND 12 ARE OBVIOUS OVER TAKAHASHI IN VIEW OF KO	41
1. Overview of Ko	41
2. Takahashi-Ko Combination	43
3. Claim 3	48
4. Claim 12	53
C. GROUND 1C—CLAIMS 5 AND 14 ARE OBVIOUS OVER TAKAHASHI IN VIEW OF SCHUTZ	53
1. Overview of Schutz	53
2. Takahashi-Schutz Combination	55
3. Claim 5	61
4. Claim 14	62
D. GROUND 2A—CLAIMS 1-18 ARE OBVIOUS OVER MIZUNO	62
1. Overview of Mizuno	62
2. Claim 1	66
3. Claim 2	81
4. Claim 3	83
5. Claim 4	85
6. Claim 5	87
7. Claim 6	88
8. Claim 7	90
9. Claim 8	91
10. Claim 9	93
11. Claim 10	94
12. Claim 11	96
13. Claim 12	96
14. Claim 13	96
15. Claim 14	96
16. Claim 15	96

17. Claim 16	96
18. Claim 17	96
19. Claim 18	96
E. GROUND 2B—CLAIMS 3 AND 12 ARE OBVIOUS OVER MIZUNO IN VIEW OF KO	96
1. Mizuno-Ko Combination	96
2. Claim 3	103
3. Claim 12	104
IV. THE BOARD SHOULD CONSIDER THE PETITION ON THE MERITS	105
A. Discretionary Denial under Section 325(d) Is Not Warranted.....	105
B. Discretionary Denial under Section 314(a) Is Not Warranted.....	106
C. The <i>Fintiv</i> Factors Weigh Against Discretionary Denial	107
V. CONCLUSION	107
VI. PAYMENT OF FEES.....	107
VII. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(A)(1).....	108
A. Real Party-in-Interest under 37 C.F.R. § 42.8(b)(1)	108
B. Related Matters under 37 C.F.R. § 42.8(b)(2)	108
C. Lead and Back-Up Counsel under 37 C.F.R. § 42.8(b)(3)	108
D. Service Information	108

LIST OF EXHIBITS

MTK-1001	U.S. Patent No. 8,854,077 to Hoberman, <i>et al.</i> (“’077 Patent)
MTK-1002	Excerpts from the Prosecution History of the ’077 Patent
MTK-1003	Declaration of Dr. Paul Min, Ph.D.
MTK-1004	U.S. Patent Publication No. 2003/0025130 to Takahashi, <i>et al.</i> (“Takahashi”)
MTK-1005	U.S. Patent Publication No. 2003/0102904 to Mizuno, <i>et al.</i> (“Mizuno”)
MTK-1006	U.S. Patent No. 7,091,766 to Ko, <i>et al.</i> (“Ko”)
MTK-1007	U.S. Patent No. 5,440,520 to Schutz, <i>et al.</i> (“Schutz”)
MTK-1008	Excerpts from Alan C. Dixon, <i>et al.</i> , <i>A Practical Approach to Digital Electronics</i> , 2000
MTK-1009	Excerpts from John D. Carpinelli, <i>Computer Systems Organization and Architecture</i> , 2001
MTK-1010	U.S. Patent No. 6,141,762 to Nicol, <i>et al.</i> (“Nicol”)
MTK-1011	U.S. Patent No. 6,087,813 to Tobita (“Tobita”)
MTK-1012	U.S. Patent No. 6,809,538 to Borkar (“Borkar”)
MTK-1013	U.S. Patent No. 6,518,826 to Zhang (“Zhang”)
MTK-1014	U.S. Patent No. 7,042,274 to Hazucha, <i>et al.</i> (“Hazucha”)
MTK-1015	Excerpts from Modern Dictionary of Electronics, Seventh Edition, 1999
MTK-1016	Excerpts from Dictionary of Science and Technology, 2003
MTK-1017	Excerpts from Adel S. Sedra, <i>et al.</i> , <i>Microelectronic Circuits</i> , 1998 (“Sedra”)
MTK-1018	U.S. Patent No. 6,791,361 to Alon, <i>et al.</i> (“Alon”)

- MTK-1019 Complaint from MOSAID Technologies Inc. v. MediaTek, Inc. *et al.*, Case No. 2:23-CV-00129, ECF No. 1 (E.D. Tex. Mar. 28, 2023)
- MTK-1020 Affidavit of Service of Summons and Complaint on MediaTek USA, Inc. in MOSAID Technologies Inc. v. MediaTek, Inc. *et al.*, Case No. 2:23-CV-00129, ECF. No. 9 (E.D. Tex. Mar. 30, 2023)
- MTK-1021 MOSAID Technologies Inc.’s Disclosure of Asserted Claims and Infringement Contentions in Case No. 2:23-CV-00129, Dated July 6, 2023
- MTK-1022 Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, Katherine K. Vidal (USPTO June 21, 2022)
- MTK-1023 Petitioner’s *Sotera* Stipulation
- MTK-1024 Declaration of June A. Munford
- MTK-1025 Claim Construction Order in *Mosaid Technologies Inc. v. Freescale Semiconductor, Inc.*, Case No. 6:11-cv-00173 (E.D. Tex. April 29, 2013)
- MTK-1026 Claim Construction Order in *Conversant Intellectual Property Management Inc., et al. v. Xilinx, Inc.*, Case No. 6:12-cv-00847 (E.D. Tex. January 9, 2015)

LISTING OF CHALLENGED CLAIMS

Claim 1	
1[p]	A method carried out in an integrated circuit that includes an adaptive leakage controller, a power manager and a plurality of power islands, the method comprising:
1[a]	receiving, at the power manager, a control signal from the adaptive leakage controller; and
1[b]	employing the power manager to dynamically change power consumptions of the plurality of power islands, the employing the power manager to dynamically change power consumptions including: generating a variable voltage based on the control signal; and providing the variable voltage to at least one of low leakage sleep circuits of the integrated circuit.
Claim 2	
2	The method as claimed in claim 1 further comprising putting to sleep and taking out of sleep, at different times, at least one of the power islands.
Claim 3	
3	The method as claimed in claim 2 wherein the power manager employs a state machine to control the putting to sleep and the taking out of sleep.
Claim 4	
4	The method as claimed in claim 1 wherein the variable voltage is an optimum voltage.
Claim 5	
5	The method as claimed in claim 4 wherein the optimum voltage is dependent upon both process variation and temperature variation.
Claim 6	
6	The method as claimed in claim 4 wherein the optimum voltage is generated by a sleep generator.

Claim 7	
7	The method as claimed in claim 1 wherein the control signal is a digital signal.
Claim 8	
8	The method as claimed in claim 1 wherein the at least one of the low leakage sleep circuits is connected in series to a source of a supply voltage and to a logic gate or storage cell of one of the power islands.
Claim 9	
9	The method as claimed in claim 8 wherein the at least one of the low leakage sleep circuits modifies the supply voltage to the one of the power islands during a sleep mode.
Claim 10	
10[p]	A method carried out in an integrated circuit that includes an adaptive leakage controller, a power manager, a plurality of power islands and a plurality of low leakage sleep circuits, the method comprising:
10[a]	receiving, at the power manager, a control signal from the adaptive leakage controller; and
10[b]	employing the power manager to dynamically change power consumptions of the plurality of power islands, the employing the power manager to dynamically change power consumptions including: generating a variable voltage based on the control signal; and providing the variable voltage to the plurality of low leakage sleep circuits,
10[c]	wherein each of low leakage sleep circuits is associated with leakage reduction of a respective one of the plurality of power islands.
Claim 11	
11	The method as claimed in claim 10 further comprising putting to sleep and taking out of sleep, at different times, at least one of the power islands.
Claim 12	
12	The method as claimed in claim 11 wherein the power manager employs a state machine to control the putting to sleep and the taking out of sleep.

Claim 13	
13	The method as claimed in claim 10 wherein the variable voltage is an optimum voltage.
Claim 14	
14	The method as claimed in claim 13 wherein the optimum voltage is dependent upon both process variation and temperature variation.
Claim 15	
15	The method as claimed in claim 13 wherein the optimum voltage is generated by a sleep generator.
Claim 16	
16	The method as claimed in claim 10 wherein the control signal is a digital signal.
Claim 17	
17	The method as claimed in claim 10 wherein at least one of the low leakage sleep circuits is connected in series to a source of a supply voltage and to a logic gate or storage cell of an associated one of the power islands.
Claim 18	
18	The method as claimed in claim 17 wherein the at least one of the low leakage sleep circuits modifies the supply voltage to the associated one of the power islands during a sleep mode.

MediaTek Inc. and MediaTek USA Inc. (“Petitioner” or “MediaTek”) petitions for *Inter Partes* Review (“IPR”) of claims 1-18 (“Challenged Claims”) of U.S. Patent No. 8,845,077 (“’077 Patent”).

I. REQUIREMENTS FOR IPR

A. Grounds for Standing

Petitioner certifies that the ’077 Patent is available for IPR, and Petitioner is not barred or estopped from requesting review of the Challenged Claims. The Petition is filed within one year of service of a complaint against Petitioner in *Mosaid Technologies Inc. v. MediaTek Inc., MediaTek USA, Inc.*, Case No. 2:23-cv-00129 (E.D. Tex. March 2023). *See* MTK-1019; MTK-1020.

B. Challenge and Relief Requested

Petitioner requests IPR of the Challenged Claims on the grounds below. Dr. Paul Min provides supporting explanations in his declaration (MTK-1003) cited throughout this petition.

Ground	Claims	Pre-AIA §103 Basis
1A	1-18	Takahashi (MTK-1004)
1B	3, 12	Takahashi in view of Ko (MTK-1006)
1C	5, 14	Takahashi in view of Schutz (MTK-1007)
2A	1-18	Mizuno
2B	3, 12	Mizuno in view of Ko

Each reference pre-dates the '077 Patent's earliest possible priority date (February 19, 2004; "Critical Date") and qualifies as prior art.¹

Reference	Date	Prior Art Under
Takahashi	February 6, 2003 (published)	§102(b)
Mizuno	June 6, 2003 (published)	§102(a)/(e)
Ko	July 3, 2003 (filed)	§102(e)
Schutz	August 8, 1995 (issued)	§102(b)

II. THE '077 PATENT

A. Brief Description

The '077 Patent relates to reducing power consumption in integrated circuits. MTK-1001, Title, Abstract, 1:29-39; MTK-1003, ¶64. An integrated circuit's total power consumption includes the power consumed while it is active and while it is inactive (idle). MTK-1001, 1:34-36; MTK-1003, ¶65. The idle power consumption is due to leakage current, which is the current flowing through the integrated circuit even while it is not performing its designed function. MTK-1001, 1:40-47; MTK-1003, ¶65

¹ In co-pending litigation between Patent Owner MOSAID Technologies Inc. ("Patent Owner" or "MOSAID") and Petitioner, MOSAID asserts the Challenged Claims are entitled to an invention date at least as early as December 11, 2003. MTK-1021, 8. Petitioner does not concede the '077 Patent is entitled to claim priority to the Critical Date or any earlier date.

The '077 Patent acknowledges that methods of reducing leakage current were well-known in the art. MTK-1001, 1:48-2:20; MTK-1003, ¶66. One solution is to include a sleep transistor in series between the circuit and a supply voltage (e.g., VDD or VSS) to act as a switch to turn the circuit on and off. MTK-1001, 2:9-20; MTK-1003, ¶66.

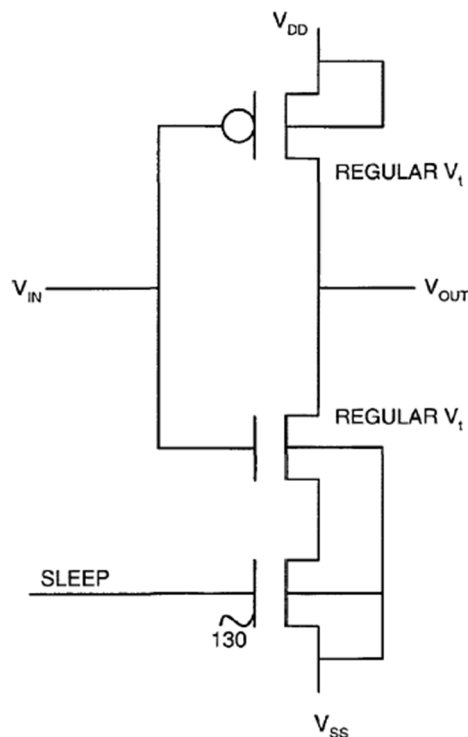
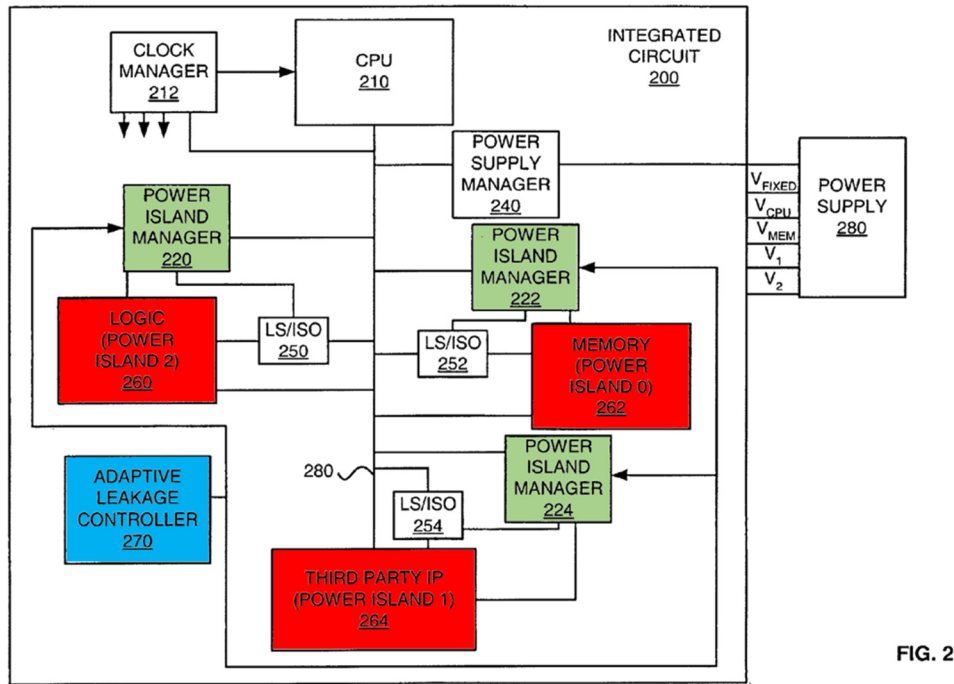


FIG. 1
PRIOR ART

MTK-1001, FIG. 1.

Another common solution is to divide the circuits into distinct power islands whose power consumptions can be controlled independently. MTK-1001, 3:49-55, 3:65-4:10; MTK-1003, ¶67.

The '077 Patent discloses a technique for reducing power consumption using sleep transistors and power islands with other functional blocks as shown in Figure 2. MTK-1001, 3:49-4:27; MTK-1003, ¶¶68.²



MTK-1001, FIG. 2 (annotated)³

² The '077 Patent discloses techniques for retaining data while in a “sleep” state. Because the Challenged Claims are not directed to those features, Petitioner does not discuss those techniques.

³ Annotations and color added unless otherwise noted.

The power islands (red) have associated low leakage circuitry such as sleep transistors. MTK-1001, 3:49-55, 3:65-4:10; MTK-1003, ¶69. Each power island connects to a power island manager (green) that provides control signals to the power island to control its power consumption. MTK-1001, 3:49-55, 4:11-20; MTK-1003, ¶70. The technique uses an adaptive leakage controller (blue) that provides control signals to the power island managers. MTK-1001, 4:21-39; MTK-1003, ¶71. The voltages to the power islands are optimized to reduce leakage currents while in sleep mode, thereby reducing overall power consumption. MTK-1001, 4:21-5:7; MTK-1003, ¶71.

B. Summary of the Prosecution History

U.S. Patent Application No. 13/569,613, which resulted in the '077 Patent, was filed on August 8, 2012, with a series of priority claims dating back to a priority filing date of February 19, 2004. MTK-1002, 98-100. Following a preliminary amendment to add new claims, the claims were allowed without rejection in a first action on January 24, 2014. *Id.*, 84-88, 157-164; MTK-1003, ¶73.

C. Level of Ordinary Skill in the Art

A person of ordinary skill in the art (“POSITA”) would have had at least a bachelor of science degree in electrical or computer engineering, computer science, or a related field, and at least two years of experience in the research, design,

development, or testing of electronic circuits or components, or software for controlling electronic circuits or components, or equivalent, with additional education substituting for experience and vice-versa. MTK-1003, ¶24.

D. Claim Construction

Claim terms generally should be given their ordinary and customary meaning according to the *Phillips* standard. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. §42.100. For purposes of this proceeding only, Petitioner submits that no claim terms require a formal construction for addressing the Grounds in this Petition. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011). Petitioner reserves the right to respond to constructions offered/adopted by the Patent Owner or Board. Petitioner does not concede that each challenged claim satisfies all statutory requirements, including §112, or waive any arguments concerning grounds that can only be raised in district court.

III. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. GROUND 1A—CLAIMS 1-18 ARE OBVIOUS OVER TAKAHASHI

1. Overview of Takahashi

Takahashi discloses systems and methods for “suppressing the leakage current in an integrated circuit.” MTK-1004, Title; MTK-1003, ¶¶77-78.

Takahashi describes an “embodiment of a semiconductor integrated circuit” in Figures 1-5. MTK-1004, [0047]-[0053]; MTK-1003, ¶79. The “device 200”

includes a “logic circuit 10 having a CMOS structure, switching circuit 20 for supplying an operating current to logic circuit 10, voltage regulator 40 capable of supplying variable and multiple voltages, and control circuit 30 for controlling voltage regulator 40.” MTK-1004, [0048].

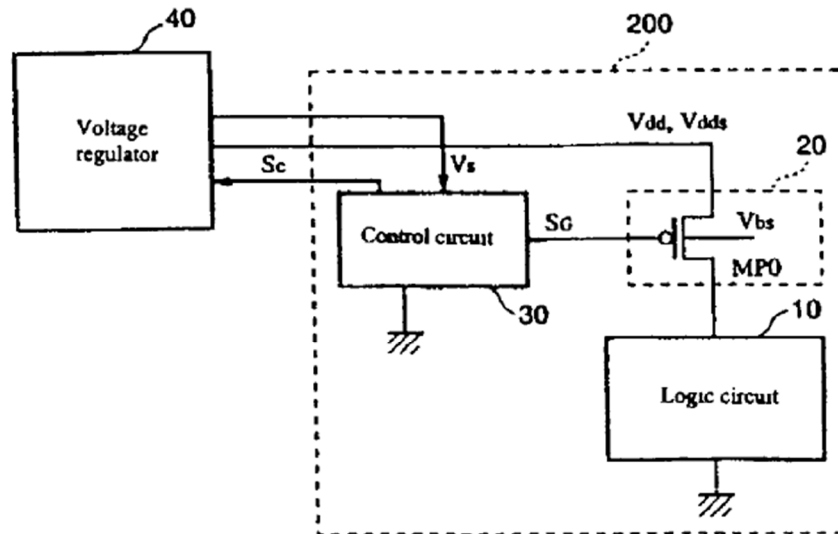


FIG. 1

MTK-1004, FIG. 1

“Switching circuit 20 supplies an operating current to logic circuit 10 during operation and suppresses the leakage current of the low threshold voltage transistor of logic circuit 10 during standby.” MTK-1004, [0052]. “Control signal S_G of different levels is applied to the gate of transistor MP0 during operation and during standby” such that “[t]ransistor MP0 is turned on or off according to the level of said control signal S_G .” MTK-1004, [0053]. MTK-1003, ¶81. “, [D]ifferent levels

are applied during operation and during standby, respectively, for the source voltage at the source of transistor MP0.” MTK-1004, [0053]; MTK-1003, ¶81. Specifically, “source voltages V_{dd} and V_{dds} ” are set to a “nominal operating voltage” while the logic circuit 10 is active and to a lower voltage while in “standby (Sleep mode).” MTK-1004, [0054], [0110]; MTK-1003, ¶81. Lowering the “source voltages” during standby places the “transistor MP0” into a “super cut-off status” that reduces leakage current and therefore power consumption during standby. *Id.*

A related embodiment shown in Figures 11-17 adds a “fusing circuit 202” to the “device 200” that is programmed with “control data DAT.” MTK-1004, [0045], [0097]-[0117]; MTK-1003, ¶82. The control data DAT is “based on the process requirements of device 200 during operation (Active mode) and during standby (Sleep mode)” such that “voltage regulator 100 generates source voltages V_{dd1} , V_{dd2} , and V_{dd3} using optimum values ... according to control data DAT and control signal S_C indicating the operating status of device 200.” MTK-1004, [0110], [0117]; MTK-1003, ¶83. By changing the source voltages based on the “process requirements” of the transistors in the device, “the effect of variations in the production process can be reduced.” MTK-1004, [0117]; MTK-1003, ¶83. The operation of “device 200” in the embodiment of Figures 11-17 otherwise remains the same as in Figures 1-5. MTK-1003, ¶83.

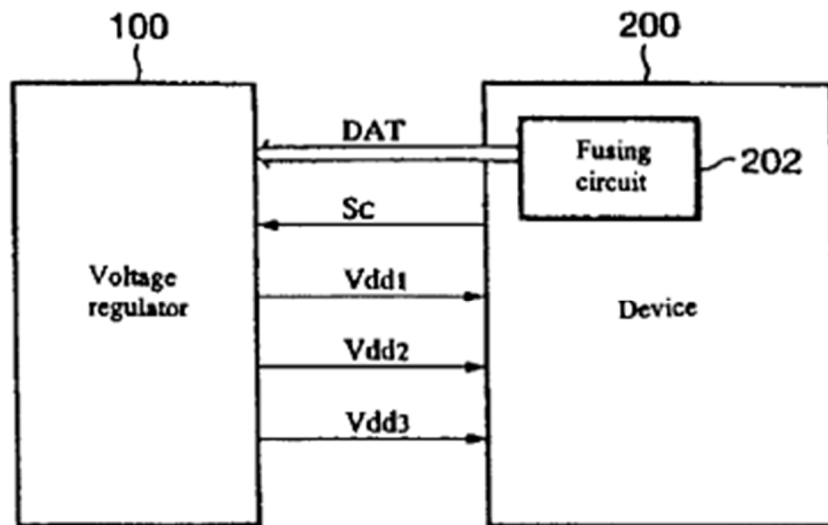


FIG. 11

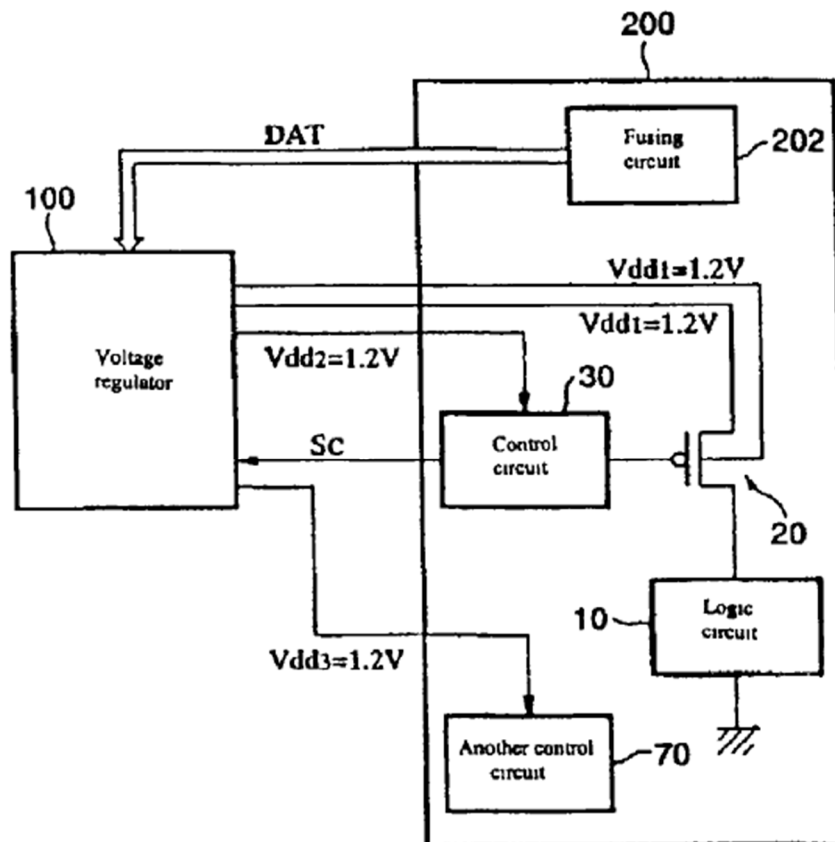


FIG. 16

MTK-1004, FIGS. 11, 16

2. Claim 1

(a) Element 1[p]

Takahashi discloses methods carried out in a “semiconductor integrated circuit.” . MTK-1004, Abstract, FIGS. 1-5, 11-17, [0001], [0047], [0097]; MTK-1003, ¶¶86-87. Takahashi discloses a “logic circuit 10 having a CMOS structure” that “is a functional circuit for performing a logic operation.” MTK-1004, [0045], [0048], [0078]. The “logic circuit 10” can be “a CMOS inverter,” “an AND circuit, a NAND circuit, or an OR circuit,” or “may consist of other kinds of logic circuits.” *Id.*, [0050]. A POSITA would have understood and found obvious that “logic circuit 10” is a power island. MTK-1003, ¶¶88-89. The ’077 patent describes a power island as any “section, delineation, partition, or division of an integrated circuit where power consumption is controlled within the section, delineation, partition, or division.” MTK-1001, 3:65-4:1. Here, power consumption within the “logic circuit 10” is controlled by the “switching circuit 20” that “supplies an operating current to logic circuit 10 during operation and suppresses the leakage current of the ... logic circuit 10 during standby.” *Id.*, [0052]; MTK-1003, ¶¶88-89.

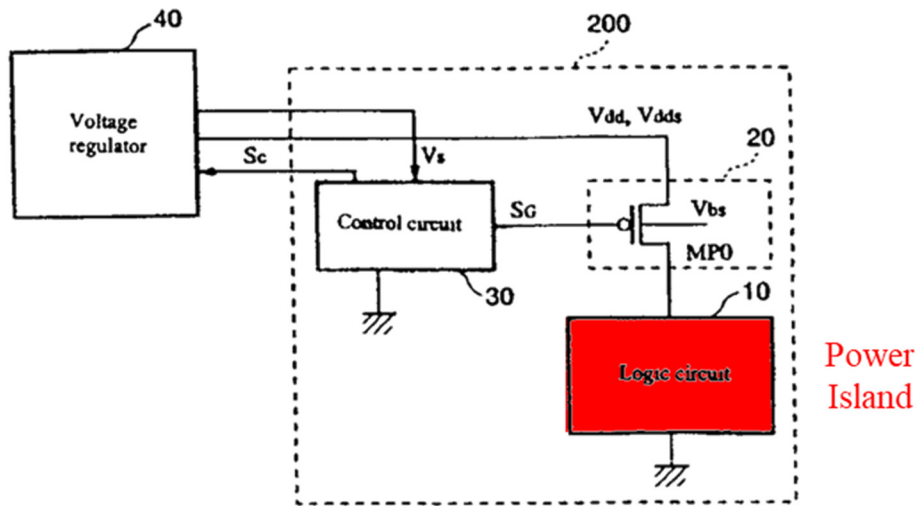


FIG. 1

MTK-1004, FIG. 1

The “device 200” of Figures 11-17 includes “another control circuit 70” for “Wake up logic.” MTK-1004, [0110]-[0116], FIGS. 14-17; MTK-1003, ¶¶90-91. A POSITA would have understood “control circuit 70” is another power island because power consumption within the other “control circuit 70” is controlled by the separate “source voltage V_{dd3} ” that varies based on whether it is in an operational or standby state. *Id.*; see also MTK-1001, 3:65-4:1.

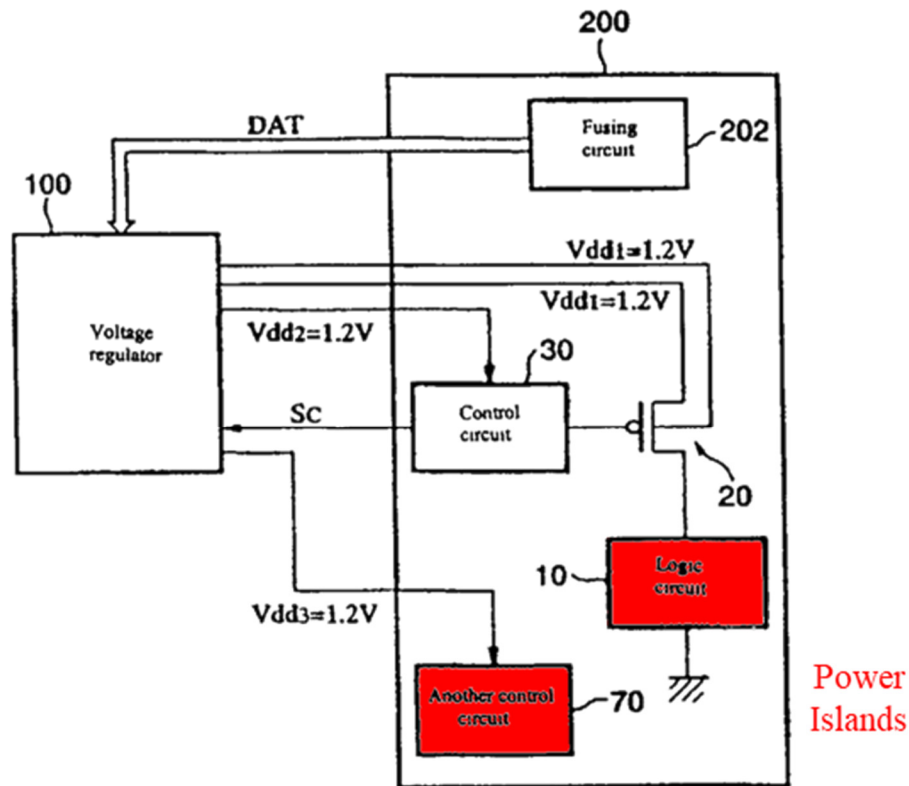


FIG. 16

MTK-1004, FIG 16

Thus, a POSITA would have understood that Takahashi's "device 200" includes multiple power islands, including the "logic circuit 10" and "control circuit 70."

MTK-1003, ¶¶90-92.

A POSITA also would have found it obvious for Takahashi's integrated circuit to include multiple power islands. The embodiments of Figures 1-5 and 11-17 disclose controlling the power consumption of individual circuit blocks such as "logic circuit 10" and "control circuit 70." A POSITA also would have found it obvious for these embodiments to include additional power islands. MTK-1003,

¶92. Figure 10 depicts a related embodiment in which the integrated circuit includes a “logic circuit 230” and includes “[m]emories 210, 220, 270, and 280, ... microprocessor core 240, DSP core 250, and peripheral circuit 260.” MTK-1004, [0089]. Like the power islands of figures 1-5 and 11-17 whose power consumption is controlled by the “switching circuit 20 ... with pMOS transistor MP0,” each of these functional circuits 210-280 is a power island whose power consumption is controlled by the “switching circuit ... with pMOS transistors 310, 320, ... , and 380.” *Id.*, [0090]; MTK-1003, ¶¶92-93. A POSITA would have found it obvious to incorporate such additional power islands into the embodiments of Figures 1-5 and 11-17 to provide additional functionality (*e.g.*, memory) and control power consumption in additional power islands using the “voltage regulator 10” and additional “switching circuits.” MTK-1003, ¶¶92-95.

Takahashi discloses a “voltage regulator” that “controls the level of voltage to be supplied to device 200.” MTK-1004, [0098]. A POSITA would have understood and found obvious that Takahashi’s “voltage regulator” is a power manager because it controls power within the power islands, *e.g.*, the “logic circuit 10” and “control circuit 70.” MTK-1003, ¶¶96-98.

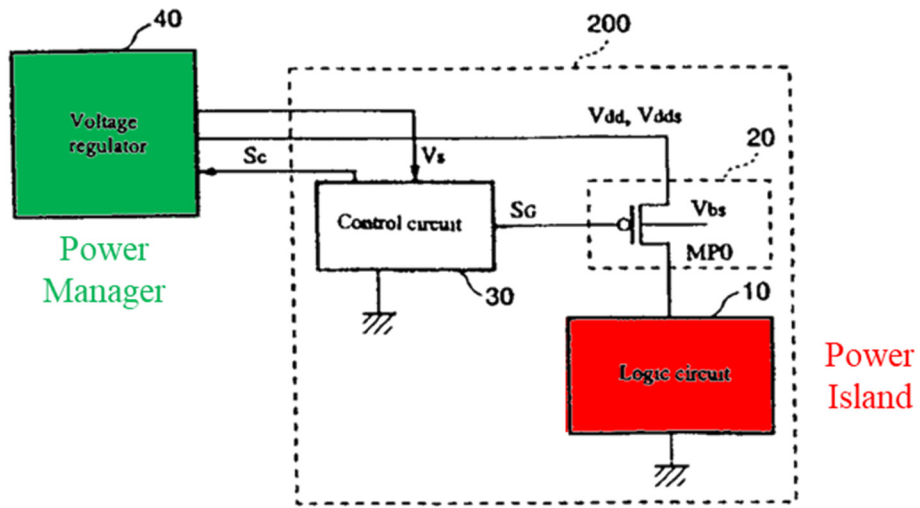


FIG. 1

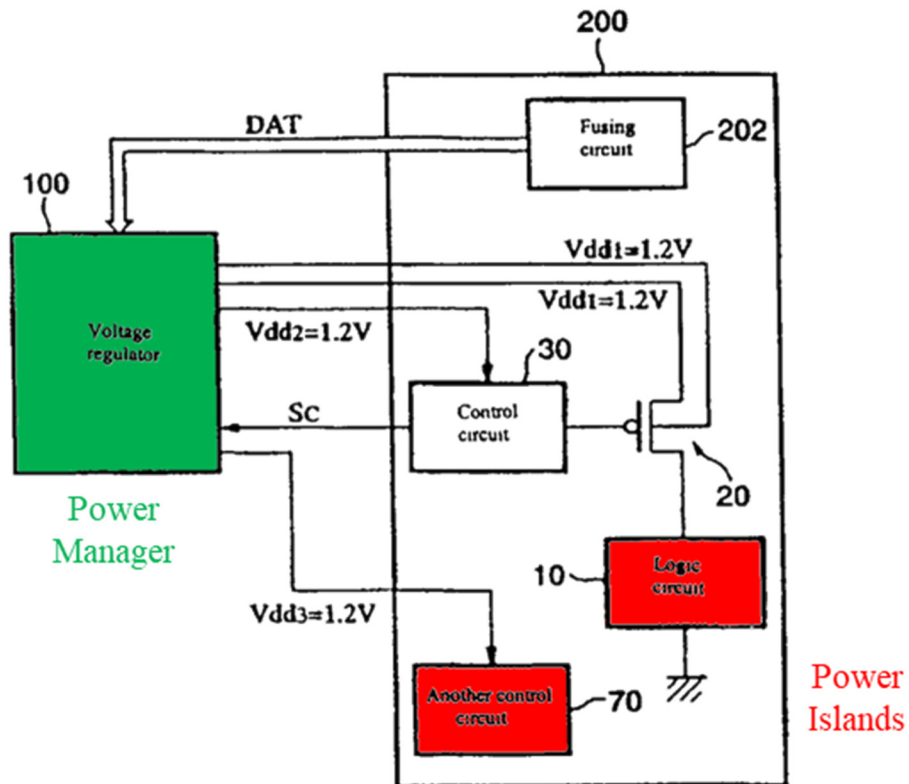


FIG. 16

MTK-1004, FIGS. 1, 16

In “Active mode,” the “voltage regulator” provides an “operating voltage” to “logic circuit 10” and “control circuit 70.” *Id.*, [0110]-[0117], FIGS. 14-17.

During “Sleep mode,” the “voltage regulator” lowers the voltage signals to place “logic circuit 10” and “control circuit 70” into a low-power standby status. *Id.*

Thus, as in the '077 Patent, the outputs of the “voltage regulator” “control power within the power island[s]” by “modify[ing] the voltage within the power island.”

MTK-1001, 4:11-14; MTK-1003, ¶¶99-100.

Active Mode	Bit Bit Bit			Vdd1	Vdd2	Vdd3	Process requirement
	2	1	0	SW Tr Source (TVDD)	SW Tr Gate	Wake up logic	
Fuse prog-0	0	0	0	1.2V	1.2V	1.20V	Weak
Fuse prog-1	0	0	1	1.15V	1.15V	1.15V	NTPW,NWPT
Fuse prog-2	0	1	0	1.05V	1.05V	1.05V	TYPIC,NSPW,NWPS
Fuse prog-3	0	1	1	0.95V	0.95V	0.95V	NSPT,NTPS
Fuse prog-4	1	0	0	0.85V	0.85V	0.85V	Strong

FIG. 14

Sleep Mode	Bit Bit Bit			Vdd1	Vdd2	Vdd3	Process requirement
	2	1	0	SW Tr Source (TVDD)	SW Tr Gate	Wake up logic	
Fuse prog-0	0	0	0	0.7V	1.0V	0.7V	Weak
Fuse prog-1	0	0	1	0.7V	1.0V	0.7V	NTPW,NWPT
Fuse prog-2	0	1	0	0.7V	1.0V	0.7V	TYPIC,NSPW,NWPS
Fuse prog-3	0	1	1	0.7V	1.0V	0.7V	NSPT,NTPS
Fuse prog-4	1	0	0	0.7V	1.0V	0.7V	Strong

FIG. 15

MTK-1004, FIGS. 14-15.

Takahashi also discloses a “control circuit 30” that is an adaptive leakage controller⁴ for controlling the “voltage regulator.” MTK-1004, [0048]; MTK-1003, ¶¶101-103. “[C]ontrol circuit 30 ... generates control signal S_c as the operating status of device 200 changes and outputs it into voltage regulator 100,” such that it “generates source voltages V_{dd1} , V_{dd2} , and V_{dd3} using optimum values under the respective preset conditions according to control data DAT and control signal S_c indicating the operating status of device 200, and outputs them into device 200.” MTK-1004, [0116]-[0117].

⁴ Petitioner submits that “adaptive leakage controller” does not need to be construed for the purpose of this petition. The ’077 patent describes, and a POSITA would understand consistent with that disclosure, that the “adaptive leakage controller” is purposed to adapt an amount of leakage current by providing “optimum voltages to be applied to sleep transistors in the power islands.” MTK-1001, 4:21-27 (citing U.S. patent application Ser. No. 10/996,739 as describing it in detail). The petition’s references’ disclosures, in light of a POSITA’s knowledge, are consistent with the ’077 patent’s descriptions and render this limitation obvious as described herein. *See* MTK-1003 ¶¶71-72, 101-114, 275-290.

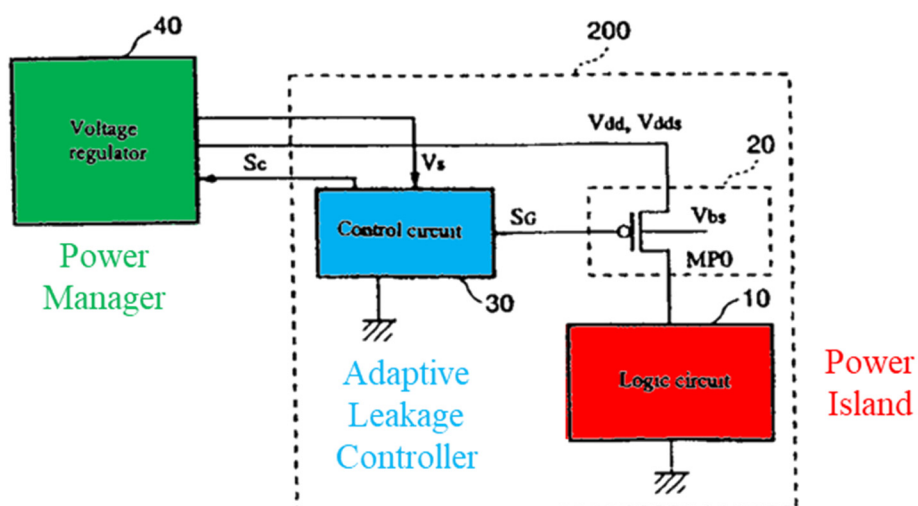


FIG. 1

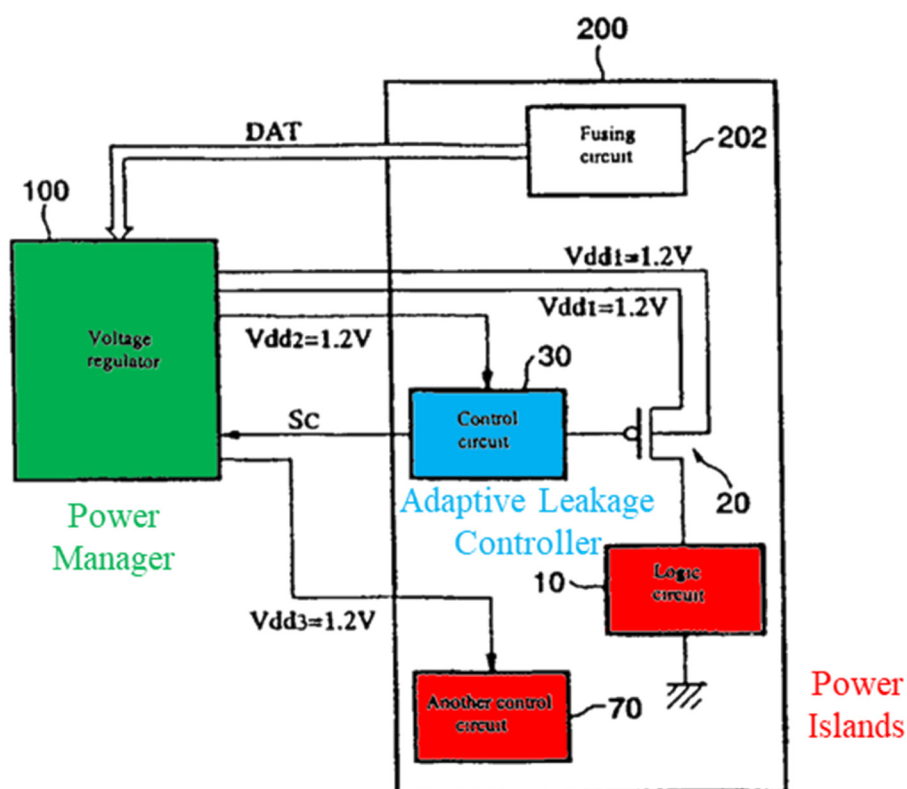


FIG. 16

MTK-1004, FIGS. 1, 16

By optimizing the source voltages, “the switching circuit can be turned on during operation to supply driving current to the logic circuit, and ... can be turned off to suppress the occurrence of leakage current in low threshold voltage transistors in the logic circuit” during standby. *Id.*, [0117]-[0118] (the “switching circuit” is put into a “super cut-off status” by applying “a voltage equal to or higher than the source voltage ... to the gate of the pMOS transistor” and “a bulk bias voltage with the same level as that of the source voltage or a higher level ... to the channel region of the transistor in order to suppress the current to the switching transistor during standby”); MTK-1003, ¶103. Thus, a POSITA would have understood and found obvious that Takahashi’s “control circuit 30” is an adaptive leakage controller that provides control signals for optimizing the voltages applied to the “switching circuit 20” and power islands of the “device 200.” MTK-1001, 4:21-23; MTK-1003, ¶¶101-109.⁵

⁵ To the extent the “adaptive leakage controller” must provide control signals to compensate for process and temperature variation to provide an optimum voltage to sleep transistors, Takahashi renders obvious those features. Takahashi discloses a “fusing circuit 202” that provides “control data DAT” indicating the “effect of variations in the production process” on the “driving capability” of the transistors

Petitioner notes that “power island” and “power manager” have been construed in prior litigations involving a patent describing similar subject matter, U.S. Patent No. 7,051,306. *See* MTK-1025 43-44 (construing “power island” as “section of an integrated circuit where power consumption is controlled by independently varying its operating voltage and its frequency of operation”); 44-46 (construing “power manager” as “circuitry, device, or system configured to determine a target power level of a power island, determine an action to change the target power level, and perform an action to change the consumption power level to the target power level”); MTK-1026 28-29 (clarifying meaning of prior construction of “power island” as “a section of an integrated circuit where power consumption is controlled by independently varying its operating voltage or its frequency of operation (or both)”), 29-34 (construing “power manager” as “any system, circuitry, or device configured to control power”). For purposes of this Petition, Petitioner submits that no construction is necessary because plain and ordinary meaning suffices. And while the prior constructions involved a different

in “device 200.” MTK-1004, [0117]; MTK-1003, ¶¶105-108. As explained at Claim 5 below, it would have been obvious to a POSITA for the “control circuit 30” to provide “control data DAT” that accounts for “variations in the production process” as well as for temperature variation. *Id.*

patent and different claims and are not binding on this proceeding, Takahashi's disclosures, in light of a POSITA's knowledge, also render these terms obvious under the prior constructions. *See* MTK-1003, ¶109.

(b) Element 1[a]

Takahashi discloses that the “control circuit 30” (*i.e.*, the adaptive leakage controller) sends an operating status “control signal S_C ” to the “voltage regulator” (*i.e.*, the power manager). The “[v]oltage regulator 100 generates different levels of source voltages during operation and during standby according to ... status control signal S_C and supplies them to device 200.” MTK-1004, [0111]; *see also id.*, [0098], [0112]-[0117], FIG. 1; MTK-1003, ¶¶111-114. For example, in the embodiment of Figures 11-17, “voltage regulator 100” “controls the levels of source voltages V_{dd1} , V_{dd2} , and V_{dd3} supplied to device 200 using predetermined optimum values according to control signal S_C indicating control data DAT and the operating condition of the device.” *Id.*, [0109].

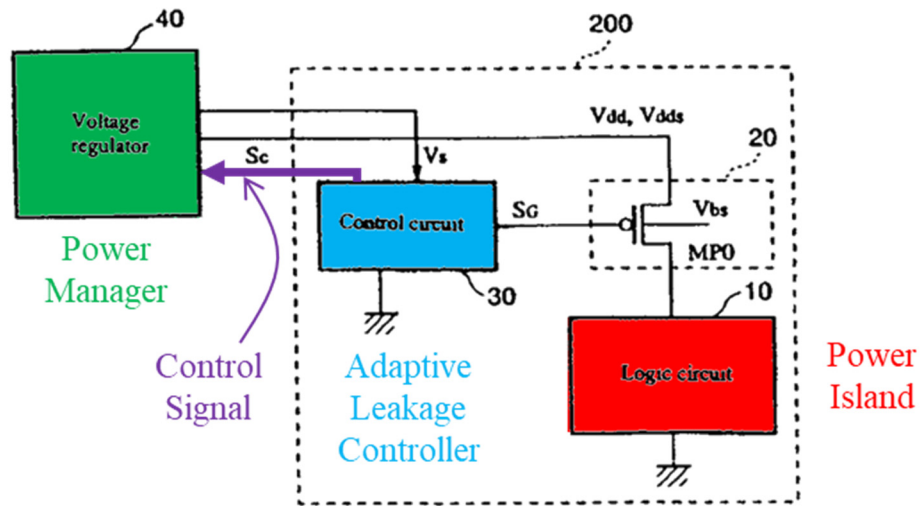


FIG. 1

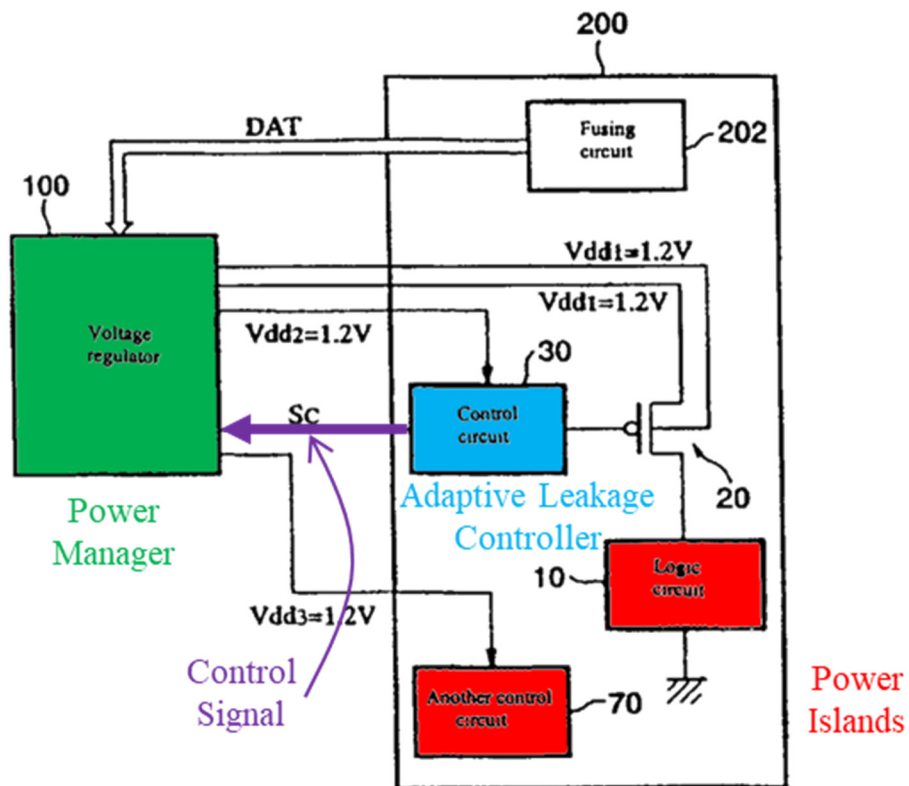


FIG. 16

MTK-1004, FIGS. 1, 16

(c) Element 1[b]

Takahashi's "voltage regulator" generates a variable voltage " V_{dd} " (Figures 1-5) or " V_{dd1} " (Figures 11-17) based on the "control signal S_c " from the "control circuit 30."

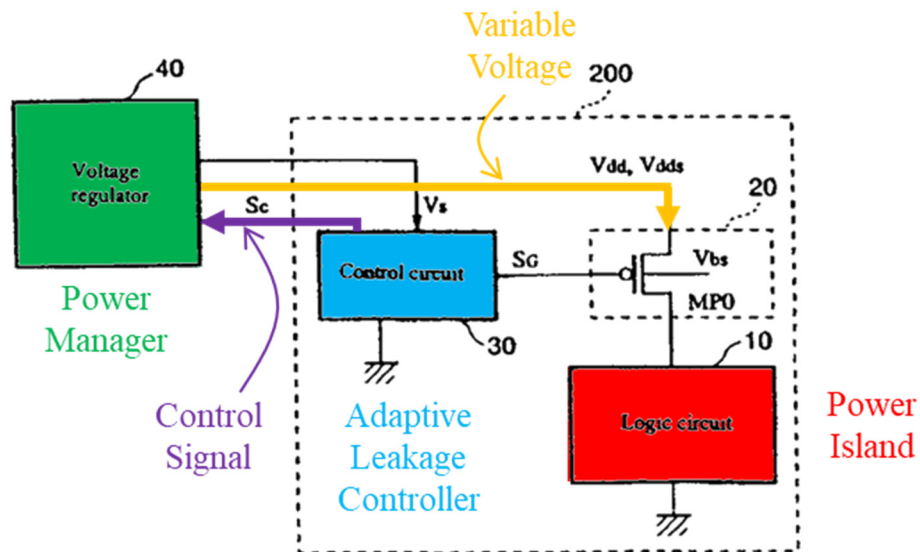


FIG. 1

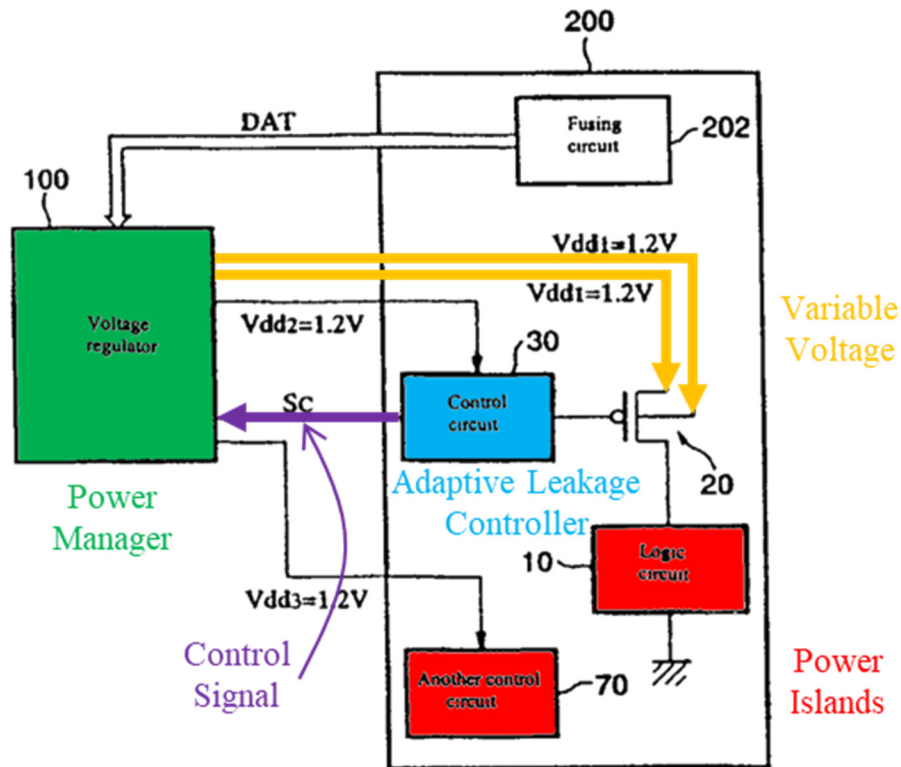


FIG. 16

MTK-1004, FIGS. 1, 16

In the Figures 11-17 embodiment, for example, “multiple different levels of voltages V_{dd1} , V_{dd2} , and V_{dd3} are supplied from voltage regulator 100 to device 200.” MTK-1004, [0098]. Based on “status control signal S_C ,” “source voltage[] V_{dd1} ... during operation [is] 1.2V as shown” in Figure 16 and “ V_{dd1} ... during standby is 0.7V” as shown in Figure 17. MTK-1004, [0109], [0111]-[0115], FIGS. 14-15; MTK-1003, ¶¶116-120.

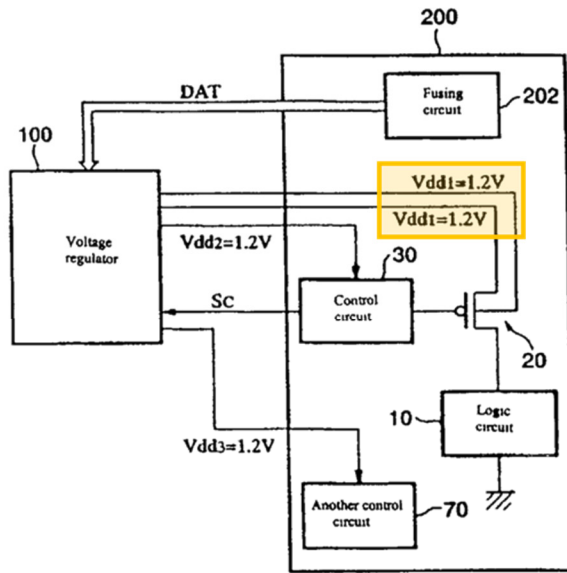


FIG. 16

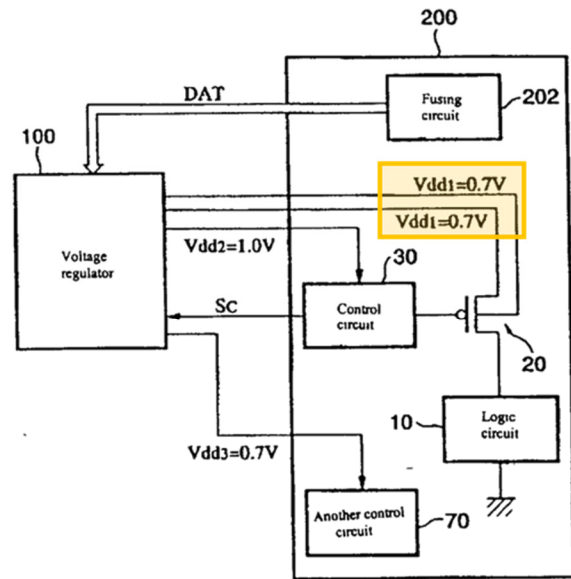


FIG. 17

MTK-1004, FIGS. 16-17

Takahashi's "voltage regulator 100" provides this variable voltage to
"switching circuit 20." MTK-1004, Abstract, [0051]-[0052], [0113]-[0116].⁶

⁶ Takahashi explains that "source voltage V_{dd2} " is provided to "SW Tr Gate," *i.e.*,
the gate of the "transistor MP0" in "switching circuit 20." MTK-1003, ¶120.

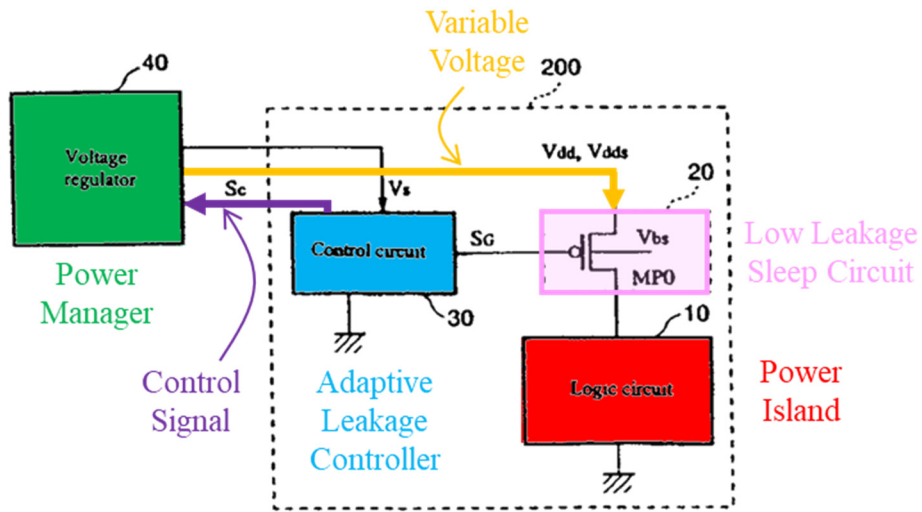


FIG. 1

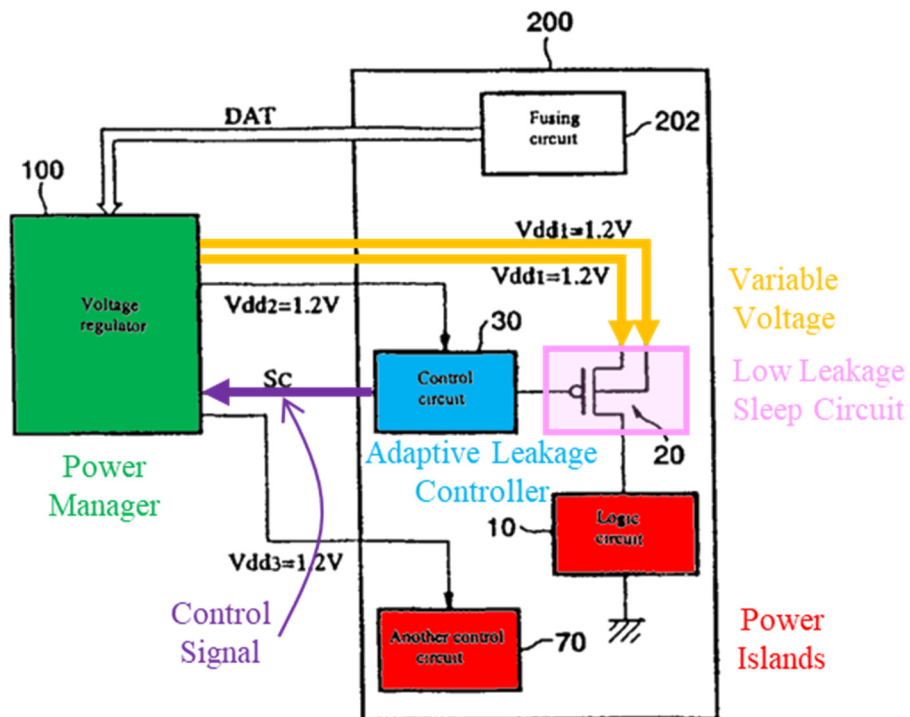


FIG. 16

MTK-1004, FIGS. 1, 16

The “switching circuit 20 is configured with pMOS transistor MP0” that “supplies an operating current to logic circuit 10 during operation and suppresses the leakage current ... of logic circuit 10 during standby.” *Id.*, [0051]-[0053]. Thus, a POSITA would understand that Takahashi’s “switching circuit 20” comprising the “transistor MP0” is a “low leakage sleep circuit”⁷ that reduces leakage during standby. MTK-1003, ¶¶120-122; *see* MTK-1001, Abstract, 2:9-20 (describing a “sleep transistor” that “act[s] as a switch to turn on and off the logic gate”), 2:45-50, 4:21-5:7, 7:12-17.

⁷ Petitioner submits that “low leakage sleep circuit” does not need to be construed for the purpose of this petition. Although “low leakage sleep circuit” does not appear in the specification, the claims of the ’077 patent use “low leakage sleep circuit” in a manner consistent with its description of a “sleep transistor.” For example, the ’077 patent describes that “sleep transistors act as a switch to turn on and off the logic gate” and are configured to “reduce power consumption” of a circuit “in the sleep state” that results in the “circuit hav[ing] low leakage based on the sleep signal” MTK-1001, 2:9-20; 2:45-50. The petition’s references’ disclosures, in light of a POSITA’s knowledge, are consistent with the ’077 patent’s descriptions and render this limitation obvious as described herein. *See* MTK-1003, ¶¶70-72, 116-129, 173-176, 180-184, 292-303, 352-355, 359-365.

A POSITA also would have found it obvious for Takahashi's integrated circuit to including multiple "switching circuits." MTK-1003, ¶¶123. Takahashi's Figure 10 depicts an embodiment with multiple power island "functional circuits" 210-280 whose power consumptions are controlled by "pMOS transistors" 310-380. MTK-1004, [0090]-[0091], [0094]; MTK-1003, ¶123. "These transistors are turned on/off ... to supply a driving current to a prescribed functional circuit when in the on status" and suppress the "occurrence of a leakage current" during standby. *Id.*, [0090]; MTK-1003, ¶123.

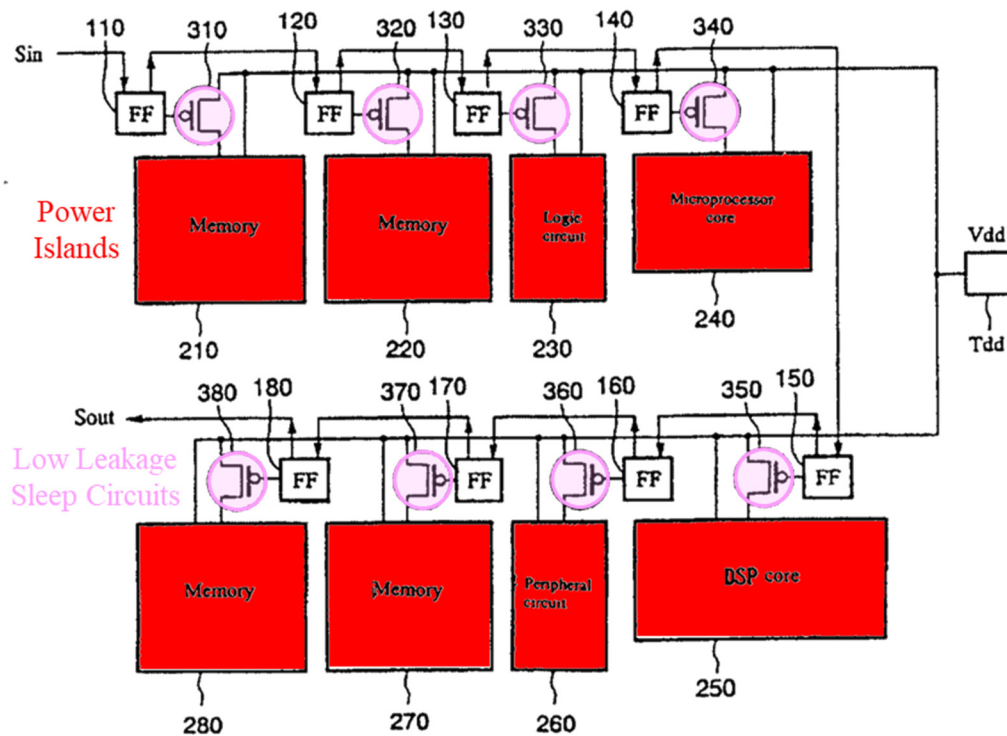


FIG. 10

MTK-1004, FIG. 10

A POSITA would have found it obvious to apply this structure to the embodiments in Figures 1-5 and 11-17. MTK-1003, ¶124. A POSITA would have understood that a device can include more than one “logic circuit 10” and been motivated to provide a “switching circuit 20” for each to obtain the same power savings described for Figure 10. MTK-1003, ¶125.

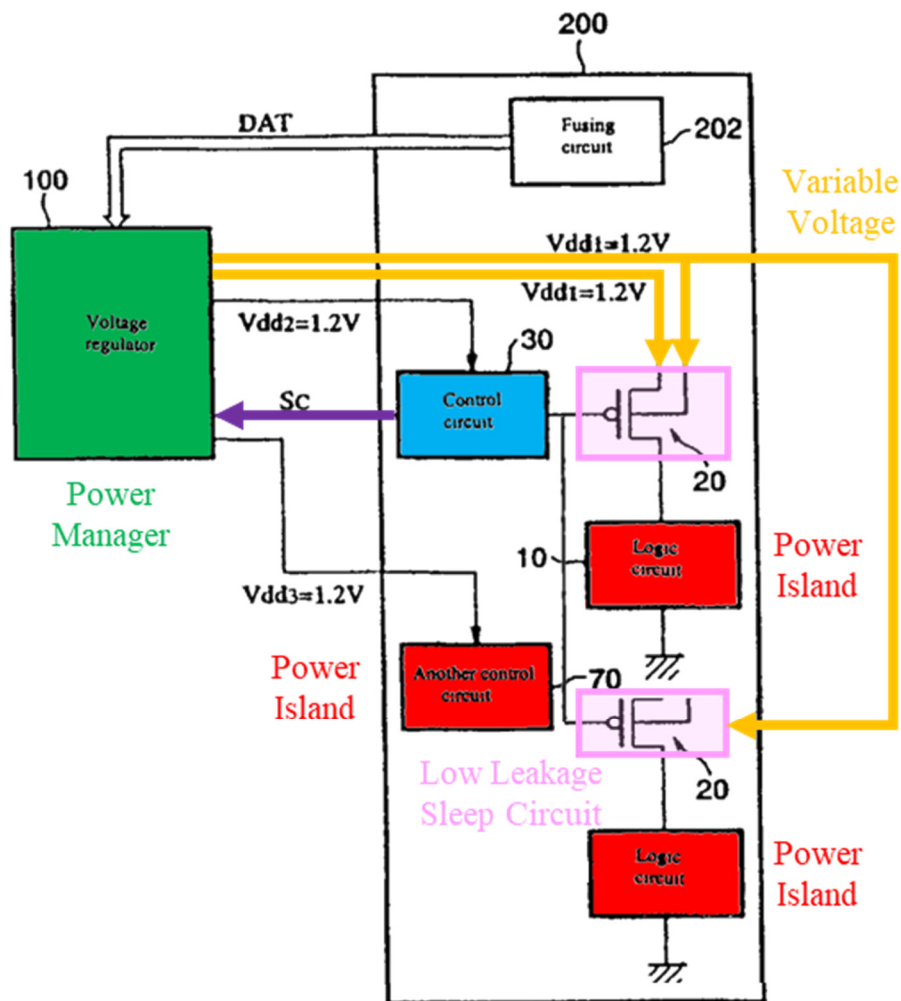


FIG. 16

EX-1004, FIG. 16 (as modified)

Similarly, a POSITA would have found it obvious to include another “switching circuit 20” to further reduce power consumption of the “Wake up logic” in “control circuit 70” during standby. MTK-1003, ¶126.

As such, Takahashi’s integrated circuit employs the “voltage regulator” to dynamically change the power consumptions of the power islands, including “logic circuit 10” and “control circuit 70.” MTK-1003, ¶126. Takahashi’s “voltage regulator” varies source voltage “ V_{dd1} ” to power “logic circuit 10” during operation and reduce power consumption due to leakage current during standby. MTK-1004, [0112]-[0116]; MTK-1003, ¶126-128. “[V]oltage regulator 100” similarly varies “source voltage V_{dd3} ” to the other “control circuit 70” to power the “Wake up logic” during operation and reduce its power consumption during standby. MTK-1004, [0110]-[0117], FIGS.14-17; MTK-1003, ¶¶126-128.

3. Claim 2

As discussed at element 1[b], Takahashi’s “logic circuit 10” and “control circuit 70” are in “standby (Sleep mode)” or “operation (Active mode)” at different times to reduce power consumption when not used. MTK-1004, [0110]; MTK-1003, ¶¶130-132. Takahashi explains that “[t]ransistor MP0 [of the switching circuit 20] is turned on or off” to supply “a driving current ... to logic circuit 10” or “cut off” the driving current such that “leakage current at logic circuit 10 is suppressed.” *Id.*, [0052]-[0053]; *see also id.*, [0098], [0112]-[0116] (addressing

Figures 11-17). Similarly, Takahashi discloses providing “control circuit 70” with a varying “source voltage V_{dd3} ” to place “Wake up logic” into a standby or operational state at different times. MTK-1004, [0098]-[0100], [0110]-[0117].

A POSITA also would have found it obvious to selectively put the “logic circuit 10” or “control circuit 70” power islands into standby or operational states at different times from other power islands as done in the embodiment of Takahashi’s Figure 10.⁸ MTK-1004, [0087]-[0095] (“[I]n FIG. 10, supply of driving current to the respective functional circuits can be controlled individually by controlling the on/off status of the respective transistors constituting the switching circuit.”); MTK-1003, ¶133. A POSITA would have been motivated to do so because selectively placing individual power islands into “standby (Sleep mode)” or “operation (Active mode)” would further reduce power consumption of the “device 200.” MTK-1003, ¶134. A POSITA would have understood that powering down unused power islands while others are operational would reduce the overall power consumption of the “device 200.” MTK-1003, ¶¶133-135. A

⁸ Petitioner does not concede that Claim 2 requires putting at least one power island to sleep and taking it out of sleep at different times *from other power islands*. MTK-1003, ¶132-133.

POSITA would have known how to implement such a feature, as shown in Figure 10 of Takahashi, in the integrated circuits of Figures 1-5 and 11-17. *Id.*

4. Claim 3

Takahashi discloses that the “voltage regulator 100” uses the inputs “control data DAT” and “control signal Sc” to determine optimum “source voltages” for putting power islands into standby and operational states. MTK-1004, [0098]-[0117]; MTK-1003, ¶¶137-143.

The “control data DAT” is set “according to the driving capabilities of the pMOS transistor and the nMOS transistor constituting device 200.” MTK-1004, [0100]. Figure 13 shows that the “levels of source voltage V_{dd} ” vary between 1.2V and 0.85V depending on the driving strength of the pMOS and nMOS transistors. MTK-1004, [0107]-[0108].

P-MOS	NWPS Vdd=1.05V	NTPS Vdd=0.95V	Strong Vdd=0.85V	Strong corner
	NWPT Vdd=1.15V	Typical Vdd=1.05V	NSPT Vdd=0.95V	
	Weak Vdd=1.2V	NTPW Vdd=1.15V	NSPW Vdd=1.05V	
Weak corner		N-MOS		

FIG. 13

MTK-1004, FIG. 13

In Figures 14-15, “[v]oltage regulator 100 generates different levels of source voltages during operation and during standby according to said control data DAT and status control signal S_C” to put the power islands into standby and operational states. MTK-1004, [0110]-[0111].

<u>Active</u> Mode	Bit2 2	Bit1 1	Bit0 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0	0	0	1.2V	1.2V	1.20V	Weak
Fuse prog-1	0	0	1	1.15V	1.15V	1.15V	NTPW,NWPT
Fuse prog-2	0	1	0	1.05V	1.05V	1.05V	TYPC,NSPW,NWPS
Fuse prog-3	0	1	1	0.95V	0.95V	0.95V	NSPT,NTPS
Fuse prog-4	1	0	0	0.85V	0.85V	0.85V	Strong

FIG. 14

<u>Sleep</u> Mode	Bit2 2	Bit1 1	Bit0 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0	0	0	0.7V	1.0V	0.7V	Weak
Fuse prog-1	0	0	1	0.7V	1.0V	0.7V	NTPW,NWPT
Fuse prog-2	0	1	0	0.7V	1.0V	0.7V	TYPC,NSPW,NWPS
Fuse prog-3	0	1	1	0.7V	1.0V	0.7V	NSPT,NTPS
Fuse prog-4	1	0	0	0.7V	1.0V	0.7V	Strong

FIG. 15

MTK-1004, FIGS. 14-15

A POSITA would have therefore understood and found obvious that Takahashi’s “voltage regulator” employs a state machine with the output states shown in Figures 14-15 that controls the power islands’ state based on “control data DAT” and “control signal S_C.” MTK-1003, ¶138; MTK-1001, 6:19-21; MTK-1008

(defining “state machine” as a “circuit containing several different states reachable from each other, with state changes happening synchronously”); MTK-1009.

5. Claim 4

Takahashi discloses that the variable “source voltage” provided by the “voltage regulator” is set to “optimum values under the respective present conditions according to control data DAT and control signal SC indicating the operating status of device 200.” MTK-1004, [0117]; *see also id.*, [0099]-[0100], [0107], [0109]-[0111], [0123], FIGS. 13-15. By optimizing the variable “source voltage,” “the effect of variations in the production process can be reduced” and the “occurrence of leakage current is suppressed.” *Id.*, Abstract, [0109], [0116]-[0118], [0123]; MTK-1003, ¶¶145-147.

6. Claim 5

As discussed at Claim 4, Takahashi discloses that the “source voltage” is optimized based on process variation so that “the effect of variations in the production process can be reduced.” MTK-1004, [0117]; *see also* Claim 4; MTK-1004, [0099]-[0100], [0107], [0109]-[0111], [0123], FIGS. 13-17.

It was also well-known at the time of the '077 Patent that transistor performance depends on both process and temperature variation. MTK-1003, 149-51; *see also, e.g.*, MTK-1010, 1:37-2:14 (“[I]t is known that varying supply voltage ... can improve performance by eliminating unexpected variability in the

supply voltage, and by accounting for process and operating temperature variations.”); MTK-1011, 12:18-21; MTK-1012, 2:34-43, FIG. 2; MTK-1013, 1:19-30; MTK-1014, 4:14-23. Thus, it would have been obvious to a POSITA to optimize the “source voltage” based on temperature variation and process variation to further improve performance of the pMOS and nMOS transistors in the “switching circuit 20” and “logic circuit 10” and further reduce power consumption due to “the occurrence of leakage current” in the “device 200.” MTK-1004, Abstract; MTK-1003, ¶¶151-153.

A POSITA would have been readily capable of implementing such a change with a reasonable expectation of success. MTK-1003, ¶¶151-153. A POSITA would have known how to incorporate a temperature sensor in Takahashi’s integrated circuit such that the “voltage regulator” would optimize the “source voltage” output based on temperature variation in addition to the process variation indicated by “control data DAT” and “status control signal S_C.” MTK-1004, [0098]-[0117], FIGS. 11-17; MTK-1003, ¶¶151-153.

7. Claim 6

Takahashi’s “voltage regulator” provides an optimum “source voltage” to “switching circuit 20” during “standby (Sleep mode).” MTK-1004, [0110], FIGS. 15, 17; MTK-1003, ¶¶155-59; *see* Claim 4.

Sleep Mode	Bit 2	Bit 1	Bit 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0	0	0	0.7V	1.0V	0.7V	Weak
Fuse prog-1	0	0	1	0.7V	1.0V	0.7V	NTPW,NWPT
Fuse prog-2	0	1	0	0.7V	1.0V	0.7V	TYPC,NSPW,NWPS
Fuse prog-3	0	1	1	0.7V	1.0V	0.7V	NSPT,NTPS
Fuse prog-4	1	0	0	0.7V	1.0V	0.7V	Strong

FIG. 15

MTK-1004, FIG. 15

As explained at Claim 4, “[v]oltage regulator 100 generates different levels of source voltages ... during standby” so that “switching circuit 20 is in the super cut-off status during standby, and the occurrence of leakage current at logic circuit 10 is suppressed.” MTK-1004, [0111], [0116]. Thus, a POSITA would understand and find obvious that the “voltage regulator 100” generates an optimum variable voltage using a sleep generator. MTK-1003, ¶¶154-59; *see* MTK-1001, 5:8-67, FIGS. 3-4.

8. Claim 7

As explained at elements 1[a]-[b], “control signal Sc” is binary, indicating either an operational or standby status of the “device 200.” MTK-1004, Abstract, [0098], [0111], [0116]-[0117]; MTK-1003, ¶¶161-62. Similarly, in other embodiments at Figures 6-9, similar “control signals Sc1 and Sc2” are provided to the “voltage switching circuit 50” that is “provided in place of the voltage

regulator.” MTK-1004, [0065]. The “control signals S_{C1} and S_{C2} ” take one of two values—either “the level of source voltage V_{ddN} ” or “ground potential GND.” MTK-1004, [0069]-[0074]. A POSITA would have understood that binary “control signals S_{C1} and S_{C2} ” are digital signals, and similarly would have understood that “control signal S_C ” that likewise takes one of two values also is digital. MTK-1015 (defining “digital signal” as “[a]n electrical signal with two states”); MTK-1016; MTK-1003, ¶¶160-63.

Moreover, the “control data DAT” is a digital signal with a specific “number of bits.” MTK-1004, [0098], [0101], [0104], [0109]-[0111], FIGS. 14-15. A POSITA would have found it obvious to use digital signals for both the “control data DAT” and “control signal S_C ” such that the “voltage regulator” selects the “source voltage” levels based solely on digital inputs rather than a mix of digital and analog inputs. MTK-1003, ¶164.

All electrical signals are either digital or analog. MTK-1003, ¶¶163-165. It would have been obvious to a POSITA for the “control signal S_C ” to be digital as one of only two options. *See Uber Techs., Inc. v. X One, Inc.*, 957 F.3d 1334, 1341 (Fed. Cir. 2020) (finding claims obvious where POSITA would have faced a “simple design choice” between two design options).

9. Claim 8

As explained at element 1[b], “switching circuit 20” is a low leakage sleep circuit connected in series between the “voltage regulator” and the “logic circuit 10” that is a power island to provide or “cut off” a driving current to the “logic circuit 10.” MTK-1004, Abstract, [0052], [0074]; MTK-1003, ¶¶167-69. The “voltage regulator” regulates a system power supply (not shown) to generate “source voltages” (e.g., “ V_{dd} ,” “ V_{ddl} ”) provided to “switching circuit 20.” MTK-1004, [0053], [0098]; MTK-1003, ¶¶167-169.

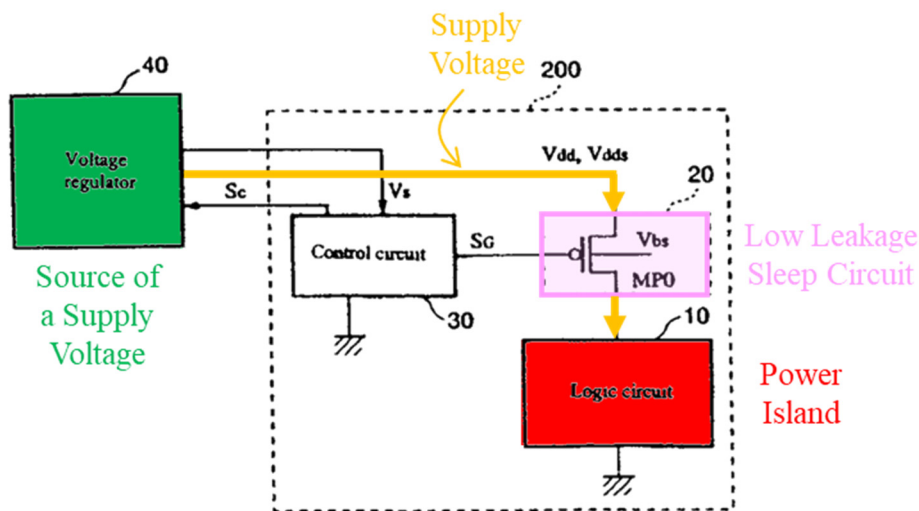


FIG. 1

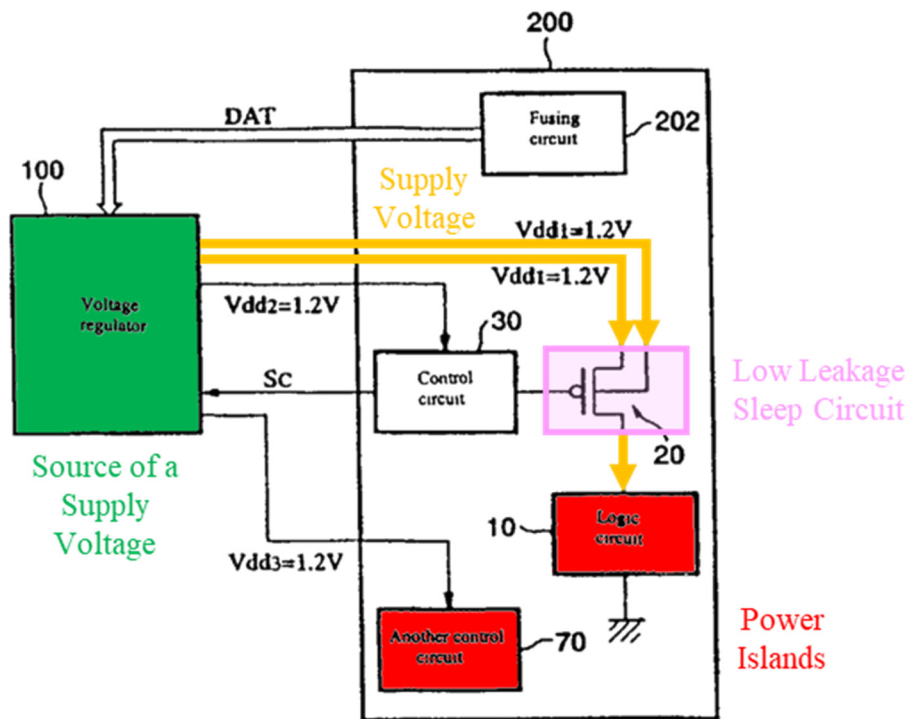


FIG. 16

MTK-1004, FIGS. 1, 16

The “logic circuit 10 [has] a CMOS structure” that includes logic gates such as “a CMOS inverter,” or “other kinds of logic circuits, such as an AND circuit, a NAND circuit, or an OR circuit.” MTK-1004, [0050]. Takahashi also discloses an embodiment in Figure 10 where “switching circuit 20” is connected in series with power islands including “[m]emories 210, 220, 270, and 280, logic circuit 230, microprocessor core 240, DSP core 250, and peripheral circuit 260.” *Id.*, [0089]; MTK-1003, ¶¶170-171.

10. Claim 9

During an operational mode, “transistor MP0” in “switching circuit 20” is “conductive (on) [such that] source voltage Vdd is applied to node N1, and a driving current is supplied to logic circuit 10.” MTK-1004, [0052]; *see also id.*, [0112]-[0116], FIGS. 2-3, 14, 16. During “Sleep mode,” “transistor MP0 is off (off) [and] supply of current to logic circuit 10 is cut off.” *Id.* Thus, Takahashi discloses that “switching circuit 20” modifies the supply voltage provided to “logic circuit 10” from an operational voltage as shown in Figures 14 and 16 to a lower voltage as shown in Figures 15 and 17 during “standby (Sleep mode).” *Id.*, [0110]-[0111]; MTK-1003, ¶¶173-175.

11. Claim 10

(a) Element 10[p]

Supra 1[p] and 1[b]. MTK-1003, ¶177.

(b) Element 10[a]

Supra 1[a]. MTK-1003, ¶178.

(c) Element 10[b]

Supra 1[b]. MTK-1003, ¶179.

(d) Element 10[c]

As explained at element 1[b], a POSITA would have found it obvious to include multiple instances of “switching circuit 20” in Takahashi’s integrated circuit. MTK-1003, ¶¶180-183. Takahashi discloses that “switching circuit 20 ...

suppresses the leakage current of ... logic circuit 10 during standby.” MTK-1004, [0052]; *see also id.*, [0054]-[0059], [0062], [0116], [0118]. In the related embodiment of Figure 10, Takahashi discloses that each of the “pMOS transistors 310, 320, ..., and 380” of the “switching circuit” can be turned off so that the “occurrence of a leakage current in the [respective] functional circuit can be suppressed.” *Id.*, [0090]; *see also id.* [0092]. A POSITA would have understood and found obvious that each “switching circuit 20” in Takahashi’s integrated circuit has an associated leakage reduction for the respective “logic circuit 10” or other power island.

12. Claim 11

Supra Claim 2 and 10[p]-10[c]. MTK-1003, ¶185.

13. Claim 12

Supra Claim 3, 10[p]-10[c], and Claim 11. MTK-1003, ¶186.

14. Claim 13

Supra Claim 4 and 10[p]-10[c]. MTK-1003, ¶187.

15. Claim 14

Supra Claim 5, 10[p]-10[c], and Claim 13. MTK-1003, ¶188.

16. Claim 15

Supra Claim 6, 10[p]-10[c], and Claim 13. MTK-1003, ¶189.

17. Claim 16

Supra Claim 7 and 10[p]-10[c]. MTK-1003, ¶190.

18. Claim 17

Supra Claim 8 and 10[p]-10[c]. MTK-1003, ¶191.

19. Claim 18

Supra Claim 9, 10[p]-10[c], and Claim 17. MTK-1003, ¶192.

**B. GROUND 1B—CLAIMS 3 AND 12 ARE OBVIOUS OVER
TAKAHASHI IN VIEW OF KO**

1. Overview of Ko

Ko “relates generally to digital integrated circuits and, more particularly, to reducing leakage current in power-saving standby modes of digital integrated circuit operation.” MTK-1006, 1:14-17; MTK-1003, ¶¶194-197. Ko’s Figure 1 illustrates a power switching arrangement where “a suitable transistor is provided as a header switch for selectively (in response to the signal UP/DN) connecting and disconnecting the module level power supply VDD to and from the chip level (permanent) power supply VCC.” MTK-1006, 2:63-3:6. A “separate power supply VRETAIN” is used to power “shadow latches” that serve to “retain[] data while power is removed” from the functional circuitry in the “logic block.” MTK-1006, 2:63-3:34; MTK-1003, ¶197.

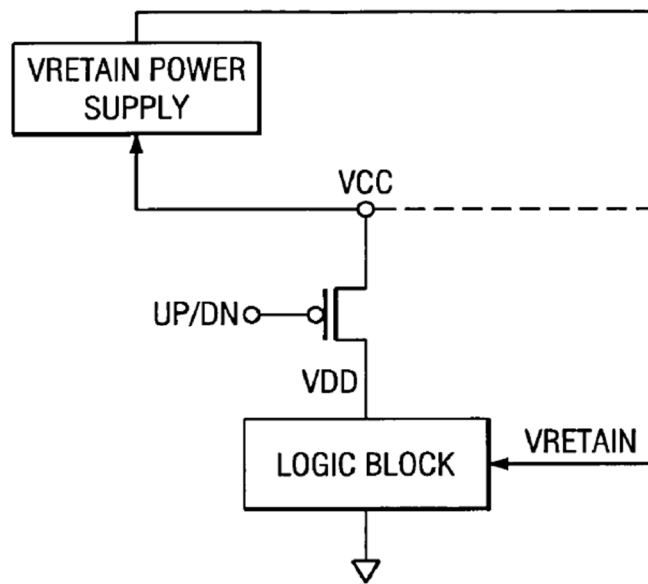


FIG. 1

MTK-1006, FIG. 1

Ko's power switching arrangement is applicable to systems with multiple logic blocks that can be powered-down individually. MTK-1006, 9:51-63, FIG. 11. Figure 4 depicts an exemplary implementation in which a wireless communication apparatus includes header switches and "a plurality of logic modules ... for performing data processing operations." MTK-1006, 7:32-50; MTK-1003, ¶¶198-199. The apparatus "includes a power state controller 45 which, in some embodiments, utilizes state machines to provide appropriate control signals to the header switches and logic modules." MTK-1006, 7:32-50; MTK-1003, ¶¶198-199. "[T]he power state controller provides control signals UP/DN to the respective header switches" to connect and disconnect the logic

modules from the power supply VCC. MTK-1006, 7:32-50; MTK-1003, ¶¶197-200.

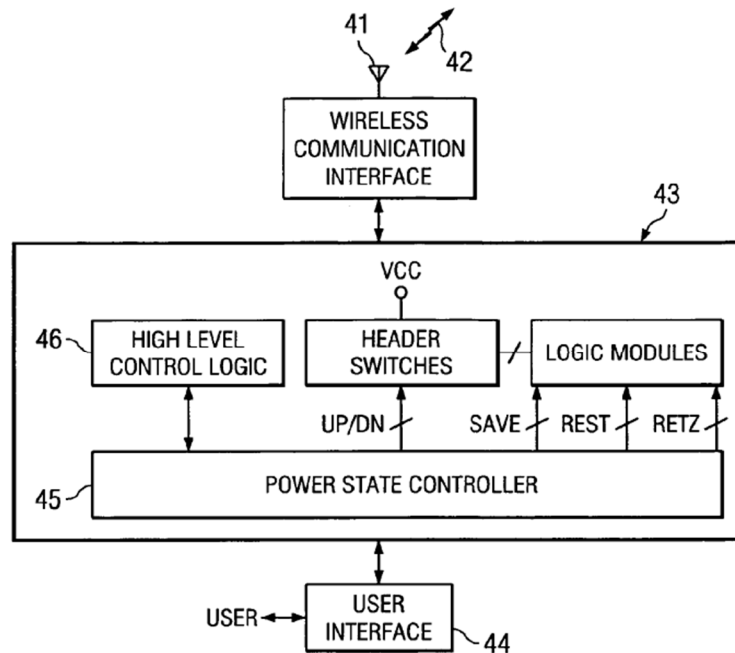


FIG. 4

MTK-1006, FIG. 4

2. Takahashi-Ko Combination

A POSITA would have been motivated to modify Takahashi's integrated circuit to incorporate Ko's teachings with a reasonable expectation of success. MTK-1003, ¶¶202-213. Takahashi and Ko are both assigned to Texas Instruments Inc. and in the same field of endeavor. *Id.* Both relate to reducing power consumption in integrated circuits, including power consumption due to leakage currents during standby. MTK-1004, Title, Abstract, [0001] (describing Field of the Invention as "a semiconductor integrated circuit by which power consumption

can be reduced by suppressing leakage current”), [0002] (discussing application to “mobile communication terminals”); MTK-1006, 1:14-17 (describing Field of the Invention as “reducing leakage current in power-saving standby modes of digital integrated circuit operation”), 3:7-34, 7:20-50 (describing a “wireless communication apparatus”), 9:2-4, 9:42-50; MTK-1003, ¶203. As explained above, the ’077 Patent is in this same field of endeavor. *See* MTK-1001, Title, Abstract, 1:29-39; MTK-1003, ¶203.

Takahashi and Ko also address the same known power consumption problem in the same way. MTK-1003, ¶204. As discussed above, both reduce overall power consumption by placing circuit blocks into a low-power standby mode when not in operation. *See, e.g.*, MTK-1004, [0017], [0052]-[0053], [0094]-[0095]; MTK-1006, 1:20-56, 2:63-3:6; MTK-1003, ¶¶203-204. To do so, Takahashi and Ko both utilize MOS transistors as switches to connect or disconnect the circuit blocks from a voltage supply. MTK-1004, [0051]-[0052] (“[S]witching circuit 20 ... with pMOS transistor MP0 ... supplies an operating current to logic circuit 10 during operation and suppresses the leakage current ... during standby.”); MTK-1006, 2:63-3:6 (“As shown in FIG. 1, a suitable transistor is provided as a header switch for selectively ... connecting and disconnecting the module level power supply VDD to and from the chip level (permanent) power supply VCC.”). They both teach modifying voltages to their respective circuit

blocks and switching transistors during operational and standby states to limit power consumption due to leakage currents. MTK-1004, [0052], [0112]-[0116]; MTK-1006, 4:1-24, 7:32-55; MTK-1003, ¶205.

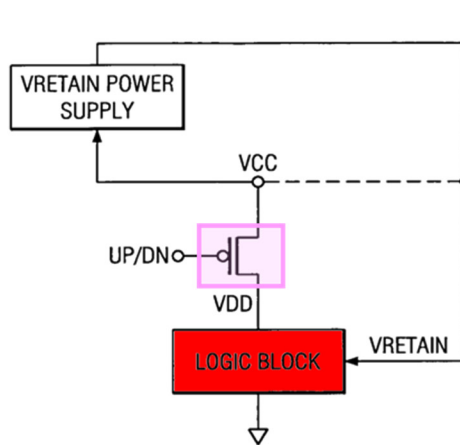


FIG. 1

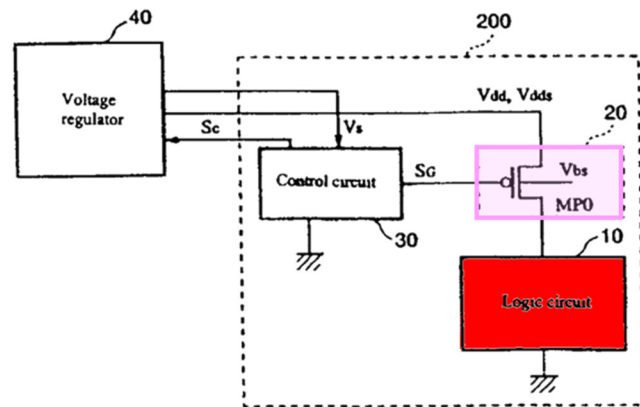


FIG. 1

MTK-1006, FIG. 1 (left); MTK-1004, FIG. 1 (right)

The similarities across Takahashi's and Ko's teachings—along with their common ownership—would have led a POSITA to employ Ko's state machine with Takahashi's "voltage regulator" to improve Takahashi's ability to reduce power consumption, including that resulting from leakage currents. MTK-1003, ¶¶206-207.⁹ For example, Takahashi discloses that the "[v]oltage regulator 100

⁹ As explained at Ground 1A, Takahashi alone discloses and renders obvious employing a state machine. To the extent that Takahashi fails to do so, Takahashi in combination with Ko renders obvious Claim 3.

controls the levels of source voltages V_{dd1} , V_{dd2} , and V_{dd3} supplied to device 200 using predetermined optimum values according to control signal S_C indicating control data DAT and the operating condition of the device.” MTK-1004, [0109]-[0117], Figures 14-17.

A POSITA would have understood that not all the circuits in “device 200” require power at all times it is operational. MTK-1003, ¶208. For example, the “source voltage V_{dd3} ” is provided to “another control circuit 70” with “Wake up logic.” MTK-1004, [0112]-[0117], FIGS. 14-17. A POSITA would have understood, consistent with its name, that “Wake up logic” is only used while “device 200” is returning to operation from standby. MTK-1003, ¶208. While “Wake up logic” could be powered down after completing its function, the “voltage regulator” in Takahashi continues to provide it with an operational “source voltage V_{dd3} .” Thus, Takahashi’s implementation results in some wasted power. MTK-1004, [0110]-[0117]; MTK-1003, ¶208.

As explained at elements 1[p] and 1[b] of Ground 1A, a POSITA would have found it obvious for Takahashi’s “device 200” to include additional power islands, such as additional memories, logic circuits, microprocessor cores, DSP cores, or peripheral circuits. MTK-1004, [0087]-[0095]; MTK-1003, ¶¶209-210. Not all these circuit blocks would require power at all times during the operation of “device 200.” MTK-1003, ¶¶209-210.

Ko addresses any perceived shortcoming of Takahashi by employing a state machine to selectively power down unused circuits within the device during its operation. MTK-1006, 2:63-3:6, 7:20-50; MTK-1003, ¶¶211-212. Ko discloses a “power state controller 45 ... [that] utilizes state machines to provide appropriate control signals to the header switches and logic modules” to power down “logic modules” not in use. MTK-1006, 2:63-3:6, 7:32-50, 9:42-50 (“it may be desirable to power-down one or more of the logic modules independently of the remaining logic modules, in order to reduce current consumption.”); MTK-1003, ¶¶210-212.

Because Takahashi and Ko are commonly owned references that provide a similar solution to a similar problem within the same field of endeavor, a POSITA would have naturally looked at, and been motivated to combine, the two references to further reduce the power consumption in Takahashi’s system. A POSITA would have been motivated to employ Ko’s “state machines” with Takahashi’s “voltage regulator” to selectively power-down circuits within Takahashi’s “device 200” when not in use.

A POSITA would have understood that employing Kos’ state machine in Takahashi’s “voltage regulator” to control the power to individual circuits would have been readily implemented by a POSITA with predictable results. MTK-1003, ¶¶212-213. The use of state machines was a well-known solution for efficiently controlling an integrated circuit, and a POSITA would have needed only routine

electrical and computer engineering principles to implement a state machine with Takahashi's "voltage regulator." MTK-1003, ¶¶212-213. As one example, a POSITA would have understood how to employ a state machine to set the individual "source voltages" to their "operational" or "standby" levels depending on whether the respective circuits powered by those "source voltages" were in use. MTK-1003, ¶¶212-213. Such a combination would predictably reduce the overall power consumption of "device 200" by reducing the power consumption of inactive circuits even while "device 200" remains operational. MTK-1003, ¶¶212-213.

3. Claim 3

The Takahashi-Ko combination renders obvious Claim 3. MTK-1003, ¶¶214-221 Ko discloses that "a suitable transistor is provided as a header switch for selectively (in response to the signal UP/DN) connecting and disconnecting the module level power supply VDD to and from the chip level (permanent) power supply VCC." MTK-1006, 2:63-3:6.

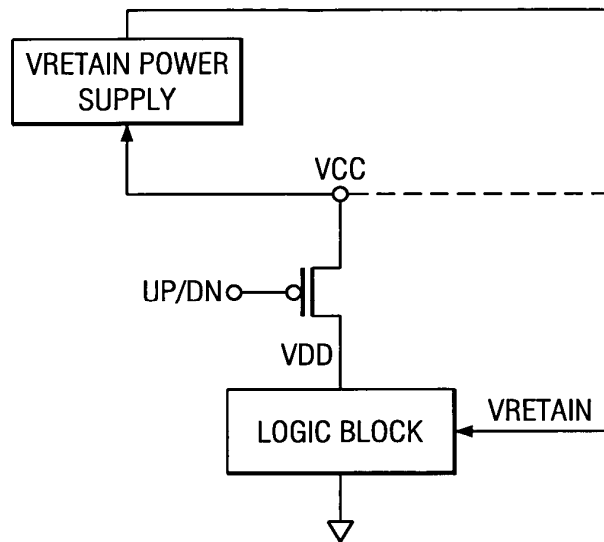


FIG. 1

MTK-1006, FIG. 1

Ko applies this technique to “a wireless communication apparatus” having multiple logic modules, so that it may “power-down one or more of the logic modules independently of the remaining logic modules, in order to reduce current consumption.” *Id.*, 7:20-50, 9:42-63; MTK-1003, ¶¶215-217. Ko “utilizes state machines to provide appropriate control signals to the header switches and logic modules.” MTK-1006, 7:38-42. Specifically, a “power state controller provides control signals UP/DN to the respective header switches” to connect and disconnect the logic modules from the system power “VCC.” *Id.*, 7:42-47; MTK-1003, ¶217.

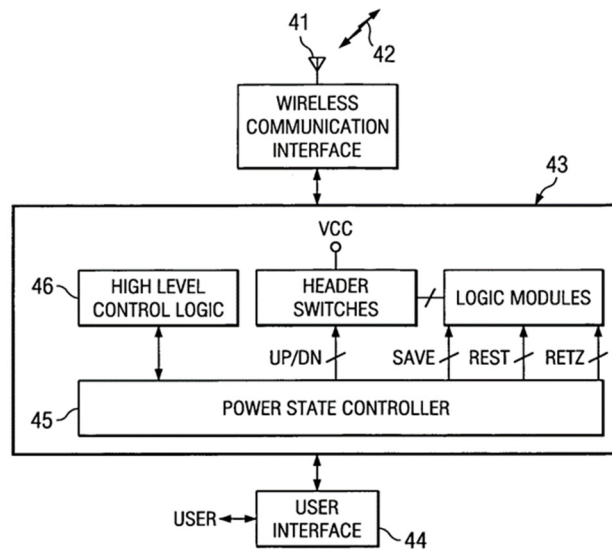


FIG. 4

MTK-1006, FIG. 4

“The power state controller 45 activates these control signals appropriately” so that the logic modules necessary for a given function are powered on while unused logic modules are powered-down to conserve power. MTK-1006, 7:32-50; MTK-1003, ¶¶217.

From Ko’s teachings, a POSITA would have found it obvious for Takahashi’s “voltage regulator” to employ a state machine to further conserve power when individual circuits in “device 200” are not in use, even while “device 200” is operational. MTK-1003, ¶¶218-219. For instance, the “voltage regulator 100” of Figures 11-17 would employ Ko’s “state machine” to provide an operational “ V_{dd3} ” to the “Wake up logic” of “control circuit 70” when “device 200” is coming out of standby, and to lower “ V_{dd3} ” to the standby level after

completing its “Wake up” function. MTK-1004, [0110]-[0117], FIGS. 14-17;
MTK-1003, ¶¶218-219.

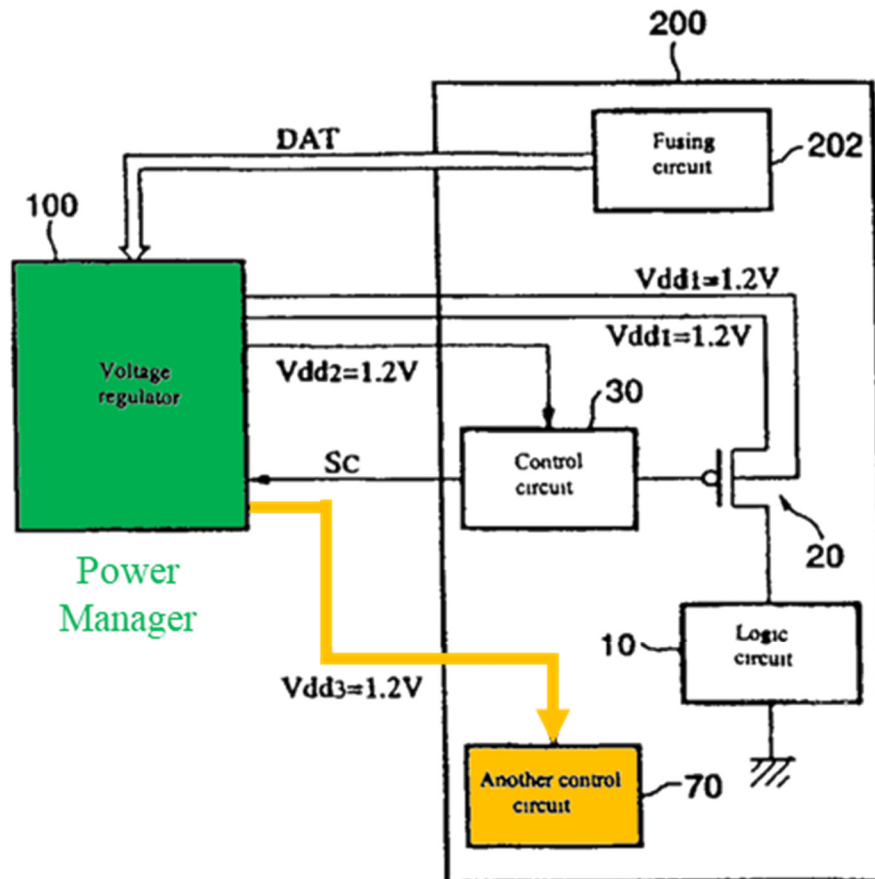


FIG. 16

MTK-1004, FIG. 16

Active Mode	Bit 2	Bit 1	Bit 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0	0	0	1.2V	1.2V	1.20V	Weak
Fuse prog-1	0	0	1	1.15V	1.15V	1.15V	NTPW,NWPT
Fuse prog-2	0	1	0	1.05V	1.05V	1.05V	TYPC,NSPW,NWPS
Fuse prog-3	0	1	1	0.95V	0.95V	0.95V	NSPT,NTPS
Fuse prog-4	1	0	0	0.85V	0.85V	0.85V	Strong

FIG. 14

Sleep Mode	Bit 2	Bit 1	Bit 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0	0	0	0.7V	1.0V	0.7V	Weak
Fuse prog-1	0	0	1	0.7V	1.0V	0.7V	NTPW,NWPT
Fuse prog-2	0	1	0	0.7V	1.0V	0.7V	TYPC,NSPW,NWPS
Fuse prog-3	0	1	1	0.7V	1.0V	0.7V	NSPT,NTPS
Fuse prog-4	1	0	0	0.7V	1.0V	0.7V	Strong

FIG. 15

MTK-1004, FIGS. 14-15

A POSITA would have had a reasonable expectation of success in combining Ko with Takahashi, because the combination would represent a simple integration of Ko's "state machine" into Takahashi's system for controlling the putting to sleep and taking out of sleep of the "logic circuit 10," "control circuit 70," and other power islands. MTK-1003, ¶219. Employing Ko's "state machine" would have required merely routine electrical or computer programming knowledge and was a task well within the skill of a POSITA. *Id.* By powering-down inactive circuits while other circuits of the "device 200" remain operational, the overall power consumption of "device 200" is reduced. Thus, incorporating

Ko’s “state machine” would improve Takahashi’s ability to “reduce the power consumption in order to allow [mobile communication terminals] to operate for a long time.” MTK-1004, [0002]; MTK-1003, ¶¶219-221.

4. Claim 12

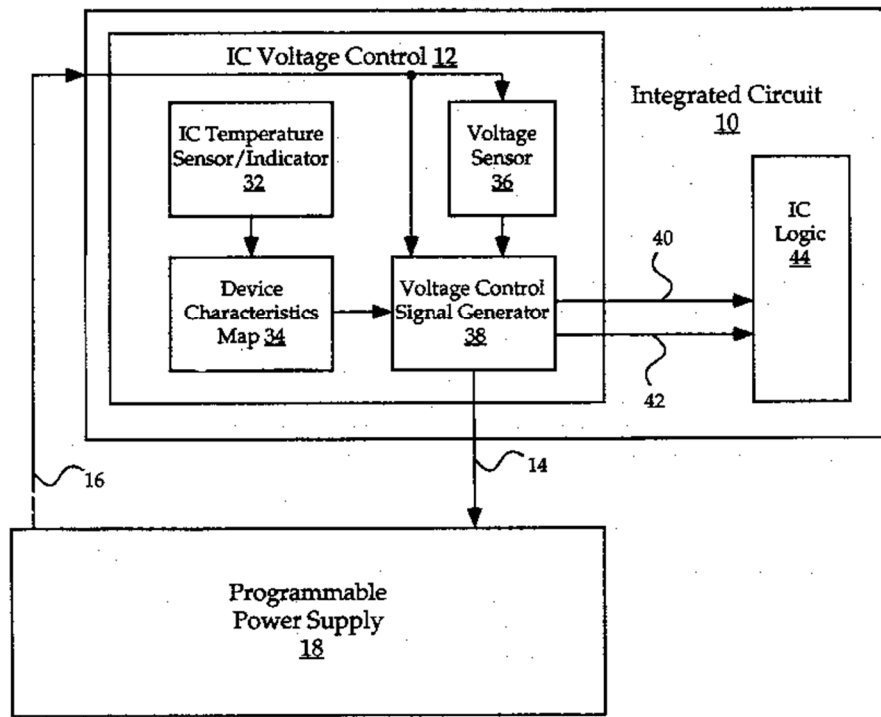
Supra Claim 3. MTK-1003, ¶222.

C. GROUND 1C—CLAIMS 5 AND 14 ARE OBVIOUS OVER TAKAHASHI IN VIEW OF SCHUTZ

1. Overview of Schutz

Schutz relates to controlling an integrated circuit’s supply voltage “to optimize performance and reduce power consumption.” MTK-1007, 1:7-36; MTK-1003, ¶¶223-228. Schutz discloses an “integrated circuit device 10 [that] selects the supply voltage 16 based on a plurality of predetermined operational voltages and the temperature of integrated circuit device 10.” *Id.*, Abstract, 6:31-35.

Figure 2



MTK-1007, FIG. 2

As shown in Figure 2, “IC voltage control circuit 12 includes an IC temperature sensor circuit 32, a device characteristics map 34, a voltage sensor circuit 36, and a voltage control signal generator 38.” *Id.*, 6:37-41. “The device characteristics map 34 stores predetermined operational characteristics of integrated circuit device 10,” which may be determined when manufacturing and testing the device. *Id.*, 6:64-66, 7:1-5, 7:24-37. Based on a temperature detected by “IC temperature sensor 32, device characteristics map 34 provides the corresponding operational voltage value to the voltage control signal generator

38,” which controls the “programmable power supply 18” to provide the selected voltage for the integrated circuit device 10. *Id.*, 7:38-45. Thus, Schutz’s “integrated circuit device 10” ensures a reliable operation speed for the device and reduces power consumption regardless of manufacturing variations and temperature changes. *Id.*, 1:13-2:45; MTK-1003, ¶228.

2. Takahashi-Schutz Combination

A POSITA would have been motivated to modify Takahashi’s integrated circuit to incorporate the teachings of Schutz with a reasonable expectation of success. MTK-1003, ¶¶229-243. Both Takahashi and Schutz are directed to optimizing power to integrated circuits, including to reduce power consumption. MTK-1004, [0001] (“The present invention pertains to a semiconductor integrated circuit ... by which power consumption can be reduced by suppressing leakage current.”), [0002] (discussing applications for “mobile communication terminals”), [0017]; MTK-1007, Title, Abstract, 1:7-10 (“The present invention relates generally to supplying electrical power to circuits”), 1:13-2:45 (discussing benefits of “reduced power consumption” including to “increase battery life of laptop and notebook computers.”). The ’077 Patent relates to this same field of endeavor. *See* MTK-1001, Abstract, 1:29-39; 2:37-50; MTK-1003, ¶¶229-230.

Both Takahashi and Schutz address the problem of providing optimum voltages to an integrated circuit and do so in similar ways. MTK-1003, ¶¶231-235.

Takahashi discloses adjusting “source voltages” “according to the driving capabilities of the transistors” in the circuit. MTK-1004, [0099]-[0100]. Schutz adjusts “supply voltage 16” to “optimize the high speed or high frequency performance” of the device depending on its “manufacturing process,” “intended use,” and “performance characteristics.” MTK-1007, 5:14-18, 7:5-8.

Both Takahashi and Schutz perform device testing to determine device characteristics. MTK-1004, [0099]-[0100], [0109]; MTK-1007, 5:14-27, 7:24-37. Takahashi and Schutz then program non-volatile memory in the devices based on the test results and use this programming to optimize the supply voltages to the integrated circuits. MTK-1004, [0098]-[0117], FIGS. 14-17; MTK-1007, 4:55-5:34, 6:64-7:45, 8:12-28, FIG. 3. Specifically, Takahashi’s “voltage regulator 100” receives “control data DAT” stored in “fusing circuit 202,” and “generates source voltages V_{dd1} , V_{dd2} , and V_{dd3} using optimum values ... according to control data DAT and control signal SC indicating the operating status of device 200.” MTK-1004, [0098], [0117]. Schutz’s “IC voltage control circuit 12” “selects one of the predetermined operational voltages stored in the device” that is the “optimized operational voltage for the measured device temperature,” after which the selected “supply voltage is generated by the programmable power supply.” MTK-1007, 8:11-28. Thus, both references reduce “the effect of variations in the production process” by powering their devices using “optimum source voltages.”

MTK-1004, [0117]; MTK-1007, 7:5-37 (“predetermined operational voltages may be chosen to optimize the high speed or high frequency performance” for a “given temperature” and “particular device”), 8:12-19.

Figure 2

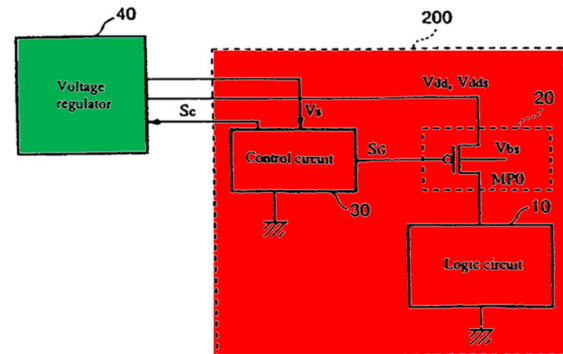
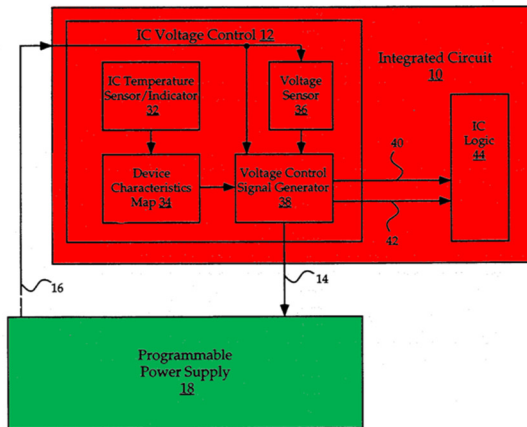


FIG. 1

MTK-1007, FIG. 2 (left); MTK-1004, FIG. 1 (right)

The similarities between Takahashi and Schutz would have led a POSITA to implement Schutz’s teachings in Takahashi’s integrated circuit to further improve Takahashi’s ability to optimize the voltages provided to “device 200.” MTK-1003, ¶¶236-237.¹⁰ Takahashi already programs “control data DAT” into the “fusing circuit 202” to account for “variations during the production process.” MTK-1004,

¹⁰ As explained at Ground 1A, Takahashi alone renders obvious the features of Claim 5. To the extent that Takahashi fails to do so, Takahashi in combination with Schutz renders obvious y Claim 5.

[0099]; MTK-1003, ¶¶236-237. As explained at Claim 5 of Ground 1A, a POSITA would have understood that other factors including temperature also impact the optimum voltages to provide “device 200.” MTK-1003, ¶¶237-238. Thus, while Takahashi’s “source voltages” are optimized for process variation, those voltages may not be the most optimal voltages for “device 200.” MTK-1004, [0117]; MTK-1003, ¶238. A POSITA therefore would have understood and been motivated to further optimize the voltages generated by “voltage regulator 100” to account for variations in temperature. MTK-1003, ¶238.

Schutz provides such a system for optimizing the voltages provided to an “integrated circuit device” to account for temperature variations. MTK-1007, Abstract; MTK-1003, ¶¶239-240. Schutz discloses that its “integrated circuit device may include a temperature sensor to allow selection of the predetermined operational voltage according to device temperature to avoid speed-limiting voltage and temperature combinations.” MTK-1007, Abstract; *see also id.*, 8:13-19 (the “optimized operational voltage” may be based on the “measured device temperature” or “other factors including ... manufacturing characteristics or the intended application of the device”). Schutz’s “IC temperature sensor 32 senses the temperature of the device 10 and indicates that temperature to the device characteristics map 34.” MTK-1007, 6:50-52. “In response ... device characteristics map 34 provides the corresponding predetermined operational

voltage value to the voltage control signal generator 38.” *Id.*, 7:38-42. The “voltage control signal generator 38” then controls the “programmable voltage generator 18” to generate the optimal “supply voltage 16” for “integrated circuit device 10.” *Id.*, 4:14-18, 8:20-28.

Because Takahashi and Schutz provide a similar solution to a similar problem within the same field of endeavor, a POSITA would have naturally looked at, and been motivated to combine, the two references to further optimize the “source voltages” in Takahashi’s system. A POSITA would have been motivated to employ Schutz’s “IC temperature sensor” to further optimize the “source voltages” from “voltage regulator 100” based on both process variation and temperature variation. MTK-1003, ¶241.

A POSITA would have readily implemented Schutz’s temperature sensor to further optimize the voltages provided to Takahashi’s “device 200” with predictable results. MTK-1003, ¶¶242-243. Temperature sensors were well known in the art, and a POSITA would have needed only routine electrical and computer engineering principles to add a temperature sensor to Takahashi’s “device 200.” MTK-1003, ¶¶242-243. A POSITA would have further known how to modify Takahashi’s “voltage regulator 100” to consider temperature in addition to the “control data DAT and status control signal Sc” when selecting the optimum

values for the “source voltages” provided to “device 200.” MTK-1004, [0111];
 MTK-1003, ¶¶242-243.

TABLE 2

predetermined operational voltage	programmed value
+5.0	000
−5.0	001
12.0	010
3.3	011
2.5	100
1.8	101
1.5	110
1.2	111

TABLE 3

0–20° C.	3.0 V	40–50° C.	3.3 V
10–20° C.	3.1 V	50–60° C.	3.4 V
20–30° C.	3.2 V	60–70° C.	3.5 V
30–40° C.	3.2 V	70–80° C.	3.6 V

Active Mode	Bit 2	Bit 1	Bit 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0	0	0	1.2V	1.2V	1.20V	Weak
Fuse prog-1	0	0	1	1.15V	1.15V	1.15V	NTPW,NWPT
Fuse prog-2	0	1	0	1.05V	1.05V	1.05V	TYP,NSPW,NWPS
Fuse prog-3	0	1	1	0.95V	0.95V	0.95V	NSPT,NTPS
Fuse prog-4	1	0	0	0.85V	0.85V	0.85V	Strong

FIG. 14

Sleep Mode	Bit 2	Bit 1	Bit 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0	0	0	0.7V	1.0V	0.7V	Weak
Fuse prog-1	0	0	1	0.7V	1.0V	0.7V	NTPW,NWPT
Fuse prog-2	0	1	0	0.7V	1.0V	0.7V	TYP,NSPW,NWPS
Fuse prog-3	0	1	1	0.7V	1.0V	0.7V	NSPT,NTPS
Fuse prog-4	1	0	0	0.7V	1.0V	0.7V	Strong

FIG. 15

MTK-1007, Tables 2-3 (left); MTK-1004, FIGS. 14-15 (right)

This combination would predictably optimize the voltages provided to “device 200” to further account for temperature variations, thereby improving its performance and power consumption MTK-1003, ¶¶242-243.

3. Claim 5

The Takahashi-Schutz combination renders obvious Claim 5. MTK-1003, ¶¶244-250. Schutz discloses an “IC voltage control circuit 12” that selects an optimum operational voltage “based on the temperature of the device” and “device characteristics.” MTK-1007, 6:64-7:37; MTK-1003, ¶246. An “IC temperature sensor 32” detects the temperature of the integrated circuit device and an “optimized operational voltage” for the device is selected based on the measured temperature and a “device characteristics map 34.” MTK-1007, 6:50-7:37, 8:12-18; MTK-1003, ¶246.

From Schutz’s teachings, a POSITA would have found it obvious for Takahashi’s “voltage regulator” to generate an optimum voltage that is dependent upon both process variation and temperature variation. It would have been obvious for the “voltage regulator 100” to receive a temperature signal from a temperature sensor like Schutz’s “IC temperature sensor 32,” and generate optimum “source voltages” based on the temperature signal in addition to the “status control signal S_C” and the “control data DAT” that accounts for process variations. MTK-1004, [0098], [0111], [0117], FIGS. 13-17; MTK-1003, ¶¶247-248.

A POSITA would have had a reasonable expectation of success in combining Schutz and Takahashi because the combination would represent a simple integration of Schutz’s “IC temperature sensor 32” into Takahashi’s system

for generating optimum source voltages for “device 200.” MTK-1003, ¶¶248-249. Employing Schutz’s “IC temperature sensor 32” would have required merely routine electrical or computer programming knowledge and was a task well within the skill of a POSITA. *Id.* Incorporating Schutz’s temperature sensing to account for temperature variation in addition to the “effect of variations in the production process” would provide additional improvements in performance and power consumption for the “device 200.” *Id.*

4. Claim 14

Supra Claim 5. MTK-1003, ¶251.

D. GROUND 2A—CLAIMS 1-18 ARE OBVIOUS OVER MIZUNO

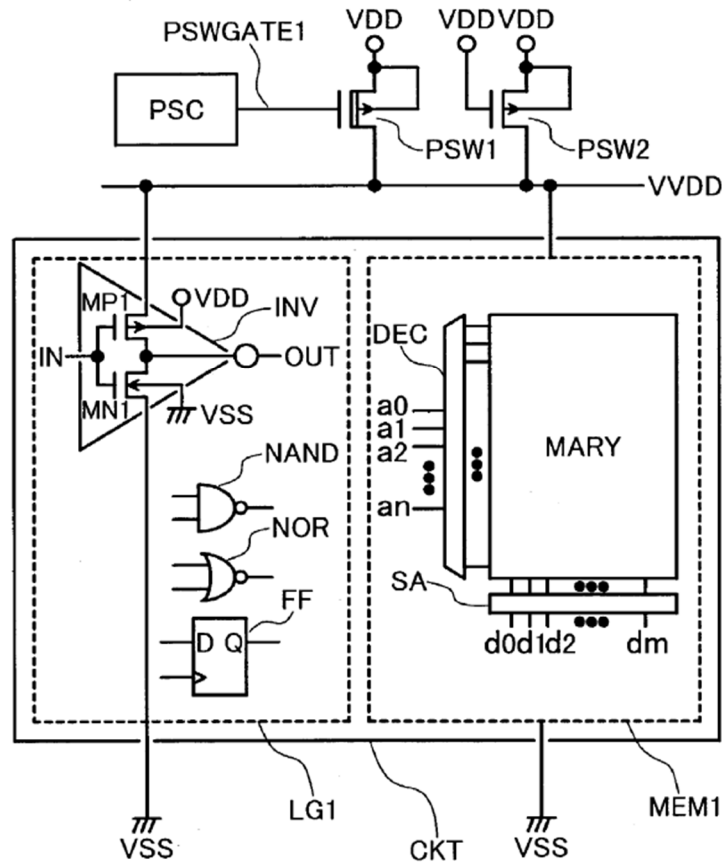
1. Overview of Mizuno

Mizuno relates to “a semiconductor integrated circuit device with excellent high speed and low power operation characteristics.” MTK-1005, [0001]; MTK-1003, ¶¶253-254. Mizuno’s integrated circuit device contains a “leakage current control circuit” coupled to a “circuit block CKT.” MTK-1005, Abstract, [0008]-[0009], [0053]. The “leakage current control circuit” is provided to “reduc[e] the different types of leakage current ...while the circuit block is in standby state,” while still “allow[ing] high speed circuit block operation while the circuit block is in the operation state.” MTK-1005, Abstract, [0008]-[0009].

Figures 1-30 depict one embodiment of Mizuno's integrated circuit device.

MTK-1005, [0052]-[0107]; MTK-1003, ¶¶255-256. In this embodiment, the “power switch controller PSC controls the on and off operation of the power switch PSW1 connected between the power supply VDD and the virtual power line VVDD” and “also controls the current flow in the power supply VDD and the virtual power line VVDD.” MTK-1005, [0054]; MTK-1003, ¶¶255-256. The “power supplied to the circuit block during operation is mainly supplied from the power switch [PSW1]; and the currently supplied to the circuit block during standby operation is mainly supplied to the current source PSW2.” MTK-1005, [0054]; MTK-1003, ¶¶255-256.

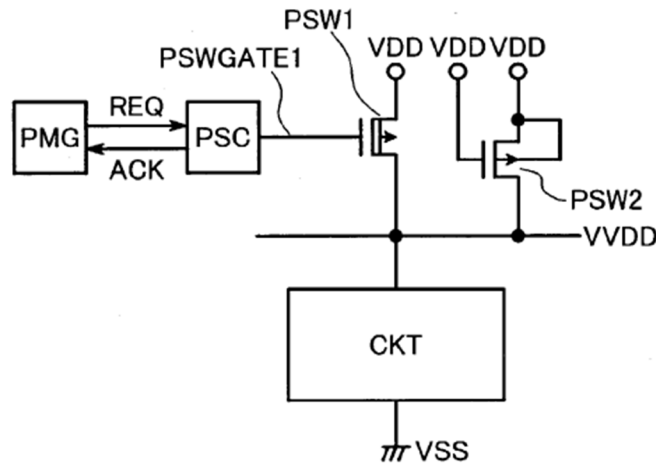
FIG.1



MTK-1005, FIG. 1

A “power controlling circuit PMG” shown in Figure 22 communicates with the “power switch controller PSC by means of the request line REQ and response line ACK [to control] the on/off operation of the power switch PSW1 and [control] the state of the circuit block.” MTK-1005, [0093]; MTK-1003, ¶¶257-258.

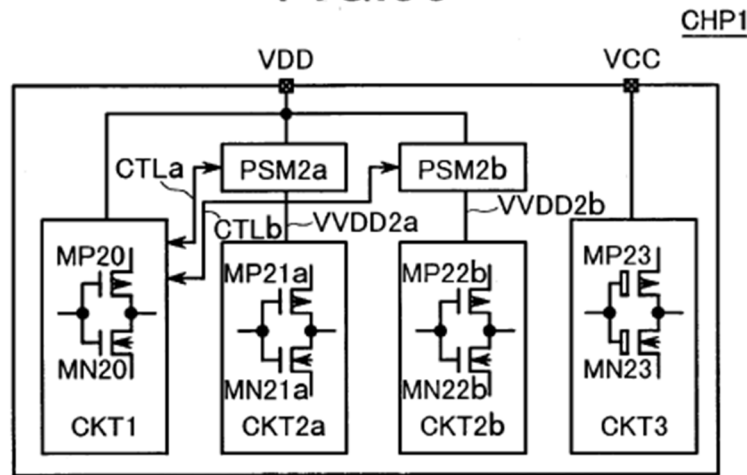
FIG.22



MTK-1005, FIG. 22

In a related embodiment depicted in Figures 35-40, an integrated circuit chip includes multiple circuit blocks whose power is provided either directly or via “leakage reduction circuits.” MTK-1005, [0120]-[0134]; MTK-1003, ¶¶259-260. Mizuno explains that “the various adaptations and specific examples disclosed for the first embodiment are also applicable to the leakage current reduction circuit of the third embodiment.” MTK-1005, [0130]. By controlling the leakage currents through individual circuit blocks using “multiple leakage control circuits [PSM2a, PSM2b] as in FIG. 35 ... the leakage current of the overall chip can be efficiently reduced.” MTK-1005, [0122]; MTK-1003, ¶¶259-260.

FIG.35



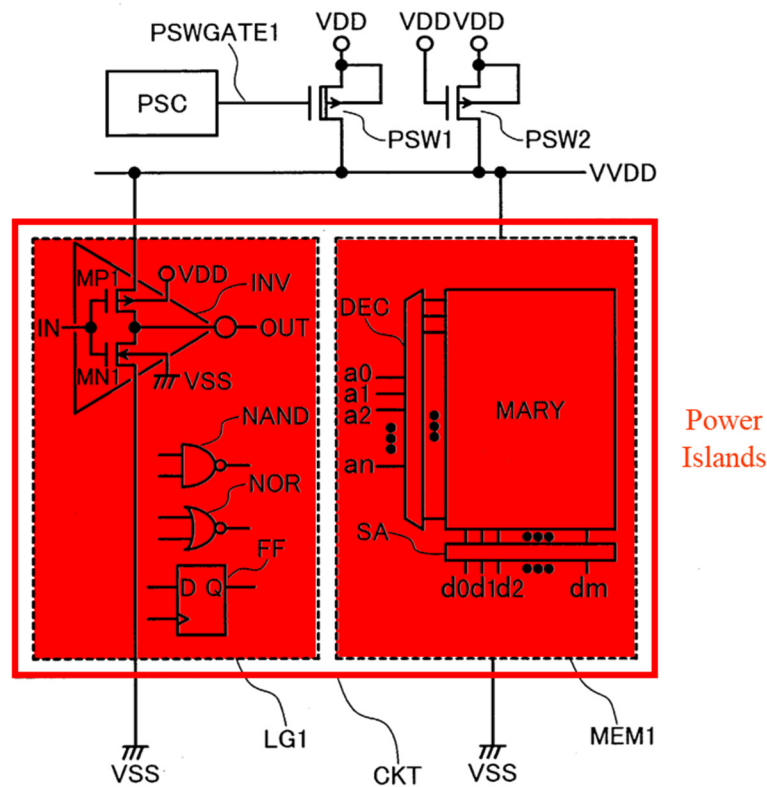
MTK-1005, FIG. 35

2. Claim 1

(a) Element 1[p]

Mizuno discloses methods carried out in “a semiconductor integrated circuit device.” MTK-1005, Title, [0001]; MTK-1003, ¶¶261-263. Mizuno’s integrated circuit includes a “circuit block CKT as shown for example in FIG. 1 contain[ing] a logic circuit LG1 ... and a memory MEM1.” MTK-1005, [0053]. A POSITA would have understood and found it obvious that “logic circuit LG1” and “memory MEM1,” both individually and collectively, are power islands because power consumption is controlled within them. *Id.*, [0054]; MTK-1003, ¶¶264-269; *see* MTK-1001, 3:65-4:1.

FIG.1

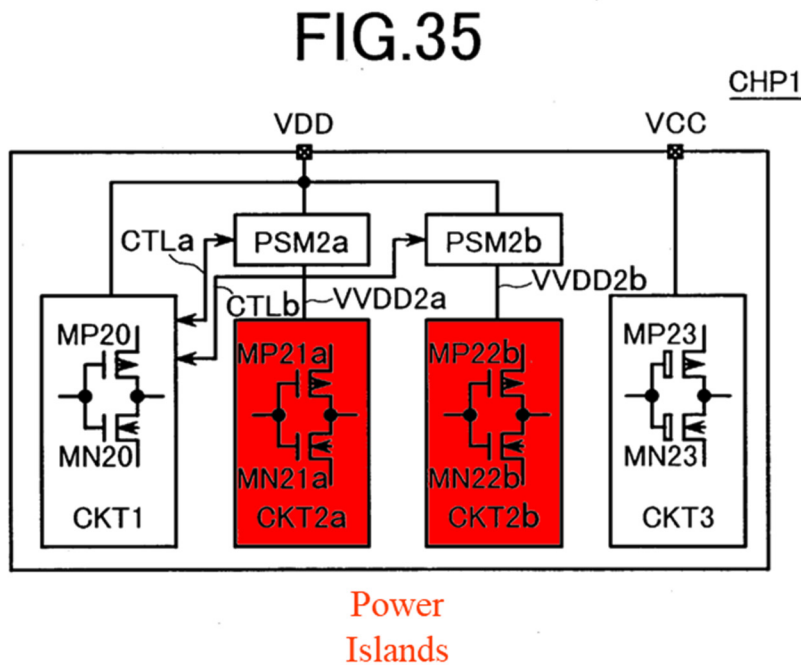


MTK-1005, FIG. 1

Specifically, during an “operating state,” “power is supplied to the circuit block CKT by way of the power switch PSW1 so that the virtual power line VVDD reaches VDD potential and the circuit block CKT is operable.” MTK-1005, [0055]. Conversely, during “standby,” “power switch PSW1 turns off” and the “voltage (or voltage potential) of virtual power line VVDD gradually discharges ... to ground VSS.” *Id.*, [0054]-[0055]. “As the voltage of the virtual power line VVDD becomes lower ... [t]he leakage current flowing to circuit block

CKT ... also gradually becomes a smaller value,” thereby reducing the power consumption of the circuit block CKT during standby. *Id.*; MTK-1003, ¶¶264-269.

Similarly, in the embodiment of Figures 35-40, Mizuno discloses an integrated circuit having multiple “circuit blocks” that are power islands.



MTK-1005, FIG. 35

For example, in Figure 35, power to the circuits CKT2a and CKT2b is controlled by the “leakage reduction circuits PSM2a and PSM2b” having a similar structure to the leakage reduction circuitry in the embodiment of Figures 1-30. *See* MTK-1005, [0125]-[0128], [0130], FIG. 38; MTK-1003, ¶¶267-269. Thus, a POSITA would have understood and found obvious that Mizuno’s integrated circuit includes multiple power islands. MTK-1003, ¶¶267-269. Mizuno’s integrated

circuit also includes a “power switch controller PSC” for controlling the power to these power islands. MTK-1005, [0054], [0093]; MTK-1003, ¶¶270-274.

Specifically, the “PSC controls the on and off operation of the power switch PSW 1 connected between the power supply VDD and the virtual power line VVDD” that powers the “circuit block CKT.” *Id.* During operation, the “PSC” turns on “power switch PSW 1” so that “the current supplied to the circuit block ... is mainly supplied from power switch [PSW1].” *Id.* During standby, the “PSC” turns off “power switch PSW1” and “the current supplied to the circuit block ... is mainly supplied [by] the current source PSW2.” *Id.* “[T]he size of the respective leakage currents ... during standby in the circuit block are determined by the current source PSW 2” and “is smaller than the leakage current flowing in the circuit block CKT during operation.” MTK-1005, [0059].

FIG.1

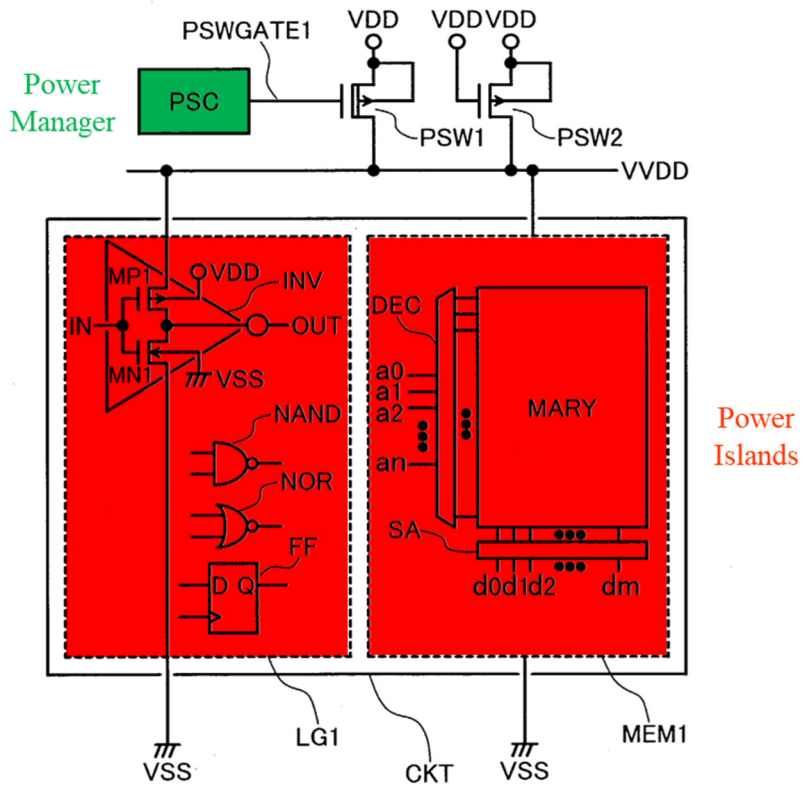
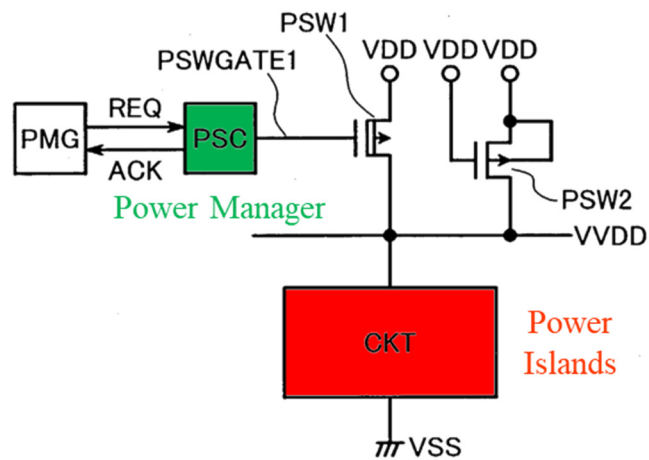
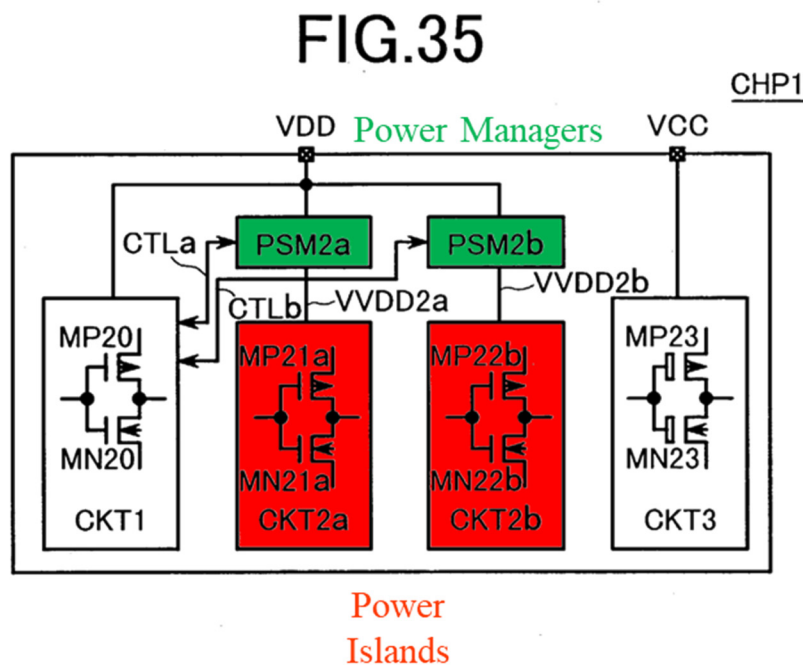


FIG.22



MTK-1005, FIGS. 1, 22

A POSITA would have understood and found obvious that Mizuno’s “power switch controller PSC” is a power manager because it controls power within the “circuit block CKT” by “modify[ing] the voltage within the power island.” See MTK-1001, 4:11-14; MTK-1003, ¶¶272-275. Similarly, in the embodiment of Figures 35-40, the “leakage reduction circuits PSM2a and PSM2b” include power managers that control power within the circuit blocks CKT2a and CKT2b, respectively. MTK-1003, ¶¶272-275; MTK-1005, [0121]-[0133].

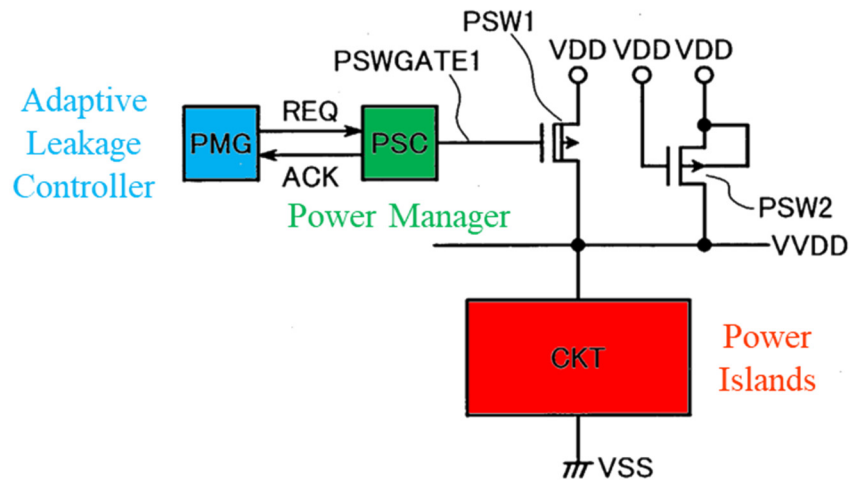


MTK-1005, FIG. 35.

Mizuno’s integrated circuit also includes a “power controlling circuit PMG that reduces power consumption in the chip overall.” MTK-1005, [0093]. To do

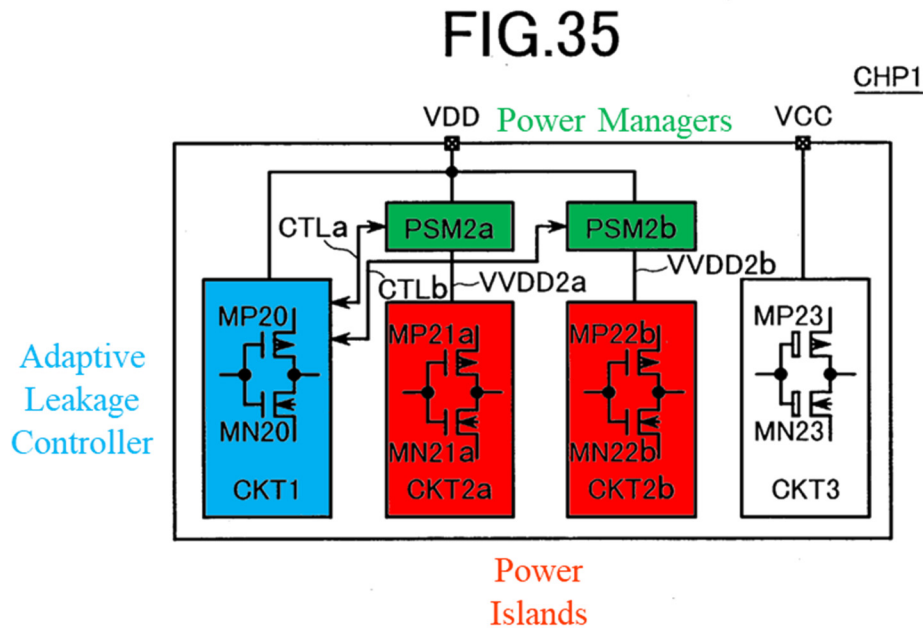
so, the “power controlling circuit PMG” controls the “PSC by means of the request line REQ and response line ACK.” *Id.*

FIG.22



MTK-1005, FIG. 22

Similarly, in the embodiment of Figures 35-40, “circuit block CKT1” has “circuits to control the leakage reduction circuits PSM2a and PSM2b” over “CTLa, CTLb ... leakage control lines” that are “equivalent to the request line REQ and response line ACK of FIG. 22.” *Id.*, [0121]; MTK-1003, ¶¶276-280.

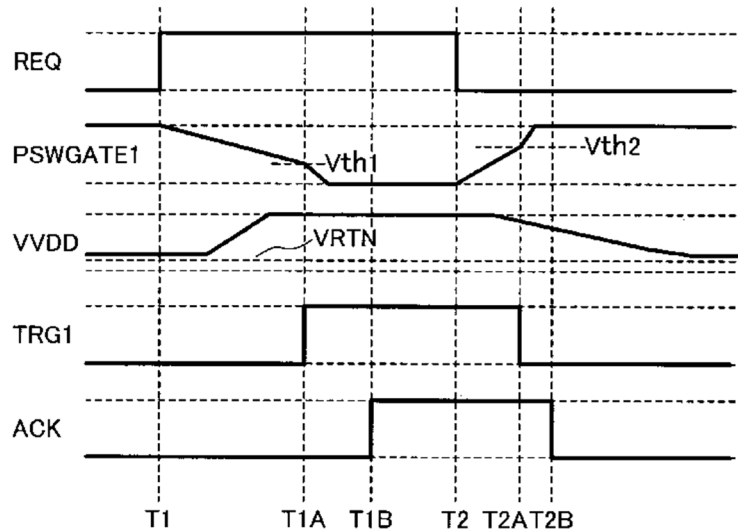


MTK-1005, FIG. 35.

“[S]etting the request line REQ to high level turns on the power switch PSW1” to provide the “circuit block CKT” with an operating voltage VDD through “power switch PSW1.” *Id.*, [0093]. “Conversely, when the request line REQ is set to low level, the power switch PSW1 turns off” and the “circuit block CKT” receives a lower voltage through “current source PSW2 [that] functions as a leak current limiter circuit.” *Id.*, [0057], [0093]; MTK-1003, ¶¶277-278. As shown in Figure 24, for instance, when Mizuno’s “power controlling circuit PMG” sets “REQ” from high to low, the voltage “VVDD” to the “circuit block CKT” decreases from VDD to VRTN and the leakage current “I_{off}(CKT)” through the

“circuit block CKT” also reduces. MTK-1005, [0096]-[0098]; MTK-1003, ¶¶278-280; *see also* MTK-1005, [0055]-[0056], [0065]-[0066], FIG. 5.

FIG.24



MTK-1005, FIG. 24

Thus, a POSITA would understand and find obvious that Mizuno’s “power controlling circuit PMG” (“circuit block CKT1” in Figures 35-40) is an adaptive leakage controller that provides control signals to optimize the voltage to the “circuit block CKT” to reduce power consumption due to leakage currents. MTK-1001, 4:21-23, MTK-1003, ¶¶280-285.¹¹

¹¹ To the extent the claimed “adaptive leakage controller” must provide control signals to compensate for process and temperature variation to provide an optimum

As noted above with respect to Ground 1A, “power island” and “power manager” have been construed in prior litigations involving a patent describing similar subject matter, U.S. Patent No. 7,051,306. *See* MTK-1025 43-44, 44-46; MTK-1026 28-29, 29-34. For purposes of this Petition, Petitioner submits that no construction is necessary because plain and ordinary meaning suffices. And while the prior constructions involved a different patent and different claims and are not binding on this proceeding, Mizuno’s disclosures, in light of a POSITA’s knowledge, also render these terms obvious under the prior constructions. *See* MTK-1003, ¶285.

(b) Element 1[a]

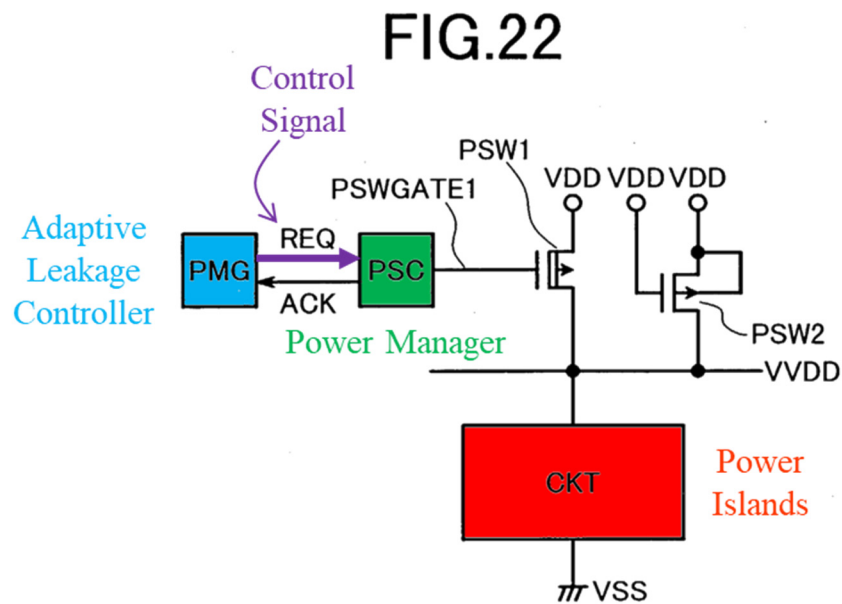
Mizuno discloses that the “power switch controller PSC” (*i.e.*, power manager) receives a control signal “REQ” from the “power controlling circuit

voltage to sleep transistors, Mizuno discloses and renders obvious those features.

Mizuno discloses that the voltages provided to the “power switch PSW1” such as VREF and VDD2a in Figures 35-40 are optimized based on the operating status and “variations (non-uniformities) in chip manufacture or information on environmental fluctuations.” MTK-1005, [0126]-[0128]; MTK-1003, ¶¶281-285.

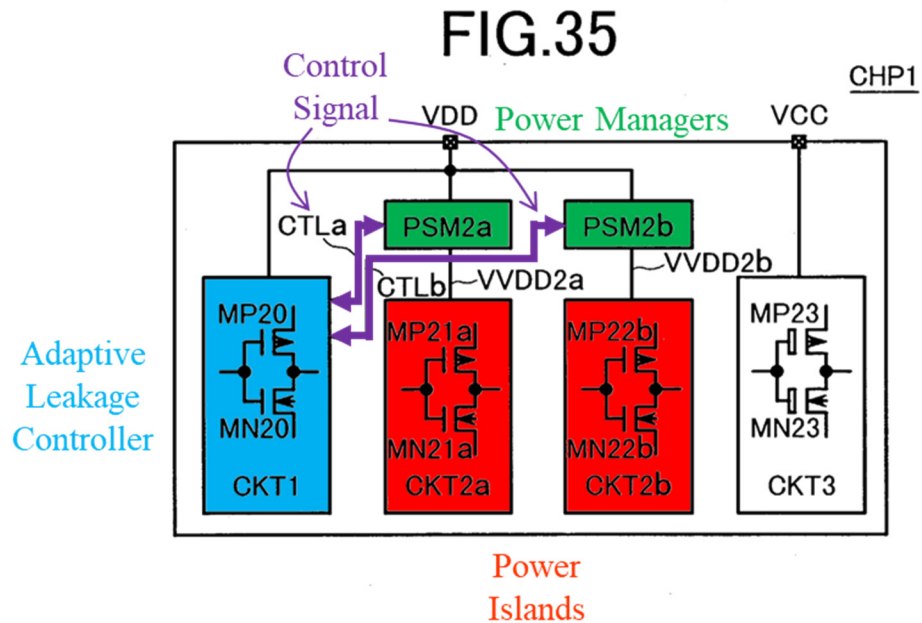
A POSITA would understand and find obvious that such information would be provided via the signal CTLA. *Id.*

PMG” (*i.e.*, adaptive leakage controller). MTK-1005, [0093]; MTK-1003, ¶¶287-292. The “REQ” signal controls the “PSC” to set “PSWGATE1” either high or low to turn the “power switch PSW1” on or off, respectively, which places the “circuit block CKT” into an operational or standby state. *Id.*



MTK-1005, FIG. 22

Similarly, in the related embodiment of Figures 35-40, “CTLa, CLTb are leakage control lines of the leakage reduction circuit of the present invention and equivalent to the request line REQ and response line ACK of FIG. 22.” MTK-1005, [0121].



MTK-1005, FIG. 35

(c) Element 1[b]

Mizuno's "PSC" generates a variable voltage "PSWGATE1" based on the control signal "REQ" received from the "power controlling circuit PMG." MTK-1003, ¶¶293-295.

MTK-1005, FIG. 22

For example, Figures 23-24 depict “drive circuits” C1DRV1 and C2DRV2 of the “PSC” generating the time varying voltage “PSWGATE1” based on the control signal “REQ.” MTK-1005, [0095]-[0099].

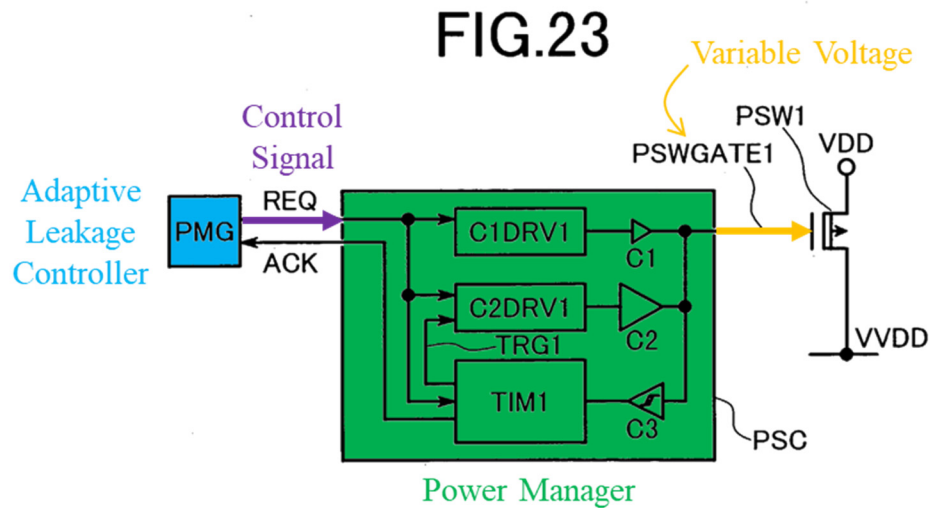
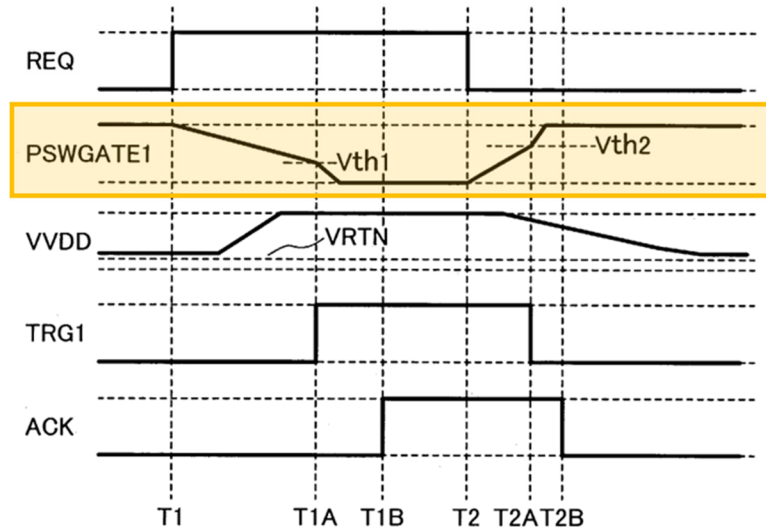


FIG.24

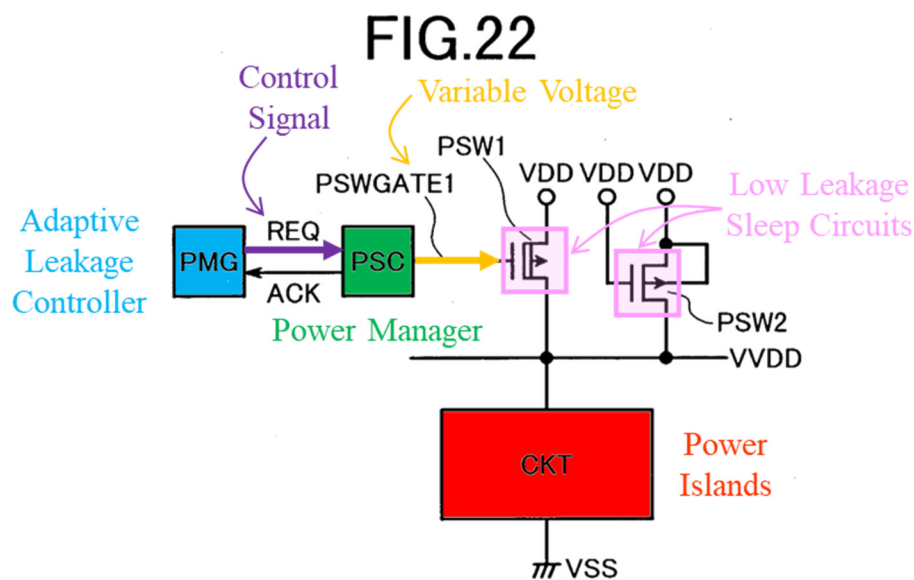


MTK-1005, FIGS. 23-24

Similarly, in the related embodiment of Figures 35-40, the “PSC” and operational amplifier “OPAMP” of the “leak regulator circuit PSM2a or PSM2b” generate variable voltages “VREF,” “PSWGATE2”, and “VVDD2a” based on the control signal “CTL_a” that is “equivalent to the request line REQ and response line ACK of Fig. 22.” MTK-1005, [0121], [0125]; MTK-1003, ¶¶297-301.

Mizuno’s “PSC” provides the variable voltage “PSWGATE1” to the “power switch PSW1” to turn the switch on and off. MTK-1005, [0054]-[0055]. To change from the operational state to standby, “the gate signal PSWGATE1 ... is driven to high level by the power switch controller PSC and the power switch PSW1 turns off.” MTK-1005, [0055]; MTK-1003, ¶¶299-301. As a result, “the

voltage of the virtual power line VVDD becomes lower,” with “the current supplied to the circuit block during standby operation ... mainly supplied [by] the current source PSW2.” MTK-1005, [0054]-[0055]; MTK-1003, ¶¶297-301; *see also* MTK-1005, [0096]-[0098]. The related embodiment of Figures 35-40 operates in the same way. MTK-1005, [0125]-[0127]; MTK-1003, ¶¶300-301.



MTK-1005, FIG. 22

In standby, the leakage current through “power switch PSW1” is substantially less than that through “current source PSW2” (*i.e.*, “ $I_{\text{off}}(\text{PSW1}) \ll I_{\text{off}}(\text{PSW2})$ ”) such that the “current source PSW2 functions as a leak current limiter circuit for circuit block CKT.” MTK-1005, [0055]-[0057], [0085], [0093], [0122]; MTK-1003, ¶¶299-302. Thus, a POSITA would have understood and found obvious that Mizuno’s “power switch PSW1” and “current

source PSW2” are low leakage sleep circuits that reduce leakage in the integrated circuit during standby. MTK-1003, ¶¶301-302; *see* MTK-1001, Abstract, 2:9-20, 2:45-50, 4:21-5:7, 7:12-17.

As such, Mizuno’s integrated circuit employs the “PSC” to dynamically change the power consumption of the power islands during operational and standby states. MTK-1003, ¶¶301-303. When transitioning from the operational state to the standby state, the voltage “VDD” provided to the “logic circuit LG1” and “memory MEM1” power islands of the “circuit block CKT” is drastically reduced, *e.g.*, from “VDD (1.0V)” to “VFNL (0.4V).” MTK-1005, [0055]. As a result, the leakage current “Ioff(CKT) ... also gradually becomes a smaller value” and “power consumption due to leakage current in the circuit block during the standby state can be greatly reduced.” *Id.*, [0055], [0087]; *see also id.*, Abstract, [0060], [0122] (in Figures 35-40, multiple “leakage controls circuits [PSM2a and PSM2b] ... control[] the leakage current of circuits grouped in multiple circuits integrated onto the chip,” such that “the leakage current of the overall chip can be efficiently reduced”); MTK-1003, ¶¶302-304.

3. Claim 2

As discussed at element 1[b], Mizuno’s “circuit block CKT” is put into standby and taken out of standby at different times to reduce power consumption when the “circuit block CKT” is not being used. MTK-1005, [0087], [0093];

MTK-1003, ¶307.¹² Specifically, the “PSC” puts the “circuit block CKT”—including the “logic circuit LG1” and “memory MEM1”—into standby or operational modes at different times by controlling “the on and off operation of the power switch PSW1” and “current flow in the power supply VDD and the virtual power line VVDD.” MTK-1005, [0054]; MTK-1003, ¶307.

To the extent required by Claim 2, Mizuno also discloses and renders obvious that power islands can be placed into standby and operational states at different times from other power islands. MTK-1003, ¶310. As discussed at element 1[b], the embodiment of Figures 35-40 includes multiple “leakage reduction circuits PSM2a and PSM2b” that control “the leakage current of circuits grouped in multiple circuits integrated onto the chip.” MTK-1005, [0121]-[0122];

¹² Mizuno discloses both a “standby (idle)” state that maintains “information within the information retention circuits within the circuit block,” as well as a “deep stand-by state” in which “information in the information retention circuit within the circuit block will be lost.” MTK-1005, [0005], [0087]. The benefit of the “deep stand-by state” is that power to the “circuit block CKT” can be reduced even further to achieve “lower power consumption than in stand-by state with data retention.” *Id.*, [0087]. A POSITA would have understood that both types of standby states are “sleep” states. MTK-1003, ¶¶307-309.

MTK-1003, ¶310. Mizuno explains that the “leakage reduction circuits PSM2a and PSM2b” are controlled by the “CTLa, CTLb ... leakage control lines of the leakage reduction circuit” that are “equivalent to the request line REQ and response line ACK of FIG. 22.” MTK-1005, [0122]. Thus, one of “[c]ircuit blocks CKT2a and CKT2b” can be placed into standby or operational mode at a different time from another using the control lines “CTLa, CTLb.” MTK-1005, [0093], [0121]; MTK-1003, ¶¶309-311.

4. Claim 3

A POSITA would have understood and found obvious that Mizuno’s “PSC” power manager employs a state machine with distinct output states to control putting a power island into standby (“sleep”) and operational (“out of sleep”) states. MTK-1003, ¶312; *see* MTK-1001, 6:19-21; MTK-1008; MTK-1009.

In Figures 23-24, for example, when “REQ reaches high level” to initiate a “shift[] from standby to the operation state” (time T1), the “PSC” enters a first state in which “the gate signal PSWGATE1 is driven to high impedance by C1 by way of the C1DRV control circuit.” MTK-1005, [0096]; MTK-1003, ¶¶313-314.

FIG.23

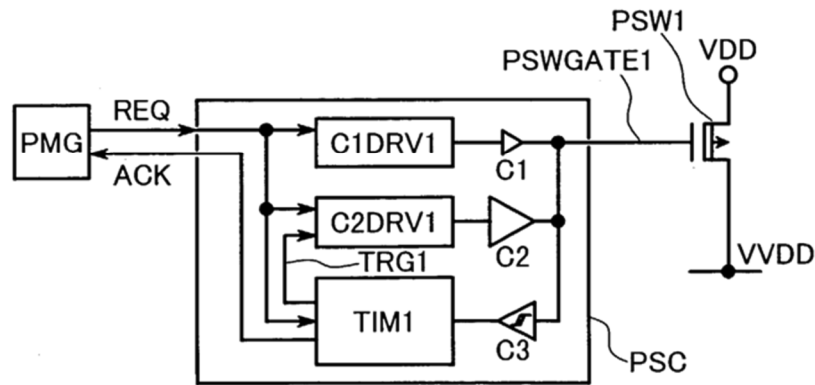
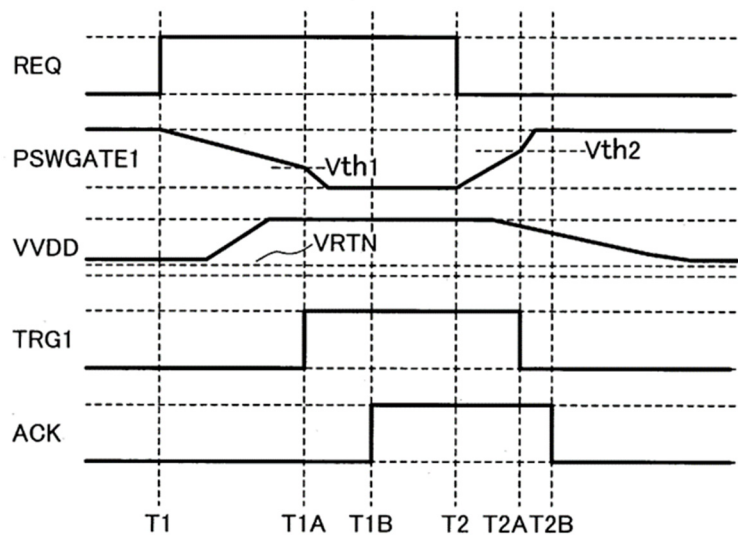


FIG.24



MTK-1005, FIGS. 23-24

Once “PSWGATE1” reaches a “level (V_{th1}) at time $T1A$,” the “PSC” enters a second state in which “PSWGATE1 is ... driven to a low impedance by C2 by way of the C2DRV control circuit” and “TRG1 is driven to high level by the timer TIM1.” *Id.* Finally, at time $T1B$, the “PSC” enters a third state in which “ACK is

driven to high level” and “the virtual power line VVDD may be fully charged up to ... VDD.” *Id.* Mizuno describes a similar state machine process for the “shift[] from the operation state to standby state.” MTK-1005, [0097]-[0101], MTK-1003, ¶¶315-320.¹³

5. Claim 4

The variable voltage “PSWGATE” is set such that when “gate signal PSWGATE1 of power switch PSW1 is driven to low level by the PSC ... the power switch PSW1 turns on,” and when “PSWGATE1 of power switch PSW1 is driven to high level by the power switch controller PSC ... the power switch PSW1 turns off.” MTK-1005, [0055]. The levels of “PSWGATE” are, therefore, optimized to be above or below the threshold voltage of the “power switch PSW1” transistor to turn the switch on or off. MTK-1005, [0058] (explaining that “the MOS transistor threshold voltage V_{th} is the gate voltage when the MOS transistor drain current ... starts to flow”), FIGS. 3, 41; MTK-1003, ¶¶321-326.

¹³ A POSITA would have understood the examples of the “power switch controller PSC” at Figures 25-30 likewise employ a state machine to control transitions between standby and operational states. MTK-1005, [0102]-[0107]; MTK-1003, ¶¶315-18.

The threshold voltage of the “power switch PSW1” depends on the structure and process used. MTK-1005, [0090]; MTK-1003, ¶¶324-326. For example, to balance the “tradeoffs” between the “on-resistance per surface area of power switch PSW1 during operation” and “gate tunneling leakage current” during standby, Mizuno proposes a structure with “a thick gate dielectric film for the MOS transistors comprising the power switch PSW1 compared to the MOS transistors comprising the circuit block CKT.” *Id.* Then, “PSWGATE1” is set to an optimum voltage that is sufficiently above or below the threshold voltage of the “power switch PSW1” such that the “on-resistance during operation can ... be reduced and a power switch with a sufficiently small leakage current during standby can be obtained.” *Id.*; *see also id.*, [0125]-[0126].

For example, during standby the current in “circuit block CKT” is dominated by the “current source PSW2,” such that “ $I_{\text{off}}(\text{PSW1}) \ll I_{\text{off}}(\text{PSW2})$.” MTK-1005, [0057], [0079]. “The condition $I_{\text{off}}(\text{PSW1}) \ll I(\text{PSW2})$ can be satisfied by selecting device parameters for the power switch PSW1 and the current source PSW2” and “overdriv[ing] the power switch PSW1 gate signal up to $V_{\text{DD}} + a$ during standby” as shown in Figures 12-13. MTK-1005, [0079].

FIG.12

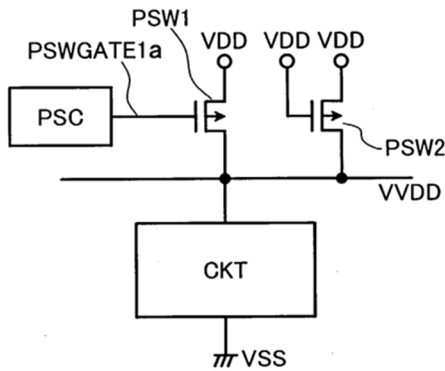
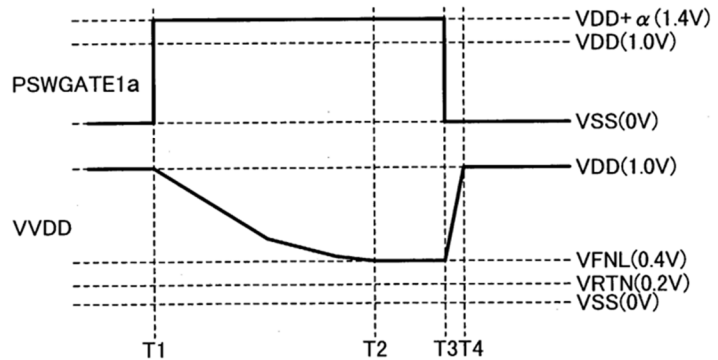


FIG.13



MTK-1005, FIGS. 12-13

By setting “PSWGATE” to the optimum level “VDD+α,” a “reverse bias voltage is ... applied across the source-drain of power switch PSW1 and the $I_{off}(PSW1)$ becomes small.” *Id.* Thus, a POSITA would have understood and found obvious that the variable voltage “PSWGATE” is an optimum voltage. MTK-1003, ¶¶323-327.

6. Claim 5

As discussed at Claim 4, Mizuno optimizes the variable “PSWGATE1” based on variations in the process used for the transistor in the “power switch PSW1.” MTK-1003, ¶¶328-335.

Moreover, as discussed at Claim 5 of Ground 1A, it was well-known that transistor performance is dependent upon process and temperature variations, and Mizuno itself discloses optimizing voltages to account for process and temperature

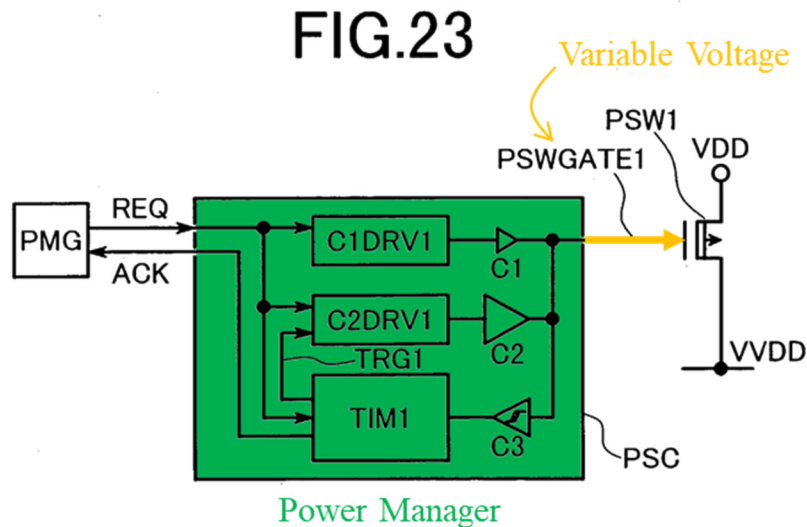
variations. *See, e.g.*, MTK-1005, [0064], [0076]-[0077] (adjusting “the substrate bias voltage value applied to the MOS transistor substrate ... according to the process, temperature and power supply voltage”), [0080]-[0081], [0086] (adjusting “output voltage VFNL ... according to the power supply VDD voltage, temperature and process conditions, etc.”), [0126] (“[t]he virtual power line VVDD2a or VVDD2b voltages can also be changed based on the information on variations (non-uniformities) in chip manufacture or information on environmental fluctuations”), [0128]; MTK-1003, ¶¶331-332.

A POSITA therefore would have found it obvious to optimize the “PSWGATE1” and other voltages generated by the “PSC” and provided to the “power switch PSW1” based on process and temperature variations. MTK-1005, [0090]-[0091] (describing a structure for “PSW1” and “PSW2” in which “the leakage current flow in the circuit block during standby due to process variations can also be reduced”); MTK-1003, ¶¶331-335.

7. Claim 6

Mizuno’s “PSC” generates an optimum voltage “PSWGATE1” to turn the “power switch PSW1” off during a standby mode. MTK-1003, ¶¶336-337. As shown in Figure 23, for example, during standby the “gate signal PSWGATE1” is “first of all driven to high impedance by C1, by way of the C1DRV control circuit for C1.” MTK-1005, [0098]. Then, once “potential detector C3 detects that the

gate signal PSWGATE1 was driven to a level V_{th2} ,” the “PSWGATE1 is ...
driven to a low impedance by C2 by way of the C2DRV control circuit for C2.”
Id.; see also *id.*, [0095], [0103]-[0106].



MTK-1005, FIG. 23

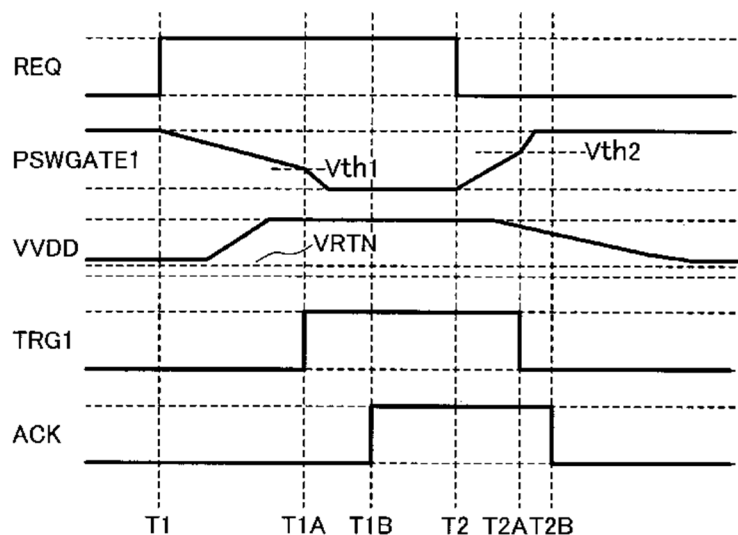
In the related embodiment of Figures 35-40, Mizuno discloses that the voltage VVDD2a provided to “power switch PSW1” is generated by “power switch PSW1s.” MTK-1005, FIGS. 27-30, 38; MTK-1003, ¶¶338-339.

Thus, a POSITA would have understood and found obvious that Mizuno’s “PSC” includes a sleep generator for providing optimum voltages to the at least one low leakage sleep circuits during standby. MTK-1003, ¶¶338-341.

8. Claim 7

Mizuno discloses that the control signal “REQ” is a digital control signal that takes one of two levels, as shown, for example, in Figure 24. MTK-1005, [0093], FIGS. 24, 26, 28, 30; MTK-1003, ¶¶342-346.

FIG.24



MTK-1005, FIG. 24

Specifically, setting “REQ” to the “high level turns on the power switch PSW1 and controls the circuit block CKT in the operation state.” *Id.* “Conversely, when the request line REQ is set to low level, the power switch PSW1 turns off and the circuit block is controlled to the standby state.” *Id.* Thus, a POSITA would have understood that “REQ” (and the “equivalent” signals “CTL_a, CTL_b”) is a digital control signal, and otherwise would have found it obvious to use a

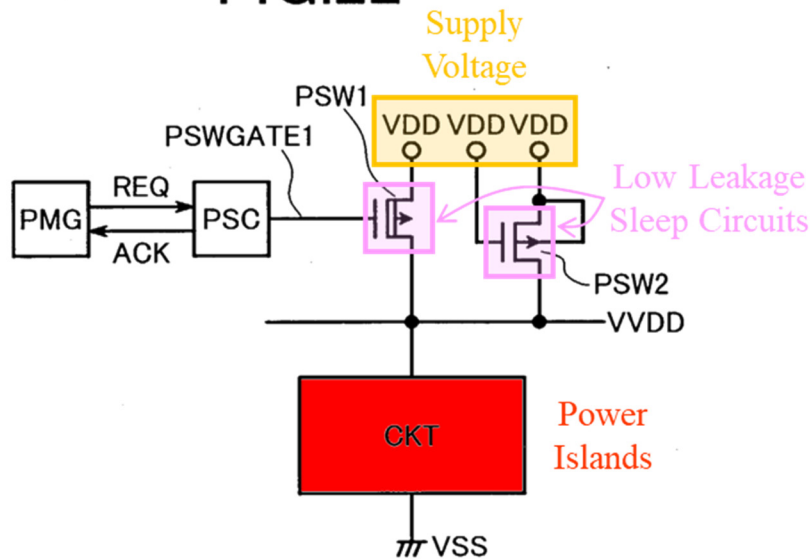
digital signal for the “request line REQ.” MTK-1003, ¶¶343-346; MTK-1015; MTK-1016.¹⁴

9. Claim 8

As explained at element 1[b], Mizuno’s “power switch PSW1” and “current source PSW2” are low leakage sleep circuits that are connected in series between a source of the “power supply VDD” and the “circuit block CKT.” MTK-1005, [0054] (“the voltage of the power supply VDD is the circuit block C operating voltage and is supplied from a stable power supply circuit”), [0093]; MTK-1003, ¶¶347-349.

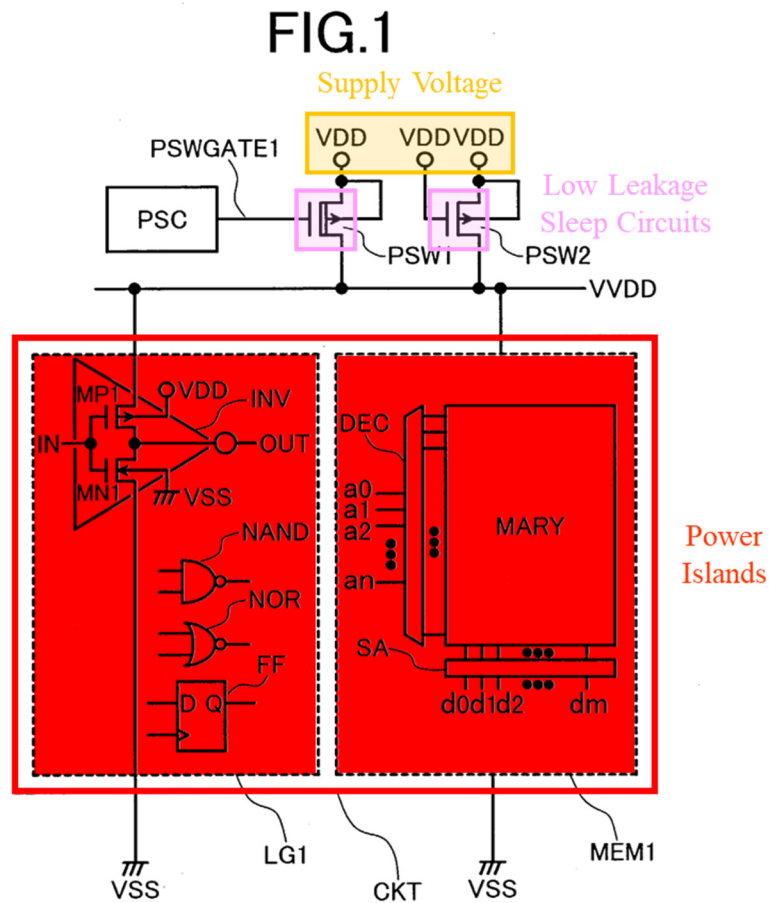
¹⁴ As explained at Claim 8 of Ground 1A, all electrical signals are either digital or analog, such that it also would have been obvious to a POSITA to use a digital signal for “REQ” as one of a finite set of two available options.

FIG.22



MTK-1005, FIG. 22; *see also* FIG. 38

The “circuit block CKT” contains “a logic circuit LG1” and a “memory MEM1.” MTK-1005, [0053]. The “logic circuit LG1” has logic gates including “an inverter INV, a NAND circuit NAND, a NOR circuit NOR and a flip-flop circuit FF,” and the “memory MEM1” includes “a memory cell array MARY.” *Id.*; MTK-1003, ¶¶350-352.

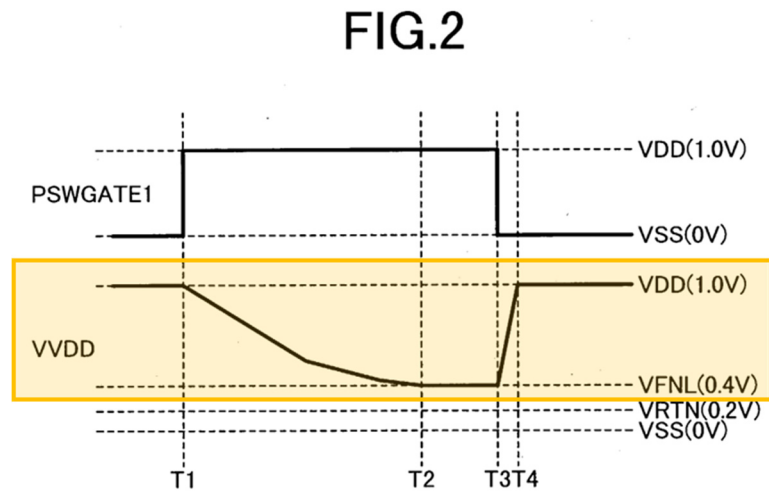


MTK-1005, FIG. 1

10. Claim 9

Mizuno’s low leakage sleep circuits “power switch PSW1” and “current source PSW2” cause the voltage “VVDD” supplied to the “circuit block CKT” to decrease during standby (“sleep”) mode. MTK-1005, [0054]-[0055], [0093]-[0106]; MTK-1003, ¶¶353-356. When the “power switch PSW1” is turned on, “the virtual power line VVDD reaches VDD potential and the circuit block CKT is operable (in operating state).” MTK-1005, [0055]. Conversely, when the “power

switch PSW1 turns off,” the “voltage (or voltage potential) of virtual power line VVDD gradually discharges” until “reach[ing] the final converging stable voltage level VFNL.” *Id.*; *see also id.*, [0125]-[0130] (addressing the virtual power line in Figures 35-40).



MTK-1005, FIG. 2

11. Claim 10

(a) Element 10[p]

Supra 1[p] and 1[b]. MTK-1003, ¶357.

(b) Element 10[a]

Supra 1[a]. MTK-1003, ¶358.

(c) Element 10[b]

Supra 1[b]. MTK-1003, ¶359.

(d) Element 10[c]

As explained with respect to element 1[b], each of Mizuno's low leakage sleep circuits including "power switch PSW1" and "current source PSW2" is associated with a leakage reduction of a power island such as the "circuit block CKT," or the "logic circuit LG1" and "memory MEM1" contained therein. MTK-1003, ¶¶360-366. Specifically, as the "power switch PSW1" and "current source PSW2" reduce the voltage "VVDD" during standby, the leakage current "I_{off}(CKT) ... also gradually becomes a smaller value." MTK-1005, [0055]; MTK-1003, ¶¶362-363. Thus, "power consumption due to leakage current in the circuit block during the standby state can be greatly reduced." MTK-1005, [0087].

Similarly, the related embodiment of Figures 35-40 discloses an integrated circuit with multiple "leakage reduction circuits PSM2a and PSM2b" that control power to corresponding power island "[c]ircuit blocks CK2a and CKT2b." MTK-1005, [0121]; MTK-1003, ¶¶364-365. The "leakage reduction circuits PSM2a and PSM2b" include low leakage sleep circuits similar to those of the embodiment in Figures 1-30. MTK-1005, [0130]; FIG. 38 (depicting a "leakage reduction circuit" PSM2a or PSM2b with a "power switch PSW1" and "current source PSW2"); MTK-1003, ¶365. Each of the "leakage reduction circuits" is associated with a leakage reduction of its respective circuit block so that "the leakage current of the

overall chip can be efficiently reduced.” MTK-1005, [0122]; MTK-1003, ¶¶365-367.

12. Claim 11

Supra Claim 2 and 10[p]-10[c]. MTK-1003, ¶368.

13. Claim 12

Supra Claim 3, 10[p]-10[c], and Claim 11. MTK-1003, ¶369.

14. Claim 13

Supra Claim 4 and 10[p]-10[c]. MTK-1003, ¶370.

15. Claim 14

Supra Claim 5, 10[p]-10[c], and Claim 13. MTK-1003, ¶371.

16. Claim 15

Supra Claim 6, 10[p]-10[c], and Claim 13. MTK-1003, ¶372.

17. Claim 16

Supra Claim 7 and 10[p]-10[c]. MTK-1003, ¶373.

18. Claim 17

Supra Claim 8 and 10[p]-10[c]. MTK-1003, ¶374.

19. Claim 18

Supra Claim 9, 10[p]-10[c], and Claim 17. MTK-1003, ¶375.

E. GROUND 2B—CLAIMS 3 AND 12 ARE OBVIOUS OVER MIZUNO IN VIEW OF KO

1. Mizuno-Ko Combination

A POSITA would have been motivated to modify Mizuno's integrated circuit to incorporate the teachings of Ko with a reasonable expectation of success. MTK-1003, ¶¶376-393. Both Mizuno and Ko are directed to reducing power consumption in integrated circuits, including power consumption due to leakage currents during standby. MTK-1005, Abstract, [0009] ("The present invention is therefore capable of reducing the different types of leakage current ... while the circuit block is in standby state"), [0087]-[0088], [0093], [0130]; MTK-1006, 1:14-17 (Ko's "invention relates ... to reducing leakage current in power-saving standby modes"), 3:7-34, 7:20-50, 9:2-4, 9:42-50; MTK-1003, ¶378.

Both are directed to retaining data in an integrated circuit during low-power standby states. MTK-1005, [0007], [0009], [0053], [0065]-[0066], [0087]-[0088] ("The present invention is characterized in that power consumption due to leakage current in the circuit block during the standby state can be greatly reduced while still maintaining (keeping) the information within the information retention circuits within the circuit block."), [0099]; MTK-1006, Title, Abstract ("[s]tate retention registers for use in low-power standby modes of digital IC operation are provided"), 4:8-13 (describing Ko's capability "to reduce the leakage current while the shadow latch is retaining data with the normal functional flip-flop circuitry powered-down"); MTK-1003, ¶379. The '077 Patent is directed to these same

fields of endeavor. *See* MTK-1001, Title, Abstract, 1:29-39; 2:24-50, 3:49-55; MTK-1003, ¶380.

Moreover, Mizuno and Ko address the same known problems in similar ways. MTK-1003, ¶381. As discussed above, both Mizuno and Ko reduce overall power consumption placing circuit blocks into a standby mode when idle. MTK-1005, [0054]-[0055], [0093], [0121]-[0122]; MTK-1006, 1:20-56, 2:63-3:6, 7:20-50; MTK-1003, ¶¶381-382. To do so, Mizuno and Ko both utilize MOS transistors (*e.g.*, the “power switch PSW1” of Mizuno and “header switch” of Ko) as switches to connect or disconnect the circuit blocks from a voltage supply. *Id.* Both Mizuno and Ko modify the voltages applied to the switching circuits and circuit blocks during operational and standby states to limit power consumption due to leakage currents. *Id.*

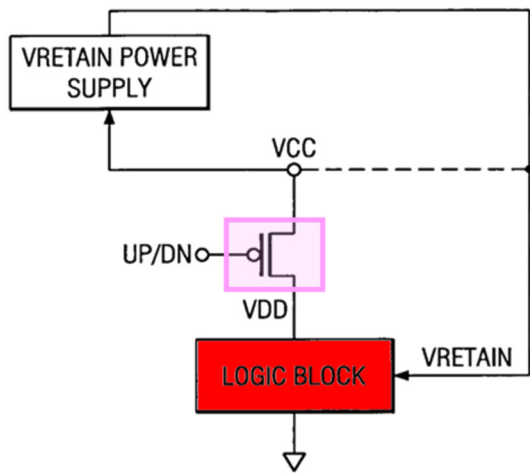


FIG. 1

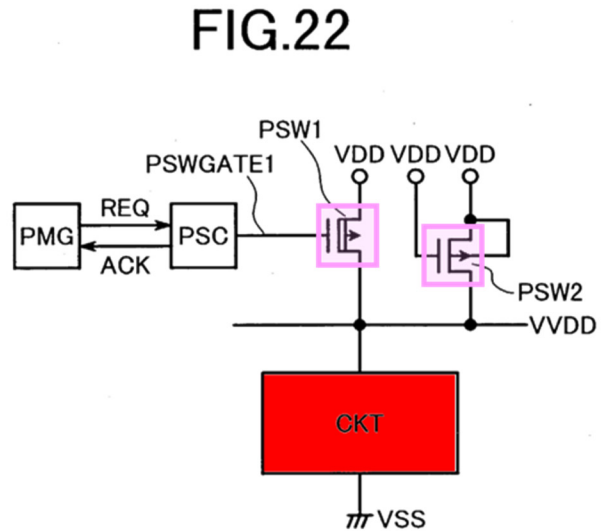


FIG. 22

MTK-1006, FIG. 1 (left); MTK-1005, FIG. 22 (right)

Mizuno and Ko also both provide for data retention functionality during low-power standby states by lowering the voltage to the circuit blocks to an optimum level. MTK-1005, [0003], [0065], [0087], [0099], MTK-1003, ¶¶383-384. “[T]o retain information stored within the information holding circuit within the circuit block CKT,” Mizuno lowers the voltage to the “circuit block CKT” to the “voltage value VFNL ... [that is] higher than voltage VRTN which is the minimum voltage capable of retaining information stored within the information holding circuit.” MTK-1005, [0065]. Similarly, Ko provides a “separate power supply VRETAIN” set to a level capable of powering data retention “shadow latches” during a “low-power standby mode.” MTK-1006, Abstract, 3:21-24; MTK-1003, ¶384.

These similarities between Mizuno and Ko would have led a POSITA to employ Ko's state machine with Mizuno's "PSC." MTK-1003, ¶¶385-390. To control putting "circuit block CKT" into standby or operational mode, Mizuno's "PSC" generates a variable voltage "PSWGATE1" that controls the on or off status of the "power switch PSW1" responsible for providing power to the "circuit block CKT." MTK-1005, [0055], [0093]-[0107]. To do so, the "PSC" employs specific combinations of control circuits (*e.g.*, "C1DRV," "C2DRV"), drive circuits (*e.g.*, "C1," "C2"), a timer (*e.g.*, "TM1"), a voltage potential detector (*e.g.*, "C3," "SENS1," "SENS2"), and/or a power switch (*e.g.*, "PSW1s"). MTK-1005, [0093]-[0107], FIGS. 22-30, 38; MTK-1003, ¶387. Mizuno utilizes this configuration so that "coupling noise from the virtual power line VVDD is reduced and the information within the information retention circuits can be prevented from being destroyed" as the "circuit block CKT" transitions between standby and operational states. MTK-1005, [0099]-[0101]. A POSITA would have understood that Mizuno's approach to controlling the transition between standby and operational states is merely one design chosen from a finite number of known solutions. MTK-1003, ¶¶388-389.

A POSITA would have further understood that Ko discloses another solution for putting circuit blocks to sleep and taking them out of sleep. MTK-1006, 7:20-50; MTK-1003, ¶389. Specifically, Ko's "power state controller 45 ... utilizes

state machines to provide appropriate control signals to the header switches and logic modules” to put the “logic modules” into standby or operational states. *Id.* Figures 5 and 13 illustrate “the timing relationships of the control signals produced by the power state controller 45” to ensure that data is not lost when putting a logic module into the “low-power standby (state retention) mode” and to restore data when entering an operational mode. MTK-1006, 7:51-55, 11:9-29; MTK-1003, ¶389.

Because Mizuno and Ko provide a similar solution to a similar problem within the same field of endeavor, a POSITA would have naturally looked at, and been motivated to combine, the two references when selecting a method for putting a circuit block into a standby or operational mode. MTK-1003, ¶¶390-391. A POSITA would have understood that Mizuno’s “PSC” could employ Ko’s “state machines” to control the “gate signal PSWGATE1 so the slew rate is reduced” when transitioning the “circuit block CKT” between standby and operational modes. MTK-1003, ¶¶390-391. Doing so would have been a mere design choice that was both obvious to try and would have yielded predictable results. MTK-

1003, ¶¶390-391.¹⁵ Modifying Mizuno’s “PSC” to employ a state machine would have required merely routine electrical or computer programming knowledge and was a task well within the skill of a POSITA. MTK-1003, ¶¶390-391.

A POSITA would have been motivated to employ Ko’s state machine to control the putting to sleep and taking out of sleep because a state machine requires less circuit area to implement and is less susceptible to processing and temperature variations. MTK-1003, ¶391. Mizuno acknowledges that “surface area overhead” was a design concern, and a POSITA would have been motivated to implement Ko’s state machine to reduce the “surface area” of the “PSC.” MTK-1003, ¶391. For example, in the embodiment of Figures 35-40, the separate “power switch controller[s] PSC” in the “leakage reduction circuits PSM2a and PSM2b” would be replaced by a single state machine capable, as taught by Ko, of controlling the states of multiple power islands (*e.g.*, “circuit blocks CKT2a and CKT2b”). MTK-1005, [0121]; MTK-1006, 7:38-42; MTK-1003, ¶391. Moreover, because Mizuno’s “PSC” implements an analog solution for controlling the timing of voltage changes to “PSWGATE1,” a POSITA would understand that the

¹⁵ As explained at Ground 2A, Mizuno alone discloses and renders obvious employing a state machine. To the extent that Mizuno fails to do so, Mizuno in combination with Ko renders Claim 3.

“PSWGATE1” signal is susceptible to process and temperature variations. MTK-1003, ¶392. A POSITA would have been motivated to utilize Ko’s “state machine” as an alternative design to Mizuno’s because Ko’s “state machine” is a digital circuit that is less susceptible to environmental and process variations. MTK-1003, ¶¶391-393. Thus, a POSITA would have been motivated to implement Ko’s “state machine” to obtain these benefits over the circuitry employed by Mizuno’s “PSC.” MTK-1003, ¶¶391-393.

2. Claim 3

The Mizuno-Ko combination renders obvious Claim 3. MTK-1003, ¶¶394-396. As explained at Claim 3 of Ground 1B, Ko employs “state machines to provide appropriate control signals to the header switches and logic modules” to power-up or power-down specific logic modules as needed. MTK-1006, 7:20-50, 9:42-50; MTK-1003, ¶395.

From Ko’s teachings, a POSITA would have found it obvious for Mizuno’s “PSC” to employ Ko’s state machine to control the putting to sleep and taking out of sleep of power islands. For instance, a POSITA would have been motivated to substitute Mizuno’s “PSC” circuitry (*e.g.*, as shown in Figure 23) with Ko’s “state machine” to reduce the “surface area overhead” of the “PSC” and reduce its susceptibility to environmental and process variations. MTK-1005, [0093]-[0107]; MTK-1003, ¶396.

A POSITA would have had a reasonable expectation of success in combining Ko with Mizuno, because the combination would represent a simple integration of Ko's "state machine" into Mizuno's system for controlling the putting to sleep and taking out of sleep of Mizuno's power islands. MTK-1003, ¶397. Employing Ko's "state machine" would have required merely routine electrical or computer programming knowledge and was a task well within the skill of a POSITA. *Id.* Incorporating Ko's "state machine" would predictably reduce the size of Mizuno's low leakage mechanism and increase its ability to transition the "circuit block CKT" between standby and operational states without data loss. MTK-1005, [0099]-[0101]; MTK-1003, ¶¶397-398.

3. Claim 12

Supra Claim 3. MTK-1003, ¶399.

IV. THE BOARD SHOULD CONSIDER THE PETITION ON THE MERITS

A. Discretionary Denial under Section 325(d) Is Not Warranted

Advanced Bionics and the *Becton* factors favor institution. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020) (precedential); *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017) (precedential as to §III.C.5, first paragraph).

Advanced Bionics Part 1—No rejection over prior art was issued during prosecution. *See generally* MTK-1002. The references relied upon here were not cited by the examiner, and are not listed on the face of the '077 Patent. *See generally* MTK-1001, MTK-1002. Thus, there is no indication that the examiner substantively considered any references, and the Petition's art and arguments are not the same as, or substantially similar to, those previously presented to the Office for the '077 Patent. *Id.* Accordingly, neither condition of the first prong of the *Advanced Bionics* framework is met.

Becton factors [a], [b], and [d] further favor institution. None of Takahashi, Mizuno, Ko, and Schutz were addressed during prosecution ([a]), nor are they cumulative of other art relied on or considered by the examiner ([b]). *Id.* There

are also no overlapping arguments ([d]) between the prosecution record and the Grounds above. Thus, *Becton* factors [a], [b], and [d] favor Petitioner.

Advanced Bionics Part 2—The Board need not reach the second prong under §325(d), since the first prong is not satisfied. *See Oticon Med. AB et. al. v. Cochlear Ltd.*, IPR2019-00975, Paper 15 at 20 (PTAB Oct. 16, 2019) (precedential) (no discretionary denial under §325(d) because of “new, noncumulative prior art asserted in the Petition”). Nonetheless, each *Becton* factor [c], [e], and [f] favors Petitioner. None of Takahashi, Mizuno, Ko, or Schutz was cited during prosecution, and did not form the basis of any rejection ([c]). As for [e] and [f], by not considering Takahashi, Mizuno, Ko, Schutz, or combinations based on them, the Office erred in its evaluation of the prior art, thus warranting reconsideration. *Advanced Bionics*, Paper 6, 10. The Grounds above demonstrate why further consideration is warranted.

B. Discretionary Denial under Section 314(a) Is Not Warranted

In *General Plastic Indus. Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357—01361, Paper 19 at 9-10 (PTAB Sept. 6, 2017) (precedential), the Board identified seven factors that inform application of discretionary denials under §314(a). Given this is the first ever petition filed against the '077 Patent, these factors do not apply. *See Acronis, Inc. v. Realtime Data LLC*, IPR2018-00706, Paper 11, 15-16 (Oct. 1, 2018).

C. The *Fintiv* Factors Weigh Against Discretionary Denial

In *Apple Inc. v. Fintiv, Inc.*, the Board enumerated six factors to determine whether a petition should be discretionarily denied institution under §314(a). IPR2020-00019, Paper 11 at 2-3 (Mar. 20, 2020) (precedential) (“*Fintiv*”). In June 2022, the USPTO issued updated guidance on the *Fintiv* factors and expressly noted that ***the PTAB will not discretionarily deny institution if Petitioner presents a Sotera stipulation.*** MTK-1022. Here, Petitioner eliminated any risk of duplicated effort by voluntarily presenting a *Sotera* stipulation. MTK-1023; *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (Dec. 1, 2020). For at least this reason, the Board should not discretionarily deny this petition.

V. CONCLUSION

As demonstrated herein, the Challenged Claims are unpatentable. Accordingly, Petitioner respectfully requests that the Board institute IPR.

VI. PAYMENT OF FEES

Petitioner authorizes charge of fees to Deposit Account 06-1050.

VII. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(A)(1)

A. Real Party-in-Interest under 37 C.F.R. § 42.8(b)(1)

MediaTek Inc. is petitioner and real party-in-interest. MediaTek USA Inc. is an additional real party-in-interest. No other parties had access to or control over the present Petition, and no other parties funded the present Petition.

B. Related Matters under 37 C.F.R. § 42.8(b)(2)

MOSAID—the alleged Patent Owner—filed a complaint asserting the '077 Patent against Petitioner on March 28, 2023 in the U.S. District Court for the Eastern District of Texas (Case No. 2:23-CV-00129).

C. Lead and Back-Up Counsel under 37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

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D. Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR44508-0023IP3@fr.com.

Respectfully submitted,

Dated: March 6, 2024

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CERTIFICATION UNDER 37 C.F.R. § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,992 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated: March 6, 2024

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) et seq. and 42.105(b), the undersigned certifies that on March 6, 2024, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided via Federal Express, to the Patent Owner by serving the correspondence address of record as follows:

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