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HIGH ELECTRON MOBILITY TRANSISTOR STRUCTURES IN THE
GALLIUM ARSENIDE AND GALLIUM NITRIDE MATERIAL SYSTEMS BY
ORGANOMETALLIC VAPOR PHASE EPITAXY

A Dissertation
Presented to the Faculty of the Graduate School
of Cornell University
in Partial Fulfillment of the Requirement for the Degree of
Doctor of Philosophy

by
Joseph A. Smart
May 2006

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BIOGRAPHICAL SKETCH

The author, Joseph A. Smart, was born on 01 April 1965 in Auburn, New York. He was raised in traditional neighborhood where he learned the importance of family values. He received his bachelor's degree in Electrical Engineering from SUNY Center at Binghamton in 1987. After working in the semiconductor industry for over seven years, he decided to return to academic studies for advance degrees in the fall of 1995 at Cornell University. In early 2000, he took a leave of absence from Cornell and was one of the co-founders of RF Nitro Communications, Inc., a semiconductor company started to commercialized GaN and GaAs based high power transistors. Joseph was the VP of Advance Technologies and then Director of GaN Technology after the company was acquired by RF Micro Devices in fall of 2001. After building the GaN facility in Charlotte, NC, Joseph returned to Cornell in Spring 2005 to complete his Ph.D. requirements. He will then pursue a challenging career in materials, and hopefully never stop learning.

Dedicated to two of my best friends.....

Mom and Dad

To my parents

"How could a blade of grass repay the warmth from the spring sun"

- Meng Chio (751-814)

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LIST OF ABBREVIATIONS AND SYMBOLS

2DEG	2 Dimensional Electron Gas
2-D	Two Dimensional
3-D	Three Dimensional
ΔE_c	Conduction Band Discontinuity
Al_2O_3	Aluminum Oxide (sapphire)
AsH_3	Arsine
AXT	American Crystal Technology
C-V	Capacitance-Voltage
DI	Deionized
ELO	Epitaxial Lateral Overgrowth
FME	Flow Modulation Epitaxy
HEMT	High Electron Mobility Transistor
LPM	Liters per Minute
LT	Low Temperature
NH_3	Ammonia
OMVPE	Organometallic Vapor Phase Epitaxy
PL	Photoluminescence
PH_3	Phosphine
RBS	Rutherford Back Scattering
RLP	Reciprocal Lattice Point
SEM	Scanning Electron Microscopy
SiH_4	Silane
SIMS	Secondary Ion Mass Spectroscopy

TEG	Triethylgallium
TEM	Transmission Electron Microscopy
TMA	Trimethylaluminum
TMI	Trimethylindium
TMG	Trimethylgallium

CHAPTER 1

INTRODUCTION

1.1 Introduction

Over the past several decades, significant advances have been made in epitaxial growth of compound semiconductors, to the point of obtaining control to the atomic scale. As a result, more complicated structures exploiting unique physical properties can be realized, such as the high electron mobility transistor (HEMT). This device utilizes a two-dimensional electron gas (2DEG) residing in the lower band gap side of certain heterostructures, and was first discovered in the AlGaAs/GaAs system in 1978 [1]. The donors supplying the electrons to the 2DEG could be remotely located in the higher band gap material, thereby reducing the effects of ionized impurity scattering. This increases the low field electron mobility within the channel, resulting in lower channel resistances. In 1985, the AlGaAs/GaAs HEMT structure was modified, incorporating a pseudomorphic GaInAs channel [2,3]. Due to the higher electron mobility and saturation velocity in the GaInAs layer, pseudomorphic HEMT's demonstrated improved power gain and low-noise performance at high frequencies [4]. Further improvements investigated in this work involve replacing AlGaAs with GaInP, and developing atomic planar doping techniques for the supply layer. With knowledge gained from the

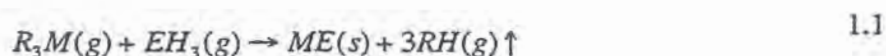
GaInP/GaAs work, transistor structures were then grown in the AlGaIn/GaN material system. This system has demonstrated great potential for high temperature, frequency and power density applications.

The main focus of the work presented in this thesis is the epitaxial growth of HEMT structures using novel organometallic vapor phase epitaxy techniques. In this chapter, background and motivation for this work is presented. The flow modulation growth process employed is introduced in Section 1.2 along with a description of the two epitaxial growth reactors used in Section 1.3. Motivation for the growth of GaInP/GaAs and AlGaIn/GaN based HEMT structure is discussed in Section 1.4. Finally, a synopsis of the thesis work is given in Section 1.5

1.2 Organometallic Vapor Phase Epitaxy Process

The crystal growth method employed is referred to as organometallic vapor phase epitaxy (OMVPE). This growth process typically uses metal alkyl (methyl and ethyl derivatives) precursors for the group III sources and hydride precursors for the group V sources [5-9]. The detailed nature of the chemical reactions occurring during OMVPE growth is still not well known. The specific reaction kinetics and thermodynamics are dependent on the precursors used, as well as the growth pressures, temperatures, carrier gases and reaction cell geometries [10]. In addition, hydrodynamics can play a strong role in the growth process at the higher temperatures employed, especially with GaN epitaxy. These complex processes contribute to the general lack of detailed understanding of the growth process. However, the

net reaction for growth of III-V binary compounds is usually pyrolysis-driven reactions of the form: [11-13]



where M is the Column III metal species (Al, Ga, or In), R is the organic radical (CH₃ or C₂H₅), and E is the Column V species (N, As, or P).

Equation 1.1 expresses the overall reaction; it ignores intermediate steps or additional compound formations that might occur. However, it provides a foundation to describe more complicated cases where more than one organometallic or hydride is used [14].

OMVPE growth rates have been shown to depend on growth temperatures. Over the typical temperature range encountered, there are three growth-rate-limiting mechanisms corresponding to distinct regions as shown in Figure 1.1 (a) and (b) [15]. The exact temperature boundaries and activation energies are process and reactor dependent, but the general behavior is universal to the OMVPE process. In the case of GaAs growth, at low temperatures the growth rate is kinetically limited, showing strong exponential temperature dependence. Growth rates in the intermediate temperature region is limited by diffusion, or mass-transport of the group III species from the gas phase through the boundary layer to the growth surface. Rates in this region are relatively insensitive to growth temperatures, and are linearly dependent on the total group III flux. At high

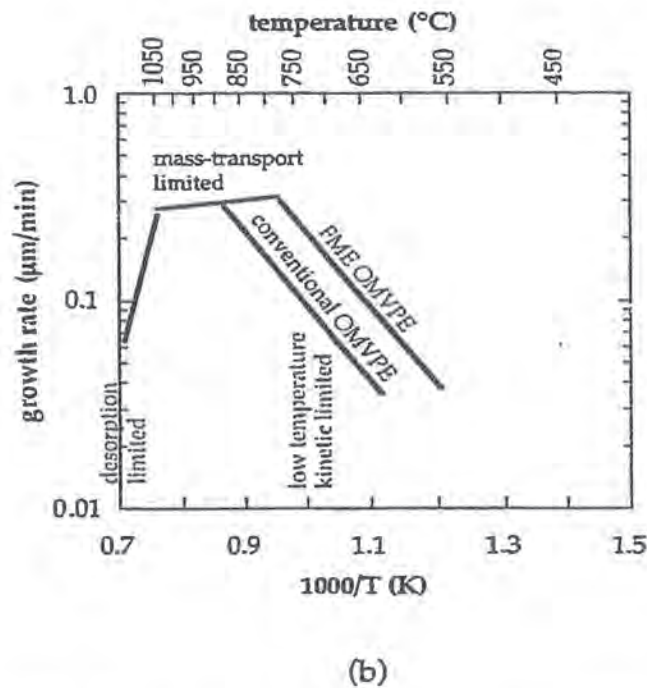
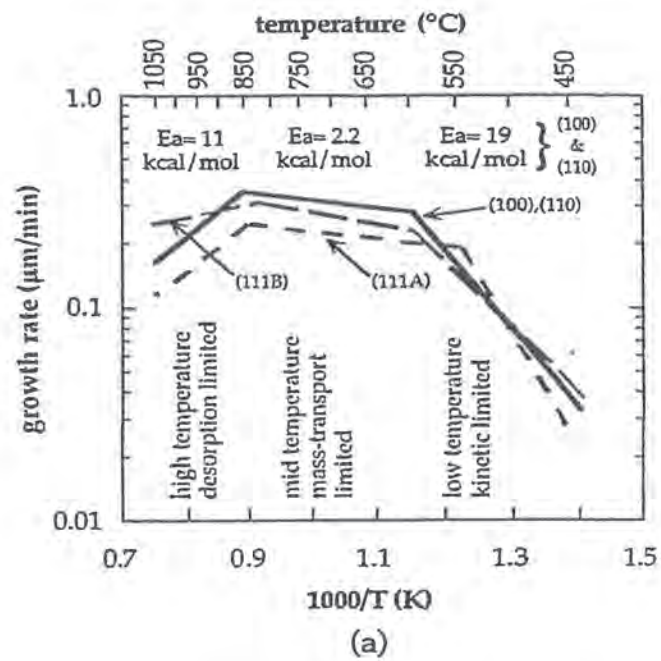
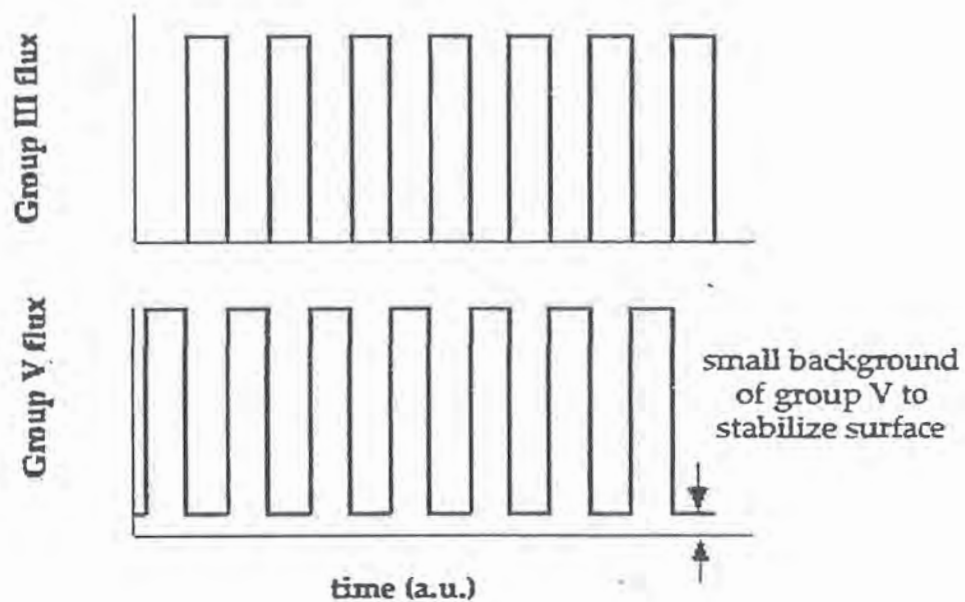


Figure 1.1 Growth rate vs. inverse temperature for GaAs using TEG and arsine (a). Three distinct regions are indicated corresponding to different growth-rate-limiting mechanisms (after [15]). Similar growth rate profiles are observed with GaN (b)

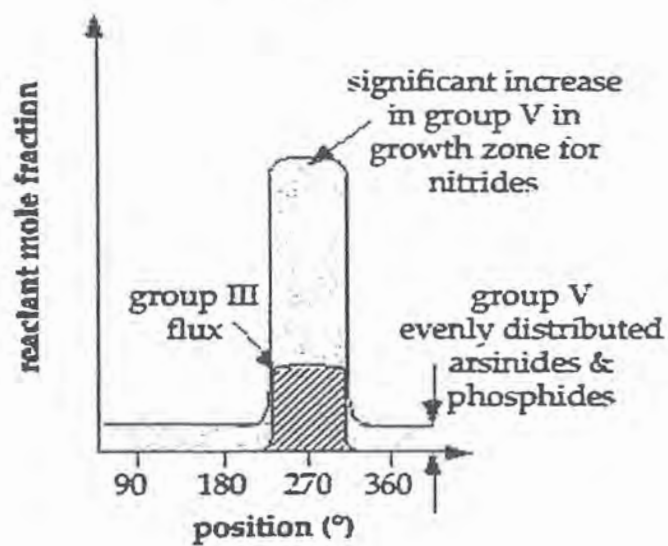
temperatures, desorption of the group III atom from the surface limits the growth rate. As expected, the growth rate in this regime is proportional to the group III flux. This same effect is observed in OMVPE growth of group III-nitrides as shown in Figure 1.1 (b). Unfortunately the mass transport limited temperature regime in GaN is very narrow for device quality material, making the temperature control and measurement a critical system requirement in GaN epitaxial growth reaction cells.

All three of these regions are encountered for epitaxial growth of HEMT structures for this work. Separate device layers within GaInP/GaAs-based transistors are grown in either the mass-transport, or kinetically limited regions depending on the structural and electrical properties desired. All GaN growth is carried out in or very near to the desorption limited regime, where the high temperature is required to decompose the ammonia adsorbed on the growth surface to produce high quality epitaxial material [16].

A variation in OMVPE growth technology known as flow-rate or flow modulation epitaxy (FME) has been developed which extends the low temperature end of the mass-transport limited regime [17-19]. Advantages of lower growth temperatures include more abrupt interface formation for heterostructures containing arsenide to phosphide transitions [20], and in the case of GaInP producing a higher degree of lattice disordering. Both of these qualities are desirable for GaInP/GaAs based HEMT's. The reactant flow profile for FME is illustrated in Figure 1.2. Substrates are subjected to a group III-rich cycle followed by a group V exposure. A small background of group V reactant is always present to stabilize the surface and prevent formation of vacancies on the group V sublattice, which differentiates this process from



(a)



(b)

Figure 1.2 Illustration of FME reactant flow profile, (a) for a switching scheme, and (b) by rotation of substrates through a group III rich growth zone

Atomic Layer Epitaxy. This advanced process is known to enhance the group III adatom surface migration length, by the presence of a metallic surface, and increases the growth rate at lower process temperatures [20]. FME techniques can be implemented by switching the reactants in-and-out of the growth chamber (Figure 1.2a), or by rotating the substrates through a group III and a group V rich growth zone (Figure 1.2b). The approach used for this work is to rotate through a group-III rich zone, which allows the process to be scalable for multi-wafer runs.

Organometallic precursors are generally transported to the reaction cell by a carrier gas, usually hydrogen. When the hydrogen gas is fully saturated with the organometallic vapor, the reactant flux can be calculated by applying Dalton's law [21]:

$$f_{III} = \frac{f_{H_2}}{\frac{P}{VP_{OM}} - 1} \quad 1.2$$

where f_{H_2} is the hydrogen flow through the organometallic bubbler, P is the pressure above the organometallic melt, and VP_{OM} is the vapor pressure of the organometallic (see [22] for an extensive list of precursor properties).

The group V species (arsine, phosphine, or ammonia) are supplied as gas sources, and their flux can be directly calculated from the mass flow controller readings. An important growth parameter is the ratio between the group V and total group III flux, known as the gas phase stoichiometry or

simply the V/III ratio. This parameter can influence surface morphology, optical quality and background impurity concentration of epitaxial films [23].

Intentional n- and p-type doping is achieved by adding shallow impurities such as Si and Te for n-type, and C, Zn and Mg for p-type. Si is amphoteric and can occupy either a group III or V sub-lattice site (either n or p type dopant). With GaAs and GaInP, a high group V flux (V/III ratio) will "force" the Si into a group III site (n-type). At the growth temperatures and V/III ratios used for GaN growth, Si doping always results in n-type material.

1.3 Experimental Apparatus

Two unique, custom-build OMVPE growth reactors were used in this work. The cold-wall, quartz reaction cells have vertical barrel geometry with RF inductive heating of the graphite susceptor. The reactants are injected at the top of the cell, flow over the heated substrates (mounted on the susceptor), and exit at the bottom through vacuum ports. In both machines, FME techniques are achieved by rotation of the substrates through a group III rich growth zone(s).

1.3.1 Arsenide/Phosphide Reactor

The reactor that supported the arsenide and phosphide epitaxy consisted of two-growth-zones reaction. A top and side view schematic of the cell is shown in Figure 1.3. The susceptor has 3 rows with 6 pockets per row, able to accommodate up to eighteen small (1-3/8" on a side) substrates. From the top view, two growth zones are shown, 180° apart separated by high hydrogen flows (shown at 90° and 270°). Group III species are injected into the growth zones, while the arsine and phosphine are delivered uniformly

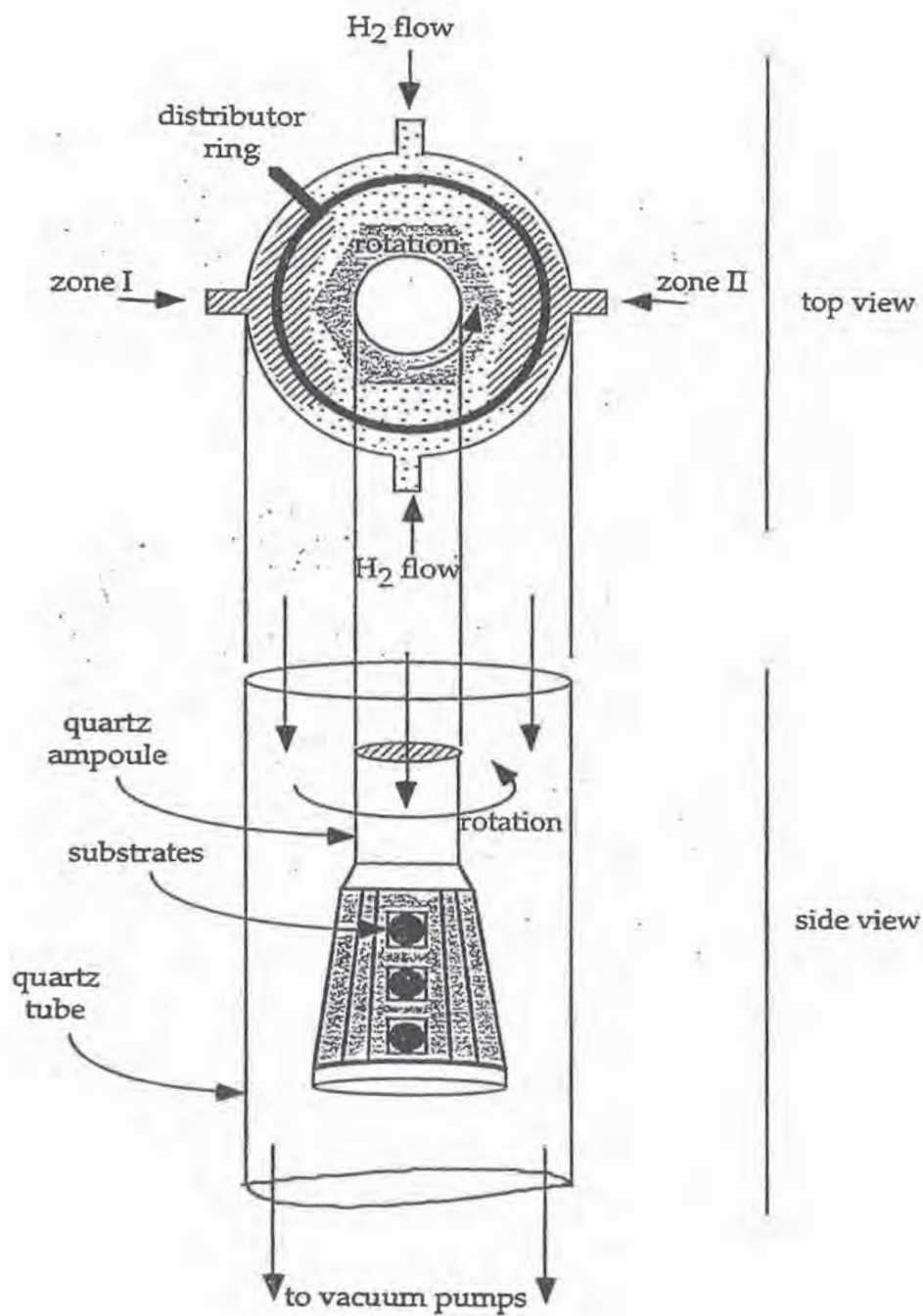


Figure 1.3 Schematic representation of reaction cell used for arsenide and phosphide growth.



Figure 1.4 Photograph of reaction cell used for arsenide and phosphide growth.

around the cell by the distributor ring. Good isolation between the growth zones has been demonstrated by parking the susceptor (no rotation) and monitoring growth rates on samples around the barrel [24]. Flow modulation is achieved by rotating the susceptor through the two different growth zones. Figure 1.4 is a photograph of the reaction cell clearly showing the external RF coil and the conical graphite susceptor.

1.3.2 Nitride Reactor

A four-growth zone reaction cell was built for III-Nitride epitaxial growth in this work. Acknowledgements for contribution in reactor design and building goes to Barry Butterfield, Dr. Keith Whittingham and Dr. David Emerson along with work in the scope of this dissertation and Professor J.R. Shealy. The growth zones are located 90° apart around the cell as shown in Figure 1.5 and isolated by large flows of a hydrogen/ammonia mixture. A "coaxial" tube-in-a-tube design was chosen to reduce the active volume of the cell and produce laminar flow over the substrate surface. The graphite susceptor accommodates up to eight 2-inch diameter substrates, which rotate through the various growth zones. By design, this growth technique is applicable to one or all eight substrates per process run. The photograph in Figure 1.6 shows the reaction cell with the eight 2-inch graphite susceptor. The process is scalable for larger diameter quartz tubes and susceptors able to handle larger diameter or more numerous substrates.

1.4 Motivation

Epitaxial material used for HEMT devices require not only high electron mobilities, but also large 2DEG sheet carrier densities (n_s) confined at the heterointerface. Maximizing the $\mu * n_s$ product results in the lowest

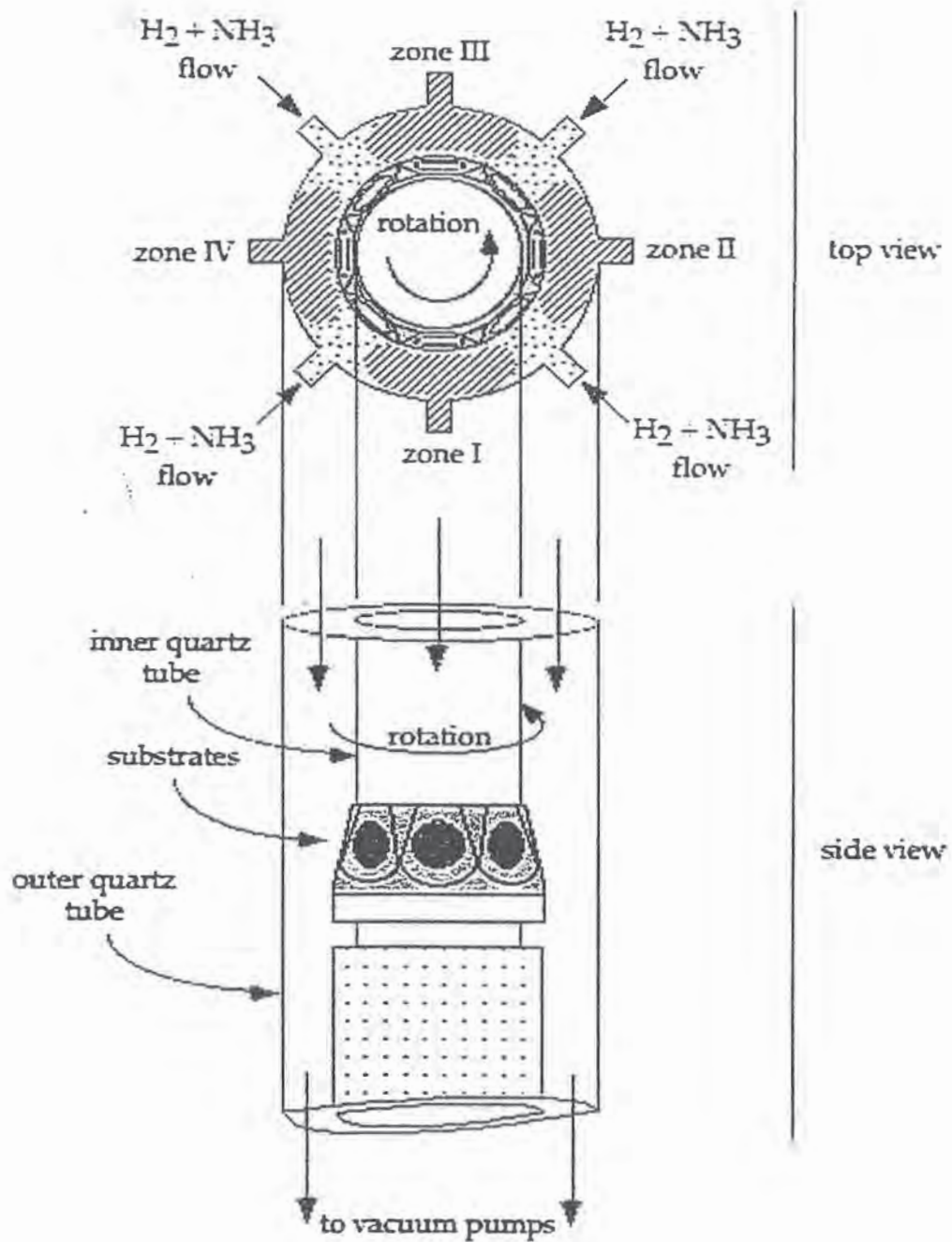


Figure 1.5 Schematic representation reaction cell used for nitride growth.

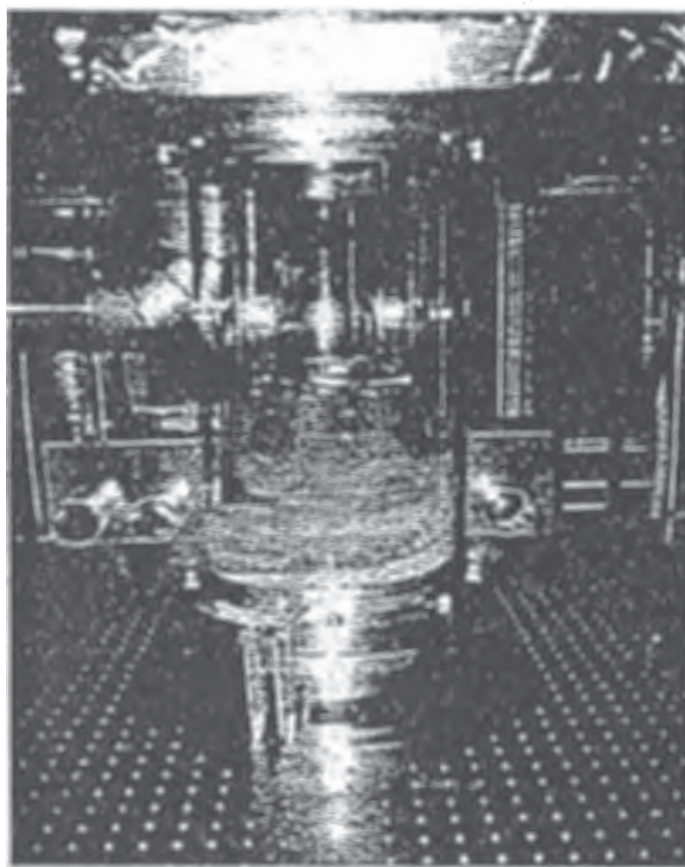


Figure 1.6 Photograph of reaction cell used for nitride growth.

channel resistance. Electron mobility in the channel is dependent on several mechanisms, such as phonon, ionized donor and crystal defect scattering as well as scattering from interface roughness. Room temperature 2DEG mobilities were optimized by producing smooth growth surfaces with very abrupt heterointerfaces. As the sheet density of the 2DEG increases, the strengthen electric field confines the carriers closer to the heterointerface, making interface roughness a more dominant effect on limiting room temperature mobility. Also, by increasing the conduction band discontinuity (ΔE_c) by compositional changes in the barrier, additional sub-bands in the quasi-triangular quantum well can fall below the Fermi level. The occupation of these additional bands can reduce mobility from intra-subband scattering. The key is band gap engineering of the conduction band to increase ΔE_c while still maintaining a smooth heterointerface and a deep quantum well with only the $n=1$ sub-band under the Fermi level.

Figure 1.7 gives mapping of band gap energies versus lattice constant for various III-V compounds. Assuming a type I heterostructure, it is seen that GaInP on GaAs as well as AlGaIn on GaN would produce sufficient conduction band offsets for use in HEMT devices. Furthermore, one can use pseudomorphic GaInAs as the channel material with a strain compensating GaInP barrier layer. Along the same lines, a GaInN channel could be used in the GaN system. This however was not attempted within the scope of this work due to the current difficulties of growing high quality GaInN thin films at the higher growth temperatures. Recent work indicates that the band gap for InN is at 0.65 eV (data point represented by the star) instead of the 1.79 eV commonly accepted.

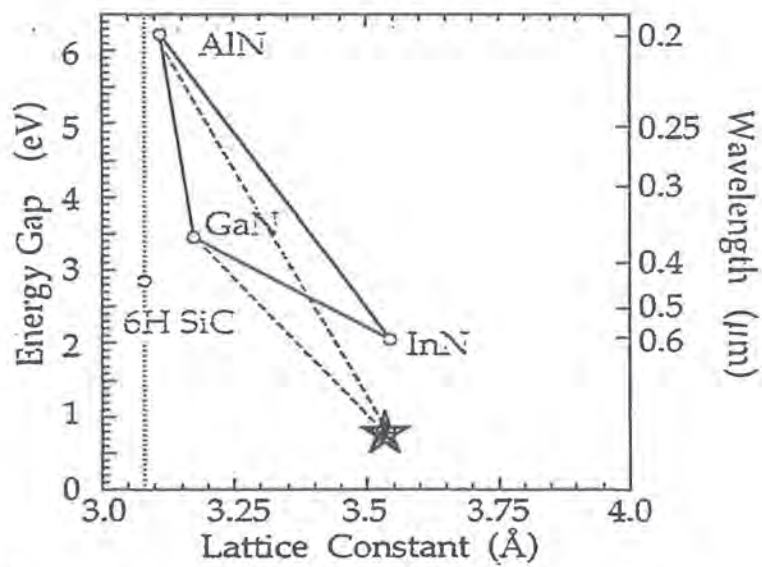
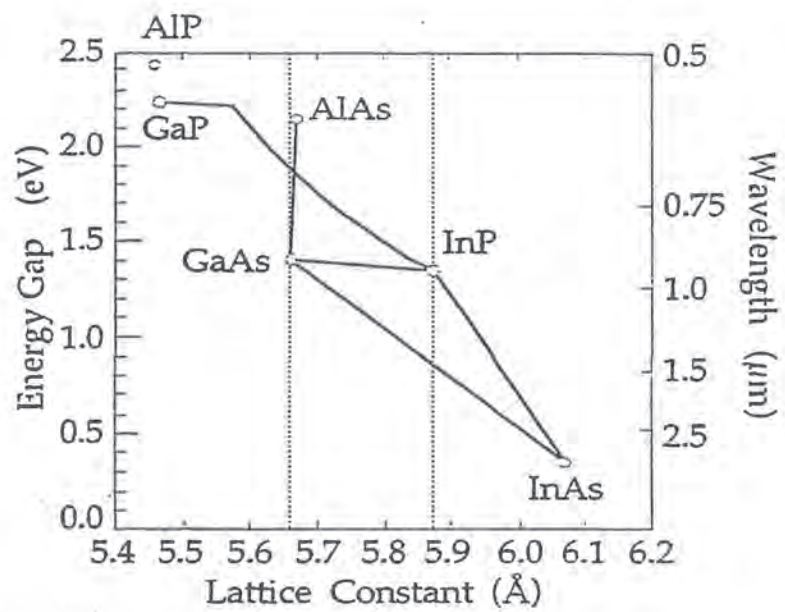


Figure 1.7 Band-gap versus lattice constant for common III/V compounds used in this work.

1.5 Dissertation Synopsis

This thesis encompasses epitaxial growth issues pertaining to transistor structures involving two entirely different material systems, namely GaAs and GaN. Where possible, the similarities are grouped together such as characterization methods used to analyze the materials as presented in Chapter 2. Chapter 3 discusses low temperature growth of GaAs, GaInP, and GaInAs used in latticed matched and pseudomorphic HEMT structures. Atomic planar doping (also known as delta doping) is also presented. Novel techniques were developed that utilizes multiple doping planes to achieve high sheet densities in the resulting 2DEG. Chapter 4 brings together all that was developed with the material studies in the previous chapter to grow complete GaAs-based HEMT transistor structures. Both latticed matched and pseudomorphic structures are addressed. Strain compensation was implemented using GaInAs channels with strained GaInP spacer, supply and barrier layers.

Growth of AlGaIn and GaN films are presented in Chapter 5. This chapter addresses nucleation strategies required to accommodate the serve mismatch between the GaN films and the SiC and sapphire substrates. Highly resistive GaN buffer layers were developed required for dc and RF transistor performance. Chapter 6 deals with the strong polarization fields present at the AlGaIn/GaN heterostructure and the concept of undoped structures. AlGaIn barrier growth is then discussed with emphasis on crystal quality and compositional and thickness control and uniformity. Lastly, reliability issues with associated with the AlGaIn barrier and device test results are given. Chapter 7 addresses future work and dissertation conclusion.

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CHAPTER 2

MATERIAL PROPERTIES AND CHARACTERIZATION METHODS USED TO ANALYZE EPITAXIAL LAYERS

2.1 Introduction

In this thesis, two separate III-V material systems were explored for the epitaxial growth of various HEMT structures. Within the GaAs system, latticed matched and/or strained $\text{Ga}_x\text{In}_{1-x}\text{P}$ films were used for the spacer, supply and barrier layers grown on either a GaAs or $\text{Ga}_y\text{In}_{1-y}\text{As}$ channel [1]. In GaN-based materials, thin AlGaN barriers were placed on top of highly resistive GaN buffer layers, forming a polarization-induced 2DEG at the heterostructure [2]. To analyze these structures, knowledge is required not only in numerical parameters, but in physical issues such as lattice ordering, strain, and polarization effects.

Characterization methods used to analyze transistor materials are briefly described in this chapter. The intent is to present calculations necessary for determining specific material properties, and not to provide a detailed description of the characterization method employed.

2.2 Material Properties

Numerical constants and physical properties are presented in this section for the GaAs and GaN material systems. In the GaAs-based system, discussion includes GaInP and GaInAs crystals used in the synthesis of

transistor structures. Similarly, AlGa_{0.5}N will be presented as well as GaN in the nitride section. Specific details on the growth conditions and experimental results are presented in the relevant chapters that follow.

2.2.1 GaAs - Based System

GaAs has a zincblende crystal structure consisting of two interpenetrating face center cubic sublattices, each containing atoms of only one type (either Ga or As). One atom of the second sublattice is located one-fourth of the distance along a major diagonal of the first, resulting in asymmetry. Each atom has four nearest neighbors belonging to a different sublattice giving a tetrahedral bonding configuration as illustrated in Figure 2.1 [3]. These Ga-As pairs enter into bonding, which is primarily covalent in nature, but also partly ionic. The As atom has higher electronegativity than the Ga, and the electron cloud shifts towards the As site. This charge transfer results in the semiconductor being polarized under electric fields. The polar axis for GaAs is along the [111] direction. Table 2.1 gives the numerical parameters for materials in the GaAs system used for calculations in this work [4-7].

With GaInP, the actual bandgap can be smaller than the nominal bandgap of 1.92 eV due to CuPt-type ordering on the group III sublattice. The difference in band gap between ordered and disordered GaInP can be as large as 150 meV [8]. It is generally accepted that the formation of ordered structures is related to surface processes during crystal growth, and depends strongly on various parameters such as growth temperatures, pressures, introduction of dopant species and substrate surface orientation [9]. Within the scope of this work, growth temperatures and substrate orientation were

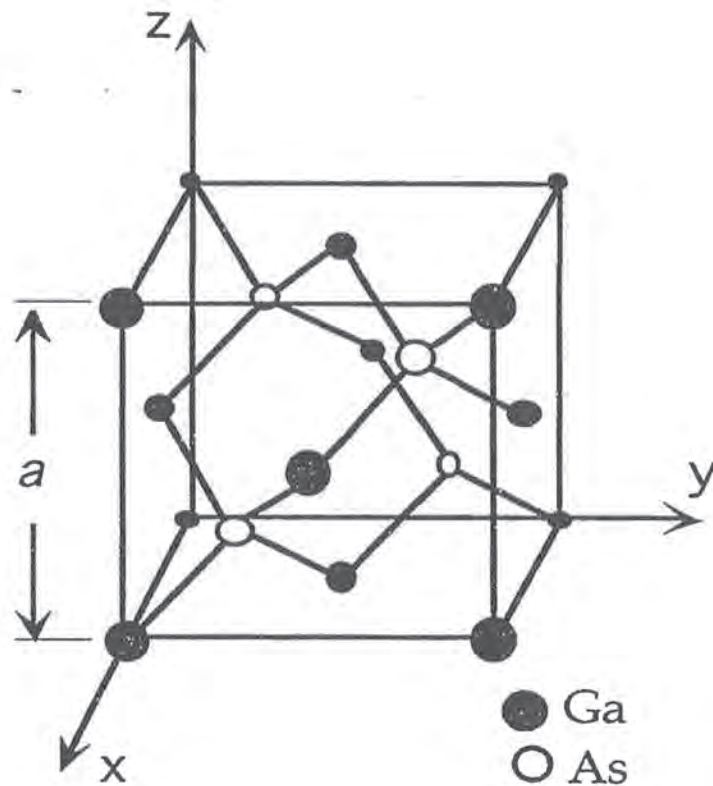


Figure 2.1 Schematic representation of a zincblende GaAs crystal.

investigated to achieve disordered GaInP as discussed in Chapter 3.

Table 2.1: Summary of pertinent numerical parameters of binary members in the GaAs system [4-7].

Parameter	Units	GaAs	InAs	InP	GaP
A_0	Å	5.6533	6.058	5.8686	5.4512
C_{11}	$\times 10^{11}$ dyn/cm ²	11.88	8.33	10.22	14.12
C_{12}	$\times 10^{11}$ dyn/cm ²	5.38	4.526	5.76	6.253
b	eV	-1.7	-1.8	-2.0	-1.5
$E_g(0)$	eV	1.52	0.41	1.42	2.9
$E_g(300)$	eV	1.441	0.36	1.34	2.742
N	—	3.3	3.995	3.03	3.0
ϵ_0	—	13.1	14.6	12.61	11.1

Since GaInAs is never latticed matched to GaAs (always in compression), when it is used for the channel layer, care must be taken not to exceed the critical thickness. Also, intentionally strained GaInP films (used for strain compensation or to increase the conduction band discontinuity) are limited in thickness before forming misfit dislocations. Theoretical calculations to estimate the critical thickness (h_c) are derived from either a force balancing [10], or energy balancing [11] models. Usually, these two

theories are considered very different from each other, yielding different values of h_c . However, it has been shown that the two theories are equivalent and give identical values for h_c if the same values of dislocation energy is used [12]. In this work, the commonly used "Matthews-Blakeslee" force-balanced equations will be used. For a single strained cubic layer, the critical thickness (h_c) can be expressed in the simplified form as [10]:

$$h_c = \left(\frac{a}{f} \right) \left(\frac{1}{4\pi\sqrt{2}} \right) \left(\frac{1-\frac{v}{4}}{1+v} \right) \ln \left(\frac{h_c\sqrt{2}}{a} \right) \quad 2.1$$

where a is the relaxed lattice constant of the ternary material determined from Vegard's law, f is the absolute value of the misfit strain between stress-free epitaxial layer and the substrate ($|a - a_0| / a_0$), and v is the Poisson ratio equal to $C_{12} / (C_{11} + C_{12})$.

For a multi-layer stack, with one layer mismatched and the other lattice matched, the critical thickness (h_c) is given by [13]:

$$h_c = \left(\frac{a}{f} \right) \left(\frac{1}{\pi\sqrt{2}} \right) \left(\frac{1-\frac{v}{4}}{1+v} \right) \ln \left(\frac{h_c\sqrt{2}}{a} + 1 \right) \quad 2.2$$

Equation (2.2) indicates that critical thickness of the mismatched layer (in a multi-layer stack) is about a factor of 4 greater than a single layer. This gives motivation to incorporate strained GaInAs channels between GaAs buffer layers and latticed matched GaInP barriers within the transistor structures.

Also, if the $\text{Ga}_x\text{In}_{1-x}\text{P}$ is in tension ($x > 51\%$), the strain within both layers can be compensated, resulting in zero strain for the entire structure.

2.2.2 Group III-Nitride System

AlN , GaN , and InN , are semiconductor compounds, which can crystallize in either the zincblende (β) or wurtzite (α) structure. However, the thermodynamically stable phase is the hexagonal wurtzite (α) structure [14]. A schematic representation of the hexagonal wurtzite structure with crystallographic directions and Burgers vectors is shown in Figure 2.2 (a). This structure is described by a basal hexagon having an edge length of a , the height c of the hexagonal prism, and an internal parameter u defined as the anion-cation bond length along the (0001) axis in units of c . The wurtzite structure has 6-fold symmetry with 2 bilayer steps per unit cell. The atoms are arranged in two closely spaced hexagonal layers, one with cations, and the other with anions, yielding two different polar faces. In Ga-face material, the metal atoms occupy the top position of the {0001} bilayer, corresponding to the [0001] polarity as shown in Figure 2.2 (b). By convention, the Ga-face [0001] direction is given by a vector pointing from the metal atom to a nearest-neighbor N atom. N-faced material is just the opposite.

Wurtzite has the highest symmetry compatible of spontaneous polarization and the piezoelectric tensor has three non-vanishing independent components [15,16]. The total polarization, in the absence of an electric field, is the sum of both the spontaneous (present with or without strain) and piezoelectric (strain dependent) components. The direction of the spontaneous polarization depends only on the polarity of the crystal, where as the direction of the piezoelectric polarization is determined by whether the material is under tensile or compressive stress as well as the polarity. The

spontaneous polarization along the c direction can be calculated simply from [16]:

$$\hat{P}_{sp} = P_{sp} \hat{z} \quad 2.3$$

where P_{sp} is the spontaneous polarization constant given in Table 2.2. For ternary compounds, a linear extrapolation is taken between the end-members.

In the linear regime, the piezoelectric polarization is related to the strain ϵ by:

$$\hat{P}_i = \sum_j e_{ij} \epsilon_j \quad 2.4$$

which defines the components of the piezoelectric tensor e_{ij} . The piezoelectric polarization is expressed via the piezoelectric coefficients e_{33} and e_{31} as:

$$P_{PE} = e_{33} \epsilon_3 + e_{31} (\epsilon_1 + \epsilon_2) \quad 2.5$$

where $\epsilon_3 = (c - c_0) / c_0$ is the strain along the c-axis, and the in-plane strain $\epsilon_1 = \epsilon_2 = (a - a_0) / a_0$ is assumed to be isotropic.

The third independent component of the piezoelectric tensor e_{15} is related to the polarization induced by a shear strain, and is not considered in this discussion. Additional details and calculations are given in Chapter 6 for the AlGa_N/Ga_N heterostructures.

Table 2.2: Selective material parameters for wurtzite nitride materials. [14-21]

parameter	units	AlN	GaN	InN
A_0	Å	3.112	3.189	3.54
C_0	Å	4.982	5.185	5.705
C_0/a_0	—	1.601	1.627	1.612
U	—	0.380	0.376	0.377
P_{SF}	C/m ²	-0.081	-0.029	-0.032
e_{33}	C/m ²	1.46	0.73	0.97
e_{31}	C/m ²	-0.60	-0.49	-0.57
e_{15}	C/m ²	-0.48	-0.3	—
ϵ_{11}	—	9.0	9.5	—
ϵ_{33}	—	10.7	10.4	—
C_{11}	GPa	396 (cal)	367 (cal)	223 (cal)
C_{12}	GPa	137 (cal)	135 (cal)	115 (cal)
C_{13}	GPa	108 (cal)	103 (cal)	92 (cal)
c_{33}	GPa	373 (cal)	405 (cal)	224 (cal)

The lack of suitable GaN substrates for homoepitaxy makes the growth of device-quality GaN materials very difficult. The key to obtaining planar, high resistivity GaN buffer layers of good structural quality is to achieve a 2-dimensional (2D) growth mode soon after the initial stages of deposition. This can be accomplished by optimizing the nucleation layer, which accommodates

the mismatch between the substrate and the epitaxial film and is discussed in detail in Chapter 5. For the work presented in this thesis, two different substrates were used for GaN growth, *c-plane* sapphire and Si-faced SiC. Relevant material parameters for these substrates are given in Table 2.3 [22-25]. Due to the difference in the thermal expansion coefficients, upon cooling from growth temperatures the GaN epitaxial layers on sapphire are in compression, while GaN films on SiC are in tension.

2.3 Methods Used to Characterize Epitaxial Layers

Characterization methods used to analyze transistor materials are described. The intent is to present calculations necessary for determining specific material properties, and not to provide a detailed description of the characterization method employed.

2.3.1 Photoluminescence

Photoluminescence (PL) is a non-destructive technique useful for estimating alloy compositions in direct band gap ternary and quaternary materials. Structural quality of the crystal can also be ascertained by relative emission intensity and full-wave-half-maximum (FWHM) widths at room temperature, or by the observation of exciton(s) in low temperature (LT) spectra. In direct band gap materials, optical excitation above band gap results in spontaneous emission (PL radiation) from the semiconductor, which is independent of the excitation wavelength. This differentiates PL from Raman emission. GaAs-based materials were optically excited with the 488 nm and/or 514 nm lines of an Argon laser, while nitride crystals were excited by either the 325 nm He-Cd laser line (AlGa_N < 12% Al), or the 257 nm line of a frequency doubled Argon laser.

Table 2.3: Useful parameters of substrates used for epitaxial growth [22-25].

parameter	Units	sapphire	SiC	Si	GaAs
A_0	Å	4.758	3.189	5.4307	5.6533
C_0	Å	12.991	5.185	-	-
C_0/a_0	-	2.730	1.627	-	-
	-			-	-
$E_g(300)$	eV	9.0	3.27 (4-H) 3.02 (6-H)	1.124 (indirect)	1.43
E_r				11.7	13.1
N	-	9.0	9.5	3.44	3.30
κ	W/cm K	0.42	3.3	1.412	0.455
α	$\times 10^{-6}/K$	a 7.5 c 8.5	4.5	2.5	5.9

Compositions can be determined if the variation in peak PL energy with alloy content is known. Vegard's law is commonly used to estimate the composition of ternary materials from extrapolating from the end-point binaries. Accuracy can be improved by taking into account the non-linear effects of alloying and adding a third term with a "bowing" parameter (b) as given in equation 2.6:

$$E_{Alloy}(x) = xE_A(x) + (1-x)E_B(x) - bx(1-x) \quad 2.6$$

In the case of GaInP, not only can the Indium mole fraction be estimated, the measured bandgap gives information on the alloy ordering. Figure 2.3 shows the dependence of peak PL energy versus growth temperature for lattice matched GaInP, where the highest degree of CuPt-type ordering is observed at 650° C [26]. Using X-ray analysis to determine the composition, the corresponding PL data can be used to estimate the degree of ordering in the GaInP films.

AlGaIn grown directly on SiC or sapphire substrates establishes its own-latticed constant after several hundred Angstroms of deposition. The Al mole fraction can then be estimated by Vegard's Law, where the bowing factor is taken to be 0.8 eV [27]. In the AlGaIn/GaN transistor structure, the thin AlGaIn barrier is in tensile strain, which shifts the near band-edge PL emission. For biaxial tensile strain [28],

$$\frac{dE_{PL}}{d\sigma} = (-27 \pm 4) \frac{meV}{GPa} \quad 2.7$$

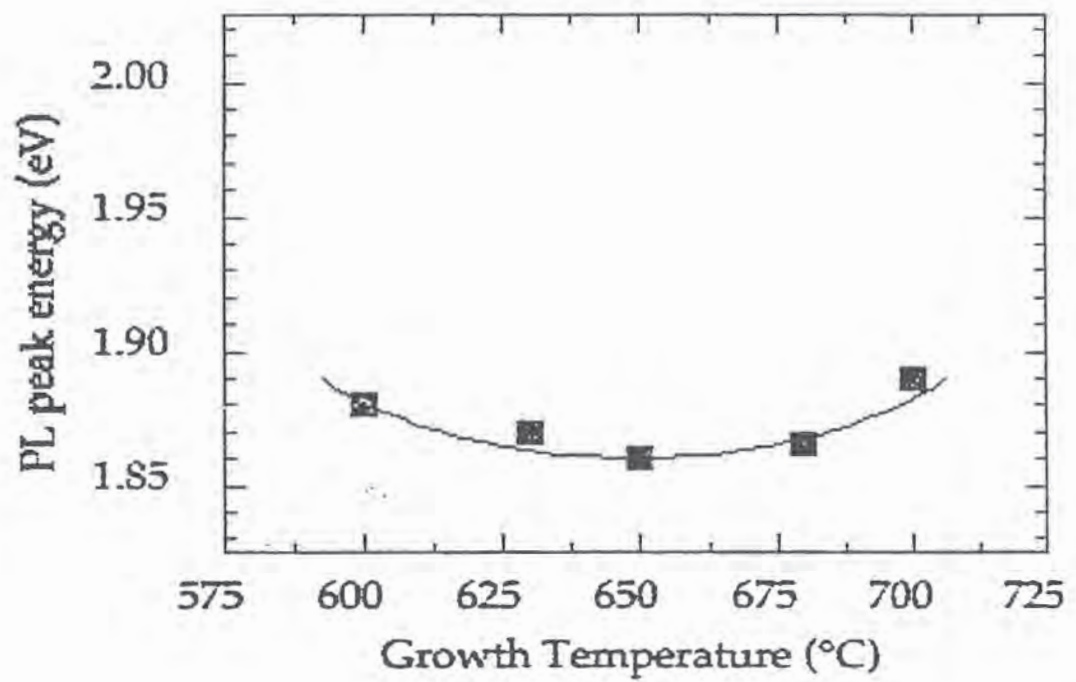


Figure 2.3 PL peak energy versus growth temperature for latticed matched GaInP to GaAs.

for this work, -25 meV/GPa was used. The pressure in tensile strained, pseudomorphic AlGaIn films on GaN can be calculated from:

$$\sigma = \varepsilon_{xx} \left(c_{11} + c_{12} - 2 \frac{c_{13}^2}{c_{33}} \right) \quad 2.8$$

The stress in pseudomorphic AlGaIn barriers can be determined from:

$$\varepsilon_{xx} = \frac{a(x) - a_0(x)}{a_0(x)} \quad 2.9$$

where $a(x)$ is the in-plane lattice constant of GaN, and $a_0(x)$ is the lattice constant of relaxed $\text{Al}_x\text{Ga}_{1-x}\text{N}$.

Therefore, an estimate of Al content from PL emissions taking strain into account can be obtained from:

$$\text{and,} \quad E_{\text{AlGaIn}}(x) = E_{\text{AlGaIn}_0}(x) + dE_{\text{PL}}(x) \quad 2.10a$$

$$E_{\text{AlGaIn}}(x) = E_{\text{AlGaIn}_0}(x) - 25 \text{ meV/GPa} \cdot \sigma(x) \quad 2.10b$$

Figure 2.4 shows the AlGaIn PL band edge dependence on Al content. The three curves correspond to using Vegard's law without (a) and with (b) the bowing factor, and with the bowing factor and accounting for strain effects (c).

2.3.2 Capacitance – Voltage Profiling

Capacitance-voltage (C-V) measurements using a non-destructive mercury droplet provide crucial information on the charge distribution within

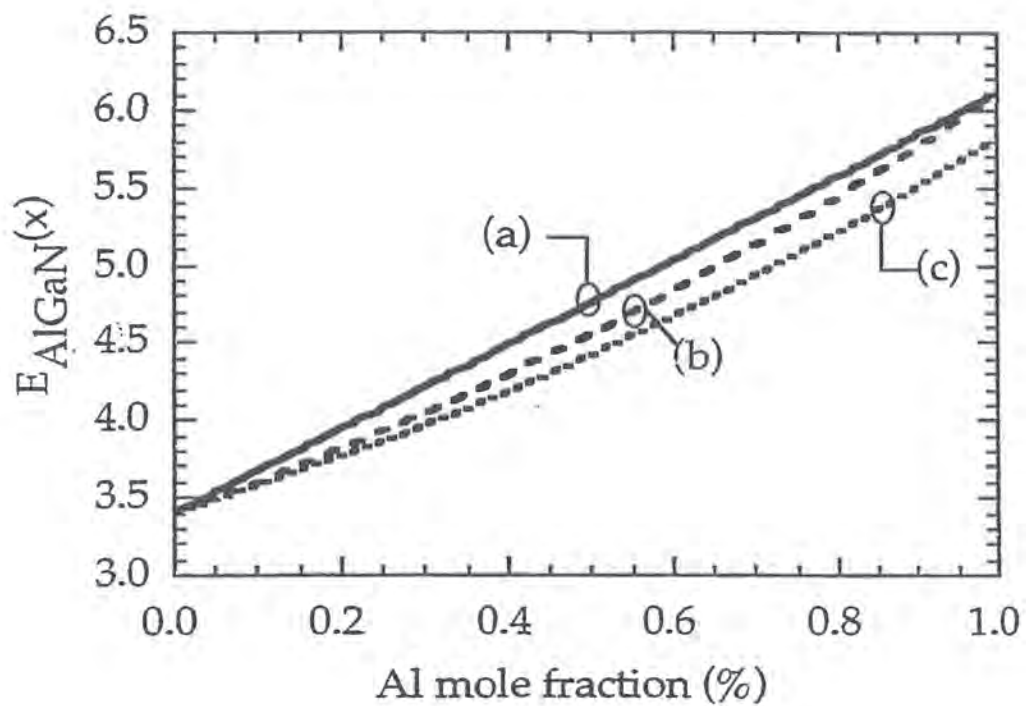


Figure 2.4 Calculated AlGaIn PL emission versus Al content, using (a) Vegard's law, (b) with a bowing parameter, and taking strain into account (c).

HEMT structures. This characterization tool can detect buried charge in the buffer layer or substrate, confirm the presence of a 2DEG and detect charge in the barrier, supply, and cap layers.

The net doping density profile may be obtained from measurement of the depletion capacitance associated with the band-bending region of a metal Schottky contact (Hg – droplet). Using a simplified case of uniform doped material, it can be shown that the depletion region behaves as a parallel plate capacitor [29]. The net free-carrier profile can then be expressed as:

$$N(x) = -\frac{C^3}{q\epsilon A^2} \left(\frac{\Delta C}{\Delta V_r} \right)^{-1} \quad 2.11$$

where ΔC is the differential change in capacitance per change in voltage (ΔV_r) and A is the area of the mercury droplet.

A typical carrier profile derived from C-V measurements for an AlGaIn/GaN HEMT is shown in Figure 2.5 (a). Clearly the 2DEG is seen near the surface with a long Debye tail extending into the substrate. No buffer charge is observed in the profile. Integrating the area under the volume concentration curve gives the carrier sheet density shown in Figure 2.5 (b) plotted against reverse bias voltage. The integrated sheet density increases as the depletion region pushes through the 2DEG, and flattens after entering the highly resistive GaN buffer. The point where the curve flattens corresponds to the pinch-off voltage for the transistor structure. The slope of the sheet density curve (within the 2DEG) can be used to estimate the AlGaIn barrier

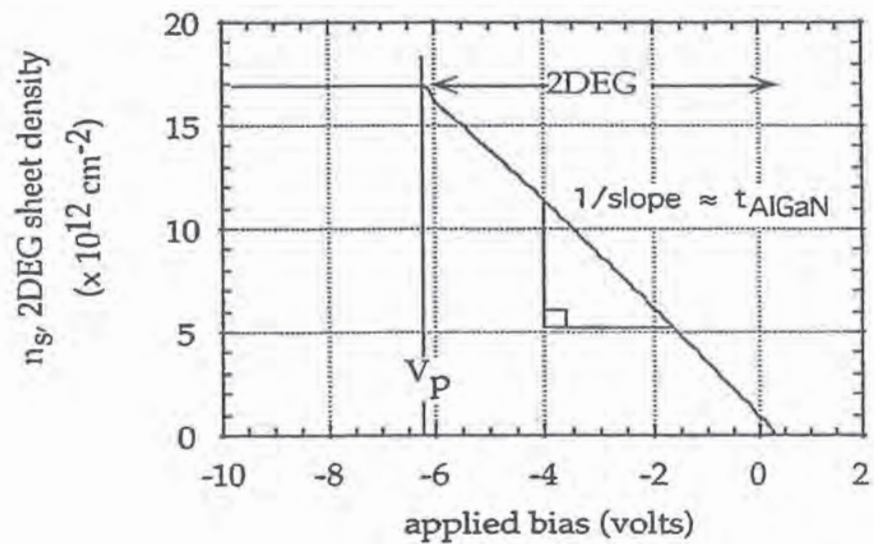
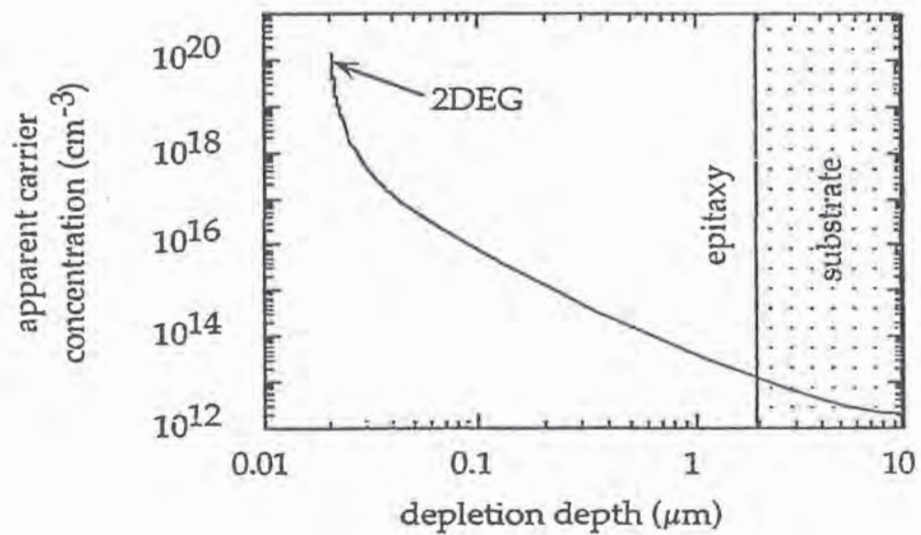


Figure 2.5 C-V measurements on AlGaIn/GaN HEMT structure, (a) shows the derived free carrier concentration profile while (b) gives the calculated sheet density profile.

thickness. Assuming a parallel plate capacitor, it is easily derived that,

$$x_d = \epsilon \epsilon_0 A \left(\frac{\Delta V}{\Delta n_s} \right) \quad 2.12$$

where $\Delta V / \Delta n_s$ is the inverse slope while in the 2DEG.

Surface states, actual 2DEG densities (dependent on Al content) and charge in the barrier can change the slope of the sheet density curve and introduce an error of about $\pm 10\%$ on the calculated thickness. Measurements are typically done at 10 KHz, with a 735 μm diameter mercury droplet.

2.3.3 X-Ray Diffraction

Structural and compositional information is conveniently obtained through non-destructive X-ray diffraction measurements. For symmetric and asymmetric measurements, a double-crystal diffractometer was used for measuring the lattice constants and assessing crystalline quality. The X-rays are produced in a Coolidge tube with a fixed Cu anode.

The condition for constructive interference of waves reflected from parallel lattice planes is given by Braggs Law [30] as:

$$n\lambda = 2d \sin \theta_g \quad 2.13$$

where n is an integer (order of reflection), λ is the X-ray wavelength and θ_g is the angle between the incident ray and the surface of the crystal as illustrated in Figure 2.6 (a).

2.3.3.1 Completely Strained Overlayer: Symmetric Reflections

Consider the case of a coherently strained layer such as a thin pseudomorphic $\text{Ga}_x\text{In}_{1-x}\text{P}$ ($x \neq 0.51$) on (001) GaAs. A coherently strained epitaxial layer will have the same in-plane lattice constant (parallel to substrate/epitaxy interface: $a_{||}$) as the underlying material. Therefore, a deformation must occur in the direction perpendicular to $a_{||}$, a Poisson expansion if the strain film is in compression (Figure 2.6 b), or in tension (Figure 2.6 c). By varying θ (rocking the sample) peaks are detected when the Bragg condition is satisfied for the strained epitaxial layer and substrate. A straightforward analysis can be made in the case of the (004) reflection for epitaxial layers grown on (001) oriented GaAs substrates in which the angle between the surface and that of the incident and reflected X-ray beams (θ_b) are equal [31]. In these symmetric reflections, the Bragg spacing is given by $a_{\perp}/4$, where $a_{\perp}=d$ is the lattice constant in the (001) direction. Neglecting any misorientation of the substrate surface from the (001) direction, the mismatch of the epitaxial layer can be calculated from:

$$\left[\frac{\Delta d}{d} \right]_{\perp} = \left[\frac{\Delta a}{a} \right]_{\perp} = \frac{a_{\perp}^e - a_{\perp}^s}{a_{\perp}^s} = -\frac{\Delta \omega}{\tan \theta_b^s} \quad 2.14a$$

where, $a_{\perp}^e$ is the lattice constant of the epitaxial layer, $a_{\perp}^s$ is that of the substrate, θ_b^s is the Bragg angle for the substrate, and $\Delta \omega$ is the measured angular separation between the Bragg peaks.

Differentiating Bragg's Law and making the small angle approximation for $\Delta \omega$ obtained this equation. If $\Delta \omega$ is not small compared to $2/(\tan \theta_b^s + 2)$, which

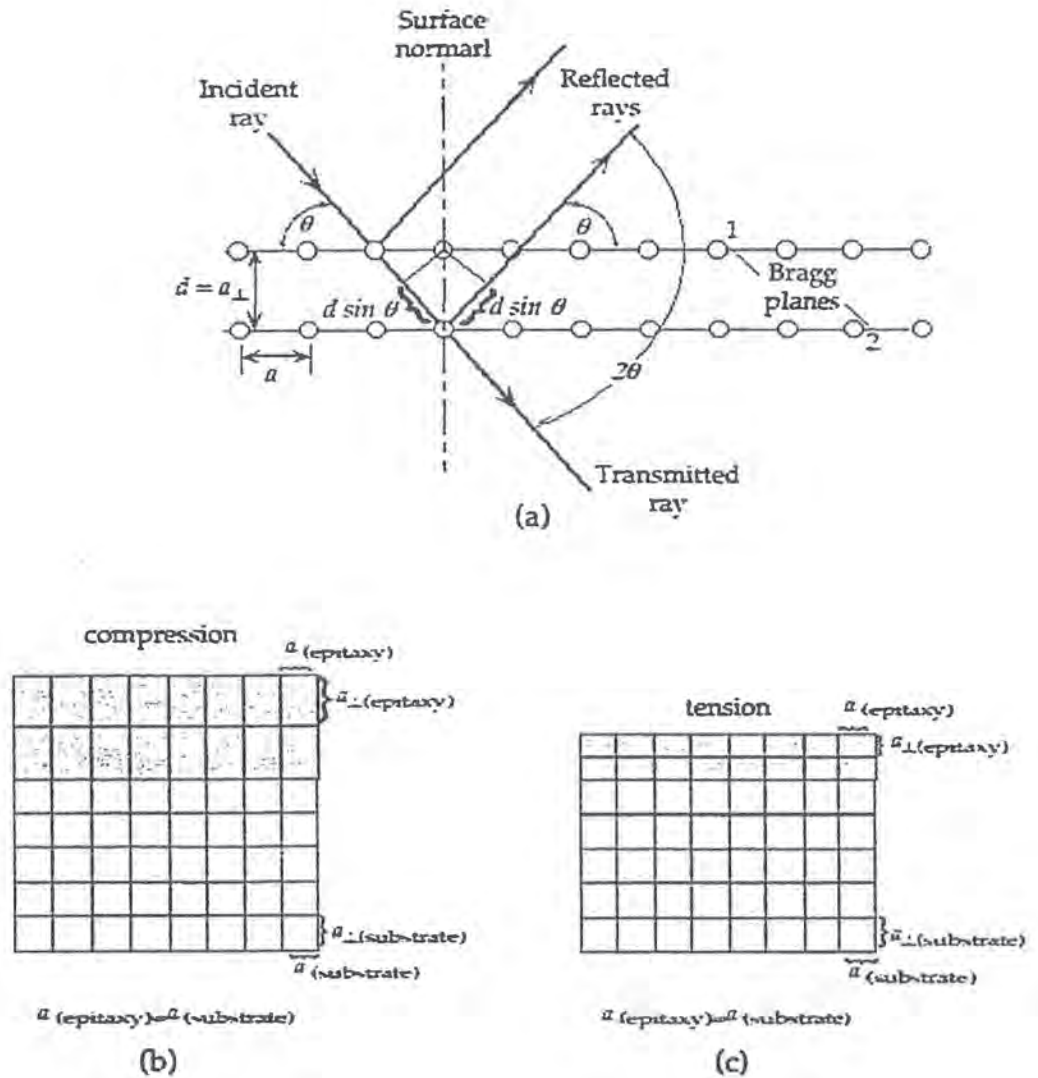


Figure 2.6 Schematic representation of Bragg's Law shown in (a). Coherently strained epitaxial layers shown in compression (b), and in tension (c).

is the case between sapphire and SiC substrates with GaN epitaxy, then the full expression must be used:

$$\left[\frac{\Delta a}{a} \right]_{\perp} = \frac{\sin \theta_{B(sub)}}{\sin(\theta_{B(sub)} + \Delta \omega)} - 1 \quad 2.14b$$

To determine composition, $[\Delta a/a]_{\perp}$ must be related to the fully relaxed lattice constants by:

$$\left[\frac{\Delta a}{a} \right]_R = \frac{a_o^e - a^s}{a^s} \quad 2.15$$

where a_o^e is the fully relaxed lattice parameter of the epitaxial layer.

The strain in the perpendicular direction (001) ε_{001} , is related to the strain in the parallel $[110]$ ε_{110} and $[1\bar{1}0]$ $\varepsilon_{1\bar{1}0}$ directions within the mismatched layer by [32]:

$$\varepsilon_{001} = -\frac{c_{12}}{c_{11}}(\varepsilon_{110} + \varepsilon_{1\bar{1}0}) \quad 2.16$$

where c_{ij} are components of the elastic stiffness tensor.

For a coherent layer, the in-plane lattice constant of the substrate and overlayer are equal, therefore:

$$\varepsilon_{110} = \varepsilon_{1\bar{1}0} = \frac{a^s - a_o^e}{a_o^e} \quad 2.17$$

Substituting equations 2.14 and 2.17 into 2.16 gives an expression for the relaxed mismatch in terms of the measured perpendicular mismatch,

$$\left[\frac{\Delta a}{a} \right]_R = - \frac{c_{11}}{c_{11} + 2c_{12}} \left[\frac{\Delta a}{a} \right]_{\perp} \quad 2.18$$

Solve for the relaxed lattice constant then use Vegard's law to calculate the composition of the strained layer. Figure 2.7 gives the (004) reflection rocking curves of a $\text{Ga}_x\text{In}_{1-x}\text{P}$ layer on GaAs, in compression (a) and in tension (b).

2.3.3.2 Partially Relaxed Epitaxial Layer: Asymmetric Reflections

If the mismatched epitaxial layer exceeds its critical thickness, misfit dislocations form to accommodate the strain and the layer is no longer coherent. Now, the in-plane mismatch defined as,

$$\left[\frac{\Delta a}{a} \right]_{\parallel} = \frac{a_{\parallel}^s - a^s}{a^s} \quad 2.19$$

must be measured to accurately determine the lattice constant. This can be accomplished by using equivalent asymmetric planes in the epitaxial layer and substrate, which are not parallel in the case of tetragonal distortion as shown in Figure 2.8 (a). The d-spacing of the asymmetric planes has components both parallel and perpendicular to the surface. By measuring a second rocking curve, rotated 180° around the surface normal, both the perpendicular and parallel mismatch lattice constants can be experimentally determined. These two configurations are referred to as glancing incidence and glancing exit and are depicted in Figure 2.8 (b) and (c) respectively. As in the case for symmetric reflections, the measured strained lattice constants can

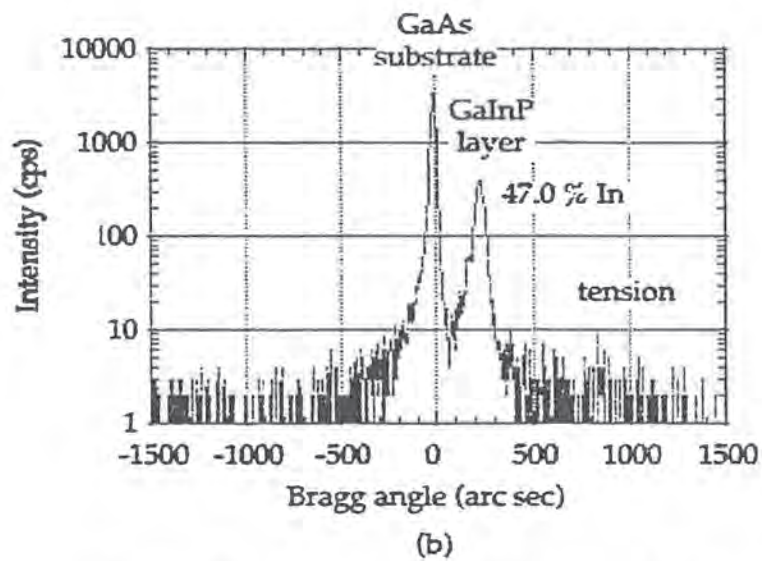
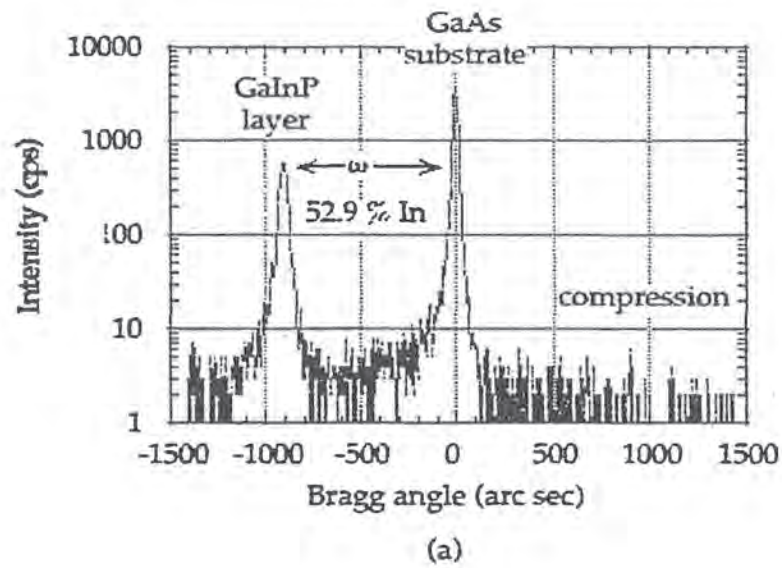


Figure 2.7 Symmetric (004) x-ray rocking curves of GaInP layers on GaAs substrates. Layer shown in (a) is in compression, while layer in (b) is in tension.

be used to compute the relaxed mismatch and composition of the epitaxial layer.

In contrast to symmetric reflections, the normal of the asymmetric planes makes an angle ϕ with the surface normal. Also, the Poisson distortion from residual strain makes an angle $\Delta\phi$ between ϕ_e and ϕ_s . Thus, the angular separation $\Delta\omega$ of the Bragg peaks have two components, $\Delta\phi$ from the tilt of the epitaxial layer planes relative to that of the substrate, and $\Delta\theta$ from the difference between the substrate and epitaxy Bragg angles. For the glancing incidence, $\Delta\omega^- = \Delta\theta - \Delta\phi$, and with the glancing exit, $\Delta\omega^+ = \Delta\theta + \Delta\phi$. These two measurements give [31],

$$\Delta\theta = \left(\frac{\Delta\omega^+ + \Delta\omega^-}{2} \right) \quad 2.21$$

and,

$$\Delta\phi = \left(\frac{\Delta\omega^+ - \Delta\omega^-}{2} \right) \quad 2.20$$

Using similar derivations as in the symmetric case, the perpendicular and parallel mismatches can be computed from,

$$\left[\frac{\Delta a}{a} \right]_{\perp} = -\Delta\theta \cot \theta_B + \Delta\phi \tan \phi_s \quad 2.22$$

and,

$$\left[\frac{\Delta a}{a} \right]_{\parallel} = -\Delta\theta \cot \theta_B - \Delta\phi \cot \phi_s \quad 2.23$$

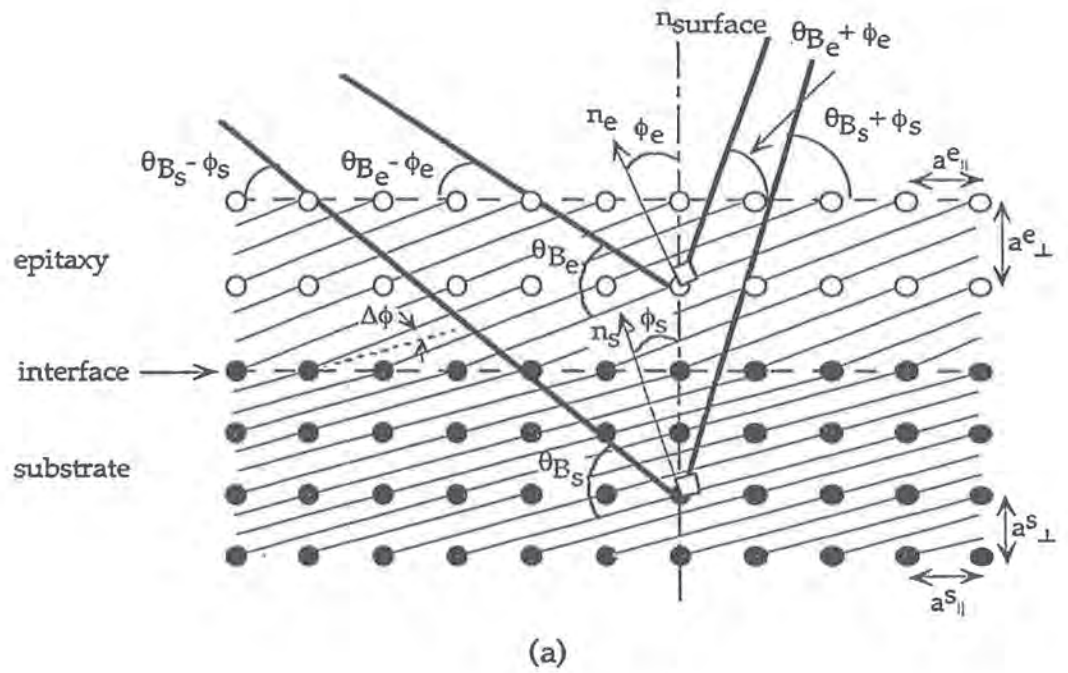


Figure 2.8 Schematic representation of asymmetric reflections (a) along with glancing incidence (b) and exit (c) configurations. Rotating sample by 180° changes configuration from glancing incidence to glancing exit.

Finally, an expression for the relaxed mismatch from measured parameters can be obtained from substituting equations 2.14, 2.17, and 2.19 into 2.16 yielding,

$$\left[\frac{\Delta a}{a} \right]_R = \frac{2c_{12} \left(\frac{\Delta a}{a} \right)_{\parallel} + c_{11} \left(\frac{\Delta a}{a} \right)_{\perp}}{c_{11} + 2c_{12}} \quad 2.24$$

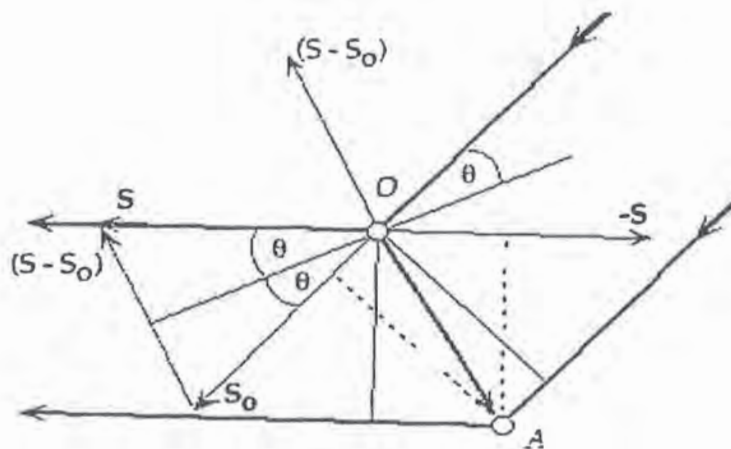
The relaxed lattice constant can then be used in Vegard's law to estimate the composition of the epitaxial layer.

2.3.3.3 Reciprocal Space Mapping

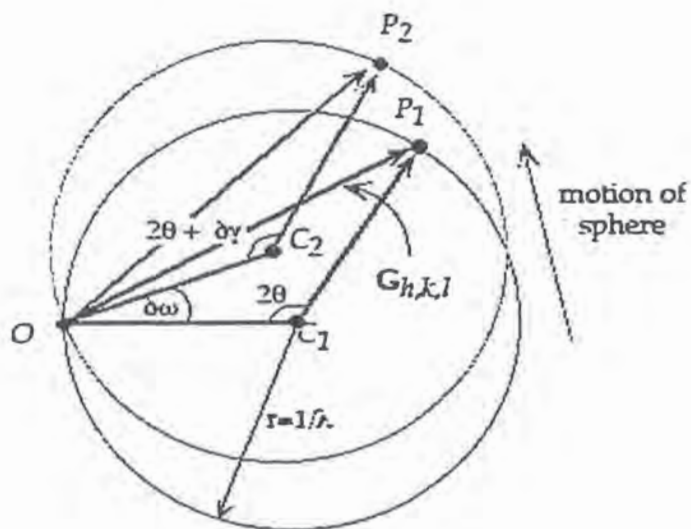
The widths of the diffraction peaks, obtained from symmetric and asymmetric measurements, are complex functions of strain variation and mosaic spread in the sample. By constructing a map of the reciprocal lattice, it is possible to differentiate strain effects from lattice plane tilts, as well as determine the amount of mismatch in the epitaxial layer.

Consider the relationship between X-rays scattered by an atom O (at the origin of the crystal) and those scattered by another atom A as shown in Figure 2.9 (a). Here, the unit vectors S_o and S are the incident and diffracted beams respectively. By determining the path difference of the rays scattered by O and A , and requiring that they be in phase (phase difference a multiple of 2π), then [32,33],

$$\frac{S - S_o}{\lambda} = G = hb_1 + kb_2 + lb_3 \quad 2.25$$



(a)



(b)

Figure 2.9 Schematic representation of diffraction in reciprocal space, (a) gives diffraction from 2 atom O and A, (b) is the Ewald construction of diffraction in reciprocal space.

Therefore, the condition for diffraction is that the vector $(\mathbf{S} - \mathbf{S}_0)/\lambda$ ends on a point in the reciprocal lattice, where h , k , and l are integers. Equation 2.25 can be represented graphically by the Ewald construction shown in Figure 2.9 (b). For diffraction from (hkl) planes, the point hkl in the reciprocal lattice must touch the surface of the sphere. When this is the case, the vector $\mathbf{OP}$ equals both $\mathbf{G}_{hkl}$ and $(\mathbf{S} - \mathbf{S}_0)/\lambda$, thus satisfying equation 2.25.

Changing the angle of incidence by $\delta\omega$, sweeps the Ewald sphere through reciprocal space, moving the center of the sphere from C_1 to C_2 as shown in Figure 2.9 (b). If the detector is moved from the initial position of 2θ to $2\theta + \delta\gamma$, the scattering from point P_2 will be measured. A detailed schematic around the diffraction points is given in Figure 2.10. The origin of the axes is the reciprocal lattice point (RLP) corresponding to the diffraction planes (hkl) . Point P_2 deviates from the RLP by the deviation vector $\mathbf{q}$. This vector has two components q_y and q_z , which are related to the change of the incidence angle ($\delta\omega$) of the beam and position of the detector ($\delta\gamma$) from their original positions at the nominal Bragg angle by [34]:

$$q_z = \frac{\delta\gamma \cos\theta}{\lambda} \quad 2.26$$

and,

$$q_y = \frac{(2\delta\omega - \delta\gamma) \sin\theta}{\lambda} \quad 2.27$$

Clearly, if the detector is kept stationary ($\delta\gamma=0$) we get a horizontal scan through reciprocal space. Conversely, if the detector tracks twice the change

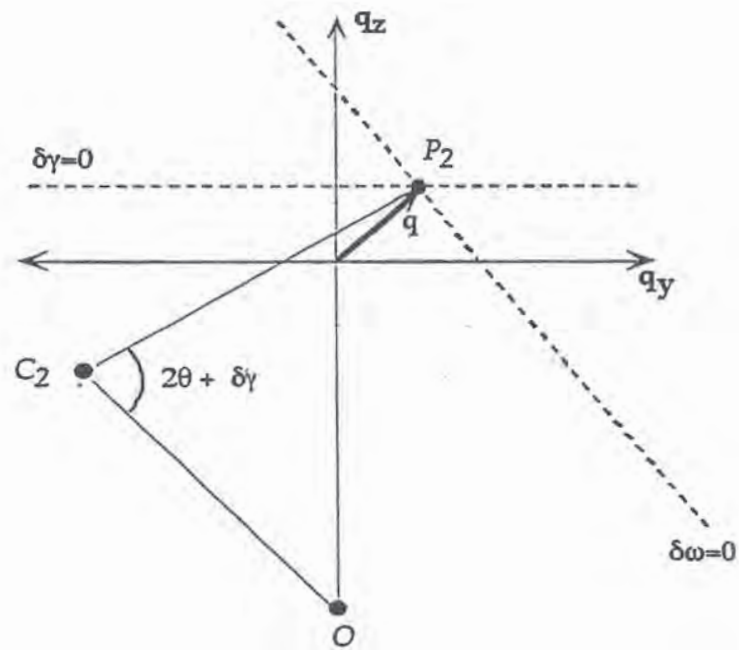


Figure 2.10 Schematic representation of the deviation vector.

in the incident angle ($2\delta\omega = \delta\gamma$) we get a vertical scan. A mapping of reciprocal space can be realized by scanning all needed points with the detector coupled to the sample ($2\delta\omega = \delta\gamma$) for each $\delta\omega$ step.

Consider changing only the angle of incidence ($\delta\omega$), while keeping the detector fixed. The Bragg condition is met at only one angle, and once rotated off no reflections should be recorded. However, if there were regions that are tilted in respect to each other, the d-spacing would not change but the Bragg angle would. By rotating the sample only, scanning in the q_y direction, the scattering intensity gives the distribution of tilted regions in the sample. On the other hand, if a coupled scan ($2\delta\omega = \delta\gamma$) is done, regions with different d-spacing will be detected. Thus, the intensity variations in the q_z direction are a measure of lattice parameter distribution of the sample. This measurement is insensitive to tilted areas within the lattice. Therefore, reciprocal space mapping allows one to distinguish between tilted regions and regions with varying lattice spacing. Reciprocal lattice maps of AlGaIn/GaN structures are given in Chapter 6.

Chapter 2 References

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CHAPTER 3

EPITAXIAL GROWTH OF GaAs, GaInP AND GaInAs

3.1 Introduction

In device structures, emphasis is usually placed on the active region(s) where all the "action is". However, the often-neglected buffer layer can be a crucial part of the structure. This is the case with laterally conducting transistor structures, where the buffer layer(s) can strongly influence the dc and RF performance. Homoepitaxial GaAs is used for the buffer layer in both the latticed-matched and pseudomorphic HEMT structures grown for this work. The GaAs epitaxy has to be highly resistive, exhibit an atomically smooth growth front and free from any mobile charge at the epitaxy / substrate interface.

In addition, $\text{Ga}_x\text{In}_{1-x}\text{P}$ can be grown on top of the GaAs buffer resulting in a two layer buffer structure. The $\text{Ga}_x\text{In}_{1-x}\text{P}$ layer provides a high ΔE_c between the buffer and channel compared to GaAs, enhancing the confinement (from the backside) of the 2DEG. The majority of structures grown for this work do not employ GaInP for the buffer, but GaInP is used for the spacer, supply, and barrier layers of the transistor. Therefore, the electrical and structural properties of $\text{Ga}_x\text{In}_{1-x}\text{P}$ must be optimized.

Both GaAs and GaInAs films can be used for the channel of the device. The $\text{Ga}_y\text{In}_{1-y}\text{As}$ is always in compression when grown on relaxed GaAs and should not exceed its critical thickness. The 2DEG resides in the channel near

the spacer (phosphide)/channel (arsenide) interface, requiring that the heterostructure be atomically smooth to obtain the highest electron mobility and saturation velocity. The arsenide to phosphide transitions, as well as the spacer/channel interface need to be as abrupt as possible.

All these growth issues are investigated on an abbreviated HEMT test structure. Detailed growth experiments and optimizations on GaAs, GaInP, and GaInAs are discussed in this chapter. Characterization includes variable temperature PL, X-ray, AFM, C-V and Hall effect measurements. Specific optimizations on the complete HEMT structure are presented in Chapter 4.

3.2 General Growth Conditions

Layers were grown in the temperature range of 530° C to 635° C in the arsenide/phosphide reactor described in Section 1.3.1. The growth pressure was maintained at 76 Torr, and the precursors used were Triethylgallium (TEG), Trimethylindium (TMI), arsine (AsH_3), and phosphine (PH_3). TEG was chosen to minimize the amount of carbon incorporated in the films, which can degrade RF performance. For the supply layer doping, silane (SiH_4) diluted in hydrogen (200 and 2000 ppm) was used. GaAs buffer layers are grown at either 100 Å/min or 35 Å/min depending on the experiment. The growth rate for GaInAs and GaInP were 95 Å/min and 70 Å/min, respectively. Varying V/III ratios were investigated for all the layers. GaAs substrates were either on-axes ($\pm 0.1^\circ$), 3° or 6° miscut towards the $\langle 111 \rangle_B$. Different pre-growth substrate surface preparations were investigated to reduce or eliminate interface charge at the substrate/epitaxy interface as described in Section 3.4.

3.3 Test Structure

An abbreviated single-side doped HEMT structure as shown in Figure 3.1 was used to monitor effects of subtle changes in growth conditions. A silicon delta doped layer is located 45 Å to 100 Å from the heterostructure. The 2DEG resides in the first 100 Å of the GaAs buffer just below the spacer layer. Lattice-matched to GaAs, this test vehicle is used to evaluate growth temperature, substrate orientation, charge transfer from the silicon delta-doping supply layer, AsH₃/PH₃ transition at the heterostructure and transport properties of the resulting 2DEG.

3.4 GaAs Buffers

Three different aspects of the GaAs buffer layer were separately optimized for the transistor structure. First, interface charge between the GaAs substrate and GaAs epitaxy had to be minimized or eliminated. Secondly, unintentional free carriers (electrons) in the buffer had to be minimized. The presence of any mobile charge (whether at the interface or in the buffer) increases drain leakage current, yielding poor pinch-off and device breakdown characteristics. Finally, the V/III ratio had to be optimized for donor compensation to produce high resistivity GaAs buffers while maintaining good surface morphology and crystal quality.

3.4.1 Epitaxy/Substrate Interface Charge

Two possible sources for the introduction of impurities at the substrate surface are contamination from the reactor during the high temperature oxide desorption [1] or the substrate surface clean by wet chemical etching [2]. Since

	<u>Structure</u>	<u>Thickness</u>	<u>x In</u>	<u>Doping</u>
	GaInP Barrier	250 Å	0.49	n.i.d.
	δ-Doped Supply Layer	≈10 Å	0.49	$n \sim 10^{12} \text{ cm}^{-2}$
	GaInP Spacer	45-100 Å	0.49	n.i.d.
2DEG				
	GaAs Buffer	>6000 Å	0.00	n.i.d.
	SI-GaAs Substrate			

*n.i.d. (not intentionally doped)

Figure 3.1 Abbreviated lattice matched HEMT structure used as a test vehicle to optimize growth parameters.

the reactor is a potential source of impurity contamination, using a lower temperature and eliminating the oxide desorption may reduce the amount of free carriers at the substrate/epitaxy interface. For low temperature growth ($<650^{\circ}\text{C}$) on GaAs, oxide desorption is usually done at the congruent sublimation temperature of 650°C under an overpressure of AsH_3 to clean and "heal" the substrate surface from the wet chemical surface preparation. Figure 3.2 gives carrier concentrations profiles derived from C-V measurements for two identical test structures with the exception of the pre-growth temperature that the substrate is subjected to: one at 650°C (solid), the other at 550°C (dashed). Both samples show an accumulation of charge at the substrate/epitaxy interface. However, comparing the peak carrier concentrations at the interface, it is easily seen that the 650°C oxide desorption has an order of magnitude higher charge. Lower temperatures were not investigated since the GaInP layers on top of the GaAs buffers is typically grown at 550°C .

Lowering the pre-growth surface clean temperature reduced that amount of charge at the interface, but did not eliminate it. Nor did the experiments eliminate the surface preparation as a source of impurities. The standard surface preparation used was an etch in 5:1:1 ($\text{H}_2\text{SO}_4\text{:H}_2\text{O}_2\text{:H}_2\text{O}$ – Caro's etch) held at 0°C , followed by a 15 minute oxide growth in deionized (DI) water, and a 6 minute oxide etch in HF. Concern that residual S (a shallow dopant) might be left on the surface, an HCl based polishing etch as well as just an HF oxide etch was investigated. It has been reported that GaAs "epi-ready" substrates from various vendors all contain high levels of Chlorine

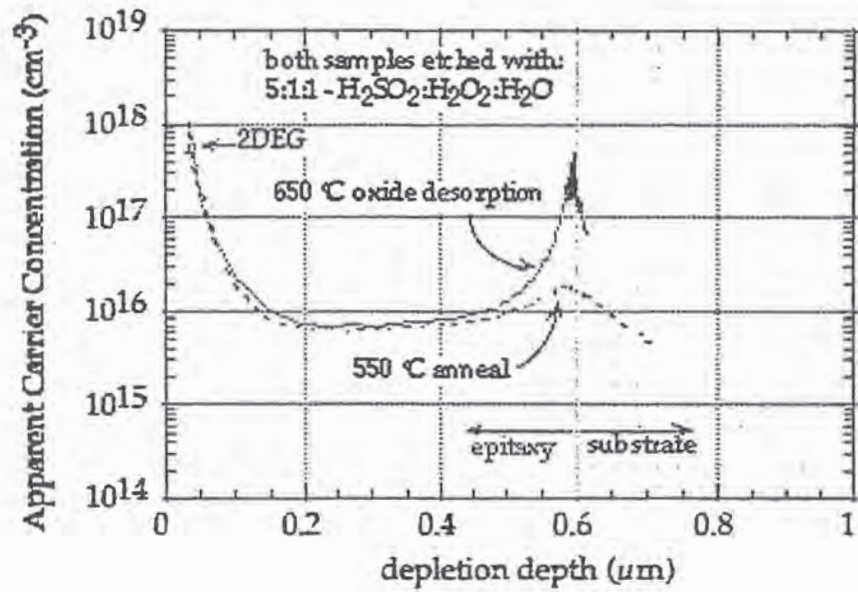


Figure 3.2 Carrier concentration profiles derived from C-V measurements for two different oxide desorption temperatures.

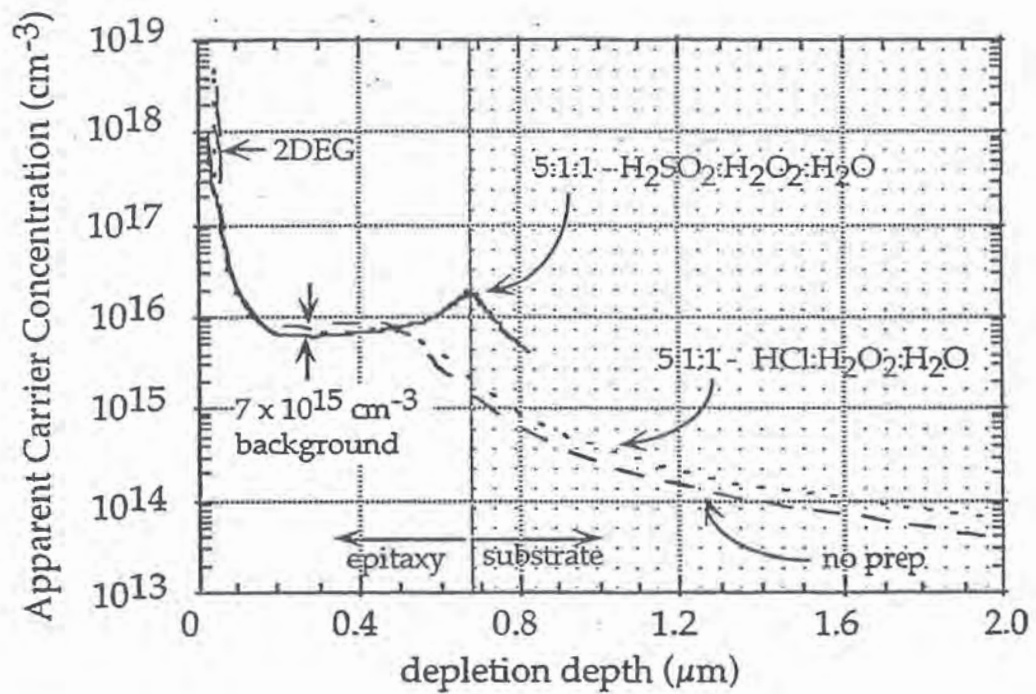


Figure 3.3 Carrier concentration profiles derived from C-V measurements for different substrate surface preparations. Oxide desorption temperatures at 650°C .

that does not appear to be an electrically active [3]. The HCl based etch was 5:1:1 (HCl:H₂O₂:H₂O) for 15 min followed by a 15 minute oxide growth in DI water, and a 6 minute oxide etch in HF. Free carrier profiles are shown in Figure 3.3, the H₂SO₄, HCl, and no-prep (as received) samples with an oxide desorption temperature of 650° C. The sample with the HF oxide etch had rough surface morphology, yielding no meaningful data. The "as received" and HCl prepped samples show no detectable interface charge, while the H₂SO₄ again indicated a large interface charge. The room temperature 2DEG mobility also improved from 4045 cm²volt⁻¹sec⁻¹ for the H₂SO₄ etched sample to 6095 cm²volt⁻¹sec⁻¹ and 6200 cm²volt⁻¹sec⁻¹ for the HCl and no-prep samples respectively. For the remainder of the growths for this project, either as received epi-ready (good for 6 months per vendors specifications - AXT) or HCl prepped substrates were used.

3.4.2 Unintentional Charge in the GaAs Buffer

High resistivity buffers can be achieved by either growing very pure material with no defects or impurities, or by compensating out free carriers. The first approach is preferred but not practical. The second method involves compensation of unwanted carriers from impurities or defects, which can produce trapping effects and limit large signal RF performance. The best approach is to make the GaAs as pure (clean) as possible, minimizing free carriers, then compensate out remaining carriers. This section focuses on improving the crystal structural quality while minimizing free carriers. Section 3.4.3. addresses the issue of compensation by varying the V/III ratio during growth.

Three buffer designs were investigated to improve the structural quality and reduce the amount of unintentional charge within the GaAs

epitaxial layer, measured to be in the high 10^{15} cm^{-3} as indicated in Figure 3.3. Two growth temperatures were investigated: at 635° C step flow growth was observed on GaAs layers, producing background carrier concentrations of $5 \times 10^{14} \text{ cm}^{-3}$, while growth at 550° C results in rough surfaces with unintentional electron concentrations as high as $1\text{-}2 \times 10^{16} \text{ cm}^{-3}$. AFM images of GaAs buffers grown at these two temperatures are shown in Figure 3.4 (a) and (b). Unfortunately, it is necessary to grow disordered GaInP for large ΔE_c , requiring temperatures well below 600° C . Exploiting the advantages of the high temperature GaAs material, a two-temperature GaAs buffer process was implemented. The bulk of the buffer layer is grown at the elevated temperature then the growth temperature is reduced for the remaining $500 \text{ \AA}$ of GaAs buffer and channel portion of the HEMT structure. The AFM image of a two-temperature buffer in Figure 3.4 (c) does not show atomic steps, but does show the reduction in free carriers as measured with C-V. The derived free carrier concentrations profiles are shown in Figure 3.5 for buffers grown entirely at 550° C (with the optimized surface preparation to eliminate interface charge), compared to the composite buffer growing first at 635° C , then at 550° C . Measured room temperature transport properties of the 2DEG did not significantly change between the different buffer structures. This is expected since the 2DEG resides in the first $100 \text{ \AA}$ of GaAs at the heterostructure which is grown on at 550° C on both structures. The inset in Figure 3.5 shows the 2DEG peak near the surface with a measured Full Wave Half Maximum (FWHM) of $92 \text{ \AA}$ in good agreement with the $87 \text{ \AA}$ calculated using C-band [4] code (simultaneously solving Poisson and Schrödinger's equations).

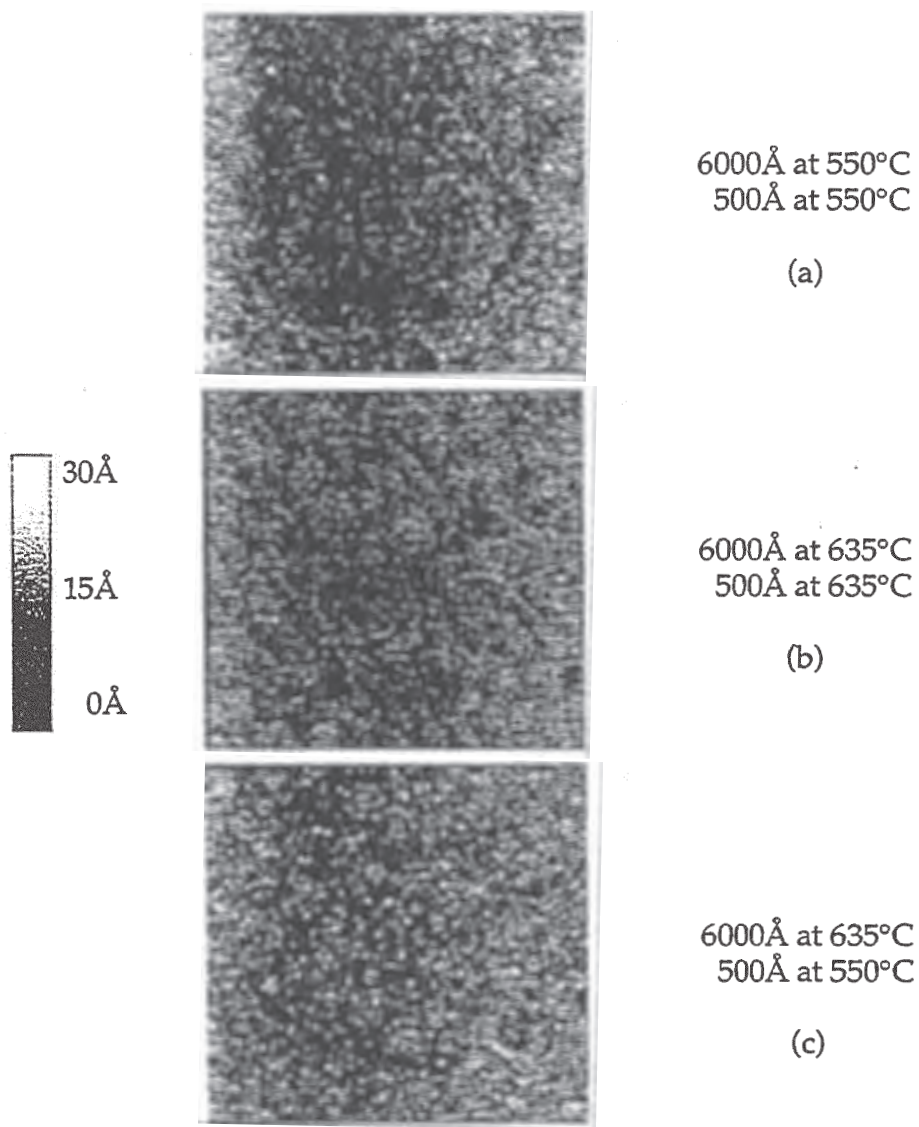


Figure 3.4 AFM images of three GaAs buffer designs, (a) is grown at 550° C, (b) is at 635° C, while (c) uses first both 635° C and 550° C growth temperatures.

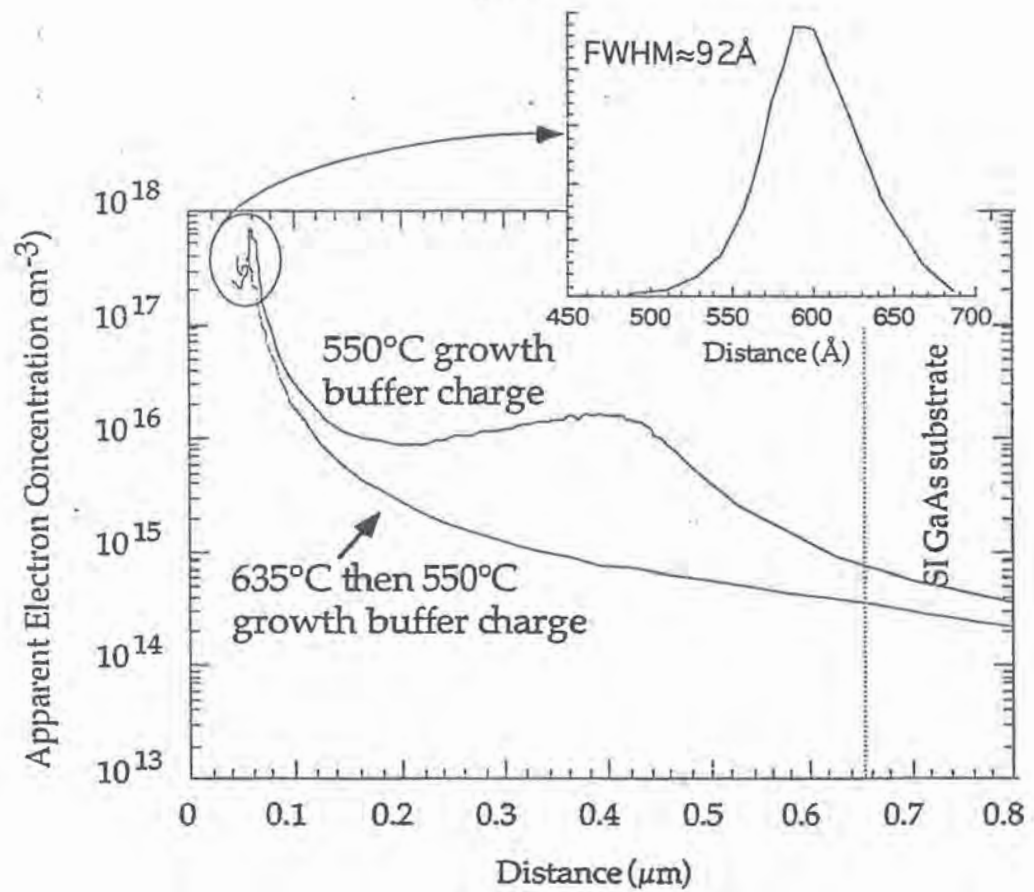


Figure 3.5 Derived carrier concentration from C-V measurements on two different GaAs buffer structures. Inset shows 2DEG profile near the heterostructure.

3.4.3 V/III Ratio

Previous work has shown that lowering the group V to group III ratio during growth of GaAs decreases the free electron carrier concentrations [1]. At lower V/III ratios, more acceptor states are created either from increased carbon incorporation or defects, which compensate the free electrons present in the GaAs film. Exploring V/III ratios in the range 1.0 to 10.0 within the GaAs buffer, maximum mobility and sheet density were achieved at a V/III of 2.25 as shown in Figure 3.6. Mobility reductions as large as 15 % were seen at V/III ratios below 2.25 due to surface roughening attributed to decomposition. At extremely low V/III ratios the surface decomposes from arsenic desorption. In the range from 2.25 to 10.0, no significant changes were seen in the room temperature electron mobility. The V/III ratio was fixed at 2.25 for the remainder of the GaAs-based epitaxy experiments.

3.4.4 Substrate Surface Miscut on GaAs Growth

Growth was suspended just after deposition of the GaAs channel (550° C) to determine effects of (100) vicinal surfaces on the growth front. Substrates were either on-axes ($\pm 0.1^\circ$), 3° or 6° miscut surfaces towards the $\langle 111 \rangle_B$. AFM images of the GaAs surface for each case are shown in Figure 3.7. Strain induced steps are seen on the non-vicinal substrate with height of ≤ 30 Å. Step bunching is present on the vicinal surfaces in the direction of the miscut with step heights of 120 Å and 200 Å for the 3° and 6° miscut, respectively. It was discovered that the bunching originates in the higher temperature GaAs buffer layer and propagates throughout the structure and results in a reduction of the room temperature electron mobility in the resulting 2DEG on the vicinal surfaces. Mobility decreases with increasing

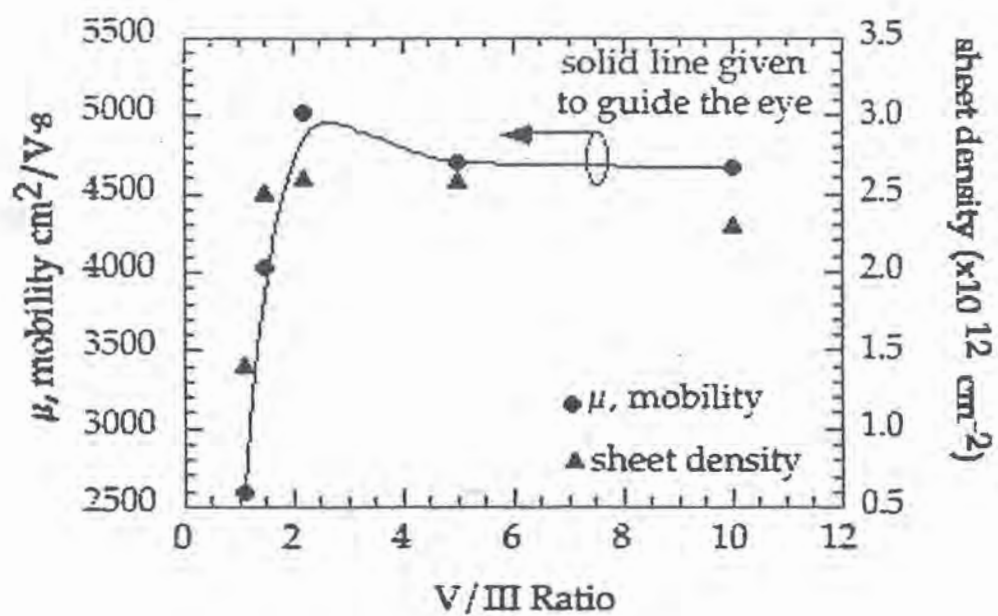


Figure 3.6 Room temperature Hall electron mobilities and sheet densities on test structures with varying V/III ratios in GaAs buffers.

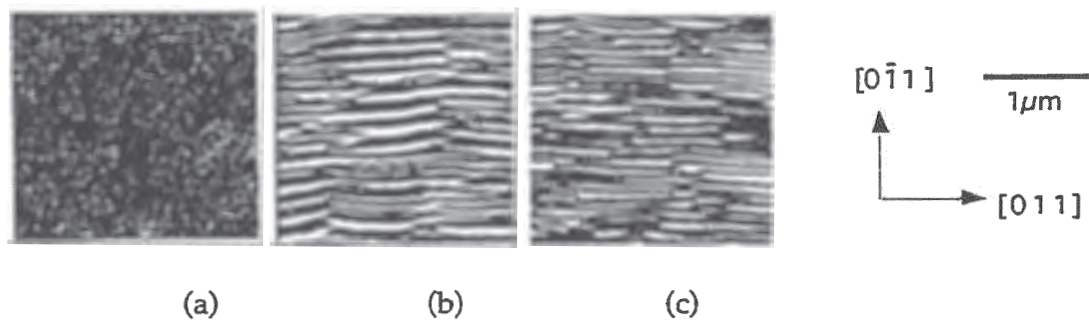


Figure 3.7 AFM images of the GaAs channel with different surface miscut angles, a) 0° , b) 3° , c) 6° towards the $\langle 111 \rangle_B$.

degree of miscut, from 5000, 2670 and 2100 $\text{cm}^2\text{volt}^{-1}\text{sec}^{-1}$ for on-axis, 3° and 6° samples, respectively. Similar electron mobilities were observed with conduction parallel or perpendicular to the direction of the step bunching.

3.5 GaInP Epitaxial Growth

Disordered $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}$ barriers latticed matched to GaAs provide larger conduction band offsets (ΔE_c) compared to $\text{Al}_{0.22}\text{Ga}_{0.78}\text{As}$ (230 meV to 180 meV), where the Al content is limited to 22 % due to problematic active DX trapping centers. Assuming a type I heterostructure and that 50% of the band gap difference between GaInP and GaAs forms in the conduction band discontinuity, even greater offsets are possible with pseudomorphic $\text{Ga}_{0.65}\text{In}_{0.35}\text{P}$ barriers (340 meV), thereby increasing the 2DEG concentration and confinement in the channel [5]. Disordered $\text{Ga}_x\text{In}_{1-x}\text{P}$ band gaps were measured from room temperature PL emissions in the compositional range from $0.4 < x < 0.6$ and correlated with X-ray analysis. The gallium mole fraction in the solid was determined from X-ray rocking curves and plotted against peak PL energy as shown in Figure 3.8. Also shown is the calculated energy in the direct band gap region for $\text{Ga}_x\text{In}_{1-x}\text{P}$ from [6]:

$$E_g(\text{eV}) = 1.351 + 0.643x + 0.786x^2 \quad 3.1$$

which fits the data well. The conduction band discontinuity is also plotted for different compositions of $\text{Ga}_x\text{In}_{1-x}\text{P}$ to a GaAs and a $\text{Ga}_{0.65}\text{In}_{0.35}\text{As}$ channel.

Advantages of a pseudomorphic $\text{Ga}_{0.65}\text{In}_{0.35}\text{As}$ channel include higher electron drift velocity compared to GaAs and a larger ΔE_c to $\text{Ga}_x\text{In}_{1-x}\text{P}$ used for the barrier. This leads to higher electron mobility and larger 2DEG densities

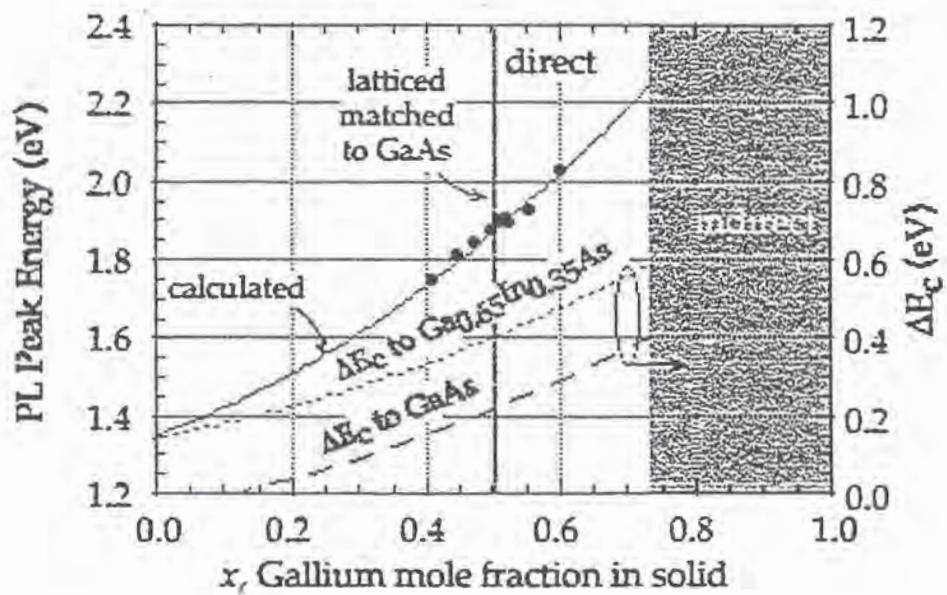


Figure 3.8 Measured GaInP peak PL energies and conduction band discontinuity versus Ga mole fraction (lower two curves).

at the heterostructure. In the case of a $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{Ga}_{0.65}\text{In}_{0.35}\text{As}/\text{GaAs}$ structure, ΔE_c is estimated to be 340 meV and with a strained $\text{Ga}_{0.65}\text{In}_{0.35}\text{P}$ barrier, ΔE_c as large as 525 meV can be achieved. Simulated 2DEG profiles of a single-sided doped transistor using C-band [1,5] predict a maximum sheet density of $0.6 \times 10^{12} \text{ cm}^{-2}$, $1.96 \times 10^{12} \text{ cm}^{-2}$, and $2.35 \times 10^{12} \text{ cm}^{-2}$ for structures with GaInP latticed matched to GaAs, latticed matched GaInP to a $\text{Ga}_{0.65}\text{In}_{0.35}\text{As}$ channel, and strained $\text{Ga}_{0.65}\text{In}_{0.35}\text{P}$ with a $\text{Ga}_{0.65}\text{In}_{0.35}\text{As}$ channel, respectively.

3.5.1 GaInP Growth Temperature

Although GaInP growth at low temperatures can result in rough surfaces, it promotes atomic disordering and simplifies formation of the required arsenide to phosphide interface [7]. The deposition temperature for GaInP in this work was varied from 530° C to 590° C, a range not typically exploited due to difficulties encountered with low temperature GaInP growth. Room temperature PL emissions were measured to determine the effect of growth temperature on band gap narrowing associated with ordering. As shown in Figure 3.9, there is only a 9 meV reduction the band gap going from 530° C to 550° C, but the PL intensity increased by more than a factor of 3, indicating an significant improvement in material quality. Further increases in growth temperature promote atomic ordering leading to an unacceptable decrease in band gap energy. Even though the PL emission intensity continues to increase with temperature (ordering) suggesting improved crystal quality, the transistor structures grown for this work were grown at or below 550° C to utilize the larger conduction band discontinuity at the heterostructure.

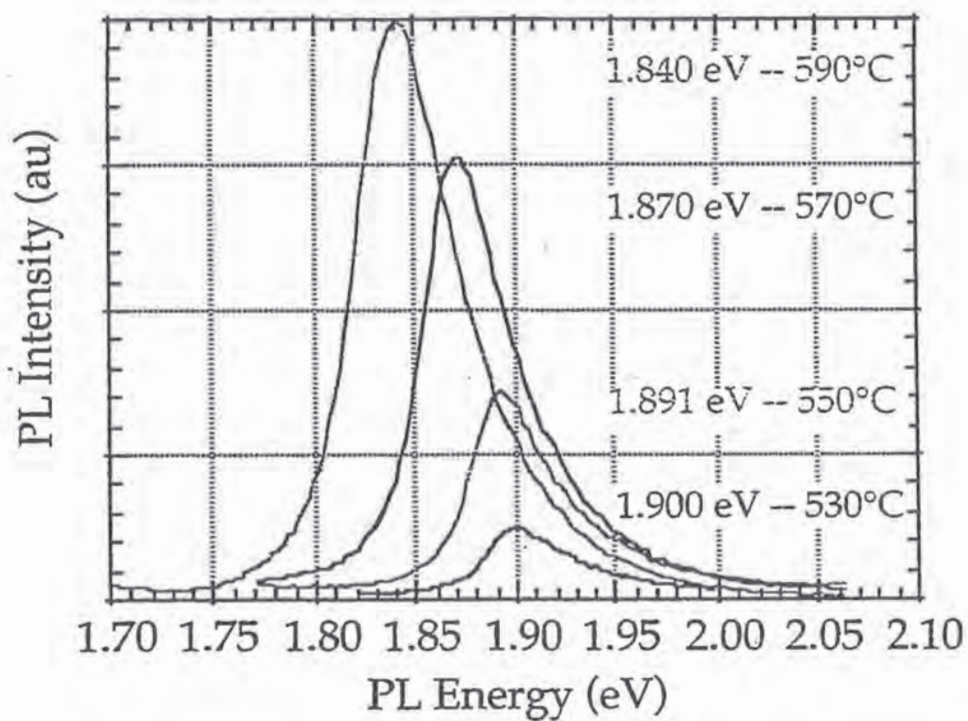


Figure 3.9 Measured GaInP peak PL energies versus growth temperature. Calculated band gap energies along with growth temperatures are given to the right.

3.5.2 Effects of Substrate Surface Miscut on GaInP

Band gap narrowing was also investigated on substrates with surface mis-orientation of 3° and 6° towards the $\langle 111 \rangle_B$, since atomic disordering of GaInP has been reported to increase with substrate miscut [8-10]. Numerous studies proposed that the Cu-Pt ordered structure forms at the surface during growth [8-14]. The related surface kinetics can be strongly influenced by two factors, the structure of the surface during growth (reconstruction, steps, step-bunching, kinks, and annealing effects), and the surface diffusion and attachment of species into the ordered "sub-lattice site". The former factors will largely determine the effects of substrate mis-orientation, especially surface reconstruction and annealing effects in the flow modulation growth technique and growth temperature employed. As the substrates are rotated out of the group-III rich growth zone, adatoms on the surface have time to find their lowest energy configuration (ie. ordered structure as seen by the surface) before being covered by the following layers when rotated back into the growth zone. This is also confirmed by the fact that rotating the samples faster leads to more disordered material. At the lowest growth temperature investigated (530°C) all three surfaces produced disordered material as evident from the band gap energies near 1.90 eV. This is expected since the adatom migration lengths are minimized at lower growth temperatures. As the growth temperature is increased, the GaInP becomes more ordered, especially on the miscut surfaces as seen in Figure 3.10. At any given growth temperature, the on-axis samples produce the most disordered crystals with the 3° and 6° samples showing similar band gap narrowing. This is contradictory to reported results and is an artifact of the flow modulation schemes with surface annealing during the growth cycle used in this work.

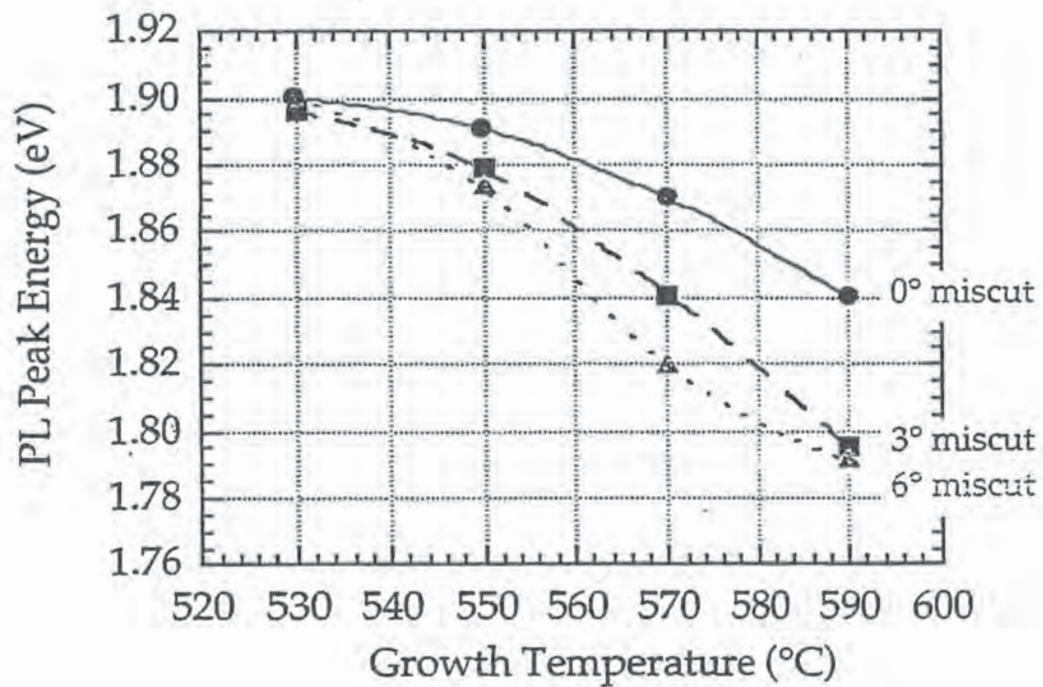


Figure 3.10 Measured GaInP peak PL energies versus GaInP growth temperature with varying substrate surface miscut toward $\langle 111 \rangle_B$. Miscut angle given to the right.

3.6 GaInAs Growth

GaInAs films can be used for the channel of the device. The $\text{Ga}_{0.65}\text{In}_{0.35}\text{As}$ is always in compression when grown on relaxed GaAs and should not exceed its critical thickness calculated to be 72 Å from equation 2.1. Advantages with $\text{Ga}_y\text{In}_{1-y}\text{As}$ channels is seen in the increased electron saturation velocity as seen in Figure 3.11 [15], narrower band gap to increase ΔE_c compared to GaAs (Figure 3.8) and the ability for strain compensation using $\text{Ga}_x\text{In}_{1-x}\text{P}$ barriers in tension ($x > 0.51$). The $\text{Ga}_{0.65}\text{In}_{0.35}\text{As}$ pseudomorphic channel was varied from 40 Å to 120 Å. A 13% reduction in mobility along with a 21% decrease in sheet density was seen on 40 Å compared to 72 Å channels as a result of weaker carrier confinement. Channels beyond the critical thickness resulted in a reduction of mobility by as much as 60 % from the film forming defects as the critical thickness is exceeded. A summary of transport properties and device test results are given in Table 3.1

Table 3.1 Hall measurement and transistor test summary for devices fabricated with varying GaInAs channel thicknesses

GaInAs Channel Width Variation				
II1051 (OMVPE) → channel width = 120 Å			$\mu(\text{Hall}) = 1819 \text{ cm}^2/\text{Vs}$	$p(\text{Hall}) = 2.57 \times 10^{12}$
II1052 (OMVPE) → channel width = 40 Å			$\mu(\text{Hall}) = 4035 \text{ cm}^2/\text{Vs}$	$p(\text{Hall}) = 2.04 \times 10^{12}$
II1053 (OMVPE) → channel width = 72 Å			$\mu(\text{Hall}) = 4620 \text{ cm}^2/\text{Vs}$	$p(\text{Hall}) = 2.57 \times 10^{12}$
150 μm HEMT w/ SD=1 μm & Lg=0.25 μm				
II1051				
120A	Device ID	ft [GHz]	Ipeak [mA/mm] (I-V w/ Vg=0.5V)	Ipeak [mA/mm] (gm w/ Vds=3.0V & Vg=1.0V)
	1a2	88.93	496 (@ Vds=2.6V)	586.7
	1a3	100.4	518 (@ Vds=2.6V)	594
	1a4	93.52	498 (@ Vds=2.6V)	584
	1a5	105.1	****	610.8
	1a1	91.37	499 (@ Vds=2.9V)	591.4
	Average	95.864	502.8	593.4
II1052				
40A	1a2	79.13	498.5 (@ Vds=2.8V)	544.5
	1a3	82.76	482.9 (@ Vds=3.0V)	525.7
	1a4	79.96	481.1 (@ Vds=2.8V)	535.9
	1a5	79.4	472.6 (@ Vds=3.0V)	531.4
	Average	80.3125	483.8	559.4
III1053				
70A	1a2	109.6	561.6 (@ Vds=2.8V)	608
	1a1	110.5	562.1 (@ Vds=2.7V)	607.2
	1a4	106.9	555.3 (@ Vds=3.2V) heating	603.4
	1a5	108.8	556.5 (@ Vds=3.0V) heating	605.5
	Average	108.95	558.9	606

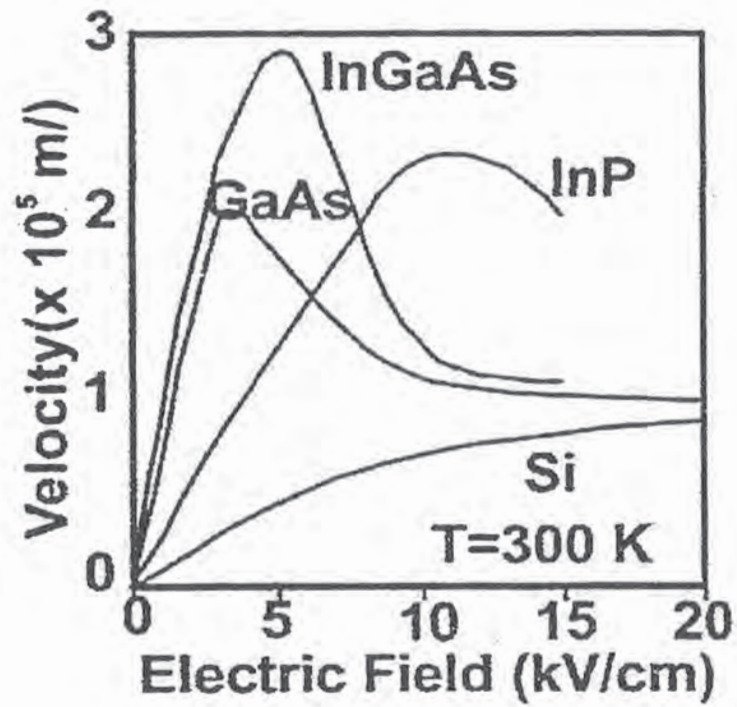


Figure 3.11 Velocity-Field Curves for GaAs, GaInAs, InP and Si at 300 K. After reference [15]

3.7 Summary

This chapter has described growth conditions and optimization of GaAs, GaInP and GaInAs films. Substrate chemical preparation as well as pre-growth annealing under arsine over-pressure was investigated to minimize mobile charge at the substrate/epitaxy interface. Growth temperature and V/III ratios were optimized in the GaAs buffer to improve crystal quality and minimize background carrier concentrations to produce highly resistive GaAs buffers. A two temperature (635° C/550° C) buffer was proposed to take advantage of high quality step flow growth GaAs while forming the GaAs (GaInAs) channel at 550° C needed for growth of the disordered GaInP supply layer and barrier. GaInP films were investigated through the growth temperature range from at 530° C to 590° C to promote atomic disordering. Films were optimized at 550° C which produced the device quality material with an acceptable band gap for GaInP/Ga(In)As HEMT's. Substrate miscut was investigated to determine its affects on crystal quality for GaAs and ordering for the GaInP. Contrary to reported literature, increasing surface miscut resulted in increasingly ordered material via PL measurements, especially as growth temperature increased. Flow modulation growth techniques employed in this work allow the surface time to reconstruct into Cu-Pt type ordering that is enhanced with increasing miscut. Finally, $\text{Ga}_{0.65}\text{In}_{0.35}\text{As}$ channels were grown at 550° C with varying thicknesses from 40 Å to 120 Å. Maximum low field 2DEG mobility and transistor performance was observed on structures with 72 Å thick $\text{Ga}_{0.65}\text{In}_{0.35}\text{As}$ channels. Optimization GaAs, GaInP and GaInAs will be utilized in complete HEMT structures to be addresses in Chapter 4.

Chapter 3 References

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CHAPTER 4

LOW TEMPERATURE GROWTH OF GaInP/GaAs AND GaInP/GaInAs/GaAs BASED HEMT'S

4.1 Introduction

Flow Modulation OMVPE is used to synthesize selectively doped GaInP/GaAs latticed-matched and GaInP/GaInAs/GaAs pseudomorphic heterostructures. Transport properties of the 2DEG are optimized for various single sided doping techniques, as well as channel and spacer layer thicknesses. A two layer GaAs buffer is deposited at 550° C and 635° C, while GaInP layers were grown at the lower temperature of 550° C to promote atomic disordering. Achieving high 2DEG densities involved incorporating several atomic doping layers (delta doping) as electron supply layers separated by thin GaInP regions. Finally, transistor test results are presented on devices with 0.25 μm X 100 μm gate geometries.

4.2 Epitaxial Device Design

The complete HEMT structure is shown in Figure 4.1. The 2DEG resides in the GaAs channel (latticed-matched) or the 72 Å thick $\text{Ga}_{0.65}\text{In}_{0.35}\text{As}$ channel (pseudomorphic) separated from the delta doped supply layer(s) by an undoped $\text{Ga}_x\text{In}_{1-x}\text{P}$ spacer. Details of the multiple delta doping scheme

employed are shown in the inset for clarity. On top of the delta doped region, an additional 160 Å thick undoped GaInP barrier was used to form the Schottky gate, while a 250 Å n+ Si:GaAs ($5 \times 10^{18} \text{ cm}^{-3}$) layer is deposited for the ohmic source/drain contacts. Details of the recessed gate device fabrication process is given in section 4.2.2.

4.2.1 Band Gap Engineering

Several aspects of the epitaxial design are crucial for high power and high frequency performance of the transistor. First, a large conduction band offset (ΔE_c) is desired at the channel/barrier heterostructure to confine the electrons in the 2DEG and provide a deeper quantum well to increase electron density. Secondly, the spacer layer separating the supply layer from the channel has to be optimized for a) sufficient electron transfer to the channel and b) adequate separation of the donors from the channel to minimize ionized impurity scattering. Finally, the barrier layer has to be relatively thin to increase modulation efficiency (frequency response) while minimizing depletion of the 2DEG from the surface.

Simultaneously solving Poisson and Schrödinger's equations using C-band code [1,2] predicts a 2DEG density of $0.60 \times 10^{12} \text{ cm}^{-2}$, $1.96 \times 10^{12} \text{ cm}^{-2}$ and $2.35 \times 10^{12} \text{ cm}^{-2}$ in the $n=1$ state for lattice matched $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{GaAs}$, lattice matched $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}$ to a strained (compression) $\text{Ga}_{0.65}\text{In}_{0.35}\text{As}$ channel and a strained (tensile) $\text{Ga}_{0.65}\text{In}_{0.35}\text{P}/\text{Ga}_{0.65}\text{In}_{0.35}\text{As}$ structure, respectively. In the case of a $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{GaAs}$ structure, ΔE_c is estimated to be 260 meV, a $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{Ga}_{0.65}\text{In}_{0.35}\text{As}/\text{GaAs}$ structure, ΔE_c is estimated to be 340 meV and with a strained $\text{Ga}_{0.65}\text{In}_{0.35}\text{P}$ barrier, ΔE_c as large as 525 meV can be achieved as shown in Figure 4.2.

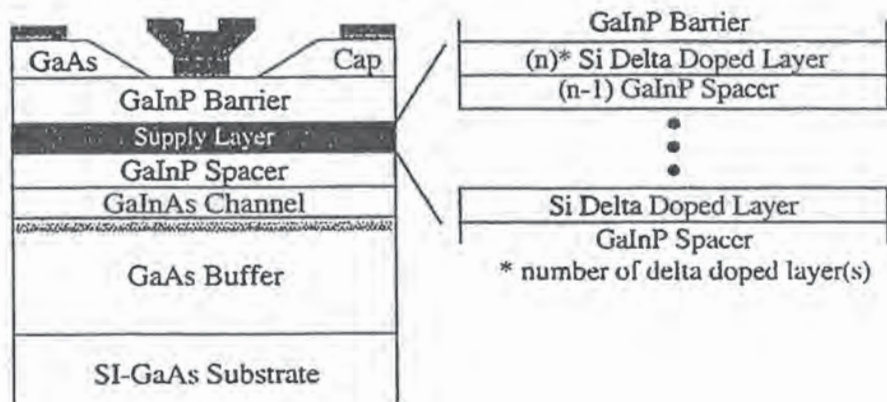


Figure 4.1 Cross section of the HEMT structure. Details of the delta doped supply layers are given to the right.

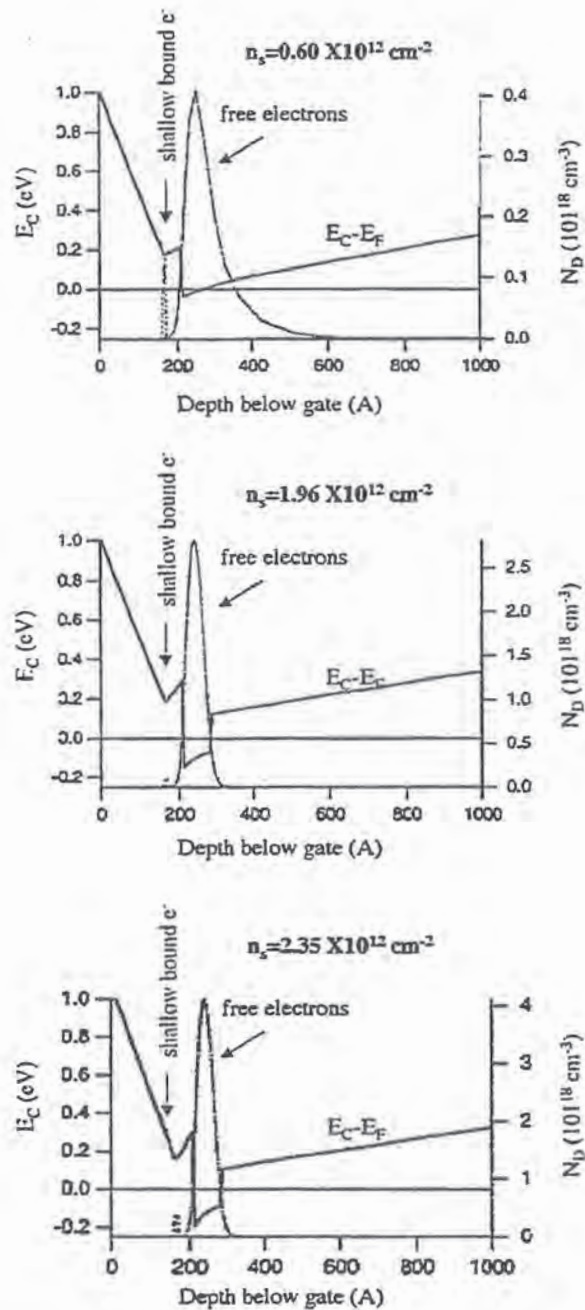


Figure 4.2 Conduction band profiles as calculated from C-band. Supply layer is represented by shallow bound electrons and the free electrons make up the 2DEG in the channel. The top figure is for lattice matched GaInP/GaAs, the middle figure is for lattice matched GaInP to a GaInAs channel and the bottom figure is strained GaInP to a GaInAs channel.

4.2.2 Device Fabrication Process

Device structures were fabricated through a three-level process, which required both optical photolithography and e-beam writing along with standard liftoff procedures to define the source, drain, and recessed gate. A GCA g-line 5:1 stepper was used for defining both the mesa structure for device isolation and the contact pads for the source, drain and gate. The 1000 Å deep mesa structure was fabricated using a non-selective acetic acid based etch. Ohmic contacts for the source and drain incorporated a Ni/AuGe/Ag/Au metallization, evaporated onto the n⁺-GaAs cap layer and subsequently annealed at 400° C for 10 seconds in an N₂/Ar environment. Source-to-drain spacing varied from 2 μm to 10 μm while the source-to-gate spacing was nominally maintained at 0.5 μm to minimize source resistance and improve frequency response. The recessed gate structures with a gate length of 0.25 μm and gate width of either 50 μm, 75 μm, 100 μm or 150 μm were written using the Cambridge EBMF e-beam system. A PMMA-based tri-layer resist was used to define the characteristic “mushroom-shape” of these gates. The recessing of the gate into the GaInP barrier layer was done with a 300:1 selective phosphoric acid-based etch. Ti/Pd/Au metallization with no annealing was used as the mushroom-shaped Schottky gate to reduce gate resistance as shown in the SEM image presented in Figure 4.3 [3]. “T” gate structures with gate width of 100 μm were fabricated as standard test structures as shown in the bottom image in Figure 4.3.

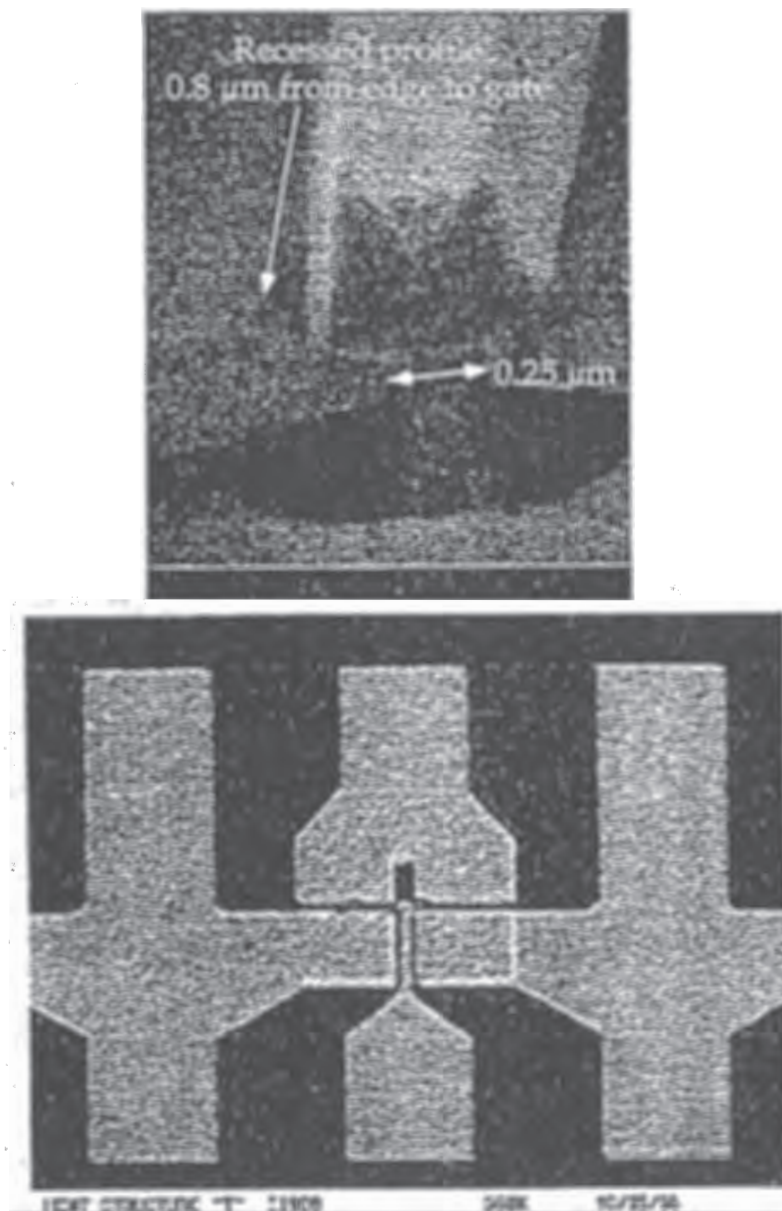


Figure 4.3 SEM image of mushroom gate structure (top image) and top view of a "T" gate transistor (bottom image).

4.3 GaInP/GaAs and GaInP/GaInAs Heterostructure Formation

Interface formation at the arsenide/phosphide transition can significantly influence the energy profile of the quantum well channel. The intermixing of AsH₃ and PH₃ result in either unwanted ternaries (GaAsP) or quaternaries (GaInAsP), which decrease the conduction band offsets and reduces the confinement of the 2DEG, degrading the performance of the transistor. A growth stop was inserted at the channel/barrier transition, where the group III species were switched out then the group V source was switched out and a H₂ purge was inserted to sweep out the residual AsH₃. Phosphine was then switched in before the Ga and In for the GaInP barrier. The growth stop occurs at the Ga(In)As channel at the growth temperature of 550° C well below the congruent sublimation temperature. A GaInP/GaAs multiple quantum well (QW) structure was used as a test vehicle for varying the H₂ purge time. GaAs QW targeted at 19 Å, 38 Å and 60 Å were grown with 500 Å GaInP barriers. While making the arsenide/phosphide transition, the H₂ purge time was varied from 6 seconds to 90 seconds. A red shift was observed in the low temperature (1.6° K) PL spectra for the shorter purge times indicating the formation of arsenide/phosphide compound. This is shown in the top plot in Figure 4.4 with the inset indicating the switching scheme used. Since the 2DEG resides in the top 100 Å of the channel, caution must be taken not to roughen the interface, which would reduce the low field electron mobility and electron saturation velocity. To check the interface quality, the single delta doped test structure discussed in Chapter 3 was used with the 6, 45 and 90 second purge times at the GaInP/GaAs heterostructure. Peak electron mobility and 2DEG density were observed at the 45 second

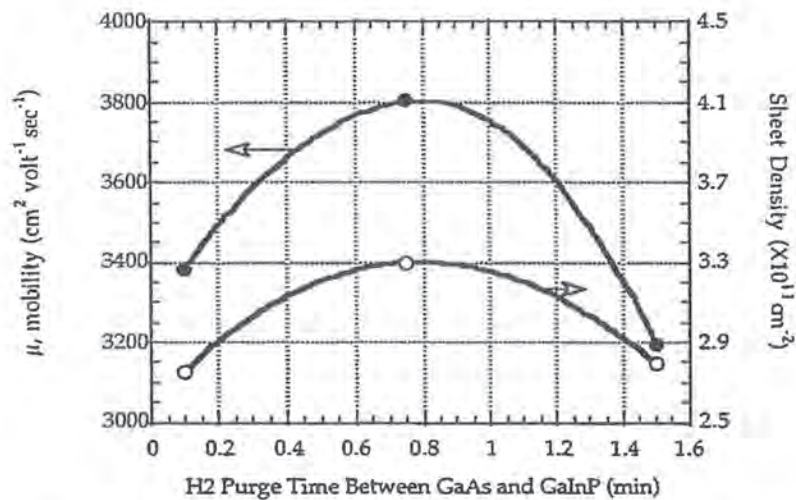
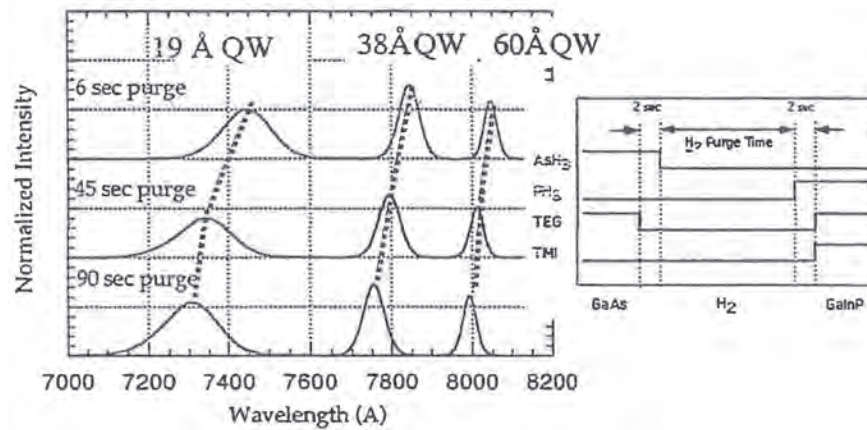


Figure 4.4 Top graph shows 1.6° K PL spectrum of GaInP/GaAs QW's. A red shift is observed as the hydrogen purge time is decreased indicating intermixing and a lowering of the QW energy level. Bottom graph represent room temperature mobilities and sheet density of abbreviated HEMT structures with varying purge times.

purge time as shown in the bottom plot in Figure 4.4. The 6 second purge time results in intermixing, while the 90 second purge time could either introduce impurities, defects and/or roughening of the interface, which would contribute to the lower mobility and electron density. All remaining structures for this work incorporated the 45 second purge at the AsH₃/PH₃ interface.

4.4 Spacer and Supply Layers

In order to achieve the high 2DEG density predicted by C-band calculation, supply and spacer layers in the barrier had to be designed to provide adequate electron transfer to the QW channel. As the undoped spacer layer is thinned to 0 Å the ionized impurity scattering from the donors (Si) degrade the transport properties of the 2DEG. If the spacer layer is too thick, insufficient electron transfer will result giving lower than desired electron density (low current – low power devices).

4.4.1 Undoped GaInP Spacer Layer

Spacer layer thickness was varied from 25 Å to 150 Å while keeping the delta doped supply layer at a constant doping level. The highest 2DEG density was observed at the thinnest spacer layer practical (25 Å) resulting in a sheet charge of $2.7 \times 10^{12} \text{ cm}^{-2}$ as seen in Figure 4.5. As the spacer layer thickness increases, transfer of electrons to the QW channel is less efficient and falls off linearly as:

$$n_s = (2.895 - 0.00828Sp_{\text{thick}}) \times 10^{12} \text{ cm}^{-2} \quad 4.1$$

where, Sp_{thick} is the undoped spacer layer thickness in cm.

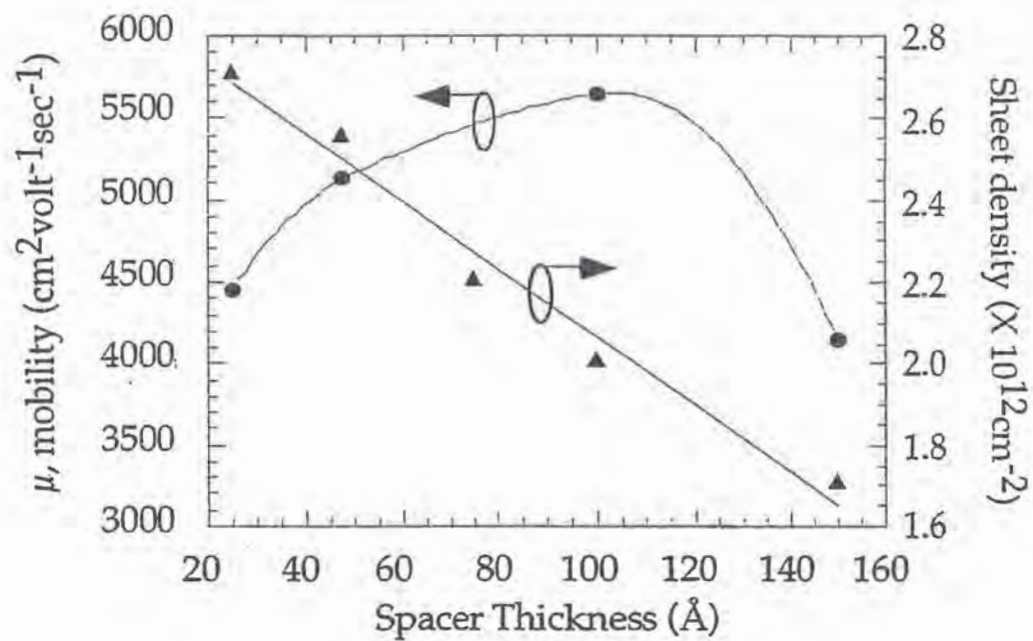


Figure 4.5 Effects on 300 K electron mobility and 2DEG density with varying GaInP spacer layer thickness.

The room temperature electron mobility peaks at a spacer layer thickness of 100 Å. However, the resulting 2DEG density is lower than desired due to the inefficient electron transfer from the supply layer as observed in Figure 4.5. For HEMT's, the mobility sheet density product ($\mu \cdot n_s$) is the more important parameter that defines the channel resistance R_s (Ω/sq) as:

$$R_s = 1/(q\mu n_s) \quad 4.2$$

The $\mu \cdot n_s$ product peaks at a spacer thickness around 50 Å. As the spacer layer becomes thinner, ionized impurity scattering begins to limit the electron mobility and thicker spacer layers increase the number of free electrons present in the GaInP barrier (parallel conduction in the barrier), which has lower mobility than the channel region. Maximum channel conductance was obtained at a spacer thickness of 50 Å with a mobility of $5100 \text{ cm}^2\text{volt}^{-1}\text{sec}^{-1}$ and the required 2DEG density of $2.6 \times 10^{12} \text{ cm}^{-2}$.

4.4.2 Delta Doped Supply Layers

In order to achieve the high 2DEG density, a sufficient density of donors needs to be present in the supply layer. Common practice is to lower the GaInP growth rate and increase the donor flux to incorporate the maximum number of donors in the supply layer, dope the channel region [4] or add aluminum to the barrier material [5]. Initial efforts on a continuously doped supply layer grown at a reduced GaInP growth rate from 70 Å/min to 17 Å/min produced a 2DEG density of only $3.0 \times 10^{11} \text{ cm}^{-2}$.

4.4.2.1 Single Delta Doped Supply Layers

By using an abbreviated HEMT structure as a test vehicle, it was possible to optimize Si delta doping by varying the dopant exposure time during the GaInP growth stop from 30 seconds to 600 seconds. With silane concentrations of 200 ppm, the 2DEG densities saturates at $1.65 \times 10^{12} \text{ cm}^{-2}$ after 600 seconds of exposure. Increasing the silane concentration to 2000 ppm, no saturation was evident up to the 600 seconds exposure time as shown in Figure 4.6. A maximum 2DEG density of $2.35 \times 10^{12} \text{ cm}^{-2}$ was achieved with this single delta doped layer with the 600 seconds (10 minutes) silane dose during the growth stop at the supply layer.

Silicon is amphoteric, it can incorporate in the crystal on either the group III or group V sub-lattice depending on the growth conditions. Both p- and n- type doping can occur by changing the V/III ratio while keeping all other growth parameters the same [6,7]. For n-type doping, high V/III ratios will promote incorporation onto the group III site and for delta doping the group V flux is maximized at the growth stop (group III » 0) prior to introduction of the Si source (silane) to quench the group V sites. However, as the Si flux is increased, a point is reached where the net electron concentration begins to be compensated by Si atoms residing on the group V site (p-type). A linear increase in electron concentration is observed as the Si flux is increased as:

$$N_D - N_A = [-0.8517 + 0.0630 (\text{SiH}_{4\text{flow}})] \times 10^{17} \text{ cm}^{-3} \quad 4.3$$

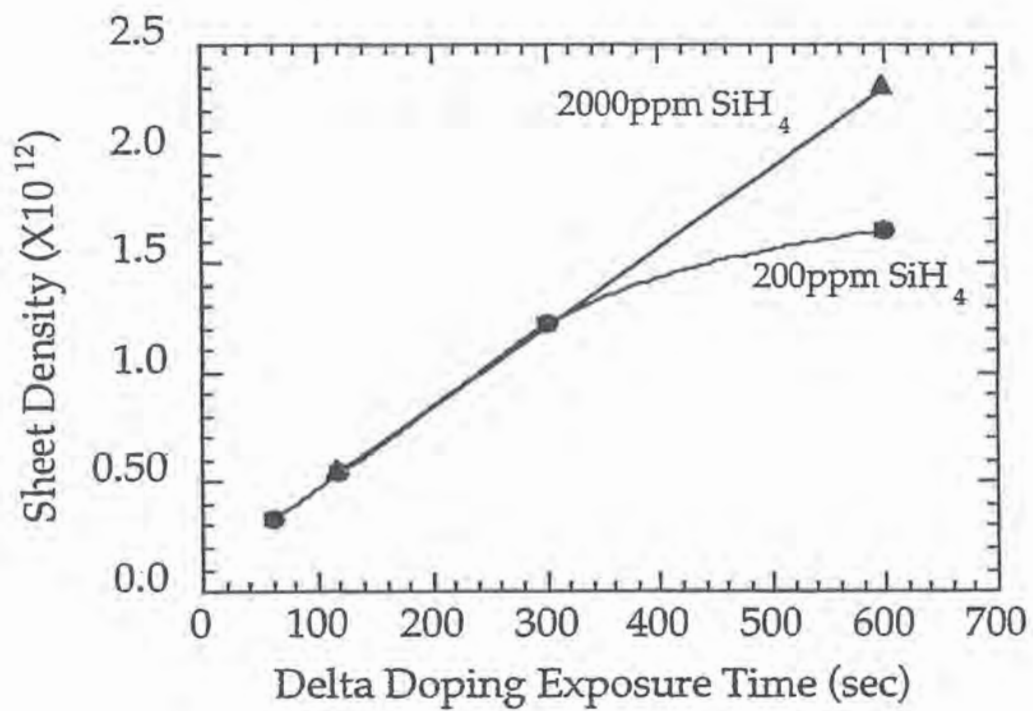


Figure 4.6 2DEG densities achieved at varying silane exposure times with 200 ppm and 2000 ppm silane concentration diluted in hydrogen.

where, SiH_4/flow equals the full range of mass flow controller setting (% - 0.00 to 1.00). This takes into account using a 100 sccm mass flow controller and silane diluted 2000 ppm in H_2 as the supply gas.

The relationship defined by equation 4.3 holds until the silicon begins to occupy the group V sites and compensate out the electrons. As this happens the net free electron concentration decreases as shown in Figure 4.7. As the flux increases above 75 %, acceptor compensation reduces the free electron concentration (data point seen at 100 % flow).

4.4.2.2 Multiple Delta Doped Supply Layers

To achieve a higher electron density, multiple delta doped layers were incorporated between thin (2-3 monolayers) GaInP layers for the supply layer as depicted in the inset of Figure 4.1. Initially, a test structure was grown with 3 delta doped layers in lattice matched GaInP to verify the doping levels and to investigate any lateral diffusion of the donors. Target depths for the placement of the delta doped layers were 2500 Å, 3000 Å and 3600 Å from the surface. Derived carrier concentration versus depth from C-V measurements is shown in the top graph in Figure 4.8. The three delta doped layers are observed at 2250 Å, 2850 Å and 3500 Å. The delta doped layers were formed by stopping the growth (switch out the group III species) while flowing phosphine and introducing silane. The silane exposure time was 2 minutes at each delta doped layer and the flux varied from 3.7×10^{-8} moles/sec, 7.4×10^{-8} moles/sec to 1.1×10^{-7} moles/sec, resulting in local peak volume concentrations of $7.2 \times 10^{16} \text{ cm}^{-3}$, $1.38 \times 10^{17} \text{ cm}^{-3}$ and $1.42 \times 10^{17} \text{ cm}^{-3}$,

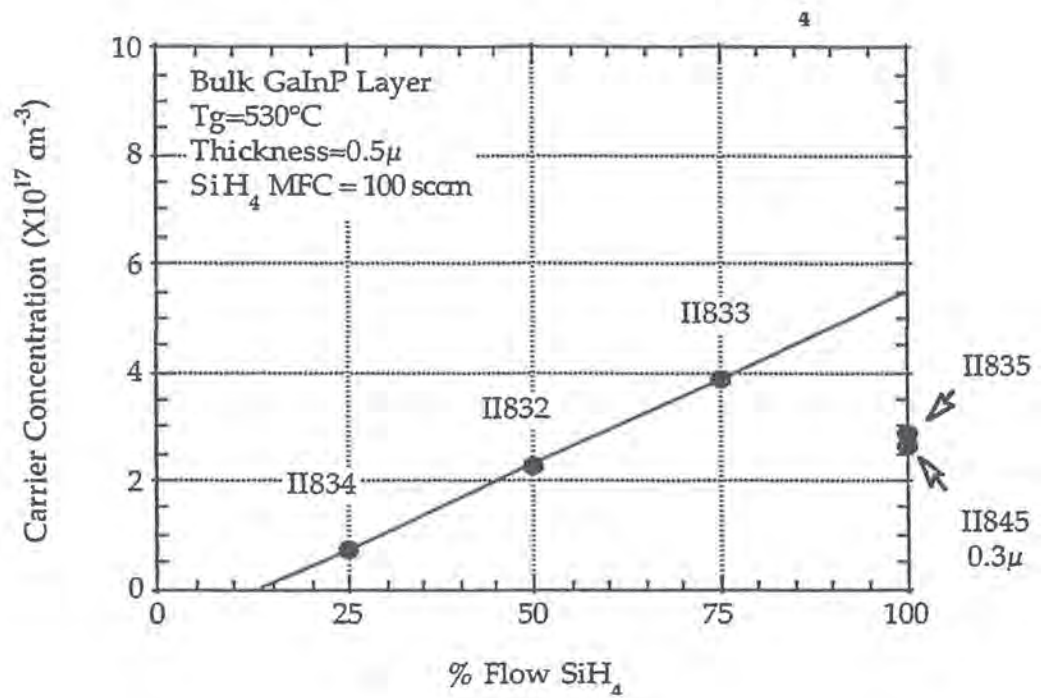


Figure 4.7 Carrier concentration ($N_D - N_A$) versus silane flux for thick layers of GaInP. As the Si starts incorporating on the group V sub-lattice, the free electron concentration decreases (seen at 100 % flow).

respectively. Since three distinct spikes are detected with approximately 600 Å separation, lateral diffusion does not appear to be an issue.

Rearranging equation 2.11, it is seen that slope of the inverse of capacitance squared corresponds to a straight line when the doping concentration is uniform throughout the sample. Equation 4.4 indicates that the slope when divided into $(2/q\epsilon)$ gives $N(x)$ directly.

$$N(x) = -\frac{2}{q\epsilon \left[\partial(1/C^2) / \partial V_a \right]} \quad 4.4$$

Since a small increase in V_a causes a small decrease in capacitance, the slope at any given point along the curve will supply information about the doping at the specific region of the sample for non-uniform doping profiles. The lower graph in Figure 4.8 gives the $1/C^2$ plot versus reverse bias for the test sample. The breaks in slope corresponds to the three delta doped regions as pointed out by the arrows.

Next, HEMT structures were grown with the optimized conditions while varying the number of delta doping layers in the supply region. A 120 second dopant exposure time was chosen for the delta doping while under a high phosphorus over pressure. Up to eight separate doping layers were deposited with approximately 10 Å of undoped GaInP separating the atomic doping layers. The 2DEG density increased linearly from $2.7 \times 10^{11} \text{ cm}^{-2}$ for

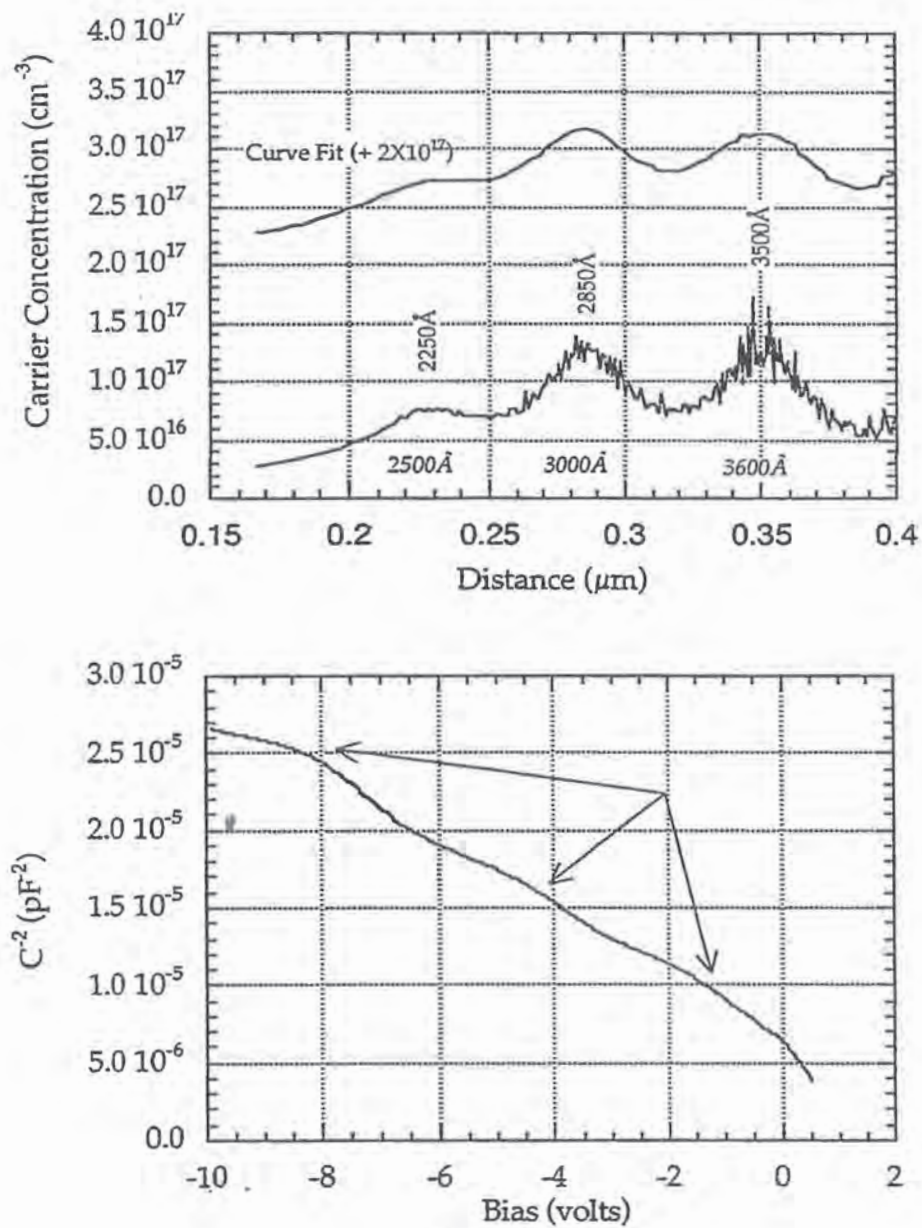


Figure 4.8 Top plot shows carrier concentration derived from C-V measurements versus depth into the structure. Top line is an offset curve fit to the data. Lower plot gives the $1/C^2$ versus bias showing three distinct features corresponding to the delta doped layers.

one delta doped layer to $3.1 \times 10^{12} \text{ cm}^{-2}$ for eight layers as:

$$n_s(x) = (3.977x - 0.465) * 10^{11} \text{ cm}^{-2} \quad 4.5$$

where, x is the number of delta doped layers in the supply region.

Electron density versus number of delta doped layers is shown graphically in Figure 4.9. Increasing the number beyond eight delta doped layers showed no increase in 2DEG density and was detrimental to the room temperature low field mobility. Either the $n=2$ sub-band began filling causing intra-subband scattering, or the electron transfer to the channel was incomplete leading to parasitic conduction in the lower mobility GaInP barrier.

4.5 Lattice Matched GaInP/GaAs Structures

First structures incorporated a GaAs channel with lattice matched $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}$ barrier layer and a delta doped supply layer. This structure should have the smallest conduction band offset and the lowest 2DEG density of the three studied. This structure was used to optimize all aspects of the epitaxial profile, incorporating the growth conditions discussed previously in Chapter 3 and Chapter 4. Both room temperature and 77° K Hall effect measurements were performed to monitor the low field electron mobilities and sheet density of the 2DEG as well as any unwanted electrons that freeze out at the lower temperature. Hall measurements show room temperature mobilities of $6,700 \text{ cm}^2\text{volt}^{-1}\text{sec}^{-1}$ with a sheet density of $4.3 \times 10^{11} \text{ cm}^{-2}$. Low

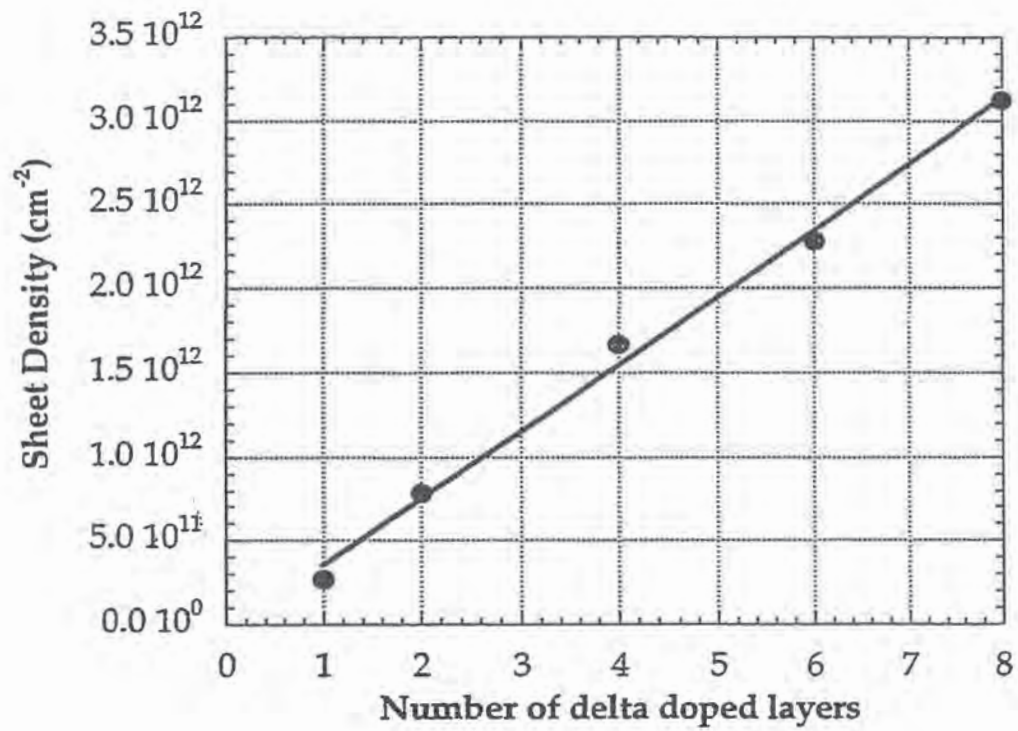


Figure 4.9 2DEG density versus the number of delta doped layers inserted in the supply region of the barrier.

temperature (77° K) Hall measurements yield electron mobilities of 24,700 $\text{cm}^2\text{volt}^{-1}\text{sec}^{-1}$ with a sheet density of $4.1 \times 10^{11} \text{ cm}^{-2}$. (run II908) The slight reduction in sheet density indicates that some charge is frozen out either in the barrier, buffer or substrate/epitaxy interface. The 2DEG density is a little lower than the calculated value of $6.0 \times 10^{11} \text{ cm}^{-2}$ given in Figure 4.2 most likely due to insufficient donor incorporation in the supply layer.

4.6 Pseudomorphic GaInP/GaAs Channel Structures

The next evolution of the transistor structure incorporated a strained $\text{Ga}_{0.65}\text{In}_{0.35}\text{P}$ barrier layer with a GaAs channel to increase the conduction band offset and the 2DEG density. Hall measurements show room temperature mobilities of 5,010 $\text{cm}^2\text{volt}^{-1}\text{sec}^{-1}$ with a sheet density of $1.67 \times 10^{12} \text{ cm}^{-2}$. C-band calculations yielded a 2DEG density of $1.96 \times 10^{12} \text{ cm}^{-2}$. Once again the lower electron density is must likely caused by insufficient donor concentration in the supply layer. Low temperature (77° K) Hall measurements yield mobilities of 21,200 $\text{cm}^2\text{volt}^{-1}\text{sec}^{-1}$ with a sheet density of $1.51 \times 10^{12} \text{ cm}^{-2}$ (run II914). The lower mobility compared to the latticed matched structure is due to intra-subband scattering, parasitic charge in the barrier and/or roughening of the heterostructure from growth of the strained $\text{Ga}_{0.65}\text{In}_{0.35}\text{P}$.

4.7 Pseudomorphic GaInP/GaInAs/GaAs Structures

The final structure investigated used a strained barrier and strained channel in a $\text{Ga}_{0.65}\text{In}_{0.35}\text{P} / \text{Ga}_{0.65}\text{In}_{0.35}\text{As} / \text{GaAs}$ transistor. This structure has the largest conduction band offset and should produce the largest 2DEG density of the HEMT structures studied. Measured transport properties yielded a

electron mobility of $4,940 \text{ cm}^2\text{volt}^{-1}\text{sec}^{-1}$ with a sheet density of $2.28 \times 10^{12} \text{ cm}^{-2}$ (run II915) compared to the calculated density of $2.35 \times 10^{12} \text{ cm}^{-2}$.

4.8 Device Test Results

Standard dc analysis of these devices were carried out using an HP4145 while S-parameter measurements providing small signal RF results from 45 MHz to 25.6 GHz were done on an HP 8510C. Limited amount of large signal test data is available and resulted in Class A power densities of approximately 0.5 W/mm at 10 GHz at a drain bias as high as 8 volts. Device characteristics are given for the $\text{Ga}_{0.65}\text{In}_{0.35}\text{P}/\text{Ga}_{0.65}\text{In}_{0.35}\text{As}/\text{GaAs}$ structure only.

4.8.1 Static Test Results

A typical family of I-V curves for a $\text{Ga}_{0.65}\text{In}_{0.35}\text{P}/\text{Ga}_{0.65}\text{In}_{0.35}\text{As}/\text{GaAs}$ transistor is shown in Figure 4.10 with the gate bias given to the right. This transistor had low source-drain isolation of roughly $40 \text{ k}\Omega$ measured between ohmic pads separated by the $1000 \text{ \AA}$ mesa etch. The poor isolation and soft pinch-off characteristics indicate free carriers in the buffer or substrate/epitaxy interface that is not accessible with reasonable gate biases. Another indication of poor isolation is the positive output conductance observed in the I-V characteristics, especially in the lower I_{ds} regions where self-heating is not as pronounced (ie. -0.1 volt to -0.5 volt on the gate). Ideally, isolation measurements should yield resistance in the mega-ohm range.

At a gate bias of $+0.5$ volt, the I_d is measured at 430 mA/mm and the device exhibits a knee voltage near 1 volt. The device has a pinch-off voltage of approximately -0.7 volt with an undesired drain leakage current of 30

mA/mm. From this, the estimated power density in Class A operation, at a bias of 8 volts is 0.75 W/mm and was measured near 0.5 W/mm at 10 GHz.

Device transconductance is the change in drain current associated with a change in gate bias and is a measure of gain in the device. This is represented in the bottom graph in Figure 4.10 and by equation 4.6 below:

$$g_m = \frac{\partial(I_D)}{\partial(V_G)} = \frac{\Delta I_D}{\Delta V_G} \quad 4.6$$

Transconductance approaches the slope of the I-V curve when the step size is very small. Maximum transconductance of 450 mS/mm was measured for this device.

4.8.2 RF Test Results

Small signal testing performed at maximum g_m ($V_{gs} \pm 0.2$ V) yielded f_T of 110.5 GHz and f_{MAX} of 160 GHz for $0.25 \mu\text{m} \times 100 \mu\text{m}$ gate geometries as shown in Figure 4.11. Maximum associated gain was measured near 28 dBs.

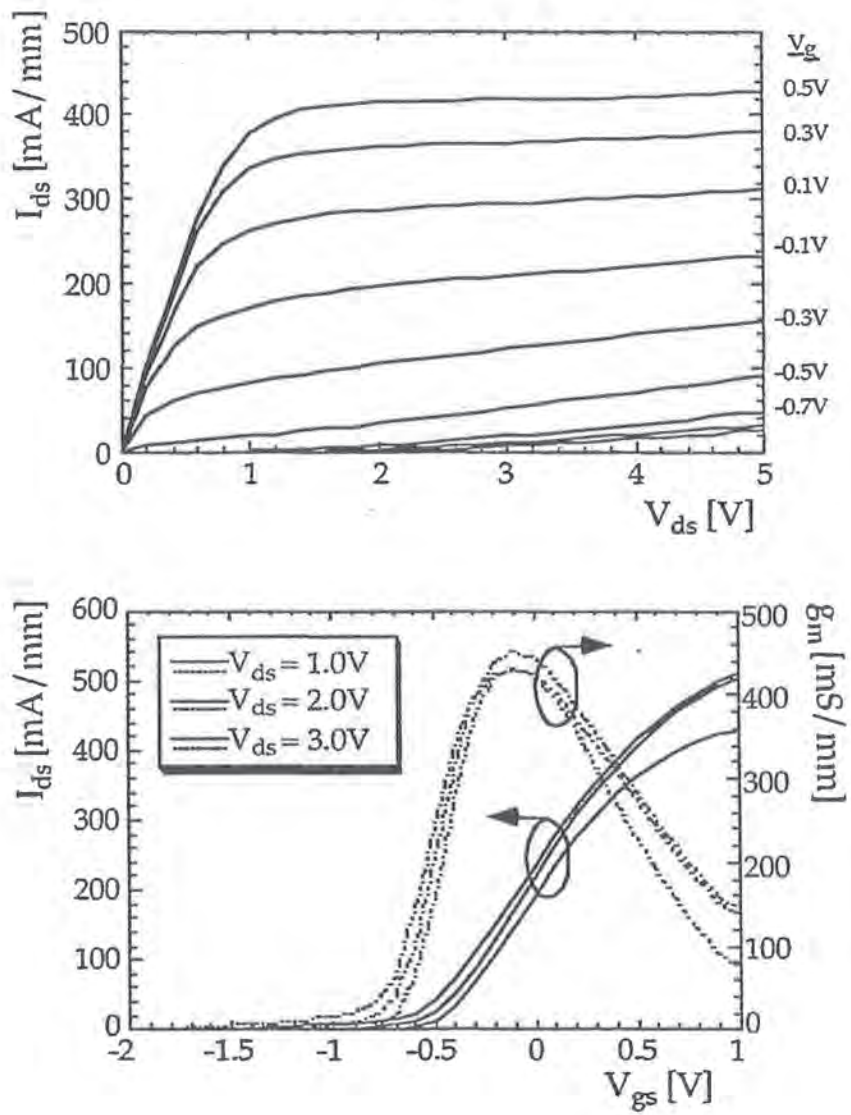


Figure 4.10 I-V curves of a GaInP/GaInAs/GaAs pseudomorphic HEMT given in the top graph with the corresponding transfer characteristics give in the lower plot.

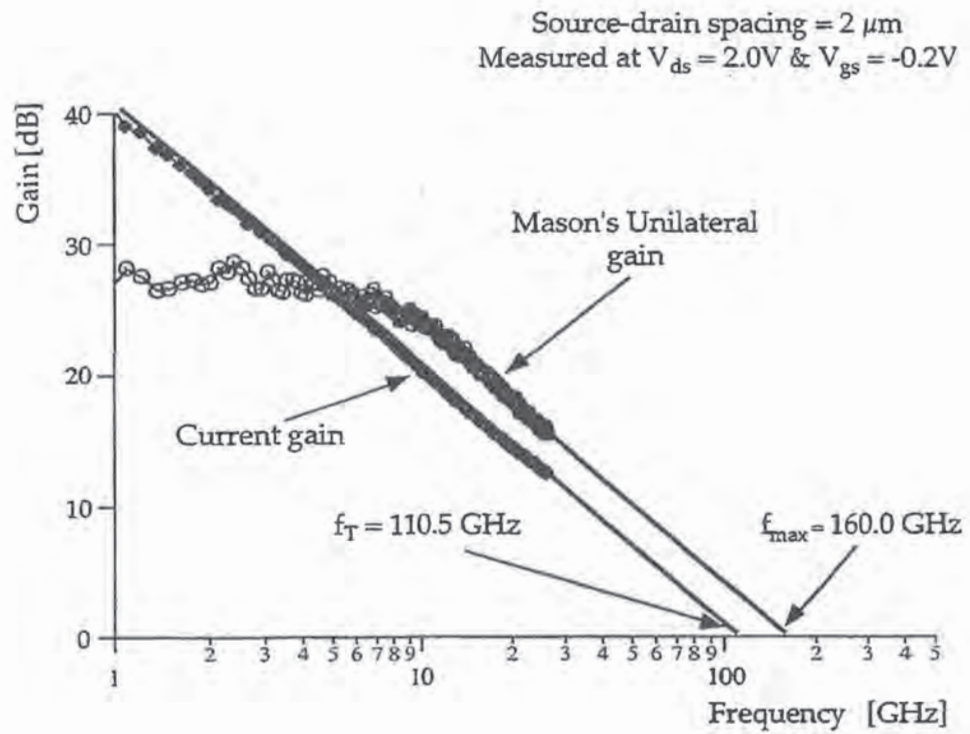


Figure 4.11 RF response from HEMT with gate geometry of $0.25\ \mu\text{m} \times 100\ \mu\text{m}$.

4.9 Summary

Three different transistor structures were synthesized using FME OMVPE growth techniques, (1) lattice matched $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{GaAs}$, (2) lattice matched $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}$ to a strained (compression) $\text{Ga}_{0.65}\text{In}_{0.35}\text{As}$ channel and (3) a strained (tensile) $\text{Ga}_{0.65}\text{In}_{0.35}\text{P}/\text{Ga}_{0.65}\text{In}_{0.35}\text{As}/\text{GaAs}$. The predicted 2DEG densities and conduction band offsets are $0.60 \times 10^{12} \text{ cm}^{-2}$ & 260 meV, $1.96 \times 10^{12} \text{ cm}^{-2}$ & 340 meV and $2.35 \times 10^{12} \text{ cm}^{-2}$ & 525 meV for the three structures. A growth stop with a 45 second H_2 purge was inserted at the arsenide/phosphide interface to reduce intermixing and maintain the larger conduction band offset. A trade-off between electron transfer and ionized impurity scattering was established with varying GaInP spacer layer thicknesses. A spacer layer of 50 Å was chosen that produced the highest $\mu \cdot n_s$ product (lowest channel resistance).

Single and multiple delta doped layers were utilized for the supply layer and compared to a continuously doped supply layer structure. Silane concentration and exposure times were varied and a 2000 ppm concentration in H_2 and 2 minute exposure time was chosen. Multiple delta doping was successfully implemented using up to eight planar doping layers separated by 2-3 monolayers of GaInP within the supply layer. Test results are given for devices fabricated from stress compensated pseudomorphic $\text{Ga}_{0.65}\text{In}_{0.35}\text{P}/\text{Ga}_{0.65}\text{In}_{0.35}\text{As}/\text{GaAs}$ heterostructures yielding drain currents up to 430 mA/mm and g_m of 450 mS/mm (0.25 μm gate length). Small signal measurements yielded an $f_t=110$ GHz and $f_{\text{max}}=160$ GHz.

Chapter 4 References

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CHAPTER 5

AlGaN NUCLEATION AND GaN BUFFER GROWTH ON SiC AND SAPPHIRE SUBSTRATES

5.1 Introduction

Flow modulation epitaxy of GaN and related alloys represents a new approach for the synthesis of nitride based structures for high power RF electronics. Gallium nitride and related alloys have demonstrated great potential for short-wavelength optical devices [1] and high frequency high power electronics [2]. The lack of suitable GaN substrates for homoepitaxy makes the growth of device-quality heterostructures in this material system difficult. Efforts have been directed towards producing nucleation and buffer layers on mismatched substrates such as sapphire, SiC, and Silicon. Hexagonal GaN growth is commonly accomplished by a two-step process consisting of a thin low temperature GaN [3] or AlN [3,4] nucleation layer followed by a thick high-temperature GaN buffer. The high-temperature GaN initially grows three dimensionally as islands, which eventually coalesce into a planar film. Although the individual GaN islands may be free of defects, [5] when they coalesce structural and native defects form at the meeting surfaces contributing to a high free carrier background concentration in the range of $10^{16} - 10^{18} \text{ cm}^{-3}$ [3,6,7]. This defect-rich part of the GaN buffer is often thicker

than 5000 Å, resulting in excess of $1 \times 10^{12} \text{ cm}^{-2}$ unintentional sheet electron concentrations with low electron mobility. This charge forms a parasitic current path, which is not accessible by reasonable gate bias on laterally conducting HEMT's [8].

A single temperature process using AlGa_xN nucleation layers has been developed in this work that produces device-quality GaN-based materials with bi-layer atomic step surfaces. The AlGa_xN nucleation layer is deposited at temperatures in excess of 1000° C, where GaN and AlGa_xN films can be subsequently grown. This process has been optimized on both sapphire and SiC substrates, where the conditions for nucleation are found to be quite different. For growth on SiC, aluminum mole fractions ranging from 6 % to 35 % result in featureless surfaces. Optimizing the alloy composition and thickness of the nucleation layer on SiC allows the deposition of GaN buffer layers exceeding 5 μm without the formation of cracks. A minimum of 15 % aluminum in the nucleation layer is required for smooth growth on sapphire substrates to accommodate the larger mismatch between the epitaxy and sapphire. However with the higher aluminum content, degradation is observed in the room temperature transport properties of the 2DEG in the HEMT test structures on both substrate types.

A single, high temperature process has been developed using Al_xGa_{1-x}N films as nucleation layers on both sapphire and SiC which results in highly resistive GaN buffer layers. This process simplifies the growth by eliminating large temperature ramps, while producing device-quality GaN-based films with low background carrier concentrations ($\leq 1 \times 10^{13} \text{ cm}^{-3}$). The introduction of aluminum in the high temperature nucleation layer, aids in the uniform wetting of the substrates as opposed to three-dimensional growth observed at

high temperatures with only GaN or using the low temperature nucleation schemes.

Over 300 epitaxial runs were done on sapphire and SiC substrates as listed in Appendix B for the custom nitride system described in Chapter 1. This chapter discusses sapphire and SiC substrate issues, nucleation strategies, metallic preparation of the substrate surface, AlGaIn nucleation and GaIn growth optimization. Uniformity issues related to the nucleation and GaIn buffer layers are also discussed which are specific to the nitride reactor used for this work. The AlGaIn barrier and optimization of the complete HEMT structure and device test results are given in Chapter 6.

5.2 Substrate Issues

Undoped AlGaIn/GaIn heterostructures were grown on either *c*-plane sapphire or SiC (both 4H semi-insulating and 6H n-type) substrates at 76 Torr [9]. Substrates were degreased in acetone and methanol, with the SiC additionally cleaned by the RCA method. The RCA wafer preparation involved etching the substrates in a 5:1:1 mixture of $\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{HCl}$ at 35° C for 5 minutes, then an etch in 5:1:1 mixture of $\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{NH}_3\text{OH}$ at 55° C for 5 minutes, followed by a buffered HF (10 %) for 5 minutes and rinsed in DI H_2O . All substrates are then subjected to 1100° C clean for 10 minutes under H_2 just prior to growth. Deposition temperatures were fixed at 1040° C for sapphire and 1010° C for SiC for the majority of the growths.

Several difficulties were encountered with both sapphire and SiC substrates. On sapphire, surface polish quality is the dominating factor for successfully nucleating the surface and producing planar films. SiC posed more challenges than sapphire in the fact that the crystals were of lesser

quality causing surface finish problems along with nano-, micro-, and macro-defects that propagate through the substrates and epitaxial layers and degrade the low field electron mobility of the 2DEG.

5.2.1 Sapphire Substrates

Surface finish on sapphire substrates plays a large role in the nucleation process. The surface defects (point, screw, edge, and macroscopic scratches) provide centers for preferential nucleation, consuming the Al in the wetting layer. This is evident as seen in Figure 5.1 where the nucleation sites are concentrated along scratches present on the surface from final polishing procedures. The optical image to the left is focused through the epitaxial film to the substrate/epitaxy interface. Scratches are clearly observed and highlighted. The image to the right is the top surface of the HEMT structure showing features aligned along the scratches. Preferential nucleation along scratches establishes a non-uniform thickness profile that propagates throughout the epitaxial structure. These variations in thickness measured around 1000 Å do not appear to effect the transport properties of the 2DEG at the top heterostructure, but create problems with sub-micron device fabrication processes. Incomplete nucleation from excessive surface damage consumes too much Al and can cause voids in the crystal.

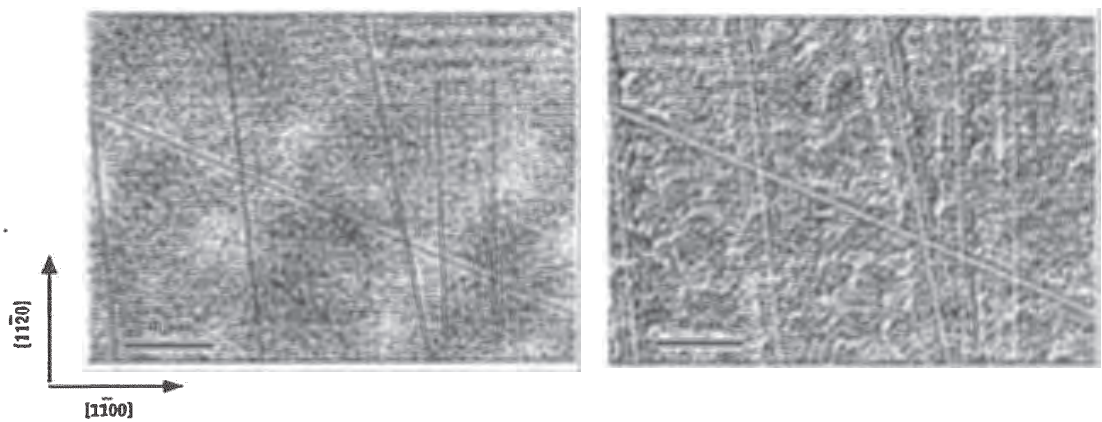


Figure 5.1. Nomarski images of surface scratches present on the sapphire surfaces (left image). One micron of GaN is then imaged on the right, showing the preferential growth along the scratches and is highlighted by the white lines.

5.2.2 SiC Substrates

The quality of semi-insulating SiC seed crystals for fabrication of substrates is poor, leading to inclusions and defects that can range from nanopipes to macro defects. With the high temperature nucleation schemes developed for this work, the substrate defects are not “healed” and trend to propagate throughout the entire thickness of the epitaxial layers. Figure 5.2 show typical defects present on 4H SI-SiC substrates. Cracks are observed in the image on the top left, and rippled surfaces are shown in the top right image. The bottom image and plot show macropipes and the large cross-sectional area and depth of these defects from surface profilometry. The macropipe defects are in the $200 - 400 \text{ cm}^{-2}$ densities across the substrate. These defects act as scattering centers in the 2DEG and significantly reduce the measured electron transport properties. Depending on the density of defects, room temperature mobilities can be reduced from 1500 to $800 \text{ cm}^2\text{volt}^{-1}\text{sec}^{-1}$ with 2 and 40 defects present, respectively. Figure 5.3 show Nomarski images of these defects (within the circles) on two Hall samples made from HEMT structures on SiC. The sample on the left has 2 defects with a measured mobility of $1505 \text{ cm}^2\text{volt}^{-1}\text{sec}^{-1}$, while the one on the right has 40 defects and a mobility of only $850 \text{ cm}^2\text{volt}^{-1}\text{sec}^{-1}$. These defects were not seen on production grade SiC, or 6H-n+ SiC substrates.

A batch of 1-3/8” SI-SiC substrates differed from previous SI-SiC leading to problems with the nucleation (a problem similar to what was seen in the past with different boules of sapphire). Growth on the new substrates, with previously optimized conditions, resulted in planar surfaces but had

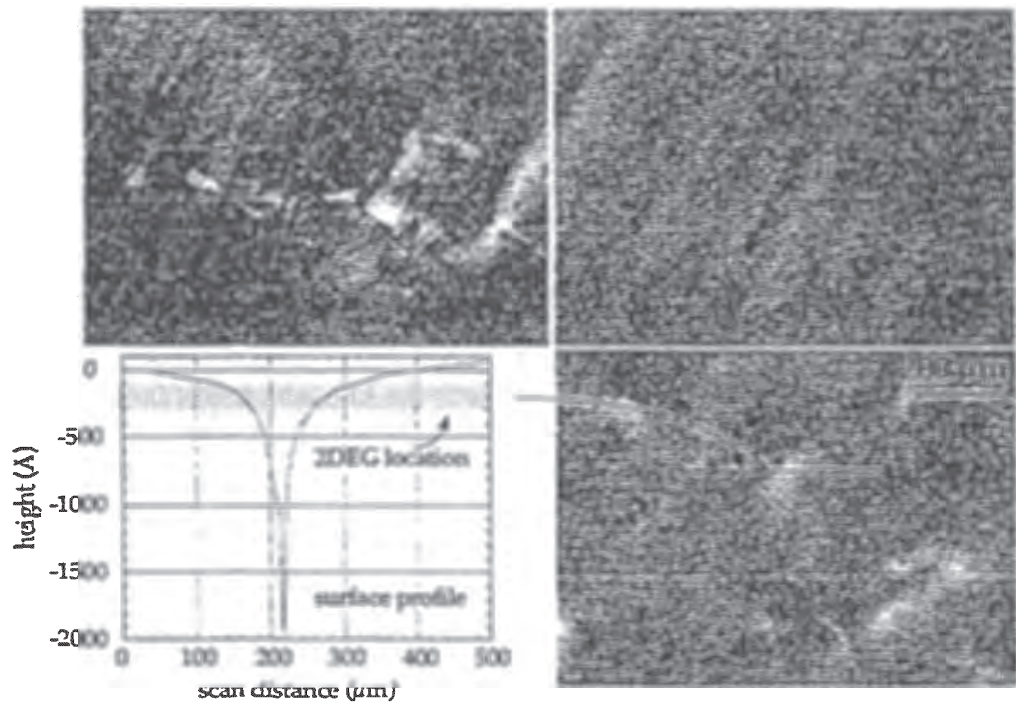


Figure 5.2. Surface features present on SiC substrates. The top left shows defects and cracks, the top right shows a region with a rippled surface. The bottom images show pit defects with the associated surface scan, indicating that the pits have a large cross section and are several thousand Angstroms deep.

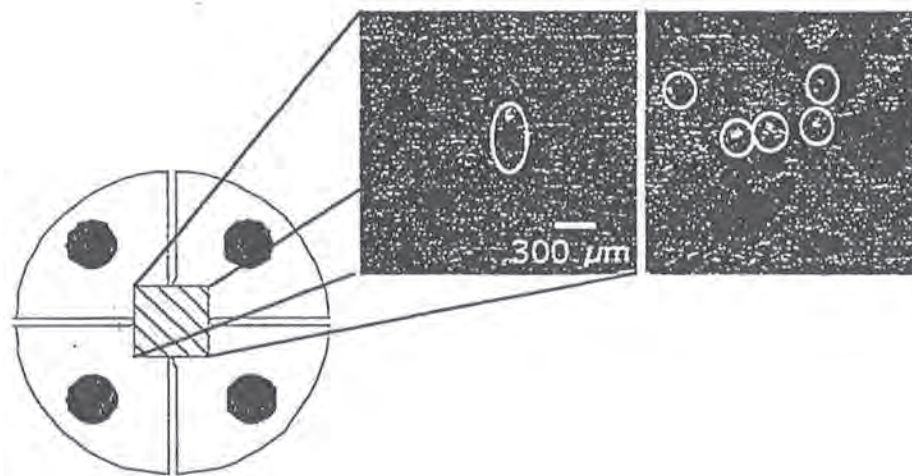


Figure 5.3. Hall sample with varying macro-defect density. The left has 2 defects yielding $1505 \text{ cm}^2\text{volt}^{-1}\text{sec}^{-1}$, while the one on the right has over 40 defects with a mobility of only $850 \text{ cm}^2\text{volt}^{-1}\text{sec}^{-1}$.

voids that extended down to the substrate as shown in Figure 5.4 (a) and (b). Control pieces included with the growth experiments showed that the “older” SI-SiC and n+ SiC resulted in successful nucleation with no voids, and no buffer charge. Therefore, the nucleation process had to be re-optimized on the new substrates.

The type of voids shown in Figure 5.4 (b) indicate insufficient Al-content in the nucleation layer, causing the point of film coalescence to be in the GaN buffer instead of the AlGaN. By increasing aluminum mole fraction, we get complete coverage of the substrate by the nucleation layer, thereby eliminating the voids as is evident in Figure 5.4 (c). The structure in Figure 5.4 (c) yielded highly resistive 1 μm thick GaN buffer layers suitable for transistor structures.

Experimentation mainly focused on optimization of the nucleation layer on various SI-SiC substrates obtained for this work. It quickly became evident that the nucleation layer needed to be re-optimized not only on substrates from different vendors (Cree, Northrop Grumman and Sterling) but also on different boules and/or surface polishing runs from the same vendor. Figure 5.5 shows surface morphology images of the transistor on various SI-SiC substrates from one growth run. Image 5.5 (1a) is from a 2-inch substrate while 5.5 (1b) is from a 1-3/8 inch substrate from the same vendor. Voids are clearly seen on (1b), aligned along straight lines corresponding to surface scratches on the substrate. From past experience, the substrate in 5.5 (2b) was “over nucleated”, suggesting that the Al content was too high in the nucleation layer. Either increasing the Al content or increasing the thickness of the nucleation layer can eliminate voids.

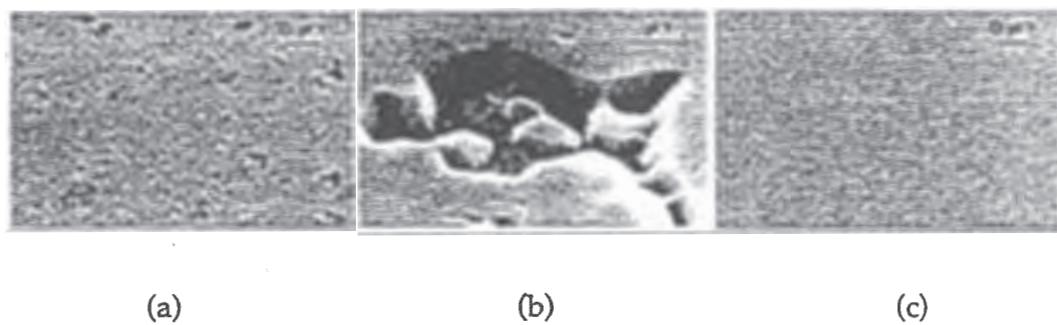


Figure 5.4. Surface micrographs of AlGaIn/GaN HEMTs grown on semi-insulation 4H-SiC. Voids are observed in the Nomarski image shown in (a) and the SEM image (b) when the Al mole fraction in the nucleation layer is below the minimum required. Increasing the Al content in the nucleation layer eliminates the voids as seen in (c)

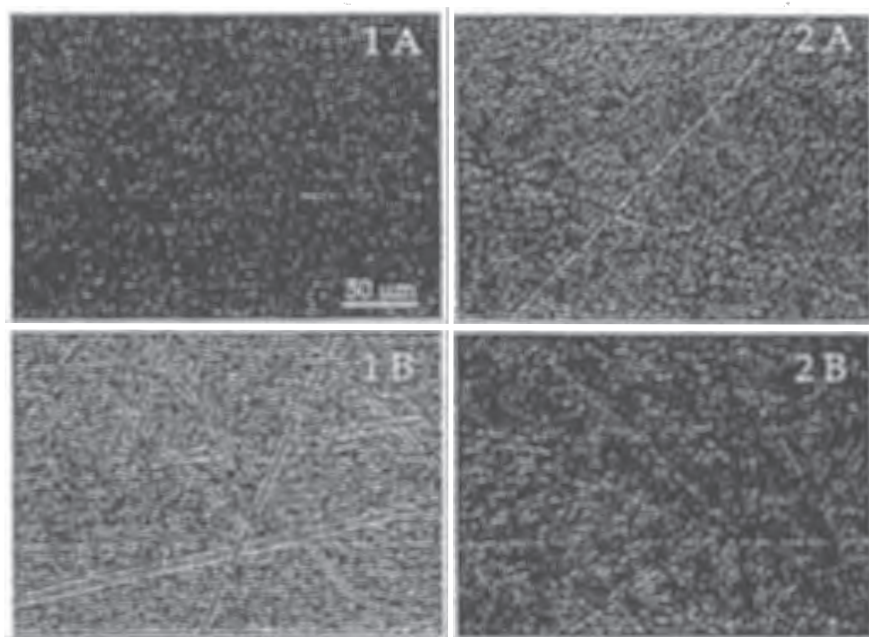


Figure 5.5. Nomarski surface images of transistor structure deposited on various Semi-Insulating SiC substrates. These 4 substrates were all in the same epitaxial growth run. The images on the right (2A&B) are structures deposited on 1-3/8 inch SI SiC from a second vendor. The top right micrograph shows voids similar to those in 1B, which can be eliminated as discussed above. In 2B, circular features are seen on the entire surface with some indications that they follow scratches on the substrate

However, both these corrective measures can lead to other problems within the device structure, such as introducing free carriers in the GaN buffer or creating shunt RF conduction paths in the nucleation layer. Therefore, a narrow process window must be defined for each substrate “group” in which the Al content and thickness of the nucleation layer are minimized while still producing device quality epitaxy. Efforts need to be directed to make the nucleation technology less sensitive to the surface preparation of these substrates. Similar problems were encountered with sapphire substrates, in which we had to re-optimized nucleation growth conditions (2-3 epitaxy runs) on each batch received. To date, there is no “epi-ready” specification for surfaces on SiC or sapphire substrates that is required for reproducibility.

5.3 Nucleation Strategies

The lack of suitable substrates for GaN based materials growth lead to the development of nitride based buffer layers on latticed mismatched substrates. Starting substrates explored included GaAs, silicon, sapphire, and SiC, with sapphire presently being the most widely used. SiC substrates are used for the higher power density applications over sapphire due to the superior thermal conductance. Heteroepitaxial growth of GaN and related alloys on severely mismatched substrates require thin layers to provide nucleation sites to initiate crystal growth. When optimized, these nucleation layers accommodate the strain between the substrate and epitaxial layers caused by lattice and thermal mismatches, while still maintaining crystallographic registration of the epitaxial films to the substrate lattice structure.

5.3.1 Two Temperature Nucleation

Accepted techniques for producing GaN buffers on sapphire using conventional OMVPE involve three growth segments. First, the sapphire (Al_2O_3) surface is converted to AlN by exposure to nitrogen (nitridation), usually supplied as NH_3 . Next, a thin ($<1000 \text{ \AA}$) low temperature ($500^\circ \text{C} - 600^\circ \text{C}$) GaN nucleation layer is grown followed by a high temperature ($> 1000^\circ \text{C}$) recrystallization and subsequent GaN growth as shown to the right in Figure 5.6. The high temperature film is one of the critical steps, as conditions must be found which initially creates large isolated islands, which eventually coalesce into a planar surface. In this work, the substrate temperature was increased to 1040°C in order to enhance the lateral growth rate to achieve planarization. Structural and electrical properties of the top GaN layer were evaluated to optimize the nitridation and nucleation steps. Initially, a series of runs were performed with nucleation temperature varied from 530°C to 670°C . The low temperature GaN layer was targeted for $500 \text{ \AA}$, while the GaN top layer was held constant at $1 \text{ }\mu\text{m}$ with a growth temperature of 1040°C . Nitridation of the sapphire surface was initially done at 550°C with ammonia exposure of 30 seconds. A nucleation temperature of 600°C provides the narrowest X-ray FWHM (00_2 reflection) from the top GaN layer as shown in Figure 5.7. To further improve the structural quality the nitridation temperature was increased to 1030°C , aiding the surface conversion to AlN. A greater than 25 % reduction in the symmetric X-ray FWHM was observed (square data point in Figure 5.7).

After defining the optimal nucleation growth temperature, the thickness of this layer was varied to determine its effects on coalescence and

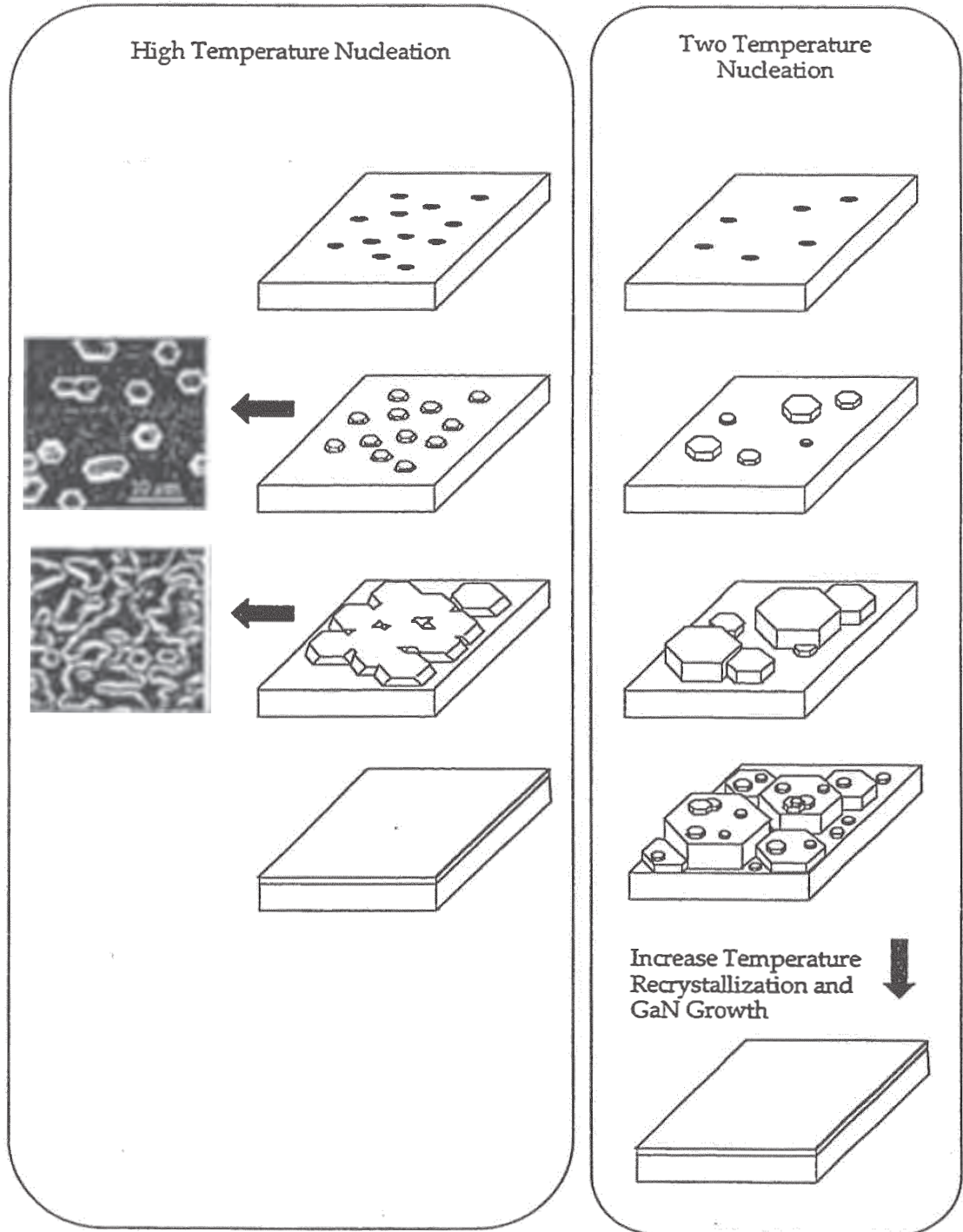


Figure 5.6 Nucleation/Growth model for single high temperature nucleation (to the left) and the conventional two-temperature scheme shown to the right.

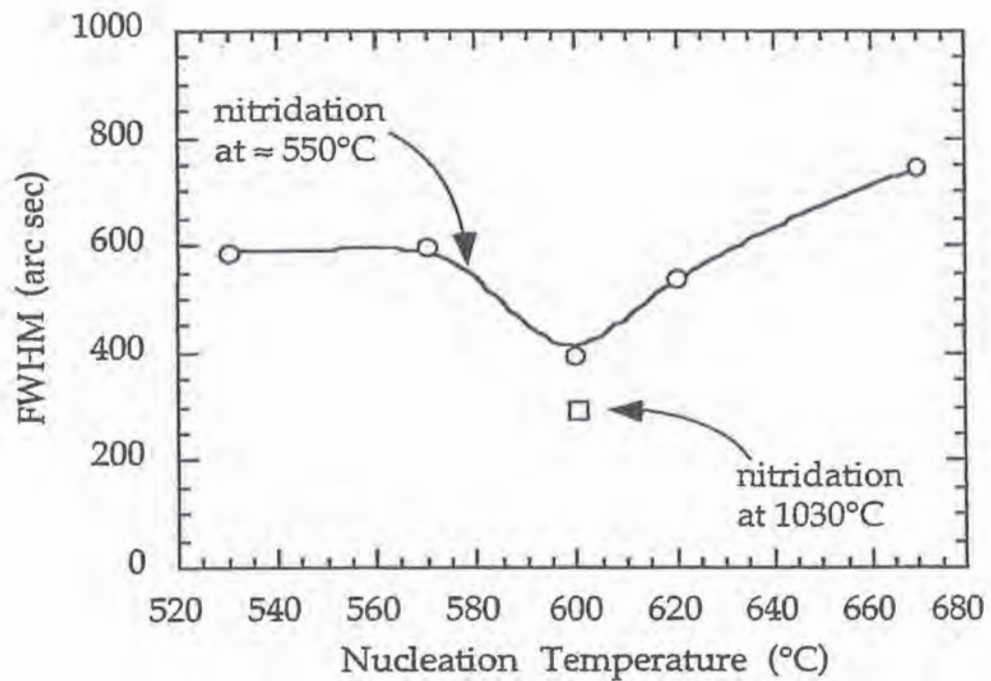


Figure 5.7. Results from symmetric (00_2) X-ray analysis showing a minimum in the FWHM at 600° C growth temperature. The nitridation temperature of the sapphire surface was then increased from 600° C to 1030° C resulting in a 25 % reduction in the FWHM.

electron mobilities of the top 1 μm thick GaN layer. A series of runs with nucleation layers thicknesses varied from 65 $\text{\AA}$ to 500 $\text{\AA}$ resulted in the highest "bulk" electron mobility of $58 \text{ cm}^2\text{volt}^{-1}\text{sec}^{-1}$ with a 125 $\text{\AA}$ thick nucleation layer. These samples exhibited unintentional electron carrier concentrations of approximately $1 \times 10^{20} \text{ cm}^{-3}$ and pyramid-like growth surfaces. Hexagon pyramids present on the growth surface indicate too low a ratio between the lateral and vertical growth rates.

To enhance the lateral growth rate within the GaN overlayer, the growth temperature was increased from 1030 $^{\circ}\text{C}$ to 1100 $^{\circ}\text{C}$. Surface morphologies of the higher nucleation temperature improved dramatically but pyramid-like structures with flat tops were still visible on thin GaN layers. However, very smooth surfaces were observed between the flat pyramid structures indicating that higher substrate temperature is desirable. Increasing the growth temperature of both the nucleation and GaN overlayer decreased the growth rate from 1 $\mu\text{m/hr}$ to 0.25 $\mu\text{m/hr}$ due to the increase in Ga-desorption (transition from mass transport limited growth to desorption limited growth as discussed in Chapter 1, Section 1.2). Layers with nominal thicknesses of 0.25 μm yielded room temperature electron mobilities of $130 \text{ cm}^2\text{volt}^{-1}\text{sec}^{-1}$ with background carrier concentration in the low 10^{18} cm^{-3} . This study indicated that higher nucleation temperature using FME produces higher quality GaN films. The next step was to introduce AlGaIn in the higher temperature nucleation layer to aid in the "wetting" of the substrate surface to increase the density of nucleation sites and coalesce the growth front earlier to reduce the cross-sectional area of any defective regions.

5.3.2 High Temperature Reactor Bake

Before detailing the high temperature nucleation schemes discovered, it is important to discuss contamination issues related to the OMVPE reactor. Previous runs will coat up the susceptor, lift tube, and outer quartz walls, which will contaminate the substrate (either sapphire or SiC) during the heat-up and hydrogen clean cycles. Nucleation on these contaminated surfaces result in three dimensional, pyramid growth not suitable for electronic applications. Figure 5.8 gives a Nomarski image of a 1 μm thick GaN film grown without a bake between two growth runs. A smooth planar film is observed under the identical growth conditions with the addition of the cell bake. Reactor cell baking procedures involve heating the reaction cell up to 1150 $^{\circ}\text{C}$ for 1 hour between epitaxial runs.

5.3.3 High Temperature AlGa_N Nucleation

An alternative single step process technique for the nucleation and subsequent epitaxial growth of GaN-based materials on mismatched substrates was developed. A single flow, single pressure, high temperature nucleation process is achieved by introduction of the group III reactants only (OM-Preflow) into the growth chamber at growth temperature of 1040 $^{\circ}\text{C}$ to wet the substrate surface prior to any actual crystal growth. It is necessary to introduce both the Gallium and Aluminum species at this step. The Aluminum reacts with the surface providing the needed nucleation sites while the Gallium prepares the Aluminum saturated surface for subsequent AlGa_N or GaN growth. In the case of a thin Al_(x)Ga_(1-x) nucleation layer where the Aluminum mole fraction is varied from 0.03 to 0.97 depending on the substrate material used. Generally, the Aluminum content requirements



Figure 5.8. Nomarski image of 1 μm thick GaN film with reactor not bake prior to epitaxial run. Pyramid (hexagonal) growth is observed from contaminated and non-uniform nucleation layers.

increase from SiC to sapphire for obtaining atomically flat two-dimensional epitaxial growth. The exposure time and flux of the group III precursors depend again on the substrate material and the crystal qualities desired, but typically varied from 30 seconds to 4 minutes. Once the group III soak of the surface is completed, the Nitrogen source (ammonia) is introduced to the growth chamber. The second nucleation layer is crystalline $\text{Al}_x\text{Ga}_{1-x}\text{N}$ of a specific thickness and Aluminum content. The Aluminum is then graded out and GaN buffer can then be grown.

A schematic representation of the nucleation process is shown in Figure 5.9. Relative reactant fluxes and exposure cycles are depicted for the Group III soak, the AlGaN nucleation film, and the transition to GaN growth on both sapphire and SiC substrates. A detailed description of the process depicted in Figure 5.9 follows:

- 1) *The substrates are heated up to 1100° C in Hydrogen for 10 minutes to clean the surface.*
- 2) *After 10 minutes, the temperature is decreased to the growth temperature of 1040° C.*
- 3) *After the temperature has stabilized, the group III reactants (namely TEG and TMA) are introduced into the growth chamber. For sapphire substrates the TMA/TEG ratio is set at 0.15, while for SiC, it is fixed at 0.06. The substrates are exposed for 100 seconds.*
- 4) *The ammonia is then switched into the cell, forming $\text{Al}_x\text{Ga}_{1-x}\text{N}$ ($x=0.06$ for SiC, and 0.15 for sapphire) on the metal rich substrate surface. Around 20 nm of AlGaN is grown.*
- 5) *The Aluminum is then ramped down to 0.0 in 30 seconds, and then switched out of the cell.*

- 6) *This results in GaN deposition, providing a buffer layer on which other GaN-based materials can subsequently be deposited without any change in chamber temperature.*

The AlGa_xN nucleation layer was extensively investigated to yield smooth growth fronts with bi-layer atomic stepped surfaces. Both the composition and thickness of the Al_xGa_{1-x}N nucleation layer were separately optimized. It was discovered that a minimum aluminum content in the nucleation layer is required to create sufficient nucleation sites on the substrates to wet the entire surface, resulting in planar growth within several hundred Angstroms as illustrated in Figure 5.6 (left side). Figure 5.10 gives a typical AFM image of a 1 μ m thick GaN buffer layer on SiC, showing atomic steps with an rms surface roughness of ≤ 0.30 nm (top image). GaN on sapphire gives similar images with an rms roughness of about 0.35 nm. Threading dislocation densities estimated from these AFM images are in the mid 10^8 cm⁻² and low 10^9 cm⁻² for growth on SiC and sapphire, respectively. Higher Al contents (up to 35 %) in the nucleation layer yielded optically smooth GaN buffers on both substrates but produced slightly poorer surface morphologies. In all cases, epitaxial growth on SiC substrates produced smoother surfaces than on sapphire.

For growth on SiC, aluminum mole fractions greater than 6% in the nucleation layer resulted in cracking of the GaN overlayer. The tensile stress of mismatched GaN grown on SiC substrates places a thickness limitation on the buffer layer. Using an Al_{0.06}Ga_{0.94}N nucleation layer, GaN buffer layers exceeding 5 μ m were successfully grown on SiC without cracks forming. A

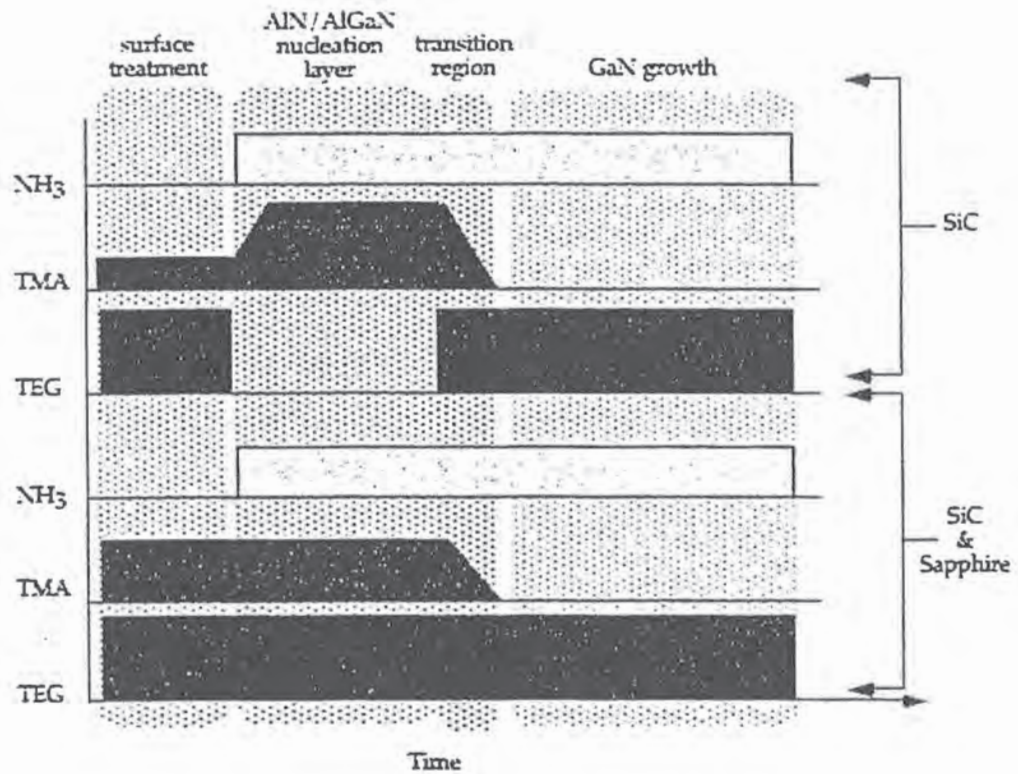


Figure 5.9 Schematic representation of reactant fluxes and exposure cycles for example nucleation technology on both sapphire and SiC substrates. Flux amplitudes are relative and not to scale.

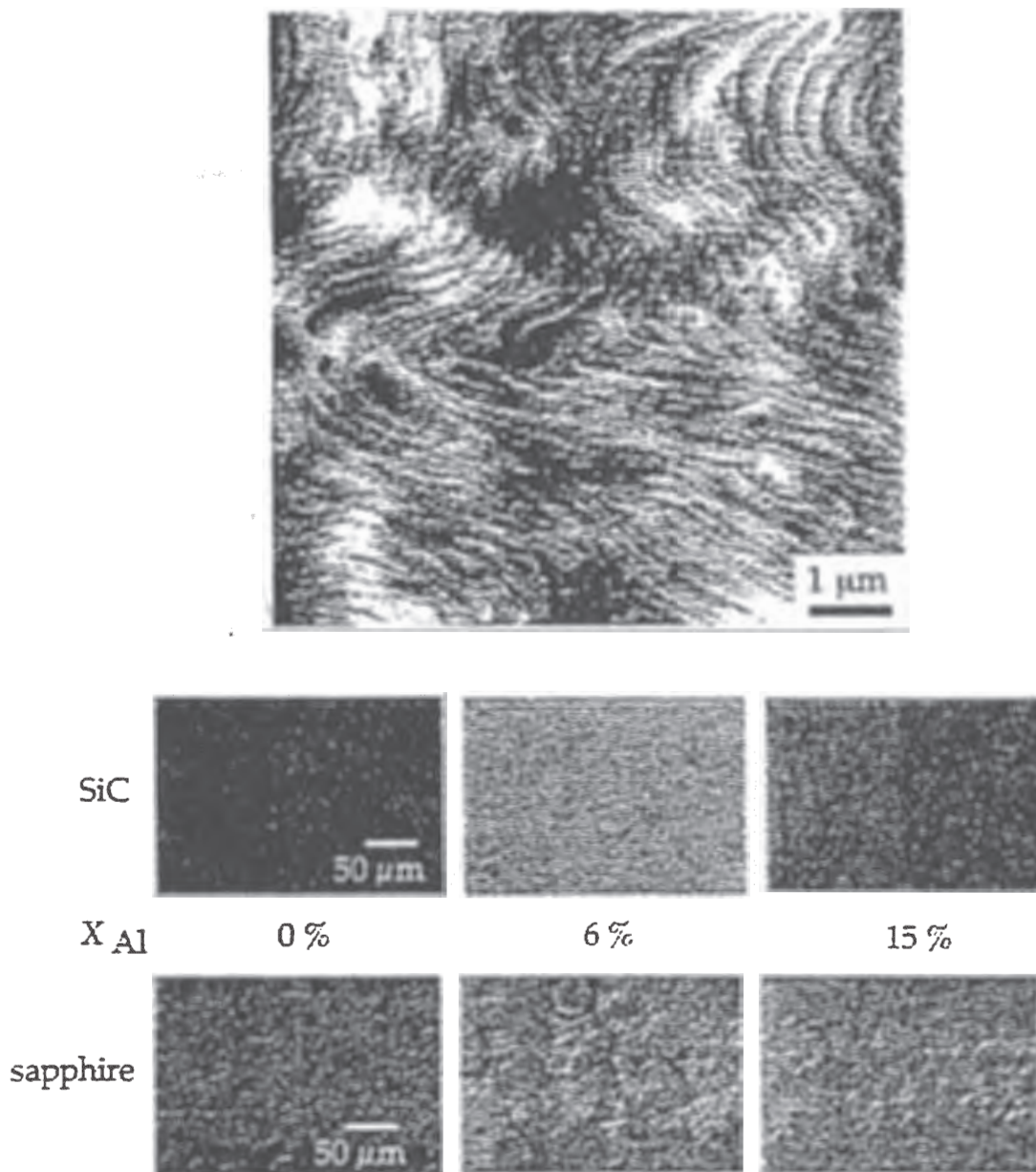


Figure 5.10 Top AFM image is a plan view of a 1 μm GaN buffer layer grown on SiC. The AlGaIn nucleation layer had approximately 6 % Al and was 1800 $\text{\AA}$ thick. The threading dislocation density is determined by counting dark circular features on the surface at step edge terminations. The bottom set of micrographs is a surface comparison of Al percentage in the AlGaIn nucleation layer and resulting surface morphologies for 1 μm GaN overlayer. Minimal of 6% and 15% Al required for SiC and sapphire respectively.

summary of surface morphology and Al content in the nucleation layer is given in the bottom set of micrographs in Figure 5.10 for growth on SiC and sapphire substrates.

Room temperature PL measurements of 1 μm thick GaN buffers deposited with and without optimized Al content in the nucleation layers are shown in Figure 5.11. Spectra of structures with optimized nucleation layers (dashed lines) are dominated by near-band-edge-related luminescence at 364.4 nm (FWHM = 32.7 meV) for SiC and 361.8 nm (FWHM = 55.5 meV) for sapphire. The insets show spectra of optimized $\text{Al}_x\text{Ga}_{1-x}\text{N}$ nucleation layers (1800 Å thick) giving Al-content of approximately 6 % on SiC and 15 % on sapphire. Al mole fraction is determined by Vegard's law using a bowing parameter of 0.8 eV assuming that the AlGa_xN nucleation layer is relaxed. GaN layers on top of nucleation layers, with Al compositions below the minimum required, show higher defect related yellow-band (Y-B) luminescence as seen in Figure 5.11 (solid lines). Increased Y-B emission is attributed to three-dimensional GaN growth, resulting from a non-planar nucleation layer. The extended point of coalescence does not influence the final surface morphology or mobility of the 2DEG, but results in a buried charge layer deep in the buffer. Carrier concentration profiles derived from C-V measurements are shown in Figure 5.12(a) for two HEMT structures grown on sapphire. The dashed line depicts the profile on a structure with the optimal 15 % Al in the nucleation layer, while buffer charge can easily be seen on the other structure that has only about 8% Al. With the 8% Al, the sapphire surface does not uniformly wet at the high growth temperatures (1040° C)

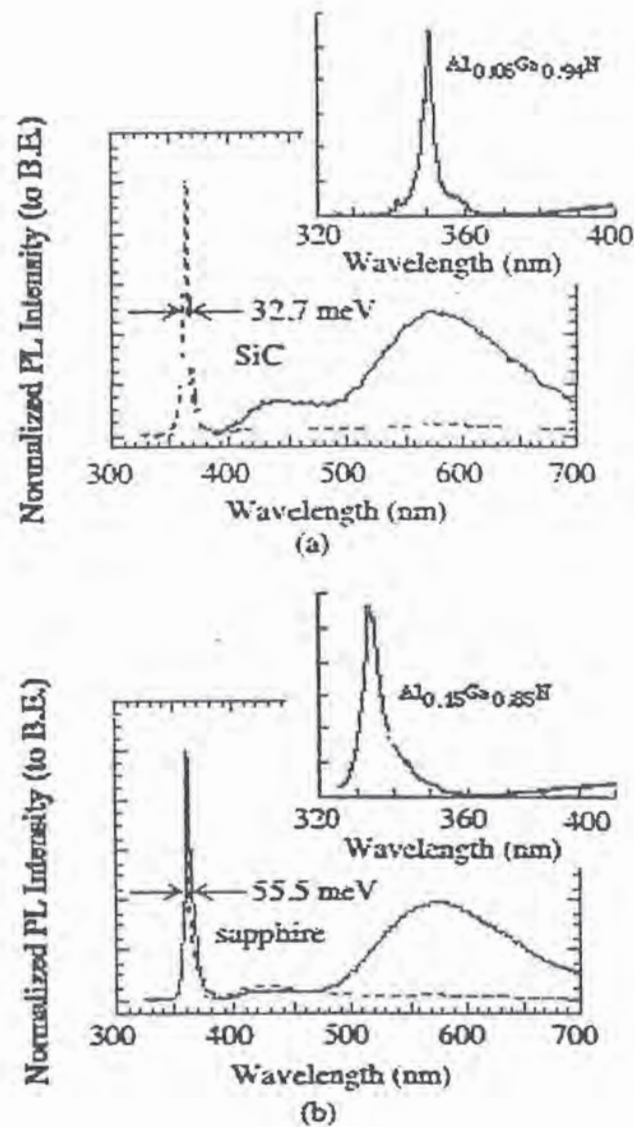


Figure 5.11. Room temperature PL measurements of 1 μm thick GaN epitaxial films with 1800 $\text{\AA}$ nucleation layers on (a) SiC and (b) sapphire substrates. Solid lines represent growth on nucleation layers below the required Al-content. The insets are spectra of the AlGaIn nucleation layer with the minimum alloy composition needed for growth of smooth epitaxial GaN buffers.

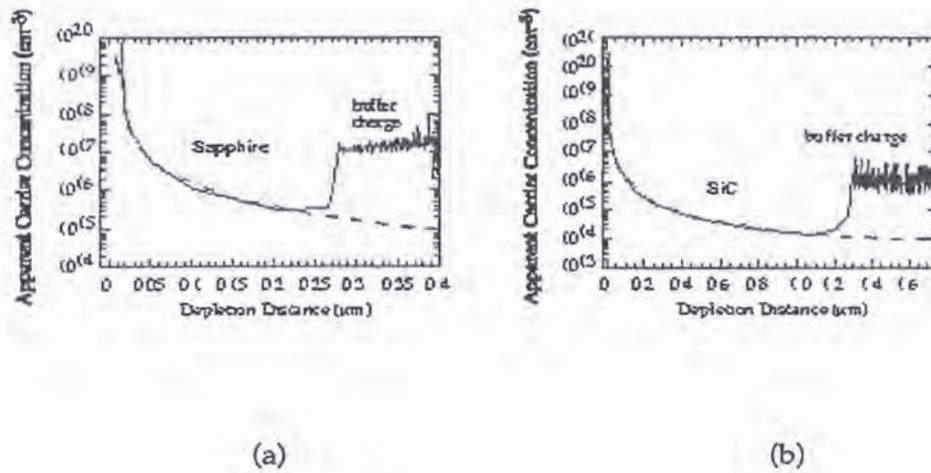


Figure 5.12. Derived carrier concentration profile from C-V measurements on a HEMT structures grown on (a) sapphire with different aluminum percentages in the AlGa_N nucleation layer, and (b) semi-insulation SiC with different AlGa_N thicknesses. Measurements are made at 10KHz with a Hg-probe.

leading to incomplete coalescence (ie. voids forming in the epitaxial layer). This produces defects with piezoelectrical induced charges resulting in a high n-type carrier background concentration. Similar behavior is seen on SiC substrates with Al composition less than the needed 6% as observed in Figure 5.12(b). From the charge distribution profile, the buried charge region in the GaN buffer extends about 0.5 μm from the substrate/epitaxy interface.

5.4 Uniformity and Flow Dynamics

Like most OMVPE-based approaches for growth of GaN, the process utilizes a large ammonia flux in a hydrogen or nitrogen carrier gas. The ammonia flux is so large that the carrier gas is essentially a 10 % mixture of ammonia, which degrades the fluid properties. For the process used in this work, a high deposition temperature is required. There is a concern that convection currents in the carrier gas will disrupt the laminar flow and degrade the reactor performance. By operation at low pressure (76 Torr), flow is observed to be laminar, convection free, with an unconstrained boundary layer.

The growth rate uniformity related to transport flow observed is characteristic of laminar flow, with a mass transport limited model, through an unconstrained boundary layer. Reaction efficiency increases with hydrogen flow (gas velocity). A series of runs were performed at a nominal growth rate of 1 $\mu\text{m/hr}$ at 1040° C. The hydrogen carrier gas was increased from 24 SLM, to 32 SLM, then finally 48 SLM with all other flows remaining fixed. The growth rate on the up stream edge was observed to increase

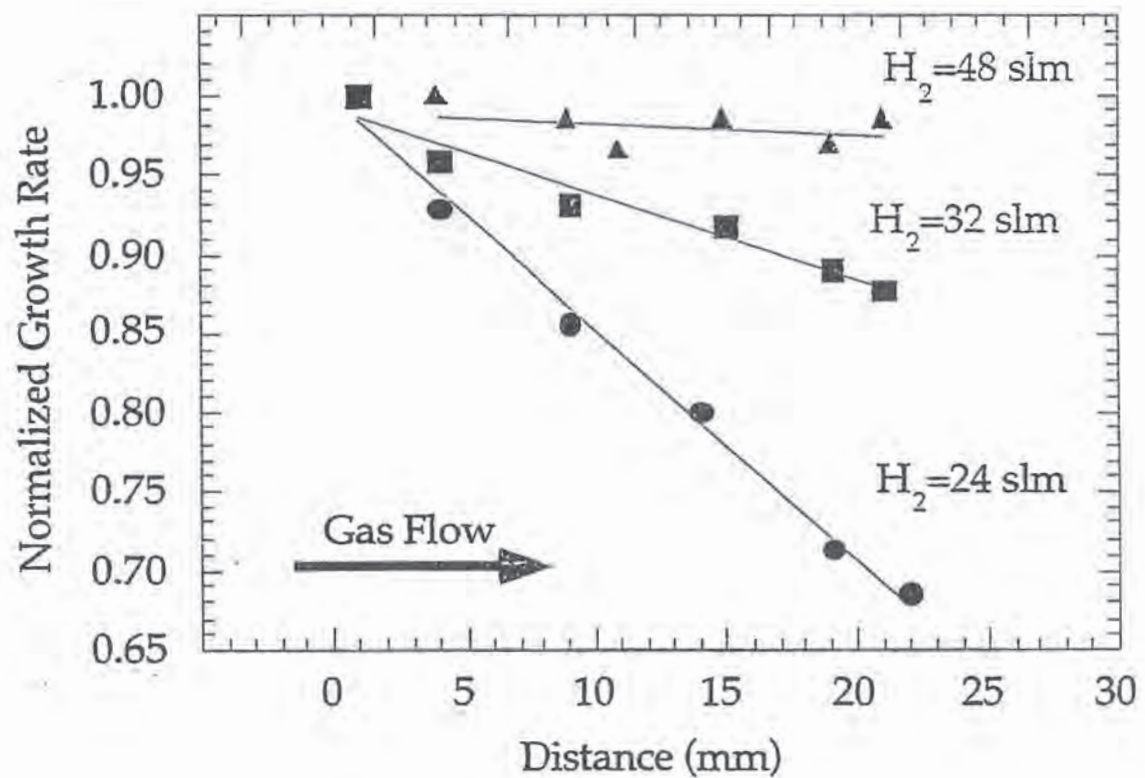


Figure 5.13. Normalized GaN growth rate versus distance across the wafers along the gas flow direction at different hydrogen transport flows. As the transport flow increases, affects of gas phase depletion are minimized.

linearly with the square root of gas velocity, indicating laminar flow and mass transport limited growth by diffusion through the boundary layer. Accordingly, increasing the total gas flow compensates for the gas phase depletion and improves the deposition uniformity. The thickness uniformity improved to less than $\pm 5.5\%$ at the larger transport gas flows as observed in Figure 5.13.

A thickness contour plot across a 2-inch wafer with the highest flow is shown in Figure 5.14 (thicknesses are in nanometers). The center 85 % of the wafer is very uniform providing sufficient area for circuit fabrication. The thicker regions at the upper corners are mainly caused by temperature variations, with the center-top being slightly hotter than the top corners. This is inherent in the present 8-wafer susceptor that has thicker cross-sectional areas between consecutive wafer pockets, resulting in a slight temperature gradient. The trend towards lower growth rates at the bottom of the wafer can be attributed to gas phase depletion.

Transport properties of the 2DEG at the AlGa_N/Ga_N interface were calculated from Hall effect measurements on one wafer from each 8-wafer lot. The location of the Hall samples and a summary of the room temperature mobilities and 2DEG sheet concentrations are given in Figure 5.15. Growth with the highest transport flow (48 LPM) consistently resulted in mobilities greater than $1200 \text{ cm}^2\text{volt}^{-1}\text{sec}^{-1}$ with corresponding 2DEG densities around $1 \times 10^{13} \text{ cm}^{-2}$. Channel sheet resistances are low and range from 460 to 583 Ω/square .

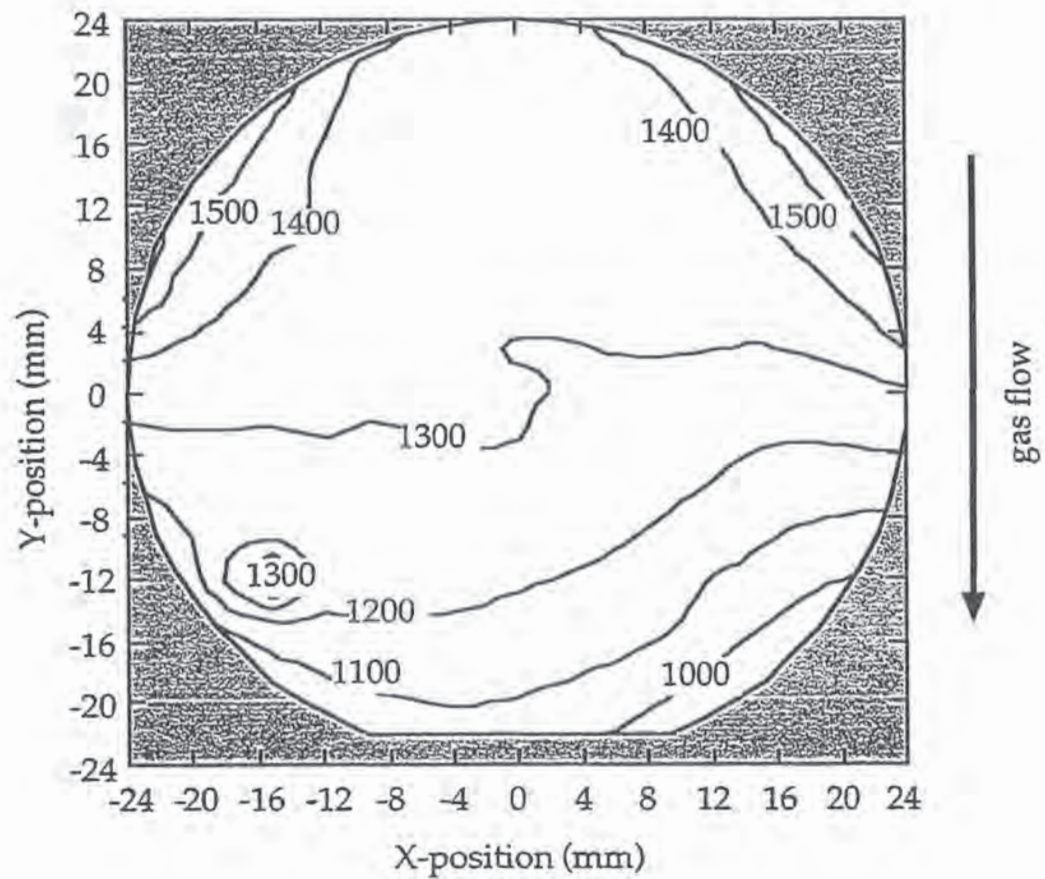


Figure 5.14. GaN layer thickness uniformity over an entire 2 inch wafer (sapphire substrate) grown with 48 LPM transport carrier flow. Thickness numbers are in nanometers.

5.5 GaN Buffers

Upon optimization of the AlGaIn nucleation layer and reactor flows for uniformity, issues pertaining to the GaN buffer layer were addressed. The thickness, threading dislocation densities and layer resistivity were investigated. To obtain highly resistive buffer layers, the material has to be either very pure or free carriers present need to be compensated. Since there is no low defect GaN substrate currently available, defects will be unavoidable for growth on foreign substrates. Therefore, compensation is the only viable method for producing highly resistive films in the GaN material system at this time.

5.5.1 GaN Buffer Layer Thickness

To improve the structural and electrical properties at the AlGaIn/GaN heterostructure, the thickness of the GaN buffer layer was increased. The increase in GaN buffer layer thickness further removes the 2DEG from the defective nucleation layer and substrate/epitaxy interface. The growth fronts smooth, decreasing the heterointerface roughness and improving the electron mobility. Figure 5.16 shows the improvement in surface morphology between structures with a 1 μm up to a 4 μm GaN buffer. The 1 μm buffer results in planar growth with circular features uniformly distributed over the surface. By increasing the buffer thickness, these surface features merge together resulting in smoother GaN growth as seen in Figure 5.16.

Room temperature 2DEG mobilities increased from $1,225 \text{ cm}^2\text{volt}^{-1}\text{sec}^{-1}$ (1 μm) to $1,700 \text{ cm}^2\text{volt}^{-1}\text{sec}^{-1}$ (4 μm) on samples with nominally $1 \times 10^{13} \text{ cm}^{-2}$ 2DEG density, indicating a significant improvement in interface roughness at the AlGaIn/GaN heterostructure. As the GaN buffer is increased above 2 μm ,

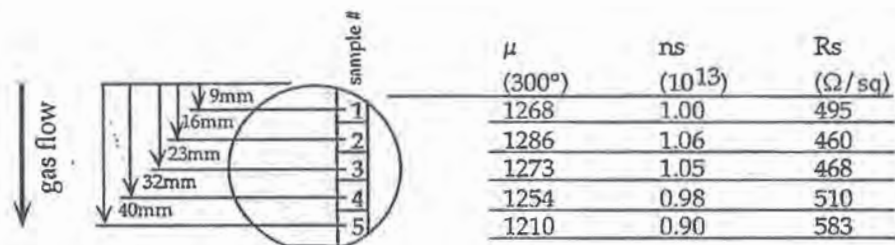


Figure 5.15. Typical room temperature Hall data on an undoped HEMT structures across a 2" sapphire substrate. This is one of eight wafers grown in this run.

a transition occurs to smoother GaN growth fronts as shown in the Nomarski images in Figure 5.16. Thicker GaN buffer layers were not attempted due to the growth rate limitation of the system using TEG (roughly $0.5 \mu\text{m/hr}$).

5.5.2 Threading Dislocation Densities

The electron mobility in n-type GaN has been shown [10] to be strongly dependent on the density of threading dislocations, which charge up and deplete nearby carriers. In the case of $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ structures, especially in the unintentionally doped devices, the mobility of the electrons in the 2DEG can be estimated analytically, assuming scattering from dislocations dominates along with the scattering by longitudinal polar optical phonons. In such a two-dimensional system, the scattering from the charged threading dislocations (and any ions) depends linearly on the average energy of the electrons being scattered. The Fermi energy in this 2DEG in GaN rises nearly linearly with the electron sheet density. Thus the electron scattering rate due only to charged dislocations is linearly dependent on the dislocation density, and reciprocally dependent on the 2DEG sheet density.

The scattering due to longitudinal polar optical phonons and piezoelectric effects predicts room-temperature mobility of around $2000 \text{ cm}^2\text{volt}^{-1}\text{sec}^{-1}$ for electrons confined near the AlGa_N/GaN interface [11]. A measured room temperature value of electron mobility of $802 \text{ cm}^2\text{volt}^{-1}\text{sec}^{-1}$ occurs for a dislocation density of $5 \times 10^9 \text{ cm}^{-2}$ and a 2DEG density of $1.0 \times 10^{13} \text{ cm}^{-2}$. An ideal mobility contribution from the charged dislocations is $1340 \text{ cm}^2\text{volt}^{-1}\text{sec}^{-1}$ for $5 \times 10^9 \text{ cm}^{-2}$ dislocations at a sheet charge density of $1.0 \times 10^{13} \text{ cm}^{-2}$. Thus the room temperature mobility of a 2DEG in this undoped

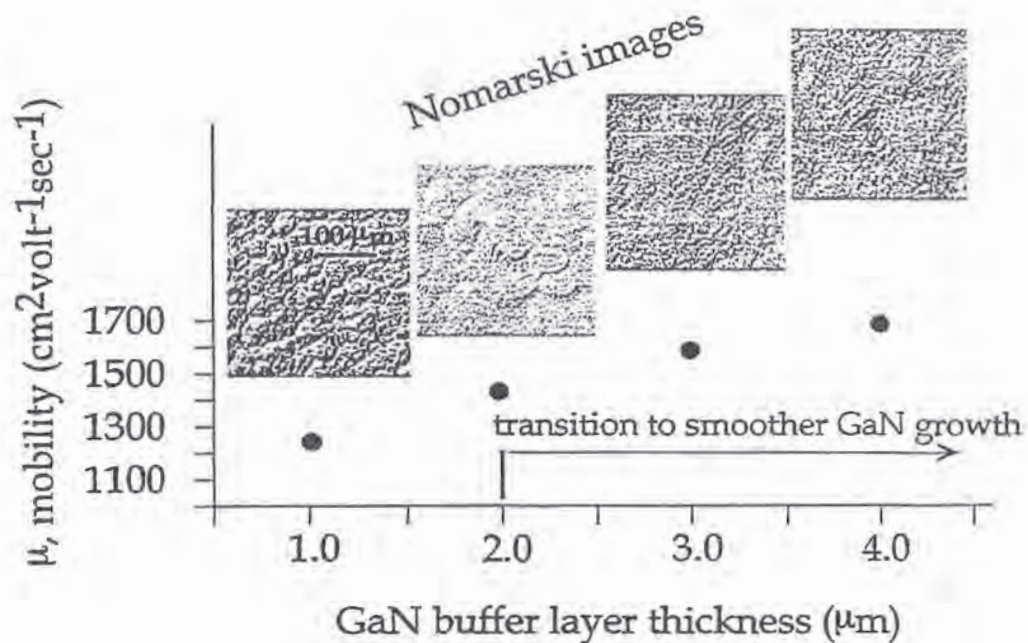


Figure 5.16. Nomarski micrographs of surface morphology of AlGaIn/GaN transistor structures grown on sapphire substrates. At 1 μm thick GaN buffer "puck-like" surfaces are observed compared to a 4 μm thick GaN buffer resulting in a smoother surface.

$\text{Al}_{0.30}\text{Ga}_{0.70}\text{GaN}/\text{GaN}$ HEMT can be plotted, as shown by the solid lines in Figure 5.17, from:

$$\frac{1}{\mu_{n2DEG}} \approx \frac{1}{2000} + \frac{1}{\mu_{dis}} \quad n_s > 5 \times 10^{12} \text{ cm}^{-2} \quad 5.1$$

and,

$$\mu_{dis} = 1339 \frac{\text{cm}^2}{V_s} \left(\frac{n_s}{1.0 \times 10^{13} \text{ cm}^{-2}} \right) \left(\frac{5 \times 10^9 \text{ cm}^{-2}}{N_{dis}} \right) \quad n_s > 3 \times 10^{12} \text{ cm}^{-2} \quad 5.2$$

where n_s is the 2DEG density and N_{dis} is the dislocation density as determined from AFM studies.

The range of dislocation defect densities observed in AFM is shown by the shaded region. Data from structures are shown with open squares (Si-face SiC), and open circles (sapphire) along with several reported results from other groups [12-19] (solid symbols). Room temperature mobilities as high as $1505 \text{ cm}^2\text{volt}^{-1}\text{sec}^{-1}$ with a 2DEG sheet carrier density of $1.4 \times 10^{13} \text{ cm}^{-2}$ were measured on SiC, and $1575 \text{ cm}^2\text{volt}^{-1}\text{sec}^{-1}$ with a sheet carrier density of $1.1 \times 10^{13} \text{ cm}^{-2}$ on sapphire. The lower than expected mobility on SiC is attributed to both a high density of large point defects ($\approx 200 \text{ cm}^{-2}$) originating from the substrates and propagating throughout the epitaxial layers, and interface roughness in the higher 2DEG density case [20,21]. Low channel sheet resistances of $275 \text{ }\Omega/\text{square}$ on SiC were measured, along with typical sheet resistances of $400 \text{ }\Omega/\text{square}$ on sapphire.

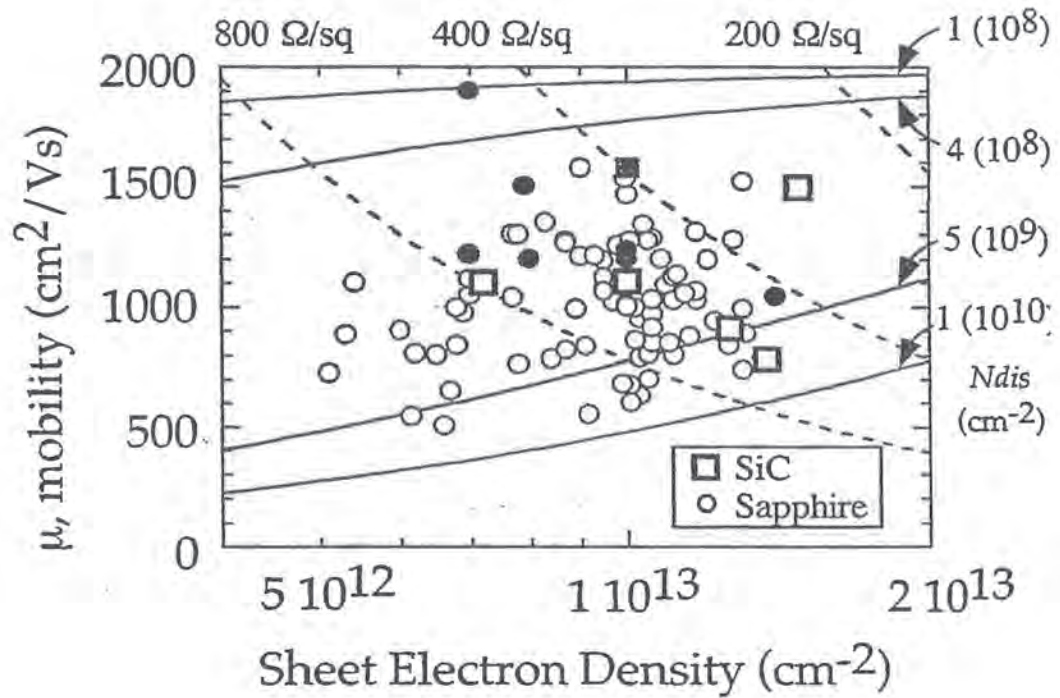


Figure 5.17. Mobility versus 2DEG sheet carrier densities of AlGaIn/GaN heterostructures grown on SiC and sapphire substrates. Solid lines are defect density (cm^{-2}) contours and dashed lines are channel sheet resistivity contours. Solid symbols are sighted from literature (12-19).

5.5.3 Buffer Layer Resistivity

Emphasis has been placed on reducing free carriers and defects in the GaN buffers to make the layer highly resistive to ensure good device isolation, low leakage current, “hard” pinch-off characteristics, low output conductance and low RF losses in large signal operation. To obtain highly resistive buffer layers, the material has to be either: (1) very pure and free from defects or (2) free carriers present need to be compensated. Since there is no low defect GaN substrate currently available, defects will be unavoidable for growth on foreign substrates. Therefore, compensation is the only viable method for producing highly resistive films in the GaN material system at this time. The possible sources of free electrons are from Silicon and Oxygen incorporating into the crystal or charged defects. Carbon, Magnesium and Iron produce acceptor states and/or defect centers required for compensation. Carbon is a by-product of the growth process from organometallics and can be controlled by varying the V/III ratio during the growth. As the V/III is increased more Carbon is present in the crystal. The Carbon level should be targeted to be slightly higher than the residual Silicon plus Oxygen level. Excessive Carbon incorporation will result in highly resistive films but will start degrading the RF performance of the devices. Magnesium and Iron were not explored due to the memory effects and possible contamination of the reaction cell.

Typical secondary ion mass spectroscopy (SIMS) data show Carbon levels near $1 \times 10^{17} \text{ cm}^{-3}$, Silicon levels of $2 \times 10^{16} \text{ cm}^{-3}$ and Oxygen at $6 \times 10^{16} \text{ cm}^{-3}$. Figure 5.18 shows a SIMS scan of a 1 μm thick GaN buffer on a sapphire substrate. The layer is highly resistive ($1.4 \times 10^8 \Omega\text{-cm}$ at 300° K – see Figure 5.21) with the Carbon level just above the sum of the Oxygen and Silicon. The

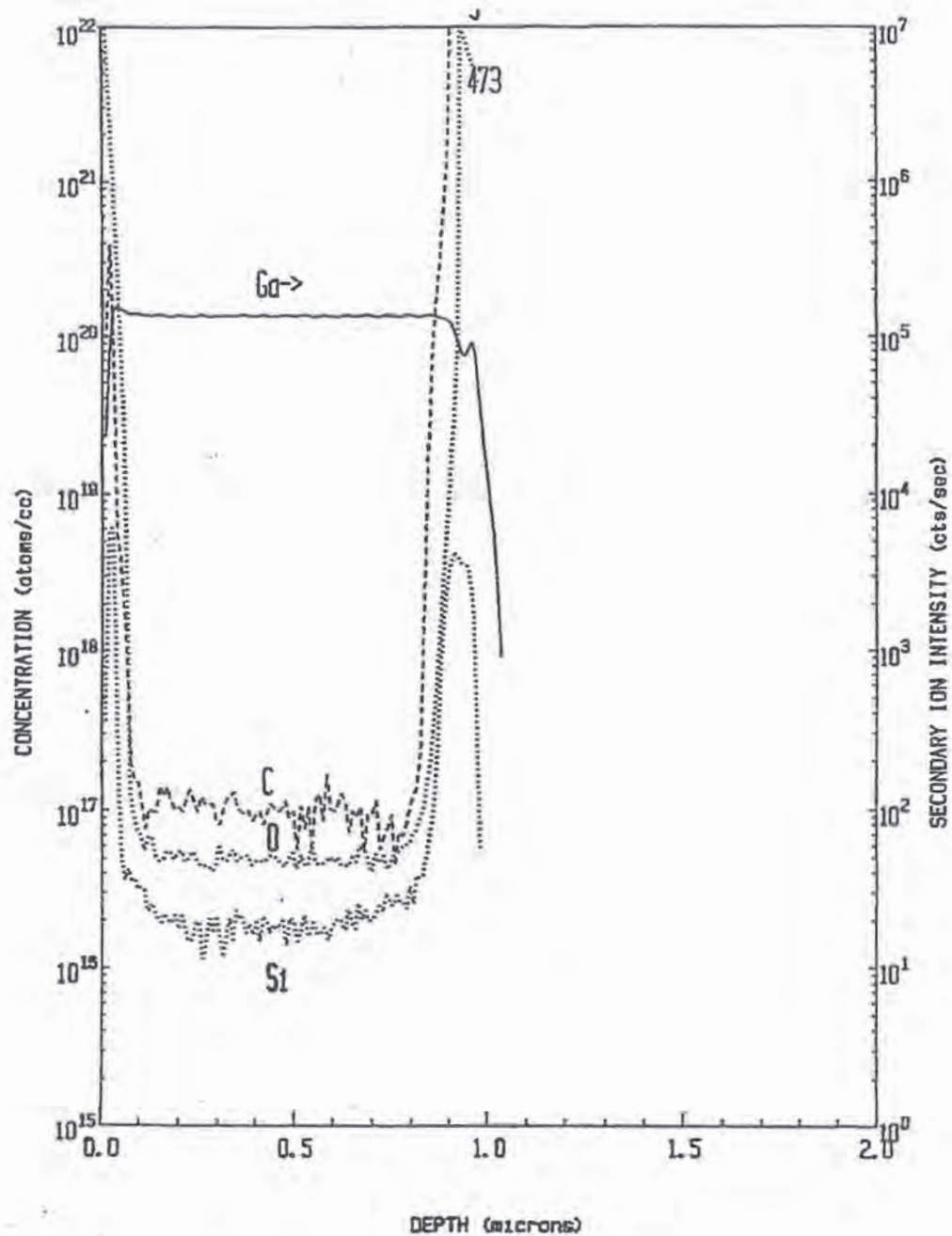


Figure 5.18 SIMS data on a GaN 1 μm thick buffer layer (III473). High temperature Hall measurements and resistivity values are given in Figure 5.22 for the same sample.

defects in the GaN buffer are not detectable by SIMS and can contribute to mobile charge that will require compensation by Carbon or Carbon related defects (acceptors). Since the layer is very resistive, the free electron contribution from defects must be less than $2 \times 10^{16} \text{ cm}^{-3}$ (at least in this particular case).

Also, the substrate/epitaxy interface has to be non-conducting and reduce or eliminate injection of carriers into trap states in the SiC substrate under high field conditions. Band gap engineering in the buffer layer(s) can isolate the active regions of the device from the defective nucleation layer and/or traps in the substrate. Once a planar growth front is established using the single step AlGaIn nucleation process, an AlN "sub-buffer" can be inserted that isolates the active region of the device from the substrate/epitaxy interface and/or traps in the SiC substrate. Advantages of the sub-buffer are seen in the reduction of gate leakage current and improved breakdown voltages on both SiC and sapphire substrates. The improvement observed in devices on sapphire is unexpected and indicates that the AlN sub-buffer also screens the device from the defective nucleation layer and not necessarily just from traps or defects in the substrates. This is shown in the top graphs in Figure 5.19 where the break down voltages increased from 20 to 30 volts (left) to over 100 volts with the insertion of a 2000 Å thick AlN sub-buffer. Gate lengths in microns are given in the figure. The bottom plot shows the 3-T break down characteristics for devices fabricated on SiC with the same 2000 Å thick AlN buffer. Break down voltages range from 82 volts to over 100 volts

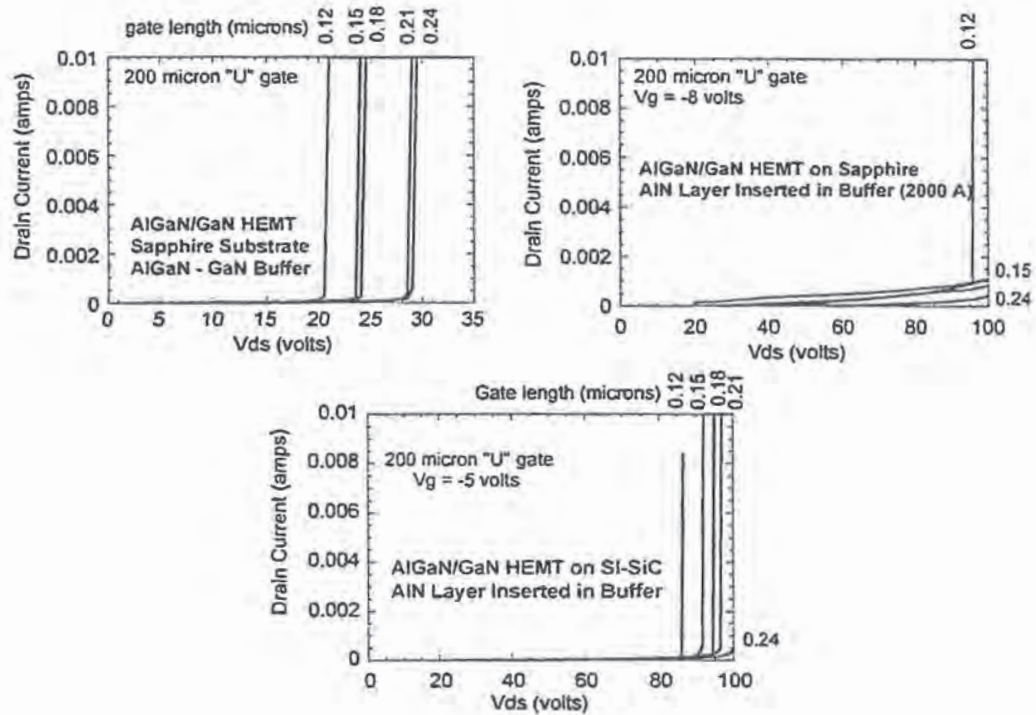


Figure 5.19 Three terminal breakdown characteristics on devices with AlGaIn nucleation layers with and without an AlN "sub-buffer". Top graphs compare these two different buffer structures on sapphire substrates, while the bottom graph gives test results on SiC with the AlN inserted.

depending on the gate lengths. The slightly lower break down voltage might be an artifact of defects in the SiC substrates. Thicker sub-buffers up to 5000 Å were grown but adversely affect the transport properties of the 2DEG and were not fabricated into devices. Thinner AlN buffers (down to 500 Å) were grown that did not improve the break down or device leakage characteristics.

Another method of accessing the GaN buffer layer is to measure the carrier concentration profile derived from variable frequency C-V measurements. At lower frequencies, slow acting traps release electrons that are easily detected as seen in the top plot in Figure 5.20. As the test frequency decreases, charge is moving towards the epitaxy/substrate interface (thick vertical line gives the epitaxy/substrate interface). These are an indication that traps along the epitaxy/substrate interface or within the defective nucleation layer are being uncovered. As the frequency is further lowered, traps in the GaN buffer are exposed and start contributing to the mobile charge seen within the buffer. The lower plot gives no indication of a frequency dependency on trapped carriers. As the frequency goes from 100 KHz down to 40 Hz, no trap related carriers are detected.

High temperature Hall effect measurements were done on a 1 μm thick GaN buffer (III473) on a sapphire substrate. The room temperature (300° K) resistivity is extracted to be $1.4 \times 10^8 \Omega\text{-cm}$. Measured resistivity at varying temperature is given in Figure 5.21 with an activation energy of 0.47 eV. As the devices heat up, especially on sapphire substrates, the buffer layer and substrate has to remain highly resistive. At a reasonable channel temperature of 200° C, the extracted resistivity of the near-by buffer is estimated to be $2.1 \times 10^5 \Omega\text{-cm}$. The graph to the right compares GaN layers grown by conventional OMVPE (Aixtron) and MBE (SVT) to the material grown for this work. The

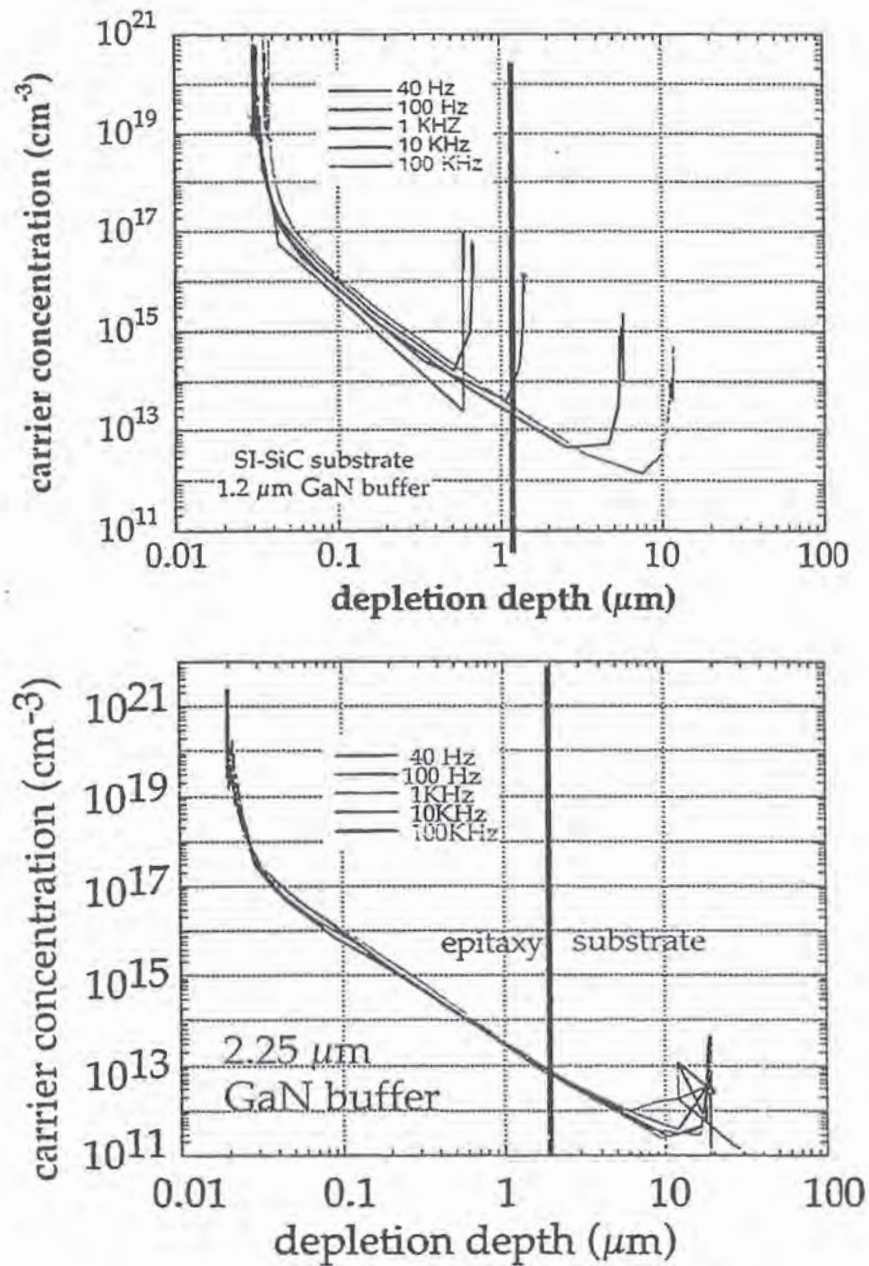


Figure 5.20. Carrier concentration profile derived from C-V measurements at different frequencies. The top plot shows mobile charge increasing as the test frequency is lowered. The bottom plot shows a clean buffer with no carriers exposed at the lower frequency.

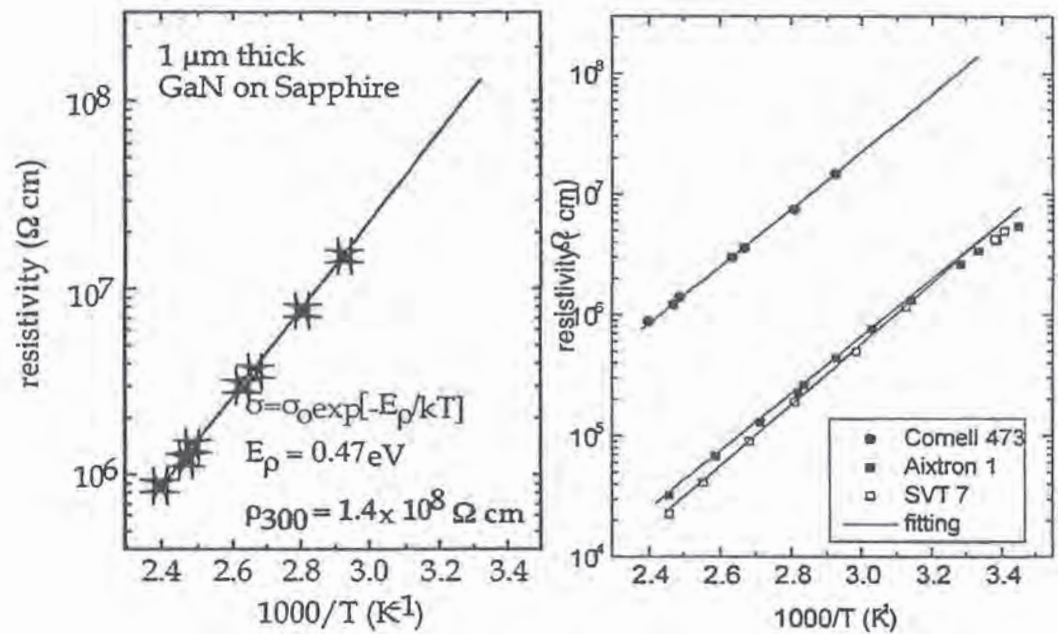


Figure 5.21. GaN buffer layer resistivity measured by high temperature Hall Effect measurements. GaN is 1 μm thick on a sapphire substrate. Plot to the right is a comparison of material grown for this work (top most line) with material supplied from Aixtron and MBE grown material (SVT). (Measurements Courtesy of Peter Kordos – ISU)

activation energies are about the same ~ 0.50 eV. Material grown by FME has around 100 times greater resistivity than the other two samples.

5.6 Summary

Sapphire and SiC substrates were used for epitaxial GaN and AlGaN growth. Both severely mismatched substrates posed challenges for successful nucleation and planar growth. Sapphire substrates were plagued with surface scratches while SiC crystals were of lesser quality with nano-, micro- and macro- defects that propagate throughout the subsequent epitaxial layers. SiC substrates also showed cracking and large areas of inclusions from the substrate fabrication process. Besides structural damage, consistency from substrate-to-substrate and from batch-to-batch was lacking, constantly changing the requirements for nucleation. First, a two-temperature nucleation process was developed that resulting in planar films with very high free carrier backgrounds unacceptable for HEMT structures. A single high temperature nucleation process was then discovered that involved an OM-Preflow to produce a metallic surface that aided in the wetting of the substrate surface on both sapphire and SiC.

After achieving acceptable nucleation layers, the GaN buffer was optimized in respect to thickness uniformity, threading dislocations, yellow band emission and resistivity. Reactor transport flows were increased from 24 LPM to 48 LPM to improve thickness uniformity across the 2 inch diameter wafers. Threading dislocation densities were mapped and a model was proposed to predict their effect on low field mobility. Lastly, the resistivity of the GaN buffer along with the nucleation layers was measured using high temperature Hall measurements yielding room temperature resistivity of $1.4 \times 10^8 \Omega\text{-cm}$.

Chapter 5 References

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CHAPTER 6

AlGaN BARRIER GROWTH AND AlGaN/GaN HEMT STRUCTURES

6.1 Introduction

After obtaining suitable nucleation and GaN buffer layers, growth efforts focused on producing high quality AlGaN barriers and undoped AlGaN/GaN heterostructures on both sapphire and semi-insulating SiC substrates. Devices were designed to have an undoped 50 Å to 250 Å thick $\text{Al}_{0.30}\text{Ga}_{0.70}\text{N}$ barrier deposited on highly resistive GaN buffers, producing a polarization induced sheet charge around $1 \times 10^{13} \text{ cm}^{-2}$ at the heterostructure.

First, a discussion on the polarization effects of wurtzite GaN and AlGaN will be given to understand the importance of composition, thickness and state-of-strain. Then AlGaN barriers optimization to produce a smooth atomically flat growth fronts are presented. Thickness and composition of the pseudomorphic barrier is mapped out and any relaxation of the barrier is determined from X-ray analysis. Once the AlGaN barrier is optimized, uniformity and repeatability studies are undertaken to understand possible variation in the thin barrier layer across the 2-inch substrates. Preliminary reliability studies are performed on Hall samples with different AlGaN barriers. Finally, dc and RF test results on fabricated devices are presented on both sapphire and SiC substrates.

6.2 Polarization Induced 2DEG

Despite the absence of intentional doping in the HEMT structures, high sheet carrier concentrations ($n_s > 10^{13} \text{ cm}^{-2}$) forming a 2DEG are observed by C-V at the $\text{Al}_{0.30}\text{Ga}_{0.70}\text{N}/\text{GaN}$ interface that is a consequence of the piezoelectric and spontaneous polarization induced sheet charge (σ) [1-3]. For the growth in the (0001) orientation of pseudomorphic Ga-face $\text{AlGa}\text{N}/\text{GaN}$ heterostructures, there will be a spontaneous polarization P_{sp} present in the wurtzite AlGaN and GaN layer ($|P_{sp}(\text{AlGa}\text{N})| > |P_{sp}(\text{GaN})|$) and an additional piezoelectric polarization P_{pe} in the strained AlGaN barrier [1]. The different polarizations in the AlGaN barrier and the GaN buffer will cause a positive sheet charge $+\sigma$ at the $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ interface, which can be calculated by [1,2]:

$$\sigma(\text{AlGa}\text{N} / \text{GaN}) = P_{pe}(\text{AlGa}\text{N}) + P_{sp}(\text{AlGa}\text{N}) - P_{sp}(\text{GaN}) \quad 6.1$$

and,

$$\sigma(\text{AlGa}\text{N} / \text{GaN}) = 2e_{31} \left(c_{11} + c_{12} - \frac{2c_{13}^2}{c_{33}} \right) \left(\frac{a(\text{GaN})}{a(\text{AlN})} - 1 \right) x + P_{sp}(\text{AlGa}\text{N}) - P_{sp}(\text{GaN}) \quad 6.2$$

where, $a(\text{GaN})$, $a(\text{AlN})$ are the lattice constants of GaN and AlN given in Table 2.2. The relevant piezoelectric constant, elastic constants and spontaneous polarization (e_{31} , c_{11} , c_{12} , c_{13} , c_{33}), lattice constants and $P_{sp}(\text{AlGa}\text{N})$ are linear approximations from the data given in Table 2.2 and from reference 4 as:

$$\text{lattice constants:} \quad a_o(x) = -0.077x + 3.189 \text{ \AA} \quad 6.3$$

$$c_o(x) = -0.203x + 5.189 \text{ \AA} \quad 6.4$$

elastic constants:	$C_{13}(x) = (5x + 103)GPa$	6.5
	$C_{33}(x) = (-32x + 405)GPa$	6.6
spontaneous polarization:	$P_{sp}(x) = (-0.052x - 0.029)\frac{C}{m^2}$	6.7

The spontaneous and piezoelectric contribution to the bound charge at the heterostructure is plotted in Figure 6.1 for a 300 Å thick barrier with various Al compositions. The spontaneous contribution (last 2 terms in equation 6.1) is slightly higher than the piezoelectric component. The top line represents the sum of both the spontaneous and piezoelectric polarization to the bound charge without consideration given to surface effects. The dotted line is the calculated density of the free electrons compensating the bound charge with surface depletion being taken into account. The bound charge (and hence the 2DEG density) increases as the Al content increases as expected. As the Al content decreases, surface effects become more dominate depleting a larger percentage of the electrons present in the 2DEG. With increasing levels of Al, the free electron densities approach that calculated from the total polarization present.

Electrons, which tend to compensate the polarization induced bound sheet charge causes a 2DEG if the band offset (ΔE_c) is sufficiently high and the structural quality of the interface is good. The maximum sheet carrier in the 2DEG (caused by polarization effects) for nominally undoped HEMTs can be calculated by [1]:

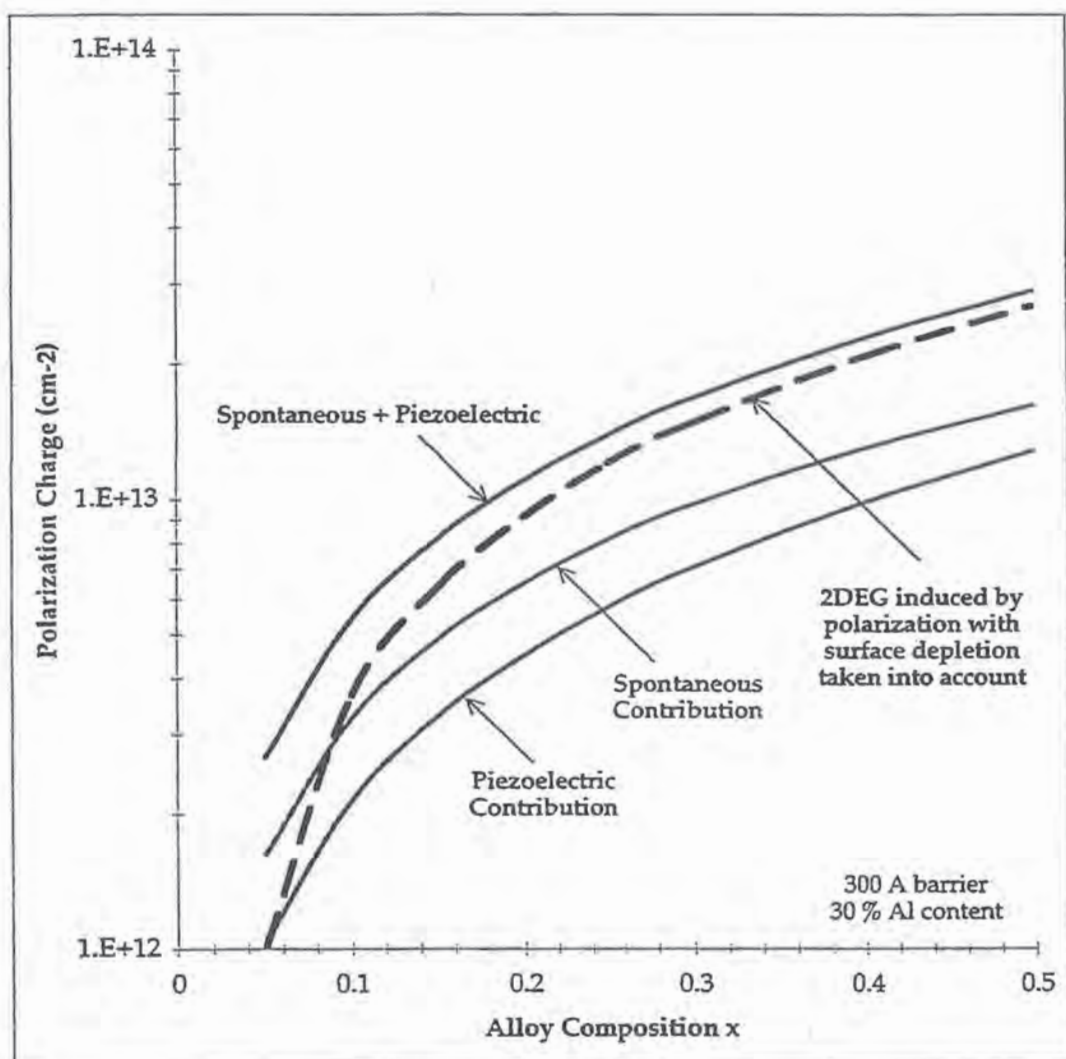


Figure 6.1 Bound charge at the AlGaIn/GaN heterostructure from both spontaneous and piezoelectric contributions. The dashed line represent the electron density in the 2DEG required to compensate out the positive bound charge, taking into account the surface effects.

$$n_s(x) = \frac{\sigma(x)}{e} - \left(\frac{\varepsilon(\text{AlGaIn})}{de^2} \right) (e\phi_b(x) + E_F(x) - \Delta E_C(x)) \quad 6.8$$

where, $\varepsilon(\text{AlGaIn})$ is the dielectric constant of AlGaIn, d is the width of the barrier, $e\phi_b(x)$ is the Schottky barrier of the gate contact (for $x = 0.3$, $e\phi_b \approx 1.25$ eV) and $E_F(x) - \Delta E_C(x)$ is the energy difference between the Fermi level and the conduction band offset (for $x = 0.3$, $E_F - \Delta E_C \approx 0.42$ eV) [3].

In more general terms, the following linear interpolations for the physical properties of the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ are used:

$$\text{dielectric constant:} \quad \varepsilon(x) = -0.3x + 10.4 \quad 6.9$$

$$\text{Schottky barrier:} \quad e\phi_b(x) = (1.3x + 0.84)\text{eV} \quad 6.10$$

$$\text{Band offset:} \quad \Delta E_C(x) = 0.7(E_g(x) - E_g(0))\text{eV} \quad 6.11$$

$\text{Al}_x\text{Ga}_{1-x}\text{N}$ band gap:

$$E_g(x) = xE_g(\text{AlN}) + (1-x)E_g(\text{GaN}) - x(1-x)1.0\text{eV} \quad 6.12a$$

and,

$$E_g(x) = x6.13\text{eV} + (1-x)3.42\text{eV} - x(1-x)1.0\text{eV} \quad 6.12b$$

For $\text{Al}_{0.30}\text{Ga}_{0.70}\text{N}/\text{GaN}$ HEMT structure, the positive polarization induced sheet charge and the maximum sheet carrier concentration of the 2DEG to be $1.67 \times 10^{13} \text{ coul}\cdot\text{cm}^{-2}$ and $1.48 \times 10^{13} \text{ cm}^{-2}$ respectively. The calculated results are in good agreement with the sheet carrier concentrations of $1.1 \times 10^{13} \text{ cm}^{-2}$

and $1.4 \times 10^{13} \text{ cm}^{-2}$ observed by C-V profiling for structures grown on sapphire and SiC, respectively [5]. Selected values for the 2DEG density calculated from equation 6.8 for varying Al content and barrier thicknesses are given in Table 6.1.

Table 6.1 Calculated values of 2DEG density with varying Al content and barrier thickness.

Al (%) in Barrier	AlGaN Thickness			
	300 Å	200 Å	100 Å	50 Å
	$n_s(x)$	$n_s(x)$	$n_s(x)$	$n_s(x)$
5	1.01E+12	2.27E+11	---	---
10	3.64E+12	2.81E+12	4.80E+11	---
15	6.34E+12	5.48E+12	3.02E+12	2.10E+11
20	9.11E+12	8.21E+12	5.65E+12	1.12E+12
25	1.20E+13	1.10E+13	8.37E+12	3.69E+12
30	1.48E+13	1.39E+13	1.11E+13	6.33E+12
35	1.78E+13	1.68E+13	1.40E+13	9.07E+12
40	2.08E+13	1.98E+13	1.70E+13	1.19E+13

Figure 6.2 plots the 2DEG density over a large range of AlGaN composition for various barrier thicknesses from 50 Å to 300 Å. From the calculations, it is seen that there is little difference in the 2DEG density between 200 Å and 300 Å barrier thicknesses. The thinner 200 Å barrier will lead to improved modulation efficiency and higher frequency response but can result in lower breakdown voltages. Electron densities at 30 % Al are given in the plot. As the barrier becomes thinner, the charge present at the surface (trapped electrons) begins to deplete the 2DEG. Figure 6.3 clearly shows this effect on heterostructures with 30 % and 50 % Al content in the barrier. The solid lines

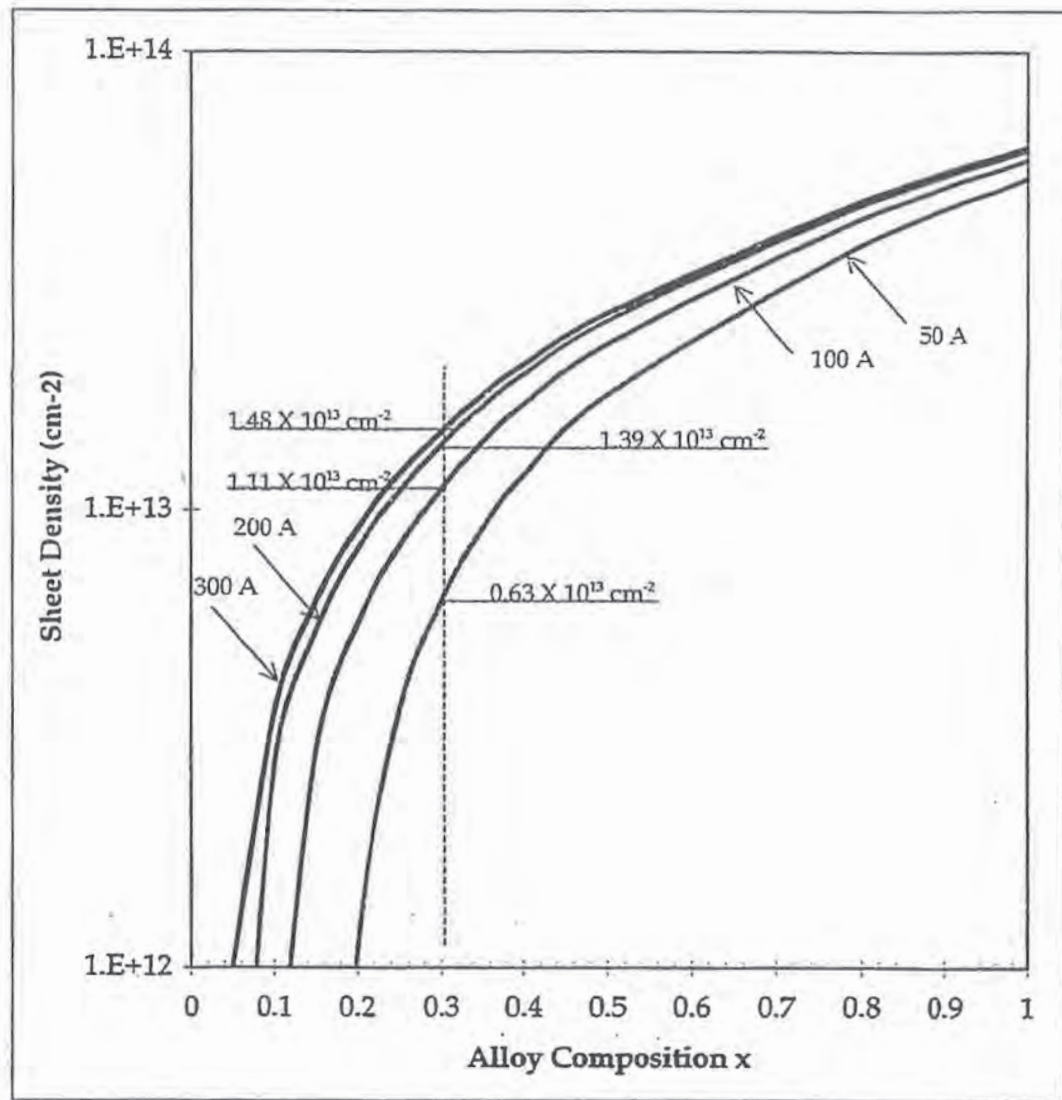


Figure 6.2 2DEG densities calculated from equation 6.8 with varying Al content in the barrier. The different lines represent different barrier layer thicknesses as depicted in the figure. Values of the 2DEG density at 30 % are given for the different barrier thicknesses.

represent calculated values from equation 6.8, while the data points correspond to measured values from this work. Excellent agreement is observed between the calculated and measured values. As the 50 % Al barrier get thicker, the layer begins relaxing and the 2DEG density does not follow the calculated values (200 Å data pt). More importantly, with very thin barriers, the entire 2DEG can be depleted leading to enhancement mode devices. With barriers under 50 Å, no 2DEG is detectable with C-V or Hall measurements on the 30 % samples. The surface can than be passivated with ~ 200 Å of SiN and the predicted 2DEG density returns to the heterostructure [6]. Although an interesting topic, enhancement mode devices were not explored within the scope of the work presented here.

6.3 AlGaN Barriers

Placing very thin films (several hundred Angstroms) of $\text{Al}_{0.30}\text{Ga}_{0.70}\text{N}$ on atomically flat GaN is expected to replicate the surface and produce atomically flat growth fronts. This however was not the case and growth conditions for the AlGaN barrier had to be optimized. The two major growth parameters governing the AlGaN quality are temperature and V/III ratio. At temperatures below 1005° C, the unintentional background carrier concentration in the AlGaN barrier dramatically increases from the mid 10^{16}cm^{-3} to high 10^{18}cm^{-3} (charged defects). At higher temperatures the material quality improves but the growth rates and compositional control gets worse due to surface desorption.

First, the V/III ratios were explored which also involved growth condition changes in the GaN channel near the heterostructure to accommodate required flow changes. Next, the thickness and compositional

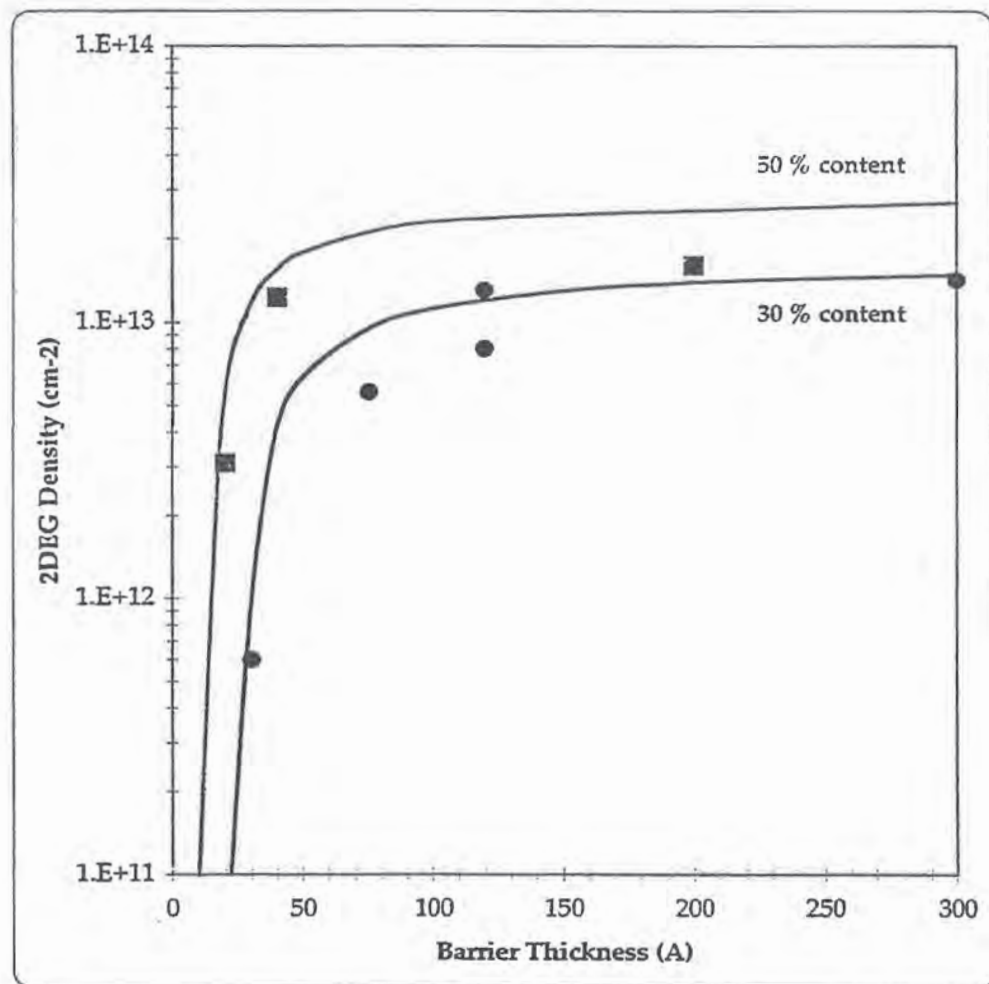


Figure 6.3 Plot of different barrier thicknesses with 30 % and 50 % Al content. The circles represent measured results from the 30 % barriers while the squares are measured results from the 50 % barriers.

limits had to be investigated for producing pseudomorphic AlGa_N layers required for high 2DEG densities and reliable devices. Once the acceptable parameter space is defined, uniformity and repeatability of producing the thin undoped 50 Å to 250 Å layers had to be understood. Finally, reliability issues related to the top AlGa_N barrier are discussed.

6.3.1 V/III Ratios

The V/III ratio not only effects the surface reactions but also can cause pre-reactions in the gas phase upstream from the wafers. Pre-reactions involving the oxidation of the aluminum will result in particle contamination of the surface and result in rough and/or 3-dimensional growth fronts. This is similar to contamination of the surface discussed in Section 5.3.2 without a cell bake between epitaxial runs. To reduce any pre-reactions, the V/III ratio should be as low as possible and the group V species (ammonia) and the TMA should be physically separated as much as possible before flowing over the wafer surface.

It has been reported that aluminum bearing layers in the nitride system grow best at lower V/III ratios than GaN [7]. Figure 6.4 show AFM images of AlGa_N surfaces at two different V/III ratios, with a targeted aluminum percentage of 35 %. The image on the left was grown with the same ratio as the underlying GaN layer (~1800 in the growth zone). The surface is very rough with crevasses extending all the way through the AlGa_N, down to the GaN channel layer. Rutherford Back Scattering (RBS) measurements show a large variation in Al content in this barrier layer, with 52 % Al detected at the surface, 29 % in the majority of the barrier and 72 % near the AlGa_N/GaN heterostructure. Reducing the V/III ratio to ~900 yielded smoother surfaces with step flow growth as shown in the AFM image the right. RBS analysis of

this film shows 34 % aluminum content with a ± 2 % variation throughout the film. Even though the AlGaIn quality and uniformity were dramatically improved with the lower V/III ratio, there still exist large grain-boundaries (shown within the circle in the right image) that may affect RF-to-dc dispersion and device reliability. Two other data points were explored, one at a V/III ratio of ~ 1250 which resulted in similar surfaces to that of the V/III ratio of at 1800 (image to the left) and one at a V/III ratio ~ 450 which did not produce a 2DEG. All structures producing a 2DEG exhibited similar room temperature electron transport properties and sheet densities. It should be noted that the V/III ratio is changed in the GaN buffer just prior to the channel region. A 500 Å thick, lower V/III ratio, GaN channel is grown where the 2DEG resides. Experimental data with GaN channels grown at a V/III of 900 with different thickness showed no degradation of the room temperature electron mobility. Structures were also grown with the V/III changed in the initial growth of the AlGaIn barrier, which produced sub-standard AlGaIn quality and caused gas flow oscillations during the entire AlGaIn barrier growth (~ 2 minutes). Growth stops at the heterointerface while changing the V/III ratio were attempted which caused a macroscopic smoothing of the growth surface but did not change the room temperature transport properties of the 2DEG and was not pursued further. Further studies are required to "close" the openings observed in the AlGaIn layer shown in the right hand image. It should be noted that the cool-down cycle might adversely affect the top surface. Hydrogen etching (most likely from the decomposition of the ammonia) of defects could damage the surface.

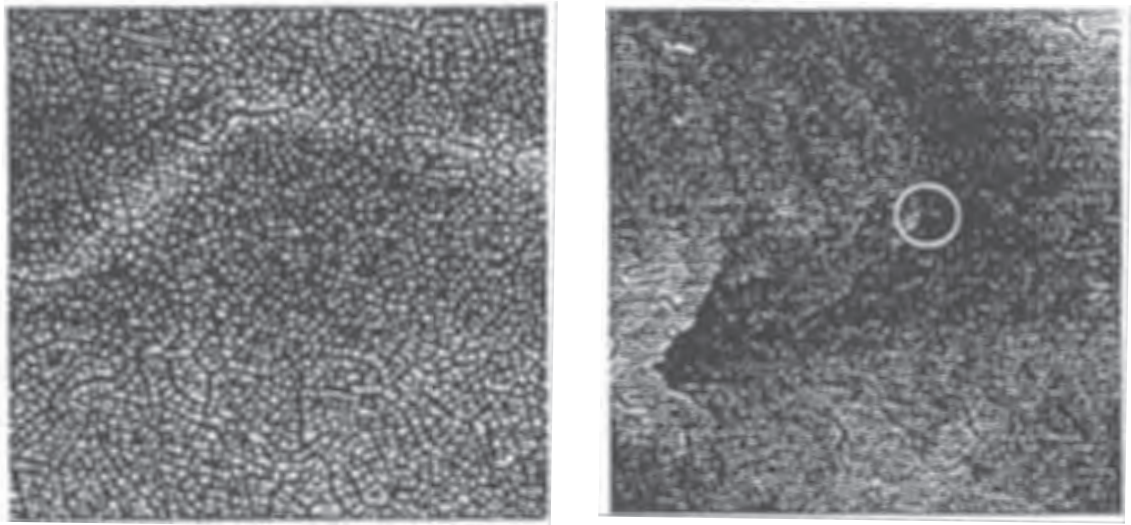


Figure 6.4. AFM images of terminated surfaces of 200 Å thick $\text{Al}_{0.30}\text{Ga}_{0.70}\text{N}$ barrier layers. Image to the right has a V/III ratio of ~1800 producing cracked 3-dimensional surfaces. The image to the left shows a 2-dimensional surface with a V/III ratio reduced to ~900.

A GaN cap or cooling in nitrogen instead of ammonia might reduce or eliminate such damage and minimize the defects at the terminated surface (see Future Work – Chapter 7).

The Aluminum content can be estimated from PL measurements and calculated taking strain into effect from the equations presented in Section 2.3.1. A typical room temperature PL spectrum of a structure incorporating the best AlGa_N (V/III ~900) is given in Figure 6.5 where the GaN peak is seen at 362.3 nm and the AlGa_N is observed at 310.6 nm corresponding to 31.3 % Al in the solid. The FWHM are given in the figure, with the AlGa_N being a narrow 133 meV indicating good crystal quality for a layer only 250 Å thick.

6.3.2 Pseudomorphic AlGa_N Layers

To achieve high 2DEG densities, the contribution from piezoelectric polarization has to be maximized. This polarization component is dependent on the strain between the AlGa_N barrier and the GaN channel and needs to be pseudomorphic and relatively free of defects. It is believed that the strain field at the heterostructure is established in the first several monolayers of the AlGa_N, the remainder of the AlGa_N barrier is necessary to remove the surface from the channel and to form the ohmic source-drain contacts as well as the Schottky gate contact. The majority of the structures grown for this work contain barriers with ~30 % Al in the entire barrier. Several structures were grown with higher Al composition within the first 15 Å to 20 Å of the AlGa_N barrier (50, 75 and 100 %) to increase the piezoelectric contribution to the

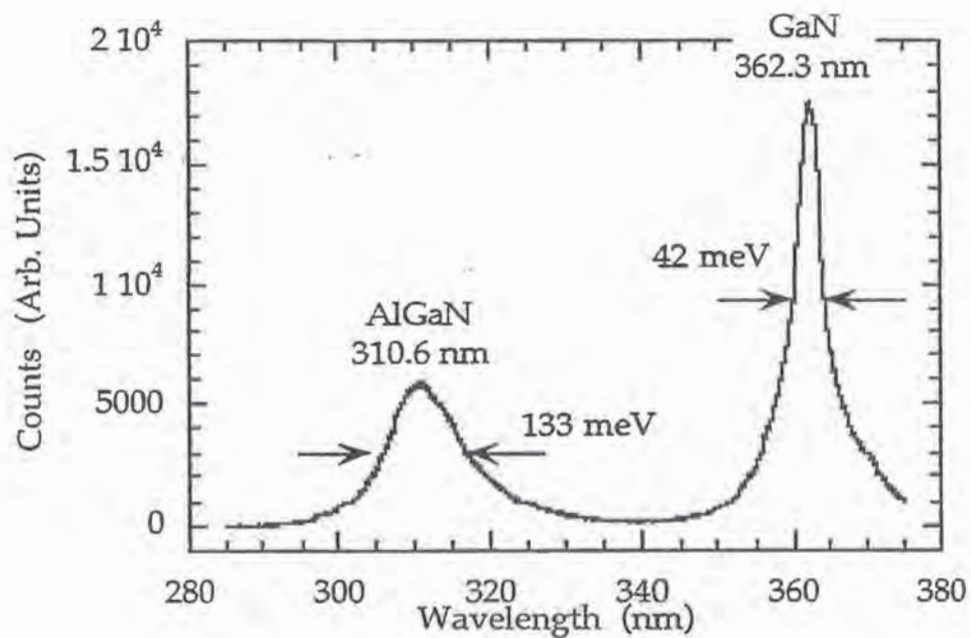


Figure 6.5. Room temperature PL measurement of an AlGaN/GaN HEMT grown on sapphire. The AlGaN peak at 310.6 nm corresponds to 31.3% Al in the solid.

2DEG. The 2DEG density increases with increasing Al content present in the thin layer at the heterostructure, from $1.10 \times 10^{13} \text{ cm}^{-2}$ to $1.29 \times 10^{13} \text{ cm}^{-2}$ to $1.62 \times 10^{13} \text{ cm}^{-2}$ for 50, 75 and 100 % respectively. The Al was then graded down to 25 % to 30 % to aid in the ohmic contact formation. When the higher composition “interlayer” at the heterostructure exceeds 15 Å to 20 Å, ohmic contacts become problematic (difficult alloying through the wide band gap interlayer to the 2DEG). The larger band gap associated with the interlayer increases the conduction band offset and reduce the overlap of the electron wavefunction into the lower mobility AlGaN barrier, theoretically improving the average electron transit velocity. For the work presented here, the higher Al structures were not further discussed due to the lack of processed devices to draw meaningful results.

6.3.2.1 Aluminum Composition

As the Al content increases in the AlGaN barrier, the layer will exceed its critical thickness and start relaxing at defects or by the formation of misfit dislocations. As this happens, coherent strain is no longer present and the piezoelectric contribution to the 2DEG can be reduced. Both the thickness and Al composition play a role in this effect as discussed in Section 2.2.1. This section will discuss the role of the Al composition.

From reciprocal space mapping, strain relaxation is detected in 300 Å thick barriers at or above 38 % Al content. As the Al content increases, the relaxation increases as defined by the semi-empirical formula for 300 Å barriers [8]:

$$r(x) = \begin{cases} 0 & 0 \leq x < 0.38 \\ 3.5x - 1.33 & 0.38 \leq x \leq 0.67 \\ 1 & 0.67 < x \leq 1 \end{cases} \quad 6.13$$

The lattice constants from the partially relaxed layers can be determined and the 2DEG can be recalculated from equation 6.8. Figure 6.6 shows (20_5) reciprocal space maps for HEMT structures with 300 Å barriers with two different Al compositions of 31 % and 39 %. The map to the left shows a pseudomorphic AlGa_{0.31}N barrier (r=0) aligned with the GaN buffer layer. The map to the right shows the partial relaxation in the AlGa_{0.39}N barrier, with approximately 12 % relaxation observed. The crystal quality of the AlGa_{0.39}N barrier suffers as the layer relaxes as evident by the “noisier” scan compared to the AlGa_{0.31}N barrier mapped in the left image. The map to the right also shows a near totally relaxed 1800 Å thick Al_{0.28}Ga_{0.72}N nucleation layer. The nucleation layer is the first layer grown on the substrate and establishes its own lattice constant (r=1) once coalesced after only several hundred Angstroms of growth. The structure to the left had a very thin AlGa_{0.31}N nucleation layer (200 Å) and is not detected.

As the alloy composition increases, the degree of relaxation increases as shown in Figure 6.7. The squares are data points from this work, while the circles are from Amano et al. [9]. The one dash line is the linear estimate of strain relaxation given in equation 6.13 [oliver JAP 2001]. The solid line is a fit to the data between 35 % and 40 % composition and fits the data better than that of equation 6.13. The second dashed line is a logarithmic fit to all the data points and might be a better estimate of the amount of relaxation above 40 %. All AlGa_{0.31-0.40}N barriers were 300 Å, ± 10 Å thick.

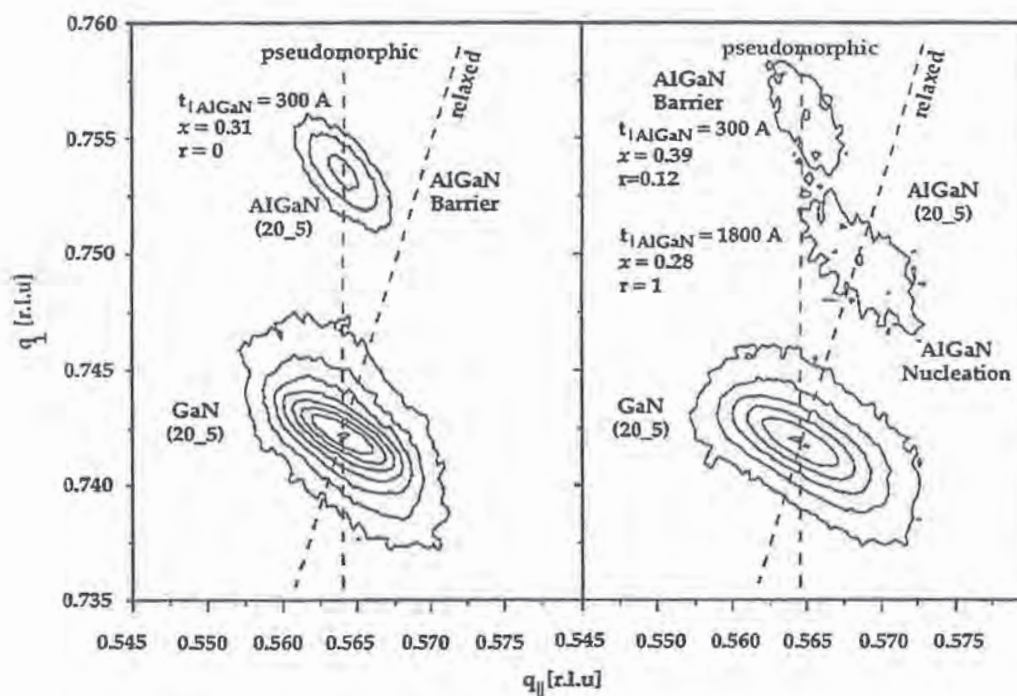


Figure 6.6. (20₅) reciprocal space maps of two different AlGaN/GaN HEMTs. The map to the left shows a pseudomorphic AlGaN barrier (31 % Al and 300 Å thick). The map to the right show the 1800 Å nucleation layer fully relaxed with a 39 % AlGaN barrier showing about 12 % relaxation. (X-ray Courtesy of Oliver Ambacher and Roman Dimitrov – Walter Schottky Institute)

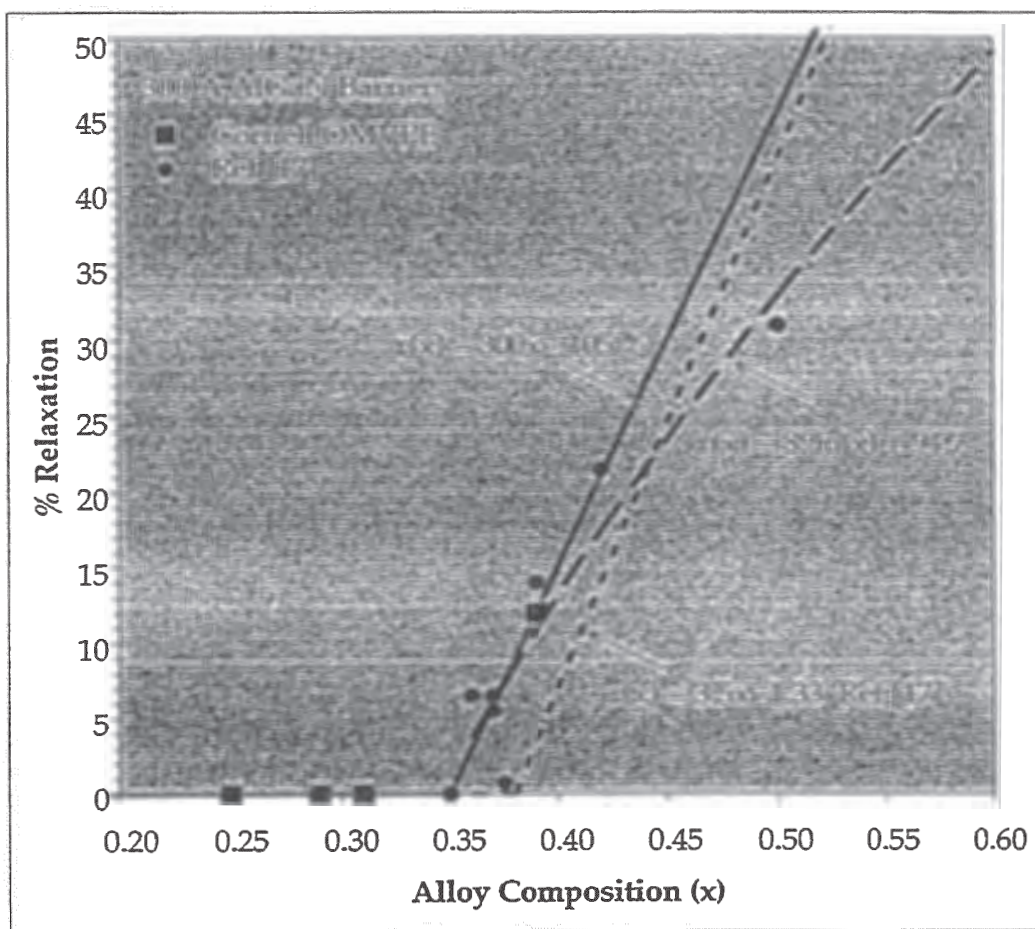


Figure 6.7. Relaxation (%) versus alloy composition for 300 Å AlGaIn barriers. The shorter dashed line is from equation 6.13, while the solid line is an improved fit to the given data points. At higher Al content, a logarithmic fit might result in a better prediction of the degree of relaxation.

6.3.2.2 Layer thickness

Since the AlGa_xN has a larger number of grain boundaries and native defects (as shown in Figure 6.4), layers can be grown thicker than the theoretical value calculated by Matthews/Blakeslee [8,10] and Fischer [11]. The calculated values for maximum Al content with 300 Å thick barriers are 14 % and 25 % from Matthews/Blakeslee and Fischer, respectively [8], which are far below what the data reveals in Figure 6.7. For the majority of the devices presented in this work, the Al GaN barriers are assumed to be pseudomorphic, with Al content below 36 % and barrier thickness of 300 Å or less.

6.3.3 AlGa_xN Uniformity and Repeatability

It has been shown in the previous sections that the AlGa_xN barrier thickness and composition play a large role in the resulting polarization induce 2DEG at the heterostructure. The majority of complete HEMT structures grown for this work were on 2-inch diameter sapphire substrates, and uniformity of the thin AlGa_xN barriers is of special concern for producing large uniform areas required for the fabrication of RF circuits.

To evaluate the AlGa_xN compositional uniformity, several multi-wafer epitaxial runs were performed on 2-inch sapphire substrates. Eight sapphire substrates were simultaneously grown on in each run, completely filling all pockets in the susceptor. The Al_xGa_{1-x}N barrier composition was checked at the center of each wafer by PL measurements, as shown for four consecutive eight wafer runs in Figure 6.8. Less than a 1 % variation in Al composition from pocket-to-pocket is observed for the different HEMT runs, with a targeted Al composition of 34 %. This demonstrates excellent uniformity for

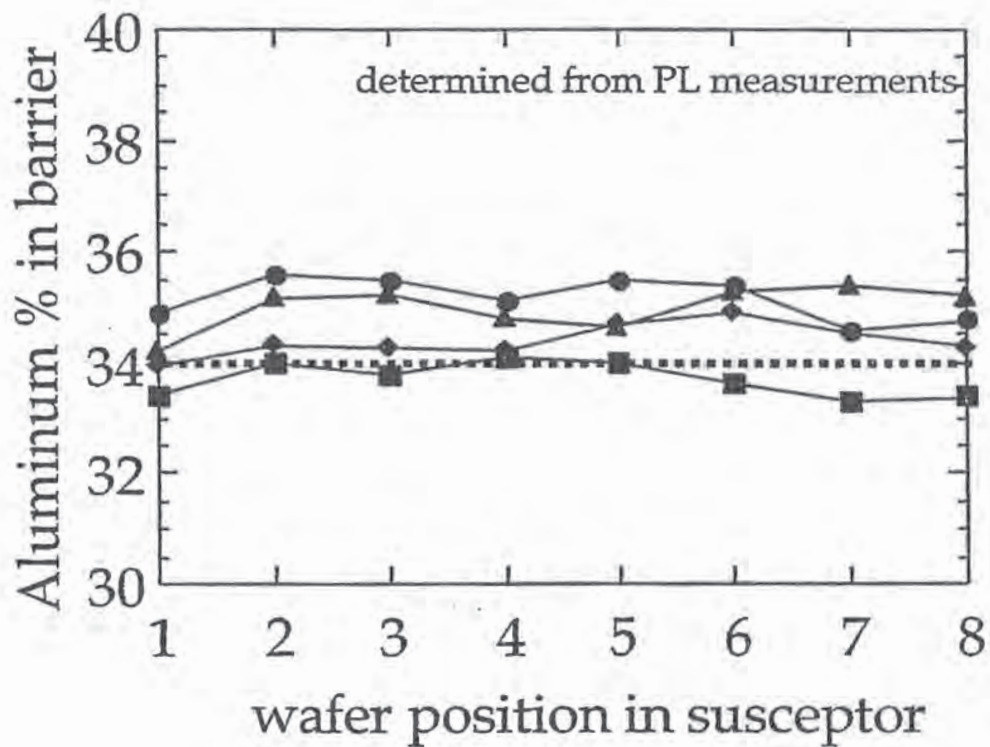


Figure 6.8. AlGaIn composition from wafer-to-wafer and between four different eight wafer epitaxial runs on sapphire substrates.

multi-wafer runs in the growth system.

Next, the compositional uniformity across each wafer was checked. Variations are seen in the direction of gas flow as in the case of GaN thickness across the wafer (Section 5.4). Figure 6.9 gives the PL spectra from five samples across a wafer from bottom to top. The compositional uniformity varies ~ 4% from 34.0 % at the top to 35.4 % near the bottom (only a 1.4 % actual change in Al content). A similar spread in composition is observed in the direction perpendicular to the gas flow. Although the compositional uniformity looks good, the PL intensity is seen to increase traveling up the wafer as observed in the top plot in Figure 6.9. Unfortunately, the increasing intensity corresponds to increasing AlGaIn thickness. The bottom graph in Figure 6.9 gives a summary of AlGaIn barrier thicknesses as derived from C-V measurements across the wafer in the gas flow direction. Different transport flows were explored in an attempt to improve the thickness uniformity. Transport flows from 32 to 48 liters per minute (LPM) hydrogen showed no improvement in AlGaIn thickness layer in contrast to GaN growth (Section 5.4). The variation observed is greater than a factor of two from top to bottom. No higher transports flows were possible due to equipment limitations, but it appears that gas phase depletion is not the cause for the non-uniformity. This is further verified by the fact that the Al composition is good across the varying thickness range. If gas phase depletion was the root cause, it is very unlikely that both the TEG (Gallium source - monomer) and TMA (Aluminum source - dimer: two OM gas molecules joined together) are depleting at the same rate to "lock" in the alloy composition. The most likely candidate is a slight temperature variation across the susceptor that significantly affects the

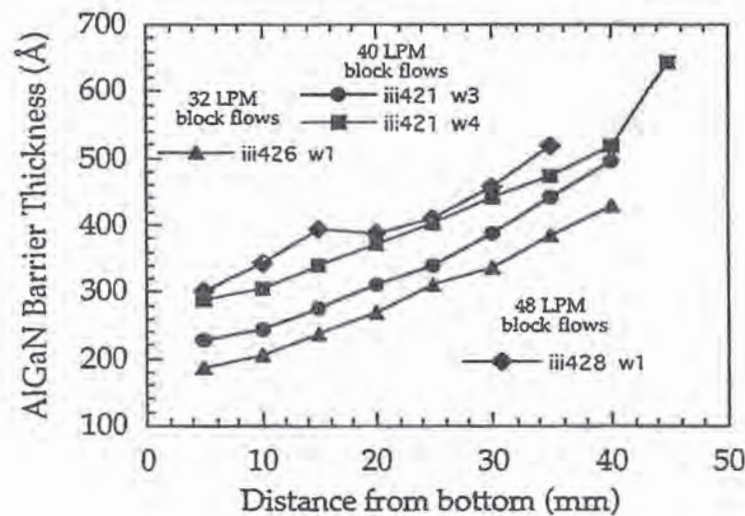
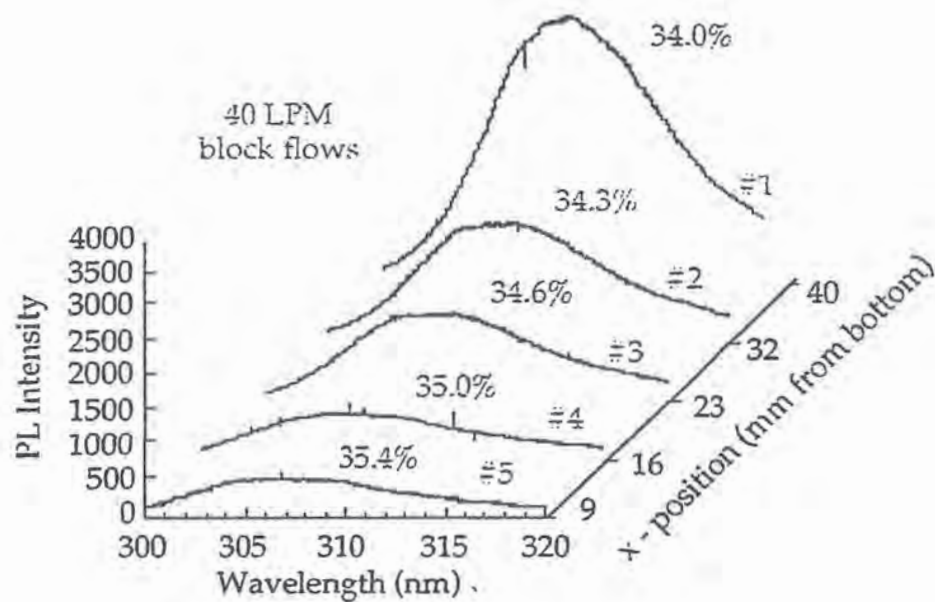


Figure 6.9 Top plot is of PL spectra on five samples across the wafer in the direction of the gas flow. The PL intensity increases towards the top of the wafer indicating that the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{In}_{0.1}\text{N}$ barrier thickness is increasing towards the top of the wafer. Bottom graph shows AlGaIn thickness uniformity along the gas flow direction. As the transport (block) flow is increased, the uniformity did not improve.

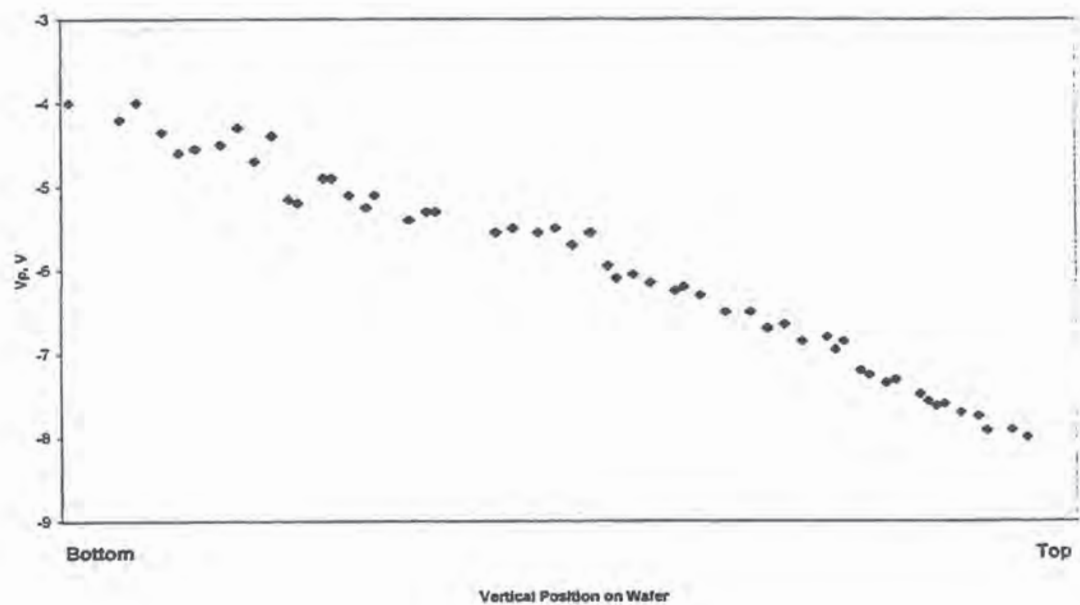


Figure 6.10 Pinch-off voltage variation from top to bottom across wafer (courtesy of Raytheon)

AlGaN growth rate. Future investigations would include redesign of the susceptor and is not addressed in the scope of work presented here. The biggest problem with the variation in AlGaN thickness is the increase in pinch-off voltage from bottom to top of the wafer. Figure 6.10 show the pinch-off variation for typical 2-inch diameter wafers with the variation going from -4 volts to -8 volts, the factor of two predicted from electrostatic calculations. For the structures grown, the AlGaN shows this type of variation across all the wafers giving a large range of barrier thicknesses. Since most of the device and circuit processing is done on 12 mm x 12 mm squares, the uniformity is considered acceptable over that sample size.

6.3.4 Reliability Issues Related to the AlGaN Barrier

Device reliability is perhaps the largest obstacle to overcome for the commercialization of high power GaN based electronics. High fields, of the order of 3 MV/cm are being applied across the thin AlGaN layer during large signal operation. Structures with the non-optimized AlGaN barriers showed device degradation over time while sitting on the shelf! This degradation is not an operational or stress test, it is a change in the device characteristics while being stored at room temperature in air. Degradation observed was a dramatic reduction in drain current at all gate biases in the I_D - V_D plane. Some devices with over 1 A/mm full channel current did not conduct at all after sitting on the shelf for 3 months. The 3-dimensional growth and Al non-uniformity (segregation) in the AlGaN can contribute to oxidation and relaxation over time, which could account of the reduction in drain current. Oxidation of the AlGaN is the most likely cause, as the 2DEG density does not appear to change significantly but the room temperature

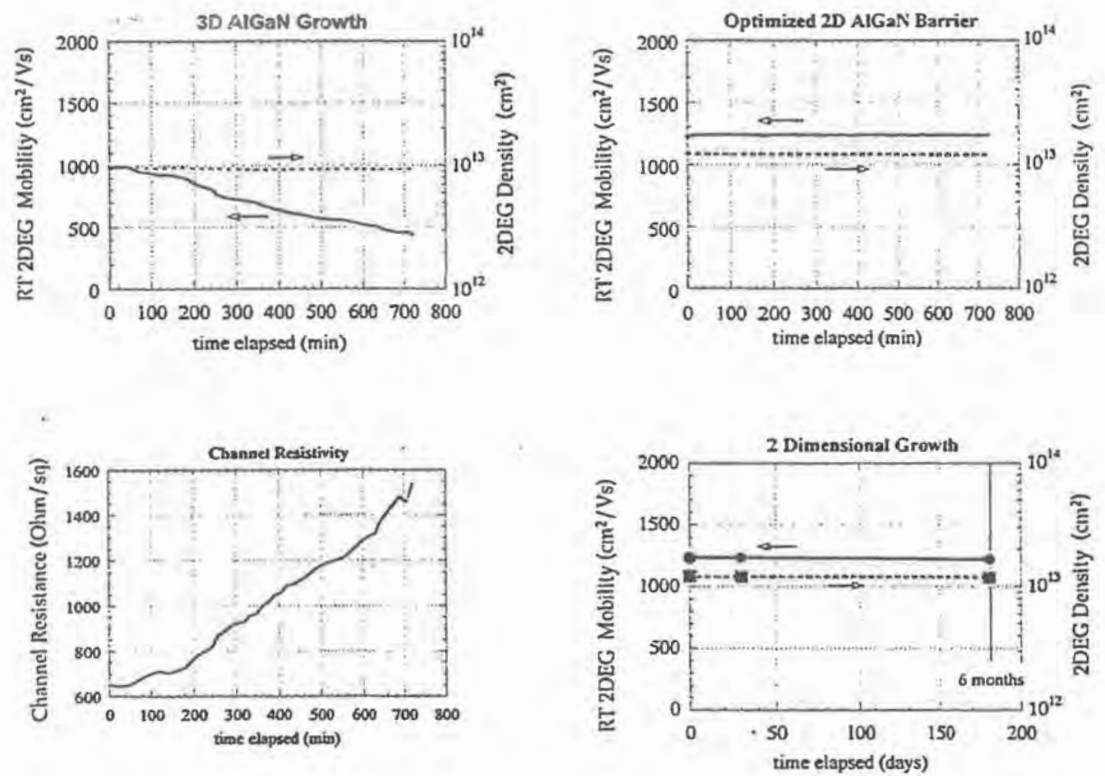


Figure 6.11 Hall measurements over time on 3-D and 2-D AlGaIn growth. The graphs to the left are of the non-optimized AlGaIn, and show degradation in RT mobility over time. The plots to the right are of devices with a 2-D AlGaIn showing no degradation over time (6 months).

mobility decreases by more than a factor of 2 over several hundred minutes stored in room ambient as observed in Hall measurements. This is shown in Figure 6.11 in the top left plot of 2DEG density and room temperature Hall mobility. The electron density does not change from Hall measurements, but the Hall mobility decreases. This will add to the channel resistance (lower left plot) and decrease drain current. The plots to the right are Hall results on the optimized AlGa_N barrier. The electron mobility is stable over time. This same sample was measured over 6 months (lower right plot) and showed no degradation over time. The Hall sample measured for the left plots did not conduct at all after 3 months of shelf storage. All AlGa_N barrier thicknesses were well below the critical thickness, eliminating cracking as the cause for the degradation

Finally, it should be noted that some wafers with the optimized AlGa_N cracked over time. There are always cracks near the edges of all the wafers and appear to propagate over time across the wafer. Therefore, whole wafers over time might develop crack structures in the AlGa_N, which will cause non-continuities in the 2DEG and degrade device performance. Wafers should either be processed soon after growth or sawn up to provide relief centers or edges for cracks that might develop to terminate. This problem is more prevalent on SiC substrated devices (run III555 for example) than for sapphire substrated devices.

6.4 Device Fabrication

Due to the inert nature of Ga_N, device processing differs significantly from GaAs device fabrication. First, there is no wet etch for Ga_N without photo assistance. Therefore, device isolation requires ion implantation or dry

etching of mesas. Next, ohmic contact formation requires very high alloy temperatures and is very sensitive to stack metals and metal layer thicknesses. Titanium is used for the contacting layer in which nitrogen is gettered out of the AlGa_N to form TiN and nitrogen vacancies during the alloying. The best electrical contact appears to be Ti/Al/Ti/Au : 200/1000/450/550 Å annealed at 825° C to 850° C in N₂. The edge acuity is less than desired and results in rough edges which could limit the device performance and breakdown voltage. Other metal stacks including tungsten as a barrier produced smoother edges but less than desirable specific contact resistance and difficulties with lift-off processes. The Schottky gate metal is Ni/Au and is defined by e-beam writing to obtain a small gate length. The most important factor in processing AlGa_N/Ga_N HEMTS is protecting the surface from damage. The mesa isolation etch cannot result in a damaged surface which can conduct under high biases and the channel region (both gated and ungated) has to be well protected during fabrication. RF-to-dc dispersion is very sensitive to the surface between the source and drain. Surface passivation using SiN_x can reduce or even eliminate the dispersion, but passivating a contaminated or damage surface will not result in optimal device performance and reliability. A complete description for the device fabrication process is given in Appendix C (courtesy of Dr. Eduardo Chumbes).

6.5 Device Test Results

The high 2DEG densities in these devices allow for full channel currents in excess of 1 A/mm. The wide band gap and thermal stability of AlN, AlGa_N and Ga_N materials support very high breakdown voltage

characteristics and allow large voltage swings across the device (100+ volts compared to 20 to 50 volts for GaAs based HEMTs). Breakdown voltages also depend on the device geometry including source-drain and gate-drain spacing as well as gate length. A semi-empirical linear relationship was determined for 3-terminal breakdown voltages as:

$$V_{bk} = \frac{35(L_g + 2t_{AlGaN})}{0.2} \quad 6.14$$

where L_g is the gate footprint, and t_{AlGaN} is the AlGaN barrier thickness (both in μm 's). For $(L_g + 2t_{AlGaN}) = 0.2 \mu\text{m}$, the drain-source breakdown is limited to approximately 35 volts.

6.5.1 Static Test Results

I-V's and transfer characteristics are given for HEMT devices on sapphire and SiC substrates. At full channel currents, self-heating effects are observed on both the sapphire and SiC substrated devices with the output conductance having a negative slope at the higher dc power dissipation. All results given are probed devices without packaging and minimal thermal management.

6.5.1.1 Device on Sapphire Substrates

Transistors fabricated on sapphire substrates are thermally limited and not limited by breakdown voltages. As more elaborate heat sinking and thermal management are developed, higher operating voltages and output

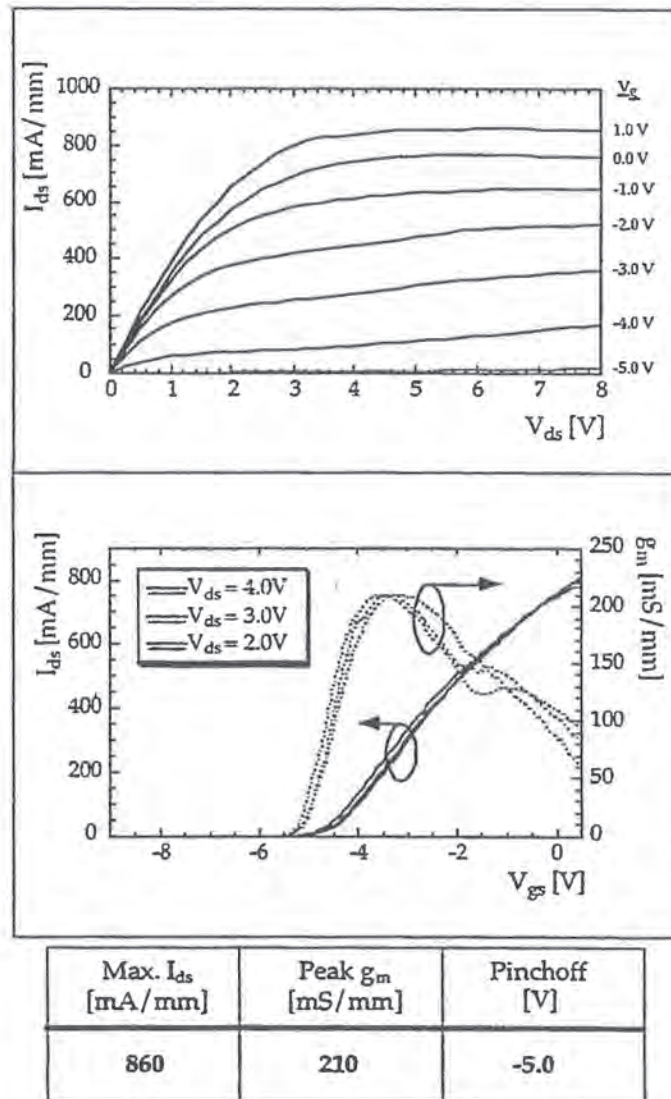


Figure 6.12 Static characteristics for AlGaIn/GaN HEMT on sapphire substrates. Gate length is $0.15 \mu\text{m}$.

powers rivaling SiC substrates may become possible. Typical dc characteristics for an AlGa_N/Ga_N HEMT with a 0.15 μm gate length on sapphire are given in Figure 6.12. The I-V scan is limited to a drain-source voltage of 8 volts and showing an I_{dmax} of 860 mA/mm corresponding to a 6.9 W/mm power dissipation. The 3-terminal breakdown voltage was measured to be 30 volts on this material with the given gate length, well below the 13 volts applied across the device. There is slight positive output conductance observed with more negative gate voltages indicating either unintentional buffer charge or parasitic charge in the AlGa_N barrier. Since the device pinches off with adequate gate bias, the charge is most likely from the AlGa_N barrier. If the charge were deep in the Ga_N buffer and/or nucleation layer, the charge would not be accessible with reasonable gate bias. The device exhibits good pinch-off characteristics with a pinch-off voltage of -5 volts and a maximum g_m of 210 mS/mm as shown in the bottom graph in Figure 6.12.

6.5.1.2 Devices on SiC Substrates

Devices fabricated on SiC can take advantage of the improved thermal conductivity of the substrates (0.33 W/°K for sapphire and 3.3 to 4.0 W/°K for SiC). For high power applications, SiC wins out big over sapphire or even silicon (1.5 W/°K) as the preferred substrate but currently cost up to 100 times more and has significant quality issues as presented in Chapter 5.

Figure 6.13 gives dc characteristics for a HEMTs fabricated on SI-SiC substrates. This is not the best device fabricated on SiC, but has interesting characteristics on potential problems and worth discussing here. The I-V curves show an I_{dmax} of only 620 mA/mm and a soft knee characteristic indicating problems with the surface or ohmic contact. The surface between

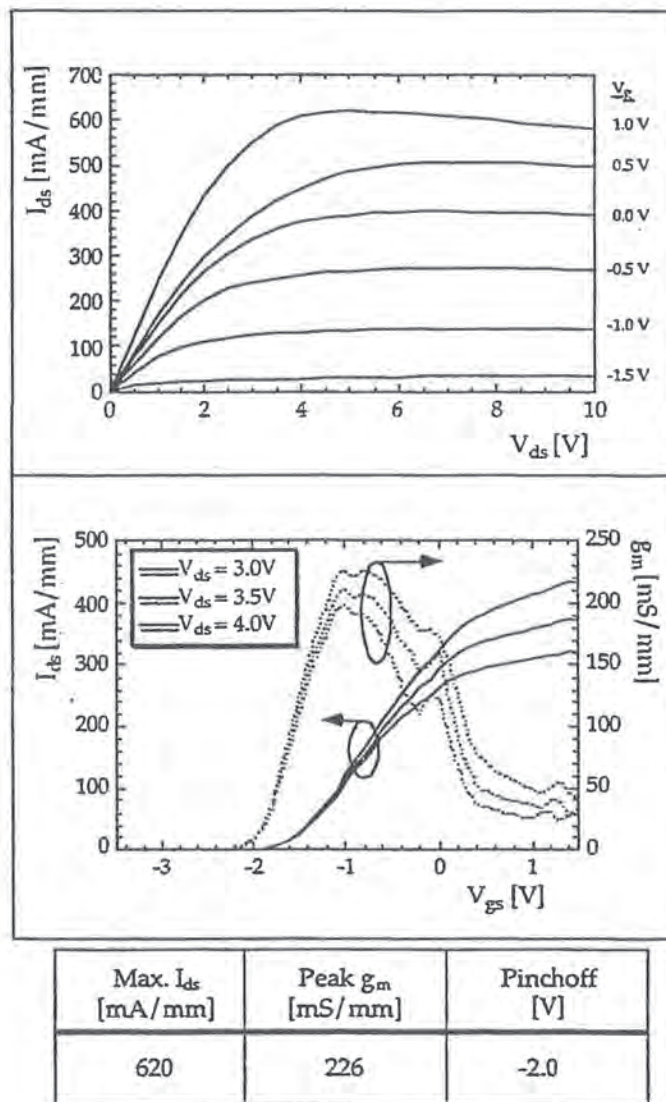


Figure 6.13 Static characteristics for AlGaIn/GaN HEMT on SiC substrates. Gate length is $0.20\ \mu\text{m}$.

the source and drain was partially etched during the RIE mesa formation process resulting in a lower pinch-off voltage of -2 volts. The thinner barrier partially depletes the 2DEG as discussed in Section 6.2 and Figure 6.3, resulting in lower current density. The transfer characteristics exhibit a maximum g_m of 226 mS/mm. The g_m and I_d greatly varies depending on the drain-source bias near the knee region. As expected from the I-V curves and is another indication that the knee is collapsing which contribute to RF-to-dc dispersion and limit large signal output powers.

6.5.2 RF Test Results

Power performance of HEMTs are usually characterized in terms of the maximum output power (P_{out}), associated gain (G_a) and maximum power added efficiency (PAE). For class A operation along the ideal load line, maximum output power predictions are given by equation 6.15

$$P_{out} = \frac{1}{8} (V_{bkgd} - V_{po} - V_{knee}) (I_{dmax} - I_{dmin}) \quad 6.15$$

where, V_{bkgd} is the gate-drain breakdown voltage, V_{po} is the pinch-off voltage, is the V_{knee} knee voltage, I_{dmax} is the maximum drain current and I_{dmin} is the minimum drain current limited by gate-drain or source-drain breakdown.

The PAE is related to the associated gain of the device and the dc power dissipated. Under class A operation, the PAE can be estimated from:

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} = \frac{P_{out} \left(1 - \frac{1}{G_a}\right)}{P_{dc}} \quad 6.16$$

where, P_{in} is the RF input power and P_{dc} is the input dc power given by :

$$P_{dc} = \frac{1}{4} (V_{bkgd} - V_{po} - V_{knee}) (I_{d\max} - I_{d\min}) \quad 6.17$$

Substituting equation 6.15 and 6.17 into equation 6.16 yields:

$$PAE = \frac{1 - \frac{1}{G_a}}{2} \quad 6.16$$

In the low frequency limit, $1/G_a$ approaches zero and the PAE approaches $1/2$ (50 %). For class B operation (biased at pinch-off), the PAE approaches $\pi/4$.

As a rule of thumb, the gate footprint is normally scaled to be 8 to 10 times the AlGaIn barrier thickness. The current gain cutoff frequency (f_T) response depends on the average transit velocity for GaN of 1.1×10^7 cm/s divided by $2\pi(L_g + 2t_{AlGaIn})$. For an effective gate length of $0.2 \mu\text{m}$, cutoff frequency of approximately 85 GHz is expected.

6.5.2.1 Devices on Sapphire Substrates

Small signal measurements were performed on transistors with $0.15 \mu\text{m} \times 100 \mu\text{m}$ gate geometry and $1.5 \mu\text{m}$ source-drain spacing. The current gain cutoff frequency (f_T) was measured to be ~ 49 GHz with a power gain cutoff frequency (f_{max}) of ~ 67 GHz as shown in the top plot in figure 6.14. The f_T is lower than the calculated value of 116 GHz for the given gate length.

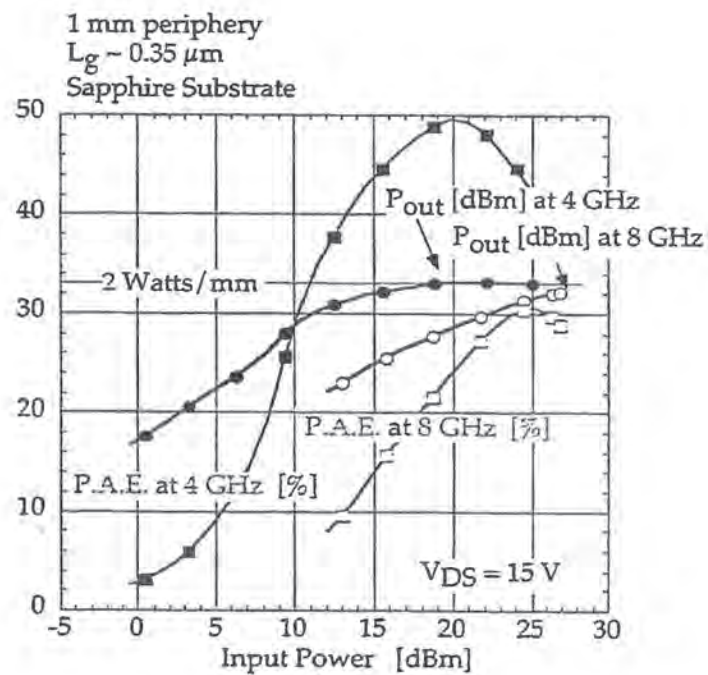
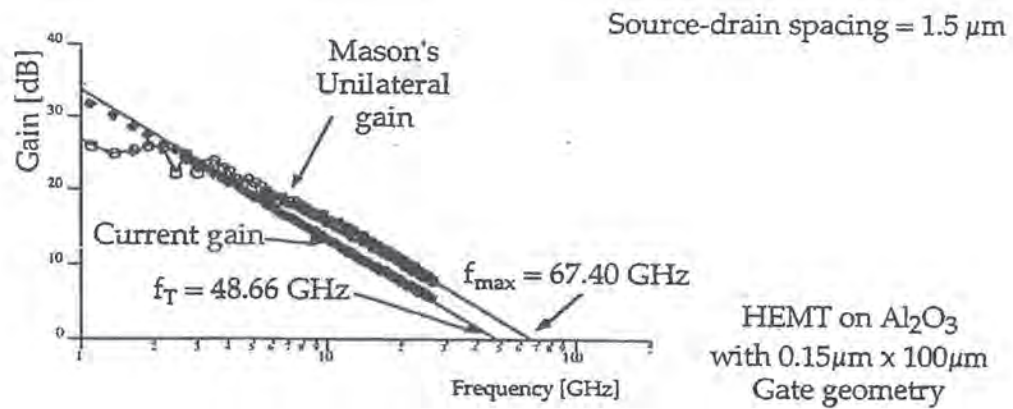


Figure 6.14 Small and large signal test results for AlGaIn/GaN HEMT on sapphire substrates.

Recalculating the saturation velocity from the results leads to a value of 0.46×10^7 cm/s instead of the 1.1×10^7 cm/s assumed. Recent studies have shown a large reduction in saturation velocity as the charge in the channel increases {}. Other factors may contribute to the lower f_T such as rough heterointerface, poor modulation efficiency, large source resistance or a large gate-to-source capacitance.

Large signal results at 4 GHz and 8 GHz are given in the bottom plot in Figure 6.14 for a device with a $0.35 \mu\text{m} \times 1 \text{ mm}$ gate geometry (larger periphery device) on sapphire. The output power saturates at the same value of 2 W/mm at both frequencies with a drain bias of 15 volts. The PAE is higher at 4 GHz as expected with higher associated gain than at 8 GHz.

6.5.2.2 Devices on SiC Substrates

Small signal measurements were performed on transistors with $0.2 \mu\text{m} \times 100 \mu\text{m}$ gate geometry and $1.5 \mu\text{m}$ source-drain spacing. The current gain cutoff frequency (f_T) was measured to be ~ 28 GHz with a power gain cutoff frequency (f_{max}) of ~ 37 GHz. These values are extremely low and indicate that there are RF losses either in the buffer layer and/or the SI-SiC substrate. A f_T/f_{max} ratio should be near 2 if there is negligible RF loss in the buffer and/or substrate.

Large signal results at 4 GHz and 8 GHz are given in the bottom plot in Figure 6.15 for a device with $0.35 \mu\text{m} \times 0.8 \text{ mm}$ gate geometry. The output power saturates at the same value at both frequencies (as in the sapphire case) of 2.8 W/mm. The devices are electrically limited due to breakdown issues rather than thermal issues as evident that the PAE has not peaked.

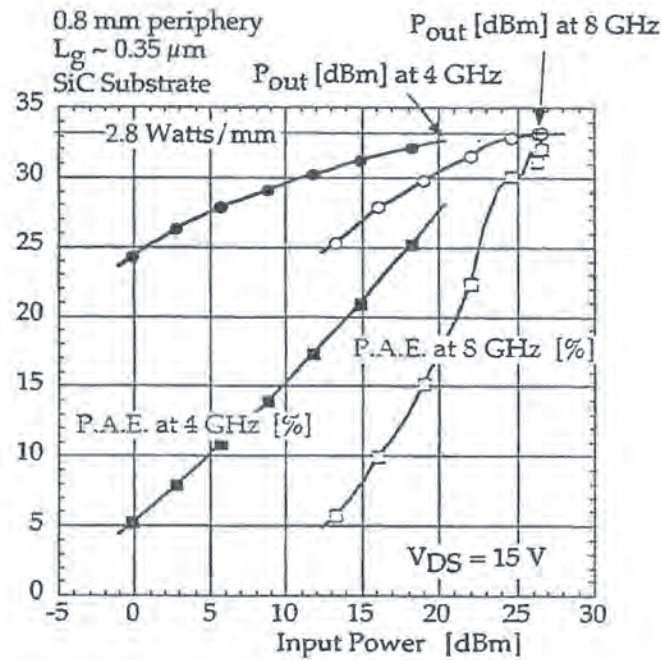
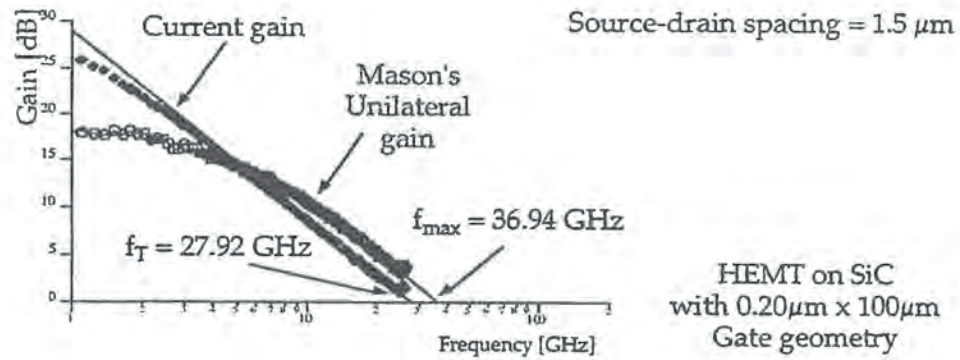


Figure 6.15 Small and large signal test results for AlGaIn/GaN HEMT on SiC substrates.

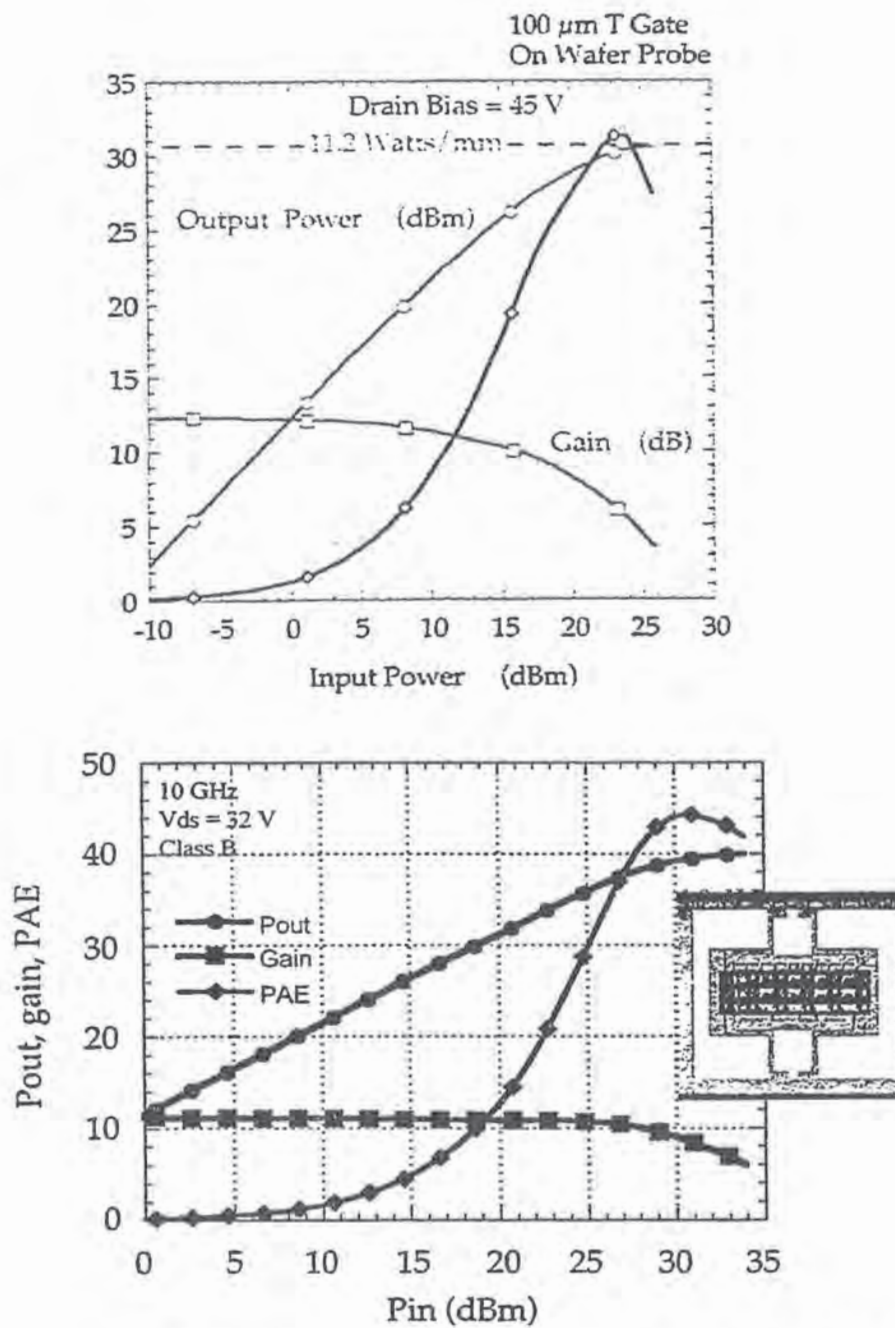


Figure 6.16 Power sweeps of optimized AlGaIn/GaN heterostructures on SiC substrates.

With improvements in materials and device fabrication techniques, higher breakdown voltages and current densities are achievable resulting in higher output power densities. Processed devices from material grown in this work produced output density as high as 11.2 W/mm at a drain bias of 45 volts as shown in the top plot in Figure 6.16 (run III555). Same material processed into a larger periphery device with a $0.35\text{ }\mu\text{m} \times 1.5\text{ mm}$ gate geometry, with ten $150\text{ }\mu\text{m}$ fingers at a $50\text{ }\mu\text{m}$ pitch produced 6.6 W/mm and a total output power of 10 Watts from a single device operating at 10 GHz. The power sweep for this device is shown in the bottom plot in Figure 6.16 at a drain bias of 32 volts. The inset is a top side image of the fabricated device.

6.6 Summary

High power transistors were fabricated out of AlGaN/GaN heterostructures where polarization bound charge at the heterostructures induces a large 2DEG density. Calculations are given for the spontaneous and piezoelectric contributions to the bound charge as well as the predicted electron concentration required to compensate the bound charge with and without surface depletion affects. AlGaN barriers with approximately 30 % Al on top of atomically flat GaN required optimization for 2-D growth that produced device quality films that proved reliable over time. Compositional and thickness control had to be understood and monitored to provide large areas for device and circuit fabrication. The V/III ratio proved to be the most important AlGaN growth parameter for compositional and crystalline uniformity throughout the film. A comparison between material reliability for 3-D and 2-D AlGaN growth was presented that indicated that 3-D growth initially yields good electron mobility but proved unreliable of storage time.

This degradation was not operational stress or accelerated life testing; it was the change in the AlGaIn barrier over storage time in regular room ambient. Static and RF test results are presented on both sapphire and SiC substrates. On SiC substrates, maximum output power density of 11.2 W/mm was measured on small periphery devices and 6.6 W/mm on 1.5 mm wide devices (10 Watts total power) at 10 GHz

Chapter 6 References

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CHAPTER 7

FUTURE WORK

7.1 Introduction

The buffer layers in both the GaAs and GaN material systems are crucial regions of the HEMT device and can significantly effect the dc and RF performance. Significant research was focused on growing highly resistive buffer structures and additional band gap engineering can be done in both material systems to further confine the electrons to the channel. Of course the active regions of the devices (namely the heterostructures and barrier layers) are just as important and produce the 2DEG used for conduction along the channel. In the GaAs system, the use of GaInAs for the channel, with a strained GaInP barrier, increased ΔE_c and allows for a larger 2DEG density, compared to latticed matched GaInP/GaAs heterostructures. Doping the supply layer with Tellurium or improvements in the multiple delta doping schemes employed can further increase the 2DEG density. Undoped AlGaIn barriers were placed on top of highly resistive GaN buffers inducing a large 2DEG density from spontaneous and piezoelectric polarization effects. Although donors are not required in the barrier, placing a doped supply layer may screen the 2DEG from the surface and reduce dc to RF dispersion. Surface termination and different cool down conditions may help protect the AlGaIn surface and reduce or eliminate dispersion and improve performance and reliability. Each of these areas will briefly be discussed in the following sections and where possible, ideas for solutions will be presented.

7.2 GaAs Material System

GaAs and GaInP buffer layers, low temperature GaInP crystal quality and delta doping of the supply layer are areas identified that can be improved to enhance the device performance. Each of these areas is discussed below with possible solutions.

7.2.1 GaAs Buffer Layers

The two-temperature composite GaAs buffer structure developed in this work produced highly resistive buffers, but the lower temperature (550° C) GaAs did not produce atomically flat growth fronts. This slight roughening occurs in the channel region right up to the heterostructure or the 72 Å GaInAs channel and can produce scattering centers reducing electron saturation velocity. Work needs to be done on defining growth conditions that will yield atomically flat GaAs surfaces at lower temperatures required for disordered GaInP, or a growth stop needs to be inserted during a temperature change from the 635° C to the 550° C. Several runs were attempted with GaInAs channels with a 10 Å GaAs smoothing layer before the GaInP spacer layer. This smoothing layer was placed on top of the surfaces represented in Figure 3.7 and did not change the surface morphology or the transport properties of the 2DEG.

7.2.2 GaInP Buffer Layers

To further confine the 2DEG to the channel region, a backside barrier can be added to the buffer structure. A GaInP layer can be inserted prior to the 200 Å to 500 Å GaAs channel. The C-band calculation of the conduction band of this type of structure is given in figure 7.1. This structure has a strained 100 Å $\text{Ga}_{0.69}\text{In}_{0.31}\text{As}$ channel and a strained $\text{Ga}_{0.65}\text{In}_{0.35}\text{P}$ barrier with a

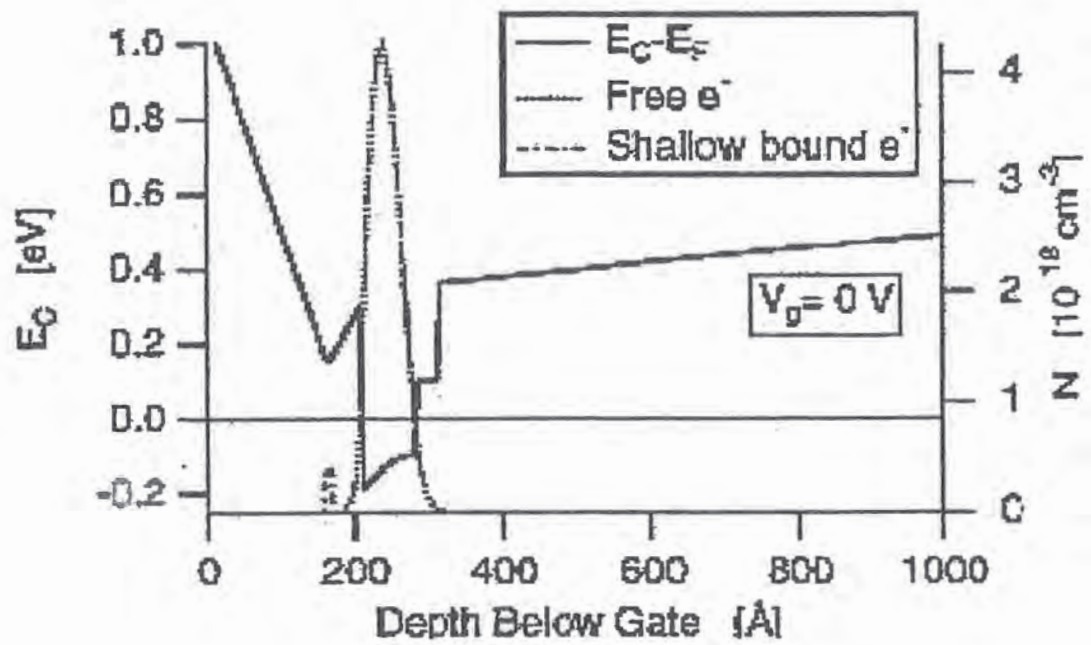


Figure 7.1 Conduction band profile for a GaInP buffer layer.

lattice matched GaInP buffer. Estimated 2DEG density for this structure is $2.51 \times 10^{12} \text{ cm}^{-2}$. Difficulties growing this structure pertain to the quality of the disordered GaInP and the additional Phosphide to Arsenide transition in the buffer layer very near the channel region.

7.2.3 GaInP Quality

As with the lower temperature GaAs, the GaInP grown at 550°C was rough and did not exhibit atomic steps. A large range of V/III ratios were attempted to improve the crystal quality, but none produce atomic steps. Other groups [] have produced disordered GaInP at the lower growth temperatures that were atomically flat. Other growth parameters such as cell pressure need to be explored to improve the GaInP used for the barrier layers.

7.2.4 Delta Doping Supply Layer

To increase the number of electrons available to form the 2DEG, Tellurium (Te) can be used as the donor species supplied by Diethyltellurium (DET). Being a group VI element, 2 electrons will be available from each donor atom. One run (II9020) was done with a single delta doped Te supply layer. The charge increased from $\sim 2.5 \times 10^{12} \text{ cm}^{-2}$ to $6.4 \times 10^{12} \text{ cm}^{-2}$ and room temperature electron mobility decreased to $1650 \text{ cm}^2 \text{ V}^{-1}\text{s}^{-1}$ from Hall measurements. The reduction in mobility indicates that the extra charge is either in additional sub-bands in the QW and/or as parasitic charge in the lower mobility material barrier.

7.3 GaN Material System

Much work and research is still required for the commercialization of GaN-based electronics. The largest barrier to entry into commercial sockets is reliability of GaN high power transistors. Before extensive reliability studies

are undertaken, the epitaxial structure and device fabrication technology requires improvements to make the devices more stable for meaningful performance and lifetime studies. Defects generated from the nucleation layer between the mismatched substrate and epitaxial layers need to be reduced or eliminated by use of novel and revolutionary nucleation schemes or the use of GaN substrates as they become available. Trapping effects in the nucleation and buffer layer need to be further investigated to increase breakdown voltage and RF output power. The surfaces of the devices are extremely sensitive and influence the dc and RF performance. Surface passivation and/or novel surface termination within the epitaxial growth could reduce or eliminate the dc-to-RF dispersion observed in the devices.

7.3.1 Nucleation Layer and Lowering Defects in GaN

Use of binary (AlN, InN and GaN), ternary (AlGaIn, InGaIn) and quaternary (AlInGaIn) nucleation layers, as well as composite nucleation schemes (a combination of different layers) could be used to accommodate the mismatch between the epitaxy and available substrates. Threading dislocation densities are established at the epitaxy/substrate transition region, insertion of novel materials and growth conditions can reduce these dislocations without the use of lateral overgrowth methods. The nucleation layer is also a critical region to accommodate the mismatch and strain from the substrate to achieve crack-free GaN films on SiC while maintaining crystal registration to the substrate. Nucleation strategies should be aimed to make growth less sensitive to substrate surface and/or crystal quality.

7.3.2 Trapping in the GaN Buffer

Trapping effects in the GaN buffer layer need to be further understood. When “as grown” material is unloaded from the reaction cell, C-V

measurements are very noisy and yield meaningless data. The samples have to sit in room atmosphere for hours before the C-V scans are well behaved. The semiconductor has to stabilize over time, either from oxidation of the surface or filling traps in the crystal itself. To try to determine if the surface was responsible, the samples were rinsed in DI water and methanol and still the C-V measurements were erratic. Every once in a while, a sample will yield good C-V data right out of the reactor. This was the exception rather than the rule. No correlation between buffer charge, unintentional charge in the barrier or device test results have been correlated to this phenomenon. It may or may not be an important signature of trapping effects either in the GaN buffer, AlGa_N barrier or at the surface.

Another effect that was discovered was that the charge measured in the 2DEG increases and the electron mobility decreases when a Hall sample is illuminated with a UV source (Hg-Ar lamp, 10 Wcm⁻² @ 253.7 nm). The Hall sample presented in Figure 7.2 is a HEMT structure on a SiC substrate. The mobility decreases from 1160 cm²V⁻¹s⁻¹ to 990 cm²V⁻¹s⁻¹ and the sheet charge increased from 1.4×10^{12} cm⁻² to 1.9×10^{12} cm⁻². After 15 minutes following the illumination, the mobility increases to 1060 cm²V⁻¹s⁻¹ and the sheet charge decreases to 1.74×10^{12} cm⁻². After 2650 minutes (44.2 hours) the mobility and sheet charge still do not recover! The mobility is at 1100 cm²V⁻¹s⁻¹ and the sheet charge is at 1.6×10^{12} cm⁻². Whatever trapping effects are activated (emptied) by the UV illumination (well above band gap for GaN and Al_{0.30}Ga_{0.70}N) have a long time constant. It should be noted that the $\mu \cdot n_s$ product (thus the channel resistivity) remains constant at 360 Ω /sq as shown

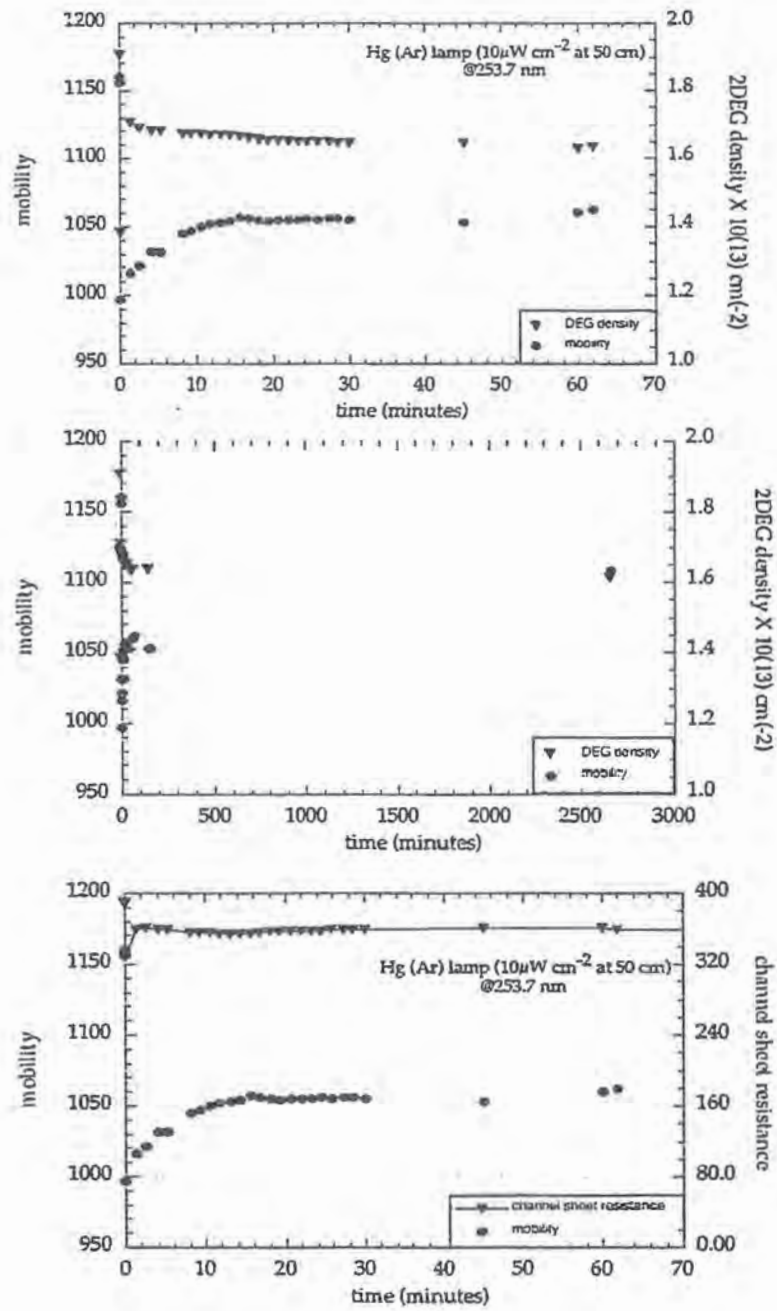


Figure 7.2 Hall measurements with and without UV illumination.

in the bottom graph of Figure 7.2. Samples investigated on sapphire substrates exhibited the same phenomena at the onset, but fully recovered after ~ 15 minutes. Although this effect is not further investigated in the scope of this work, it is a concern since the photolithography used during device fabrication utilizes UV sources for mask exposure and resist patterning.

7.3.3 AlGaN Quality

As discussed in Section 6.3.1, the AlGaN barrier layer grows better at a reduced V/III ratio compared to the GaN layers. Further studies are required to close the openings observed in AFM images of the terminated surface. Cool down cycle might adversely affect the top surface in which Hydrogen etching (most likely from the decomposition of the ammonia) of defects could damage the AlGaN crystal. A GaN or AlN cap or cooling in nitrogen instead of ammonia might reduce or eliminate such damage and minimize the defects at the surface

7.3.4 Novel *in-situ* Surface Termination

Feedback from device processing and testing revealed that gate leakage contributed to low breakdown voltages on the transistors. To reduce gate leakage, a thin GaN cap layer (to enlarge the thickness of the barrier for reduced tunneling current) was added to the structure. The conduction band profile of HEMT structures with and without a GaN cap is shown at the top of Figure 7.3. The enhanced barrier height and thickness increases the flat-band voltage to 4.5 volts, in good agreement with conductance measurements shown at the bottom of Figure 7.3. The third scan in the conductance graph is from a structure that had unintentional charge in the barrier from too high a

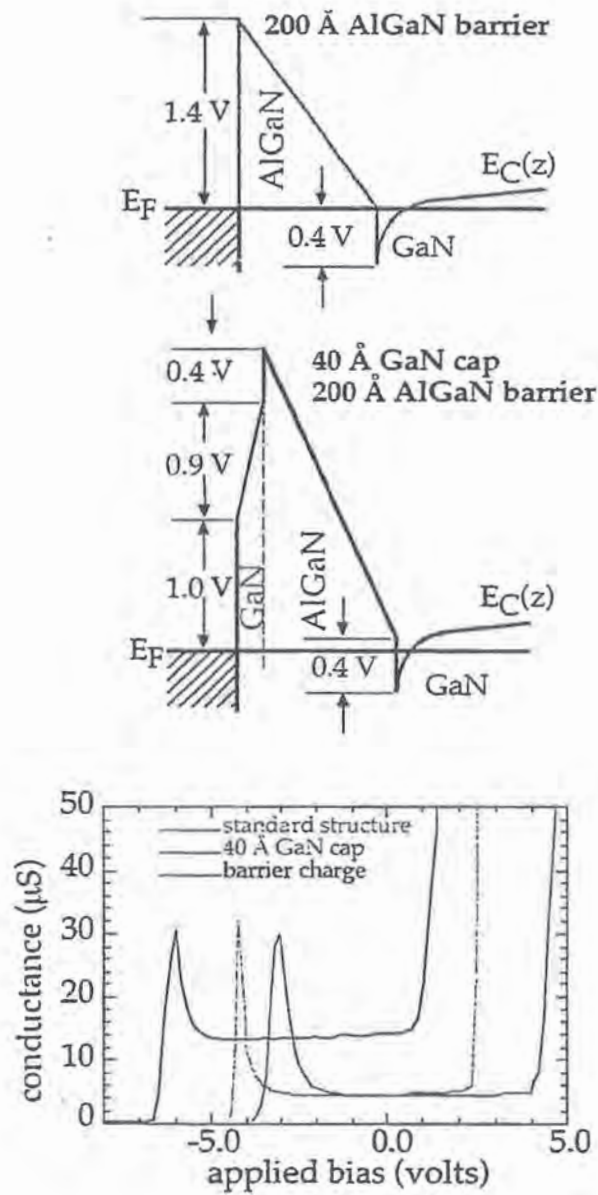


Figure 7.3 Conduction band profile with and without a GaN cap layer. Bottom graph is the conductance measured by C-V.

V/III ratio. Devices fabricated from this material showed very high gate leakage. A correlation between forward bias conductance, gate leakage and device performance needs to be performed.

The crystalline quality of the terminated AlGa_N barrier is an important parameter for device performance and reliability. The combination of threading dislocations propagating to the surface, along with surface traps associated with termination of the semiconductor make processed transistors very sensitive to surface effects. Two mechanisms have been identified that partially deplete the 2DEG during RF drive causing RF-to-dc dispersion. One mechanism is related to charging of the dislocations that extend through the channel. This results in depletion of the 2DEG around the dislocation lines. The second effect is trapping of electrons at the surface on the drain side of the gate. These traps charge up and are too slow to respond to the RF input on the gate. This produces a "virtual gate " next to the physical gate that depletes the 2DEG producing a highly resistive region in the channel. To reduce or eliminate these effects, the surface needs to be taken care of. Surface passivation neutralizes the surface traps and blocks the injection of electrons from the gate into the surface states. Several passivation materials have been investigated including Si₃N₄, SiO₂, and polyamide. A high temperature pyrolytic deposition of Si₃N₄ can be deposited *in-situ* on the epitaxial structure during the cool down cycle by flowing silane and ammonia at 500° C to 800° C. Other surface termination schemes can involve investigation of an epitaxial GaN cap layer or an AlN cap for a wet etching recessed gate process as well as surface passivation. All of these cap layers can be grown in the GaN reaction cell after the AlGa_N/GaN transistor structure is completed, eliminating any chance of atmospheric contamination

of the AlGa_N surface. The AlN cap can be very thin (~ 25 – 50 Å), which is thin enough to fabricate a metal-insulator-semiconductor field effect transistor (MISFET). Thicker layers AlN layers can be wet chemically etched with KOH, allowing for a recessed gate technology. Termination of the surface with a thin GaN (30 – 50 Å) layer enhances the Schottky barrier height, reduces gate leakage current, and electric fields under the gate. The most promising surface termination is growing a silicon nitride layer at 500° C to 800° C during the cool down cycle. The pyrolytic silicon nitride grown at the appropriate temperature and conditions can be wet chemically etched with HF providing an effective recessed gate technology or an enhancement mode device.

7.3.5 Decrease Source Resistance

Several groups are investigating the effects of space charge limited current in the GaN buffer layer (including the channel region), but no conclusive evidence as been shown that relates it as a limiting factor in these devices under RF drive. This effect is “2nd order” compared to other challenges associated with epitaxial growth and device fabrication. However, material quality and fabrication processes have dramatically improved over the past several years making issues such as space charge limited current increasingly important. Device layout as well as doped and composite channels may reduce any space charge effects that modulated the source resistance during RF drive.

7.3.6 Increase Frequency Response

At the high 2DEG densities present at the heterostructure, interface roughness is the dominant electron scattering mechanism at room temperature. To increase the electron velocity (mobility) the AlGa_N/GaN

interface roughness must be minimized. This can be accomplished by; 1) reducing defects in the crystal (nucleation layer optimization), 2) increasing the GaN buffer layer thickness, 3) implementing growth stops near the heterostructures, or a combination of these process improvements.

Appendix A
GaAs Growth Records

RUN #	Date	Description	Results
II743	12/1/95	GaInP/GaAs, 530°C, for lattice matching, 0.2 rev.sec rotation speed	44.7% In, slight cross hatching, 0.54μm/hr,
II744	12/8/95	GaInP/GaAs, 530°C, for lattice matching, 0.2 rev.sec rotation speed, after bake	47.7% In, 0.54μm/hr, RT PL 1.9ev
II745	12/12/96	GaInP/GaAs, 530°C, for lattice matching, 0.1 rev.sec rotation speed	50.1% In, 0.56μm/hr
II748	12/30/95	GaInP/GaAs, 530°C, for lattice matching, 0.1 rev.sec rotation speed	41.2% In, 0.61μm/hr
II749	1/5/96	GaInP/GaAs, 530°C, for lattice matching, 0.1 rev.sec rotation speed	46.1% In, 0.54μm/hr
II750	1/6/96	GaInP/GaAs, 530°C, for lattice matching, 0.1 rev.sec rotation speed	46.5% In, 0.55μm/hr
II755	1/15/96	GaInP/GaAs, 530°C, for lattice matching, 0.1 rev.sec rotation speed	51.0% In
II757	1/17/96	GaInP/GaAs, 530°C, for lattice matching, 0.1 rev.sec rotation speed	First run after TMI bubbler mistake, terrible morphology, In rich
II758	1/18/96	GaInP/GaAs, 530°C, for lattice matching, after cell bake	terrible morphology, In rich
II759	1/19/96	GaAs buffer layer, 530°C, TMI line closed	Good surface morphology, 0.2μm/hr, AFM rough
II760	1/20/96	GaInP/GaAs, 530°C, for lattice matching	terrible morphology, In rich
II761	1/22/96	GaAs buffer layer, 530°C, TMI line opened to cell	Good surface morphology, 0.2μm/hr, AFM rough

RUN #	Date	Description	Results
II762	1/24/96	GaInP/GaAs, 530°C, for lattice matching	terrible morphology, In rich
II763	1/26/96	GaInP/GaAs, 530°C, for lattice matching, first run with new TEG bubbler	terrible morphology, In rich
II764	1/26/96	GaInP/GaAs, 530°C, for lattice matching	53.3% In, crossed-hatched, 1.27 μ m/hr, higher growth rate
II765	1/30/96	GaInP/GaAs, 530°C, for lattice matching	45.2% In, crossed-hatched.
II767	2/2/96	GaInP/GaAs, 0.2 rev/sec rotation speed, 530°C	48.0% In, good morphology, 1.25 μ m/hr, higher growth rate, poor RT PL
II768	2/2/96	GaInP/GaAs, 0.1 rev/sec rotation speed, 530°C	48.0% In, good morphology, 1.26 μ m/hr, higher growth rate, 0.1 rev/sec
II769	2/5/96	GaInP/GaAs, 0.3 rev/sec rotation speed, 530°C	48.2% In, good morphology, 1.27 μ m/hr, higher growth rate, 0.3 rev/sec
II770	2/6/96	GaInP/GaAs, 530°C	60.0% In, crossed-hatched, 0.91 μ m/hr, tried to reduce growth rate while keeping lattice match
II781	2/26/96	GaInP/GaAs, 530°C, 0.4 rev/sec rotation speed	48.0% In, 1.32 μ m/hr, higher growth rate, 0.4 rev/sec
II782	2/28/96	GaInP/GaAs, 530°C, 0.05 rev/sec rotation speed	43.7% In, 1.4 μ m/hr, higher growth rate, 0.05 rev/sec, crossed-hatched with numerous defects
II783	3/1/96	GaInP/GaAs, 530°C	37.8% In, 0.52 μ m/hr
II784	3/2/96	GaInP/GaAs, 530°C	40.6% In, 0.57 μ m/hr

RUN #	Date	Description	Results
II785	3/5/96	GaInP/GaAs, 530°C	47.0% In, 0.43 μ m/hr
II786	3/6/96	GaInP/GaAs, 530°C	47.2% In, 0.48 μ m/hr, RT μ =2500, 77°K μ =4300
II787	3/7/96	GaInP/GaAs, 0.2 rev/sec rotation speed, 530°C	50.8% In, 0.50 μ m/hr
II788	3/8/96	GaInP/GaAs, 0.4 rev/sec rotation speed, 530°C	47.5% In, 0.45 μ m/hr
II789	3/8/96	GaInP/GaAs, 0.1 rev/sec rotation speed, 530°C	47.2% In, 0.49 μ m/hr RT μ =2000 CC=2E16
II817	4/3/96	GaInP/GaAs, increased H ₂ purge from 6.0 sec to 90 sec for AsH ₃ to PH ₃ interchange	29.9% In, crossed-hatched
II818	4/4/96	GaInP bulk, 530°C	49.1% In, 0.45 μ m/hr
II819	4/4/96	GaInP bulk terminated with GaP (20Å), 530°C	49.3% In, oval defects on surface, alot of AFM data
II820	4/5/96	GaInP bulk terminated with GaAsP (20Å), 530°C	49.4% In, alot of AFM data
II831	4/18/96	530°C test structure, 1.0 min delta doping exposure time, 95Å spacer, thin buffer	RT μ =2000, LT μ = 1200
II832	4/18/96	530°C, GaInP:Si calibration layer, 5 min buffer (50% Gas1 MFC)	44.7% In, oval defects on surface, 0.47 μ m/hr, CC 2.3E17, RT μ =2000, LT μ =2100
II833	4/23/96	530°C, GaInP:Si calibration layer, 5 min buffer (75% Gas1 MFC)	52.9% In, fewer oval defects, 0.54 μ m/hr, CC=3.8E17, RT μ =820, LT μ =990

RUN #	Date	Description	Results
II834	4/23/96	530°C, GaInP:Si calibration layer, 5 min buffer (25% Gas1 MFC)	51.5% In, no oval defects, 0.59 μ m/hr, CC=7.3E17, RT μ =1475, LT μ =3250
II835	4/24/96	530°C, GaInP:Si calibration layer, 5 min buffer (100% Gas1 MFC)	48.2% In, few oval defects on surface, 0.62 μ m/hr, CC=2.9E17, RT μ =950, LT μ =1800
II836	4/24/96	530°C test structure, 1.0 min delta doping exposure time, 95Å spacer, thick buffer	RT (μ =3300, SD=1.4E12), LT (μ =18800, SD=6.5E11)
II837	4/26/96	530°C test structure, 0.5 min delta doping exposure time, 95Å spacer	RT (μ =2800, SD=1.64E11), LT (μ =9400, SD=1.26E11)
II838	4/27/96	530°C test structure, 0.75 min delta doping exposure time, 95Å spacer	No conduction for Hall measurements????
II839	4/28/96	530°C test structure, 0.75 min delta doping exposure time, 95Å spacer	RT (μ =3000, SD=2.0E11), LT (μ =4400, SD=2.0E11)
II840	4/30/96	530°C test structure, 0.75 min delta doping exposure time, 95Å spacer, after bake	RT (μ =3400, SD=3.8E11), LT (μ =13600, SD=3.6E11)
II841	4/30/96	530°C test structure, 1min delta doping exposure time, 95Å spacer	RT (μ =2600, SD=2.36E11), LT (μ =2300, SD=3.3E11)
II842	5/1/96	530°C test structure, 1min delta doping exposure time, 47Å spacer	RT (μ =3600, SD=2.85E11), LT (μ =13500, SD=3.1E11)
II843	5/2/96	530°C test structure, 2.0 min delta doped exposure time	RT (μ =3500, SD=1.15E11), LT (μ =14700, SD=1.1E11)
II844	5/3/96	550°C test structure, 2.0 min delta doped exposure time	RT (μ =4097, SD=3.84E11), LT (μ =13100, SD=8.9E11)
II845	5/6/96	GaInP:Si calibration layer (530°C)	48.2% In, RT μ =990, CC=2.65E17, LT μ =13000 ??? NOTE LT μ , a 2DEG between GaAs and GaInP

RUN #	Date	Description	Results
II846	5/7/96	570°C test structure, 2.0 min delta doped exposure time	RT ($\mu=4600$, SD=5.4E11), LT ($\mu=16000$, SD=5.9E11)
II847	5/8/96	590°C test structure, 2.0 min delta doped exposure time	RT ($\mu=3100$, SD=1.2E12), LT ($\mu=12500$, SD=7.3E11)
II848	5/9/96	AsH3 to PH3 90 sec H2 purge, 2.0 min delta doped test structure	RT ($\mu=3400$, SD=2.8E11), LT ($\mu=13000$, SD=5.3E11)
II849	5/9/96	AsH3 to PH3 6 sec H2 purge, 2.0 min delta doped test structure	RT ($\mu=3200$, SD=3.4E11), LT ($\mu=13000$, SD=4.5E11)
II850	5/10/96	AsH3 to PH3 45 sec H2 purge, 2.0 min delta doped test structure	RT ($\mu=4000$, SD=3.4E11), LT ($\mu=15000$, SD=3.7E11)
II891	7/4/96	GaInP:Si calibration layer with new silane tank	48.9% In, 0.60 μ m/hr, RT $\mu=1000$, CC=6.6E17
II892	7/6/96	GaInP/GaAsP SL structure, 530°C	Approx 2.5-3% P in GaAsP well, 68Å period
II893	7/8/96	GaInP/GaAsP SL structure, 530°C	Approx 11% P in GaAsP well, 66Å period, good X-ray
II894	7/9/96	GaInP/GaAsP SL structure, 530°C	Approx 5% P in GaAsP well, 69Å period
II895	7/9/96	GaInP/GaAsP SL structure, 530°C	Approx 7-8% P in GaAsP well, 69Å period
II896	7/10/96	3 delta doping layers, 2.0, 1.0, 0.5 min exposure times	48.5% In, (2500Å, 3000Å, 3600Å) 2250Å, 2850Å, 3500Å
II897	7/11/96	120 sec delta doping exposure time on test structure	RT ($\mu=4200$, SD=1.37E12)

RUN #	Date	Description	Results
II898	7/12/96	60 sec delta doping exposure time on test structure	RT (μ =4700, SD=4.3E11), LT (μ =15400, SD=4.3E11)
II899	7/13/96	300 sec delta doping exposure time on test structure	RT (μ =5500, SD=9.2E11), LT (μ =21800, SD=4.2E11)
II900	7/16/96	30 sec delta doping exposure time on test structure	RT (μ =5900, SD=6.2E11), LT (μ =18300, SD=6.3E11)
II901	7/17/96	GaInAs calibration run, (30%In), 550°C	36.4% In, 1.12 μ m/hr
II902	7/19/96	GaInAs calibration run, (30%In), 550°C	31.2% In
II903	7/22/96	GaInP:Si doping calibration, 550°C (75% Gas1 MCF) Thick buffer	48.2% In, RT (μ =1300, CC=5E17), CV shows CC=1E18, can't deplete to buffer
II904	7/23/96	GaAs:Si doping calibration, 550°C	
II905	7/23/96	1 delta doped layer	Substrate/Buffer charge mid 10(17), RT (μ =5031, SD=1.1E12), LT (μ =15300, SD=8.6E11)
II906	7/24/96	1 delta doped layer, no anneal	Substrate/Buffer charge low 10(17), RT (μ =5090, SD=8.6E11), LT (μ =19000, SD=5.4E11)
II907	7/29/96	1 delta doped layer, different wafer preps, after cell bake	Substrate/Buffer charge mid 10(17), RT (μ =5690, SD=1.27E11), LT n/a
II908	7/31/96	1 delta doped layer, different wafer preps	RT (μ =6700, SD=3.4E11), LT (μ =24700, SD=4.2E11)
II909	8/2/96	1 delta doped layer, first 2.0min dopant exposure time	RT (μ =5560, SD=3.4E11)

RUN #	Date	Description	Results
II910	8/3/96	1 delta doped layers with 47Å spacer QW GaAs with GaInP buffer	2DEG at GaInP/GaAs buffer interface. RT (μ =5850, SD=8.0E11)
II911	8/7/96	1 delta doped layers with 47Å spacer (pseudomorphic channel only)	RT (μ =5720, SD=8.28E11)
II912	8/7/96	1 delta doped layers with 47Å spacer (pseudomorphic barrier, spacer, channel)	RT (μ =4900, SD=2.8E11)
II913	8/8/96	2 delta doped layers with 47Å spacer (pseudomorphic barrier, spacer, channel)	RT (μ =4690, SD=7.4E11)
II914	8/9/96	4 delta doped layers with 47Å spacer (pseudomorphic barrier, spacer, channel)	RT (μ =5010, SD=1.67E12)
II915	8/12/96	6 delta doped layers with 47Å spacer (pseudomorphic barrier, spacer, channel)	RT (μ =4940, SD=2.28E12), LT (μ =14200, SD=5.12E11)
II916	8/14/96	6 delta doped layers with 24Å spacer (pseudomorphic barrier, spacer, channel)	RT (μ =3570, SD=1.83E12), LT (μ =24700, SD=2.87E11)
II917	8/15/96	6 delta doped layers with 38Å spacer (pseudomorphic barrier, spacer, channel)	RT (μ =3810, SD=9.7E11), LT (μ =29100, SD=1.77E11)
II918	8/17/96	6 delta doped layers with 59Å spacer (pseudomorphic barrier, spacer, channel)	RT (μ =5375, SD=2.167E12)
II919	8/19/96	Bulk GaInP:Si calibration layer	XX.X% In, 0.48 μ m/hr
II920	8/20/96	Single DeTe delta doped pseudomorphic HEMT structure	RT (μ =1622, SD=6.42E12), LT (μ =6964, SD=2.24E12) : With Cap layer etched off, No CV even with cap off, overload
II983	11/7/96	GaInP Calibration layer, repeat of II982	Multiple Peak on X-Ray, more In-rich than II982, TEG running out

RUN #	Date	Description	Results
II984	11/9/96	GaInP Calibration layer, new TEG bubbler	Latticed matched
II985	11/10/96	GaInP/GaAs QW samples, 90 sec H2 purge at AsH3 to PH3 interchange	LT PL
II986	11/10/96	GaInP/GaAs QW samples, 6 sec H2 purge at AsH3 to PH3 interchange	LT PL
II987	11/10/96	GaInP/GaAs QW samples, 45 sec H2 purge at AsH3 to PH3 interchange	LT PL
II988	11/12/96	HEMT Structure with 550°C buffer only 500Å thick (slow growth rate)	RT ($\mu=1200$, $SD=7.2E11$), LT ($\mu=1700$, $SD=9.3E11$), no 2DEG in CV measurements
II989	11/13/96	HEMT Structure with 550°C buffer old structure for check	RT ($\mu=4750$, $SD=9.3E11$), LT ($\mu=15900$, $SD=7.7E11$), 2DEG seen in CV measurements
II990	11/13/96	HEMT Structure with 550°C buffer only 2000Å thick (slow growth rate)	RT ($\mu=790$, $SD=8.0E11$), 2DEG seen in CV measurements
II991	11/15/96	HEMT Structure with 635°C buffer 6000Å thick/ 550°C buffer 500Å (slow growth rate)	RT ($\mu=3600$, $SD=8.4E11$), LT ($\mu=11500$, $SD=7.0E11$), 2DEG seen in CV measurements
II992	11/15/96	HEMT Structure with 635°C buffer 6000Å thick/ 550°C buffer 1000Å (slow growth rate)	RT ($\mu=3600$, $SD=7.3E11$), LT ($\mu=14800$, $SD=4.7E11$), 2DEG seen in CV measurements
II993	11/17/96	GaInAs on Compliant substrate, 550°C, 16° twist bonded	Bad surface morphology, broad X-ray signature similar to GaAs control samples
II994	11/20/96	HEMT Structure with 635°C buffer 6000Å thick/ 550°C buffer 100Å (slow growth rate)	RT ($\mu=1900$, $SD=1.1E12$), LT ($\mu=5000$, $SD=8.2E11$), CV ????

RUN #	Date	Description	Results
II995	11/20/96	PHEMT Structure with 635°C buffer 6000Å thick/ 550°C buffer 500Å 47Å spacer	RT ($\mu = 2440$, $SD = 1.2E12$), 2DEG seen in CV measurements
II996	11/22/96	HEMT Structure with 635°C buffer 6000Å thick/ 550°C buffer 500Å 56Å spacer	
II997	11/22/96	PHEMT Structure with 635°C buffer 6000Å thick/ 550°C buffer 500Å 80Å spacer	
II1015	12/19/96	GaInP:Si doping and lattice matching calibration/ 100Å GaAs cap for compliant	GaAs cap measured 100Å,
II1016	1/4/97	PHEMT Structure with 635°C buffer 6000Å thick/ 550°C buffer 500Å 47Å spacer	
II1017	1/6/97	PHEMT Structure with 635°C buffer 6000Å thick/ 550°C buffer 500Å 47Å spacer 8Δ	
II1018	1/7/97	GaAs Buffer layer 530°C on prep (5:1:1) substrates	AFM Study and SL project
II1019	1/8/97	Part of PHEMT structure/ Buffer 635/550°C, with 72Å GaInAs channel	AFM
II1020	1/10/97	GaAs Buffer plus GaInP buffer used in SL study	AFM
II1021	1/14/97	GaAs(P)/GaInP SL, repeat of II892	AFM
II1022	1/16/97	PHEMT with thick 635°C GaAs buffer to improve V_{bk}	

RUN #	Date	Description	Results
II1023	1/17/97	GaAsP bulk layer Xas=0.47, 650°C	
II1024	1/18/97	1.42 min GaInP on Si tips, Tips prep with buffered HF 10 sec.	
II1025	1/20/97	GaAsP bulk layer, Xas=0.47 500Å thick, 650°C	
II1026	1/22/97	GaAsP bulk layer, Xas=0.19, 650°C	
II1027	1/24/97	GaAs smoothing layer on top of GaInAs channel, 8Δ dopings PHEMT, repeat of II1017	
II1028	1/24/97	GaInAs PHEMT channel with 10Å GaAs smoothing layer, same as II1019	
II1029	1/25/97	PHEMT structure with 8Δ layers, 635/550 buffers	
II1030	1/27/97	GaAs buffer used in HEMTS, 635/550°C same as II1028 with out channel	
II1031	1/27/97	GaAsP bulk layer, Xas=0.47, trying for 2μm, otherwise same as II1023	
II1032	1/28/97	GaAsP Bulk layer, Xas=0.19, 100Å, 650°C	
II1033		GaAsP Bulk layer	
II1034		GaAs buffer layer, 635°C V/III=10	

RUN #	Date	Description	Results
II1035		GaAsP Bulk layer	
II1036		GaAsP Bulk layer	
II1037		GaAs buffer layer, 550/550°C	
II1038		0.75 min GaInP on Si tips, Tips prep with buffered HF 10 sec.	
II1039		Single delta-doping, tank calibration	
II1040		Single delta-doping, tank calibration	
II1041		Standard HEMT structure for calibration	RT ($\mu = 3173$, $SD = 2.56E12$),
II1042		Standard structure with 150 Å GaInP spacer	Smoked?
II1043		Standard structure with 100 Å GaInP spacer	Smoked?
II1044		Standard structure with 25 Å GaInP spacer	Smoked?
II1045		Standard structure with 120 Å GaInAs channel	Smoked?
II1046		Standard structure with 40 Å GaInAs channel	Smoked?

RUN #	Date	Description	Results
II1047		Standard structure with 2 sec H2 purge	
II1048		Standard structure with 45 sec H2 purge	
II1049		Standard structure with 100 Å GaInP spacer	
II1050		Standard structure with 25 Å GaInP spacer	
II1051		Standard structure with 120 Å GaInAs channel	
II1052		Standard structure with 40 Å GaInAs channel	
II1053		Standard structure for calibration	RT (μ =4668, SD=2.57E12),
II1054		Standard structure for calibration	
II1055		Single delta-doping 200 ppm tank calibration 2 min exposure	RT (μ =4570, SD=5.4E11),
II1056		Single delta-doping 200 ppm tank calibration 30 sec exposure	RT (μ =5090, SD=6.1E11),
II1057		Single delta-doping 200 ppm tank calibration 5 min exposure	RUN ABORTED MACHINE FAILURE
II1058		Standard structure with 75 Å GaInP spacer	

RUN #	Date	Description	Results
II1059		Standard structure with buffer layer v/iii ratio at 2.2	RT (μ =5015, SD=2.54E12),
II1060		Single delta-doping 200 ppm tank calibration 10 min exposure	RT (μ =4390, SD=1.65E12),
II1061		Single delta-doping 200 ppm tank calibration 1 min exposure	RT (μ =5150, SD=3.3E11),
II1062		Single delta-doping 200 ppm tank calibration 5 min exposure	RT (μ =5062, SD=1.22E12),
II1063		Continuous doping in supply layer	RT (μ =5314, SD=3.4E11),
II1064		Standard structure with buffer layer v/iii ratio at 1.1	RT (μ =5314, SD=1.4E12),
II1065		Standard structure with buffer layer v/iii ratio at 1.5	RT (μ =4030, SD=2.5E12),
II1066		New Silane tank 2000 ppm GaAs:Si	CC=4.62E18 cm-3
II1067		Single delta-doping 2000 ppm tank calibration 10 min exposure	RT (μ =2100, SD=2.3E12),
II1068		Single delta-doping 2000 ppm tank calibration 2 min exposure	RT (μ =2840, SD=5.5E11),
II1069		Single delta-doping 2000 ppm tank calibration 1 min exposure	
II1070		4 delta doped layers with 2000 ppm silane	RT (μ =3010, SD=3. 1E12),

Appendix B
GaN Growth Records

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RUN #	Date	Description	Results
III185	6/19/97	GaN on GaN Template	First run after machine maint.
III186	6/20/97	AlGaN Calibration	30 minute GaN, 45 minutes AlGaN
III187	6/21/97	AlGaN Calibration	30 minute GaN, 45 minutes AlGaN, Increased Al Flux
III188	6/24/97	AlGaN Calibration	30 minute GaN, 45 minutes AlGaN, New TMA bubbler, increased bubbler temperature to 17.5 C
III189	6/25/97	AlGaN Calibration	30 minute GaN, 45 minutes AlGaN
III190	6/26/97	AlGaN Calibration	30 minute GaN, 90 minutes AlGaN
III191	6/26/97	AlGaN Calibration	30 minute GaN, 90 minutes AlGaN
III192	6/27/97	AlGaN Calibration	30 minute GaN, 90 minutes AlGaN
III193	7/7/97	GaN Calibration	Changed block flows
III194	7/8/97	GaN Calibration	Increased Growth Temperature and TEG Flux
III195	7/9/97	GaN Calibration	60 minute GaN, no outer wall cooling to increase Tg
III196	7/10/97	GaN Calibration	60 minute GaN, modified heat stage for higher Tg

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RUN #	Date	Description	Results
III197	7/11/97	GaN Calibration	120 minutes GaN, higher Tg, lower growth rate
III198	7/11/97	AlGaN and GaN Calibration	30 minute GaN (1800 A), 45 minute AlGaN (3000 A)
III199	7/13/97	AlGaN Calibration	30 minute GaN, 45 minutes AlGaN, Increased Al Flux
III200	7/14/97	AlGaN Doping Calibration n-type	30 minute GaN, 45 minutes AlGaN, Increased Al Flux, added Silane
III201	7/15/97	AlGaN Doping Calibration n-type	30 minute GaN, 45 minutes AlGaN:Si, $8.5 \text{ E } 17 \text{ cm}^{-3}$
III202	7/16/97	AlGaN Doping Calibration p-type	30 minute GaN, 45 minutes AlGaN:Mg
III203	7/16/97	Two-Temperature GaN Buffer	15 minute 550 C, 60 minutes 1030 C
III204	7/17/97	AlGaN Doping Calibration p-type	30 minute GaN, 45 minutes AlGaN:Mg
III205	7/19/97	AlGaN Doping Calibration p-type	30 minute GaN, 45 minutes AlGaN:Mg
III206	7/20/97	GaN Doping Calibration n-type	GaN :Si
III207	7/20/97	GaN Doping Calibration n-type	GaN :Si, Two temperature GaN:Si layers
III208	7/21/97	Low Temperature GaN	120 minutes GaN on sapphire substrate

RUN #	Date	Description	Results
III209	7/21/97	GaN Doping Calibration n-type	GaN :Si
III210	7/22/97	Two-Temperature GaN Buffer	15 minute 400 C, 60 minutes 745 C
III211	7/23/97	GaN Doping Calibration n-type	30 minutes GaN, 90 minutes GaN:Si
III212	7/24/97	GaN Doping Calibration n-type	30 minutes GaN, 90 minutes GaN:Si
III213	7/25/97	GaN Doping Calibration n-type	30 minutes GaN, 90 minutes GaN:Si
III214	7/27/97	LED Structure	Full GaN LED with Zn:Si co-doping in active layer
III215	7/28/97	LED Structure	Full GaN LED with Zn:Si co-doping in active layer
III216	8/1/97	Co-doped GaN layer Calibration	GaN:Si:Zn 90 minutes
III217	8/2/97	Lower Portion of LED Structure	GaN:Si, AlGaN:Si, GaN:Si:Zn
III218	8/3/97	Co-doped GaN layer Calibration	GaN:Si:Zn turned down Zn from 30 % to 15 %
III219	8/4/97	Nucleation on Sapphire	Two temperature GaN nucleation with H2 clean
III220	8/4/97	Nucleation on Sapphire	Two temperature GaN nucleation lower temp on first layer

RUN #	Date	Description	Results
III221	8/5/97	Nucleation on Sapphire	Two temperature GaN nucleation with H2 clean
III222	8/5/97	Nucleation on Sapphire	Two temperature GaN nucleation with H2 clean
III223	8/11/97	Nitridation Experiment	Nitridation of Sapphire Surface at 1020 C
III224	8/12/97	Nucleation on Sapphire	Run ABORTED RF FAILURE
III225	8/13/97	Nitridation/Nucleation Experiment	Nitridation of Sapphire Surface at 1020 C, 60 sec ammonia flow
III226	8/14/97	Nitridation/Nucleation Experiment	Nitridation of Sapphire Surface at 1020 C, 3.5 minute GaN nuke
III227	8/16/97	Nitridation/Nucleation Experiment	Nitridation of Sapphire Surface at 1020 C, 0.88 minute GaN nuke
III228	8/16/97	Nucleation on Sapphire	Decreased Nucleation Temperature
III234	8/22/97	Hydrogen Clean Experiment	Clean at 1100 C to see effect on sapphire surface
III235	8/22/97	Nitridation Experiment	Stop growth right after H2 clean and Nitridation step
III236	8/22/97	Nucleation Experiment	Stop growth right after H2 clean, Nitridation and Nucleation

RUN #	Date	Description	Results
III237	8/22/97	Nucleation Experiment	Stop growth right after H2 clean, Nitridation, Nucleation and 10 minutes of GaN growth
III241	8/26/97	Two Temperature Nucleation	Varying Nucleation Time
III248	9/17/97	Two Temperature Nucleation	New TEG Bubbler
III249	9/18/97	Two Temperature Nucleation	Lower GaN Buffer Temperature
III250	9/18/97	Two Temperature Nucleation	Higher GaN Buffer Temperature
III251	9/26/97	Two Temperature Nucleation	Re-built cell
III252	9/27/97	Two Temperature Nucleation	Higher Cell Pressure (225 Torr)
III253	9/27/97	Two Temperature Nucleation	Increased GaN V/III ratio
III265	10/14/97	Two Temperature Nucleation	Increased Nucleation time from 10 minutes to 20 minutes
III266	10/16/97	Two Temperature Nucleation	Decreased block flow to improve nucleation uniformity
III267	10/17/97	Two Temperature Nucleation	Further decreased block flow to improve nucleation uniformity

RUN #	Date	Description	Results
III268	10/20/97	Two Temperature Nucleation	Run ABORTED rotation problem
III269	10/21/97	Two Temperature Nucleation	Decreased nucleation time to 10 minutes, block at 32 LPM
III270	10/22/97	Two Temperature Nucleation	Nucleation time set at 15 minutes
III271	10/23/97	Two Temperature Nucleation	Increased GaN over layer temperature
III272	10/24/97	Two Temperature Nucleation	Repeat of III271 with Hydrogen bake between runs
III274	10/27/97	Two Temperature Nucleation	Decreased heat-up time from nucleation to HT GaN
ALL RUNS NOW INCORPORATE A CLEANING BAKE BETWEEN RUNS			
III275	10/28/97	Two Temperature Nucleation	Repeat of III274 longer HT GaN layer
III276	10/30/97	GaN on Patterned Si substrates	H2 clean then 120 minutes GaN (HT)
III277	11/2/97	Two Temperature Nucleation	HCl bake of cell prior to run
III278	11/3/97	Two Temperature Nucleation	Decreased nucleation time to 5 minutes
III279	11/4/97	Two Temperature Nucleation	Decreased nucleation time to 2.5 minutes

RUN #	Date	Description	Results
III280	11/5/97	Two Temperature Nucleation	Decreased nucleation time to 1.25 minutes
III283	11/12/97	Two Temperature Nucleation	Repeat of III280 new Tc on susceptor
III284	11/12/97	Two Temperature Nucleation	Decreased nucleation time to 0.75 minutes
III285	11/13/97	Two Temperature Nucleation	Decreased nucleation time to 0.33 minutes
III287	11/17/97	Two Temperature Nucleation	Take out Nitridation step
III290	11/20/97	Two Temperature Nucleation	Decreased TEG flux in nucleation layer by factor of 4
III291	11/20/97	Two Temperature Nucleation	Decreased TEG and Ammonia by 2X
III292	11/21/97	Two Temperature Nucleation	Increased V/III ratio during HT GaN over layer
III293	11/26/97	Two Temperature Nucleation	Oscillation of ammonia line – total mess
III294	11/28/97	Two Temperature Nucleation	Rebuilt ammonia gettering melt
III295	12/1/97	Two Temperature Nucleation	Increased V/III ratio during HT GaN over layer
III296	12/8/97	Two Temperature Nucleation	Increased block ammonia flow to 100 %

RUN #	Date	Description	Results
III297	12/9/97	Two Temperature Nucleation	Changed ammonia MFC from 5K to 15 K to increase V/III ratios
III298	12/10/97	Two Temperature Nucleation	Parked susceptor, no rotation, increase growth times by 3X
III299	12/13/97	Two Temperature Nucleation	Parked susceptor, no rotation, increase growth times by 3X
III300	12/16/97	Two Temperature Nucleation	Parked suceptor, no rotation, increase HT GaN growth time
III301	12/18/97	Two Temperature Nucleation	Low temperature nitridation, new TEG, new ammonia tanks
III302	12/25/97	Two Temperature Nucleation	Repeat of III258, changed filters in lower end cap
III303	12/29/97	Two Temperature Nucleation	Increased nucleation time from 10 to 20 minutes
III304	12/31/97	High Temperature Nucleation on SiC	4 minute OM preflow prior to growth
FIRST SUCCESSFUL NUCLEATION LAYER			
III305	1/4/98	AlGaIn Calibration, New Nucleation	HT nucleation scheme, 4 minute TMA & TEG preflow
III306	1/6/98	AlGaIn Calibration, no OM preflow	NO preflow, to see if nucleation works without it
III307	1/6/98	Ammonia Preflow Experiment	Ammonia into cell 2 seconds before OM's

RUN #	Date	Description	Results
III308	1/7/98	Repeat of III 305	HT nucleation scheme, 4 minute TMA & TEG preflow
III309	1/8/98	AlGa _N Calibration, New Nucleation	HT nucleation scheme, 4 minute TMA & TEG preflow
III310	1/8/98	GaN Calibration, New Nucleation	AlGa _N Nuke graded to GaN. GaN for 270 minutes
III311	1/13/98	AlGa _N Composition Calibration	AlGa _N (3% Al)/GaN/AlGa _N (30 % Al)
III312	1/15/98	AlGa _N Calibration, no OM preflow	13 % AlGa _N no OM preflow
III313	1/18/98	AlGa _N Calibration, OM preflow	30 minutes AlGa _N at 1040 C
III314	1/19/98	FIRST HEMT STRUCTURE	2500 Å AlGa _N /2 um GaN/AlGa _N Barrier
III315	1/25/98	HEMT Structure	AlGa _N nuke/GaN buffer/AlGa _N Barrier
III316	1/29/98	HEMT Structure	Decreased Al in nucleation layer (3.4 %)
III317	1/30/98	HEMT Structure	Increase Al in nucleation layer (6.5 %)
III318	1/31/98	Repeat of III 313	AlGa _N Calibration
III319	2/1/98	HEMT Structure	Increase Al in barrier to 40 %

RUN #	Date	Description	Results
III320	2/3/98	AlGaN on Patterned Si Substrates	All at High Temperature
III326	2/10/98	AlGaN Calibration on SiC and Sapphire	30 minutes AlGaN at 1040 C
III327	2/11/99	AlGaN Calibration on Sapphire	Trying to get HT nucleation to work on sapphire
III328	2/13/98	AlGaN Calibration on SiC	30 % AlGaN
III329	2/14/98	HEMT Structure	AlGaN nuke/ GaN buffer/ AlGaN Barrier
III330	2/19/98	HEMT Structure	AlGaN nuke/ GaN buffer/ AlGaN Barrier - filter change
III331	2/21/98	HEMT Structure	AlGaN nuke/ GaN buffer/ AlGaN Barrier - thicker barrier
III332	2/23/98	HEMT Structure	AlGaN nuke/ GaN buffer/ AlGaN Barrier SiC substrates
III333	2/24/98	FIRST ELO RUN, Patterned Substrates	420 minute GaN buffer, full HEMT structure
III334	3/1/98	ELO on Patterned Substrates	Whiskers growing up from surface
III335	3/5/98	AlGaN Calibration	15 % AlGaN, rebuilt ammonia gettering melt
III336	3/6/98	HEMT Structure on Sapphire	17.5 % AlGaN nuke/ GaN buffer/ AlGaN Barrier

RUN #	Date	Description	Results
III337	3/9/98	HEMT Structure on Sapphire	17.5 % AlGaIn nucleation/GaN buffer/ AlGaIn Barrier
III338	3/13/98	AlGaIn Calibration	Thickness and composition check
III339	3/14/98	HEMT Structure on Sapphire	Reduced OM-preflow from 4 to 1 minute
III340	3/16/98	HEMT Structure on Sapphire	Reduced OM-preflow from 1 to 0.5 minute
III343	3/20/98	HEMT Structure	Reduce AlGaIn nucleation layer thickness from 1000 to 300 Å
III344	3/23/98	HEMT Structure	Reduce AlGaIn nucleation layer thickness from 300 to 150 Å
III345	3/25/98	HEMT Structure	No AlGaIn buffer layer
III346	3/26/98	ELO of AlGaIn Buffer	60 minutes AlGaIn buffer on patterned substrates
III347	3/30/98	ELO RUN, Patterned Substrates	420 minute GaN buffer, no AlGaIn barrier
III348	4/1/98	AlGaIn Calibration	Reduced rotation speed only during the AlGaIn layer
III349	4/2/98	ELO RUN, Patterned Substrates	420 minute GaN buffer, no AlGaIn barrier
III350	4/6/98	Repeat of III346, ELO	60 minutes AlGaIn buffer on patterned substrates

RUN #	Date	Description	Results
III351	4/7/98	AlGaN Calibration	Reduced rotation speed only during the AlGaN layer
III353	4/9/98	ELO RUN, Patterned Substrates	Thick GaN buffer, no AlGaN barrier
III356	4/21/98	AlGaN Barrier Calibration	Calibration on SiC substrates
III357	4/22/98	HEMT Structure	Increase Al in AlGaN barrier
III358	4/28/98	HEMT Structure	Increased GaN buffer thickness to improve 2DEG mobility
III359	4/30/98	HEMT Structure	Reduce AlGaN nucleation layer thickness from 1800 to 900 Å
III360	5/3/98	HEMT Structure	Increase AlGaN nucleation layer thickness from 1800 to 2700 Å
III361	5/5/98	HEMT Structure	Repeat of III344, on whole 2" diameter sapphire substrates
III362	5/7/98	HEMT Structure	Repeat of III361 with increased block flows for uniformity
III387	7/22/98	HEMT Structure	Standard structure, throttle valve went wide open during GaN
III388	7/24/98	HEMT Structure	Increase OM preflow time and AlGaN buffer thickness

RUN #	Date	Description	Results
III389	7/28/98	HEMT Structure	Standard structure, NEW SUSCEPTOR – 8 – 2” pockets
III390	7/29/98	HEMT Structure	Standard structure, higher growth temperature
III391	7/30/98	AlGaIn Calibration	30 minutes AlGaIn, 40 LPM block flows
III392	8/3/98	AlGaIn Calibration	30 minutes AlGaIn, 48 LPM block flows
III393	8/5/98	AlGaIn Calibration	Increased Al flux in preflow and AlGaIn layer
III394	8/6/98	HEMT Structure	Standard structure, higher block flows
III395	8/7/98	AlGaIn Calibration	New TMA bubbler, slightly higher growth temperature
III396	8/8/98	AlGaIn Calibration	30 minutes AlGaIn, 32 LPM block flows
III397	8/10/98	AlGaIn Calibration	30 minutes AlGaIn
III398	8/11/98	AlGaIn Calibration	30 minutes AlGaIn, longer hydrogen clean time (23 minutes)
III399	8/13/98	AlGaIn Calibration	30 minutes AlGaIn, increasing Al flux to get sapphire to work
III401	8/15/98	AlGaIn Calibration	30 minutes AlGaIn, new sapphire substrates

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RUN #	Date	Description	Results
III425	9/24/98	HT Nitridation Experiment	Stop run right after nitridation of sapphire surface
III426	9/25/98	HEMT Structure	Lower Al % in nucleation, reduce OM preflow to 60 seconds
III427	9/26/98	HEMT Structure	Lost ammonia gettering melt and H2 pressure during run
III428	9/30/98	HEMT Structure	Increase block flows to 48 LPM, rebuilt ammonia gettering melt
III429	10/2/98	HEMT Structure	Increased OM preflow to 4 minutes
III430	10/5/98	HEMT Structure	Decrease Al % in nucleation layers
III431	10/7/98	HEMT Structure	Increase Al % in nucleation layers
III433	10/8/98	HEMT Structure	Used lower block flow in nucleation and OM preflow (32 LPM)
III434	10/12/98	HEMT Structure	48 LPM block flows, increased growth temperature
III435	10/13/98	HEMT Structure	Low-Hi block flows and lower growth temperature
III436	10/16/98	HEMT Structure	Low-Hi block flows and lower growth temperature
III437	10/23/98	HEMT Structure	Low-Hi block flows and lower growth temperature

RUN #	Date	Description	Results
III438	10/29/98	HEMT Structure	Low-Hi block flows and lower growth temperature
III439	10/30/98	HEMT Structure	Low-Hi block flows and lower growth temperature
III440	11/1/98	HEMT Structure	Low-Hi block flows and lower growth temperature
III441	11/3/98	HEMT Structure	Low-Hi block flows and lower growth temperature
III442	11/4/98	HEMT Structure	Trying to get grey-ish OM preflow line to move up wafer
III443	11/5/98	HEMT Structure	High block flow (48 LPM)
III444	11/6/98	HEMT Structure	Decreasing Al % in OM preflow and AlGaIn nucleation
III445	11/10/98	HEMT Structure	High block flow
III446	11/12/98	HEMT Structure	Higher growth rates, lower growth temperatures
III447	11/13/98	First 8-Wafer Run, HEMT Structure	Concern about surface temperature with thermal load on susceptor
III448	11/16/98	8-Wafer Run, HEMT Structure	Concern about surface temperature with thermal load on susceptor
III449	11/18/98	8-Wafer Run, HEMT Structure	Concern about surface temperature with thermal load on susceptor

RUN #	Date	Description	Results
III450	11/19/98	8-Wafer Run, HEMT Structure	Increase AlGaIn buffer thickness
III451	11/20/98	HEMT Run on SiC	Standard Structure
III452	11/22/98	HEMT Run on SiC	Standard Structure, lower V/III ratio in barrier (1100 to 900)
III453	11/26/98	HEMT Run on SiC	Standard Structure, repeat of III451
III463	12/25/98	HEMT Run on Sapphire	Standard Structure
III464	12/30/98	HEMT Run on Sapphire	Standard Structure, reduced AlGaIn nucleation to 1 minute
III465	1/2/99	HEMT Run on Sapphire	Standard Structure
III466	1/8/99	HEMT Run on Sapphire	Standard Structure, trying to get rid of buffer charge
III467	1/13/99	HEMT Run on Sapphire	Standard Structure, new sapphire substrates
III468	2/4/99	HEMT Run on Sapphire	Reduced AlGaIn nuke thickness
III471	2/13/99	HEMT Run on Sapphire	New 3 um filters installed in lower end cap
III472	2/14/99	HEMT Run on Sapphire	Repeat of III471

RUN #	Date	Description	Results
III473	2/16/99	GaN Buffer Layer 8-Wafer Run	1 um GaN buffer structure
III474	2/18/99	HEMT Run on Sapphire	Standard structure
III475	2/24/98	HEMT Run on Sapphire 8-wafer	Standard structure, lower Al in nuke layer
III476	2/28/99	HEMT Run on Sapphire 8-wafer	8 hr GaN buffer layer (4 um thickness)
III477	3/4/99	HEMT Run on Sapphire 8-wafer	Hi-Low-Hi Temperature GaN buffer structure (increase growth rate in GaN buffer by lowering temperature)
III478	3/10/99	HEMT on SiC	Lower Al in OM preflow and AlGaN buffer
III479	3/12/99	HEMT on SiC	Higher Al in OM preflow and AlGaN buffer
III480	3/13/99	HEMT on SiC	Ran out of TEG
III481	3/24/99	HEMT with GaN Cap Layer	50 A GaN cap layer on top of AlGaN barrier
III482	3/26/99	HEMT on SiC	Repeat of III479
III483	4/1/99	HEMT on SiC	Repeat of III479
III484	4/6/99	HEMT on SiC	Repeat of III483, lower Al in preflow and V/III in barrier

RUN #	Date	Description	Results
III485	4/14/99	HEMT on SiC	Standard structure on various SI-SiC substrates
III489	4/30/99	HEMT on Silicon Wafers	No hydrogen pre-clean in reaction cell
III490	5/1/99	HEMT on Silicon Wafers	1/2 the AlN thickness
III491	5/7/99	HEMT on Silicon Wafers	Further reduce AlN thickness
III492	5/8/99	HEMT on Silicon Wafers	Al OM preflow inserted
III508	8/30/99	Standard HEMT on Sapphire	Low V/III ratio in barrier, new boule of sapphire
III509	9/2/99	Standard HEMT on Sapphire	Low V/III ratio in barrier, higher Al in nucleation
III510	9/16/99	Standard HEMT on Sapphire	Slight buffer charge, low V/III ratio in barrier, repeat of III509, new filters
III511	10/6/99	Standard HEMT on Sapphire	Low V/III ratio in barrier, lower Al in nucleation
III512	10/10/99	Standard HEMT on SiC Substrates	Standard HEMT Structure
III513	10/14/99	Standard HEMT on SiC Substrates	Increase Al in barrier, Sterlings wafer
III514	11/4/99	Standard HEMT on SiC Substrates	Polycrystalline SiC Kyrocera, repeat of III513

in social behavior be not as different as it seems to be. In fact, we can

RUN #	Date	Description	Results
			new) New boule did not work out well, bad surface morphology, older substrate worked ok.
III526	1/3/00	Standard HEMT on Sapphire	Eleventh run in thin barrier experiment, increased Al in nucleation layers 2 wafers from new boule, worked out well
III527	1/8/00	Standard HEMT on Sapphire	8-wafer run, 175 Å barrier layer target thickness
III528	1/11/00	Standard HEMT on SiC Substrates	Calibration of AlGaIn barrier thickness and composition
III529	1/13/00	Standard HEMT on SiC Substrates	Repeat of III528, 30 Å GaN cap layer
III530	1/20/00	Standard HEMT on Sapphire	Repeat of III527 with 30 Å GaN cap layer
III531	2/15/00	Standard HEMT on Sapphire	Calibration run
III532	2/16/00	Standard HEMT on SiC Substrates	Repeat of III529 with NO GaN cap
III533	2/17/00	Standard HEMT on SiC Substrates	30 Å GaN cap layer
III534	2/18/00	Standard HEMT on SiC Substrates	Increased temperature in all Al bearing layers
III535	3/1/00	Standard HEMT on Sapphire	Calibration run
III536	3/2/00	Standard HEMT on Sapphire	Calibration run

RUN #	Date	Description	Results
III537	3/6/00	Standard HEMT on Sapphire	Increase Al % in OM preflow and nucleation layers
III538	3/10/00	HEMT on Sapphire	Buried AlGaIn layer to backside confine the 2DEG
III539	3/19/00	Standard HEMT on SiC Substrates	Repeat of III529 with 30 Å GaN cap
III540	4/26/00	Standard HEMT on Sapphire	Calibration run
III541	4/30/00	Standard HEMT on SiC Substrates	Calibration run with 30 Å GaN cap
III542	5/2/00	Standard HEMT on SiC Substrates	Repeat of III541 with GaN cap
III543	5/4/00	HEMT on SiC Substrates	Buried AlGaIn layer to backside confine the 2DEG
III544	5/4/00	Standard HEMT on SiC Substrates	Calibration run, NO GaN cap
III545	5/5/00	Standard HEMT on Sapphire	Calibration run on 0.006" thick sapphire substrates
III546	5/7/00	Standard HEMT on Sapphire	Calibration run on 0.006" thick sapphire substrates
III547	5/8/00	Standard HEMT on SiC Substrates	Calibration run, NO GaN cap, to eliminate buffer charge
III548	5/10/00	Standard HEMT on Sapphire 8-wafer	Calibration run on 0.006" thick sapphire substrates

Appendix C

GaN HEMT Fabrication Outline

Procedure AlGaIn/GaN-based HEMTs processing
(updated 5-15-98, E.M. Chumbes)

Alignment

Procedure	Description
• Wafer Cleaving	Scribe 1.3-1.4cm x 1.3-1.4cm squares.
• Wafer Cleaning	Acetone, Methanol, IPA rinse
• Dehydrate Bake	Oven bake for 10' @ 170C
• Resist Spinning I	Spin 4% PMMA at 5 krpm for 1min 200 nm
• Resist Bake	Bake wafers at 170°C for 1hr in oven (15 min on hotplate)
• Resist Spinning II	Spin 9% P(MMA-MAA) at 3 krpm for 1min 400 nm
• Resist Bake	Bake wafers at 170°C for 1hr in oven (15 min on hotplate)
• Au deposition	Thermal Evaporator 150Å
• E-beam Exposure	EBMF using 600 μ m aperture & 1.6 mm field size Beam current @ 10 nA $\rightarrow$ Beam diameter approx. 100-110 nm Area dosage I: 135 μ C/cm ² Area dosage II: 180 μ C/cm ²
• Au etch	KI, for 30s. Followed by rinse
• Development	MIBK:IPA (1:1) ~70sec followed by IPA rinse
• Descum	2min in O ₂ plasma in Branson barrel asher
• Oxide Etch	30:1 BOE for 30s followed by quick DI rinse
• Align. Mark Depos.	Ti[E1,200Å], Pt[E2,1500Å] Base pressure must be around 2-3 μ torr
• Lift-Off	Soak samples in Methylene Chloride (no dilution) for 10' Squirt wafer w/ strong stream of Acetone until excess metal is removed. Acetone, Methanol, IPA rinse Inspect & Blue Magic Tape (optional)
Thickness of the metal measurements	Check the thickness of the metal with Alpha step

Mesa

Procedure	Description
• Wafer Cleaning I	Acetone, Methanol, IPA rinse Blow dry w/ N2 gas
• Vapor Prime	HMDS Vapor Prime on YES Oven (34 min.)
• Resist Spinning	Shipley 1813 at 5 krpm for 60 sec. (~1.2 μ m) Use swab and Acetone to clean resist off back of wafers.
• Pre exposure bake	115°C Hot Plate for 1.5 min
• Exposure	5:1 GCA Stepper (TRANSPARENT MODE) Exposure Time = 0.35 sec. Focus 276 (SiC) = 0.32 sec. Focus 257 (Al ₂ O ₃) 5:1 GCA Stepper (OPAQUE MODE) Exposure Time = 0.50 sec. Focus 251 (Si) Jobs Ref1 and Ref2 in \$RG\$dx0 Ref2 -> Initial alignment & tilt compensation Ref1 -> Final alignment & exposure
• Development	MF-312:DI (1:1) for 1 min. Slight agitation, Rinse w/ DI water, Blow dry w/ N2 gas.
• Descum	Branson Barrel Asher process 1: 90C. process 2: 1 min
• Post-Develop Bake	115C hotplate for 5'.
• Measure Thickness	Measure resist thickness on Tencor Alpha Step.
• Mesa Etch	ECR-based Etching using Ken's recipe Measure etch depth using Tencor Alpha Step.
• O ₂ plasma resist strip	Branson Barrel Asher process 3: 3 min @ T = 170C
• Complete resist removal	Soak in doubly covered 1165 Remover for overnight. Complete rinse in strong & long stream of IPA and DI followed w/ blow dry w/ N ₂
• Measure Thickness	Measure mesa thickness on Tencor Alpha Step to ensure resist was not attacked

Ohmic

Procedure	Description
• Wafer Cleaning	Acetone, Methanol, IPA rinse Blow dry w/ N ₂ gas
• Native oxide strip	30:1 BOE (no dilution) for 30 s followed by quick DI rinse
• Oxide Deposition	PECVD SiO ₂ @ 300°C (ramp up from 30°C) for 3.0 min → 1000Å
• Vapor Prime	HMDS Vapor Prime on YES Oven (34 min.).
• Resist Spinning	Shipley 1813 at 5 krpm for 60 sec. (~1.2µm)
• Preexposure Bake	115°C Hot Plate for 1.5 min for SiC 2.5 min for Al ₂ O ₃ Use swab and Acetone to clean resist off back of wafers.
• Exposure	5:1 GCA Stepper (TRANSPARENT MODE) "OHMIC FOR HEMTs" Mask Exposure Time = 0.40 sec, Focus 251 for SiC = 0.32 sec, Focus 257 for Al ₂ O ₃ Directory \$RG\$dx0 , job NMODOH for (L&R alignments) , job NGHMOH for (T&B alignments) Position of Alignment marks -5.0 and 5.0
Purge Yes oven	Purge Yes oven for 15 min.
• Image Reversal	YES Oven NH ₃ Process (80 min.).
• Flood Exposure	HTG Contact Aligner UV flood exposure for 30 sec.
• Development	MF-321 Developer (no dilution) for 40-50 sec. Rinse w/ DI water & blow dry w/ N ₂ gas.
• Descum	Branson Barrel Asher Process 1: 90C. Process 2: 1 min
• Oxide Etch	6:1 BOE:H ₂ O (1:1) for 1'20" followed by quick DI rinse.
• Evaporation	Ti[E1,200Å]. Al[T2(E2),1000Å]. Ti[E2(E3),450Å] Au[T3,550Å] Base pressure must be around 2-3 µtorr.
• Lift-Off	Soak wafer in Acetone. Squirt wafer w/ a strong stream of Acetone until excess metal is removed. Acetone for 1 min. Methanol for 1 min. quick IPA rinse. Blow dry w/ N ₂ gas. Inspect & Blue Magic Tape (optional)
• Strip Oxide	6:1 BOE:H ₂ O (1:1) for 1'20" followed by quick DI rinse.

Thickness of the metal measurements	Check the thickness of the metal with Alpha
• Annealing	Optimize temperature with TLM RTA in N ₂ at ≈800°C for 15 sec steps (45 – 60 sec total).
Measure Ohmic Contacts	Measure Ohmic contacts, G-D, G-S & device isolation. Observe smoothness & morphology of annealed contacts

Pad

Procedure	Description
• Wafer Cleaning	Acetone, Methanol, IPA rinse Blow dry w/ N ₂ gas
• Vapor Prime	HMDS Vapor Prime on YES Oven (34 min.).
• Resist Spinning	Shipley 1813 at 5 krpm for 60 sec. (~1.2μm).
• Preexposure Bake	115°C Hot Plate for 1.5 min for SiC 2.5 min for Al ₂ O ₃ Use swab and Acetone to clean resist off back of wafers.
• Exposure	5:1 GCA Stepper (TRANSPARENT MODE) “OHMIC FOR HEMTs” Mask Exposure Time = 0.40 sec, Focus 251 for SiC = 0.32 sec, Focus 257 for Al ₂ O ₃ Directory \$RG\$dx0 , job NMODOH for (L&R alignments) , job NGHMOH for (T&B alignments) Position of Alignment marks -5.0 and 5.0
Purge Yes oven	Purge Yes oven for 15 min.
• Image Reversal	YES Oven NH ₃ Process (80 min.).
• Flood Exposure	HTG Contact Aligner UV flood exposure for 30 sec.
• Development	MF-321 Developer (no dilution) for 40-50 sec. Rinse w/ DI water & blow dry w/ N ₂ gas.
• Descum	Branson Barrel Asher Process 1: 90C. Process 2: 1 min
• Oxide Etch	6:1 BOE:H ₂ O (1:1) for 1'20'' followed by quick DI rinse.
• Evaporation	Ti(Ni)[E1, 100(200Å)]. Au[T2, 3500Å] Base pressure must be around 2-3 μtorr.
• Lift-Off	Soak wafer in Acetone. Squirt wafer w/ a strong stream of Acetone until excess metal is removed. Acetone for 1 min. Methanol for 1 min. quick IPA rinse. Blow dry w/ N ₂ gas. Inspect & Blue Magic Tape (optional)
• Strip Oxide	6:1 BOE:H ₂ O (1:1) for 1'20'' followed by quick DI rinse.
Thickness of the metal measurements	Check the thickness of the metal with Alpha

Gate

Procedure	Description
• Wafer Cleaning (optional)	Acetone, Methanol, IPA rinse Blow dry w/ N ₂ gas
• Dehydration Bake	Bake wafers at 170°C for 10min.
• Resist Spinning I	Spin 4% PMMA at 5 krpm for 1min 200 nm
• Resist Bake	Bake wafers at 170°C for 1hr in oven (15 min on hotplate)
• Resist Spinning II	Spin 9% P(MMA-MAA) at 3 krpm for 1min 400 nm
• Resist Bake	Bake wafers at 170°C for 1hr in oven (15 min on hotplate)
• Resist Spinning III	Spin 4% PMMA at 5 krpm for 1min 200 nm
• Resist Bake	Bake wafers at 170°C for 1hr in oven (15 min on hotplate)
• e-beam exposure	EBMF using 400 μ m aperture & 1.6 mm field size Beam current @ 0.8 – 0.9 nA → Beam diameter approx. 65-70 nm Area dosage: 80 μ C/cm ² Line dosage: 1.1 – 2.5 nC/cm
• Development	For TOP layer: Toulene for 15 s For MID layer: MIBK:IPA (1:1) until 72DM is totally developed For BOT layer: MIBK:IPA (1:1) until 72DM is totally developed
• Descum	4 min in O ₂ plasma in Branson etcher
• Oxide Etch	30:1 BOE for 30s with quick H ₂ O rinse
• Evaporation	Ni[E1,200Å] , Au[T1,4000Å] Base pressure must be around 2-3 μ torr
• Measure metal thickness	Measure Meatal thickness using Alpha to make sure that the metal thickness is OK.
• Lift-off	Methyl.Chloride Soak for 4-5 hrs or overnight Acetone, Methanol, IPA rinse Blow dry w. N ₂ .
• END!!!!	