

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Mianyang BOE Optoelectronics Technology Co., Ltd.; Wuhan China Star
Optoelectronics Semiconductor Display Technology Co., Ltd.; Tianma
Microelectronics Co. Ltd.; and Visionox Technology, Inc.,
Petitioner,

v.

Samsung Display Company, Ltd.,
Patent Owner.

U.S. Patent No. 9,330,593

Case No. IPR2024-00620

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 9,330,593**

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	MANDATORY NOTICES	2
	A. Real Parties-in-Interest	2
	B. Related Matters.....	2
	C. Counsel, Service, and Fee Information	3
III.	REQUIREMENTS FOR IPR	3
	A. Grounds for Standing	3
	B. Identification of Challenge.....	4
IV.	LEVEL OF ORDINARY SKILL IN THE ART.....	5
V.	INSTITUTION SHOULD BE GRANTED.....	5
	A. There Are No Grounds for a § 314 Discretionary Denial.....	5
	B. Denial Under § 325(d) Would Be Inappropriate	6
VI.	THE '593 PATENT.....	7
	A. The Patent's Purported Contribution	7
	B. Prosecution History	9
	C. Claim Construction.....	10
VII.	THE PRIOR ART.....	10
	A. Kimura.....	10
	B. Shin.....	11
	C. Sasaki.....	12
	D. Tobita.....	13
	E. Jeong.....	13

VIII. THE CHALLENGED CLAIMS ARE UNPATENTABLE.....	14
A. GROUND 1: Kimura Renders Claims 1-8, 14-22, and 25 Obvious..	14
1. Independent Claim 1	16
a) [1-PRE]	16
b) Element [1-A]	17
c) Element [1-B]	19
d) Element [1-C]	22
e) Element [1-D]	24
2. Claim 2	24
3. Claim 3	26
4. Claim 4	27
5. Claim 5	28
6. Claim 6	29
7. Claim 7	32
8. Claim 8	34
9. Claim 14	36
10. Independent Claim 15	37
a) [15-PRE]	37
b) Element [15-A]	37
c) Element [15-B]	38
d) Element [15-C]	39
e) Elements [15-D]-[15-G]	41
11. Claim 16	41

12.	Claim 17.....	42
13.	Claim 18.....	42
14.	Claim 19.....	43
15.	Claim 20.....	43
16.	Claim 21.....	44
17.	Claim 22.....	44
18.	Claim 25.....	44
B.	GROUND 2: Shin and Sasaki Render Claims 1-6, 8, 14-20, 22, and 25 Obvious	44
1.	Independent Claim 1	53
	a) [1-PRE].....	53
	b) Element [1-A]	54
	c) Element [1-B]	56
	d) Element [1-C]	57
	e) Element [1-D]	58
2.	Claim 2.....	59
3.	Claim 3.....	61
4.	Claim 4.....	62
5.	Claim 5.....	63
6.	Claim 6.....	63
7.	Claim 8.....	64
8.	Claim 14.....	66
9.	Independent Claim 15.....	67

a)	[15-PRE]	67
b)	Element [15-A]	67
c)	Element [15-B]	68
d)	Element [15-C]	69
e)	Elements [15-D]-[15-G]	71
10.	Claim 16	71
11.	Claim 17	71
12.	Claim 18	71
13.	Claim 19	73
14.	Claim 20	73
15.	Claim 22	73
16.	Claim 25	73
C.	GROUND 3: Shin, Sasaki, and Jeong Render Claims 7 and 21 Obvious.....	74
D.	GROUND 4: Tobita Renders Claims 1-2 and 15-18 Obvious	80
1.	Independent Claim 1	81
a)	[1-PRE]	81
b)	Element [1-A]	82
c)	Element [1-B]	84
a)	Element [1-C]	85
b)	Element [1-D]	86
2.	Claim 2	87
3.	Independent Claim 15	88

a)	[15-PRE]	88
b)	Element [15-A]	89
c)	Element [15-B]	90
d)	Element [15-C]	91
e)	Elements [15-D]-[15-G]	93
4.	Claim 16	93
5.	Claim 17	94
6.	Claim 18	94
E.	GROUND 5: Tobita in View of Jeong Renders Claims 7 and 21 Obvious	95
IX.	SECONDARY CONSIDERATIONS	98
X.	CONCLUSION	98

LISTING OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 9,330,593 (the “’593 patent”)
1002	Prosecution History of U.S. Patent No. 9,330,593
1003	Declaration of Dr. Daniel Foty
1004	U.S. Patent Publication No. 2011/057190A1 (“Kimura”)
1005	U.S. Patent Publication No. 2007/0063950A1 (“Shin”)
1006	U.S. Patent Publication No. 2008/0101529A1 (“Tobita”)
1007	U.S. Patent Publication No. 2008/0062097A1 (“Jeong”)
1008	Excerpts from <i>Analog Integrated Circuit Design</i> , David A. Johns et al., John Wiley & Sons, Inc. (1997)
1009	Complainant’s Opening Claim Construction Brief, <i>In the Matter of Certain Active Matrix Organic Light-Emitting Diode Display Panels and Modules for Mobile Devices, and Components Thereof</i> , Inv. No. 337-TA-1351
1010	Excerpts from <i>Physics and Technology of Semiconductor Devices</i> , A. Grove, John Wiley & Sons (1967)
1011	Excerpts from <i>CMOS Digital Integrated Circuits: Analysis and Design</i> , (third edition), S. Kang et al., McGraw-Hill (2003)
1012	Docket from <i>Samsung Display Co., Ltd. v. BOE Technology Co., Ltd.</i> , E.D. Tex. 2-23-cv-00309
1013	U.S. Patent Publication No. 2003/0132931A1 (“Kimura”)
1014	U.S. Patent Publication No. 2005/0185752A1 (“Sasaki”)
1015	U.S. Patent Publication No. 2007/0139348A1 (“Lee”)

1016	U.S. Patent No. 4,720,815 (“Ogawa”)
1017	EP 0 138 406 A2 (“Takemae”)
1018	U.S. Patent No. 4,740,922 (“Ogawa II”)
1019	Excerpts from Wolf, “Silicon Processing for the VLSI Era: Volume 2 – Process Integration” (1990)
1020	U.S. Patent Publication No. 2007/0263763 A1 to Moon (“Moon”)
1021	<i>Intentionally Omitted</i>
1022	J. Miller, “Dependence of the input impedance of a three-electrode vacuum tube upon the load in the plate circuit,” Scientific Papers of the Bureau of Standards, 15(351), pp. 367–385 (1920)
1023	US Patent Publication No. 2007/0085808A1 (“Lee”)
1024	US Patent Publication No. 2009/0115792A1 (“Otose”)

CHALLENGED CLAIM LISTING

Claim	Limitation No.	Limitation
1	[1-PRE]	A stage circuit having a first input terminal, a second input terminal, a third input terminal, and an output terminal, the stage circuit comprising:
	[1-A]	an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node;
	[1-B]	a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal; and
	[1-C]	a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node,
	[1-D]	wherein the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver.
2	[2-A]	The stage circuit as claimed in claim 1, wherein the first input terminal receives an output signal of a previous stage circuit or a start signal,
	[2-B]	wherein the second input terminal receives a first clock signal, and
	[2-C]	wherein the third input terminal receives a second clock signal.
3	3	The stage circuit as claimed in claim 2, wherein the first clock signal and the second clock signal have the same period and have phases that do not overlap.

Claim	Limitation No.	Limitation
4	4	The stage circuit as claimed in claim 3, wherein the first clock signal and the second clock signal have a period equal to two horizontal periods 2H and are supplied in different horizontal periods as low signals.
5	5	The stage circuit as claimed in claim 2, wherein the start signal is supplied to overlap the first clock signal.
6	[6-A]	The stage circuit as claimed in claim 2, wherein the first driver includes: a first transistor between the first input terminal and the second node, the first transistor having a gate electrode coupled to the second input terminal; and
	[6-B]	a second transistor and a third transistor serially positioned between the second node and the first power supply,
	[6-C]	wherein a gate electrode of the second transistor is coupled to the third input terminal, and
	[6-D]	wherein a gate electrode of the third transistor is coupled to the first node.
7	[7-A]	The stage circuit as claimed in claim 2, wherein the outputting unit includes: a fourth transistor between the first power supply and the output terminal, the fourth transistor having a gate electrode coupled to the first node:
	[7-B]	a fifth transistor between the output terminal and the third input terminal, the fifth transistor having a gate electrode coupled to the second node;

Claim	Limitation No.	Limitation
	[7-C]	a first capacitor between the second node and the output terminal; and
	[7-D]	a second capacitor between the first node and the first power supply.
8	[8-A]	The stage circuit as claimed in claim 2, wherein the second driver includes: a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and
	[8-B]	a seventh transistor between the first node and a second power supply, the second power supply having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal.
14	14	The stage circuit as claimed in claim 1, wherein the transistor controls the voltage of the second node according to the on/off operation thereof.
15	[15-PRE]	An organic light emitting display, comprising:
	[15-A]	pixels positioned in regions partitioned by scan lines and data lines;
	[15-B]	a data driver for supplying data signals to the pixels through the data lines; and
	[15-C]	a scan driver for supplying scan signals to the pixels through the scan lines, the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals and having a first input terminal, a second input terminal, a third input terminal, and an output terminal,

Claim	Limitation No.	Limitation
	[15-D]	wherein each of the stage circuits includes: an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node,
	[15-E]	a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal, and
	[15-F]	a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node,
	[15-G]	wherein the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver.
16	16	The organic light emitting display as claimed in claim 15, wherein a clock signal supplied to the third input terminal is used as the scan signal.
17	17	The organic light emitting display as claimed in claim 15, wherein the first input terminal receives a scan signal of a previous stage circuit or a start signal.
18	[18-A]	The organic light emitting display as claimed in claim 17, wherein second input terminals of odd stage circuits receive a first clock signal and third input terminals of odd stage circuits receive a second clock signal, and

Claim	Limitation No.	Limitation
	[18-B]	wherein second input terminals of even stage circuits receive the second clock signal and third input terminals of even stage circuits receive the first clock signal.
19	19	The organic light emitting display as claimed in claim 18, wherein the first clock signal and the second clock signal have the same period and have phases that do not overlap.
20	[20-A]	The organic light emitting display as claimed in claim 18, wherein the first driver includes: a first transistor between the first input terminal and the second node, the first transistor having a gate electrode coupled to the second input terminal; and
	[20-B]	a second transistor and a third transistor serially positioned between the second node and the first power supply,
	[20-C]	wherein a gate electrode of the second transistor is coupled to the third input terminal, and
	[20-D]	wherein a gate electrode of the third transistor is coupled to the first node.
21	[21-A]	The organic light emitting display as claimed in claim 18, wherein the outputting unit includes: a fourth transistor between the first power supply and the output terminal, the fourth transistor having a gate electrode coupled to the first node;
	[21-B]	a fifth transistor between the output terminal and the third input terminal, the fifth transistor having a gate electrode coupled to the second node;
	[21-C]	a first capacitor between the second node and the output terminal; and

Claim	Limitation No.	Limitation
	[21-D]	a second capacitor between the first node and the first power supply.
22	[22-A]	The organic light emitting display as claimed in claim 18, wherein the second driver includes: a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and
	[22-B]	a seventh transistor between the first node and a second power supply, the second power supply having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal.
25	25	The organic light emitting display as claimed in claim 18, wherein the scan signal of the previous stage circuit or the start signal supplied to the first input terminal overlaps the clock signal supplied to the second input terminal.

I. INTRODUCTION

Pursuant to 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42, Petitioner respectfully requests *inter partes* review (“IPR”) of Claims 1-8, 14-22, and 25 (“Challenged Claims”) of U.S. Patent No. 9,330,593 (the “’593 patent”).

The ’593 patent relates to stage circuits for organic light emitting diode (“OLED”) displays. The patent admits that stage circuits are a “[c]onventional” part of a display. Ex. 1001, 1:17-47. But, the ’593 patent criticizes existing stage circuits for purportedly having too many transistors or initializing signals. It then purports to disclose stage circuits with “a reduced number of transistors and that output scan signals only using first and second clock signals.” *Id.*, 9:12-26.

The ’593 patent’s claims further require a particular “on/off” transistor in the stage circuit: “the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver.” See Claims 1, 15. This requirement was added during prosecution to overcome prior art stage circuits teaching everything else the claims require.

But this allegedly distinguishing feature was also in the prior art. As this Petition shows, it was well-known to include a transistor directly controlled by the signal of a third input terminal in the first driver of a stage circuit.

Petitioner requests that the PTAB institute trial and find the Challenged Claims unpatentable for the reasons set forth herein.

II. MANDATORY NOTICES

A. Real Parties-in-Interest

Mianyang BOE Optoelectronics Technology Co., Ltd. (“BOE”); Wuhan China Star Optoelectronics Semiconductor Display Technology Co., Ltd.; Tianma Microelectronics Co. Ltd.; and Visionox Technology, Inc. and their subsidiaries are the real parties-in-interest. No other parties exercised or could have exercised control over this Petition; no other parties funded or directed this Petition. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48759-60.

B. Related Matters

To the best knowledge of Petitioner, the ‘593 patent has been involved in the following matters:

Case Name	Filed
ITC Investigation No. 337-TA-1351, <i>In the Matter of Certain Active Matrix Organic Light-Emitting Diode Display Panels and Modules for Mobile Devices, and Components Thereof</i>	December 28, 2022
<i>Samsung Display Co., Ltd. v. BOE Technology Co., Ltd.</i> , E.D. Tex. 2-23-cv-00309	June 26, 2023

Petitioner previously filed another petition for *inter partes* review relating to the ‘593 patent in IPR2023-01221. But, Petitioner withdrew that petition—and the proceeding was subsequently terminated—prior to the filing of Patent Owner’s preliminary response.

C. Counsel, Service, and Fee Information

Petitioner's Lead Counsel	Petitioner's Back-Up Counsel
K. Patrick Herman Reg. No. 75,018 Orrick, Herrington & Sutcliffe LLP 51 West 52nd Street New York, NY 10019 Telephone: (212) 506-3596 P52PTABDocket@orrick.com	Richard F. Martinelli Reg. No. 52,003 Orrick, Herrington & Sutcliffe LLP 51 West 52nd Street New York, NY 10019-6142 Telephone: (212) 506-3702 RFMPTABDocket@orrick.com Xiang Wang Reg. No. 45,547 Orrick, Herrington & Sutcliffe LLP 5701 China World Tower A No. 1 Jianguomenwai Avenue Beijing, 100004 People's Republic of China Telephone: +86 10 8595-5600 XW0PTABDocket@orrick.com

Petitioner submits a Power of Attorney with this Petition. Please address all correspondence to lead counsel. Petitioner consents to service by email at the email addresses listed above.

The USPTO is authorized to charge the filing fee and any other fees incurred by Petitioner to the deposit account of Orrick, Herrington, & Sutcliffe LLP: 15-0665.

III. REQUIREMENTS FOR IPR

A. Grounds for Standing

Petitioner certifies that the '593 patent is available for IPR, and that Petitioner

is not barred or estopped from requesting this IPR.

B. Identification of Challenge

Petitioner requests IPR of claims 1-8, 14-22, and 25. This petition discusses claim construction, explains why the claims are unpatentable, provides details regarding where the various claim limitations are found in the prior art, and is supported by the accompanying Declaration of Dr. Daniel Foty (Ex. 1003, “Decl.”).

The ’593 patent claims priority to foreign application KR 10-2012-0104512, filed on September 20, 2012. For purposes of this petition only, it is assumed that the claims are entitled to the benefit of this date.

Petitioner relies on the following references, each of which is prior art under 35 U.S.C. §102(b):

Patent/Publication	Published	Ex.
U.S. Pub. 2011/057190A1 (“Kimura”)	3/10/2011	1004
U.S. Pub. 2007/0063950A1 (“Shin”)	3/22/2007	1005
U.S. Pub. 2005/0185752A1 (“Sasaki”)	8/25/2005	1014
U.S. Pub. 2008/0101529A1 (“Tobita”)	7/28/2011	1006
U.S. Pub. 2008/0062097A1 (“Jeong”)	3/13/2008	1007

Below are the specific grounds on which the claims are challenged:

Ground	Basis
1	Claims 1-8, 14-22, and 25 obvious over Kimura

Ground	Basis
2	Claims 1-6, 8, 14-20, 22, and 25 obvious over Shin and Sasaki
3	Claims 7 and 21 obvious over Shin, Sasaki, and Jeong
4	Claims 1-2 and 15-18 obvious Tobita
5	Claims 7 and 21 obvious over Tobita and Jeong

IV. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA in the technology described in the '593 patent in 2012 would have had a Bachelor's degree in electrical engineering or a similar discipline, along with 2-3 years of circuit design experience. Decl., ¶¶ 27-29.

V. INSTITUTION SHOULD BE GRANTED

This Petition establishes a reasonable likelihood of success on the merits. And, all other requirements for IPR are met.

A. There Are No Grounds for a § 314 Discretionary Denial

There are co-pending ITC and district court proceedings involving the '593 patent. The Board considers the factors set forth in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020), clarified by the Director, when determining whether to institute when there are co-pending proceedings. When considered as a whole, the factors weigh strongly in favor of institution. In particular, the co-pending ITC proceeding has no bearing on whether institution is appropriate. See Interim Procedure for Discretionary Denials at 2-3 (June 21, 2022).

And, the co-pending district court proceeding has been stayed pending resolution of the ITC proceeding. It has not meaningfully progressed. *See* Ex. 1012. This weighs in favor of institution. *See Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 8-9, 11 (PTAB June 16, 2020). Moreover, “compelling, meritorious challenges will be allowed to proceed at the PTAB even where district court litigation is proceeding in parallel.” *Id.* at 4-5. That is the case here: as explained below, the Challenged Claims of the ’593 patent are plainly unpatentable in view of the prior art.

Finally, while petitioner did file another IPR petition challenging the claims of the ’593 patent, it withdrew that petition before both the filing of Patent Owner’s preliminary response and the Board’s statutory deadline for issuing an institution decision. *See* IPR2023-01221, Paper 10. Petitioner did so to avoid a dispute regarding the ’593 patent’s date of invention: unlike certain of the references in the prior petition, the references here all qualify as prior art under pre-AIA 102(b). Thus, this is not a case where there are multiple IPRs challenging the same patent: only this IPR is at issue.

Should Patent Owner urge the Board to exercise its discretion to deny institution, Petitioner respectfully requests a reply brief.

B. Denial Under § 325(d) Would Be Inappropriate

No ground presented here was considered by the Examiner or otherwise

previously considered by the Patent Office. Kimura, Shin, Sasaki, and Tobita were not cited by the applicant or considered by the Examiner. *See generally* Ex. 1002. Further, as explained in Section VI.B below, the prior art references the Examiner did address purportedly failed to teach a transistor whose on/off operation is directly controlled by the signal of the third input terminal. In contrast, Kimura, the combination of Shin and Sasaki, and Tobita all specifically teach shift registers that include this very type of transistor. Thus, this art is substantively different from and overcomes any purported deficiencies identified in connection with the art considered by the Examiner.

VI. THE '593 PATENT

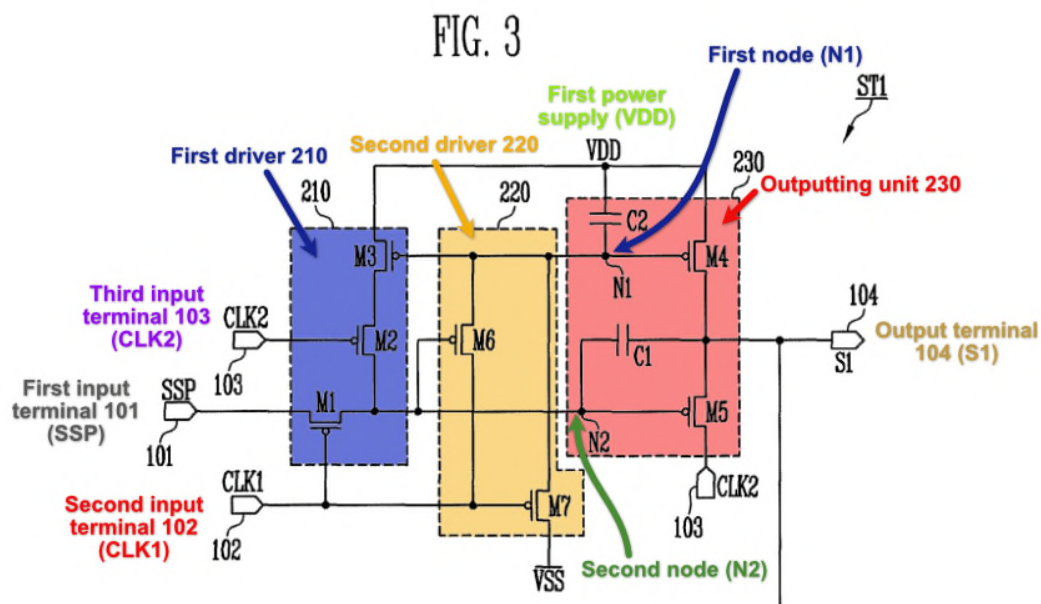
The '593 patent relates to stage circuits for OLED displays. Ex. 1001, 1:17-18. These circuits were admittedly well-known. *See id.*, 1:20-47. According to the patent, a “[c]onventional” OLED “display includes a data driver” that supplies “data signals” to data lines, a “scan driver for sequentially supplying scan signals to scan lines, and ... a plurality of pixels coupled to the scan lines and the data lines.” *Id.*, 1:34-38. “The scan driver includes stage circuits” that “supply the scan signals....” *Id.*, 1:45-47.

A. The Patent’s Purported Contribution

“[C]onventional” stage circuits purportedly require large numbers of transistors and/or initializing signals. Ex. 1001, 9:15-18. The patent thus proposes

a circuit with fewer transistors/signals. *Id.*, 9:12-14; *see also* Decl., ¶¶ 83-84. This purportedly increases production yield and improves stability through decreased complexity. Ex. 1001, 9:18-26; Decl., ¶ 84. Nothing in the claims, however, limits the numbers of transistors or input signals. *See, e.g.*, claim 1 (“comprising”); Decl., ¶ 84.

Figure 3—annotated to show the components required by claim 1—depicts a preferred embodiment:



Ex. 1001, Fig. 3.¹ The circuit includes a first input terminal SSP, a second input terminal CLK1, a third input terminal CLK2, a first power supply VDD, and an

¹ All color has been added by Petitioner.

output terminal Sn (n denotes the stage number).² The first input terminal SSP receives a start signal or the output signal from the previous stage. *Id.*, 5:1-7. The second and third input terminals receive clock signals having the same period but nonoverlapping phases. *Id.*, 5:8-28. The components are grouped into a so-called first driver, second driver, and outputting unit. The first driver and the second driver respectively control the voltage of the second node N2 and the first node N1. *Id.*, 5:63-67, 6:22-26. The outputting unit supplies either CLK2 or VDD to the output terminal Sn according to the first node or the second node voltage. *Id.*, 5:37-41.

As shown, the first driver includes a transistor M2. The same third input CLK2 supplied to the output terminal is supplied to this transistor's gate. *See id.*, Fig. 3; *see also* Decl., ¶¶ 85-87. The patentee highlighted this during prosecution to overcome prior-art rejections. *See infra* Section VI.B.

B. Prosecution History

During prosecution, the claims were rejected as anticipated by or obvious over Jeong. Ex. 1002, pp. 123-133.

In response, the patentee amended the claims to require that “the signal of the third input terminal at least controls an on/off operation of a switch.” *Id.*, pp. 101-108. According to the patentee, Jeong does not teach this because its third input

² Colored text matches that used to annotate the figures.

terminal (CLK3) is connected only to a transistor's drain, and not its gate. *See id.* at 110-111.

The Examiner then again rejected the claims as obvious in view of Jeong and supplemental references. *Id.* at 81-92. This eventually led the patentee to amend the claims to require that the “transistor” that “controls an on/off operation” be “included in the first driver.” *Id.* at 31, 34-35; *see id.* at 40-42. A notice of allowance followed. *See id.* at 11-14; *see also* Decl., ¶¶ 88-97.

C. Claim Construction

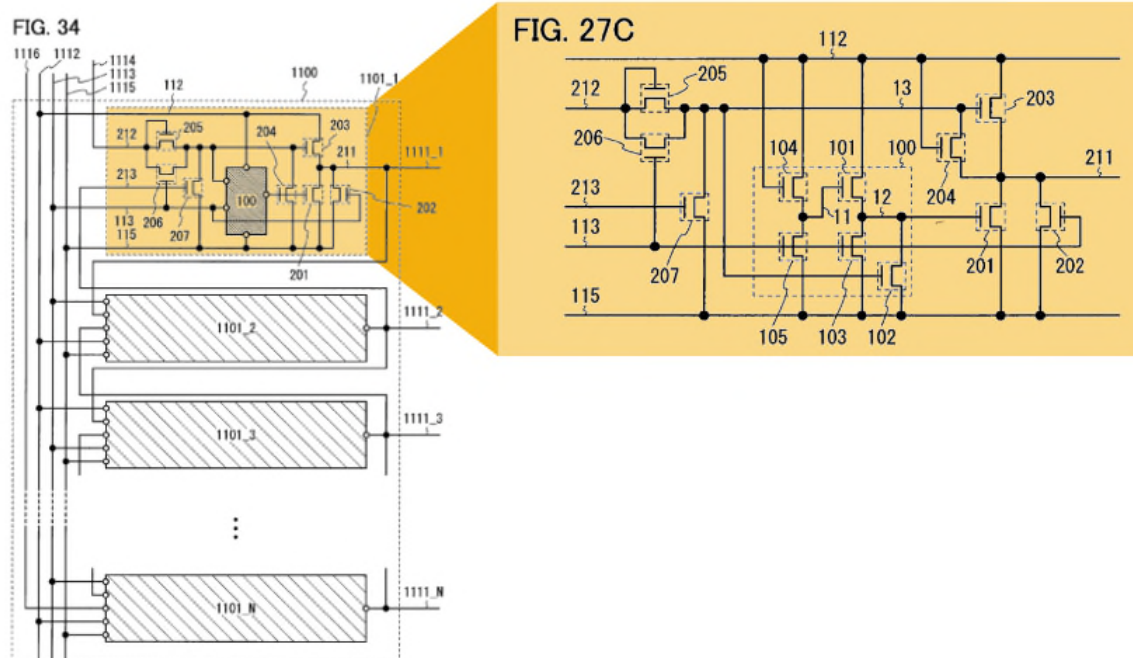
The Board applies the same *Phillips* claim construction standard used by district courts. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). Petitioner does not believe any claim construction is necessary here. In a related ITC proceeding, Patent Owner argued that all terms should be given their plain and ordinary meaning. For purpose of this proceeding, Petitioner applies Patent Owner's position without agreeing to its correctness. *See also* Decl., ¶¶ 98-100.

VII. THE PRIOR ART

A. Kimura

Kimura teaches a “display device” with a “shift register circuit.” Kimura, [0320]. This “shift register circuit 1100” includes stages of “flip-flop circuits 1101_1 to 1101_N....” *Id.*, [0333]. Kimura includes numerous embodiments. This petition focuses on the stage circuit of Figure 27C. Figure 34 shows an overall

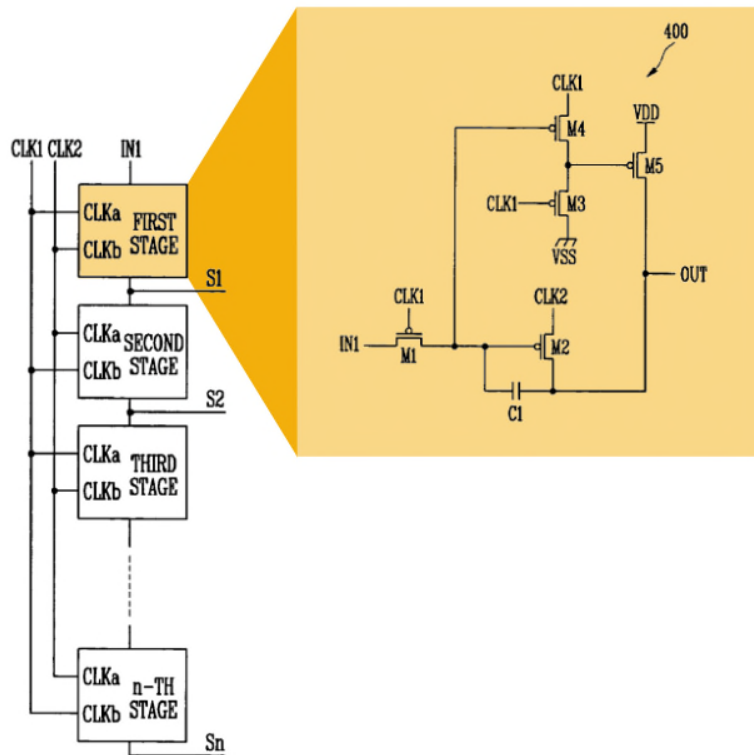
register including such a stage:



Id., Figs. 27C, 34; *see also* Decl., ¶¶ 102-108.

B. Shin

Shin relates to a “scan driving circuit” for an OLED display. Shin, [0003]. Shin seeks to improve on prior art by removing excessive “static” or “constant” “current flows.” *Id.*, [0012]-[0015]. Figure 10 provides an example “scan driver.” *Id.*, [0115]. Figure 11 shows “stage” of Figure 10’s scan driver. *Id.*, [0120].



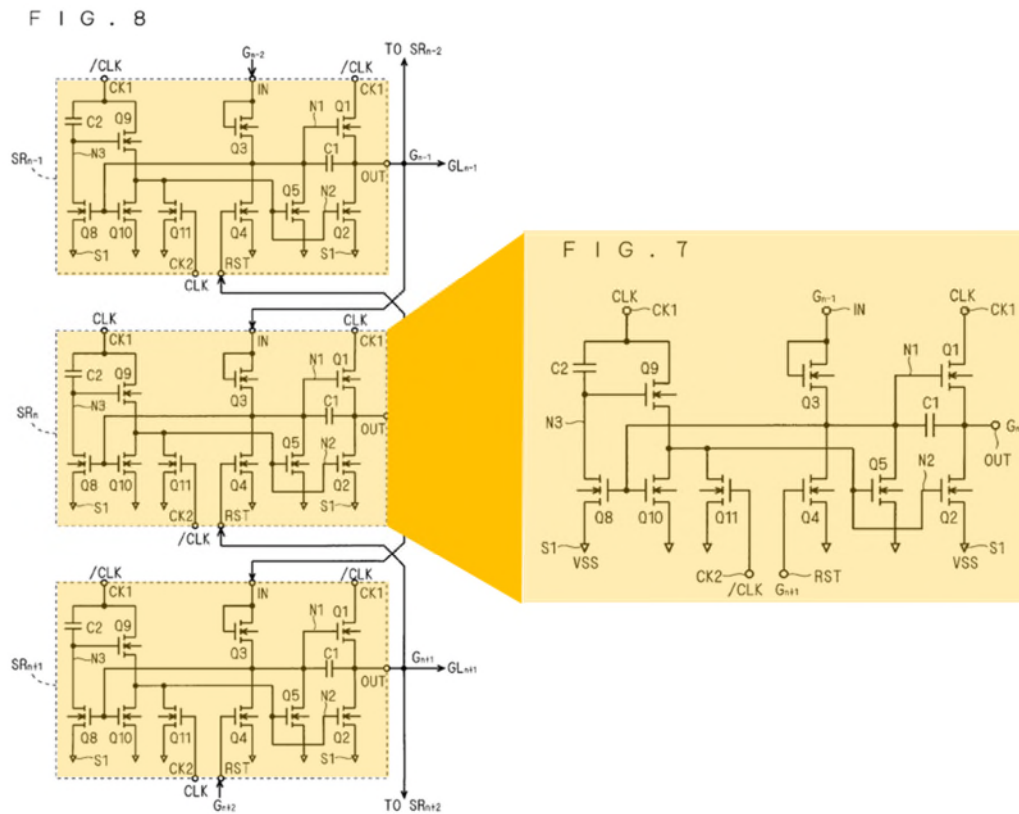
Id., Figs. 10, 11 (both excerpted); *see also* Decl., ¶¶ 109-113.

C. Sasaki

Sasaki relates to a “shift register” circuit for a “display device.” Sasaki, [0003]. Sasaki explains that such circuits experience problems if transistor “control electrode[s]” enter a “floating state.” *Id.*, [0042]. This makes it possible that the transistor may be “reversed” leading to output of the wrong signal. *Id.* To address this, Sasaki employs an “anti-reversal circuit.” *Id.*, [0042]. The anti-reversal circuit includes two serially arranged transistors that supply a signal preventing output transistor reversal. *Id.*; *see also* Decl., ¶¶ 114-118.

D. Tobita

Tobita also discloses a display “shift register ... circuit[.]” Tobita, [0002]. The shift register includes a gate-line driving circuit (or scanning-line driving circuit) 30 with multiple stages. *Id.*, [0027], [0117]. Each stage—or unit shift register SR_n —can have the structure shown in Figure 7:



Id., Figs. 7-8, [0026]-[0027], [0117], [0167]. Figures 19 and 20 depict variants of Figure 7 with many overlapping, shared elements. *Id.*, [0168], [0172], [0177]; see also Decl., ¶¶ 119-124.

E. Jeong

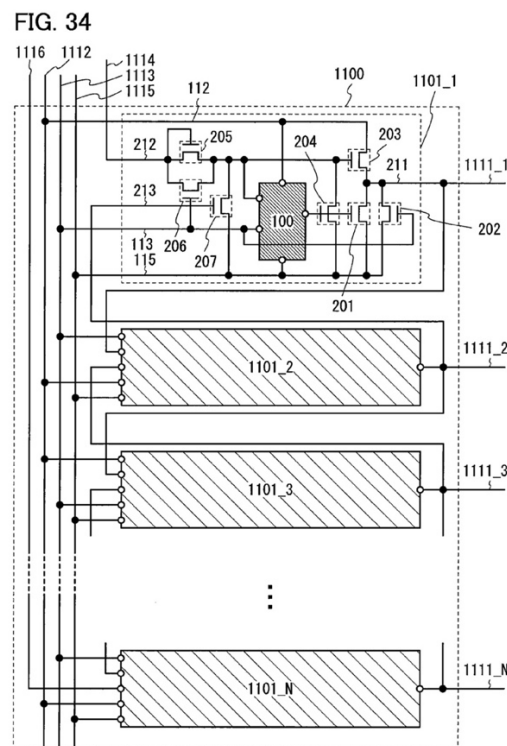
Jeong discloses shift registers for an OLED display scan driver. Jeong,

[0002]. Among other components, each stage of the register includes capacitors to reduce transistor gate voltage variation and improve output. *Id.*, [0056]-[0057]; see also Decl., ¶¶ 125-129.

VIII. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. GROUND 1: Kimura Renders Claims 1-8, 14-22, and 25 Obvious

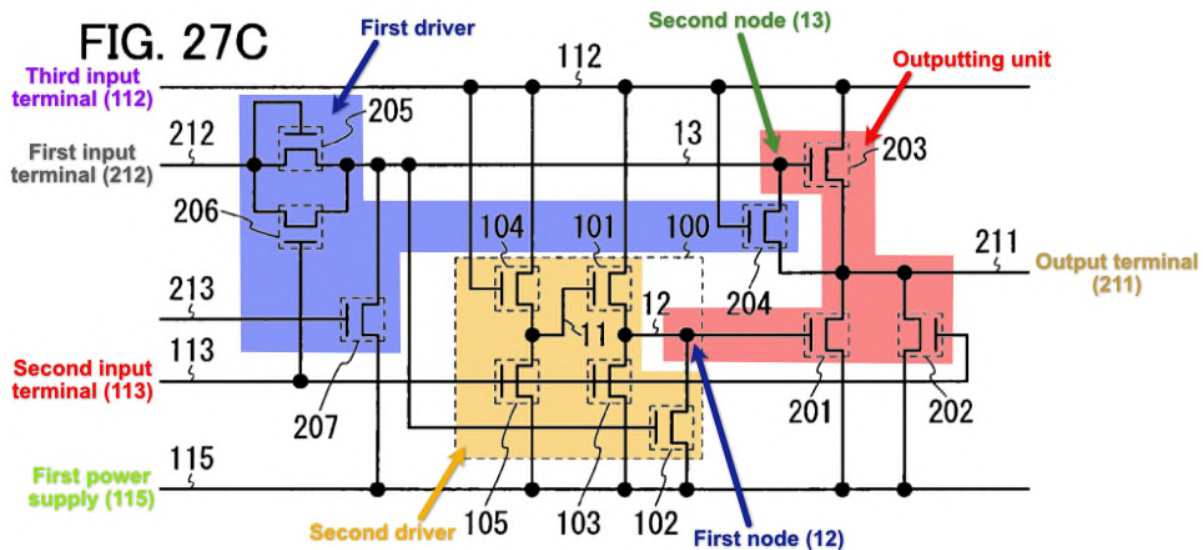
Kimura renders claims 1-8, 14-22, and 25 obvious. Kimura teaches a “display device” with a “shift register circuit.” Kimura, [0320]. Fig. 34 shows one such “shift register” formed from stages 1101_1-1101_N. *Id.*, [0333].



Id., Fig. 34.

Any of the “semiconductor device[s]” Kimura discusses can be used as circuits 1101_1-1101_N. *Id.*, [0320], [0339]. Figure 27C shows one such device.

Id., [0072]. This shift register stage includes all the components required by independent claims 1 and 15 of the '593 patent (and many dependent claims):



Id., Fig. 27C; Decl., ¶¶ 133-147.

This ground is expressed in terms of obviousness, and not anticipation, because the portion of Kimura discussing Figure 27C does not itself mention all the depicted transistors, inputs, and outputs. Kimura explains, however, that the device of Figure 27C builds on and shares components with the devices of its other figures. Kimura, [0282]-[0286]. Thus, a POSITA would have understood that any shared components in Figure 27C not specifically discussed in the portion of Kimura addressing the figure would obviously be connected—and function—in the same way discussed elsewhere. See Decl., ¶ 146. To be clear, this ground—at least with respect to claims 1 and 15—does not propose that Kimura’s embodiments be

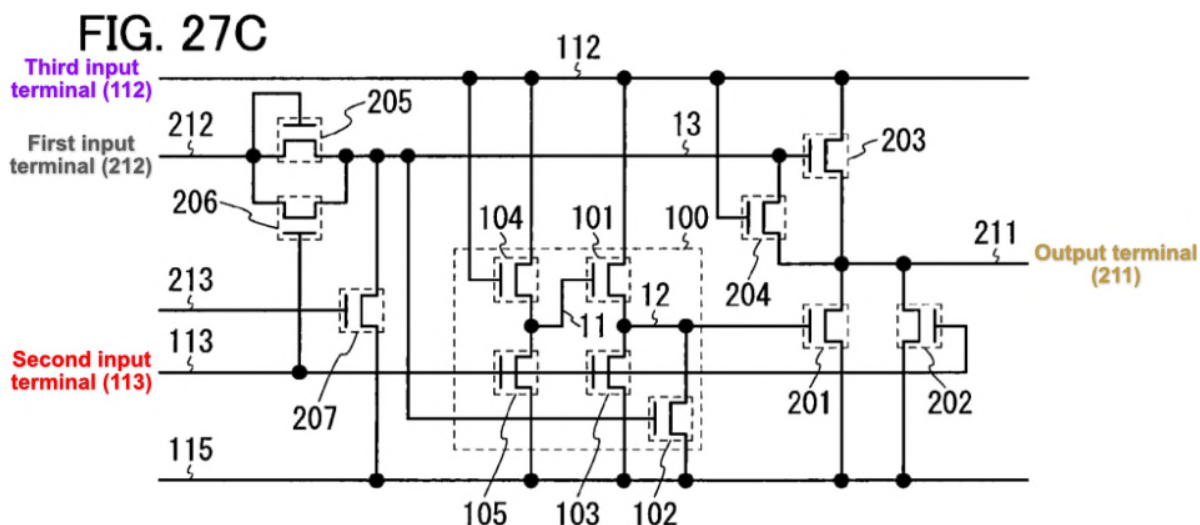
combined, or that the device of Figure 27C be modified. Instead, when the totality of Kimura’s teachings are considered, the device of Figure 27C itself renders the claims obvious. *See, e.g., Game and Tech. Co. v. Activision Blizzard Inc.*, 926 F.3d 1370, 1381 (Fed. Cir. 2019).

Dependent claims 6-8 and 20-22 include additional elements not part of Figure 27C. Kimura explains, however, that the figure’s device can be supplemented with—and improved by—the further components these claims require.

1. Independent Claim 1

a) [1-PRE]

To the extent limiting, Kimura teaches “[a] stage circuit having a first input terminal, a second input terminal, a third input terminal, and an output terminal”:

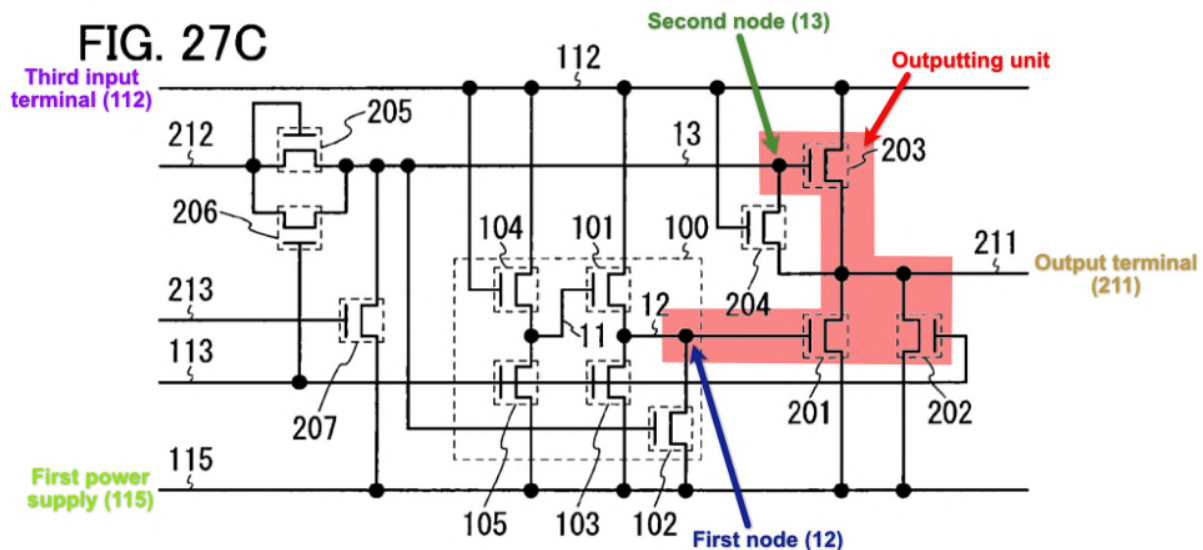


Kimura, Fig. 27C. Again, this figure depicts a “stage” of a display’s “shift register

circuit.” *Id.*, [0320], [0324], [0333]. The “signal IN4”—which “function[s] as a start pulse”—“is input to the wiring 212” (the claimed first input terminal). *Id.*, [0266]. “A signal IN1 is input” to “wiring 112” (the third input terminal). *Id.*, [0104]. “A signal IN2 is input to the wiring 113” (the second input terminal). *Id.* IN1 and IN2 are both “clock signal[s].” *Id.*, [0109]; *see also id.*, [0230]-[0232]. “[W]iring 211” (the output terminal) outputs the “signal GOUT[.]” *Id.*, [0226]; *see also id.*, ¶ [0103]; Decl. ¶¶ 136-144.

b) Element [1-A]

Kimura includes the claimed “outputting unit”:



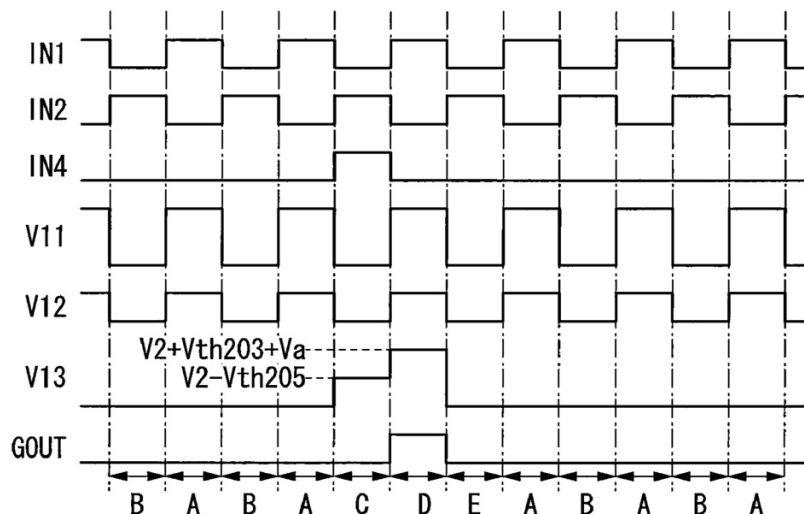
Kimura, Fig. 27C. Transistors 201-203 are responsible for generating stage output. More specifically, a “signal IN1 is input to the wiring 112” (the claimed third input terminal). *Id.*, [0104]. “[T]ransistor 203 ... control[s] conduction between the

wiring 112 and the wiring 211” (the claimed **output terminal**). *Id.*, [0250]. “[T]ransistor 203” is “controlled by the potential of the node 13” (the **second node**). *Id.* “A voltage V_1 is supplied to the wiring 115” (the claimed **first power supply**). *Id.*, [0105]. “The voltage V_1 is” a “power supply voltage.” *Id.* “[T]ransistor 201 ... control[s] conduction between the wiring 115 and the wiring 211” (again, the **output terminal**). *Id.*, [0222]. The “transistor 201 can be controlled by the output signal of the circuit 100.” *Id.* As shown in Figure 27C, the gate of transistor 201 is connected to and controlled by node 12 (the **first node**) exiting from circuit 100. *Id.*, Fig. 27C; *see also id.*, ¶ [0226] (“circuit 100” outputs a signal to “node 12”). Like transistor 201, transistor 202 also operates to connect wiring 115 to wiring 211. But, it does so in response to the signal provided via wiring 113. *Id.*, [0245]-[0246]; *see also* Decl., ¶¶ 148-160.

In operation, during a “period A” input signals are supplied to the shift register to cause “the potential of the node 12” to be “set at a H level.” Kimura, [0253]. This causes “transistor 201” to be “turned on” supplying “the potential of the wiring 115 (e.g., the voltage V_1) ... to the wiring 211.” *Id.* During “period C” and “period D[,]” however, different input signals cause “the potential of the node 12” to be “set at an L level” so that “transistor 201 is turned off.” *Id.*, [0255]-[0256]. At the same time, “the potential of the node 13 becomes an H level” allowing “transistor 203” to be turned on and “signal IN1” to be supplied to wiring 211. *Id.*, [0256].

Figure 21B provides an example “timing chart for illustrating operation of the semiconductor device[.]” *Id.*, [0062], [0066]. While the chart is not specific to the device of Figure 27C, a POSITA would have understood that that device—because it includes the same input and output lines and many of the same transistors as Kimura’s other circuits—would (or at least obviously could) be supplied with input signals in the same manner and with the same timing. *See Decl.*, ¶¶ 160-165.

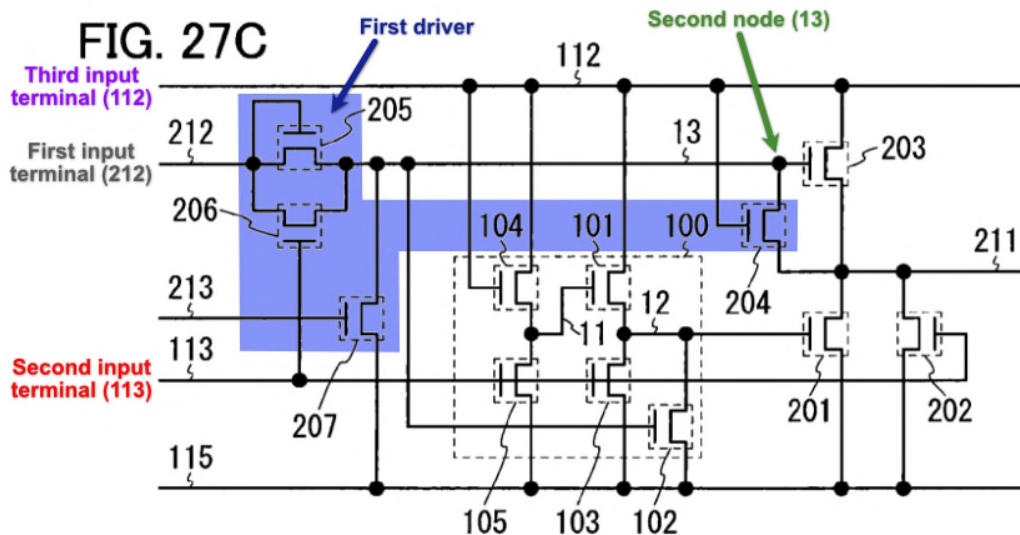
FIG. 21B



Kimura, Fig. 21B; *see also id.*, Fig. 17B.

c) Element [1-B]

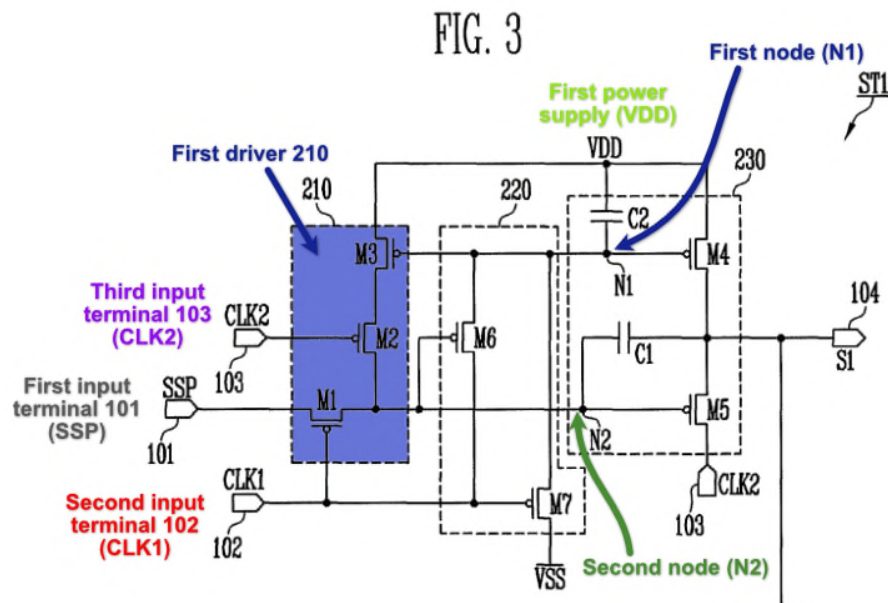
Figure 27C of Kimura includes the claimed “[first driver](#) to control the voltage of the [second node](#)”:



Kimura, Fig. 27C; see also Decl. ¶¶ 170-171. As shown, a “transistor 205” is diode connected to “wiring 212” (Kimura’s first input terminal, receiving signal IN4). Kimura, [0264]-[0265]. This transistor “control[s] conduction between the wiring 212 and the node 13” (Kimura’s second node). *Id.*, [0268]. Among other things, it can supply a “H-level signal” from wiring 212 to the node. *Id.* Next, a “transistor 206” includes one “terminal connected to the wiring 212” (the first input terminal), another “terminal ... connected to the node 13[,]” and a “gate ... connected to the wiring 113” (the second input terminal, receiving signal IN2). *Id.*, [0270]-[0271]. Using the signal from wiring 113, this transistor also facilitates “conduction between the wiring 212 and the node 13 and allows for the supply of a “L-level signal” to the node 13. *Id.*, [0272]. Another “transistor 204” has its “first terminal ... connected to the wiring 211” and a gate “connected to wiring 112” (the third input terminal).

Id., [0286]. This allows “the potential of the node 13” to be “lowered” for purposes of preventing “dielectric breakdown or deterioration of” any transistors connected to the node. *Id.* Finally, a transistor 207 receives input from wiring 213 and operates to connect “wiring 115” to the “node 13.” *Id.*, [0276]-[0280]. Thus, transistors 204-207 (the **first driver**) collectively receive input from wires 212 (the **first input terminal**), 113 (the **second input terminal**), 112 (the **third input terminal**), and 213 for purposes of controlling node 13’s (the **second node**) potential. *See id.*, Figs. 17B, 21B; *see also* Decl., ¶¶ 172-179.

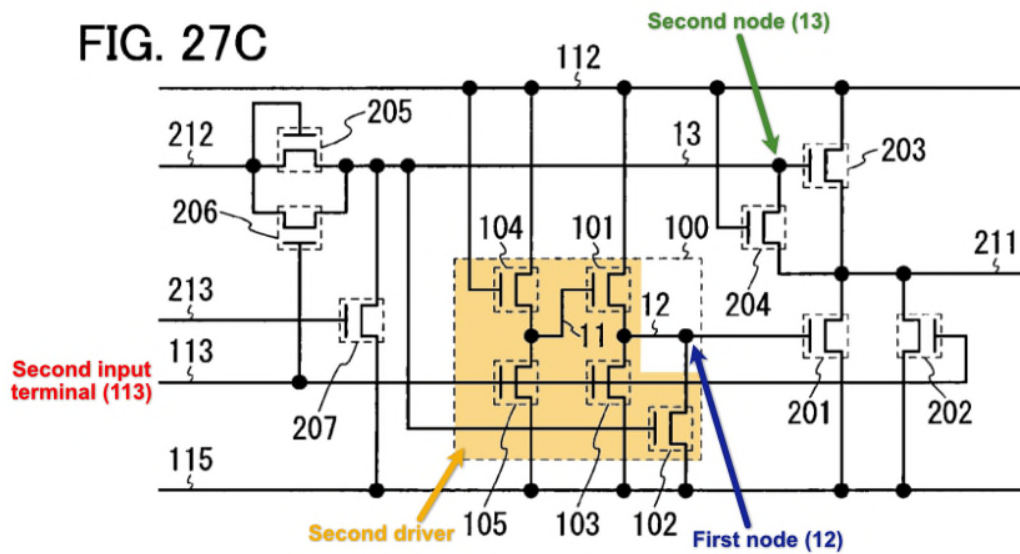
While Kimura’s **first driver** receives inputs in addition to those specified in this claim limit, nothing about claim 1 requires control “in accordance with” *only* the recited signal. Claim 1 is a “comprising” claim and is thus open to other input signals besides those specifically recited. *Genentech, Inc. v. Chiron Corp.*, 112 F.3d 495, 501 (Fed. Cir. 1997). Moreover, Figure 3 of the ’593 patent shows a preferred embodiment of a “first driver 210” that controls the voltage of the second node N2....” Ex. 1001, 5:29-36, 63-65. And, this driver receives input not only from terminals 101-103, but also from node N1 and power supply VDD:



Ex. 1001, Fig. 3; *see also id.*, 5:65-67, 6:16-21 (“first driver 210” is “coupled to the first node N1” and “controls coupling” with “first power supply VDD”). It follows that claim’s 1 first driver can receive signals in addition to those recited. Decl., ¶¶ 166-169. Otherwise, the patent’s preferred embodiment would be read out of the claim scope. *See Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996).

d) Element [1-C]

Figure 27C also includes “a **second driver** to control the voltage of the **first node**”:



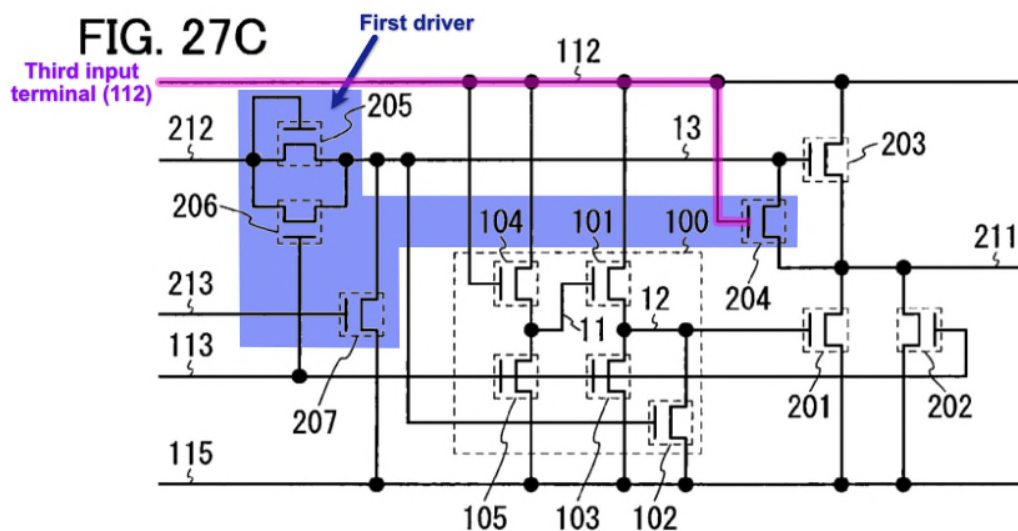
Kimura, Fig. 27C; *see also* Decl., ¶¶ 180-181. Kimura’s circuit 100 (the **second driver**) controls voltage of node 12 (the claimed **first node**) and connected transistor 201. Kimura, [0222], [0226]. This circuit includes a series of transistors 101-105 and “is controlled in response to signals IN1 to IN3.” *Id.*, [0114]-[0115]. Transistors 103 and 105 both have gates connected to wire 113 (the claimed **second input terminal**) and are thus “controlled by the potential” of signal IN2 carried by this wire. *Id.*, [0119], [0121]. “[T]he gate of transistor 102” is “connected to the node 13” (the **second node**) which supplies a controlling “signal IN3.” *Id.*, ¶ [0249]; *see also* Figs. 17B, 21B; Decl., ¶¶ 182-187.

This claim limit also cannot be properly interpreted to require control “in accordance with” *only* the recited signal for the same reasons explained for element [1-B]. Moreover, both claim limits [1-B] and [1-C] use the same term a “driver to

control the voltage of [a] node in accordance with [recited] signal(s).” They presumptively “should be given the same meaning.” *Fin Control Sytems Pty, Ltd. v. OAM, Inc.*, 265 F.3d 1311, 1318 (Fed. Cir. 2001).

e) Element [1-D]

Kimura teaches that “the signal of the **third input terminal** directly controls an on/off operation of a transistor, the transistor included in the **first driver**.” As shown, wiring 112 (the **third input terminal**) is connected to the gate of transistor 204 (part of the **first driver**):



Kimura, Fig. 27C; *see also id.*, [0285]-[0286]; *see also Decl.*, ¶¶ 188-190.

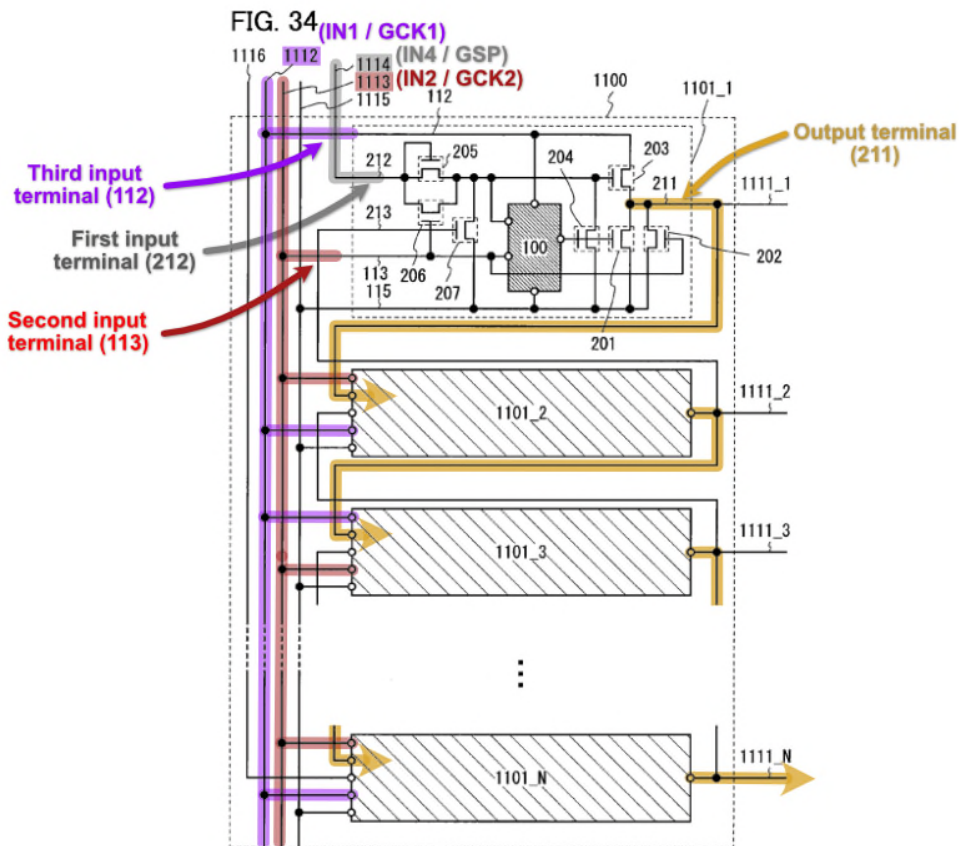
2. Claim 2

Claim 2 depends from Claim 1 and further requires that “the **first input terminal** receives an **output signal** of a previous stage circuit or a start signal,” “the

second input terminal receives a first clock signal,” and “the third input terminal receives a second clock signal.”

As shown in Fig. 34, in the first stage 1101_1 of Kimura’s shift register, “wiring 212” (the claimed first input terminal) is connected to “wiring 1114.” Kimura, [0333]-[0334], [0336]. “A signal GSP is input to the wiring 1114” and servers the same function as “IN4.” *Id.* Signal IN4 “can function as a start pulse.” *Id.*, [0266]. The stages also respectively output “signals GOUT_1 to GOUT_N” (the output signals). *Id.*, [0336]. According to Kimura, the output of a preceding stage is input into subsequent stages in lieu of the separate start pulse: “the signal GOUT_i is input to a flip-flop circuit 1101_i+1” to allow that circuit to “start[] operation.” *Id.*, [0338]. Thus, Kimura teaches a first input terminal receiving either GOUT (the previous stage’s output signal) or IN4/GSP (a start signal). See Decl., ¶¶ 192-200

Next, wiring 112 (the third input terminal) and wiring 113 (the second input terminal) are supplied with “clock signal[s]” IN1 (the second clock signal) and IN2 (the first clock signal). Kimura, [0104], [0109], [0230]-[0232]. In Figure 34 these are depicted as a “signal GCK1 input to the wiring 1112, and a signal GCK2 ... input to the wiring 1113.” *Id.*, [0336].

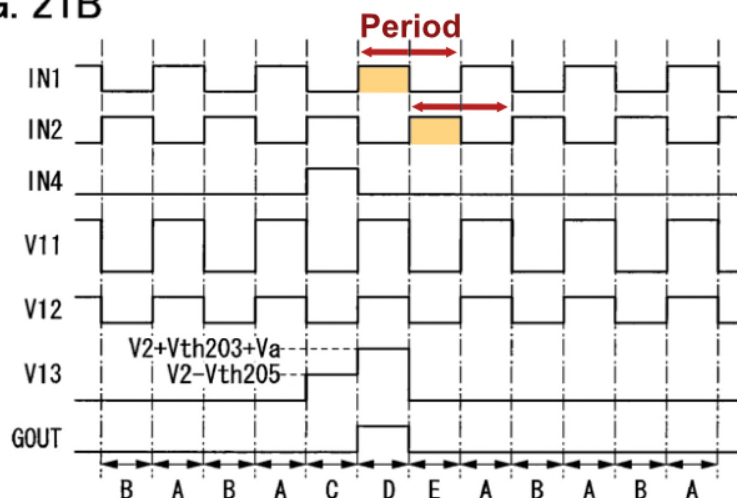


Id., Fig. 34; see also Decl. ¶¶ 201-202.

3. Claim 3

Claim 3 depends from Claim 2 and further requires that “the first clock signal and the second clock signal have the same period and have phases that do not overlap.” Kimura’s first and second clock signals IN2 and IN2 have the same period (red) and active phases that do not overlap (orange):

FIG. 21B

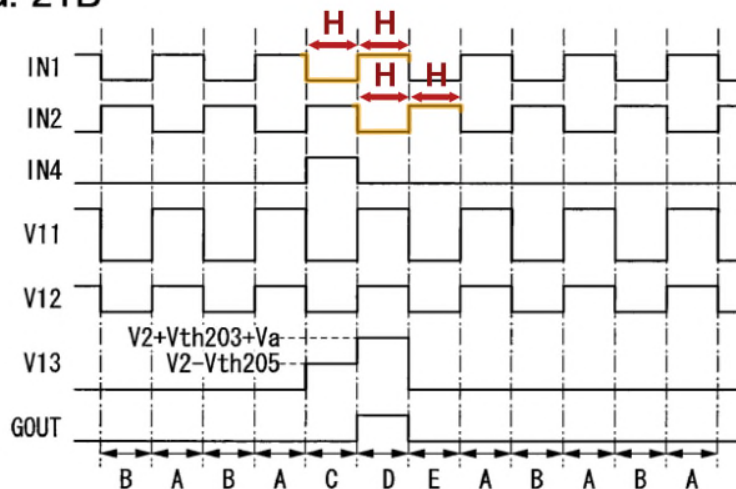


Kimura, Fig. 21B; *see also id.*, [0109], [0231] (IN1 and IN2 are “180° out of phase”); *see also* Decl., ¶¶ 203-218.

4. Claim 4

Claim 4 depends from Claim 3 and requires that “the first clock signal and the second clock signal have a period equal to two horizontal periods 2H and are supplied in different horizontal periods as low signals.” In Kimura, signals are supplied across a series of equal “period[s]” A-E. *See* Kimura, [0016]. Both IN2 and IN1 span two periods and enter a low state in different, subsequent periods:

FIG. 21B

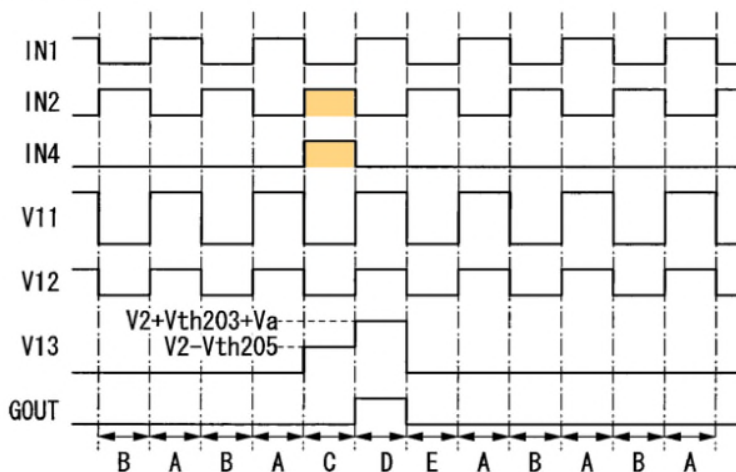


Id., Fig. 21B; *see also* Decl., ¶¶ 219-228; Ex. 1001, Fig. 4 (similarly showing CLK1 and CLK2 spanning two “1H” intervals).

5. Claim 5

Claim 5 depends from Claim 2 and requires that “the start signal is supplied to overlap the first clock signal.” In Kimura, signals IN4 (the start signal) and IN2 (the first clock signal) overlap with the same active high state in period C:

FIG. 21B

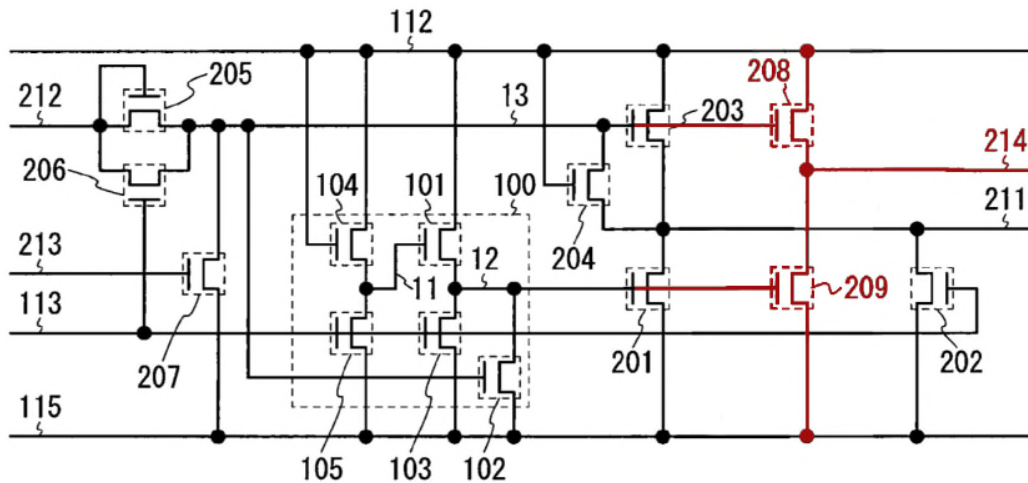


Kimura, Fig. 21B; *see also id.* [0255], [0269]; Decl., ¶¶ 229-234.

6. Claim 6

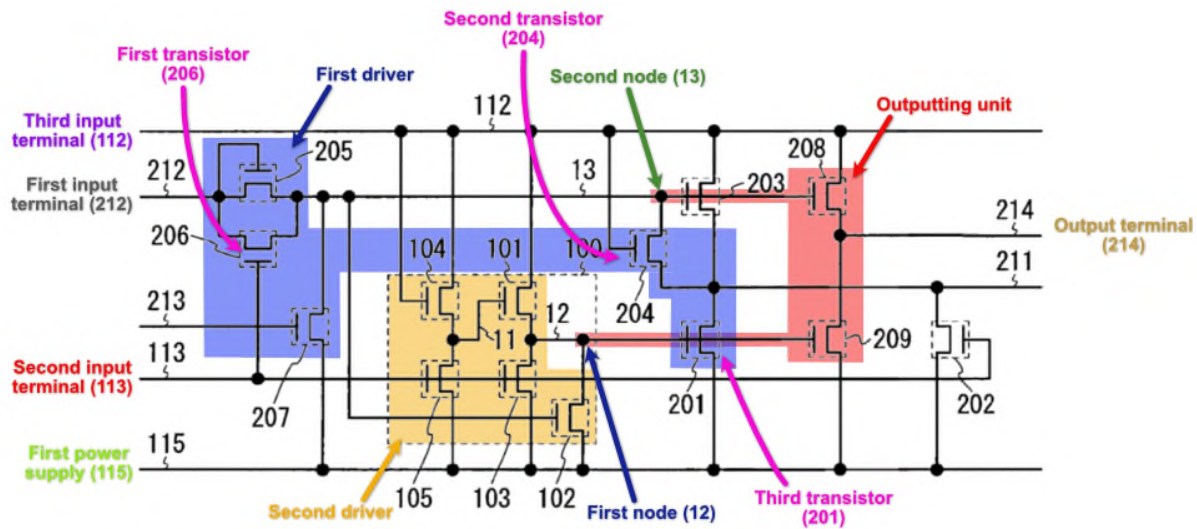
Claim 6 depends from Claim 2. This claim further requires that the “first driver” include “first,” “second,” and “third” transistors arranged in a particular way. This is taught by Kimura when Figure 27C is modified to include the additional features of Figure 31B.

According to Kimura, its devices—including that in Figure 27C—can be provided with additional transistors 208 and 209. Kimura, [0304]. These transistors facilitate generation of a “different” output “signal SOUT” for “input to a semiconductor device in a different stage as a start pulse.” *Id.* Using this signal lowers “delay or distortion.” *Id.* “Transistor 208” has a gate is connected to “node 13” and operates to interconnect “wiring 112” to output “wiring 214.” *Id.*, ¶ [0305]. “Transistor 209” has a “gate connected to the node 12” and interconnects “wiring 115” to output “wiring 214.” *Id.* Thus, transistors 208 and 209 are respectively controlled by the signals applied to nodes 13 and 12, and both serve output functions. *See id.* When these additional transistors are applied to Figure 27C, the following device results (with the added elements shown in red):



See *id.*, Figs. 27C, 31A-B; Decl., ¶¶ 235-240.

As shown below, added transistors 208 and 209 now form the device's **outputting unit** supplying a signal SOUT to wiring 214 (the **output terminal**). These transistors are controlled by the same node 12 (the **first node**) and node 13 (the **second node**) employed by the device of Figure 27C. The device's various inputs 112, 113, 212, and 115 remain the same as in Figure 27C. The **first driver**, however, has expanded to include transistor 201. While one of this transistor's functions is to control output to line 211, it also operates to connect wiring 115 to node 13 via transistor 204. See Kimura, Figs. 27C. This allows for the provision of V_1 from wiring 115 to the node 13 when potential of node 12 and signal IN1 are both high (*i.e.*, during time period A). *Id.*, Figs. 17B, 21B, 31C. The **second driver** is the same as that in Figure 27C:



Decl., ¶ 241-243.

Moving on to the elements added by claim 6, as shown above, the first driver of Figures 27C and 31B includes the required “first transistor [206] between the first input terminal [wiring 212] and the second node [13], the first transistor [206] having a gate electrode coupled to the second input terminal [wiring 113].” *See Id.* It also includes “a second transistor [204] and a third transistor [201] serially positioned between the second node [13] and the first power supply [wiring 115],” that “a gate electrode of the second transistor [204] is coupled to the third input terminal [wiring 112],” and that “a gate electrode of the third transistor [201] is coupled to the first node [12].” *See id.*

A POSITA would have been motivated to apply additional output 214 and transistors 208 and 209 to Figure 27C (and would have expected the application to be successful) both because Kimura itself contemplates this, and because it explains

that doing so allows the signal delay from shift register stage-to-stage to be reduced. *See id.*, ¶¶ 238-239, 244-246. A POSITA would have recognized that this would improve display operation, particularly when a large number of stages are employed. *See id.*

7. Claim 7

Claim 7 depends from Claim 2. This claim requires that the “outputting unit” include not only “fourth” and “fifth” transistors, but also “first” and “second” capacitors. Kimura explains that “[c]apacitors can be additionally provided” along with the transistors in its shift register. Kimura, [0198]. Capacitors can be added in various places. For example, a “capacitor 122” can be connected between wiring 115 and the wiring leading to the gate of a transistor (like transistor 103 in Figure 1A) that generates the circuit’s output signal. *Id.*, [0190]-[0191]. According to Kimura, doing so reduces the “fall time of the signal OUT.” *Id.* Further, a “capacitor 220” can be “connected between the node 13” and output “wiring 211.” *Id.*, [0303]. This similarly serves to “shorten” “the fall time or rise time” of the output signal. *Id.*, [0304].

FIG. 9C

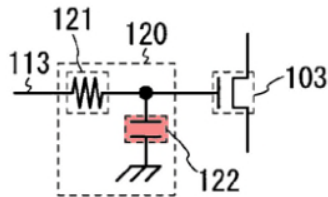
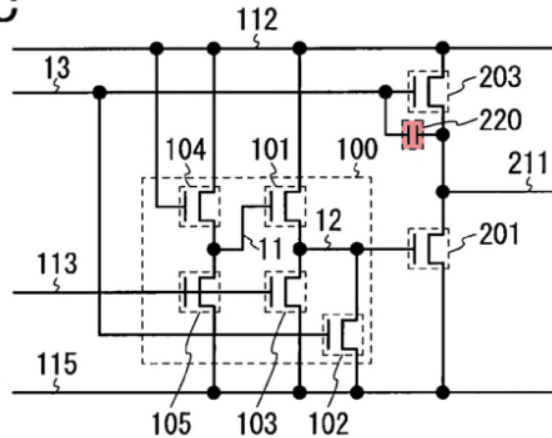
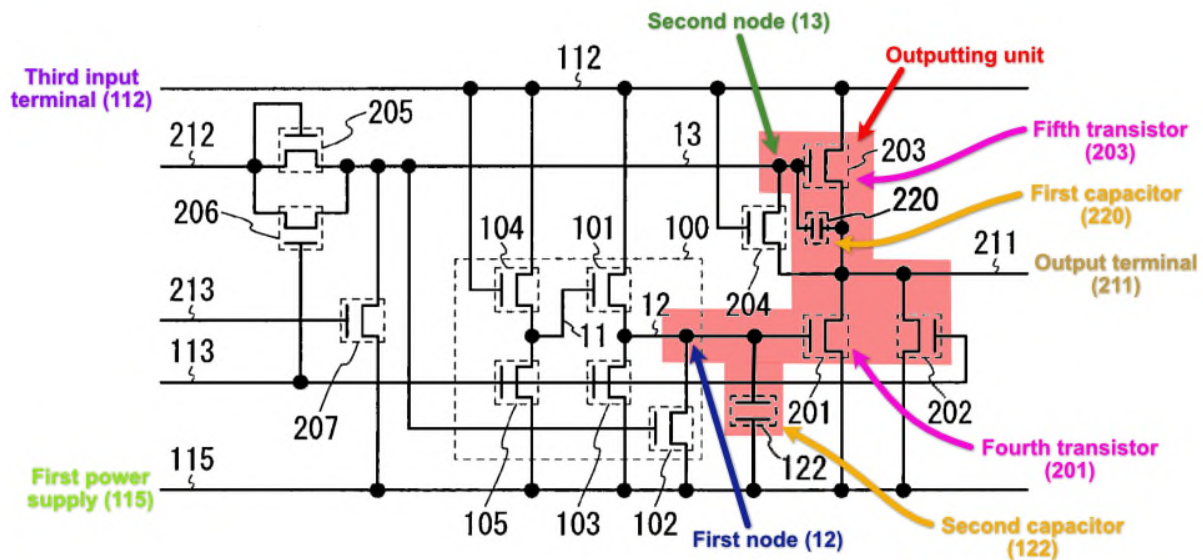


FIG. 30C



Id., Figs. 9C, 30C. The capacitors can be used with any of Kimura's devices, including that in Figure 27C. *See, e.g., id.*, [0304].

When capacitors 122 and 220 are applied to the device of Figure 27C—in particular, to transistors 201 and 203 responsible for generating output—claim 7 is satisfied. The “**outputting unit**” now includes “a **fourth transistor [201]** between the **first power supply [wiring 115]** and the **output terminal [wiring 211]**, the **fourth transistor [201]** having a gate electrode coupled to the **first node [12]**” and “a **fifth transistor [203]** between the **output terminal [wiring 211]** and the **third input terminal [wiring 112]**, the **fifth transistor [203]** having a gate electrode coupled to the **second node [13]**.” Moreover, the “**outputting unit**” also now includes “a **first capacitor [220]** between the **second node [13]** and the **output terminal [wiring 211]**,” and “a **second capacitor [122]** between the **first node [12]** and the **first power supply [wiring 115]**”:



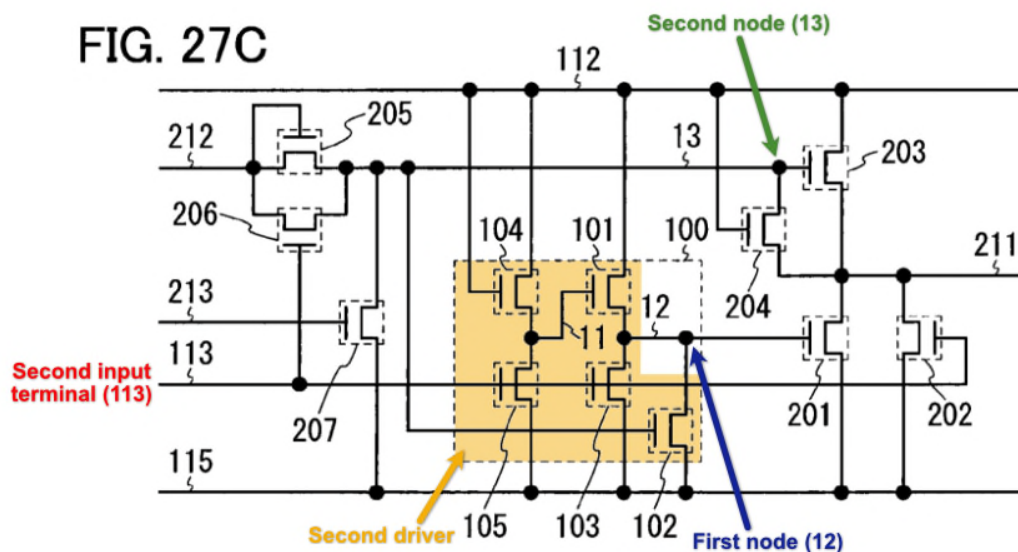
Decl., ¶¶ 247-248, 258-265. A POSITA would have been motivated to include these capacitors (and would have expected the inclusion to be successful) both because Kimura itself contemplates that the capacitors can be employed and because it explains that its device’s output signal is improved when the capacitors are used. *See id.*, ¶¶ 258-261. Further, it was well-known in the art that use of capacitors improves the robustness of, reduces variation of voltage applied to, and can stabilize operation of certain of a shift register’s output transistors. *See, e.g.*, Jeong, ¶¶ [0056]-[0057]. This would have further motivated use of such capacitors with Kimura. *See* Ex. 1003, ¶¶ 248-257, 261, 265-266.

8. Claim 8

Claim 8 depends from Claim 2 and further requires that the “second driver” include both (1) “a sixth transistor between the first node and the second input

terminal, the sixth transistor having a gate electrode coupled to the second node” and (2) “a seventh transistor between the first node and a second power supply, the second power supply having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal.”

As explained when discussing claim 1, the “second driver” shown in Figure 27C of Kimura includes transistors 101-105:



Kimura, Fig. 27C; *see also supra* limit [1-C]; Decl., ¶¶ 267-270. While none of Figure 27C’s transistors are connected in the way the claim requires, Kimura provides a number of design alternatives for use with its devices. For instance, “the first terminal of the transistor 102” can be “connected to the wiring 113” instead of wiring 115. Kimura, [0169]. This, according to Kimura, “suppresse[s]” transistor “deterioration.” *Id.* When so connected, transistor 102 is claimed “sixth transistor”:

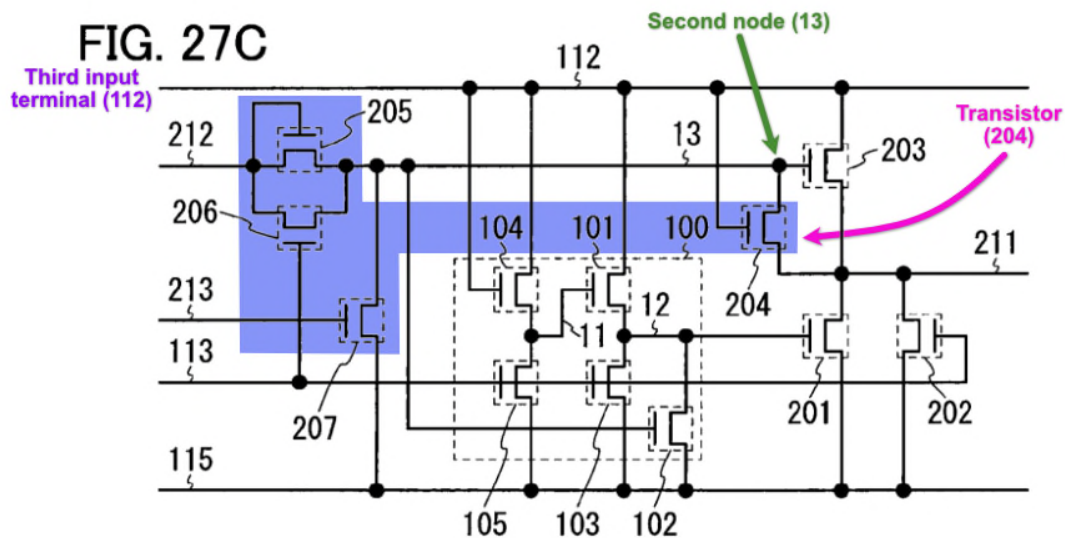
it is located between the “first node” (node 12) and the “second input terminal” (wiring 113). And, its gate is coupled to the “second node” (node 13). *See* Decl., ¶¶ 271-273.

Next, Kimura explains that its devices can employ “a power supply voltage, reference voltage, ground voltage, ground, or negative power supply voltage.” Kimura, [0105]. Moreover, Kimura also teaches that the same device can be provided with multiple different power supply voltages. *See id.*, [0173], [0299]. For instance, in Figure 30A, transistor 103 is connected to a different power supply with a different voltage (wiring 115B) than output transistor 201 (wiring 115D). *See id.*, Fig. 30A. When so configured, transistor 103 is the claimed “seventh transistor”: it is located between the “first node” (node 12) and “second power supply” (wiring 115B), and has its gate connected to “second input terminal” (wiring 113). *See* Decl., ¶¶ 274-275. And, again, Kimura explains that wiring 115B can be supplied with a lower voltage supply (such as a “power supply voltage” that is relatively “negative”). Kimura, [0105]; *see also id.*, [0162], [0170] (referencing supply of a “H-level signal to the first terminal of ... transistor 103”); Decl., ¶¶ 276-278.

9. Claim 14

Claim 14 depends from Claim 1 and requires that “the transistor controls the voltage of the second node according to the on/off operation thereof.” The referenced “transistor” is the “transistor” of claim 1 that is controlled by the “third

input terminal” and is “included in the first driver.” Kimura’s transistor 204 satisfies these limitations: It is part of the first driver, and receives a signal IN1 from wiring 112 (the third input terminal). This transistor is also connected to node 13 (the second node). See Kimura, [0286].



Id., Fig. 27C; see also Decl., ¶¶ 279-285 .

10. Independent Claim 15

a) [15-PRE]

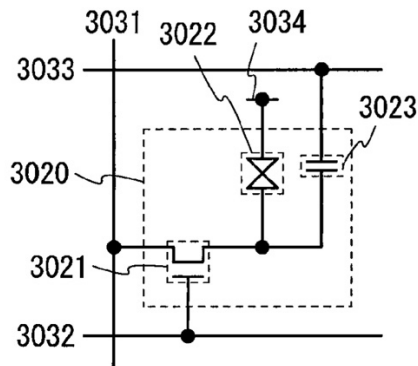
Claim 15 is directed to “[a]n organic light emitting display.” To the extent limiting, this is what Kimura teaches. See, e.g., Kimura, [0320] (Kimura’s “shift register” is part of a “display device”); [0388] (the display can employ “organic EL element[s]”); Decl., ¶¶ 287-289.

b) Element [15-A]

Kimura teaches “pixels positioned in regions partitioned by scan lines and

data lines.” Kimura’s display includes a “circuit 1001, a circuit 1002, a circuit 1003, a pixel portion 1004, and a terminal 1005.” Kimura, [0321]. The pixels are arranged in multiple “row[s]” and “columns.” *Id.*, [0349]. Figure 33E depicts a single “pixel portion.” *Id.*, [0330].

FIG. 33E



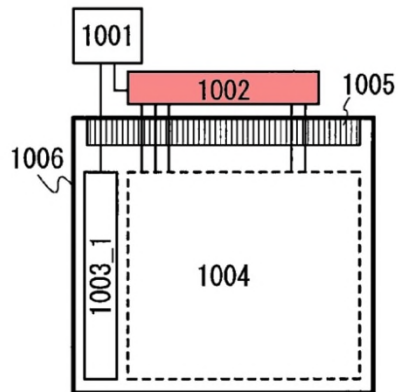
Id., Fig. 33E. “[P]ixel 3020” is surrounded by and connected to both a “wiring 3031” and “wiring 3032.” *Id.*, [0331]. “A video signal is input ... to the wiring 3031.” *Id.* This is the claimed “data line.” See Decl., ¶¶ 291-292. “A scan signal ... is input ... to the wiring 3032.” Kimura, [0331]. This is the claimed “scan line.” See Decl., ¶ 292. While Figure 33E shows only one pixel, a POSITA would understand that Kimura’s display is formed by an array or matrix of such pixels surrounded by contiguous video signal and scan lines. *Id.*, ¶¶ 293-294.

c) Element [15-B]

Kimura teaches “a data driver for supplying data signals to the pixels through the data lines.” Kimura’s display includes a “circuit 1002” that “functions ... as a

driver circuit” for “supplying a video signal to the pixel portion 1004.” Kimura, [0323].

FIG. 33A

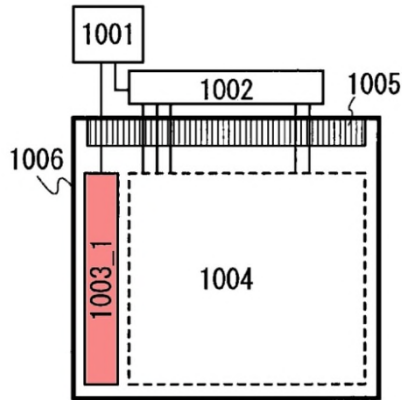


Id., Fig. 33A; *see also* Decl., ¶¶ 295-297.

d) Element [15-C]

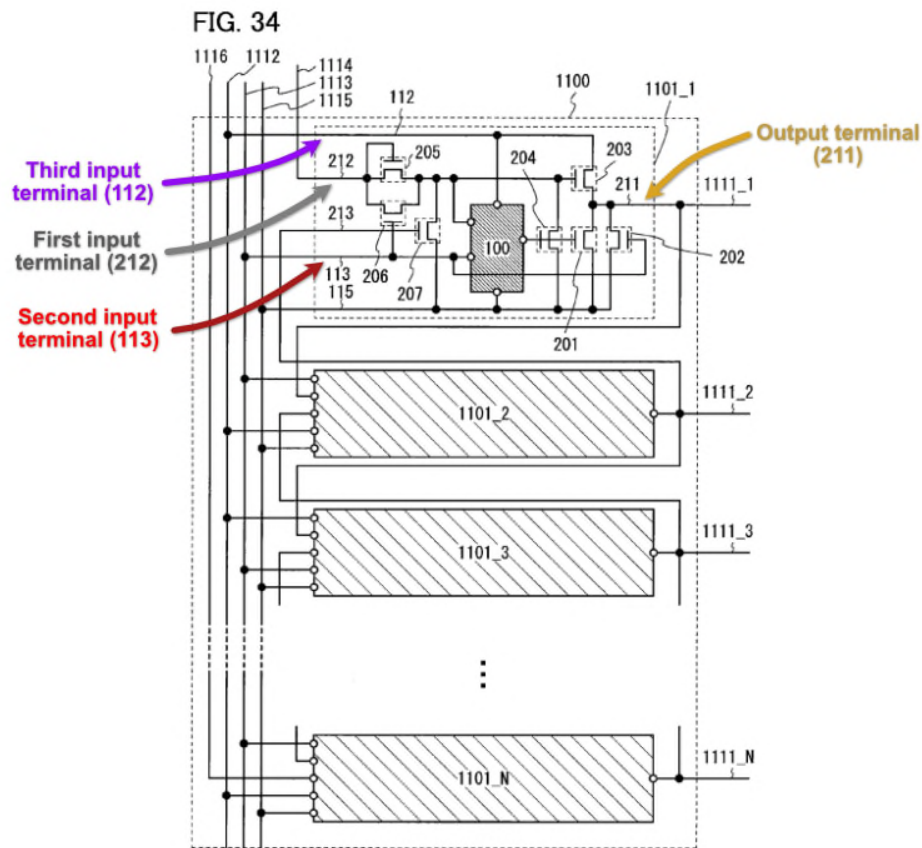
Kimura teaches “a scan driver for supplying scan signals to the pixels through the scan lines, the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals and having a first input terminal, a second input terminal, a third input terminal, and an output terminal.” Kimura’s “circuit 1003_1” is a “scan line driver” for “supplying a scan signal ... to the pixel portion 1004.” Kimura, [0324].

FIG. 33A



Id., Fig. 33A; *see also* Decl., ¶¶ 299-301.

Next, a “shift register circuit” like that shown in Figure 34 “can be included in “the circuit 1003_1.” Kimura, [0333]. This circuit includes stages of “flip-flop circuits 1101_1 to 1101_N.” *Id.*, [0334]. Each stage output signals “GOUT_1” to “GOUT_N” to “wirings 1111_1 to 1111_N.” *Id.*, [0335]-[0336]. Any of the circuits of “Embodiments 1 or 2” can be used to form the stages. *Id.*, [0333]. Finally, as shown below, each of stage of Kimura’s shift register receives input from wiring 212, 113, and 112 (the first input terminal, second input terminal, and third input terminal) and provides output to wiring 211 (the output terminal):



Id., Fig. 34; see also *supra* element [1-PRE]; Decl., ¶¶ 302-308 .

e) Elements [15-D]-[15-G]

Elements [15-D]-[15-G] are the same as Elements [1-A]-[1-D]. Thus, Kimura teaches these elements for the same reasons discussed for claim 1. *See supra* claim 1; Decl., ¶¶ 309-317.

11. Claim 16

Claim 16 depends from Claim 15 and additionally requires that “a clock signal supplied to the third input terminal is used as the scan signal.” Per Kimura, “signal IN1 is input” to “wiring 112” (Kimura’s *third input terminal*). Kimura, [0104]. “[A] clock signal is used as the signal IN1.” *Id.*, [0109], [0230]-[0232]. And, in a “period

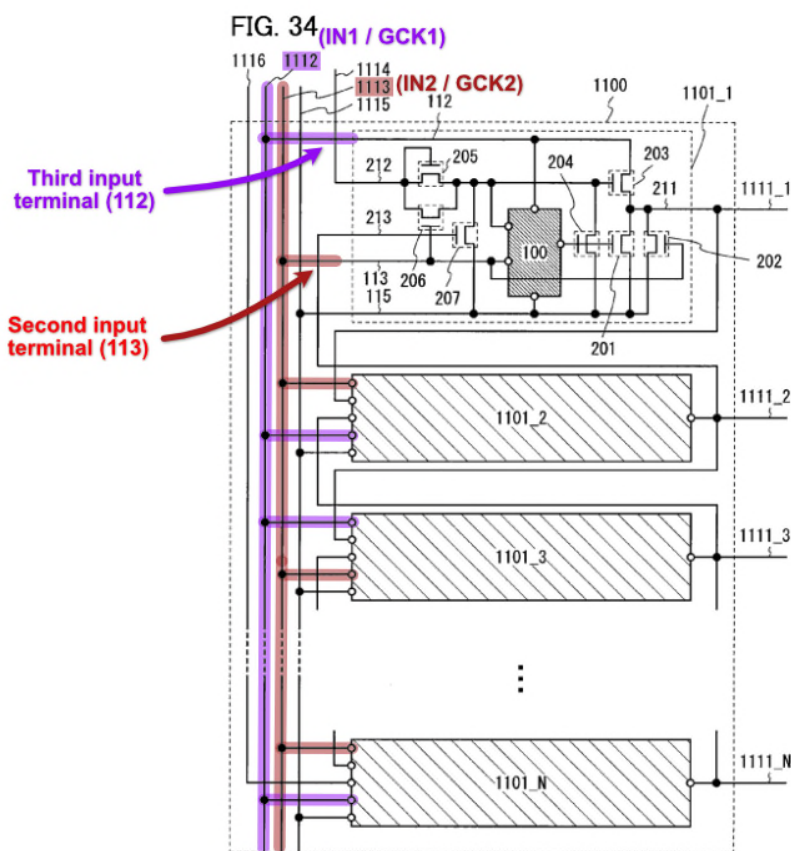
D” of the device’s operation, “potential of the wiring 112”—which has changed to “the signal IN1 at an H level”—is “supplied to the wiring 211” as an output signal. *Id.*, [0256]; *see also supra* discussion of element [1-PRE]. This output signal is employed as a display’s “scan signal.” Kimura, [0324]; Fig. 27C, 34; *see also* Decl., ¶¶ 319-325.

12. Claim 17

Claim 17 depends from claim 16 and adds the same limit as claim 2. Kimura teaches what this claim requires for the same reasons explained for that claim. *See supra* claim 2; Decl. ¶¶ 326-329.

13. Claim 18

Claim 18 depends from Claim 17 and requires that the “second input terminals of odd stage circuits receive a first clock signal and third input terminals of odd stage circuits receive a second clock signal” and “second input terminals of even stage circuits receive the second clock signal and third input terminals of even stage circuits receive the first clock signal.” This is taught by Kimura. As shown in Figure 34, in the odd stage circuits (*e.g.*, circuits 1101_1, 1101_3, etc.), wiring 113 (the **second input terminal**) receives IN2/GCK2 (the **first clock signal**) and wiring 112 (the **third input terminal**) receive IN1/GCK1 (the **second clock signal**). The even stage circuits (*e.g.*, circuits 1101_2, etc.) reverse the input signal-to-wiring correlation:



Kimura, Fig. 34; *see also id.*, [0335] (explaining that the signals to which “wiring 112 and the wiring 113 are connected are inversed” in the odd/even stages); Decl., ¶¶ 330-335.

14. Claim 19

Claim 19 depends from claim 18 and adds the same limit claim 3. Kimura teaches what this claim requires for same reasons explained for that claim. *See supra* claim 3; Decl., ¶¶ 336-339.

15. Claim 20

Claim 20 depends from claim 18 and adds the same limit as claim 6. Kimura

teaches what this claim requires for same reasons discussed for that claim. *See supra* claim 6; Decl., ¶¶ 340-343.

16. Claim 21

Claim 21 depends from claim 18 and the same limit as claim 7. Kimura teaches what this claim requires for same reasons discussed for that claim. *See supra* claim 7; Decl., ¶¶ 344-347.

17. Claim 22

Claim 22 depends from claim 18 and adds the same further limit as claim 8. Kimura teaches what this claim requires for the same reasons discussed above for that claim. *See supra* claim 8; Decl., ¶¶ 348-351.

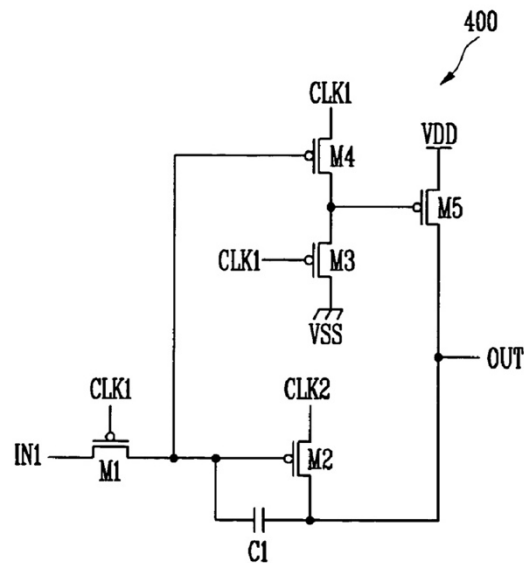
18. Claim 25

Claim 25 depends from Claim 18 and requires that “the scan signal of the previous stage circuit or the start signal supplied to the first input terminal overlaps the clock signal supplied to the second input terminal.” This is taught by Kimura for the same reasons discussed for claim 5: Kimura’s “start signal supplied to the first input terminal” (signal IN4 supplied to wiring 212) overlaps the “clock signal supplied to the second input terminal” (signal IN2 supplied to wiring 113). *See supra* claim 5; Decl., ¶¶ 352-356.

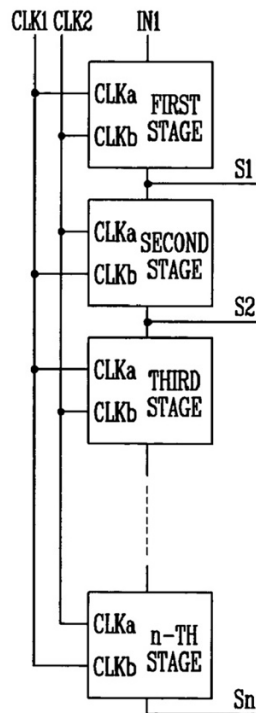
B. GROUND 2: Shin and Sasaki Render Claims 1-6, 8, 14-20, 22, and 25 Obvious

Shin relates to a “scan driving circuit” for an “organic light emitting display.”

Shin, [0003]. Shin teaches an improved “scan driving circuit” design that “remov[es] a current flow path of a static current from a stage of each unit” to reduce power consumption. *Id.*, [0016]. Figure 11 is an example:



Id., Fig. 11 (excerpted). Unlike the circuit of Figure 2, this circuit no longer has multiple VDD to ground paths. *See id.* It continues, however, to function as a scan driving circuit. According to Shin, the circuit’s transistors are opened and closed by start signal IN1 and clock signals CLK1 and CLK2 for purposes of supplying either a “high” or “low” signal to OUT. *See id.*, [0075], [0099]-[0107]; Fig. 12. A series of such circuits are arranged one after another in stages to supply signals to a display’s scan lines:

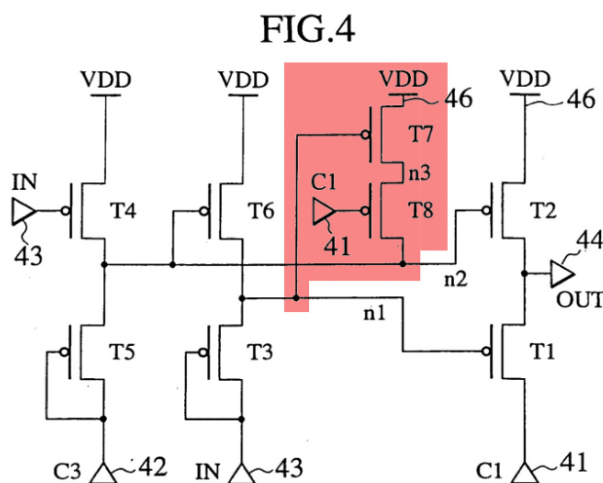


Id., Fig. 10 (excerpted); see also Fig. 4.

While a POSITA would have considered Shin’s circuit beneficial due to its reduced power consumption, they also would have recognized that it is subject to a potential problem. See Decl., ¶¶ 364-369. This is highlighted by Sasaki. Sasaki—like Shin—relates to a “shift register” circuit for a “display device.” Sasaki, [0003]. Sasaki’s circuit includes “transistors” with gates connected to a “control electrode.” *Id.*, [0011]. This allows the circuit to apply either a high or low signal to an output terminal. See *id.*, Fig. 4. According to Sasaki, if either transistor’s “control electrode” enters a “floating state” because “the high voltage VDD is not supplied,” it is possible that the transistor may be “reversed” (*i.e.*, open when it is supposed to be closed). *Id.*, [0042]. This can result in unwanted mixing of high and low signals

at the output terminal. *Id.*

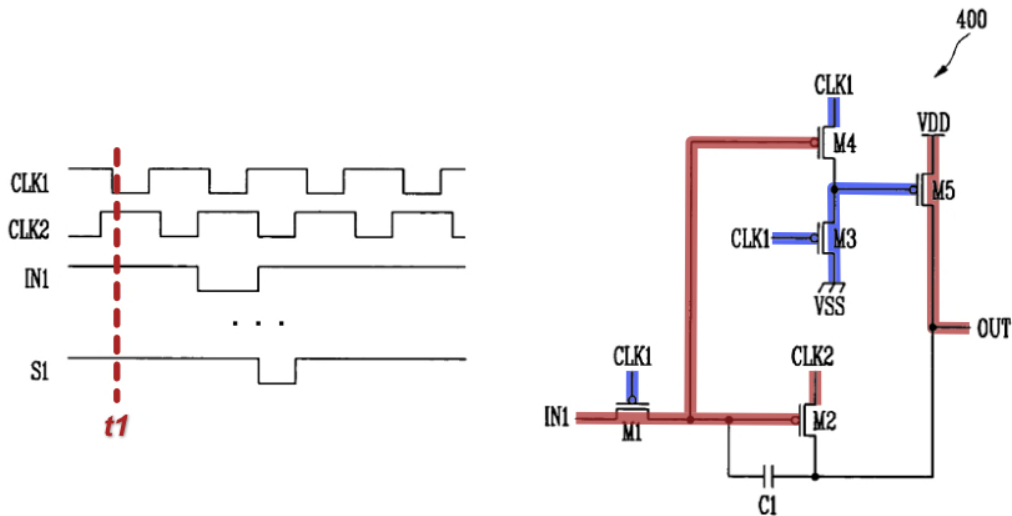
To address this problem, Sasaki employs an “anti-reversal circuit” like that in Figure 4. *Id.*, [0042].



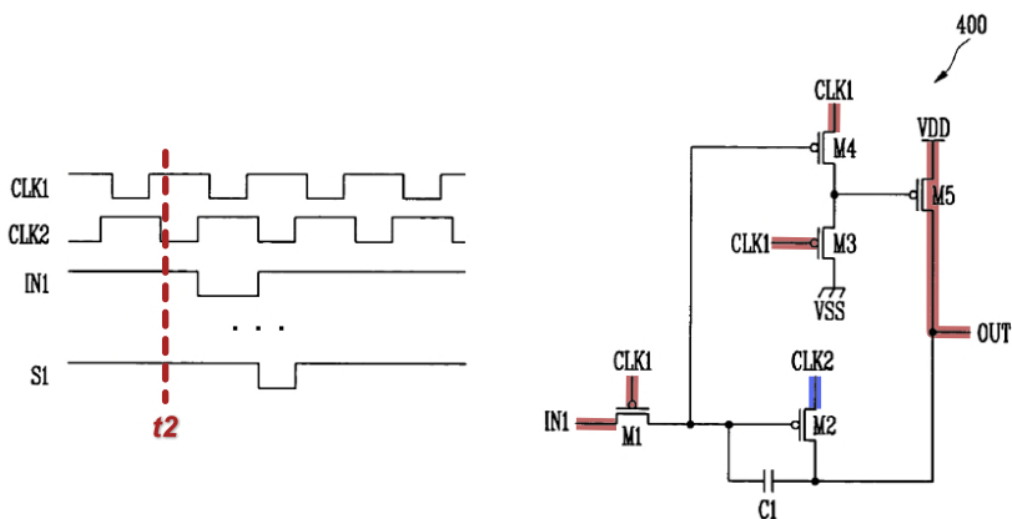
Id., Fig. 4. “The anti-reversal circuit includes a seventh transistor T7 and an eighth transistor T8.” *Id.*, [0042]. These two transistors operate to keep transistor T2 closed by supplying a high VDD signal to transistor T2’s gate when transistor T1 is open and C1 is supplying a low signal to OUT. *See Decl.*, ¶¶ 370-373. This ensures that the high VDD signal is not inadvertently supplied to OUT along with the low signal. *See id.*, ¶¶ 374-378.

A POSITA would have recognized that Shin’s scan driving circuit is subject to a problem like that identified by Sasaki. *See id.*, ¶ 379. The below demonstratives—generated using Figures 9 and 11 of Shin—provide an example. In period **t1**, CLK1 is low (blue), opening transistors M1, M3, and M5. CLK2 is

high (red). IN1 is also high, closing transistor M2. A high signal is supplied to OUT from VDD:



Id., Figs. 9, 11 (excerpted); *see also* Decl., ¶¶ 380-382. Here, M2 is closed by an applied signal and is not subject to a floating potential. This changes in period $t2$. Now, CLK1 is high and CLK2 is low. This closes transistors M1 and M3. No signal is applied to the gate of transistor M5, so this transistor remains open and a high signal continues to be supplied to OUT from VDD:

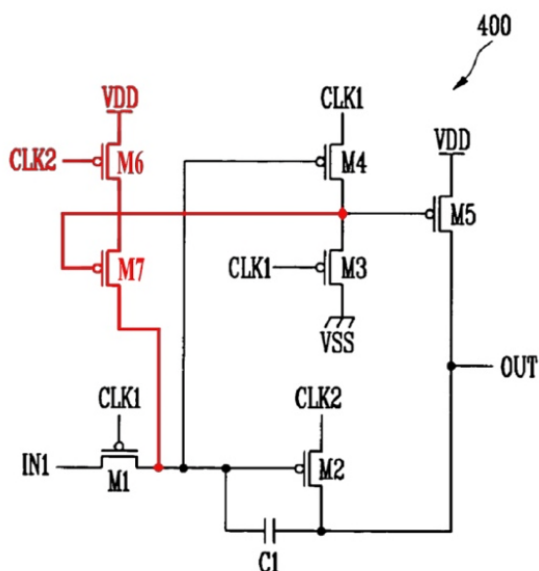


Shin, Figs. 9, 11 (excerpted); *see also* Decl., ¶ 383. For OUT to be high as intended, however, transistor M2 must remain closed (otherwise, a low signal CLK2 will also be supplied). But, the electrode leading to transistor M2's gate is no longer being supplied with a signal and is now floating. *See id.*, ¶ 384. This creates the potential of reversal: interference and spurious signals could cause the transistor to inadvertently open. *See id.*

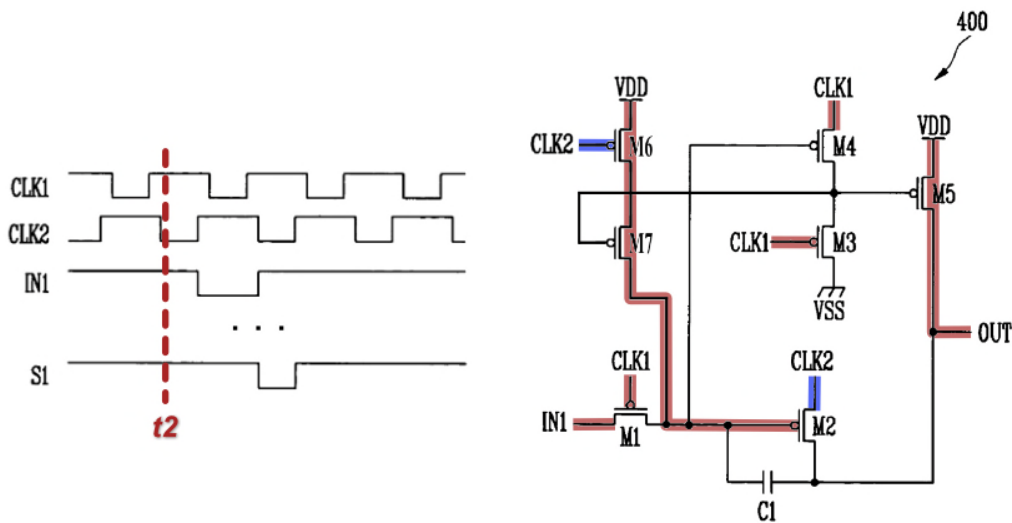
Shin does include a capacitor C1 electrically connected to transistor M2's gate. But, a POSITA would have recognized that this capacitor is not sufficient by itself to address Shin's anti-reversal problem. In subsequent steps, this capacitor is charged by an applied low-level signal to keep transistor M2 open after the low-level signal ceases. *See* Shin, [0099]. But, in period *t2*, the capacitor has not accumulated significant charge that would allow it to guarantee reversal protection. *See* Decl., ¶ 385. Further, the lowering of the potential at transistor M2's gate due to the transition of CLK2 to low further minimizes the capacitor's effect. *See id.*, ¶¶ 383-386, 389. A POSITA would have recognized that Sasaki's anti-reversal circuit accounts for the lack of robustness of the capacitor and ensures that transistor M2 is reliably kept closed. *See id.*, ¶¶ 387-389. Indeed, recognizing the lack of robustness of capacitors, numerous prior art references employ **both** capacitors and transistors to control node voltage. *See, e.g.*, Ex. 1016, Fig. 1A (capacitors 133-234 and transistors 226-227 all connected to node N226); Kimura, [0286], [0302]-[0303]

(both a “transistor 204” and “capacitor 220” control node 13 potential).

A POSITA would have recognized that applying Sasaki’s anti-reversal circuit to Shin would eliminate the reversal problem. The below modified version of Shin’s Figure 11 circuit shows how a POSITA would have added Sasaki’s anti-reversal circuit, with the added elements shown in red:



See Decl., ¶ 390. In operation, added transistors M6 and M7 operate to supply a high VDD signal to transistor M2’s gate to prevent the transistor from opening and inadvertently supplying a low CLK2 signal to OUT at a time when the circuit’s output is intended to be high:

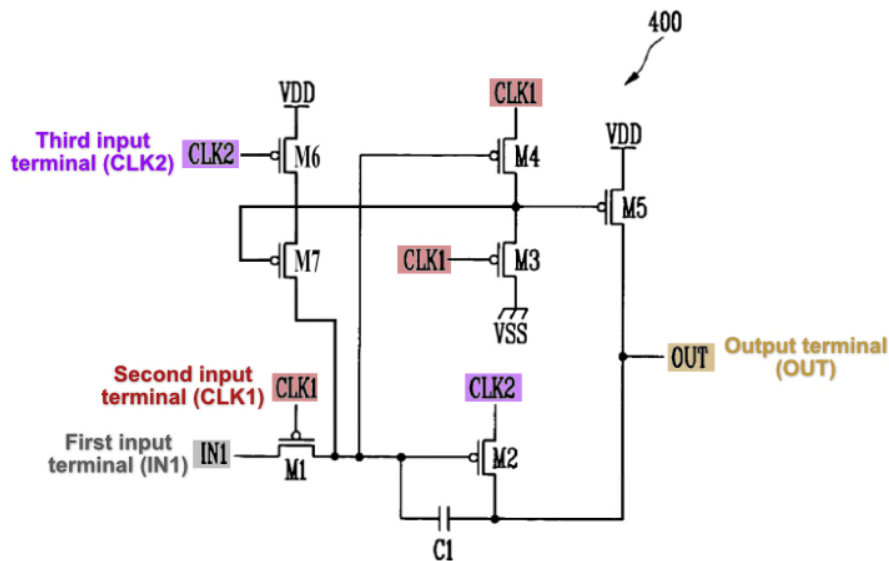


See *id.*, ¶ 390. Other than the above application of a high signal to keep transistor M2 closed during period t_2 , the rest of Shin’s operation remains the same. See *id.*

A POSITA would have been motivated to apply Sasaki’s anti-reversal circuit to Shin. Again, because there are periods of time where Shin’s transistor M2—which is responsible for controlling application of a low signal to OUT—has a floating potential, this transistor is subject to inadvertent reversal. See *id.*, ¶¶ 363, 389-391. A POSITA would have recognized that applying Sasaki’s anti-reversal circuit eliminates this, avoids the inadvertent application of a low signal to OUT, increases the fidelity of signal output by Shin’s circuit, and reduces malfunction and error. See *id.* This would in turn improve display performance. See *id.* Moreover, a POSITA would have recognized that transistors arranged as a logical AND—as transistors M6 and M7 are above—were routinely used to control node potential decades before the ’593 patent. See, *e.g.*, Ex. 1016, 1:8-9, 3:32-36, Fig. 1A (“shift

register” with in-series transistors 226-227 controlling node N226’s potential); Ex. 1017, Abstract, 7:26-35, Fig. 6 (“shift register” with in-series transistors Q₁₀₆-Q₁₀₇ controlling node N13’s potential); Ex. 1018, 5:11-17; Fig. 9 (circuit with in-series transistors Q_{73A}-Q_{73B} controlling potential of node leading to transistor Q₇₀). Given this, a POSITA would have considered use of these transistors with Shin to amount to nothing more than a routine design choice. *See* Decl., ¶¶ 391-396.

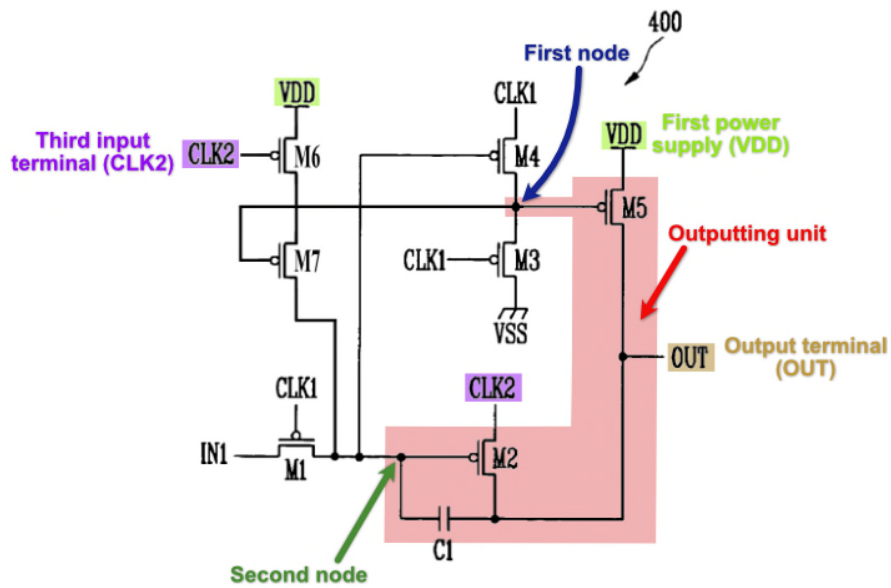
A POSITA would also have had a reasonable expectation of success. *See id.*, ¶¶ 363, 390-396. Sasaki’s anti-reversal circuit is specifically designed for use with circuit like that taught by Shin. *See* Sasaki, [0003]. And, this type of anti-reversal circuit was routinely used. *See* Decl., ¶¶ 363, 390-396. While Sasaki does use its anti-reversal circuit to keep its transistor T2 from opening and inadvertently supplying a high VDD signal to OUT at a time when C1 is supplying a low signal (*see generally* Sasaki, Figs. 4-5), a POSITA would not consider its teachings to be so limited. Instead, a POSITA would have understood that any transistor that can be inadvertently opened resulting in improper supply of a conflicting signal can (and obviously should) be protected by an anti-reversal circuit. *See* Decl., ¶¶ 387-390. It would also make little sense to bodily graft Sasaki’s anti-reversal circuit onto Shin for purposes of keeping transistor M5 (which controls the supply of high VDD to OUT) closed. When a low CLK2 signal is supplied to OUT through transistor M2, transistor M5’s gate is not floating and is instead kept closed by a high CLK1 signal



Decl., ¶ 399. According to Shin, the above circuit operates as a stage of a “scan driv[er]” for a “display.” Shin, [0003]. As shown, each “stage[]” includes a terminal that “receive[s]” a “first input signal IN1” (the claimed **first input terminal**), along with “first clock terminal CLKa” (the **second input terminal**) and “second clock terminal CLKb” (the **third input terminal**) that respectively receive “first and second clock signals CLK1 and CLK2.” *Id.*, [0072]-[0075], [0088]-[0090]. And, an “output line” from each “stage[]” of the “scan drive unit” “provide[s] a selection signal to respective pixels defining” a display’s “pixel array.” *Id.*, [0070], [0072]. This selection signal is generated on “the output line OUT” (the **output terminal**). *Id.*, [0089]; see also Decl., ¶¶ 400-402.

b) Element [1-A]

Shin and Sasaki teach the claimed “**outputting unit**”:



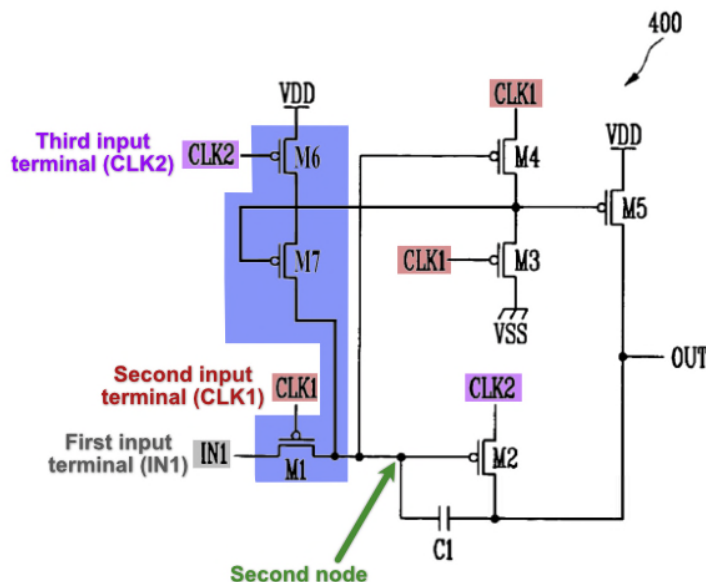
Decl., ¶ 404. Transistors M2 and M5 are responsible for generating output. More particularly, in each shift register stage, a “PMOS transistor M2 is coupled with a second clock terminal” receiving CLK2 (the claimed **third output terminal**) “and an output line OUT” (the **output terminal**). Shin, [0088]. This transistor’s gate is coupled to a point where lines leading to or from the output of transistor M1, capacitor C1, and the gate of transistor M4 intersect (the **second node**). *Id.* Another “PMOS transistor M5 is coupled between a first power supply VDD” (the **first power supply**) “and the output line OUT.” *Id.*, [0089]. Its gate is connected to a “first node N1” (the **first node**) located between transistors M3 and M4. *Id.*

In operation, these two transistors allow the stage to output either a high or low level signal from OUT. *See id.*, [0075]. More particularly, during a “precharge period,” input and clock signals are provided such that “first node N1” is supplied

with a “low-level signal” opening transistor M5 allowing high “first power supply VDD” to be “output through an output terminal OUT.” *Id.*, [0099]. During an “evaluation period,” signals are supplied to turn off transistors M1, M3, and M5. *Id.*, [0099]-[0107]. Capacitor C1 allows “transistor M2” to maintain an open state allowing the “stage [to] output[] a low-level” CLK2 “signal.” *Id.*, [0103], [0105]; *see also id.*, Fig. 12. In sum, transistors M2 and M5 of Shin’s **outputting unit** allow either VDD (the **first power supply**) or CLK2 (the **third input terminal**’s signal) to be supplied to OUT (the **output terminal**) depending on the voltage of Shin’s **first node** or **second node**. *See Decl.*, ¶¶ 406-414.

c) Element [1-B]

Shin and Sasaki teach “a **first driver** to control the voltage of the **second node**”:



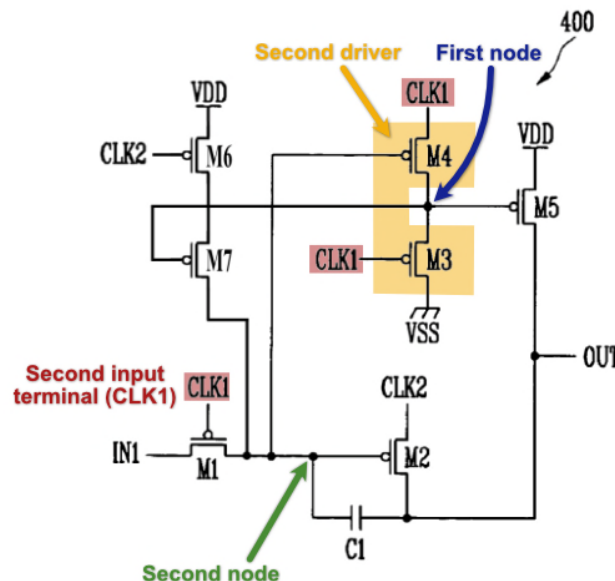
Id., ¶ 415. As shown, Shin includes a “first transistor M1.” Shin, [0088], [0105].

This transistor is “controlled by the first clock signal CLK1” (the signal supplied by

the **second input terminal**), and operates to “transfer[]” “input signal IN1” (the signal supplied by the **first input terminal**) to the node (the **second node**) leading to transistor M2’s gate. *Id.*, [0088], [0098]. Further, transistors M6 and M7—the anti-reversal circuit added following Sasaki’s teachings—supplement transistor M1’s operation by receiving an input signal from CLK2 (the signal supplied by the **third input terminal**) and controlling the potential of the same node (the **second node**) for purposes of keeping transistor M2 closed when CLK2 is low but OUT is intended to be high. *See* Sasaki, [0042]; *see also* Decl., ¶¶ 416-420. Together, transistors M1, M6, and M7 form the **first driver**. *See id.*, ¶ 421.

d) Element [1-C]

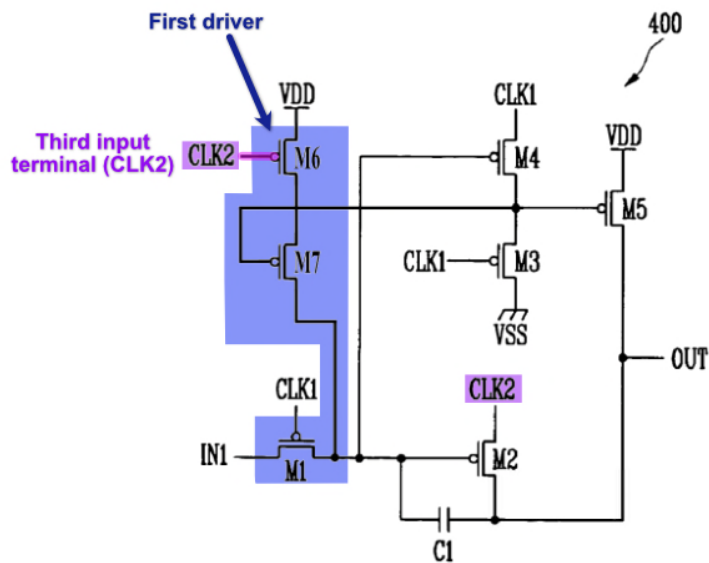
Shin and Sasaki teach “a **second driver** to control the voltage of the **first node**”:



Id., ¶ 423. Here, Shin includes a “third PMOS transistor M3 ... coupled between a second power supply VSS and a first node N1” (the claimed **first node**). Shin, [0088]. This transistor’s gate receives input from and is controlled by “the first clock terminal” supplying CLK1 (the **second input terminal**). *Id.* “[F]ourth PMOS transistor M4 is coupled between the first clock terminal” and “the first node N1.” *Id.* This transistor’s gate is connected to the same node (the **second node**) as the “output terminal of the first PMOS transistor M1.” *Id.* Node N1 (the **first node**) is “coupled” to the “gate terminal” of transistor M5. *Id.* In operation, Shin employs CLK1 and the signal received from its second node to control transistors M3 and M4. *See id.* These transistors in turn control the potential of node N1 for purposes of opening/closing transistor M5. *See id.*, [0098]-[0103]. Thus, transistors M3 and M4 thus form Shin’s **second driver**. *See Decl.*, ¶¶ 424-430.

e) Element [1-D]

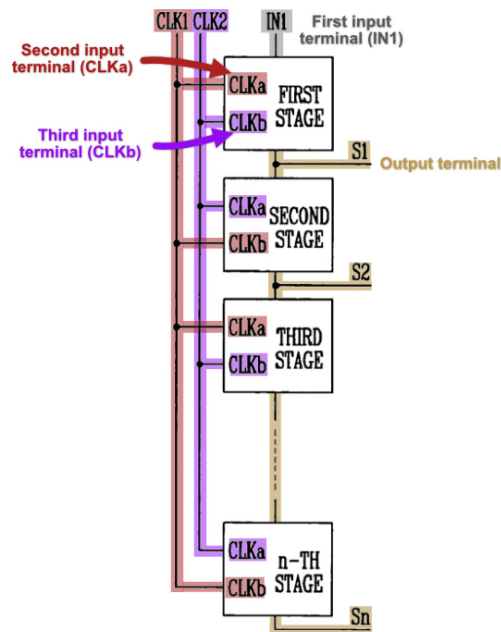
In Shin and Sasaki, “the signal of the **third input terminal** directly controls an on/off operation of a transistor, the transistor included in the **first driver**.” This is shown below. As required, CLK2 (the signal supplied by the **third input terminal**) is directly coupled to the gate—and thus controls the on/off functionality—of transistor M6 (one of the transistors in the **first driver**):



Id., ¶ 431.

2. Claim 2

Claim 2 depends from Claim 1 and further requires that “the first input terminal receives an output signal of a previous stage circuit or a start signal,” “the second input terminal receives a first clock signal,” and “the third input terminal receives a second clock signal.” This is what Shin and Sasaki teach:



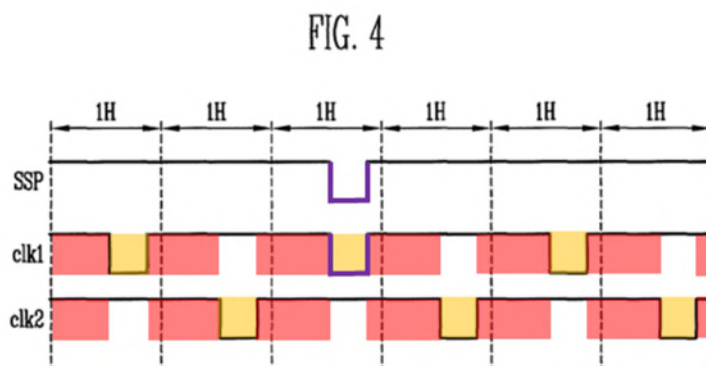
Shin, Fig. 10 (excerpted). More specifically, Shin’s first stage receives a “first input signal IN1” (the claimed start signal). *Id.*, [0073]. All the subsequent stages receive the “output signals” of the previous stages (the claimed output signal) as an “input signal.” *Id.* As shown in Figures 9 and 12, this signal operates as a start pulse. *See id.*, Figs. 9, 12; *see also id.*, [0010] (“conventional scan driving circuit[s]” are supplied “with a start pulse SP”); [0098] (IN1 starts the “precharge period” of operation). “Further, each stage of the scan drive unit ... includes a first clock terminal CLKa and a second clock terminal CLKb” receiving “clock signals CLK1 and CLK2.” *Id.*, [0074]. In the odd stages, terminal CLKa (the second input terminal) receives CLK1 (the first clock signal), while CLKb (the third input terminal) receives CLK2 (the second clock signal). *Id.*; *see also id.*, [0090]. The

even stages reverse the terminal-to-signal correlation. *Id.*, [0074], [0090]; *see also* Decl., ¶¶ 434-443.

3. Claim 3

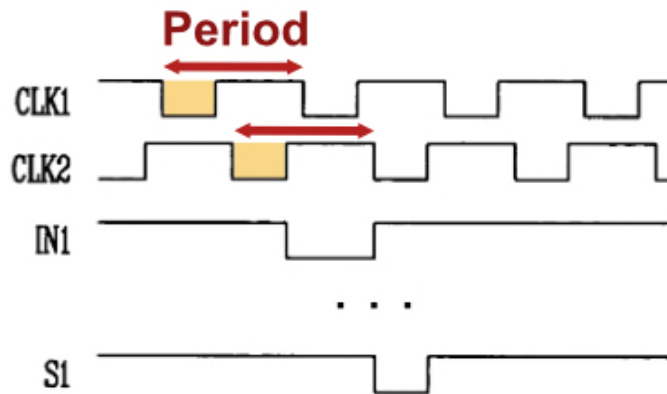
Claim 3 depends from Claim 2 and requires that “the first clock signal and the second clock signal have the same period and have phases that do not overlap.”

A POSITA would understand the term “phases” in this limit to refer to the signals’ active phases. Decl., ¶¶ 204-216. This is what the ’593 patent discloses. The patent’s embodiments employ pMOS transistors turned on by a low voltage. *See* Ex. 1001, 6:39-40. As shown in Figure 4 below, the low, active phases (orange) of the clk1 and clk2 signals—the “on” logic state in this example—do not overlap. However, the high, inactive phases (red) are overlapping:



Id., Fig. 4 (partial); *see also id.*, 5:21-24 (explaining that CLK1 and CLK2 “do not overlap”; 2:4-5; 5:24-28; 3:51-53; Decl., ¶ 216.

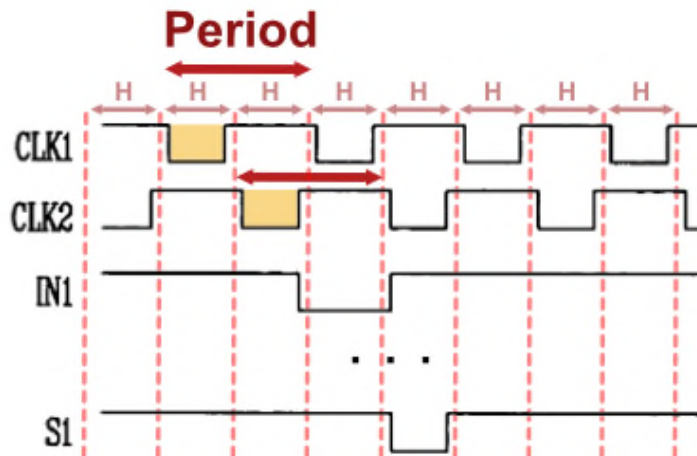
As shown below, Shin’s first and second clock signals—CLK1 and CLK2—have the same period (red arrows) and active phases (orange) that do not overlap:



Shin, Fig. 9 (excerpted); *see also* Decl., ¶¶ 444-450.

4. Claim 4

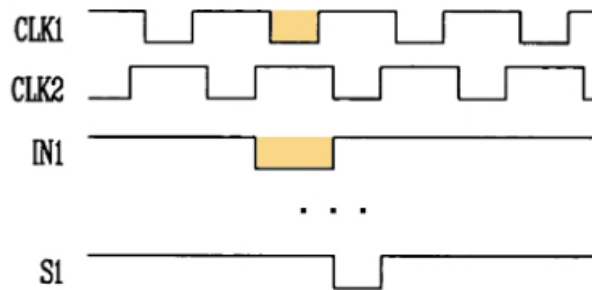
Claim 4 depends from Claim 3 and requires that “the first clock signal and the second clock signal have a period equal to two horizontal periods 2H and are supplied in different horizontal periods as low signals.” This is exactly what Shin teaches:



Shin, Fig. 9 (excerpted); *see also supra* Section VIII.A.4; Decl., ¶¶ 451-454.

5. Claim 5

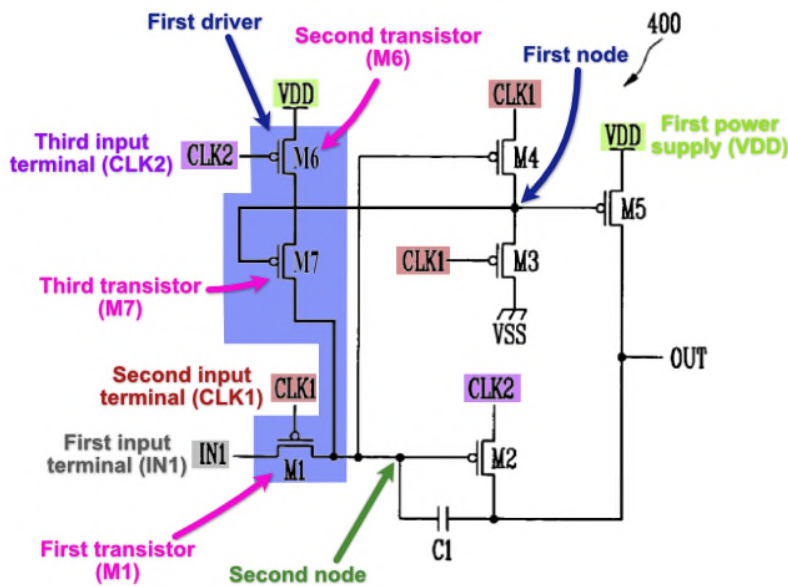
Claim 5 depends from Claim 2 and requires that “the start signal is supplied to overlap the first clock signal.” As shown below, Shin’s signals IN1 (the start signal) and CLK1 (the first clock signal) overlap:



Shin, Fig. 9 (excerpted); Decl., ¶¶ 455-459.

6. Claim 6

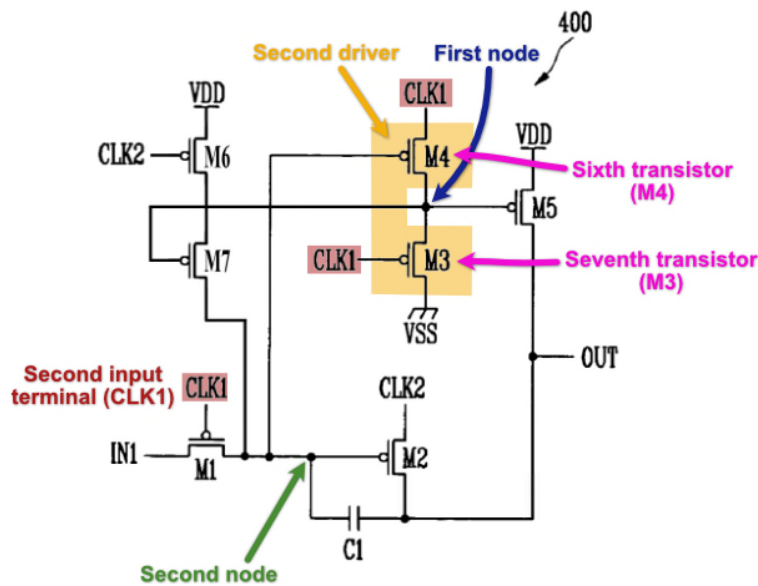
Claim 6 depends from Claim 2. Shin and Sasaki teach what this claim requires:



Decl., ¶¶ 460-462. As explained when discussing claim 1, Shin's first driver includes transistors M1, M6, and M7. *See supra* limitation [1-B]. Further, just as claim 6 requires, this first driver includes a "first transistor [M1] between the first input terminal [the terminal supplying IN1] and the second node [the electrode leading to transistor M2's gate], the first transistor [M1] having a gate electrode coupled to the second input terminal [the terminal supplying CLK1]." *See Id.*, ¶¶ 462-463. The first driver also includes "a second transistor [M6] and a third transistor [M7] serially positioned between the second node and the first power supply [VDD]," where "a gate electrode of the second transistor [M6] is coupled to the third input terminal [the terminal supplying CLK2]," and "a gate electrode of the third transistor [M7] is coupled to the first node [node 1 between transistors M3 and M4]." *See id.*, ¶¶ 465-473.

7. Claim 8

Claim 8 depends from Claim 2. Shin and Sasaki also teach what this claim requires:

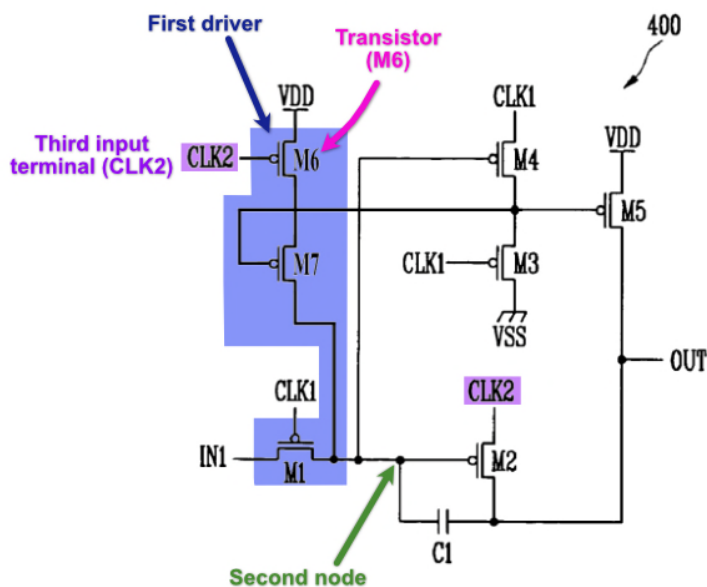


Id., ¶ 477. As explained when discussing claim 1, Shin’s second driver includes transistors M3 and M4. *See supra* limitation [1-C]. Further, as claim 8 requires, this “second driver includes: a sixth transistor [M4] between the first node [node N1 between transistors M3 and M4] and the second input terminal [the terminal applying CLK1], the sixth transistor [M4] having a gate electrode coupled to the second node [the electrode leading to transistor M2’s gate].” *Id.*, ¶¶ 477-479. The second driver also includes and “a seventh transistor [M3] between the first node and a second power supply [VSS], the second power supply having a lower voltage than the first power supply [VDD], the seventh transistor [M3] having a gate electrode coupled to the second input terminal [the terminal supplying CLK1].” *Id.* ¶¶ 480-481 Moreover, Shin explains that the “VDD” “power supply” has a “high level” potential, while “VSS” provides either a “negative supply voltage” or is

“grounded.” Shin., [0093], [0099]. Thus, Shin’s “second power supply” (VSS) has a “lower voltage” than its “first power supply” (VDD). See Decl., ¶ 482.

8. Claim 14

Claim 14 depends from Claim 1 and requires that “the transistor controls the voltage of the second node according to the on/off operation thereof.” Shin/Sasaki’s transistor M6 satisfies this claim: It is part of the first driver, is connected to the terminal receiving CLK2 (the third input terminal), and is connected to and turns on/off to control the voltage of the node leading to transistor M2’s gate (the second node):



See *id.*, ¶¶ 484-491; see also *supra* Section VIII.B.

9. Independent Claim 15

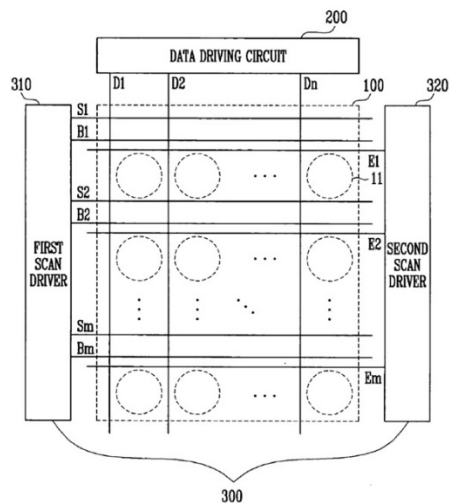
a) [15-PRE]

Claim 15 is directed to “[a]n organic light emitting display.” To the extent limiting, this is what Shin and Sasaki teach. *See, e.g.*, Shin, [0002] (explaining that Shin’s “scan driving circuit” is for use with an “organic light emitting display.”); *see also id.*, Abstract, Title, [0016], [0041]-[0042]; Decl., ¶¶ 493-496.

b) Element [15-A]

Shin teaches “pixels positioned in regions partitioned by scan lines and data lines.” Figure 4 of Shin depicts an “organic light emitting display” with a “display panel 100.” Shin, [0042]. The panel includes a “plurality of pixel circuits 11 ... arranged in an array.” *Id.*, [0044]. The pixel circuits are separated by horizontal “signal lines S1 to Sm for transferring a selection signal to a select a row of pixels” and vertical “data lines D1 through Dn.” *Id.*, [0046]-[0047]. The signal lines are connected to a “scan driving circuit 300,” while the data lines are connected to a “data driving circuit 200.” *Id.*

FIG. 4

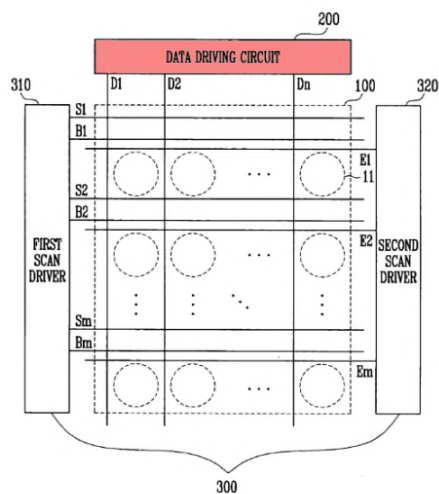


Id., Fig. 4; Decl., ¶¶ 497-501.

c) Element [15-B]

Shin teaches “a data driver for supplying data signals to the pixels through the data lines.” Again, “data lines D1 through Dn” are connected to a “data driving circuit 200” that “applies a data current I_{DATA} ” to each of the data lines. Shin, [0047].

FIG. 4



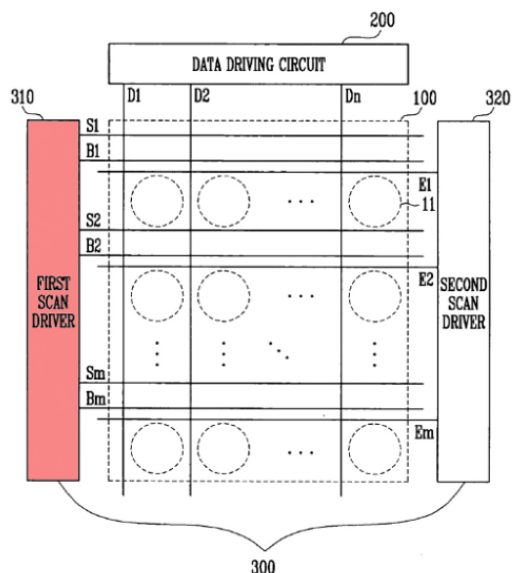
Id., Fig. 4; *see also* Decl., ¶¶ 502-504.

d) Element [15-C]

Shin also teaches “a scan driver for supplying scan signals to the pixels through the scan lines, the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals and having a first input terminal, a second input terminal, a third input terminal, and an output terminal.”

In particular, according to Shin, its display includes a “first scan driver 310” that “sequentially applies a selecting signal for selecting a pixel circuit 11 to the selection signal lines S1 to Sm.” Shin, [0047].

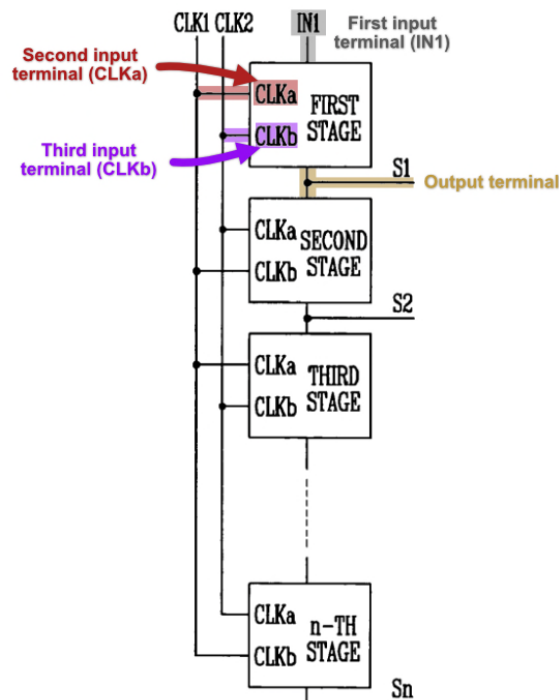
FIG. 4



Id., Fig. 4.

Next, Shin’s “first scan driver” includes a “scan drive unit 312” formed from

a series of “stages” that are “coupled” with various “input signal ... lines.” *Id.*, [0070]-[0071]. As shown below, a “first input signal IN1 is supplied to a first stage” (via the claimed **first input terminal**). *Id.*, [0073]. Next, “each stage ... includes a first clock terminal CLKa” (the **second input terminal**) and “second clock terminal CLKb” (the **third input terminal**) receiving “[f]irst and second clock signals CLK1 and CLK2....” *Id.*, [0074]. Finally, each stage includes an “output lin[e]” (the **output terminal**) “coupled with ... row lines S1 to Sn” to “provide” the pixel “selection signal.” *Id.*, [0072].



Id., Fig. 10; *see also supra* discussion of element [1-PRE]; Decl., ¶¶ 505-518.

e) Elements [15-D]-[15-G]

Elements [15-D]-[15-G] are the same as Elements [1-A]-[1-D]. Thus, Shin—when modified to include Sasaki’s anti-reversal circuit—teaches these elements for the same reasons discussed for claim 1. *See supra* claim 1; Decl., ¶¶ 520-528.

10. Claim 16

Claim 16 depends from Claim 15 and additionally requires that “a clock signal supplied to the third input terminal is used as the scan signal.” Each stage of Shin’s circuit receives “[f]irst and second clock signals CLK1 and CLK2....” Shin, [0074]. Transistor M2 controls provision of clock signal CLK2 from the “second clock terminal” (the claimed **third output terminal**) to “an output line OUT.” *Id.*, [0088]. This output is then used as a “scan driving” “selection signal.” *Id.*, [0047], [0072]; *see also* Decl., ¶¶ 530-536.

11. Claim 17

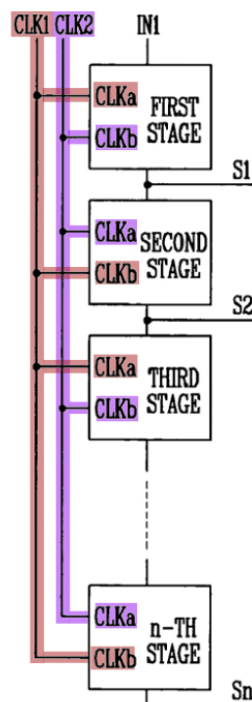
The additional limitation of Claim 17 is the same as Claim Element [2-A] because a scan signal is an output signal as just explained with respect to Claim 16. Thus, Shin and Sasaki discloses Claim 17 for the same reasons discussed above for Claim 2. *See supra* claim 2; *see also* Decl., ¶¶ 537-540.

12. Claim 18

Claim 18 depends from Claim 17 and requires that the “second input terminals of odd stage circuits receive a first clock signal and third input terminals of odd stage

circuits receive a second clock signal” and “second input terminals of even stage circuits receive the second clock signal and third input terminals of even stage circuits receive the first clock signal.” According to Shin, in its “odd numbered stage[s],” “a first clock signal CLK1” (the claimed **first clock signal**) “is supplied to the first clock terminal” (the **second input terminal**) while “a second clock signal CLK2” (the **second clock signal**) “is supplied to the second clock terminal” (the **third input terminal**). Shin, [0090]. The “even-numbered stage[s]” are reversed. *Id.*

Figure 4 below shows this alternating supply:



Id., Fig. 4; see also Decl., ¶¶ 541-545.

13. Claim 19

Claim 19 depends from claim 18 and adds the same further limit as claim 3. Shin and Sasaki teach what this claim requires for same reasons discussed for that claim. *See supra* claim 3; Decl., ¶¶ 546-548.

14. Claim 20

Claim 20 depends from claim 18 and adds the same limit as claim 6. Shin and Sasaki teach what this claim requires for same reasons discussed for that claim. *See supra* claim 6; Decl., ¶¶ 549-552.

15. Claim 22

Claim 22 depends from claim 18 and adds the same further limit as claim 8. Shin and Sasaki teach what this claim requires for the same reasons discussed above for that claim. *See supra* claim 8; Decl., ¶¶ 553-556.

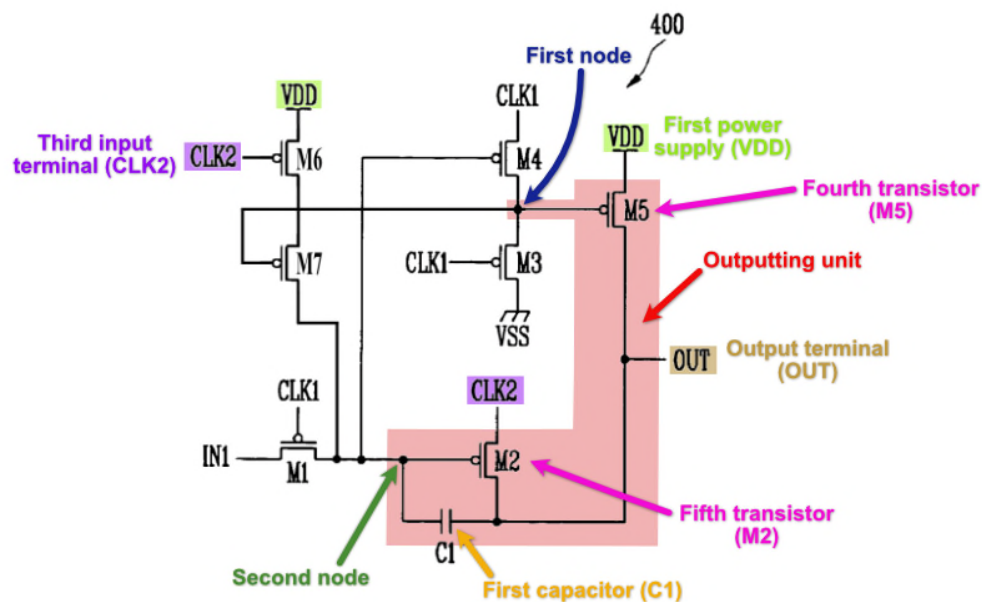
16. Claim 25

Claim 25 depends from Claim 18 and requires that “the scan signal of the previous stage circuit or the start signal supplied to the first input terminal overlaps the clock signal supplied to the second input terminal.” This is taught by Shin and Sasaki for the same reasons discussed for claim 5: Shin’s “start signal supplied to the first input terminal” (signal IN1) overlaps the “clock signal supplied to the second input terminal” (CLK1). *See supra* claim 5; Decl., ¶¶ 557-566.

C. GROUND 3: Shin, Sasaki, and Jeong Render Claims 7 and 21 Obvious

Claim 7 depends from Claim 2. Claim 21 depends from claim 18. Both claims include the same additional limitations requiring that the claimed “outputting unit” include both “fourth” and “fifth” transistors and “first” and “second” capacitors.

As shown below, Shin’s circuit includes most the elements required by claims 7 and 21:

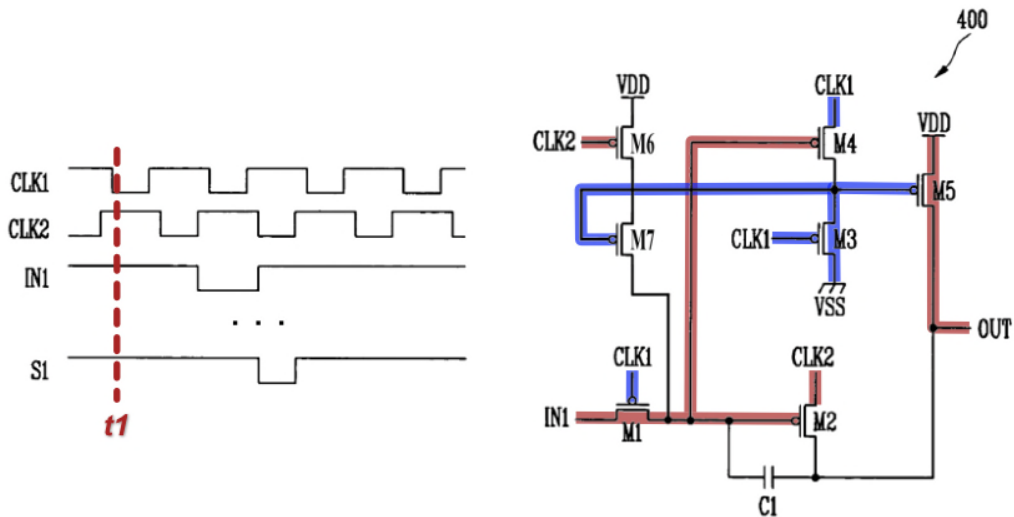


Decl., ¶¶ 572-574. In particular, Shin’s “outputting unit includes: a fourth transistor [M5] between the first power supply [VDD] and the output terminal [OUT].” *Id.* This “fourth transistor [M5] ha[s] a gate electrode coupled to the first node” as required. *Id.*; see also Shin, [0088] (“transistor M5 is coupled between ... VDD and ... OUT” and has its gate “coupled with the first node N1”). Next, Shin’s outputting

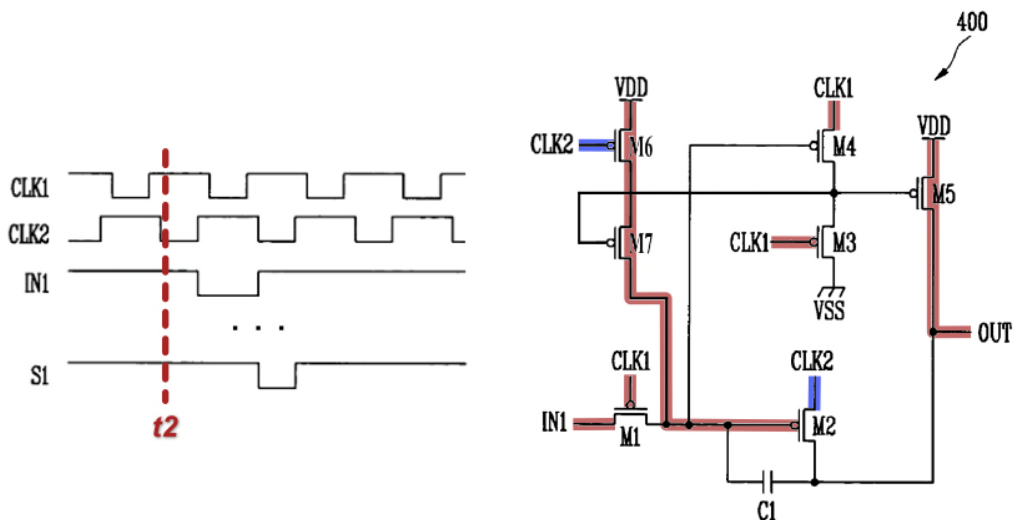
unit includes the required “fifth transistor [M2] between the output terminal [OUT] and the third input terminal [the terminal supplying CLK2].” Decl., ¶¶ 572-574. This “fifth transistor [M2] ha[s] a gate electrode coupled to the second node[.]” *Id.*; see also Shin, [0088] (“transistor M2 is coupled with a second clock terminal and ... OUT,” and has its gate “coupled with the output ... of ... transistor M1”). Moreover, Shin includes claim 7 and 21’s “first capacitor [C1] between the second node and the output terminal [OUT][.]” Decl., ¶¶ 572-574; see also Shin, [0089] (“first capacitor C1 that is coupled between an output terminal of ... transistor M1 and ...OUT”). All that is missing is “a second capacitor between the first node and the first power supply.” See Decl., ¶ 574.

A POSITA would have considered it obvious to include this additional “second capacitor” this claim requires in Shin and Sasaki’s circuit. See *id.*, ¶¶ 569-571, 574-589. As of the ’593 patent’s filing, capacitors were routinely employed to control the voltage of the gates of transistors responsible for passing signals to the output of a scan driver stage. Indeed, Shin itself already employs one such capacitor: “capacitor C1” stores a received “low-level” IN1 signal for purposes of keeping transistor M2 “turned-on” after supply of the low signal ceases (and the transistor’s gate would otherwise be floating). Shin, [0102]. A POSITA would have recognized that Shin’s transistor M5 is subject to similar operating conditions. In particular, during the below period **t1**, transistor M4 is closed and M3 is open allowing a low

signal to be applied to transistor M5 from VSS. This results in the supply of a high signal from VDD to OUT:

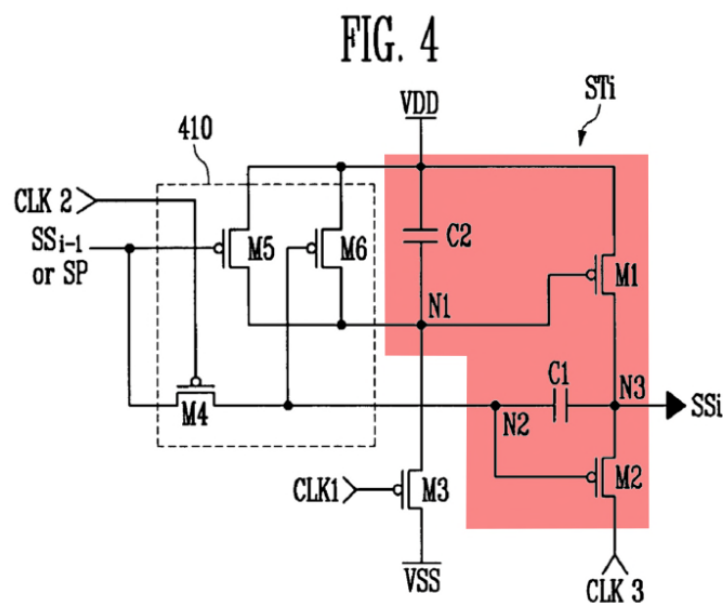


Decl., ¶¶ 575-576. In period t_2 , both transistors M3 and M4 are closed, leaving the gate of transistor M5 floating. During this time, however, Shin still intends to supply a high signal from VDD to OUT:



Id., ¶¶ 577-580. This leads to a problem: electromagnetic interference or other perturbances may cause changes in the voltage (and spurious signals) on the line leading to transistor M5's gate. This could cause it to close when it should be open. *See id.* A POSITA would have understood that this problem would be eliminated by including another capacitor. *See id.*, ¶¶ 581-583

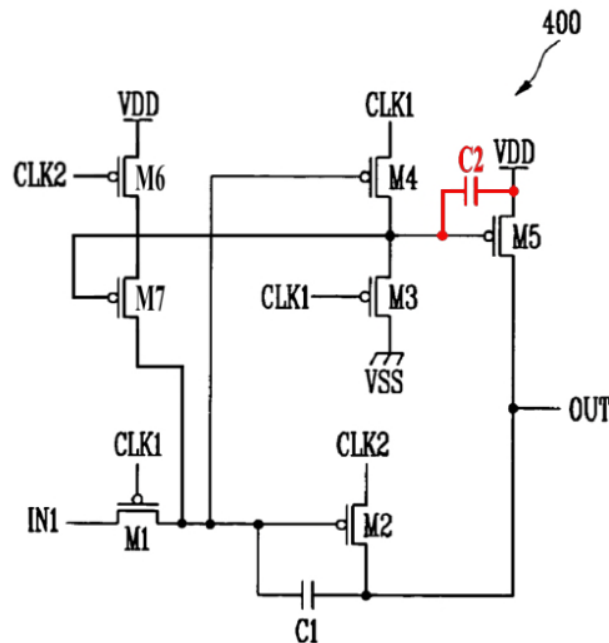
Another reference—Jeong—provides an example. Jeong, like Shin, relates to a “shift register” for an “organic light emitting display.” Jeong, [0002]. Figure 4 of Jeong is a “detailed circuit diagram” of one shift register “stage.” *Id.*, [0044].



Id., Fig. 4. Transistor M2 (like Shin’s similarly labeled transistor M2) is responsible for controlling provision of a clock signal to the stage’s output. *See id.*, [0053]. Transistor M1 (like Shin’s transistor M5) controls provision of VDD to the output. *See id.*, [0052]. Jeong includes two capacitors C1 and C2. *See id.*, [0056]-[0057]

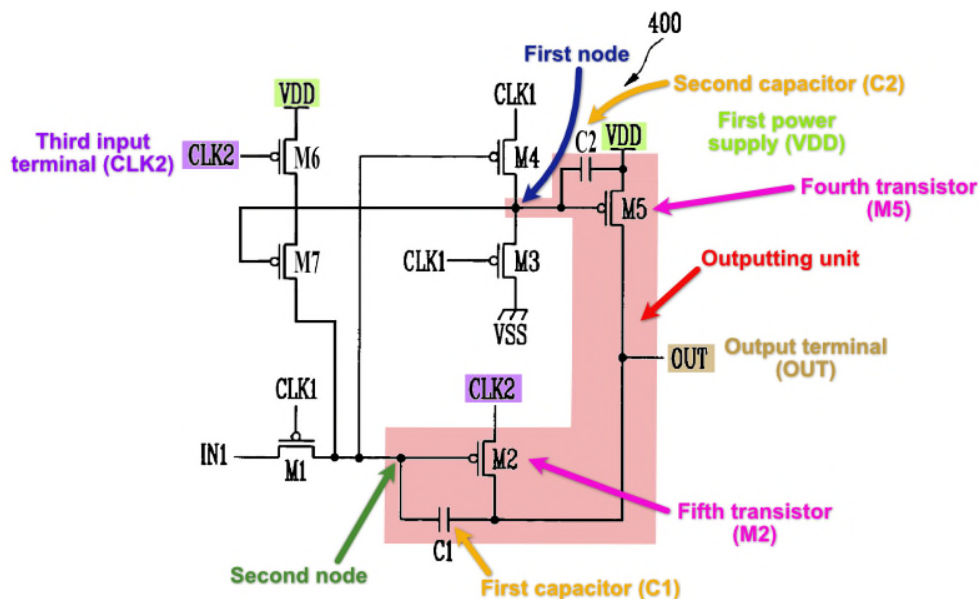
Capacitor C1 performs a function similar to Shin’s capacitor C1: it “stabilize[s] an operation of the second transistor M2.” *Id.*, [0056]. Capacitor C2 performs the function that Shin is missing: it “reduce[s] variation of a voltage” at a “first node N1” leading to the gate of transistor M1. *Id.*, [0056].

A POSITA would have recognized that Shin would be improved by including a capacitor C2. As in Jeong, this capacitor would be “coupled between the first power supply VDD and the first node N1.” *Id.*



Decl., ¶¶ 583-587. In operation, capacitor C2 would be charged by the low signal from VSS during period *t1* discussed above. *See id.*, ¶¶ 588-589. Then, during period *t2*, the capacitor would discharge and function to ensure that transistor M5 remains open. *See id.* When this second capacitor is applied, Shin includes the

“second capacitor [C2] between the first node and the first power supply [VDD]”
required by claims 7 and 21:



Id., ¶¶ 590-591.

A POSITA would have been motivated to apply a second capacitor like that shown in Jeong to Shin and Sasaki. A POSITA would have recognized that doing so would have improved Shin and Sasaki by reducing the potential effects of interference and spurious signals on transistor M5’s operation. *See id.*, ¶¶ 581, 587-589. This would have in turn improved scan drive unit’s operation and the fidelity of the signal it outputs. *See id.* Further, a POSITA would have recognized that capacitors were routinely used in the prior art scan drive units to stabilize transistor operation. *See id.*, ¶¶ 581-586; *see also* Jeong, [0057]; Ex. 1020, [0053]. Given this,

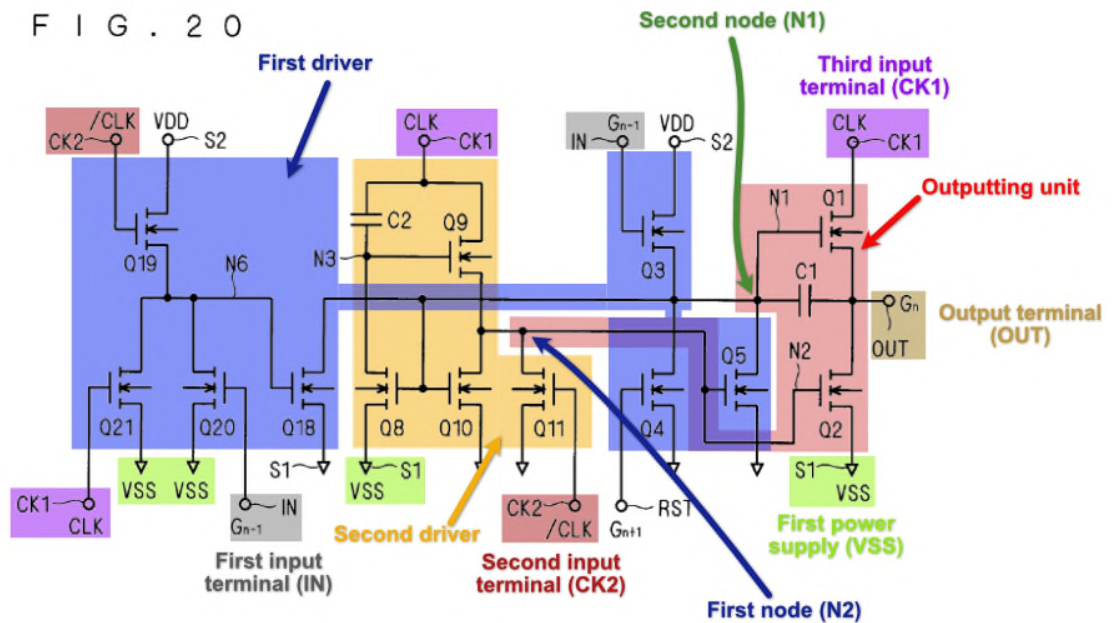
a POSITA would have considered use of a such a transistor with Shin and Sasaki to be nothing more than a routine, minor design choice. *See id.*, ¶¶ 569-571, 581-582.

A POSITA would also have had a reasonable expectation of success. Shin is already open to the use of capacitors to stabilize operation of its transistors. Indeed, it already employs capacitor C1 to keep transistor M2 open. *See Shin*, [0089]. Thus, application of Jeong is nothing more than an extension of an approach Shin already employs for an analogous purpose. *See id.* Moreover, a POSITA would have recognized that Jeong’s example capacitor—which is no different from those routinely used in the art—is specifically designed for use in a scan drive unit like that taught by Shin and Sasaki. *See Decl.*, ¶¶ 126-128, 569-571, 583-584. This would have given a POSITA every reason to believe and no reason to doubt that it could have been successfully used with Shin and Sasaki. *See id.*

D. GROUND 4: Tobita Renders Claims 1-2 and 15-18 Obvious

Tobita teaches a “shift register” for a display. Tobita, [0002]. The shift register includes multiple interconnected stages. *See, e.g., id.*, Fig. 8. “FIG. 20” depicts one such stage. *Id.*, [0172]. As discussed in greater detail below, this stage’s circuit includes all the components required by many of the ’593 patent’s claims:

FIG. 20



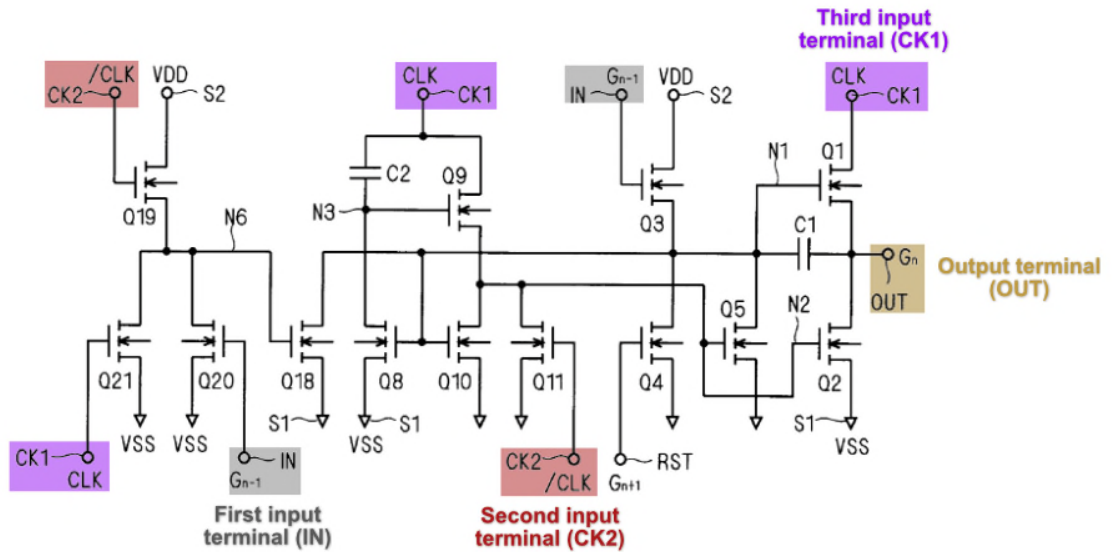
Decl., ¶ 596.

1. Independent Claim 1

a) [1-PRE]

Tobita teaches “[a] stage circuit having a first input terminal [IN], a **second input terminal [CK2]**, a **third input terminal [CK1]**, and an **output terminal [OUT]**.” See, e.g., Tobita, [0109], [0111], [0115], [0173], [0178] (describing circuit with a “first clock terminal CK1,” an “input terminal IN,” a “second clock terminal CK2,” and an “output terminal OUT”):

F I G . 2 0

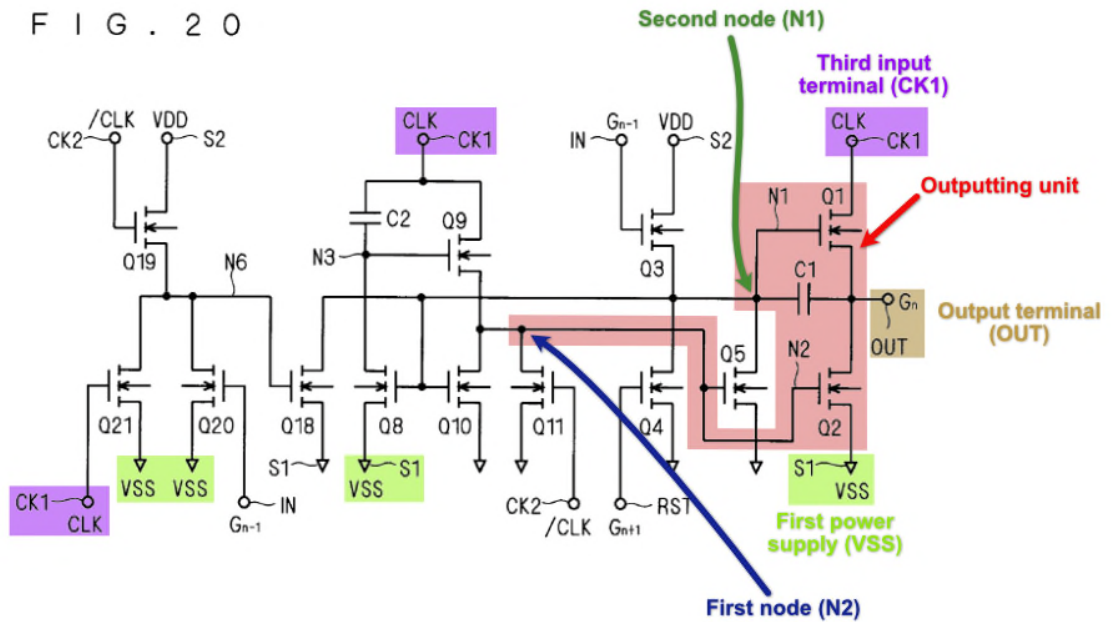


Tobita, Fig. 20; *see also* Decl., ¶¶ 598-601.

b) Element [1-A]

Tobita teaches the claimed “**outputting unit**”:

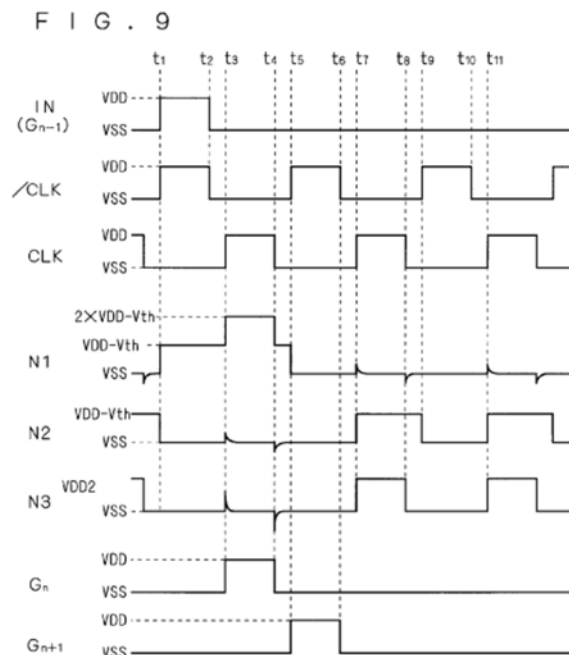
F I G . 2 0



Tobita, Fig. 20; *see also id.*, [0109]; Decl., ¶ 603. In Tobita, transistor Q1 and Q2

supply signals to “output terminal OUT” (the claimed **output terminal**): “Q1 ... suppl[ies] the clock signal” from “clock terminal CK1” (the claimed **third input terminal**) and “Q2 ... suppl[ies] the low supply voltage VSS” (the claimed **first power supply**). Tobita, [0109]. The gate electrodes of Q1 and Q2 are respectively connected to—and thus controlled by—Tobita’s node N1 (the claimed **second node**) and the node N2 (the claimed **first node**). Decl., ¶¶ 603-604.

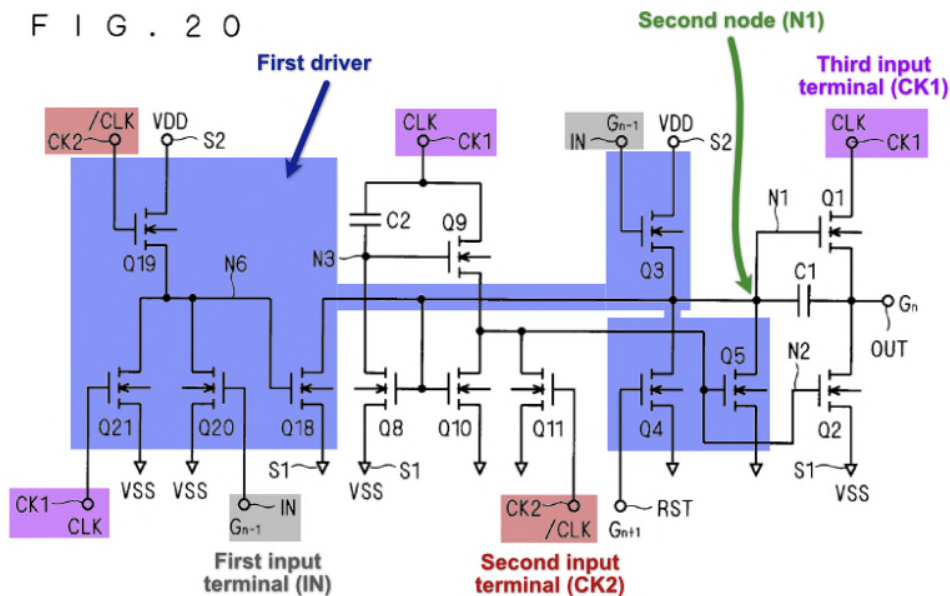
This functionality is summarized in Tobita’s circuit timing diagrams. One of these is specific to Figure 7. As Figures 7 and 20 share many common components and functionalities (*compare* Exs. 1006, Figs. 7, 20), a POSITA would have understood that it also applies to Figure 20’s circuit. Tobita, ¶¶ [0026]-[0028], [0117], [0195]; Decl., ¶ 606.



Tobita, Fig. 9, [0120]-[0137]. As shown, during t_1 -to- t_2 and t_2 -to- t_3 , node N2 is low, turning off transistor Q2. *Id.*, [0120]-[0121]. Node N1 is high, turning on transistor Q1. *Id.* Thus, CLK is transferred to OUT. *Id.* During t_7 -to- t_8 and t_8 -to- t_9 , node N2 is high (turning on Q2) while node N1 is low (turning off Q1). *Id.*, [0131]-[0133]. VSS is coupled to OUT through Q2. *Id.*, [0132]-[0135]; *see also* Decl., ¶¶ 605-613.

c) Element [1-B]

Tobita teaches the claimed “first driver to control the voltage of the second node”:



Tobita, Fig. 20; *see also id.*, [0111], [0173]; Decl., ¶ 614. Signal G_{n-1} received at IN (Tobita’s first input terminal) controls the on/off operation of transistor Q3, which in turn contributes to control of the voltage of node N1 (the claimed second node). *See, e.g.*, Tobita, [0120]-[0121], [0125]. Transistors Q18-Q21—which receive

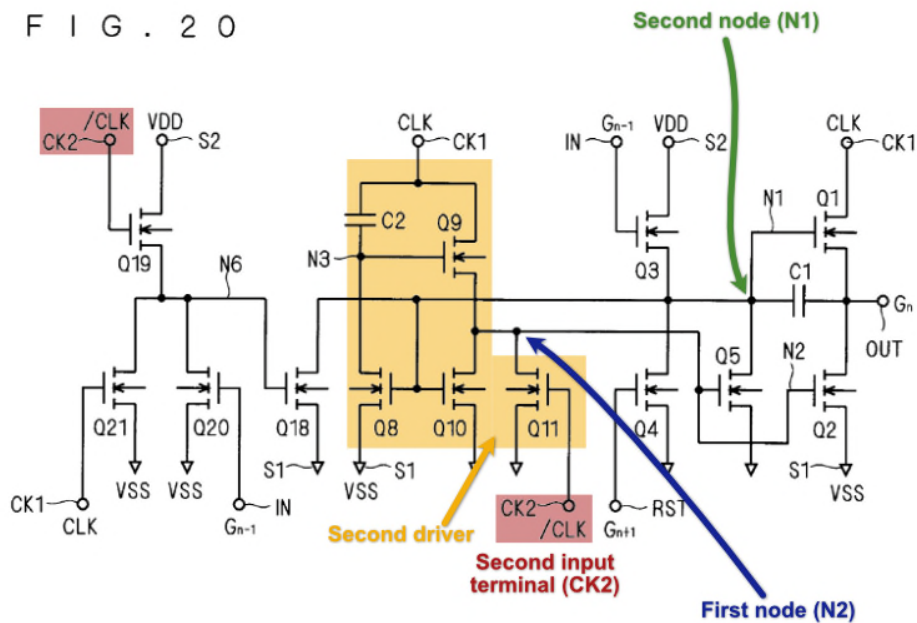
signals from IN (the first input terminal), CK2 (the second input terminal), and CK1 (the third input terminal)—also control the voltage of the node N1 by, e.g., bringing it to a low level. *Id.*, [0172], [0174]-[0177]. Transistors Q4 and Q5 likewise provide output to and operate to control the potential of node N1. *Id.*, [0175]-[0176]. Thus, transistors Q3-Q5 and Q18-Q21 are the claimed first driver: they receive input from IN, CK2, and CK1 (the claimed first input terminal, second input terminal, and third input terminal) and collectively operate to control the voltage of node N1 (the claimed second node). Decl., ¶¶ 614-621.

While Tobita uses more transistors than the '593 patent's example "first driver" does, claim 1 does not limit the number of transistors in the first driver (or any other component). *Id.*, ¶ 622. Additionally, while certain of Tobita's transistors do not directly provide output to node N1, Patent Owner has taken the position in the associated ITC action that the claimed "first driver" can indirectly control node voltage. *E.g.*, Ex. 1009, 22-23. Regardless, Tobita's "first driver" does directly provide output to—and controls—node N1 via transistors Q3-Q5 and Q18. *See* Decl., ¶ 622.

a) Element [1-C]

Tobita includes the claimed "second driver to control the voltage of the first node":

F I G . 2 0

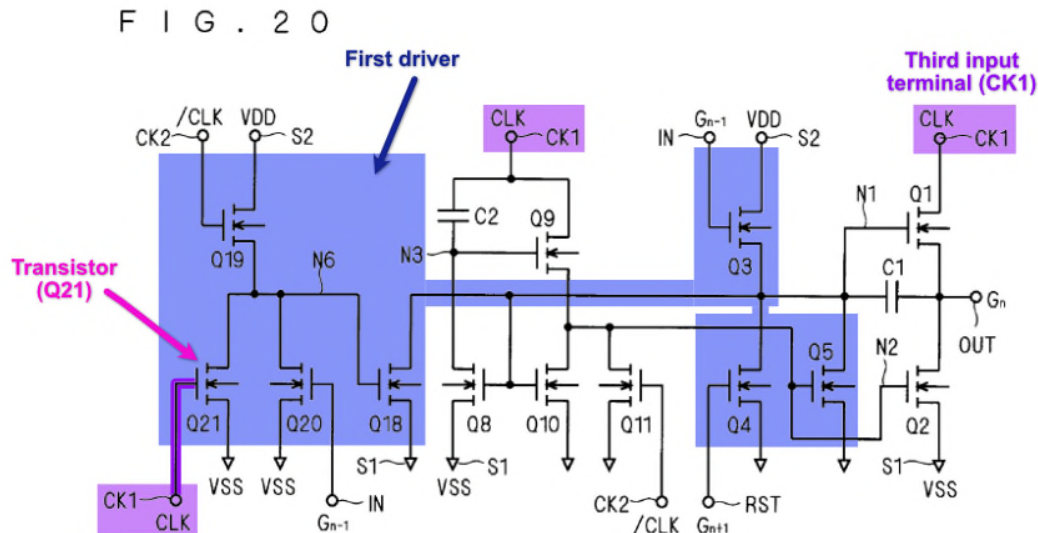


Tobita, Fig. 20; *see also id.*, [0113]-[0114]; Decl., ¶ 624. Node N2 (the claimed [first node](#)) is coupled to gate electrode and controls operation of transistor Q2. *See, e.g.*, Tobita, [0120], [0123]-[0124], [0132], [0134], [0136]; Decl., ¶¶ 624-625. The potential of node N2 is itself controlled by the output of transistors Q8-Q11. *See, e.g.*, Tobita [0115], [0120]-[0121], [0123]-[0124], [0129]-[0132], [0134], [0136]. These transistors constitute the [second driver](#). Of these, Q8 and Q10 have their gates connected to and are controlled by node N1 (the claimed [second node](#)). *Id.* Transistor Q11 is controlled by the /CLK signal supplied to CK2 (the [second input terminal](#)). *Id.*; *see also* Decl., ¶¶ 626-630.

b) Element [1-D]

In Tobita, “the signal of the third input terminal directly controls an on/off operation of a transistor” in “the first driver”: the gate of [transistor Q21](#) (part of

Tobita's **first driver**) is coupled to has its on/off functionality controlled by the CLK signal supplied to CK1 (the **third input terminal**):

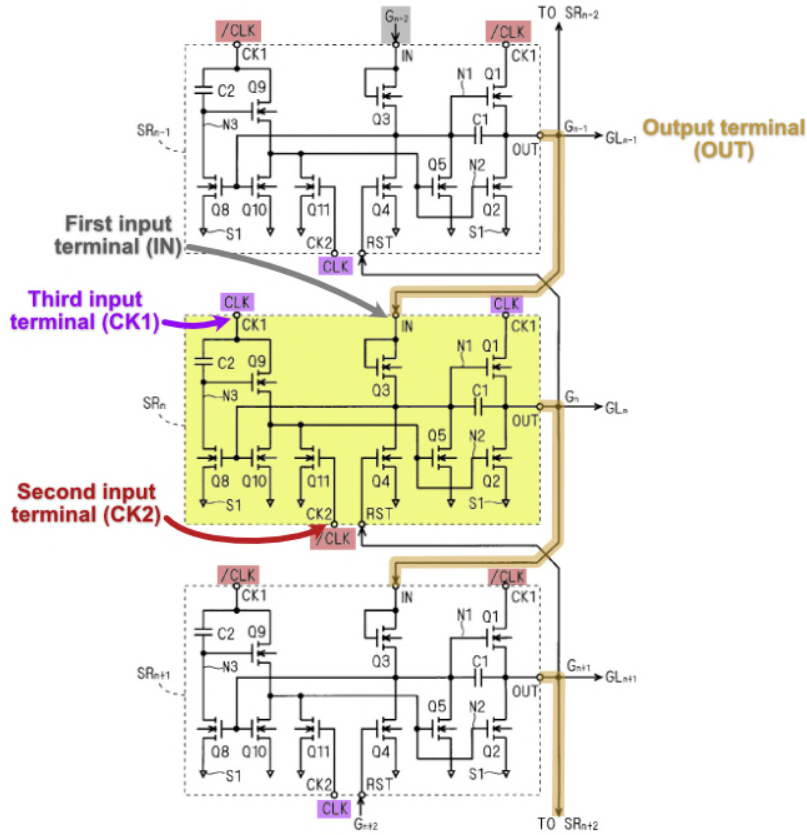


Tobita, Fig. 20; *see also id.*, [0086]; [0177]; Decl., ¶¶ 631-632.

2. Claim 2

Claim 2 depends from Claim 1 and requires that “the first input terminal receives an output signal of a previous stage circuit or a start signal,” “the second input terminal receives a first clock signal,” and “the third input terminal receives a second clock signal.” Tobita teaches a shift register including stages SR_{n-1} , SR_n , SR_{n+1} , etc.:

FIG. 8



Tobita, Fig. 8, [0117]. As shown, terminal IN (the first input terminal) of stage SR_n receives output signal G_{n-1} of the previous stage circuit SR_{n-1} (that stage's output signal). *Id.* Terminal CK2 (the second input terminal) of SR_n receives $/CLK$ (the claimed first clock signal), and terminal CK1 (the third input terminal) of SR_n receives CLK (the claimed second clock signal). Both $/CLK$ and CLK are clock signals. *Id.*, [0118]; see also Decl., ¶¶ 634-642.

3. Independent Claim 15

a) [15-PRE]

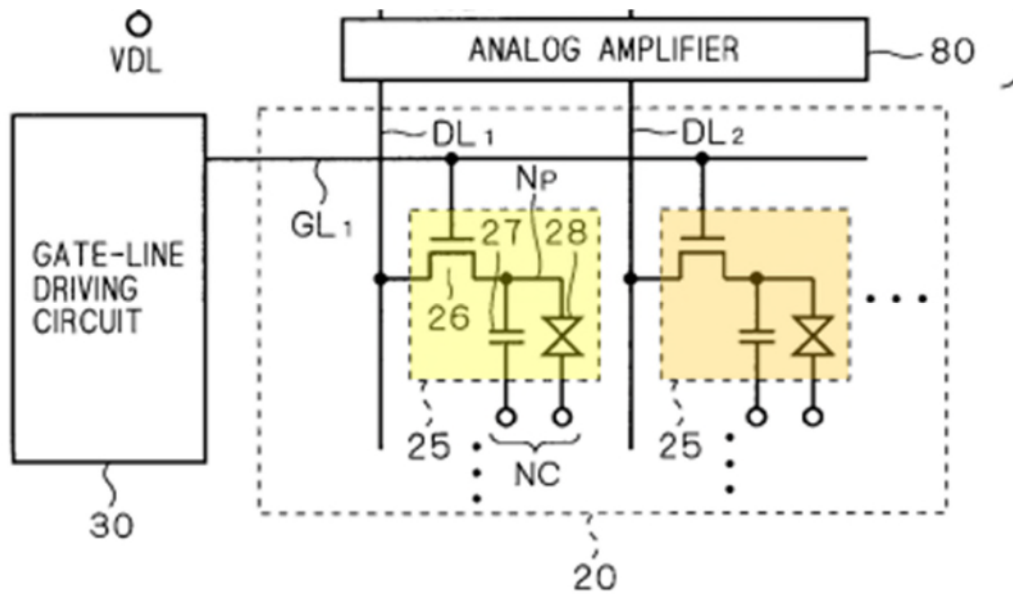
Claim 15 is directed to “[a]n organic light emitting display.” This preamble

is a non-limiting label of intended use. *See Arctic Cat Inc. v. GEP Power Prod., Inc.*, 919 F.3d 1320, 1329-30 (Fed. Cir. 2019).

Regardless, even if limiting, a POSITA would have found it obvious to employ Tobita's circuit with an OLED. Decl., ¶¶ 646-648. While Tobita references "a liquid crystal display," this is only an example. Tobita, [0004]. Tobita explains that its teachings broadly apply to any "display apparatus." *Id.* And, when the '593 patent was filed, OLEDs were well-known. Decl., ¶¶ 647-651. They were also known to share features with LCD displays including pixel matrices, data drivers, and scan drivers. *Id.*, ¶ 650. It was also well-known that LCD and OLED displays can employ structurally and functionally similar stage circuits. *See, e.g.*, Ex. 1015 at 14-16 (claims 1, 14).

b) Element [15-A]

Tobita teaches "pixels positioned in regions partitioned by scan lines and data lines." Figure 1 shows "pixels 25 arrayed in a matrix." Tobita, [0059]. Gate or scanning lines—GL₁, GL₂, etc.—are connected to rows of pixels, and data lines—DL₁, DL₂, etc.—are connected to columns of pixels. *Id.*, [0004], [0059]. The scan lines and data lines are located between and separate the pixels (yellow/orange boxes):

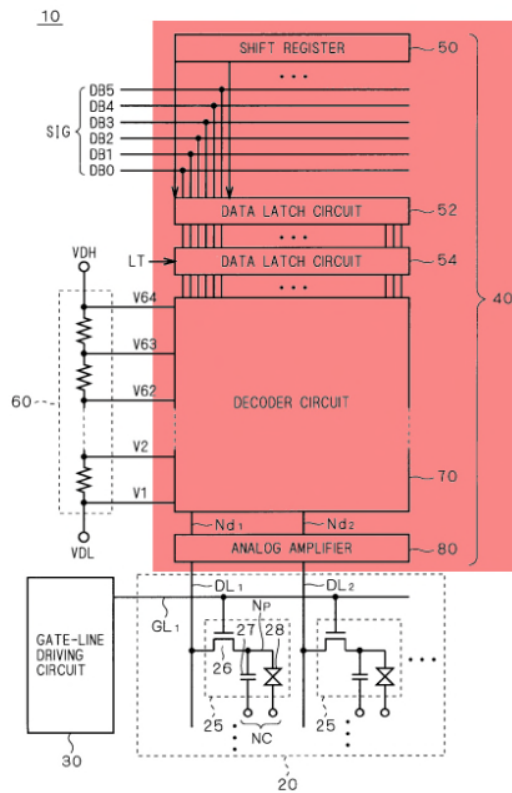


Id. Fig. 1 (partial); *see also id.*, [0059]-[0060]; Decl., ¶¶ 653-656.

c) Element [15-B]

Tobita teaches “a data driver for supplying data signals to the pixels through the data lines.” Tobita’s source driver 40 is responsible for “output[ting] display voltages set stepwise by a display signal SIG ... to the data lines DL.” Tobita, [0062]; *see also id.*, [0071]. The displayed image is based on this signal. *Id.*

F I G . 1

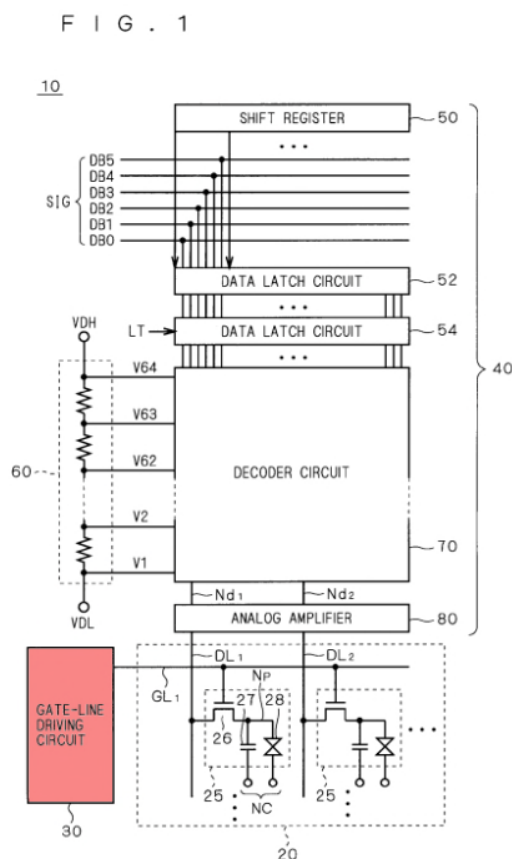


Id., Fig. 1; Decl., ¶¶ 657-659.

d) Element [15-C]

Tobita discloses “a scan driver for supplying scan signals to the pixels through the scan lines, the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals and having a first input terminal, a second input terminal, a third input terminal, and an output terminal.” Tobita employs “a gate-line driving circuit (scanning-line driving circuit) 30.” Tobita, [0058]. This circuit “sequentially drives the gate lines GL_1 , GL_2 , #. . . in synchronization with the scanning cycle.” *Id.*, [0071]; *see also id.*,

[0061].



Tobita, Fig. 1; see also Decl., ¶¶ 661-663.

The scan line drive circuit includes stages of “cascade-connected unit shift registers SR.” Tobita, [0167]. Each unit shift register receives input from IN (the first input terminal), CK2 (the second input terminal), and CK1 (the third input terminal), and outputs a corresponding scan signal G_n to OUT (the output terminal) which is then provided to scan line GL. See *supra* discussion of element [1-A]; Decl., ¶¶ 664-670.

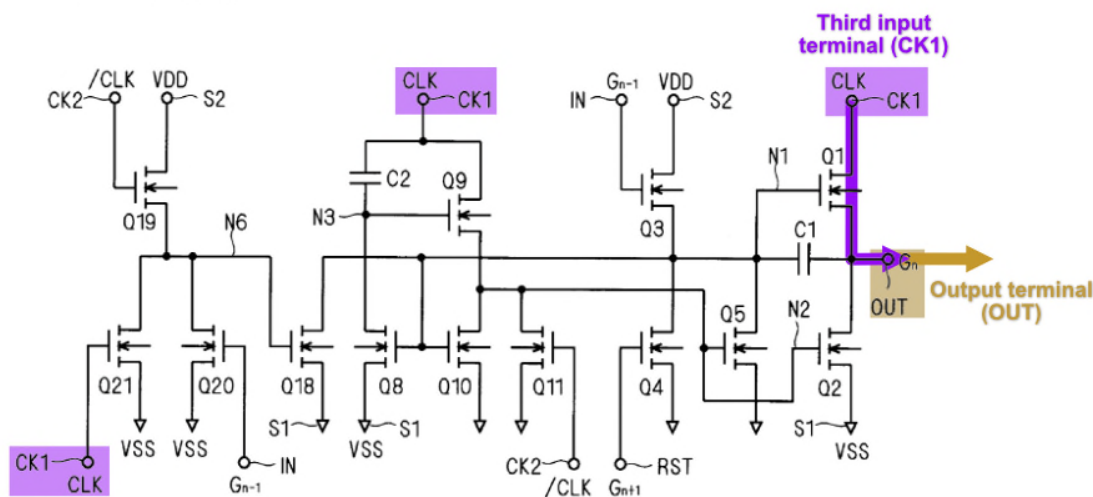
e) Elements [15-D]-[15-G]

Elements [15-D]-[15-G] are the same as elements [1-A]-[1-D] of claim 1. Thus, Tobita teaches the elements for the same reasons discussed. *See supra* claim 1; Decl., ¶¶ 672-680.

4. Claim 16

Claim 16 depends from Claim 15 and additionally requires that “a clock signal supplied to the third input terminal is used as the scan signal.” Tobita’s circuit supplies the CLK signal from terminal CK1 (the **third input terminal**) to OUT for use as gate line / scan signal G_n :

F I G . 20



Tobita, Fig. 20; *see also id.*, [0109], [0117], [0122], [0125]-[0126]; Decl. ¶¶ 682-689.

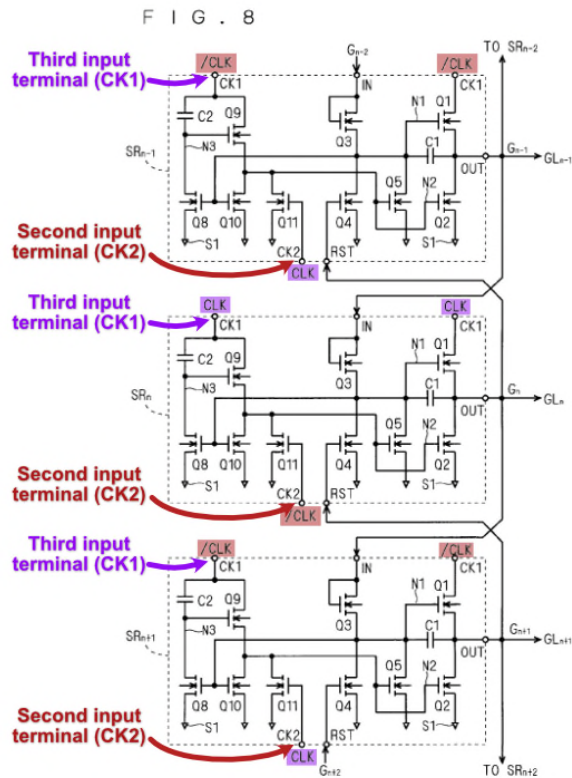
5. Claim 17

Claim 17 depends on claim 16 and adds the same limit as claim 2. Tobita thus teaches what this claim requires for same reasons discussed for that claim. See *supra* claim 2; Decl. ¶¶ 690-693.

6. Claim 18

Claim 18 depends from Claim 17 and requires that the “second input terminals of odd stage circuits receive a first clock signal and third input terminals of odd stage circuits receive a second clock signal” and “second input terminals of even stage circuits receive the second clock signal and third input terminals of even stage circuits receive the first clock signal.”

As shown below, in Tobita’s odd stage circuits (*e.g.*, SR_n), the **second input terminals (CK2)** receive a **first clock signal (/CLK)** and the **third input terminals (CK1)** receive a **second clock signal (CLK)**. The even stage circuits (*e.g.*, SR_{n-1} , SR_{n+1}) are reversed:

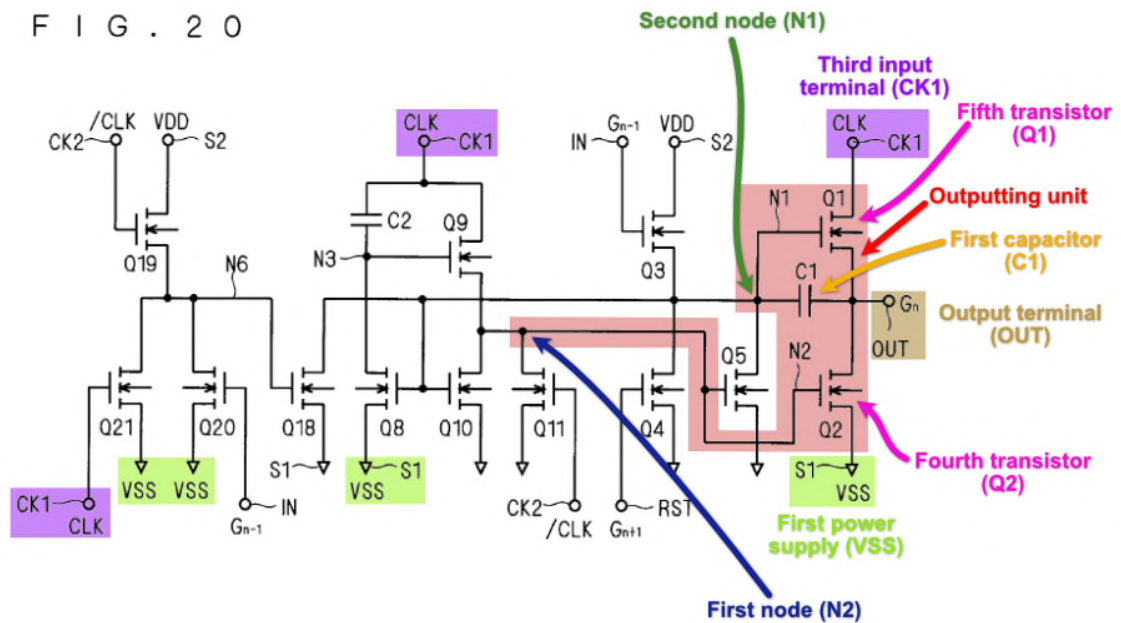


Tobita, Fig. 8; see also Decl., ¶¶ 694-700.

E. GROUND 5: Tobita in View of Jeong Renders Claims 7 and 21 Obvious

Claim 7 depends from Claim 2. Claim 21 depends on claim 18. Both include the same additional limitations requiring that the “outputting unit” include a “fourth transistor,” “fifth transistor,” “first capacitor,” and “second capacitor” connected in particular ways. Tobita’s **outputting unit** contains all the required components except the second capacitor:

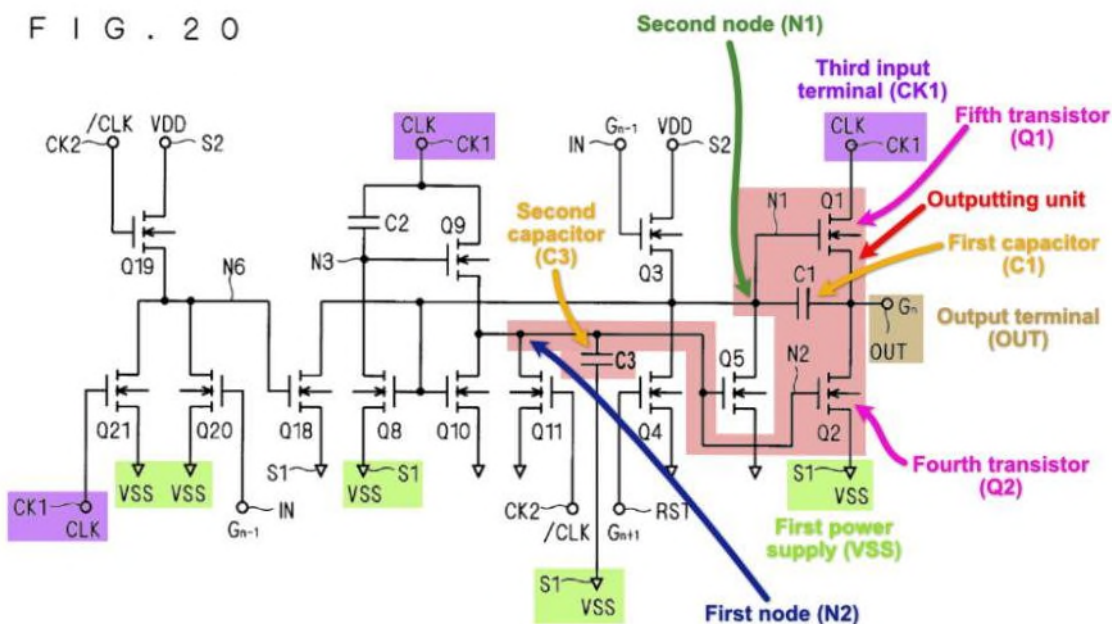
F I G . 2 0



Tobita, Fig. 20; see also Decl., ¶ 708. More specifically, there is “a fourth transistor [Q2] between the first power supply [VSS] and the output terminal [OUT], the fourth transistor [Q2] having a gate electrode coupled to the first node [N2],” “a fifth transistor [Q1] between the output terminal [OUT] and the third input terminal [CK1], the fifth transistor [Q1] having a gate electrode coupled to the second node [N1],” “a first capacitor [C1] between the second node [N1] and the output terminal [OUT].”

A POSITA would have recognized that node N2 only has a small amount of capacitance and may not adequately maintain a fixed voltage level in the presence of perturbations in electrical charge level or when the node is electrically isolated (when Q9-Q11 are all off). Decl., ¶¶ 708-713. To avoid this and increase the robustness of the circuit’s operation, a POSITA would have been motivated to add

a capacitor to this node as taught by Jeong. *Id.*, ¶¶ 714-721. As explained (*see supra* Section VIII.C), Jeong teaches that added capacitors operate “to reduce” “variation of” node “voltage.” Jeong, [0057]; Decl., ¶¶ 717-719. Applying this to Tobita results in a stage that includes the **second capacitor [C3]** as claimed:



Id., ¶ 722.

A POSITA would have found it obvious to apply Jeong’s capacitors to Tobita. A POSITA would have recognized that Tobita’s circuit could experience unintended—and highly undesirable—voltage variation, motivating the addition of second capacitor C2 between Tobita’s first power supply VSS and first node N2 to address this problem. *Id.*, ¶¶ 709-712. This would have in turn improved the operation of Tobita’s circuit and reduced the possibility of malfunction. *Id.* Moreover, a POSITA would have recognized capacitors were routinely used in stage

circuits for this purpose. *Id.*, ¶¶ 713-716.

Both Tobita and Jeong also relate to shift registers in a scan driver for pixel-matrix displays. Thus, a POSITA would have considered using their teachings in combination to be nothing more than a routine design choice. Decl., ¶¶ 703-705. Integrating the compatible circuits of Tobita and Jeong to achieve these circuits' respective advantages entails nothing more than an application of common sense. *Id.* Although Tobita illustrates its embodiments using nMOS transistors and Jeong uses pMOS transistors, the translation from one type to the other were well known. *Id.* ¶ 704. Further, the similarity of the functions and designs of Tobita and Jeong would have confirmed that combination of the references' teachings involved nothing more than straightforward modifications with predictable outcomes and a reasonable expectation of success. *Id.*, ¶ 705.

IX. SECONDARY CONSIDERATIONS

While Patent Owner may attempt to rely on alleged secondary considerations, no such considerations would overcome the showing of obviousness detailed above. *Tokai Corp. v. Easton Enters., Inc.*, 632 F.3d 1358, 1370 (Fed. Cir. 2011).

X. CONCLUSION

For the foregoing reasons, Petitioner respectfully requests the Board institute review of the '593 patent and cancel all Challenged Claims.

Respectfully submitted,

ORRICK, HERRINGTON & SUTCLIFFE LLP

Dated: March 6, 2024

/K. Patrick Herman/

K. Patrick Herman, Reg. No. 75,018
Orrick, Herrington & Sutcliffe LLP
51 West 52nd Street
New York, NY 10019
Telephone: (212) 506-3596
P52PTABDocket@orrick.com

Attorney for Petitioner

CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,330,593 complies with the type volume limitation in 37 C.F.R. § 42.24(a)(1). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, a table of authorities, mandatory notices under § 42.8, certificate of service, certificate of word count, or listing of exhibits, and claim listing—contains 13,775 words.

Dated: March 6, 2024

By: /K. Patrick Herman/

K. Patrick Herman, Reg. No. 75,018
Orrick, Herrington & Sutcliffe LLP
51 West 52nd Street
New York, NY 10019
Telephone: (212) 506-3596
P52PTABDocket@orrick.com

Counsel for Petitioner.

CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing PETITION FOR *INTER PARTES* REVIEW and the associated Exhibits were caused to be served on March 6, 2024 via overnight courier upon the following counsel of record for Patent Owner:

LEE IP LAW, P.C.
3060 WILLIAMS DRIVE
SUITE 300 #12
FAIRFAX, VA 22031

Copies were also served via email on Patent Owner's counsel of record in withdrawn IPR2023-01221:

David A. Garr (dgarr@cov.com)
Scott C. Weidenfeller (sweidenfeller@cov.com)
Covington & Burling LLP

/K. Patrick Herman/

K. Patrick Herman, Reg. No. 75,018
Orrick, Herrington & Sutcliffe LLP
51 West 52nd Street
New York, NY 10019
Telephone: (212) 506-3596
P52PTABDocket@orrick.com