IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MIANYANG BOE OPTOELECTRONICS TECHNOLOGY CO., LTD.; WUHAN CHINA STAR OPTOELECTRONICS SEMICONDUCTOR DISPLAY TECHNOLOGY CO., LTD.; TIANMA MICROELECTRONICS CO. LTD.; AND VISIONOX TECHNOLOGY, INC.
Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.
Patent Owner.

U.S. Patent No. 9,330,593

Inter Partes Review No. IPR2024-00620

DECLARATION OF DR. DANIEL FOTY

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I. INTRODUCTION

1. I have been retained by counsel for Mianyang BOE Optoelectronics Technology Group Co., Ltd. et al. ("BOE" or "Petitioner") in the above-captioned matter as an independent consultant to offer opinions regarding the patentability of the claims in U.S. Patent No. 9,330,593 ("the '593 patent" or "the challenged patent").

2. In the preparation of this Declaration, I have confined my analysis to the materials and opinions that were available at the time of the preparation of this Declaration – supplemented with my own knowledge and experience in the field. Should new materials, analyses, or opinions be introduced subsequent to the filing of this Declaration, I reserve the right to provide supplementary Declarations to the extent necessary to address any such newly introduced items.

3. If requested, I am prepared to explain (in a deposition or at a trial before the Patent Trial and Appeal Board (the "Board")) the technology disclosed in the challenged patent – including the state of the art in the relevant timeframe. Similarly, I am prepared to explain the technology disclosed in the prior art references cited herein. This may include, among other things, background information on driver circuits and OLED displays.

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II. QUALIFICATIONS

4. My qualifications to testify as an expert in electronics technology are set forth in my *curriculum vitae* attached as Appendix A – which includes a listing of cases in which I have provided expert testimony. I have more than thirty years of experience as an engineer, scientist, and consultant in the electronics industry, including in the areas of integrated circuit (IC) design, layout, structure, and operation, in the design and analysis of transistor-based digital and analog circuits, in RF technology for wireless communications, in technology development, and in technical and business development.

5. My curriculum vitae contains further details regarding my experience, education, publications, and other qualifications that allow me to render expert opinions in connection with this proceeding.

III. COMPENSATION

6. I am being compensated for my work in this matter at an hourly rate of $425 for consulting services. My compensation does not depend on the content of my opinions or the outcome of this proceeding.

IV. MATERIALS CONSIDERED

7. In preparing this declaration, I reviewed and considered the following materials, along with any other materials referenced in the body of my declaration:

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Exhibit	Description
1004	U.S. Patent Publication No. 2011/057190A1 ("Kimura")
1005	U.S. Patent Publication No. 2007/0063950A1 ("Shin")
1006	U.S. Patent Publication No. 2008/0101529A1 ("Tobita")
1007	U.S. Patent Publication No. 2008/0062097A1 ("Jeong")
1008	Excerpts from *Analog Integrated Circuit Design*, David A. Johns et al., John Wiley & Sons, Inc. (1997)
1009	Complainant's Opening Claim Construction Brief, *In the Matter of Certain Active Matrix Organic Light-Emitting Diode Display Panels and Modules for Mobile Devices, and Components Thereof*, Inv. No. 337-TA-1351
1010	Excerpts from *Physics and Technology of Semiconductor Devices*, A. Grove, John Wiley & Sons (1967)
1011	Excerpts from *CMOS Digital Integrated Circuits: Analysis and Design*, (third edition), S. Kang et al., McGraw-Hill (2003)
1013	U.S. Patent Publication No. 2003/0132931A1 ("Kimura '931")
1014	U.S. Patent Publication No. 2005/0185752A1 ("Sasaki")
1015	U.S. Patent Publication No. 2007/0139348A1 ("Lee")
1016	U.S. Patent No. 4,720,815 ("Ogawa")
1017	EP 0 138 406 A2 ("Takemae")
1018	U.S. Patent No. 4,740,922 ("Ogawa II")
1019	Excerpts from Wolf, "Silicon Processing for the VLSI Era: Volume 2 – Process Integration" (1990)

1020	U.S. Patent Publication No. 2007/0263763 A1 to Moon ("Moon")
1022	J. Miller, "Dependence of the input impedance of a three-electrode vacuum tube upon the load in the plate circuit," Scientific Papers of the Bureau of Standards, 15(351), pp. 367–385 (1920)
1023	US Patent Publication No. 2007/0085808A1 ("Lee")
1024	US Patent Publication No. 2009/0115792A1 ("Otose")

8. I may use these documents and information, or other information obtained during the course of this proceeding, as well as representative charts, graphs, schematics and diagrams, animations, and models based on those documents and information, to support and to explain my testimony.

9. My opinions are based in part on a review and analysis of the above-mentioned documents and materials. I have also drawn on my education, experience, and knowledge of basic engineering and circuit design principles in forming my opinions.

V. UNDERSTANDING OF THE LAW

A. Legal Standards

10. I am not an attorney, but I have been informed of several legal principles, which I have employed in forming my opinions in this declaration. I have been informed that each patent claim is considered separately for purposes of patentability and that a dependent claim that depends from another claim includes all of the limitations of the claim it depends from.

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1. Claim Construction

11. I have been informed that the claims of the challenged patent in this proceeding are to be construed using the same claim construction standard applied in district court. I have been informed the claim construction analysis begins with the ordinary meaning of a claim term, and there is a presumption that the term carries its plain and ordinary meaning to persons of ordinary skill in the art as of the effective filing date of the patent. I have also been informed that the most important sources for determining the meaning of a claim term are the claims, the specification, and the prosecution history of the patent at issue, which collectively is called "intrinsic evidence." I have been further informed that the meaning of a claim term may also be guided by "extrinsic evidence," such as contemporaneous dictionaries and treatises, as well as the testimony of technically skilled witnesses such as myself.

2. Burden of Proof

12. I have been informed that the petitioner in an *inter partes* review bears the burden of establishing unpatentability by "a preponderance of the evidence." I have been further informed and understand that, to prove an assertion by "a preponderance of the evidence," the party with the burden of proof must demonstrate that it is more likely than not that the assertion is true.

3. Obviousness

13. I have been informed that a patent claim is unpatentable if it would have been obvious to a person of ordinary skill in the art ("POSITA") at the time of the

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claimed invention. I have been further informed that a claimed invention is not patentable if differences between it and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. I have been informed that factors relevant to the determination of obviousness include the scope and content of the prior art, the level of ordinary skill in the art at the time of the invention, differences between the claimed invention and the prior art, and "secondary considerations" or objective indicia of non-obviousness.

14. I have been informed that a single reference alone can render a patent claim obvious, if any differences between the reference and the claim would have been known or obvious to a POSITA at the time of the invention. That is, if the POSITA could have adapted the reference to meet the claims of the patent by applying known concepts to achieve expected results, then the patent claims are rendered obvious by that reference.

15. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yielding predictable results. I have been further informed and understand that when a patent claim simply arranges old elements with each performing the same function it had been known to perform, and yields no more than one of ordinary skill would expect from such an arrangement, the combination is obvious.

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16. I have been informed that a patent claim composed of several limitations is not obvious merely because each limitation was independently known in the prior art. Hindsight reasoning is not an appropriate basis for combining references to form an obviousness combination. I have been further informed that it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine multiple prior art references, or multiple teachings of the same prior art reference.

17. I have been informed that various "secondary considerations" (sometimes referred to as objective indicia of non-obviousness) may support a determination of non-obviousness and that such secondary considerations must be considered as part of an obviousness analysis. I have been informed that even strong evidence of secondary considerations may not be sufficient to rebut a strong showing of obviousness. I have been informed that the patentee bears the burden of showing the existence and effect of secondary considerations of non-obviousness, after which the burden of coming forward with rebuttal evidence shifts to the party arguing obviousness. I have been informed that the following secondary considerations may indicate non-obviousness:

18. Copying: evidence that others, including the accused infringer, copied the patented invention.

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19. Long-standing problem or need: evidence of a persistent problem or need in the art that was resolved by the patented invention.

20. Prior failure: evidence that others have tried and failed to solve the problem or failed to provide the need resolved by the claimed invention.

21. Commercial acquiescence of competitors: the willingness of industry to license the patent at issue.

22. Skepticism: evidence that those of ordinary skill in the art were skeptical as to the merits of the invention.

23. Praise: evidence of praise directed to an invention by others in the field.

24. Unexpected results: evidence that those of ordinary skill in the art were surprised by the capabilities of the claimed invention.

25. I have also been informed that the near-simultaneous invention by others can be evidence that a claimed invention is obvious. I have further been informed that the patentee bears the burden of showing a "nexus" between the claimed invention and the evidence proffered on secondary considerations (*e.g.*, proof of commercial success of a product that practices the claimed invention is not enough; there must be evidence that the commercial success resulted, at least in part, from the claimed invention).

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B. Priority Date

26. I have been informed that a U.S. patent may claim "priority" to the filing date of one or more earlier filed applications. I have been informed that the priority date, also called the "effective filing date," is the earliest filing date to which a claim is entitled – and that such date is relevant for determining what qualifies as prior art. I understand that a claim must have written description support in the application(s) to which it claims priority to be entitled to an earlier effective filing date. I have been informed that the priority date determination is done on a claim-by-claim basis, and that claims in the same patent may have different priority dates.

C. Level of Skill in the Art

27. I have been informed that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons one of ordinary skill in the art may have for combining references.

28. I have been informed that factors that may be considered in determining the level of ordinary skill include: (1) the type of problems encountered in the art; (2) prior art solutions to those problems; (3) rapidity with which innovations are made; (4) sophistication of the technology; and (5) education level of active workers in the relevant field. I have been further informed that a POSITA is also a person of ordinary creativity.

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29. The challenged patent pertains generally to the field of OLED displays, and more particularly to the circuitry used to drive and control the pixels that comprise the light-generating elements of the display. A person of ordinary skill in the art in the technology field of the ’593 patent at the time of the alleged invention would have had a Bachelor’s degree in electrical engineering or a similar discipline, along with 2-3 years of circuit design experience. A Master’s or Ph.D. degree in a relevant field may substitute for some work experience and vice versa. I was at the time of the alleged invention at least a POSITA in the art relevant to the challenged patent. Further, based on my experience, I understand and know of the capabilities of a POSITA in 2012 – and I am familiar with how a POSITA would have understood and used the terminology found in the challenged patent at the time of its filing, and with the state of the art at that time.

VI. SUMMARY OF OPINIONS

30. I have been asked to compare various prior art references to Claims 1-8, 14-22, and 25 of the ’593 patent (the “Challenged Claims”). In my opinion, the Challenged Claims are all unpatentable as anticipated or obvious – based on these prior art references, combined with the knowledge of a POSITA.

31. My substantive analysis in Section XII provides examples of why these prior art references render the Challenged Claims unpatentable. I reserve the right

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to cite and rely on additional portions of these references in any future declarations or depositions.

VII. TECHNOLOGY BACKGROUND

32. Before considering the ‘593 patent in detail, some background on the technology of the ‘593 patent should be considered. This involves both the basic notions of transistor-based circuits, and of light-emitting elements (and their use in display screens).

A. Fundamental Concepts of Transistor-Based Circuit Design

33. Ever since the invention of the first transistor in 1947, transistors have been used as fundamental building blocks for the design of electronic circuits. Although a variety of transistor types have appeared over the years, by 2003 the transistor space was overwhelmingly dominated by a type of transistor that is known as the “field-effect transistor” (for reasons that will be described below). The circuitry disclosed in the ‘593 patent is based on the use of field-effect transistors as the fundamental building blocks – with that particular type being known as a “thin-film transistor” (TFT); the TFT can be readily understood, due to its strong similarity to the better-known (and extremely ubiquitous) silicon-based metal-oxide-semiconductor field-effect transistor (MOSFET).[1]

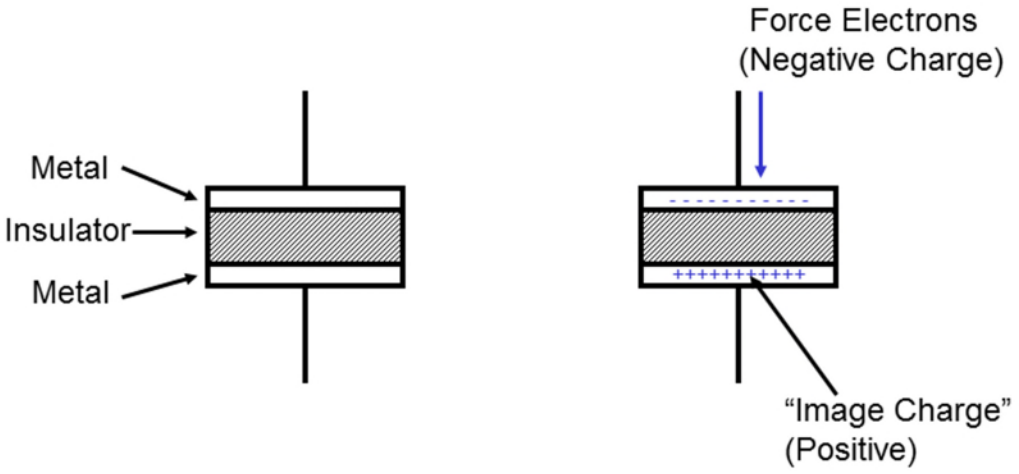
[1] It is the silicon MOSFET that has been the specific transistor type that has made “Moore’s Law” possible.

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34. Thus, before considering the ‘593 patent (and similar prior art), it is helpful to provide a brief overview of the basics of field-effect transistors and their usage in circuitry.

1. Field-Effect Transistors (FETs)

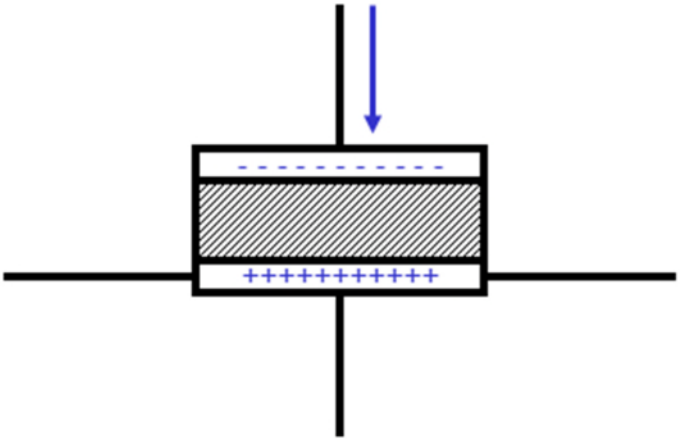
35. The field-effect transistor (FET) is actually based on a charge control mechanism that has long been known in the art – which is the simple charge control inherent in a basic capacitor.



When a negative charge (electrons) is forced onto one plate of the capacitor, basic electromagnetic theory requires that a corresponding “image charge” (i.e., an equal-but-opposite charge) appear on the other plate of the capacitor. In the same way, if a positive charge is forced onto one plate of the capacitor, an equal-but-opposite negative charge appears on the other plate of the capacitor. A capacitor will store charge and maintain a voltage until discharged.

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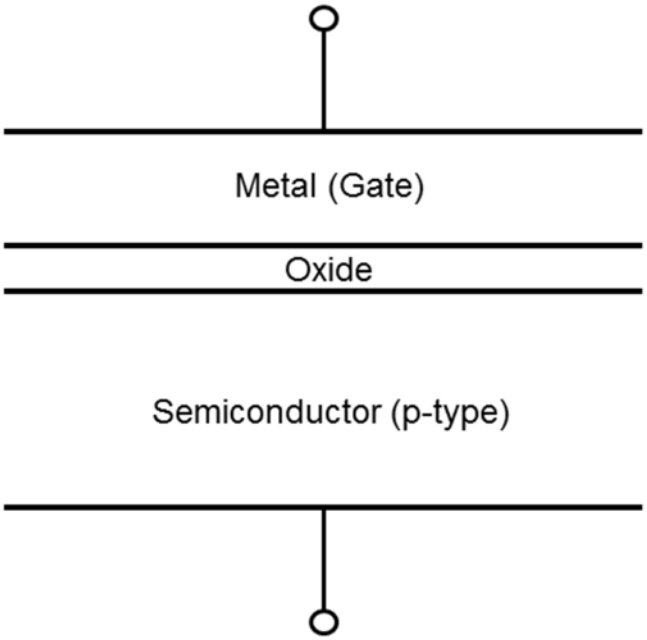
36. A field-effect transistor is based on using this ability (to create or remove a charge layer on the other plate of a capacitor as a charge-control mechanism) – combined with the addition of lateral contacts that allow current to flow when the image charge is present and to *not* flow when the image charge is absent.



This, of course, indicates the possibility of using this type of structure as an on/off switch (with no moving parts).

37. In 1955, it was discovered (accidentally) that an insulating silicon dioxide layer can easily be grown on top of a silicon semiconductor substrate; by depositing a metal layer (such as aluminum) on top of the oxide, a simple capacitor is formed.

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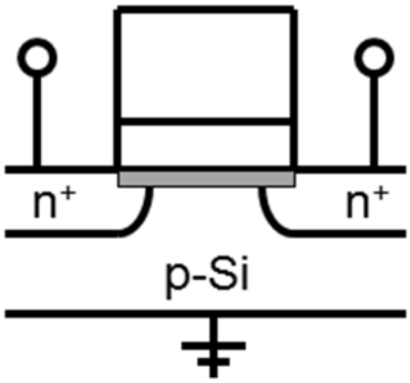


38. The silicon semiconductor layer is described as "p-type" – as it has (intentionally) been infused with a concentration of atoms of a species (usually boron) that contribute free positive (hence "p-type") charge to the silicon; these introduced impurity atoms are called "dopants," and the process of infusing them into silicon (or another semiconductor material) is known as "doping." When a positive charge is applied to the metal contact layer (i.e., the upper plate of the capacitor), a negative image charge forms at the surface of the silicon (as in a simple capacitor) – and is trapped there by the silicon dioxide insulator layer.

39. It was also long-known in the art that if other particular types of atoms (such as phosphorous and arsenic) are used as dopants, these atoms will cause negative-polarity free-charge to appear in the silicon – and it will be known as "n-type." If a very large amount of phosphorus or arsenic is infused into silicon that is

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already p-type, the n-type atoms will simply overwhelm (by sheer numbers) the p-type atoms – and the silicon so-infused will become selectively n-type. By infusing a small pocket of n-type atoms (in such a high concentration that the silicon becomes so strongly n-type that is often called "n+"), it is possible to create the sought-after two lateral contacts.



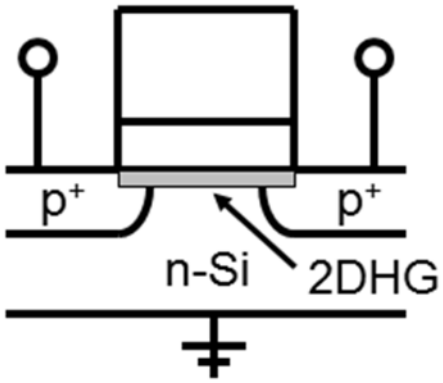
This structure provides the capacitor-with-lateral-contacts discussed earlier – so that the gate voltage controls the presence (shown in the figure) or absence of charge in the capacitor structure; meanwhile, the n^+ pockets provide the lateral contacts – so that current can flow (or not flow) based upon the presence of (or absence of) the induced charge layer; when the charge layer is present, applying a voltage difference between the lateral contacts will cause current to flow in the device. This type of transistor is known as an "nMOS transistor."

40. Also, while the MOS transistor clearly can be used as a simple on/off switch, it should be noted (for future reference herein) that the MOS transistor is a

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voltage-controlled current source – as the voltage on the gate controls whether or not (and to what degree) current flows between the lateral terminals.

41. Returning to the basic MOSFET structure, it is possible to reverse the polarities of the dopant atoms – so that the silicon substrate is n-type and the contact pockets are p^+.



Here, a negative voltage on the gate terminal will cause a positive charge layer to appear in the silicon, and current will flow when a voltage is applied between the two lateral terminals. This type of transistor is known as a "pMOS transistor."

42. It has long been known in the art that these two types of transistors (nMOS and pMOS) are not only structurally mirror images of each other – they are also electrical mirror images of each other. Writing in 1967, Andy Grove[2] (at pp. 329 – 330) described this situation for the two types of transistor:

[2] Ex. 1010, A. Grove, *Physics and Technology of Semiconductor Devices*, John Wiley & Sons, 1967.

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> The preceding discussion so far was for an *n*-channel device of the type where we have to apply a positive voltage to the gate in order to bring about the onset of channel conduction. By complete analogy, the discussion could have been applied to a *p*-channel where a negative gate voltage would have been required to bring about channel conduction. Because with zero gate voltage applied neither of these devices conducts, such devices are called *normally "off"* MOS transistors. (Emphasis in the original.)

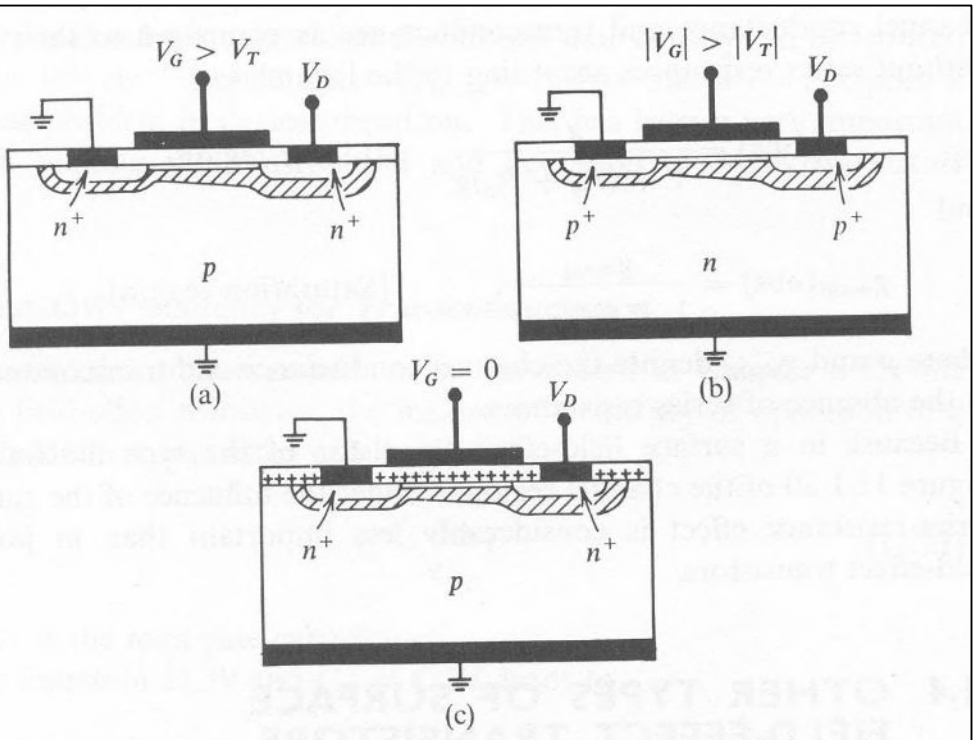


Fig. 11.8 Surface field-effect transistors with field-induced channels.
(a) Normally "off" *n*-channel device.
(b) Normally "off" *p*-channel device.
(c) Normally "on" *n*-channel device.

The MOS transistor was new at the time, and so this was the physics-based state of the art at the time.

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43. However, it was soon realized that nMOS transistors and pMOS transistors could be made to be "complementary" (a word-usage that will be explained momentarily) by changing the substrate bias that is applied to the pMOS transistor. As a more-recent textbook[3] on digital design states (at p. 71) the situation, "Notice that in order to be biased properly, the n-well region must also have a VDD contact." As is well-known in the art, the n-well provides the substrate contact (via which the substrate bias is applied) for a pMOS transistor in a typical silicon fabrication process.

44. However, as they are fabricated in (as the name indicates) a thin film (rather than in a silicon substrate), thin-film transistors are unable to have a substrate contact (of the type shown above, in the figure from Grove 1967); only a gate contact and the two lateral contacts (for the current flow) are available.

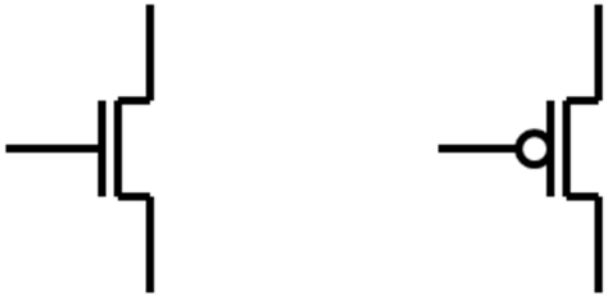
45. Thus, thin-film transistors will not be able to use the type of complementarity that is fundamental to silicon-based transistor technology (such as the ubiquitous complementary MOS (CMOS) technology that dominates the semiconductor landscape today). Instead, nMOS thin-film transistors and pMOS thin-film transistors must be operated as per the discussion in Grove 1967 that was quoted above – that in order to induce conduction in an nMOS transistor a positive

[3] Ex. 1011, S. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design* (third edition), McGraw-Hill, 2003.

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voltage must be applied to the gate, while in a pMOS transistor a negative voltage must be applied to the gate. In this way, nMOS and pMOS transistors are able to provide simple on/off switches – which turn on or off under mirror-opposite control voltages.

46. Further, the "complementary" situation also led, in the art, to the following simple circuit symbols for nMOS (left) and pMOS (right) transistor types.



An analog CMOS textbook[4] (from 1997) also shows commonly-used nMOS and pMOS transistor symbols. *See* EX1008 at 18 (especially Figure 1.7(a) and Figure 1.8(c)). The pMOS symbol in particular is notable for its inclusion of a small circle on the gate contact; this symbol is used in electronic circuitry (and digital-logic circuitry) to indicate "NOT" – which is a way of denoting a pMOS transistor as behaving in the opposite (i.e., "NOT") way as an nMOS transistor behaves.

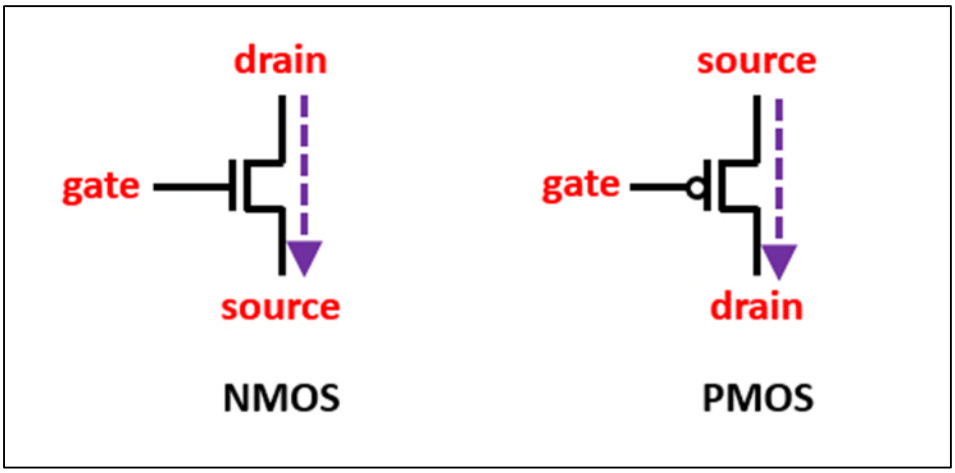
[4] Ex. 1008, D. Johns and K. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, 1997.

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47. Even though a pMOS thin-film transistor is not able be rendered "complementary" (as it lacks a substrate contact), the use of the pMOS symbol depicted above is still commonly used in the art to represent a pMOS TFT.

48. Further, although the MOS transistor is inherently a symmetric device, some way of separately identifying the two lateral terminals is required. For historical reasons, the side that provides the entry point for carrier flow came to be known as the "source," while the side that provides the exit point for the carrier flow came to be known as the "drain." However, defining the "direction" of the current flow is slightly problematic – as "current" is defined in the art (and has been for centuries) as the direction in which what would be positive charge flows; thus, for example, if there is a flow of negatively-charged electrons moving in some direction, the defined direction of the current flow is the *opposite* of the direction in which the electrons are actually moving.

49. This situation can be depicted graphically:



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This methodology allows the "source" and the "drain" to be defined via the direction of the current flow (which is determined by the relative voltages on the lateral terminals) in any particular transistor (of either type). This is explained succinctly in Chapter 1 of Johns & Martin 1997:

> It should be noted that there is no physical difference between the drain and the source. *The source terminal of an n-channel transistor is defined as whichever of the two terminals has a lower voltage.* For a p-channel transistor, the source would be the terminal with the higher voltage. When a transistor is turned on, current flows from the drain to the source in an n-channel transistor and from the source to the drain in a p-channel transistor. In both cases, the true carriers travel from the source to the drain, but the current directions are different because n-channel carriers (electrons) are negative, whereas p-channel carriers (holes) are positive.

Ex. 1008 at 16-17 (emphasis in original).

50. In most circuit applications, the flow of current through any transistor during circuit operation is one-way – that is, current flows through any particular transistor in only one of the two possible ways[5]; this allows the current flow to define what are the "source" and the "drain" of any transistor based on this operational characteristic. However, the MOS transistor is inherently a symmetric device – where the current can be induced to flow in either direction by the application of

[5] This is the case for the circuitry disclosed in the '593 patent, and for the prior art considered in this Declaration.

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different voltage differences between the two lateral terminals; a prominent example of this situation is the single transistor which controls the charge-storage node of a DRAM memory cell – where different lateral voltages (i.e., positive or negative) are used to put charge into the storage node and to take charge out of the storage node. In theory, the "source" and the "drain" would be swapped back-and-forth during these different circuit operations – even though there is (obviously) no material change in the transistor itself. Further, when a circuit "netlist" is created (usually for purposes of describing the circuit to a circuit simulation CAD tool, such as a SPICE circuit simulator), the four terminals of a MOS transistor (the drain, the gate, the source, and the substrate) must be explicitly specified – and will not be changed "on the fly" based on the voltages applied to a particular transistor; however, in this type of situation, if the sign of the voltage between the drain and source is reversed, the circuit simulator will simply cope with this – since, as mentioned above, the MOS transistor is inherently symmetric (and can be "operated" in either direction).

51. Fortunately (as mentioned above) this complex issue need not be of concern here – since (as also mentioned above) the circuitry described in the '593 patent (and in the prior art to be discussed later in this Declaration) operates such that current will only flow through any MOS transistor in one direction only. Thus, the scheme discussed above (and depicted in the figure above) of defining the "source" and the "drain" in terms of the current flow in the type of device in question

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(nMOS or pMOS) is workable here; thus, the working definition of "source" and "drain" will be used in this Declaration.

52. Finally, with respect to field-effect transistors in general and the '593 patent in particular, as was noted above the field-effect transistors in the '593 patent are of type known as a thin-film transistor (TFT). A TFT is sufficiently similar to a MOSFET (or, basically, any other type of field-effect transistor) to allow the basic understandings and descriptions (both qualitative and quantitative) associated with the ubiquitous MOSFET (as detailed above) to be applied to the TFT. The patentee was aware of this basic relationship (as would be a POSITA) – and used it (as will be detailed later) to describe the TFTs that appear in the '593 patent.

53. TFTs are very advantageous in display applications – as they can be fabricated directly on the glass that is used in the display; however, TFTs (as just noted) are still field-effect transistors – and operate in the same way as do silicon-based field-effect transistors (as described above).

2. nMOS/pMOS Interchangeability

54. As detailed above, the nMOS transistor and the pMOS transistor are essentially mirror images of each other. Furthermore, as was detailed earlier, a field-effect transistor, in its simplest usage, provides an electronic on/off switch with no moving parts – and this statement applies to both nMOS and pMOS transistors. This

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has long been well-known in the art – as can be seen in Kang and Leblebici 2003 (Ex. 1011 at 198):

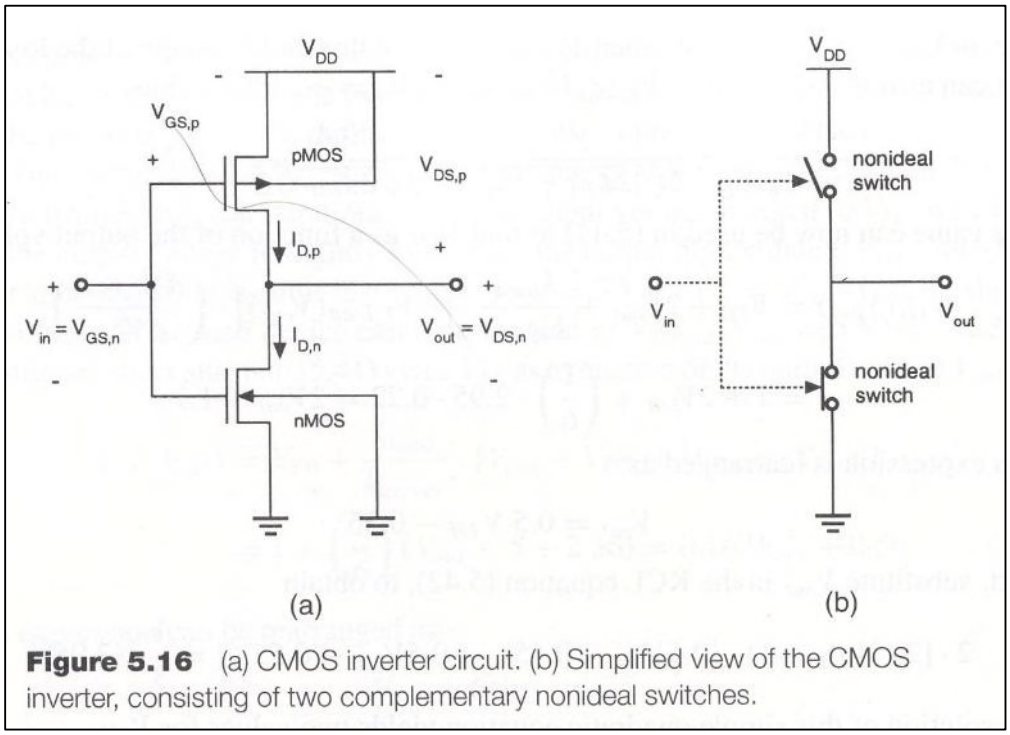


Figure 5.16 (a) CMOS inverter circuit. (b) Simplified view of the CMOS inverter, consisting of two complementary nonideal switches.

55. If the design need is for a transistor to be used as a simple on/off switch, then either an nMOS transistor or a pMOS transistor can be chosen – since, as shown in the figure from Kang and Leblebici 2003 above, each can function as a simple on-off switch. As the primary operational difference between nMOS and pMOS (when a simple switch is desired) is that the on/off characteristics are the opposite of each other – and the on-off signals to be applied must be altered (i.e., reversed as it were) to account for this. In particular, as described in Section VII.A.1, nMOS devices turn on in response to a "high" voltage on the gate terminal and turn off when a "low" voltage is applied. This is known in the art as "active-high" signaling. pMOS

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transistors are just the opposite – they turn on when a "low" voltage is applied to the gate terminal and turn off in response to a "high" voltage on the gate. This is known in the art as "active-low" signaling. Changing the polarity of a switching transistor (from nMOS to pMOS or vice versa) would require changing the polarity of the gate signal to achieve the same functionality, but doing so was easy and well-known to a POSITA by the effective filing date of the '593 patent. For example, U.S. Patent Publication No. 2003/0132931 ("Kimura '931") (Ex. 1013) teaches replacing nMOS transistors with pMOS transistors when the transistors function as simple on/off switches. *See, e.g.*, Ex. 1013, [0438] ("Note that a structure is used [in Figs. 3B-3D] in which the TFTs 304 and 306 are n-channel TFTs.…**However, the TFTs 304 and 306 function as simple switching devices, and therefore any polarity may be used.**" (Emphasis added)); *id*., [0396] (same for Figs. 1B-2); *id.*, [0445] (same for Figs. 4B-4D); *id*., [0649] ("All other TFTs are only used as switching devices for performing only on and off control, and therefore may be of any polarity."); *id*., [0362] (showing an all-pMOS driver circuit in Fig. 22). Note that it was well known at the time to a POSITA that "any polarity" refers to the use of either nMOS or pMOS transistors (and see also Figure 5.16 from Kang and Leblebici, above).

56. Further, beyond just generally teaching the interchangeability of nMOS and pMOS switching transistors, Kimura '931 actually provides further details about using pMOS transistors. For instance, Kimura '931 discusses the replacement of the

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first or fourth transistor in Figure 33 with a pMOS device – and even provides an example circuit in Figure 34A, where the fourth transistor is a pMOS device. *See* EX1013, [0659] ("[T]he polarity of one of the TFTs [first or fourth transistors] may be made opposite to the polarity of the other TFT…."). It was well-known to a POSITA at the time that "opposite polarity" refers to the two different transistor types – nMOS and pMOS (and again, see also Figure 5.16 from Kang and Leblebici, above).

57. As a further example, U.S. Patent Publication No. 2005/0185752 ("Sasaki") (Ex. 1014) presents two equivalent embodiments, in which the pMOS transistors of one embodiment (as depicted in Figure 4) are replaced by nMOS transistors in another embodiment (as depicted in Figure 18):

FIG.4

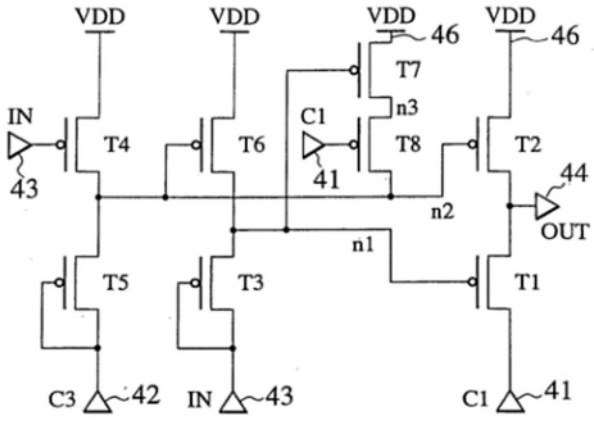
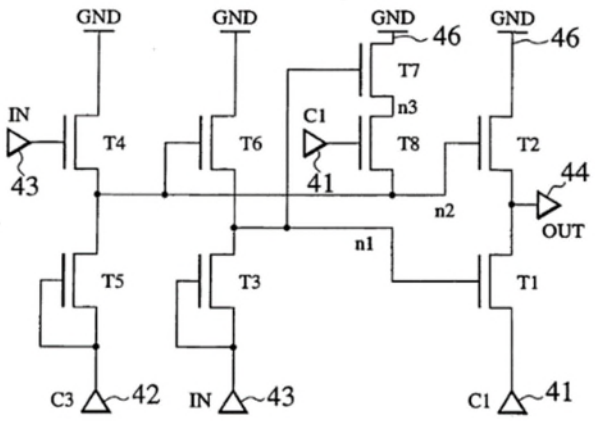


FIG.18



Ex. 1014, Figs. 4, 18. As Sasaki explains,

> Heretofore, description has been made throughout the first to the eighth embodiments regarding a case where the shift register is composed only of the p-MOS transistors for shifting the phase of the input signal IN having a concave waveform. Alternatively, it is also possible to arrange a shift resister composed only of n-MOS transistors for shifting a phase of an input Signal IN having a convex waveform. As shown in FIG. 18, all the transistors in the shift register of a ninth embodiment are n-MOS transistors. This shift register has a constitution where all the transistors shown in FIG. 4 are replaced by n-MOS transistors, and the voltage electrode 46 is connected to the ground potential GND. As a matter of course, without limitation to the shift register of FIG. 4, n-MOS transistors may replace the p-MOS transistors of the shift register in any of the other embodiments.

Ex. 1014, [0084]. Note that, in contrast to Kimura '931, Sasaki's architecture requires a wholesale usage of transistors of all one polarity or the other (i.e., all-nMOS or all-pMOS), and the change from the VDD connections at the top (pMOS implementation) to GND connections at the top (nMOS implementation); however,

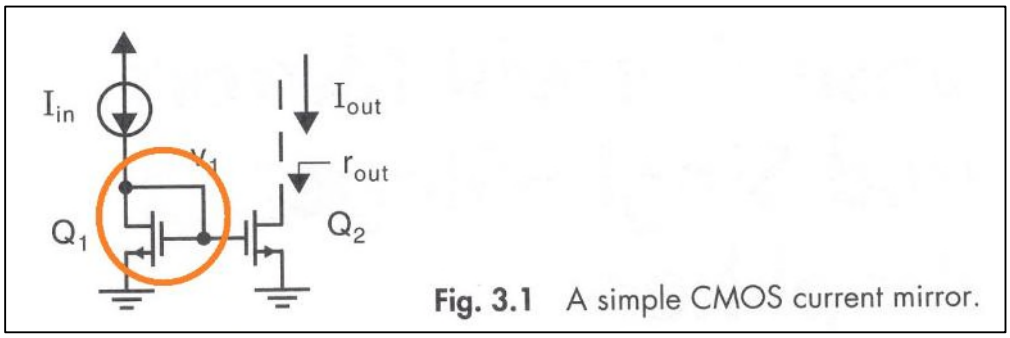
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the basic notion of the simple ability to exchange nMOS switching transistors for pMOS switching transistors is clearly shown.

58. These two examples confirm, as stated above, that it was well known in the art at the time of the '593 patent that, when used as simple switches, nMOS transistors and pMOS transistors are interchangeable.

3. The Diode-Connected Configuration of a Field-Effect Transistor

59. To connect a transistor "in the form of a diode" is something that is well-known in the art – and refers to a configuration of a field-effect transistor in which the gate of the transistor is directly connected to either the source or the drain of that same transistor. For example, Johns and Martins 1997 illustrates this well-known configuration being used in a current mirror:



Ex. 1008 at 125-126; annotation added. Referring to this figure, this text states (on p. 125): "Note that Q1 is diode-connected (i.e., its drain and gate are connected)…." As can be seen, in this configuration, the gate and the drain are directly connected together – so that the voltages on these two transistor terminals will always be the

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same in this configuration. As the gate/drain voltage is increased above the threshold voltage, the output current increases in a form that strongly resembles the current-voltage characteristic of a forward-biased diode – and hence the name of this structure, even though the transistor is not actually functioning explicitly as a diode does.

4. The Transistor Threshold Voltage

60. In Section VII.A.1, the basic notions of field-effect transistors were presented. In particular, for the simplified case of the use of such transistors as simple on/off switches, the operational considerations for the transistors involved are also rather simple.

61. However, one issue that was glossed over is how the "off" state and the "on" state are differentiated from each other – other than that these two operational states actually exist. The only other consideration (to be discussed below) is to make sure that the "on" state is really on, and (more challenging) that the "off" state is really off.

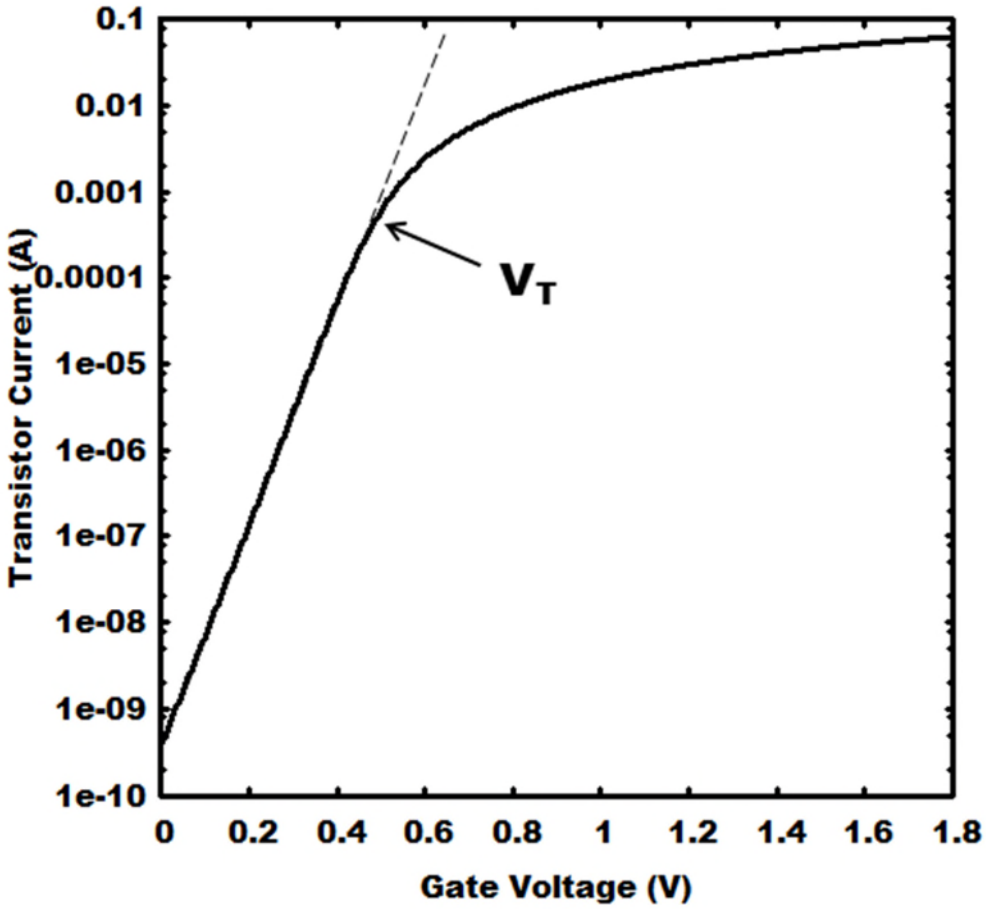
62. In Section VII.A.1, it was described how a field-effect transistor is turned on or off by changing the gate voltage from either high-to-low or low-to-high). That the "change" must occur at *some* particular (and identifiable) gate voltage value (for a particular transistor); that particular voltage value has long been known in the art as the "threshold voltage." *See*, *e.g.*, Ex. 1008 at 20.

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63. In an ideal transistor, for a gate voltage below the threshold voltage, the transistor would simply be completely off (i.e., absolutely *no* current flowing through it), while for a gate voltage above the threshold voltage, the transistor would be in a completely-on state (i.e., for any gate voltage above the threshold voltage, the current is constant at the "on" current level). In fact, in this situation, the actual value of the threshold voltage would essentially not matter – as long as it was somewhere between the low voltage level and the high voltage level (of the on/off logic voltage levels).

64. However, the field-effect transistor is not so simple a structure – and the threshold voltage behavior is much more complex. This is readily illustrated by an exemplary depiction of the device current (in logarithmic scale) versus the applied gate voltage.

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In this figure, the threshold voltage can be defined via the point where the straight line at low gate voltage changes (as the gate voltage increases) to the more-slowly increasing curve.

65. This curve shows that the MOS transistor does not, in detail, operate explicitly as a simple on/off switch; rather, the behavior of the current as a function of the gate voltage shows what was stated earlier – that in detail, the MOS transistor (like all field-effect transistors) is a voltage-controlled current source. In addition, this curve highlights the two critical issues that revolve around the "threshold

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voltage" *not* being able to exist as a simple dividing point between (as described above) all-off and all-on.

66. First, it can be easily seen that for gate voltages above the threshold voltage, the current is not a constant with gate voltage – but, rather, increases noticeably for higher gate voltages. As circuit switching speed is (among other things) a direct function of the current, it is desirable (in the on state) to have as much current as possible flowing through the transistor – which indicates that the threshold voltage should be as low as possible.

67. Second, though, it can also be seen that the characteristic behavior of a field-effect transistor is not ideal – in that the transistor current does not go to zero just below the threshold voltage, but rather decreases (exponentially) as the gate voltage decreases below the threshold voltage. As a result, the threshold voltage has to be chosen (during manufacturing-process design) to be somewhat higher than the desired near-zero gate-voltage value – so that the off-state current that flows through the transistor will not be too large.

68. In sum, the value of the threshold voltage should be as low as possible – but not lower; otherwise, even though the transistor will be to some degree "off," there will be too much current flowing in the "off" state – which is something that can have serious-and-unpleasant consequences in most circuit applications.

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B. Pixel-Based Displays

69. As the title of the ‘593 patent indicates, the ‘593 patent involves displays. As the ‘593 patent makes clear (such as in Figure 1), these displays are comprised of pixels – wherein a “pixel” (short for picture element) is a single dot in the display, and a very large number of such pixels are constructed together, so that the pixels can, collectively, produce an image on the display.

70. There are two notably aspects of such displays that are material to the disclosures of the ‘593 patent. One is the particular technology that is used for the fabrication and operation of the pixels themselves, and the other is the organization and control of the set of pixels in a display (so that an image can be created on the display); these two issues will be considered in turn, with the second issue being divided into two separate sections.

1. Pixel Technologies

71. As its title indicates (via “organic light emitting display”), the ‘593 patent involves the use of organic light-emitting diodes (OLEDs). OLEDs are able to be used in pixels (to create an image on a display), since they will emit light – and will do so under the control of electronic circuitry. OLEDs function in basically the same manner as do conventional LEDs – but they have come into wide use in

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displays, for a variety of reasons. Among the noted advantages[6] of OLEDs (particularly when used in displays) are the lighter materials involved (which are plastic), flexibility (again, because OLEDs use plastic material), greater brightness, lower power consumption, and ease of manufacturing (as they can be produced in sheet form rather than as individual LEDs).

72. However, other types of pixel technologies were well known in the art (and had been for some time). One prominent example is liquid crystal display (LCD) technology. As the name implies, an LCD pixel involves a liquid crystal – with the key aspect that the liquid crystal configuration can be changed using an applied electric field; the applied field is able to change the configuration of the liquid crystal from one of two possible forms to the other, with the configuration remaining in place even after the electric field is removed. The state of the liquid crystal can thus be induced by applying an electric field – so that the liquid crystal (working in tandem with polarizers) either passes or blocks the passage of light. By placing a liquid crystal in front of backlight, the light can be allowed to pass, or it can be blocked; by using a large number of such liquid crystals as pixels, an image can be created on a display by controlling each pixel as an individual unit (in

[6] https://electronics.howstuffworks.com/oled5.htm.

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essentially the same general way as is done with LED/OLED-based pixels in displays based on LEDs/OLEDs).

73. Like OLED technology, LCD technology allows for the easy creation, along with the pixel-base technology, of thin-film transistors (TFTs) in the same manufacturing process. Thus, again like OLEDs, the control circuitry for LCDs can be created *in-situ* with the pixels – so that the control circuitry need not be separate.

74. LCD TFTs provide the same advantages as those discussed above with respect to OLEDs. LCD displays are often preferable in situations where either cost or power consumption (or both) is of high importance.

2. Pixels and Pixel Arrays

75. A pixel is the basic unit of a light-based display screen – with that display consisting of row and columns of pixels – with a higher pixel density leading to a higher resolution in the display. This row/column structure of a display is well-known in the art by the use of the number of rows and columns that a display has – such as 1280 x 720, 1920 x 1080, and so forth. Note that these numbers provide the total number of pixels in a display – irrespective of the physical size of the display. In general, it is the areal density of pixels in a display that defines the quality of the image that can be produced by a display. Each pixel includes driving circuitry that provides current to the diode; further, each pixel typically includes a "driving

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transistor" to provide current for the light emitting diode, and various "switching transistors" that act as on/off switches to control the operation of the pixel.

76. Further, as the numbers above indicate (and as mentioned in association with them), in a display, the pixels are arranged into rows and columns – and these row and columns of the display are activated sequentially to produce images on a display screen.

77. In addition to pixel density, the quality of a display image is also a function of the brightness of the pixels – with brighter pixels generally leading to better image quality.

3. Scan Lines and Control Signals in a Display

78. As noted above, in a display based on pixels, the pixels are typically arranged in a row-and-column fashion. In operation, the individual pixels are generally not all "fired" simultaneously – that is, as individual pixels must change (i.e., turn on or off) when the image to be displayed changes, the individual pixels typically do not all change together at the same time.

79. Rather, a technique that has been used since the invention of screens that create dynamic images using some form of light (that is, going back to the earliest days of cathode-ray tubes (CRTs), such as those used in the first televisions) has been adopted. In this technique, the rows (sometimes called "lines") of the display are treated as the basic units for changing pixel output as the display image

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changes – with all the pixels of a single row being changed as needed, and then the same process being applied to the next row, etc. In the context of an OLED display or LCD (liquid crystal display), a "scan signal" or "scan line signal" generally refers to the aforementioned control signal that is used for programming a line/row of pixels. This process continues until the entire display has been refreshed – via this sequential refreshing of each row; further, once the entire display has been refreshed in sequence, the next overall refresh sequence can begin.[7] As long as the speed of the refresh rate is faster than the ability of the human eye to detect it, the viewer will perceive the entire image changing fluidly upon the screen.[8]

80. As can be inferred from this discussion, a significant amount of behind-the-scenes control circuitry has long been required to manage this rather intricate sort of screen-refresh operation. But this was a well-explored and well-understood technical field – wherein various basic circuit concepts were routinely mixed and

[7] There have long been variations on this basic theme – such as, for example, refreshing every other row in one refresh pass, then refreshing the previously-unrefreshed row in the next refresh path; however, the basic approach of refreshing the display by sequentially (in one form or another) refreshing rows of pixels remains essentially the same.

[8] If the refresh rate is "too slow," the human eye will perceive a noticeable (and unpleasant) flicker in the display.

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matched as needed to achieve a POSITA's design goals. It was this sort of control circuitry that is the main topic of the '593 patent.

VIII. THE CHALLENGED PATENT

81. U.S. Patent No. 9,330,593 ("the '593 patent" or "the challenged patent") is entitled "Stage Circuit and Organic Light Emitting Display Using the Same." The listed inventor is H. Jang. The '593 patent claims priority to a Korean application (No. 10-2012-0104512), which was filed on September 20, 2012.

82. For purposes of this declaration, I have been instructed to use September 20, 2012 as the effective filing date of the '593 patent. My opinions in this declaration were formed from the perspective of a POSITA as of September 20, 2012, including both the knowledge of a POSITA at that time as well as how a POSITA would have understood the prior art. My opinions, however, would be the same even if the patent is only entitled to a February 2013 filing date.

A. General Overview

83. As the title indicates, the '593 patent discloses circuitry that is used to control the OLED light emitters that are used in displays; the patentee claims that the disclosed circuitry is simpler and requires fewer transistors. As the '593 patent asserts, its embodiments "provide stages having a reduced number of transistors and that output scan signals only using first and second clock signals. In contrast, conventional stage circuits includes [sic] a plurality of transistors, e.g., at least ten

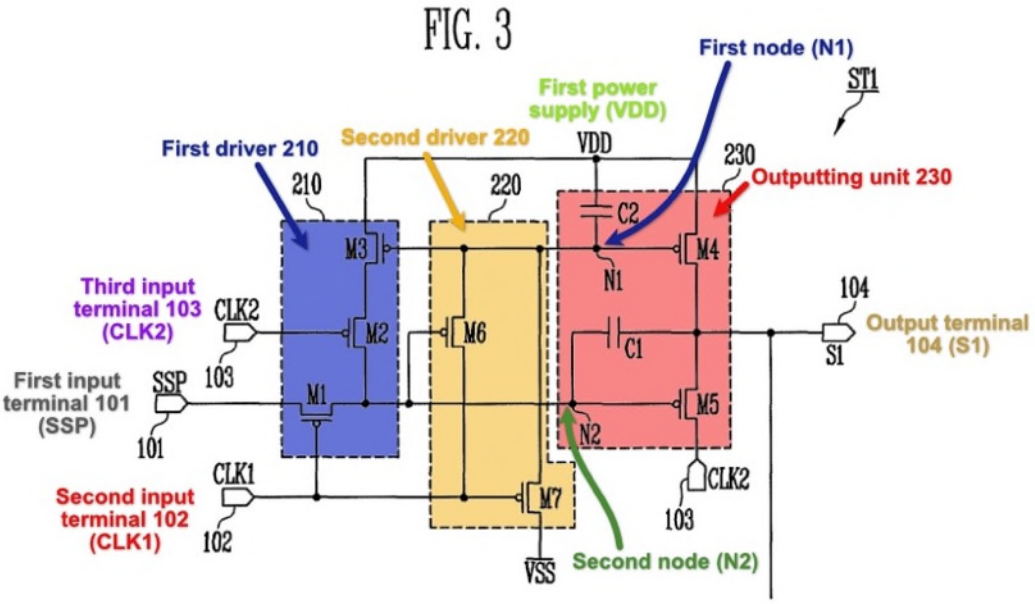
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transistors, to supply the scan signals and/or require use of initializing signal in addition to the first and second clock signals." ('593 patent at 9:12-18.)

84. The '593 patent goes on to explain what it considers to be the benefits of having a reduced number of transistors and initializing signals: "When a number of transistors in a stage increases, process yield deteriorates, so that stability of driving is deteriorated. When more initializing signals are required, there is less time for supplying scan signals, therey [sic] reducing stability. When a number of transistors is increased and/or more initializing signals are required, complexity increases. Therefore, stages according to embodiments, and an organic light emitting display using the same, improve stability and reduce complexity." (*Id.* at 9:18-26.) The '593 patent thus asserts that the components' arrangements in the circuits in its specification are the purported inventive concept, and are necessary to achieve these recited benefits. Consistent with Patent Owner's proposed constructions and infringement theories from the related ITC Investigation, however, the claims of the '593 patent impose no requirements on the number of transistors or initializing signals.

85. Figure 3 shows the preferred embodiment of the '593 patent. The annotated version of Figure 3, below, shows the correspondance the Figure 3 depiction and the circuit components and signals recited in independent Claims 1 and 15.

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Ex. 1001, Fig. 3. In the figure above—and in all similarly-annotated figures throughout this declaration—all color has been added.

86. As shown, the preferred embodiment of the ’593 patent comprises a first input terminal SSP, a second input terminal CLK1, a third input terminal CLK2, and an output terminal Sn, where n denotes the stage number. The first input terminal SSP receives either a start signal or the output signal from the previous stage, *e.g.*, Sn-1 for the n-th stage. *Id.*, 5:1-7. The second input terminal and the third input terminal receive two clock signals – wherein these two clock signals have the same period and nonoverlapping phases. *Id.*, 5:8-28. The circuits are partitioned into a first driver, a second driver, and an outputting unit. The first driver and the second driver control the voltage of the second node N2 and the first node N1, respectively. *Id.*, 5:63-67, 6:22-26. The outputting unit supplies a voltage to the

output terminal Sn according to the voltage at the first node or at the second node. *Id.*, 5:37-41. Note that the colored text in the above discussion (and throughout this declaration) is meant to match that used in the associated annotated figure.

87. "On/off transistor" M2 corresponds to the claim limitation: "the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver." It is the placement of transitor M2 in the first driver, having the "third input" coupled to its gate, where the "third input" is also applied to the outputting unit, that the patentee highlighted to overcome prior-art rejections during prosecution.

B. File History

88. The application which led eventually to the issuance of the '593 patent was filed with the USPTO on February 20, 2013, and claims priority to a Korean application (No. 10-2012-0104512), which was filed on September 20, 2012. This application was published on March 20, 2014 as US2014/0078029.

89. On October 21, 2014, the applicant received a non-final rejection from the USPTO, on the grounds that the application contained "independent or distinct" species – and the applicant was required (by law) "to elect a single disclosed species, or a single grouping of patentably indistinct species."

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90. On December 19, 2014, the applicant replied that were identifying a particular species, and as support provided a Korean patent application (KR 10-2013-0000020).

91. On February 9, 2015, the applicant received a non-final rejection from the USPTO. Claims 1-3, 5, 7, 8, 14-18, 20, 21, and 27 were rejected as being anticipated by Jeong (US2008/0062097), Claim 4 was rejected as being unpatentable based on Jeong in view of Chung (US2011/0227884), and Claims 6 and 19 were rejected as being unpatentable based on Jeong in view of Kim (US2012/0062525).

92. On May 5, 2015, the applicant provided a reply, in which Claims 1 and 14 were amended, Claims 9 - 13 and Claims 22 - 26 were withdrawn, and a new claim (Claim 28) was added.

93. On June 17, 2015, the applicant received a final rejection from the USPTO. Claims 1-3, 5, 7, 8, 14-18, 20, 21, 27 and 28 were rejected as being unpatentable based on Jeong in view of Lee (2011/0115835), Claim 4 was rejected as being unpatentable based on Jeong in view of Lee in further view of Chung, and Claims 6 and 19 were rejected as being unpatentable based on Jeong in view of Lee in further view of Kim.

94. On August 13, 2015, the applicant provided a reply, in which Claims 1, 2, 13, 14, 16, 17, and 26 - 28 were amended.

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95. Following an interview on August 21, 2015 (in which U.S. Patent 8,553,026 was discussed), on August 27, 2015 the Examiner provided a reply in which he stated that he "believes that CK2 of Fig. 3 of the '026 patent discloses Applicant's amended limitation and may anticipate claim 1."

96. On September 17, 2015, the applicant provided a reply, in which Claims 1, 2, 13, 14, 16, 17, and 26 - 28 were amended. The applicant argued that the amended claims including "the signal of the third input terminal directly ~~at least~~ controls an on/off operation of a transistor, the transistor included in the first driver ~~switch~~" were allowable over the Examiner's references.

97. On January 4, 2016, the Applicant received a notice of allowability. The reason of allowance cited the last amendment in reasons for allowance and withdrew the earlier restriction requirement. U.S Patent No. 9,330,593 issued on May 3, 2016.

C. Claim Construction

98. It is my understanding that the Board only construes particular claim terms of the patent at issue when necessary. Otherwise, all claim terms should be given their plain-and-ordinary meaning, as that meaning would have been understood by a person of ordinary skill in the art at the time of the alleged invention, taking into consideration the language of the claims, the specification, and the prosecution history.

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99. In this proceeding, consistent with Patent Owner's proposed constructions and infringement theories in the related ITC Investigation, I have applied plain-and-ordinary meaning to all claim terms – though I do not necessarily agree with Patent Owner that all claim terms should be construed based on their plain-and-ordinary meaning. Further, as I will describe in Section XII (below), there are certain terms for which I have provided further explanations of what that plain-and-ordinary meaning would have been to a POSITA as of the '593 patent's effective filing date.

100. Should the Board construe a term differently, I reserve the right to supplement my analysis and conclusions – particularly if the construction of any term changes the substance of my analysis and/or conclusions.

IX. OVERVIEW OF THE PRIOR ART REFERENCES

101. In the unpatentability analysis which follows in Section XII, five grounds of unpatentability are provided – based on four prior art references. A brief overview of each of these references will be provided here.

A. Kimura

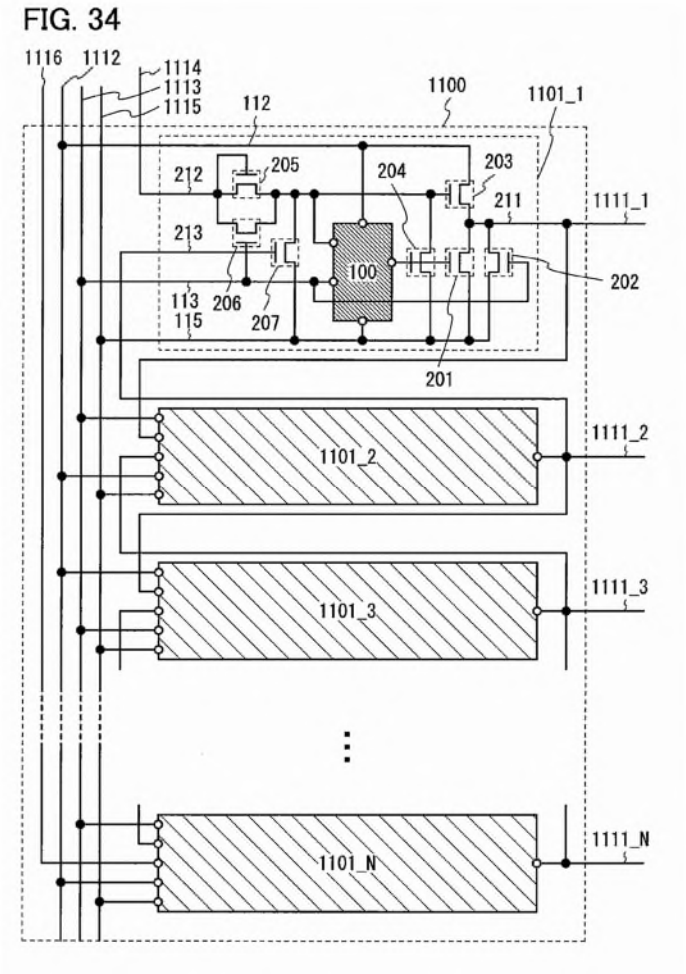
102. U.S. Patent Publication No. 2011/0057190 A1 to Kimura ("Kimura") was published on March 10, 2011, and is prior art to the '593 patent under at least 35 U.S.C. § 102(b). Kimura is not cited by the '593 patent, and was not considered during prosecution. *See generally* Exs. 1001, 1002.

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103. Kimura discloses "[a] semiconductor device and [a] display device." Kimura at title; by "semiconductor device," Kimura is referring to transistor-based circuitry. (See, e.g., Kimura at Abstract.)

104. In more detail, Kimura teaches "a display device, a pixel included in the display device and a shift register circuit included in the display device." Ex. 1004, ¶ [0320].

105. Kimura provides a description of such a shift-register in Figure 34 – where the shift register circuit is displayed largely in block-level form:

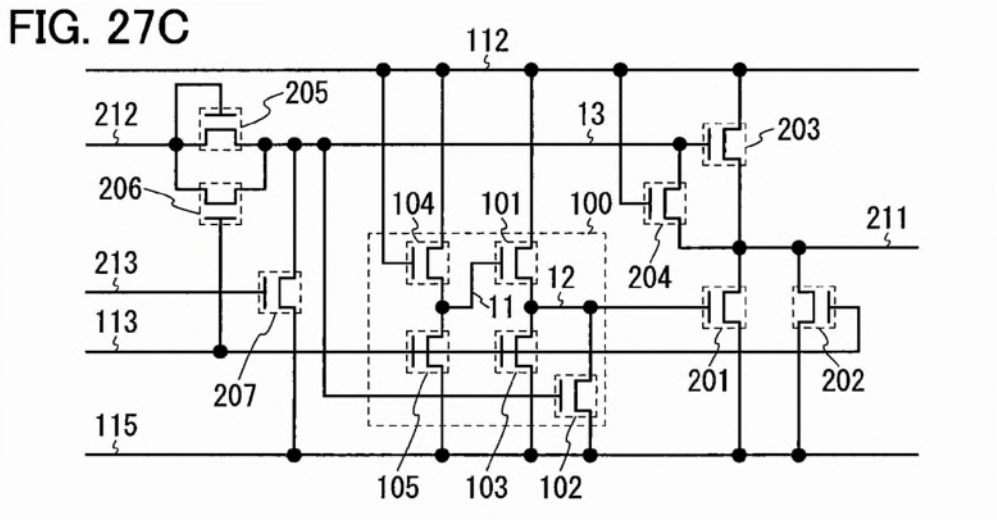


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Id., Figure 34. As Kimura explains, the "shift register circuit 1100 includes a plurality of flip-flop circuits 1101_1 to 1101_N (N is a natural number)." *Id.*, ¶ [0334]. Here, for the first flip-flop stage in the otherwise-block-level depiction, a particular embodiment is included (at the circuit level) for the first flip-flop stage; however, as Kimura states, this particular inclusion is merely exemplary – as a "semiconductor device [i.e., a flip-flop circuit] described in Embodiment 1 or 2 can be used for each of the flip-flop circuits 1101_1 to 1101_N." *Id.*

106. One possible such "semiconductor device" (i.e., flip-flop circuit) from "Embodiment 1 or 2" is provided in the embodiment of Figure 27C:

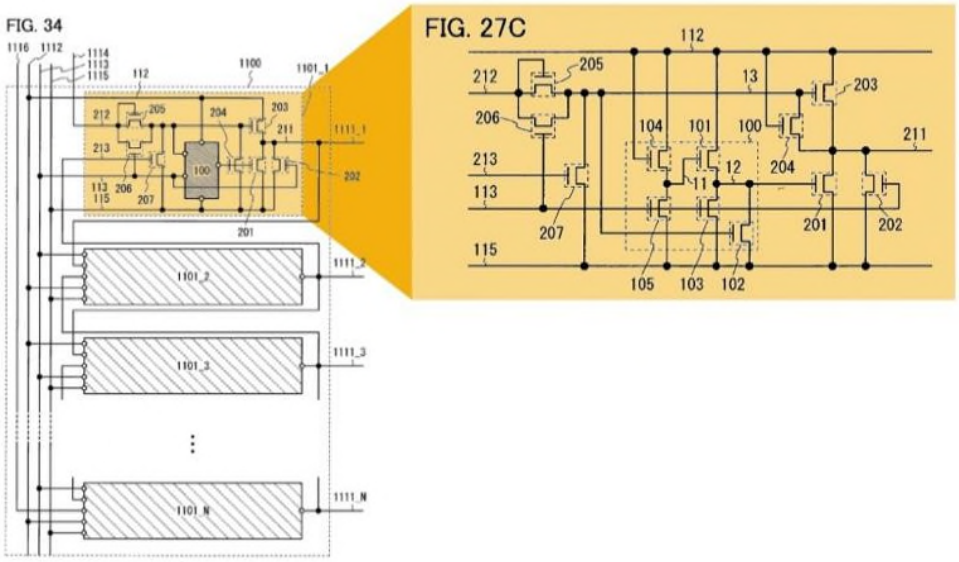
FIG. 27C



Id., Fig. 27C. Kimura identifies this flip-flop circuit as being such a "semiconductor device described in Embodiment 1 or 2" at ¶ [0072].

107. Thus, the flip-flop circuit embodiment of Figure 27C could also be used as the "semiconductor device" (i.e., flip-flop circuit) in the shift register circuitry of Figure 34; this can be illustrated as follows:

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Id., Figure 34 and Figure 27C (annotations added).

108. Kimura also discusses flip-flop circuitry "which does not easily deteriorate." (Kimura at Abstract.) In the specification, Kimura further-elaborates on this point – noting that "dielectric breakdown, deterioration, or the like of the transistor 101 can be prevented." *Id.*, ¶ [0206]; *see also* ¶¶ [0283], [0286]. Dielectric breakdown (which is either destructive and renders a transistor inoperative, or a more gradual process that degrades the transistor characteristics) and "deterioration" (i.e., the non-destructive but gradual degrading of transistor characteristics over time due hot-carrier injection) have long been well-known problems in the transistor art (and semiconductor physics).[9]

[9] See, for example, Wolf, "Silicon Processing for the VLSI Era: Volume 2 – Process Integration" (1990) (Ex. 1019) at 348-351, 468-472.

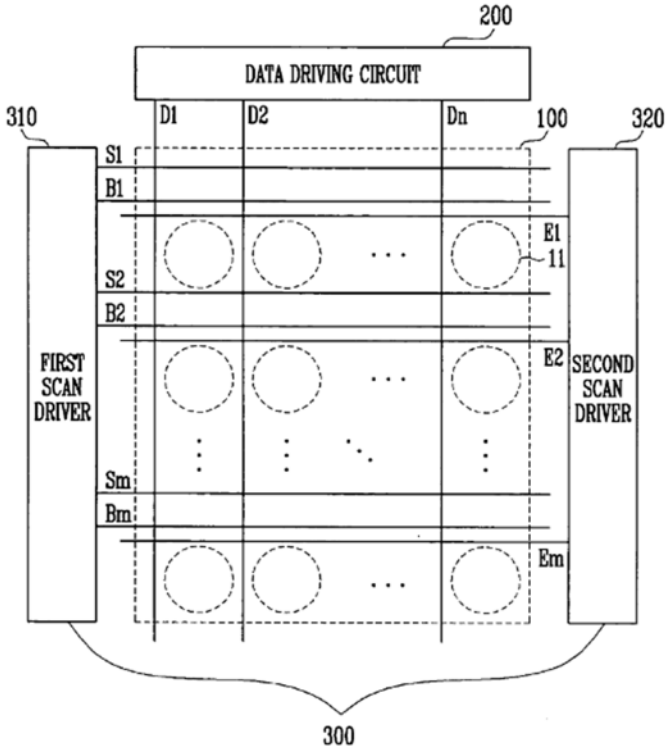
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B. Shin

109. U.S. Patent Publication No. 2007/0063950 A1 to Shin ("Shin") was published on March 22, 2007, and is prior art to the '593 patent under at least 35 U.S.C. § 102(b). Shin is not cited by the '593 patent, and was not considered during prosecution. *See generally* Exs. 1001, 1002.

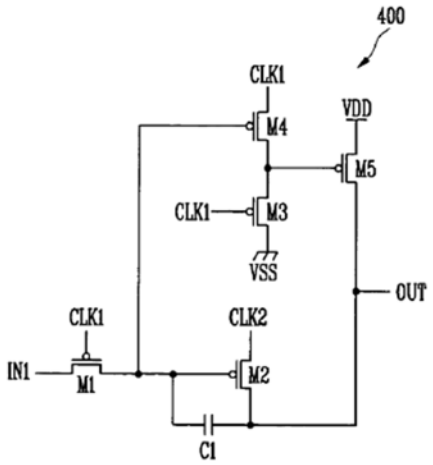
110. Shin discloses "an organic light emitting display, and more particular to a scan driving circuit used for a current programming type organic light emitting display." Ex. 1005, ¶ [0003]. Shin's "active matrix type of organic light emitting display includes a display panel, a data driving circuit, a scan driving circuit, and a timing controller. The scan driving circuit receives a scan drive control signal from the timing controller, generates a scan signal, and sequentially provides the scan signal to scan lines of the display panel. That is, the scan driving circuit functions to sequentially generate the scan signal to be provided to the display panel in order to drive pixels included in the display panel." *Id.*, ¶ [0009]. An embodiment of a circuit for driving such a display is shown below:

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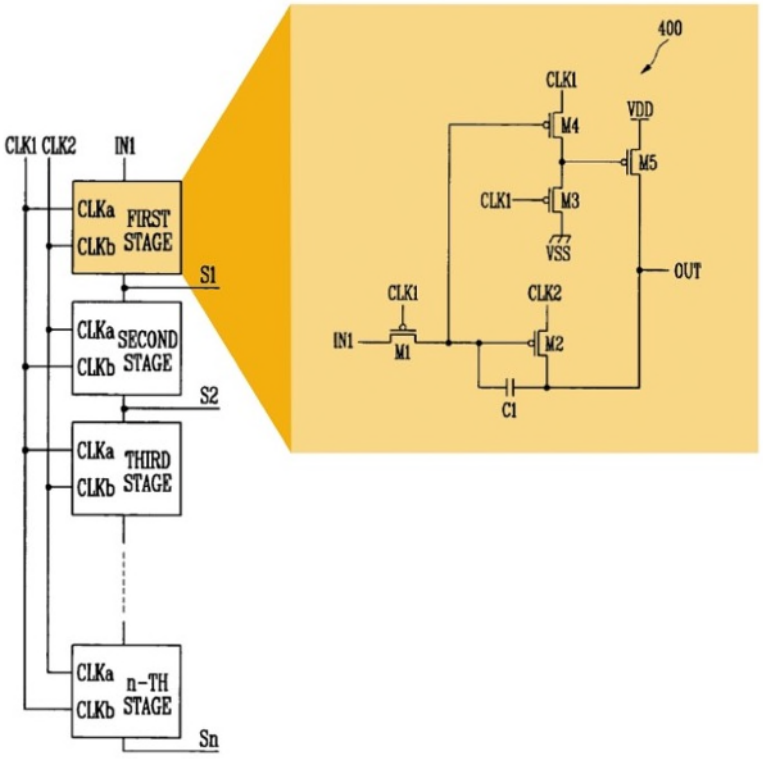
Id., Fig. 4.

111. The scan driving circuit 300 may comprise a cascade-connected, multistage shift register – in which a single stage can have the following configuration:



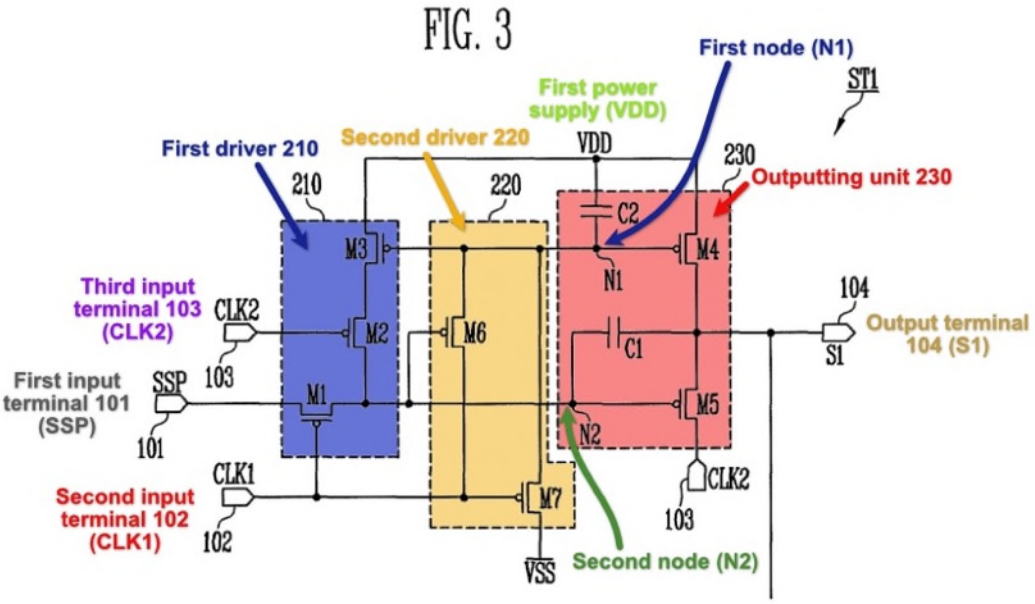
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Id., Fig. 11; *see also* ¶¶ [0047]-[0048], ¶ [0121]. This stage circuit is used as a building block for the cascade-connected, multistage shift register that was mentioned above; Shin provides a block-diagram depiction of this shift register in (e.g.) Figure 7 – with the stage circuit embodiment of Figure 11 being suitable for use as the stage circuit:



112. Depending on what part of this stage circuit is selected as the first driver, Shin's stage circuits may not include a specific set of transistors of the disclosed first driver, specifically the transistors located between the first power supply and the second node (*i.e.*, transistors M2 and M3) as shown in Figure 3 of the '593 patent specification:

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Ex. 1001, Fig. 3 (annotations added).

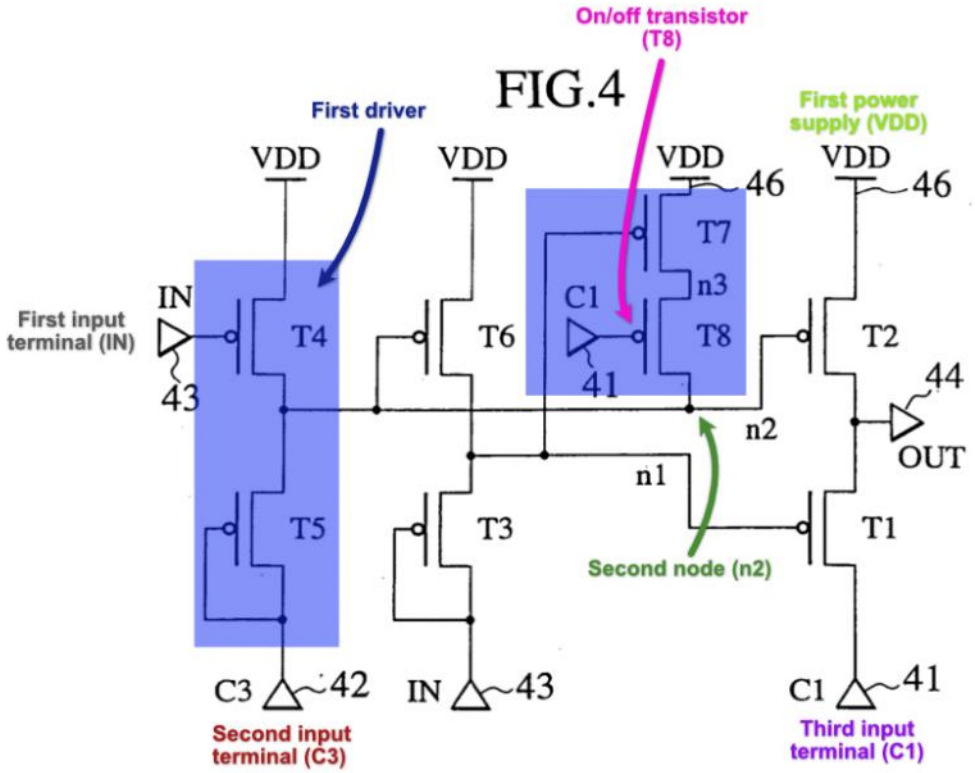
113. However, as discussed further below, a POSITA would have found it obvious to modify Shin to add additional circuitry (via adding additional transistors) to so as to provide a desired control scheme, and there certainly were no technical challenges to understanding how Shin's circuitry would predictably operate when that circuitry was added. A POSITA would have been motivated to combine Shin with Sasaki in this manner for at least the reasons discussed in Section IV.F.1 below.

C. Sasaki

114. U.S. Patent Publication No. 2005/0185752 A1 to Sasaki ("Sasaki") was published on August 25, 2005, and is prior art to the '593 patent under at least 35 U.S.C. § 102(b). Sasaki is not cited by the '593 patent, and was not considered during prosecution. *See generally* Exs. 1001, 1002.

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115. Sasaki discloses "a shift register in an electronic circuit being operated by a pulse-cut clock signal, and to a drive circuit, an electrode substrate and a display device that include [sic] the shift register." Ex. 1014, ¶ [0003]. An embodiment of Sasaki's shift register stage circuit is shown in Fig. 4:



Id., Fig. 4.

116. As seen above in Sasaki Figure 4, Sasaki provides multiple ways to control its second node n2, specifically it lowers the voltage on n2 when C3 is low via T5, it raises the voltage of n2 in response to initialization signal IN, and it further can raise the voltage of n2 through the use of what Sasaki calls an "anti-reversal

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circuit" (*Id.*, ¶ [0042] ("An anti-reversal circuit includes a seventh transistor T7 and an eighth transistor T8.")) that is formed using transistors T7 and T8 (configured as shown in Sasaki). This design provides control flexibility that would be appreciated by a POSITA. In particular, Sasaki teaches the benefits of this anti-reversal circuit, connected in series between the first power supply VDD and the second node n2, with the gate of T7 connected to the first node n1 and the gate of T8 connected to third input clock signal C1.

117. Sasaki describes the purpose of this anti-reversal circuit at several places in the specification; for example,

> The anti-reversal circuit prevents a voltage level at the control electrode of the second transistor T2 from being reversed, which is attributable to a floating state of the control electrode of the second transistor T2, where if a voltage level of the first clock signal C1 is reversed in the state where the first transistor T1 is turned on and the second transistor T2 is turned off.

Id., ¶ [0042].

118. This circuitry was added by Sasaki to make sure that the node is at the expected value before the control sequence stops; without this connection to reset the node, there is a risk that the voltage will be "reversed" from the expected value during the control sequence.

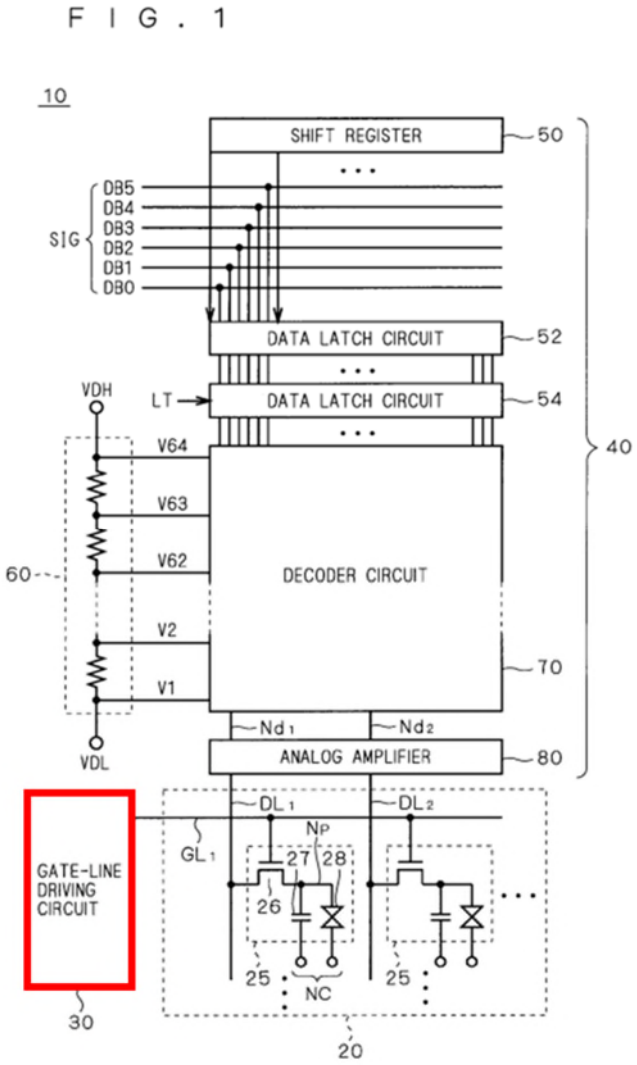
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D. Tobita

119. U.S. Patent Publication No. 2008/0101529 A1 to Tobita ("Tobita") was published on May 1, 2008, and is prior art to the '593 patent under at least 35 U.S.C. § 102(b). Tobita is not cited by the '593 patent, and was not considered during prosecution. *See generally* Exs. 1001, 1002.

120. Tobita discloses "a shift register for use as a scanning-line driving circuit for an image display apparatus." Ex. 1006, ¶ [0002]. This circuit may be used in a liquid crystal display ("LCD"); an LCD, like the later-developed OLED displays, comprises a matrix of pixels driven by scan lines and data lines. *Id.*, ¶¶ [0004], [0059]. An embodiment of a circuit that drives such a display is shown below:

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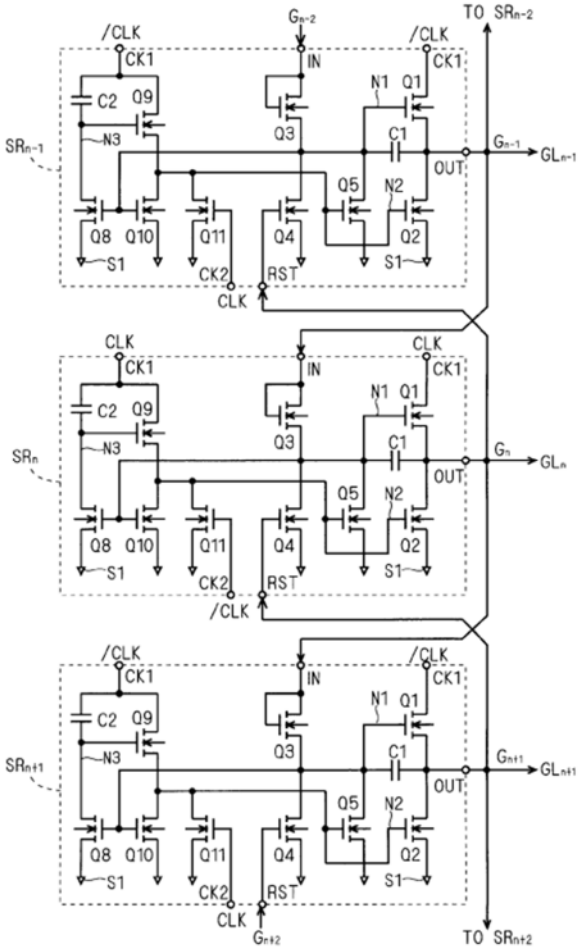


Id., Fig. 1.

121. The gate-line driving circuit (or scanning-line driving circuit) 30 may comprise a cascade-connected, multistage shift register as shown below:

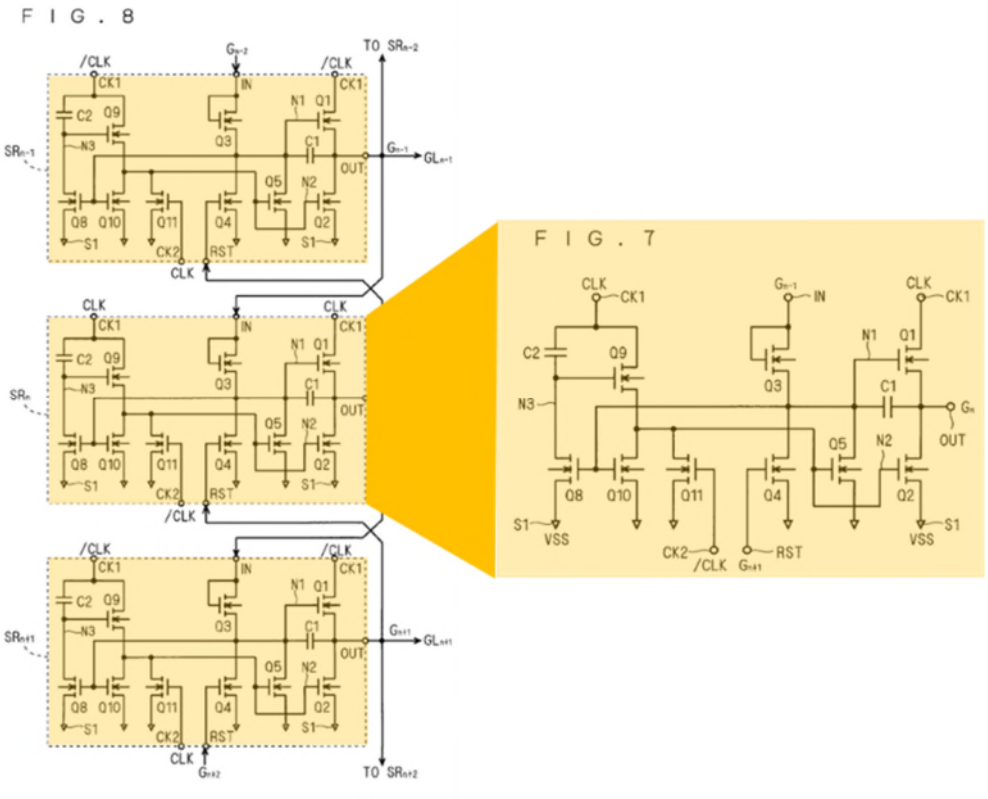
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FIG. 8



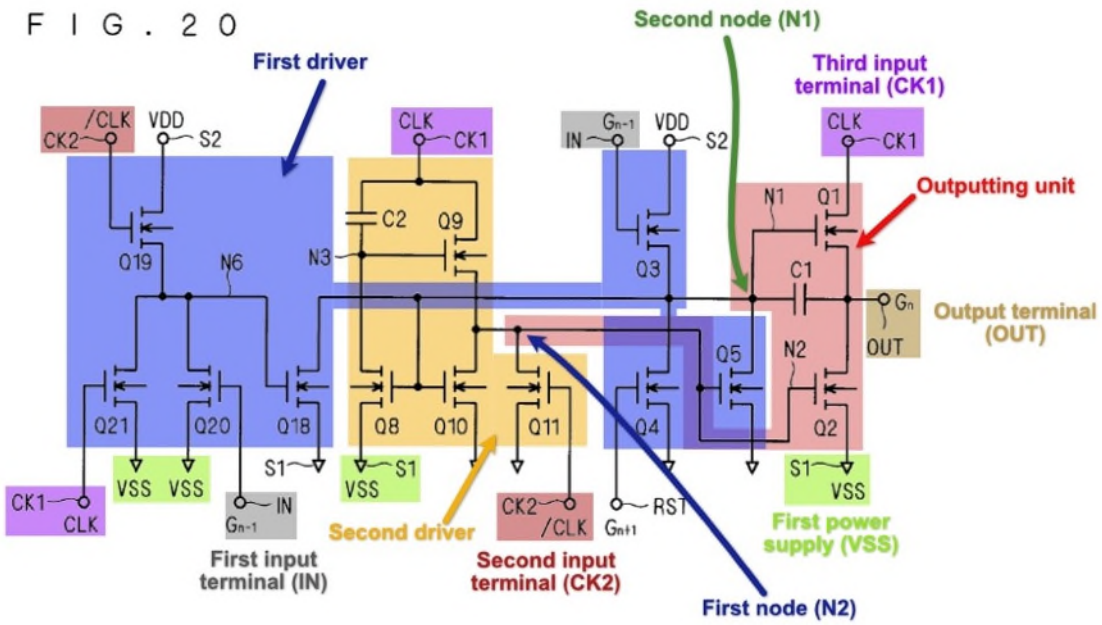
Id., Fig. 8; *see also* ¶¶ [0027], [0117].

122. Each unit shift register SRn in this multistage shift register can include the embodiment shown in Figure 7:



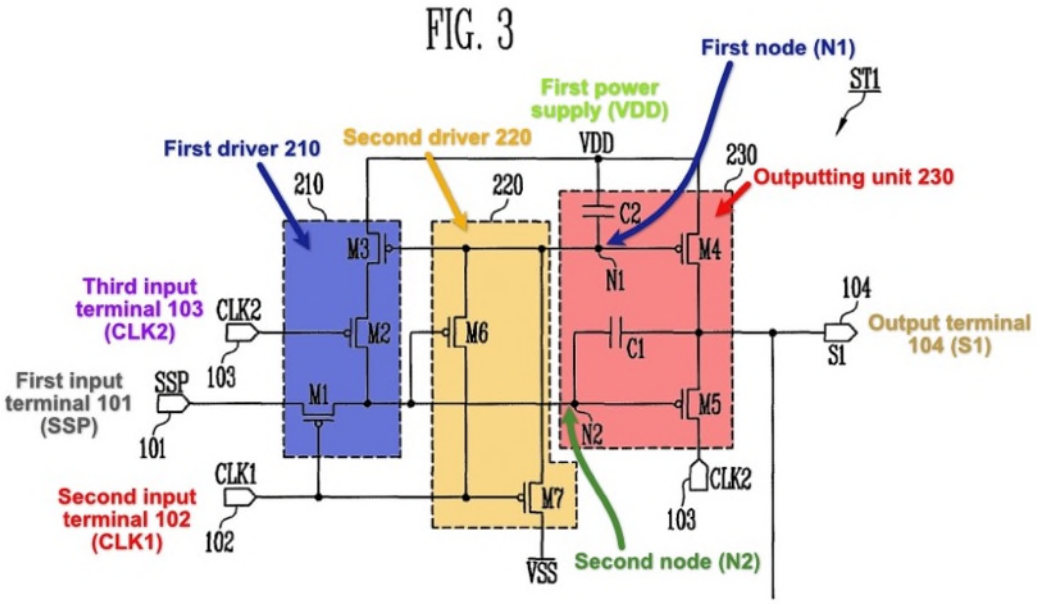
Id., Figs. 7-8, ¶¶ [0026]-[0027], [0117], [0167].

123. Embodiments of Figures 19 and 20 are variants of Figure 7. *Id.*, ¶¶ [0168], [0172], [0177]. In these figures, elements having similar or analogous functions are shown by the same reference designators. *Id.* Further, these embodiments have the same functionality. *Id.*, ¶ [0109]. The embodiment of Figure 20 is shown below:



Id., Fig. 20 (annotations added).

124. As shown above, Tobita demonstrates a circuit with robust and various circuit structure to exercise control over the voltages of the first and second nodes, and by extension exercises control over the outputting unit. In particular, comparing the Tobita embodiment above with the preferred embodiment of the ’593 patent below reveals that all of the same input/output signals and the same or similar claimed features are present in both.

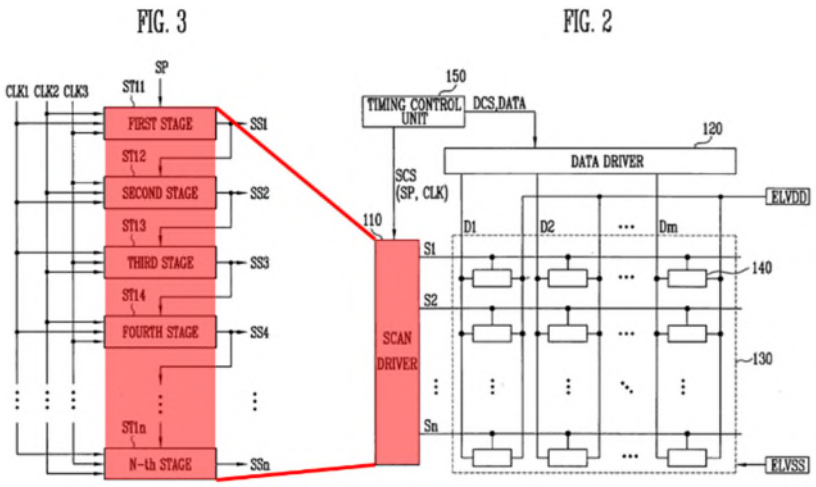


Ex. 1001, Fig. 3 (annotations added).

E. Jeong

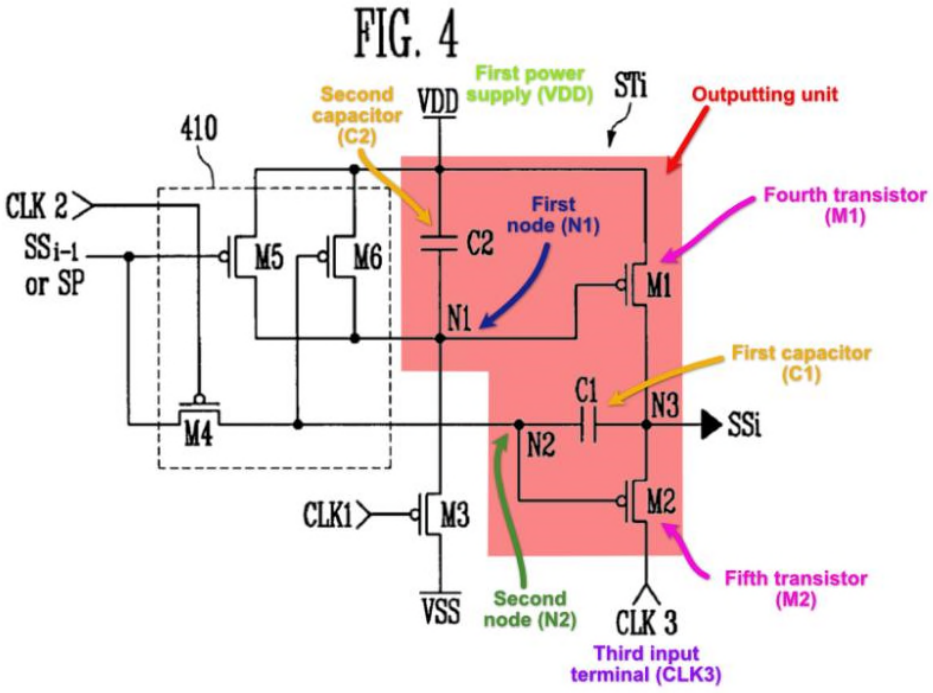
125. U.S. Patent Publication No. 2008/0062097 A1 to Jeong ("Jeong") was published on March 13, 2008, and is prior art to the '593 patent under at least 35 U.S.C. § 102(b).

126. Jeong discloses shift registers for a scan driver for driving the pixels of an OLED display. Ex. 1007, ¶ [0002].



Id., Figs. 2-3 (annotated).

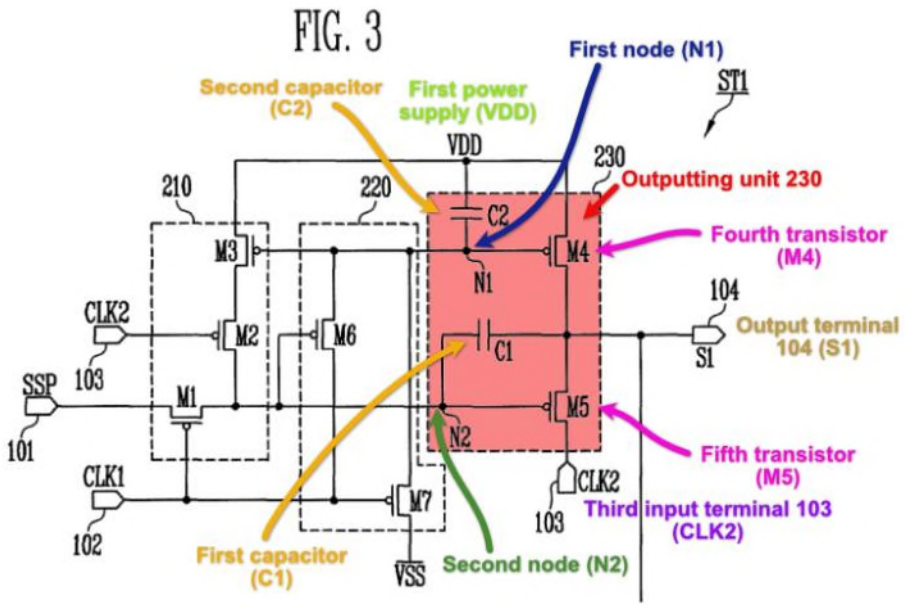
127. Successive stages generate successive output signals SS1 through SSn, which are output to the respective scan lines. *Id.*, ¶ [0041]. Each stage of the scan driver comprises a shift register:



Id., Fig. 4 (annotated).

128. Capacitor C2 is coupled between the first power supply VDD and the node N1, and functions to reduce voltage variation the voltage at node N1. *Id.*, ¶ [0057]. What Jeong is describing is well-known in the art – that by maintaining the voltage at a node using a capacitor (rather than simply via the wiring), more charge is used for that maintenance; by thusly using more charge, the voltage on the node will be less susceptible to fluctuations in that voltage due to fluctuations in, e.g., the VDD voltage – as the changes in charge due to those fluctuations will be reduced in proportionality.

129. Comparing the Jeong embodiment above with the preferred embodiment of the '593 patent below reveals that all of the same input/output signals, nodes, and components of the outputting unit are present in both.



Ex. 1001, Fig. 3 (annotations added).

X. MOTIVATION TO COMBINE CERTAIN PRIOR ART REFERENCES

130. As will be explained below (in Section XII), all of the challenged claims of the ‘593 patent may be found in the referenced prior art – either explicitly, or in forms that require only modest (and obvious) modification. In one particular instance, a POSITA would be motivated to combine two prior art references – and would be able to do so without undue experimentation and a high expectation of success; these combinations will be considered in the discussions of Ground 3, (in Section XII.C) and Ground 5 (in Section XII.E).

XI. CLAIM TERMS

131. As explained in Section VIII.C, consistent with SDC’s proposed constructions and infringement theories from the related ITC Investigation, I have given the terms in the challenged claims their plain and ordinary meanings, as would have been understood by a person of ordinary skill in the art at the time of the alleged invention, taking into consideration the language of the claims, the specification, and the prosecution history of the ’593 patent. I have applied these understandings of the claim terms in my analysis and in forming my opinions where appropriate in this Declaration. As noted in Section VIII.C, there are certain terms where I have provided some additional explanation of what a POSITA would have considered the plain-and-ordinary meaning to be.

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XII. UNPATENTABILITY ANALYSIS

132. As briefly mentioned above, from the analysis which follows, it is my conclusion and opinion that the challenged claims of the ‘593 patent are unpatentable – based on disclosures in the prior art. This analysis will encompass four separate grounds of unpatentability.

A. Ground 1: Kimura Renders Obvious Claims 1-8, 14-22, and 25

133. As will be discussed below, it is my conclusion and opinion that, when viewed and considered in light of the knowledge possessed by a POSITA, Claims 1-8, 14-22, and 25 of the ’593 patent are rendered obvious by Kimura.

1. Independent Claim 1

134. It is my conclusion and opinion that Claim 1 of the ’593 patent is rendered obvious by Kimura.

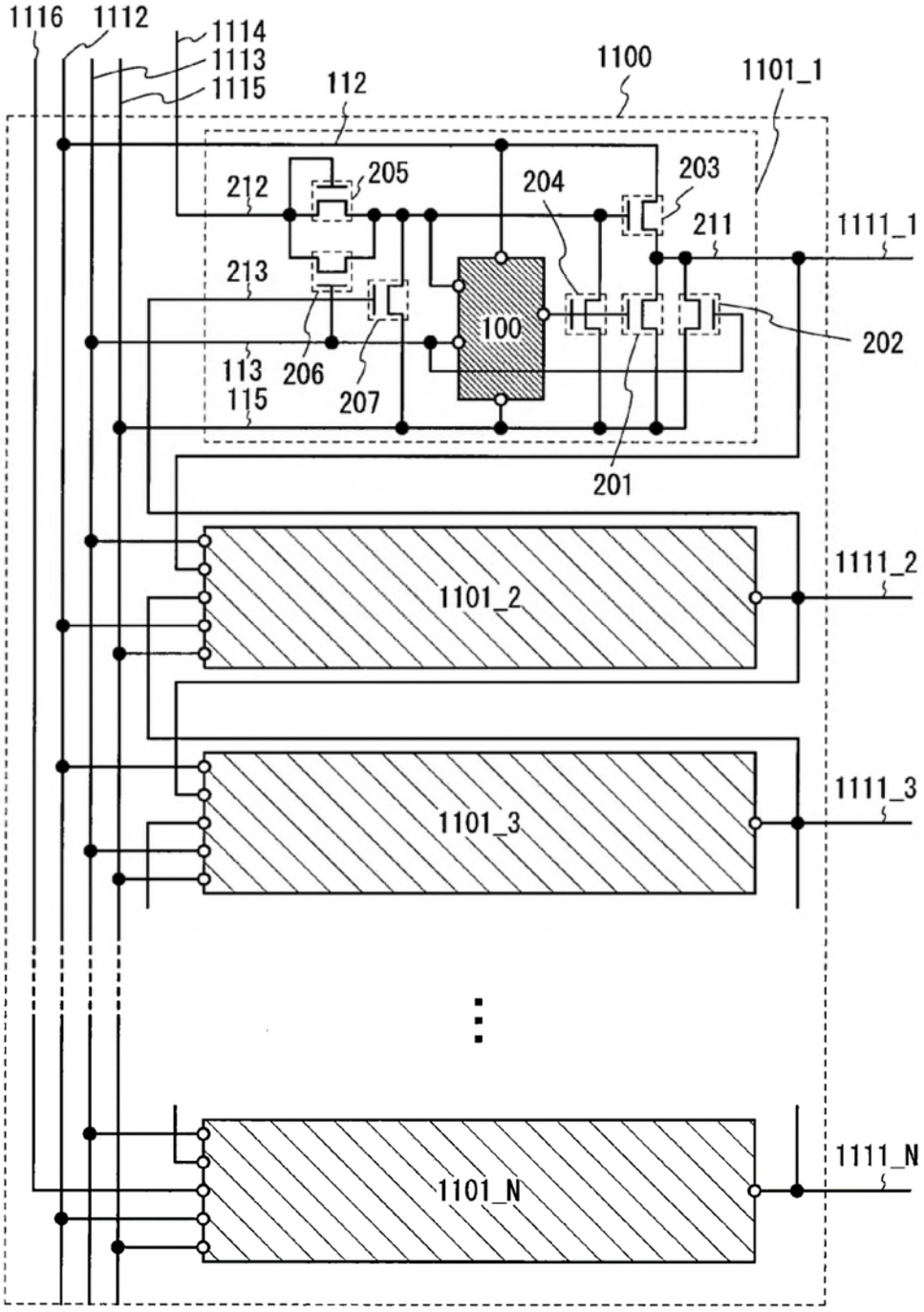
a. [1-pre]: “A stage circuit having a first input terminal, a second input terminal, a third input terminal, and an output terminal, the stage circuit comprising:”

135. As an initial matter, I will be offering no opinion regarding whether or not the preamble of Claim 1 is limiting. I have been instructed by counsel for Petitioner to offer an opinion as to whether or not the prior art discloses the preamble, regardless of whether or not the preamble is limiting.

136. Kimura discloses the preamble of Claim 1 of the ’593 patent; this can be seen readily via Figure 34 of Kimura:

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FIG. 34



Id., Fig. 34. Kimura explains that any of the "semiconductor device[s] in Embodiment 1 or 2" can be used to form the shift register's circuits 1101_1 to 1101_N. *Id.*, ¶¶ [0320], [0339].

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137. In more detail, Kimura provides reasonably-comprehensive identification of the various items that comprise the circuitry depicted in Figure 34 (at ¶¶ [0333] – [0339]). 1100 is identified as being a shift-register circuit, while the repeated circuitry 1101_1, 1101_2, 1101_3, … 1101_N) items are identified as being repetitions of a flip-flop circuit; the signal lines on the right-hand side – 1111_1, 1111_2, 1111_3, … 1111_N are identified as being the output lines – with the numbering arranged to signify the output line corresponding to the identically-numbered flip-flop circuit. In addition, each flip-flop circuit has five input terminals – which involve the signal lines labeled as 1112, 1113, 1114, 1115, and 1116.

138. The most-notable architectural feature of this circuitry is that, beginning with second flip-flop circuit, an input terminal of each flip-flop receives as an input signal the output of the preceding flip-flop circuit. Arranged in this way, this shift register is comprised of a cascade of stage circuits – which, here, are flip-flop circuits. Thus, this shift register circuitry of Figure 34 of Kimura contains stage circuits, as required by the claim preamble.

139. Kimura further identifies lines 1112, 1113, 1114, 1115, and 1116 as input terminal lines that provide input signals. Notably, lines 1112, 1113, and 1115 are connected to input terminals of each-and-every stage circuit – while input line 1116 is provided to the final stage and input line 1114 is provided only to the first stage. With regard to input signal line 1114, as Kimura explains, 1114 provides a

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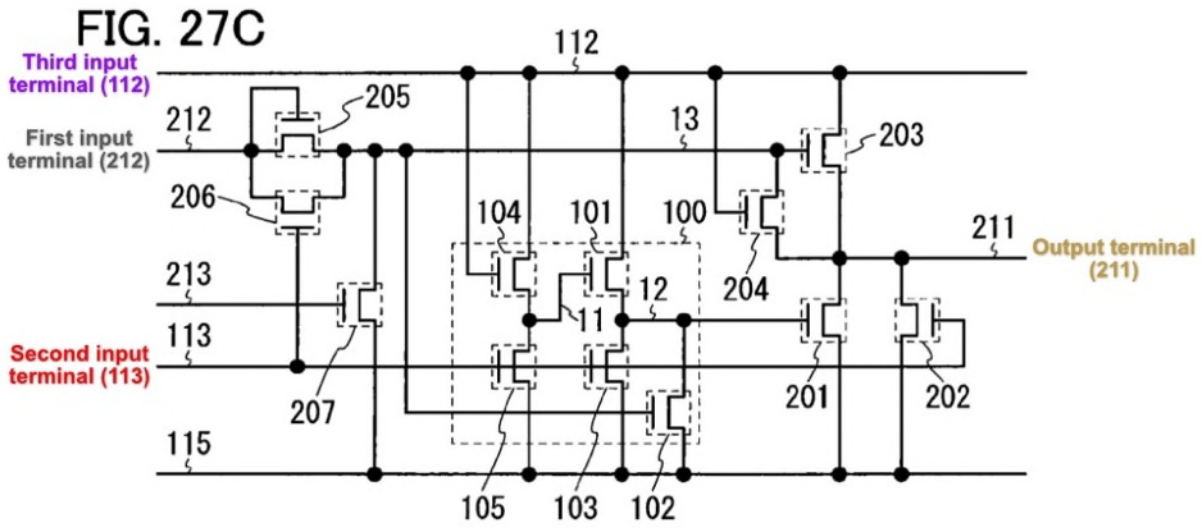
start signal for the first stage – and that the same input line in subsequent stages is provided by the output of the prior stage circuit in the cascade of stage circuits (as outlined briefly above).[10]

140. Of additional note (and as mentioned briefly above), in this figure, Kimura provides a circuit-level depiction of the first stage circuit, but thereafter provides only "black box" renditions of the succeeding (identical) stage circuits. As Kimura notes, while one particular embodiment is depicted for the stage circuit here (via the use of a detailed circuit depiction, as just described), the stage circuit(s) could consist of any of the suitable embodiments of stage circuits described elsewhere in the specification.

141. From that description provided by Kimura, it should be further-noted here that the embodiment of Figure 27C shows one of the "semiconductor device[s] in Embodiment 2[.]" *Id.*, ¶ [0072]:

[10] Input signal line 1116 is provided to the last stage in the cascade because this particular circuit architecture also includes the use of the output signal from a particular stage to the input of the *prior* stage; while this feature of the Figure 34 circuitry of Kimura will make a brief explanatory appearance below, nothing of this sort of appears in the architecture of the circuitry of the '593 patent – and thus this feature of Kimura's circuitry is of no relevance here.

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Id., Fig. 27C (annotations added). This detailed (circuit-level) embodiment shows a stage circuit having a first input terminal, a second input terminal, a third input terminal, and an output terminal,

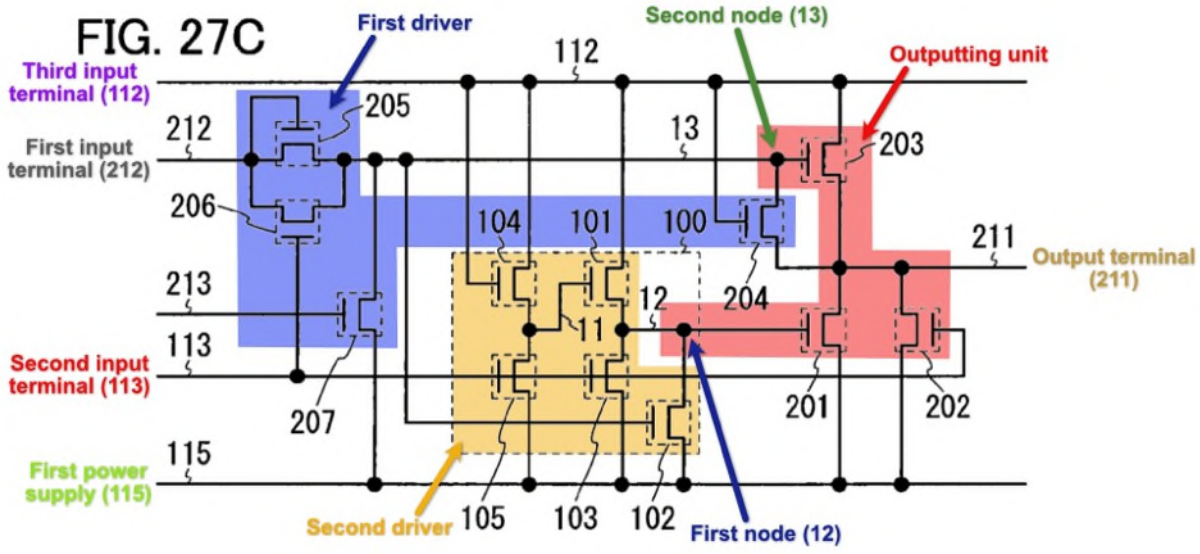
142. More particularly, this figure depicts circuitry that is meant for use as a "stage" of a display's "shift register circuit." *Id.*, ¶¶ [0320], [0324], [0333]. The "signal IN4"—which Kimura explains "can function as a start pulse" for the shift register—"is input to the wiring 212" (the first input terminal). *Id.*, ¶ 0266. "A signal IN1 is input" to the shift register's "wiring 112" (Kimura's third input terminal). *Id.*, ¶ [0104]. "A signal IN2 is input to the wiring 113" (the second input terminal). Id.

143. According to Kimura, "a clock signal is used as the signal IN1" and "a signal which is approximately 180° out of phase from the signal IN1 is used as the signal IN2…." *Id.*, ¶ [0109]; *see also id.*, ¶¶ [0230]-[0232]. The "wiring 211" (the

output terminal) receives the register's "signal GOUT[.]" *Id.*, ¶ 0226; *see also id.*, ¶ [0103] (referencing a "signal OUT" that is "output from the wiring").

144. Thus, Kimura discloses the preamble of Claim 1 of the '593 patent.

145. Having explained the basic teachings of Kimura, this is a convenient place to foreshadow the details of the remaining analysis of Kimura and the claims of the '593 patent. This can best be done by providing another annotated version of Figure 27C – with additional annotations:



Id., Fig. 27C (annotations added). As shown – and as will be discussed in greater detail in the following sections – the shift register stage embodiment of Figure 27C includes all of the components required by independent claims 1 and 15 of the '593 patent; as will also be discussed in greater detail in the following sections, this embodiment also includes the components required by many dependent claims.

146. The portion of Kimura's specification relating to Figure 27C is brief – and does not mention all of the transistors, inputs, and outputs shown in the figure above; however, Kimura explains that the circuitry of Figure 27C builds on and shares components with the devices shown in other figures – including those of Figs. 10A-C, 14A, 16A, 17A, 20A, 21A, 23A, 25A, and 47A-B. Ex. 1004, ¶¶ [0282]-[0286].

147. Dependent claims 6, 7, 8, 20, 21, and 22 include additional elements that are not already part of Figure 27C; however, as I will explain below, Kimura also teaches that the circuitry of Figure 27C can be supplemented with (and improved by) the addition of further transistors, capacitors, and other elements. As will be discussed below, these claims are also rendered obvious.

b. [1-a]: "an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node:"

148. Claim element [1-a] is rather long – and thus the analysis will be simpler to explain if this claim element is broken up into sub-elements.

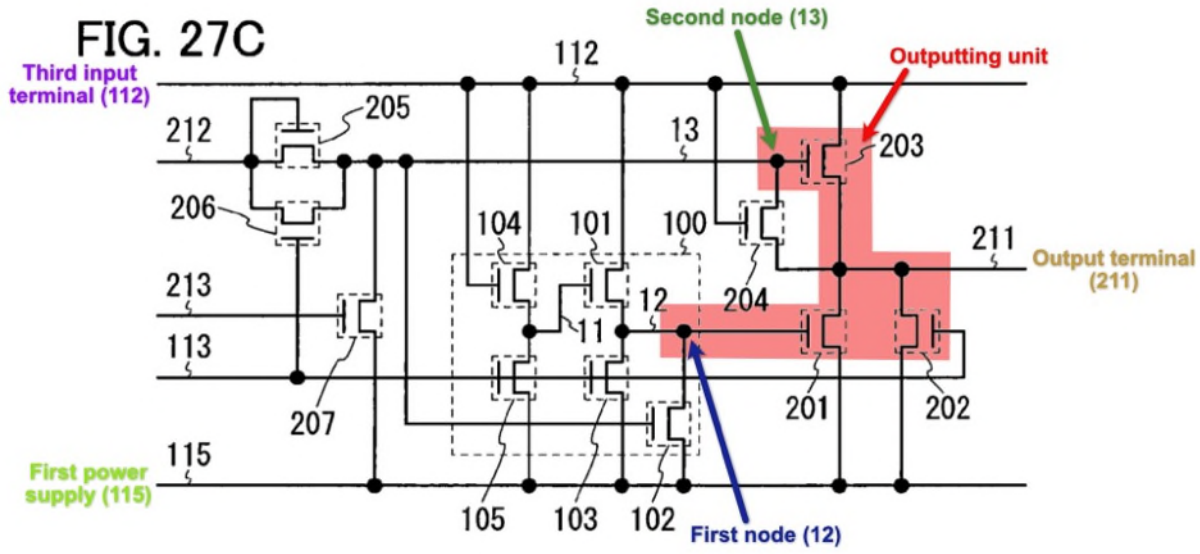
149. As a preliminary matter, it should be noted that – as described above – Kimura discloses a general shift register architecture, comprised of a cascade of stage circuits; Kimura further discloses a number of different embodiments for the

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stage circuit that may be used in the more-general architecture. Thus, any of these embodiments may be used for the analysis of the possible unpatentability of the claims of the '593 patent. As was discussed above, for the analysis of Claim 1 that is to follow here, the embodiment of Figure 27C of Kimura will be used as an example.

i. [1-a-1]: "an outputting unit having a first node and a second node,"

150. Kimura discloses this claim sub-element; this is evident via an annotated version of Figure 27C of Kimura:

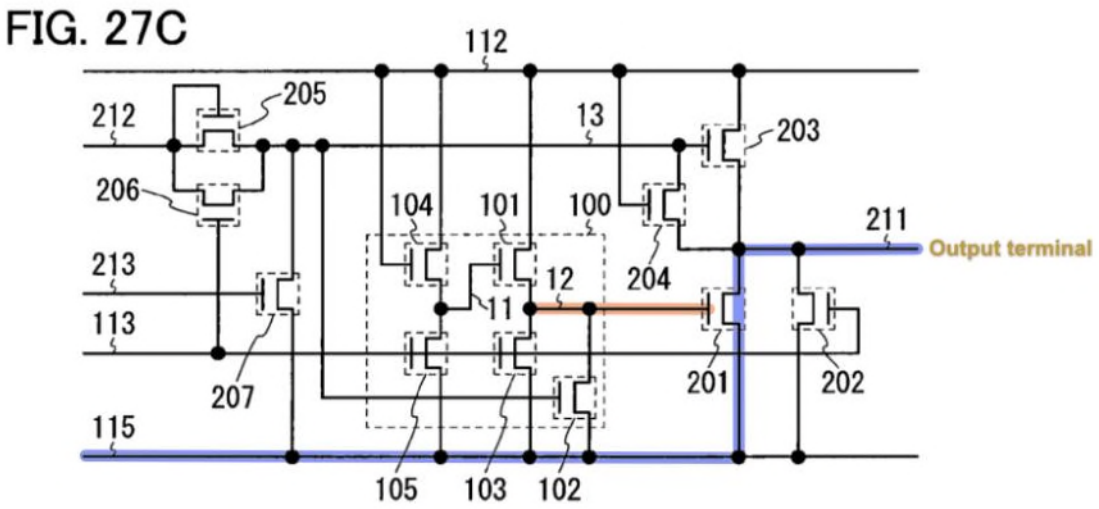


Id., Fig. 27C (annotations added). The node labeled "12" is the first node, and the node labeled "13" is the second node – while the "outputting unit" is a shown via the annotation box-bounding in red.

151. Thus, Kimura discloses this claim sub-element of this claim element of Claim 1 of the ’593 patent.

ii. [1-a-2]: “the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node”

152. Kimura discloses this claim sub-element; this is evident via an annotated version of Figure 27C of Kimura:



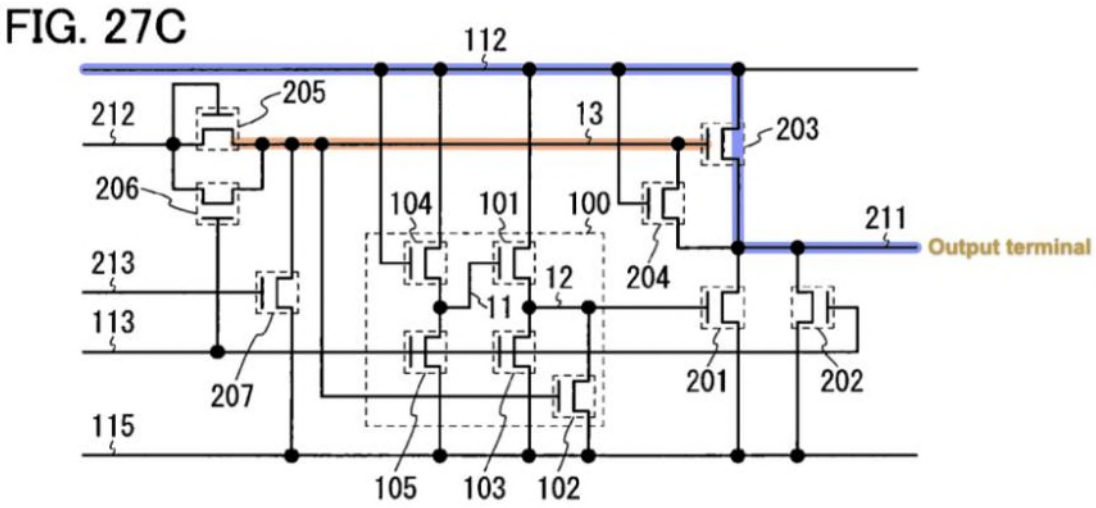
Id., Fig. 27C (annotations added). As the annotations show, with the first power supply applied to input terminal 115, when an appropriate (i.e., turn-on) voltage is applied at the first node (the node labeled 12), transistor 201 will turn on; this will connect the first power supply voltage (at input terminal 115) to the node of the output terminal (211) – and thus the voltage of the first power supply is supplied to the output terminal. (On the other hand, when a turn-on voltage is not applied at the

first node 12), transistor 201 will not turn on – and the voltage of the first power supply connection is not supplied to the output terminal through transistor 201.)

153. Thus, Kimura discloses this claim sub-element of this claim element of Claim 1 of the ’593 patent.

iii. [1-a-3]: “and a signal of the third input terminal to the output terminal according to a voltage applied to the second node:”

154. Kimura discloses this claim sub-element; this is evident via an annotated version of Figure 27C of Kimura:



Id., Fig. 27C (annotations added). As the annotations show, when an appropriate (i.e., turn-on) voltage is applied at the second node (the node labeled 13), transistor 203 will turn on; this will connect the signal of the third input terminal (112) to the node of the output terminal (211) – and thus the signal of the third input terminal (112) is supplied to the output terminal (211). (On the other hand, when a turn-on

voltage is not applied at the second node (13), transistor 203 will not turn on – and thus the signal of the third input terminal (112) in not supplied to the output terminal (211).)

155. Thus, Kimura discloses this claim sub-element of this claim element of Claim 1 of the ’593 patent.

iv. Claim Element [1-a] Summary

156. As just demonstrated, Kimura discloses claim sub-elements [1-a-1], [1-a-2], and [1-a-3] of the ’593 patent; thus, Kimura renders obvious claim element [1-a] of Claim 1 of the ’593 patent.

157. However, while it was convenient to break claim element [1-a] up into sub-elements (so as to clearly-and-separately show the presence of each of these sub-elements in Kimura), the circuitry of claim element [1-a] is also characterized by a functionality that encompasses the entire claim element; this will be explained next – as per Kimura’s description of that functionality.

158. Kimura describes how the outputting unit functions in a manner that matches the teachings of this claim element. As discussed above, transistors 201-203 are responsible for generating output. Again, a “signal IN1 is input to the wiring 112” (Kimura’s third input terminal). Ex. 1004, ¶ [0104]. A “transistor 203 has a function of controlling conduction between the wiring 112 and the wiring 211” (the output terminal). *Id.*, ¶ [0250]. The “transistor 203” is “controlled by the potential

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of the node 13" (the second node). *Id.* "A voltage V1 is supplied to the wiring 115" (Kimura's first power supply). *Id.*, ¶ [0105]. "The voltage V1 is" a "power supply voltage." *Id.*

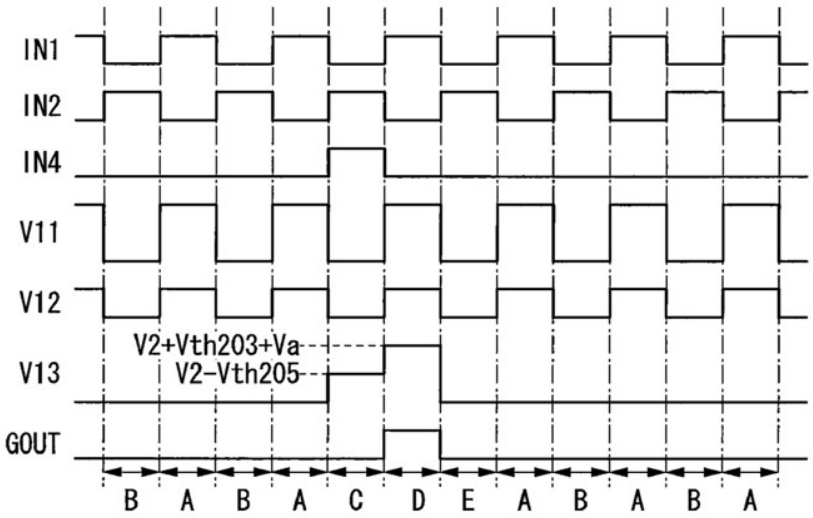
159. Furthermore, a "transistor 201 has a function of controlling conduction between the wiring 115 and the wiring 211" (the output terminal). *Id.*, ¶ [0222]. The "transistor 201 can be controlled by the output signal of the circuit 100." Id. As shown in Figure 27C, the gate of transistor 201 is connected to node 12 (Kimura's first node) exiting from circuit 100. *Id.*, Fig. 27C. In other words, circuit 100 outputs a signal to "node 12" for purposes of controlling transistor 201. *See id.*, ¶ [0226]. Like transistor 201, transistor 202 also operates so as to connect wiring 115 to wiring 211. As part of this, it receives a signal provided via wiring 113 at its gate. *Id.*, ¶¶ [0245]-[0246].

160. These transistors—along with the other transistors making up the circuit of Figure 27C—operate to supply logic-low and logic-high signals to the output line. Figure 21B provides an example of a "timing chart for illustrating operation of the semiconductor device" in the manner discussed above. *Id.*, ¶¶ [0062], [0066]. While Kimura does not provide a timing chart that is specific to the circuitry of Figure 27C, it is readily comprehensible (and would so be understood by a POSITA) that this circuitry (of Figure 27C) would be supplied with input signals in the same manner and with the same timing – since, as mentioned earlier,

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Kimura teaches that the many different stage circuit embodiments disclosed by Kimura can be used in the general architecture of the disclosed shift register circuit embodiments. As shown below, the time encompassed by the timing diagram is divided into five periods – which are, for explanatory purposes, labeled as A-E:

FIG. 21B



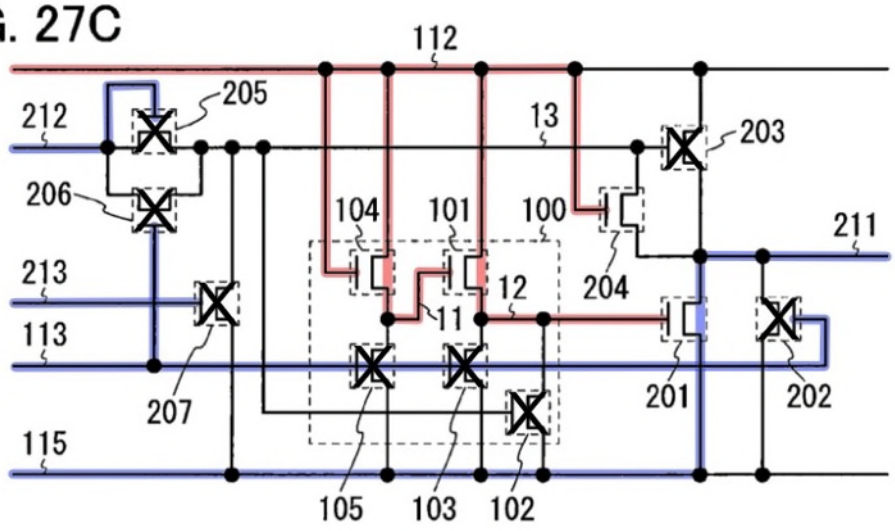
Ex. 1004, Fig. 21B. The only input missing from this diagram is that provided via wire 213 in Figure 27C. According to Kimura, this wire can receive "a signal IN5" that "function[s] as a reset signal." *Id.*, ¶ [0278]; as shown in Figure 25B, the reset signal IN5 is low in all periods except for period E. *See id.*, Fig. 25B.

161. During the "period A" shown above, input signals are supplied to the shift register to cause "the potential of the node 12" to be "set at a H level." *Id.*, ¶ [0253]. According to Kimura, because node 12 is high, "transistor 201" is "turned on, so that the wiring 115 and the wiring 211 are brought into conduction. Then, the potential of the wiring 115 (e.g., the voltage V1) is supplied to the wiring 211." *Id.*

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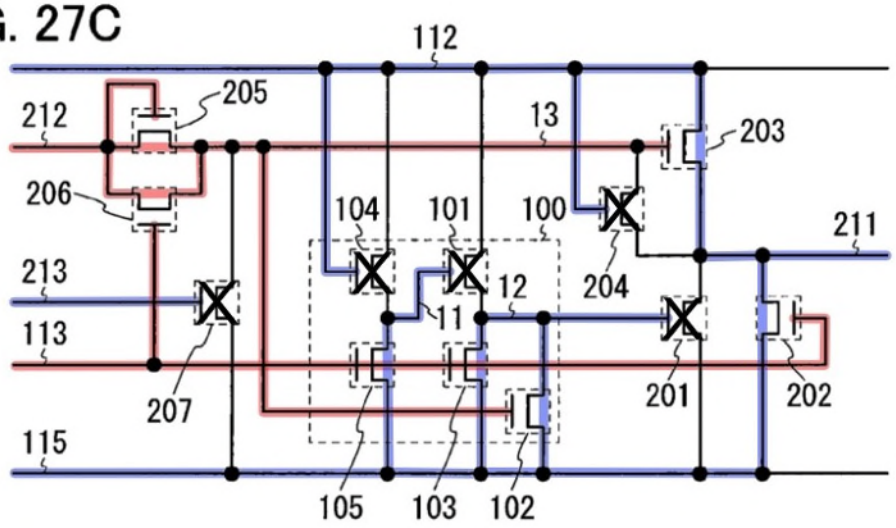
This results in "the signal GOUT" being "set at an L level." *Id.* Transistor 203 is off due to the supply of a low IN4 signal through transistor 206 (which was turned on by a high IN2 signal) in the previous period. *See id.*, Fig. 21B. This operation is summarized below via an annotated version of Figure 27C – with the logic-low signals shown in blue and the logic-high signals shown in red:

FIG. 27C



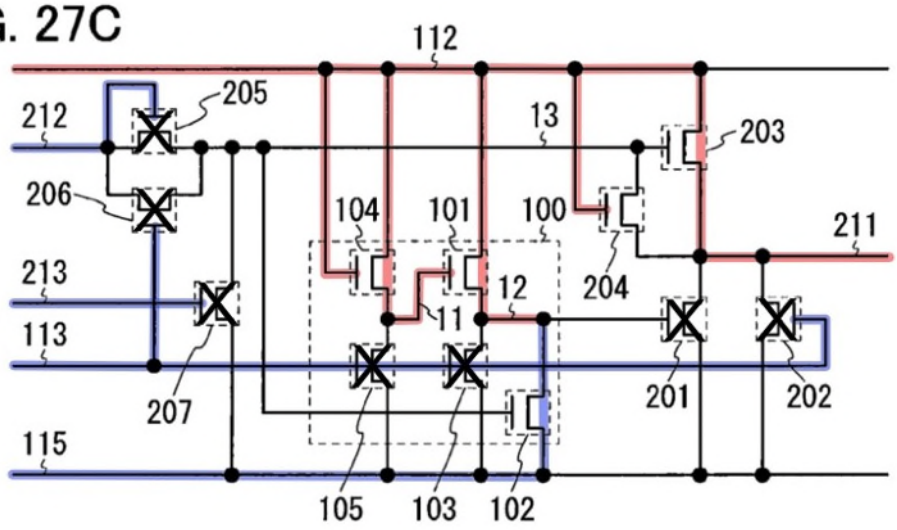
162. During the (later) "period C" shown in the annotated timing diagram above, different input signals cause "the potential of the node 12" to be "set at an L level" so that "transistor 201 is turned off" – which amount in effect to disconnecting "the wiring 115 and the wiring 211." *Id.*, ¶ [0255]. At the same time, "the potential of the node 13 becomes an H level so that transistor 203 is turned on. Then, the wiring 112 and the wiring 211 are brought into conduction, so that the potential of the wiring 112 (the signal IN1 at an L level) is supplied to the wiring 211." *Id.* This operating phase is depicted below:

FIG. 27C



163. Later, in a "period D," the "node 13" enters a "floating state" allowing the "potential of the wiring 112"—which has changed to "the signal IN1 at an H level"—to be "supplied to the wiring 211." *Id.*, ¶ [0256]. "Transistor 201" remains off during this period, resulting in "the signal GOUT" being "set at an H level." *Id.* This is depicted below:

FIG. 27C



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164. Thus, in sum, transistors 201-203 are ultimately responsible for the relay of either (among other things) the voltage V_1 or the signal IN1 to the output line – at the appropriate times.

165. This further shows the Kimura renders obvious claim element [1-a] of Claim 1 of the ’593 patent.

c. [1-b]: “a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal; and”

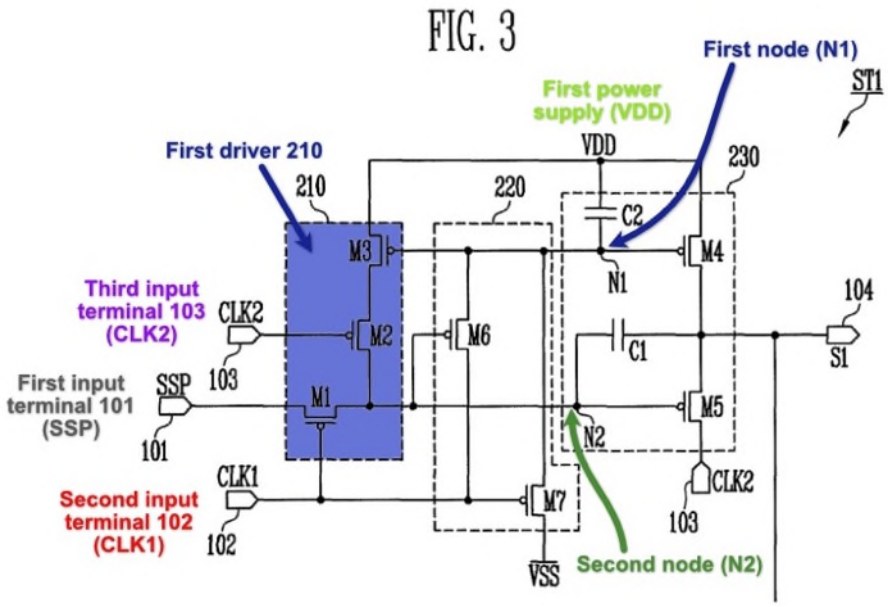
166. As an initial matter, analysis of this claim element indicates that one should not understand this claim element to require control “in accordance with” only the recited signal; further, it is my conclusion and opinion that a POSITA reviewing the ‘593 patent would reach a similar conclusion – for the reasons to be explained here.

167. Overall, Claim 1 is a “comprising” claim. It is my understanding that, in the context of the claim element itself, this type of claim is open to the presence of other input signals besides those specifically recited.

168. Moreover, Figure 3 of the ’593 patent shows a preferred embodiment of a “first driver 210” that controls the voltage of the second node N2….” Ex. 1001, 5:29-36, 63-65 – and that, further, as shown below, this first driver receives input not only from terminals 101-103, but also from at least node N1 (connected to the

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gate of transistor M3) and power supply VDD (connected to one side of the same transistor):



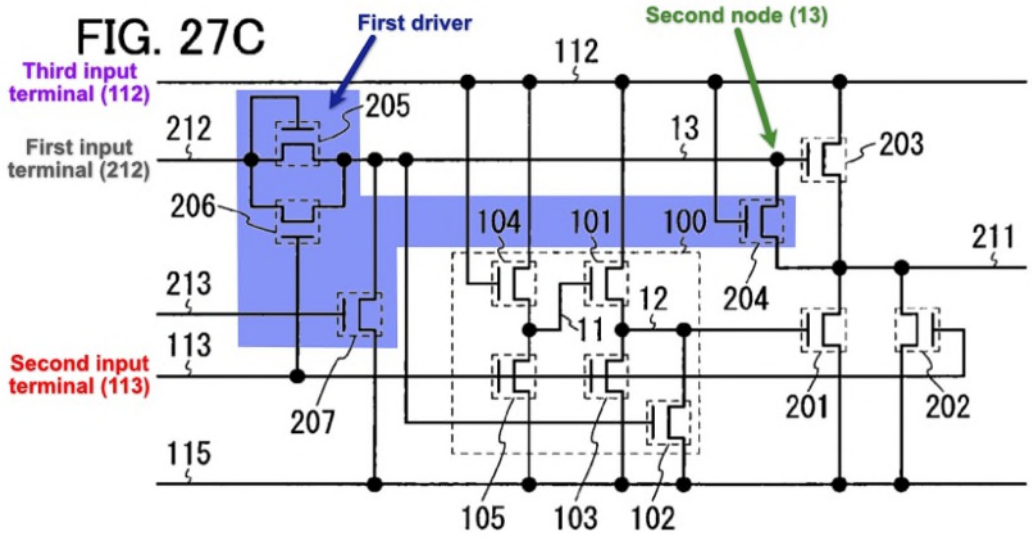
Ex. 1001, Fig. 3 (annotations added).

169. Similarly, the ’593 patent explains that its “first driver 210” includes a “third transistor M3” that is “coupled to the first node N1” and “controls coupling” with “first power supply VDD.” *Id.*, 5:65-67, 6:16-21. If the claim (and this claim element) were to be construed so as to require control in accordance with only the signals listed in the claim, this embodiment would be read out of the claim scope. I understand that this is rarely appropriate.

170. Returning to Kimura, Figure 27C (of Kimura) includes the claimed “a first driver to control the voltage of the second node [13] in accordance with signals

of the first input terminal [wiring 212], the second input terminal [wiring 113], and the third input terminal [wiring 112]."

171. Kimura's first driver is depicted as follows:

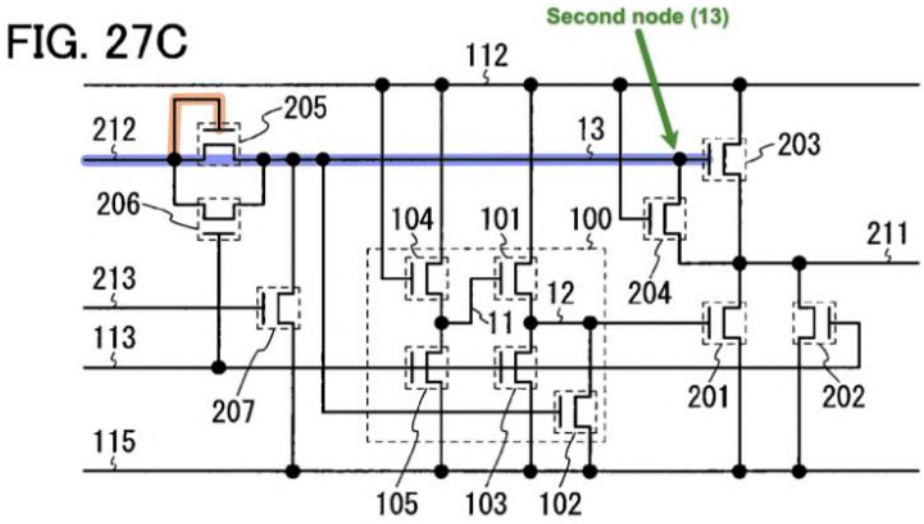


Ex. 1004, Fig. 27C (annotated). The first driver is annotated with blue boxing – and as the annotations show, it contains all of the items identified in this claim element.

172. Further, this first driver consists of components that are connected together – and this first driver functions in a manner consistent with the listed requirements of this claim element.

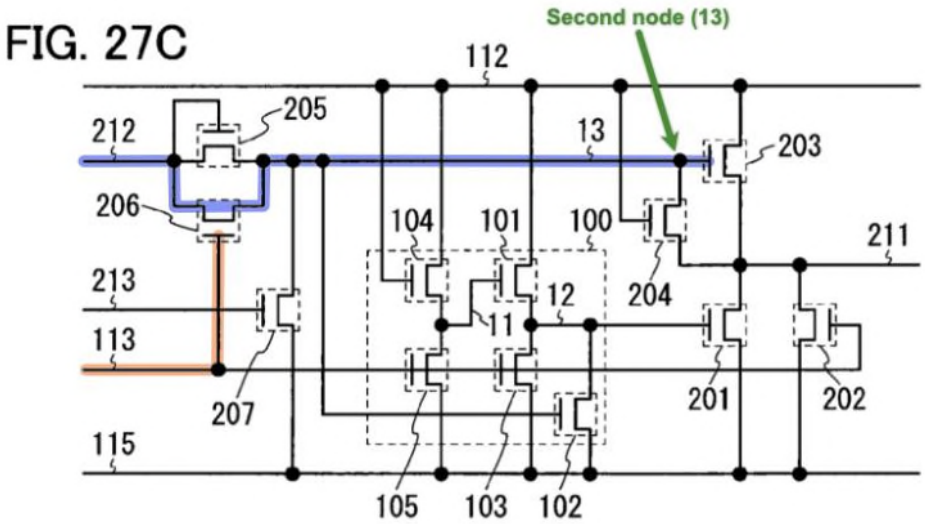
173. In particular, a "transistor 205" is connected in what is known as the "diode-connected configuration" (*see* Section VII.A.3) to "wiring 212" (which is Kimura's first input terminal, and receives signal IN4). Ex. 1004, ¶¶ [0264]-[0265]. This transistor "has the function of controlling conduction between the wiring 212 and the node 13" (Kimura's second node). *Id.*, ¶ [0268].

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Id., Fig. 27C (annotations added). Among other things, this arrangement can supply a "H-level signal" (i.e., a high logic-level signal) from wiring 212 to the node. Id.

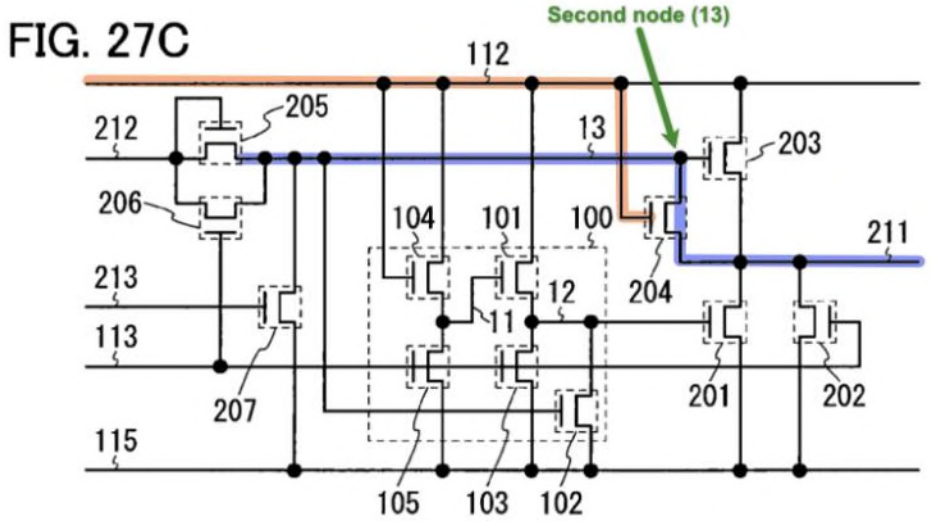
174. Next, a "transistor 206" includes one "terminal connected to the wiring 212" (the first input terminal), another "terminal … connected to the node 13[,]" and a "gate … connected to the wiring 113" (which is Kimura's second input terminal, and receives signal IN2). *Id.*, ¶¶ [0270]-[0271].



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Id., Fig. 27C (annotations added). Using the signal from wiring 113, this transistor also facilitates "conduction between the wiring 212 and the node 13" and allows for the supply of a "L-level signal" (i.e., a low logic-level signal) or "H-level signal" (i.e., a high logic-level signal) to the node 13. *Id.*, ¶ [0272].

175. The structure also includes yet another transistor: "transistor 204." *Id.*, ¶ [0286]. "[T]he first terminal of the transistor 204 is connected to the wiring 211 and the gate of the transistor 204 is connected to wiring 112" (which is Kimura's third input terminal). *Id.* The transistor's other terminal is connected to node 13. *Id.*, ¶¶ [0285]-[0286]; Fig. 27C.



Id., Fig. 27C (annotations added). This transistor (204) allows "the potential of the node 13" to be "lowered" to prevent "dielectric breakdown or deterioration" of transistors connected to the node. Id. (The background of the issues of possible

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"dielectric breakdown or deterioration" of transistors was briefly discussed in the overview of Kimura provides in Section IX.A.)

176. Finally, a transistor 207 receives input from wiring 213, and operates to connect "wiring 115" to the "node 13." *Id.*, ¶¶ [0276]-[0280].

177. Thus, transistors 204-207 collectively receive input from, among other things, wires 112, 113, and 212—which are the various claimed input terminals—for purposes of controlling the voltage at node 13—which is the claimed second node.

178. The impact that these received input signals have on the voltage of node 13 is also reflected in Kimura's example timing charts. *See, e.g.*, Ex. 1004, Figs. 17B, 21B, 25B.

179. Thus, Kimura discloses this claim element of Claim 1 of the '593 patent.

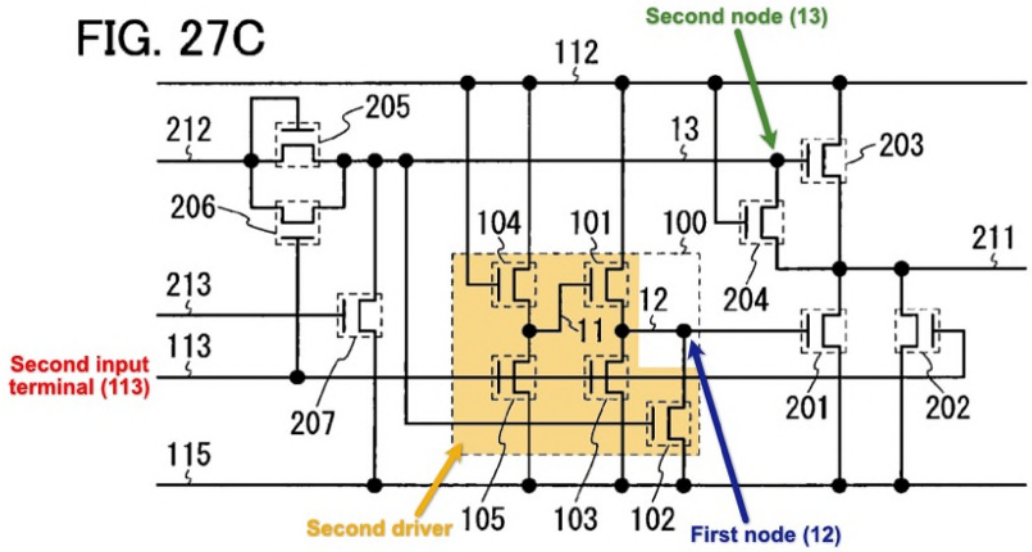
d. [1-c]: "a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node, wherein"

180. As was the case with claim element [1-b] – and as described above in the discussion of claim element [1-b], this claim element also does not require control "in accordance with" *only* the recited signal – for the same reasons as those discussed above with respect to claim element [1-b]. Moreover, both claim elements [1-b] and [1-c] use the same term – a "driver to control the voltage of [a] node in

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accordance with [recited] signal(s)." It is my understanding that similar claim terms are presumptively given the same meaning.

181. Returning to Kimura, as shown below, in Figure 27C Kimura includes "a second driver to control the voltage of the first node [12] in accordance with the signal [IN2] of the second input terminal [113] and the voltage of the second node [13]."



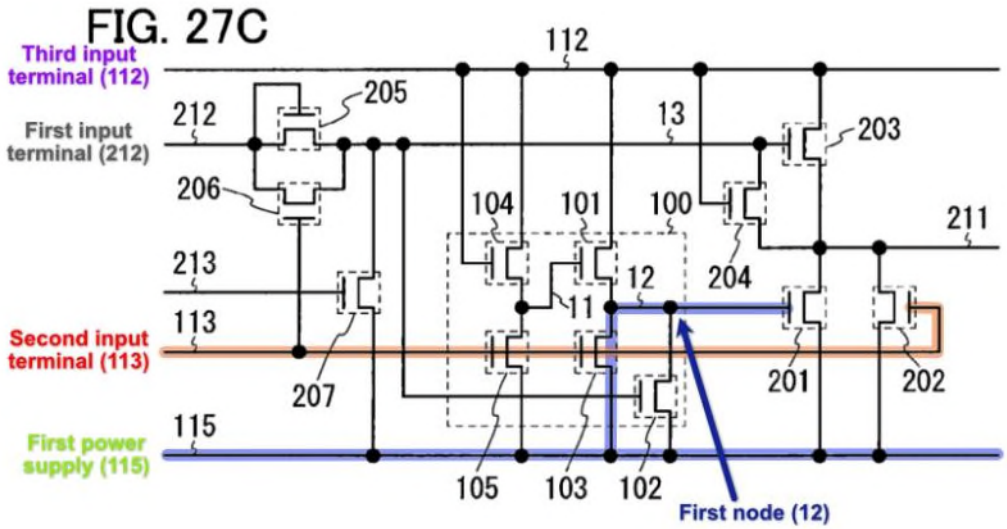
Ex. 1004, Fig. 27C (annotations added). The second driver is annotated with gold boxing – and as the annotations show, it contains all of the items identified in this claim element.

182. Further, this second driver consists of components that are connected together – and this second driver functions in a manner consistent with the listed requirements of this claim element.

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183. As shown, circuit 100 controls voltage of node 12 (Kimura's first node) and connected transistor 201. Ex. 1004, ¶¶ [0222], [0226].

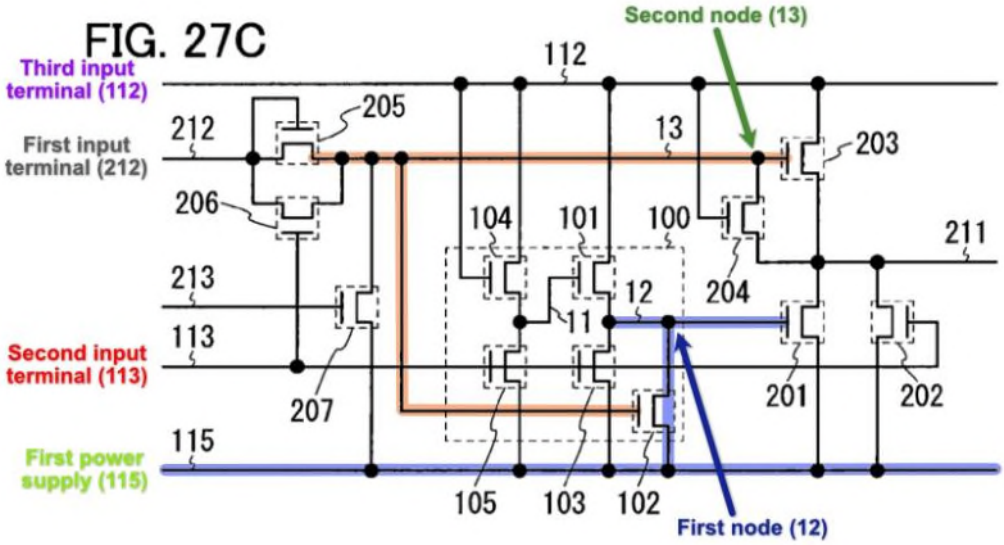
184. Further, this second driver circuit includes a series of transistors 101-105 – and "is controlled in response to," among other things, signals IN2 and IN3. *Id.*, ¶¶ [0114]-[0115].



Id., Fig. 27C (annotations added). Transistors 103 and 105 of the circuit 100 both have gates connected to wire 113 (Kimura's second input terminal), and are thus "controlled by the potential" (where, again, "potential" is another word for "voltage") of this wire and the signal IN2 it carries. *Id.*, ¶¶ [0119], [0121]. Of particular note, a signal applied to the second input terminal (113) is connected to the gate of transistor 103 – and transistor 103 is connected directly to the first node; thus, the voltage of the first node is controlled in accordance with the signal of the second input terminal.

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185. Further, "the gate of transistor 102 can be connected to the node 13" (Kimura's second node) such that this node supplies transistor 102 with controlling "signal IN3." *Id.*, ¶ [0249].



Id., Fig. 27C (annotations added). As can be seen via the annotations, second node (13) is connected to the gate of transistor 102 – and transistor 102 is connected directly to the first node; thus, the voltage of the first node is controlled in accordance with the voltage of the second node.

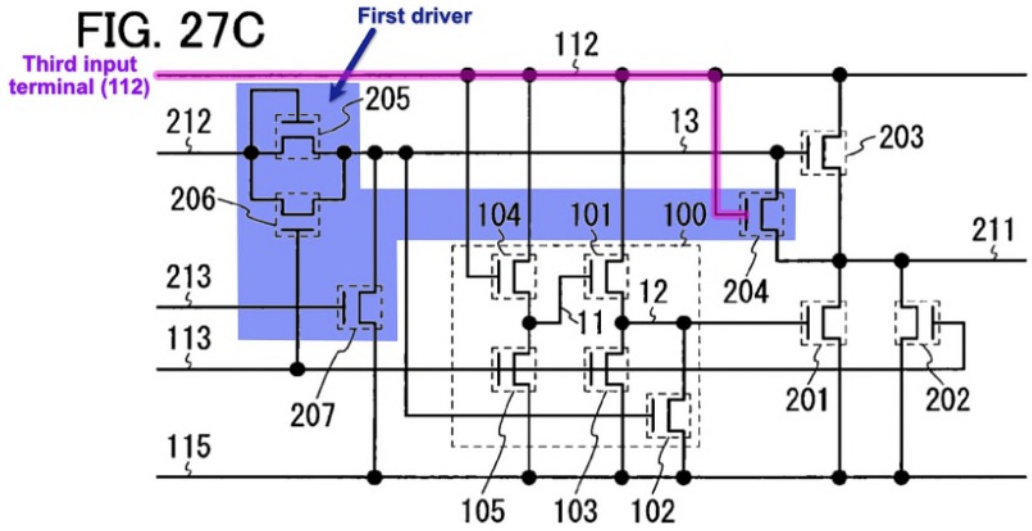
186. As was the case with the other claim limitations discussed above, Kimura's example timing charts show the impact that these received signals have on the potential of node 12. *See, e.g., id.*, Figs. 17B, 21B.

187. Thus, Kimura discloses this claim element of Claim 1 of the '593 patent.

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e. [1-d]: "the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver."

188. Kimura discloses this claim element of the '593 patent; this is evident via an annotated version of Figure 27C of Kimura:



Id., Fig. 27C (annotations added). As can be seen in this figure, the third input terminal (at 112) is connected directly to the gate of transistor 204; thus, the signal applied to the third input terminal (at 112) directly controls the on/off operation of transistor 204. As the annotations show, transistor 204 is part of the first driver.

189. In particular, Kimura teaches that "the gate of the transistor 204 is connected to the wiring 112." (*Id.*, ¶ [0286].) As was described above in the discussion of the preamble of Claim 1 ([1-pre], discussed in Section XII.A.1.a), "A signal IN1 is input" to the shift register's "wiring 112" *Id.*, ¶ [0104]. As Kimura describes repeatedly in its various timing diagrams (e.g., Figures 15A – 15C, Figure

17B, Figure 21B, Figure 25B, Figure 31C, and Figure 32B), the signal IN1 is a clock signal – which takes on either a high voltage (i.e., a high logic-level) or a low voltage (i.e., a low logic-level); these two logic levels will turn transistor 204 on and off (on for a high logic level, and off for a low logic level). Thus, this signal IN1, applied to the third input terminal, directly controls an on/off operation of transistor 204.

190. Thus, Kimura discloses this claim element of Claim 1 of the ’593 patent.

f. Claim 1 Summary

191. As just shown, Kimura discloses each element of Claim 1 of the ’593 patent; thus, Kimura renders obvious Claim 1 of the ’593 patent.

2. Dependent Claim 2

192. As an initial matter, Claim 2 depends from Claim 1; as was shown above, Claim 1 of the ‘593 patent is disclosed by Kimura.

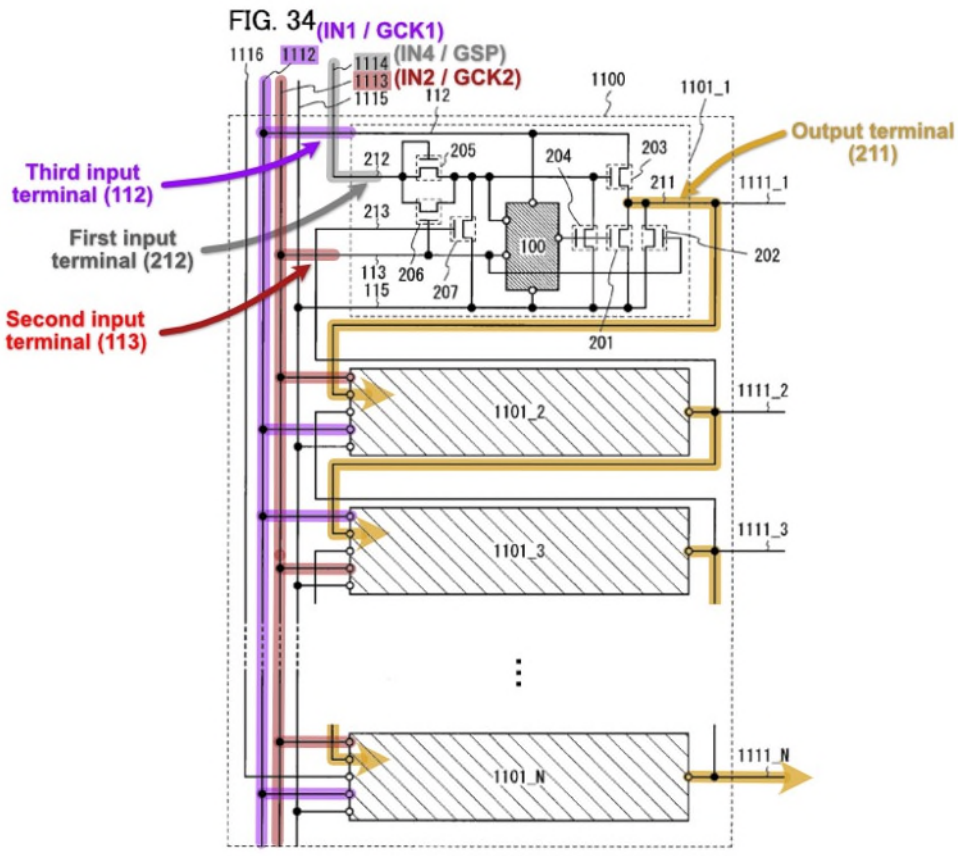
193. Claim 2 further requires that “wherein the first input terminal receives an output signal of a previous stage circuit or a start signal, wherein the second input terminal receives a first clock signal, and wherein the third input terminal receives a second clock signal.” Kimura discloses this claim of the ‘593 patent.

194. Preliminarily, I note that Claim 2 recites “an output signal” without reciting any relationship of this signal to the “output terminal” of Claim 1.

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195. To begin, note that the first part of the claim language just cited includes "wherein the first input terminal receives an output signal of a previous stage circuit or a start signal" (emphasis added). Because of the use of "or," the presence of this claim element term can be shown to be present in Kimura if the first input terminal receives "an output signal of a previous stage circuit" or "a start signal"; it will be shown here that Kimura discloses both of these two options.

196. Consider an annotated version of Figure 34 of Kimura:



Ex. 1004, Fig. 34 (annotations added). As was explained (at least in part) in the discussion of the preamble of Claim 1 ([1-pre]) in Section XII.A.1.a, Figure 34 of

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Kimura depicts an exemplary "shift register circuit 1100," which includes a series of "semiconductor device[s]" or "flip-flop circuits" 1101 – such as the embodiment shown in Figure 27C. *Id.*, ¶¶ [0333]-[0334]. As per Kimura, "the first input terminal [wiring 212] receives an output signal [GOUT] of a previous stage circuit or a start signal [IN4]," "the second input terminal [wiring 113] receives a first clock signal [IN2 or GCK2]," and "the third input terminal [wiring 112] receives a second clock signal [IN1 or GCK1]."

197. As shown in the annotated figure above, first stage 1101_1's "wiring 212" (Kimura's first input terminal) is connected to "wiring 1114." *Id.*, ¶ [0336]. "A signal GSP is input to the wiring 1114. The signal GSP can have a function which is similar to that of the signal IN4." Id. Again, per Kimura, signal IN4 "can function as a start pulse" for the shift register. *Id.*, ¶ [0266].

198. Thus, Kimura discloses the second of the two options in the claim language, as was noted above.

199. In addition, the stages also respectively output "signals GOUT_1 to GOUT_N" (the output signals). *Id.*, ¶ [0336]. According to Kimura, the output of a preceding stage is input into the subsequent stage – and thus provides a start signal that is supplied to that stage's wiring 212 (in lieu of the separate start pulse provided over wiring 1114 to the first stage): "the signal GOUT_i is input to a flip-flop circuit 1101_i+1" to allow that circuit to "start[] operation." *Id.*, ¶ [0338].

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200. Thus, Kimura also discloses the first of the two options in the claim language, as was noted above.

201. Finally, with regard to the rest of the claim language (involving the second input terminal and the third input terminal), wiring 112 (Kimura's third input terminal) and wiring 113 (the second input terminal) can respectively be supplied with "clock signal[s]" IN1 and IN2. *Id.*, ¶¶ [0104], [0109], [0230]-[0232]. These clock signals are depicted by annotation to Figure 34 – where they are depicted as a "signal GCK1 input to the wiring 1112, and a signal GCK2 … input to the wiring 1113." *Id.*, ¶ [0336].

202. Thus, Kimura renders obvious Claim 2 of the '593 patent.

3. Dependent Claim 3

203. As an initial matter, Claim 3 depends from Claim 2, and Claim 2 depends from Claim 1; as was shown above, Claim 1 and Claim 2 of the '593 patent are disclosed by Kimura.

204. Claim 3 further requires that "wherein the first clock signal and the second clock signal have the same period and have phases that do not overlap."

205. As an initial matter, the terms "period" and "phase"/"phases" require some discussion – as they must be evaluated in terms of the context and usage in the '593 patent.

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206. In the context of the ‘593, the term “period” is rather straightforward – as it is used in a conventional manner; the term period is defined[11] as “a portion of time determined by some recurring phenomenon,” and in particular as “the interval of time required for a cyclic motion or phenomenon to complete a cycle and begin to repeat itself.” This conventional, dictionary definition is sufficient for evaluation of the use of that term in Claim 3 of the ’593 patent – in that “period” is the amount of time that it takes for a recurring phenomenon to repeat itself.

207. This claim—and the ’593 patent—also uses the term “phases” (and, of course, the singular term “phase”).

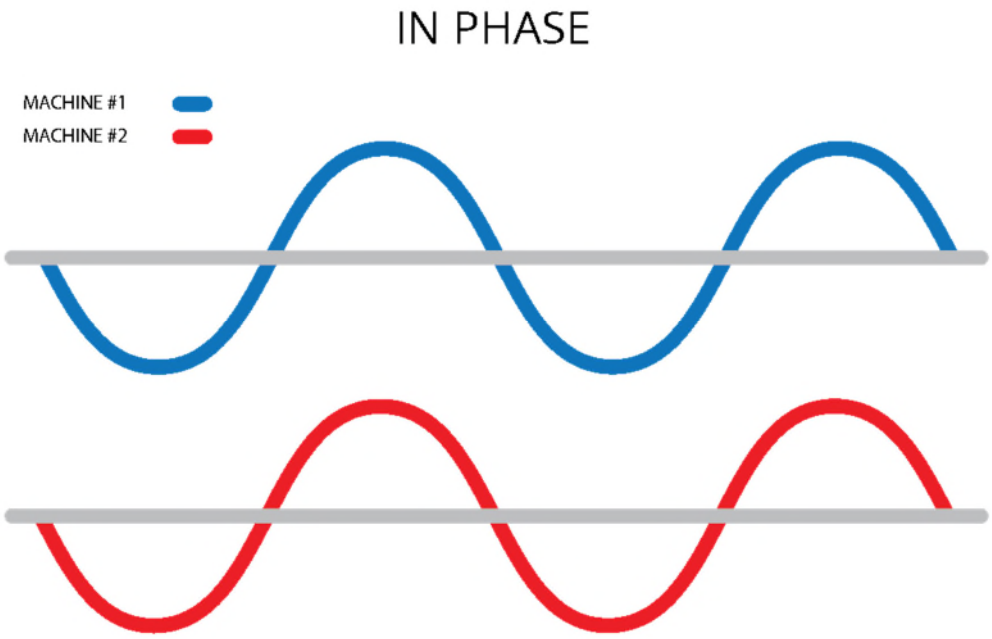
208. In terms of electrical signals, a conventional dictionary definition[12] of “phase” is “the point or stage in a period of uniform circular motion, harmonic motion, or the periodic changes of any magnitude varying according to a simple harmonic law to which the rotation, oscillation, or variation has advanced from its standard position or assumed instant of starting.” This is the most-commonly encountered definition of “phase” with respect to electrical signals – and is a slightly-complicated way of defining “phase” in terms of the degree (if any) of offset between two (otherwise-identical) sinusoidal signals.

[11] *E.g.*, https://www.merriam-webster.com/dictionary/period.

[12] *E.g.*, https://www.merriam-webster.com/dictionary/phase .

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209. First, consider two sinusoidal signals that are (in time) lined up exactly with each other[13]:



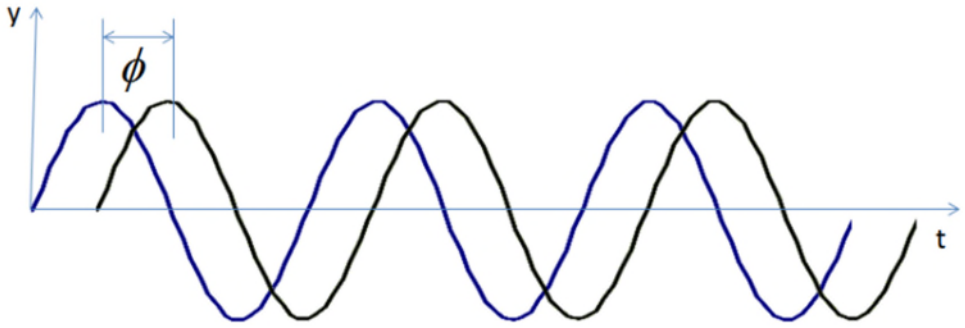
As the figure caption (at its top, above) indicates, these two sinusoidal signals are "in phase" – which means that they are lined up exactly (in time) with each other. (That is two sinusoidal signals are identical (and indistinguishable from each other) if their magnitudes, frequencies, and phases are identical.)

210. However, now consider the situation where the two otherwise-identical sinusoidal signals are *not* lined up together in time[14]:

[13] *E.g.*, https://ivctechnologies.com/wp-content/uploads/2019/08/Phase-Examples_In-Phase-1024x683.png .

[14] *E.g.*, https://i.stack.imgur.com/8hYOn.png .

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Here, the magnitude and frequency of the two sinusoids are still the same; however, they are shifted in time from each other – and therefore (unlike the "in-phase" situation above), they do not overlap exactly here.

211. Qualitatively, it is often said that these two signals are "out of phase." However, the problem also lends itself to quantitative analysis – and the use of the symbol φ serves to indicate *by how much* the two signals are "out of phase." For two sinusoidal signals that are "in phase," φ will equal zero. For two signals that are "out of phase," φ can be quantified as varying from -180° to +180° (or, if units of radians rather than degrees are used, $-\pi$ to $+\pi$).

212. However, as should be clear at this point, this conventional interpretation of "phase" and "phases" with respect to electrical signals does not apply to the teachings of the '593 patent – as the circuitry and signaling described in the '593 patent do *not* involve sinusoidal signals (which generally relate to analog signals and analog circuitry). Rather, the signaling and circuitry described in the '593 patent involve digital signaling – with circuitry that is clearly being used in a

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digital form; the former refers to square-wave waveforms that contain-and-convey digital (i.e., binary-on and binary-off) information, while the latter involve transistors being used as switches that are turned on or off (using the aforementioned digital signals).

213. Thus, the dictionary definition for "phase" cited above provides only a tangential understanding of the '593 patent and its claims.

214. The source cited above[15] also offers definitions of phase that appear to be somewhat more suitable – "a particular appearance or state in a regularly recurring cycle of changes" and "a distinguishable part in a course, development, or cycle." This implies that the use of the term "phase" in the '593 patent refers to a digital signal as having a "high" signal phase and a "low" signal phase – with a non-DC digital signal having times of having a "high" signal phase and times of having a "low" signal phase.[16]

215. Thus, a POSITA would give the terms "phase" and "phases" their plain-and-ordinary meaning(s) – in the context of the digital signaling waveforms discussed in the '593 patent. Again, as described above, any digital signaling

[15] *E.g.*, https://www.merriam-webster.com/dictionary/phase .

[16] For completeness, it can be said that, by implied definition, a DC digital signal would be in either a "high" signal phase or a "low" signal phase – but would not have this phase change during operation.

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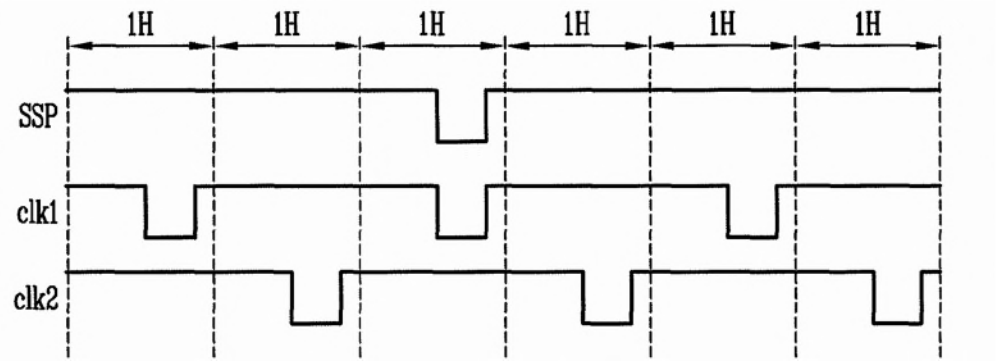
waveform would be in either a "high" signal phase or a "low" signal phase; further, it would be understood that no other phases are available or possible – as these are binary digital signals.

216. Turning now to the phrase "do not overlap" in Claim 3 of the '593 patent, the patent provides some guidance regarding this phrase in the specification at 5:16-28 – particularly at 5:21-28:

> In particular, times when the first and second clock signals CLK1 and CLK2 are supplied, e.g., the first and second clock signals CLK1 and CLK2 have a low level, *do not overlap*, although times when the first and second clock signals CLK1 and CLK2 are not supplied may overlap, e.g., both the first and second clock signals CLK1 and CLK2 may have a high level at the same time. ('593 patent at 5:21-28; emphasis added to highlight the claim language.)

(Note that as the '593 patent uses pMOS transistors, a "low level" corresponds to the on/active state, while a "high level" corresponds to the off/inactive state.) The key item from this excerpt (for the definition of the claim phrase "do not overlap") is the explanation that "the first and second clock signals… have a low level" and "do not overlap." This clearly shows that the meaning of "do not overlap" is that the two clock signals are not in the same state at the same time – with particular focus on the situation when one or the other clock signal has a low level (corresponding to the on/active state). This is readily seen via examination of Figure 4 of the '593 patent:

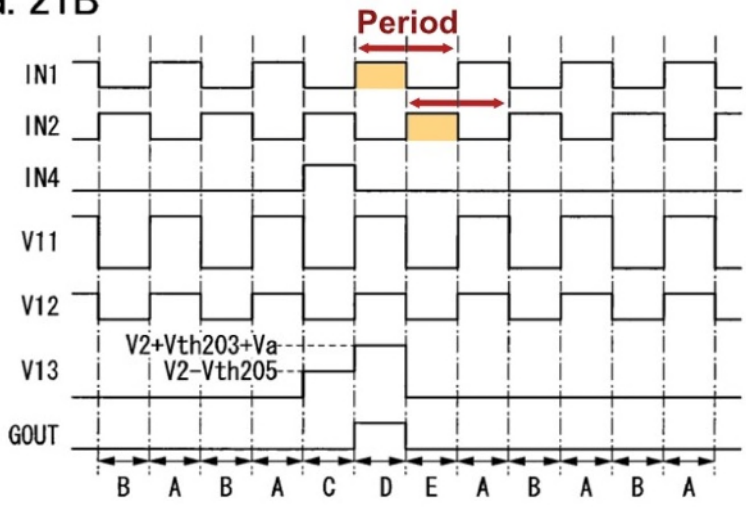
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As can be seen (and consistent with what was said above), the two clock signals (clk1 and clk2) do not overlap; that is, clk1 and clk2 are never both in the low (on/active) state at the same time.

217. Returning to Kimura, as shown in the annotated figure below, the first and second clock signals IN2 and IN2 have the same period and the same active phases, and do not overlap *e.g.*, IN1 and IN2 are high at different times (IN1 and IN2 are never both high at the same time, and never both low at the same time):

FIG. 21B



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Ex. 1004, Fig. 21B. Consistent with this, Kimura explains that IN1 and IN2 are clock signals that are "180° out of phase" with each other – which is a different way of stating what was already stated above. *Id.*, ¶¶ [0109], [0231].

218. Thus, Kimura renders obvious Claim 3 of the '593 patent.

4. Dependent Claim 4

219. As an initial matter, Claim 4 depends from Claim 3, which depends from Claim 2, which depends from Claim 1; as was shown above, Claim 1, Claim 2, and Claim 3 of the '593 patent are disclosed by Kimura.

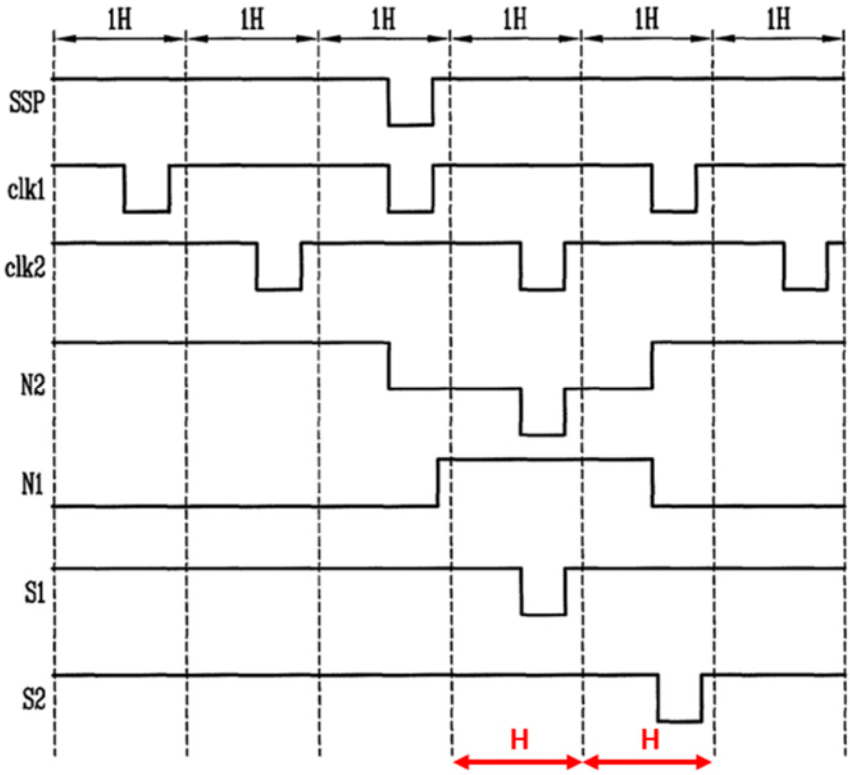
220. Claim 4 further requires "wherein the first clock signal and the second clock signal have a period equal to two horizontal periods 2H and are supplied in different horizontal periods as low signals." The language in this claim may be somewhat confusing – as the word "period" appears three times but the word clearly carries two different meanings depending on the usage.

221. The first instance of "period" is described via "the first clock signal and the second clock signal have a period"; this "period" is of the form described above with respect to Claim 3, in which "period" refers to the amount of time it takes for a recurring waveform to repeat itself.

222. The second instance of "period" occurs twice later in the claim, and refers (in both usages) to "horizontal periods"; this "period" refers to a particular amount of time (as in "a period of time"), and not to the repetition of a recurring

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waveform. More specifically, the ’593 patent refers to “a period in which a scan signal is supplied to one scan line” as an exemplary horizontal period. Ex. 1001, 5:18-20. This period corresponds to the time span between outputs of successive stages, e.g., between S1 and S2, as shown in an annotated version of ’593 patent Figure 4:



Id., Fig. 4 (annotated).

223. Thus, the claim basically states that the amount of time of the period of the recurring waveforms (the first clock signal and the second clock signal) is twice as long as two sub-periods (“H”) that, in sum, are the length (in time) of the time it takes for the recurring waveform to repeat itself. Further, the claim states that these

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sub-periods sum to "2H" – which means that each sub-period has a duration of H, so that the duration of the two sub-periods is the same.

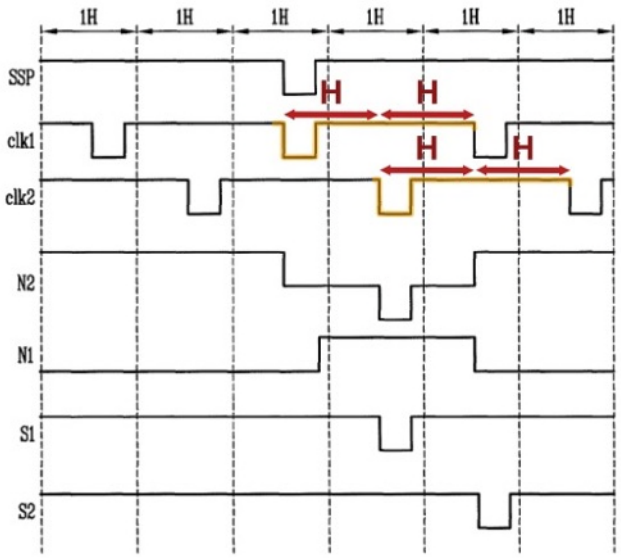
224. The final stipulation of Claim 4 is that the first clock signal and the second clock signal are "supplied in different horizontal periods as low signals." As the '593 patent uses pMOS transistors in its circuitry, low signals will be the turn-on voltage level for the transistors used in the circuitry in the '593 patent. So, essentially, this requirement is the same as the one discussed above with respect to Claim 3 and "phases that do not overlap."

225. In Kimura, there are stage circuit embodiments that use nMOS transistors (such as the embodiment of Figure 27C, which has been presented above), and stage circuit embodiments that use pMOS transistors (such as Figure 32A) that use pMOS transistors. As in both cases the transistors are used as simple switching transistors, there is no material difference between the use of nMOS transistors and the use of pMOS transistors in any particular circuit architecture – as was explained earlier (in Section VII.2). In terms of signaling, the only difference is that in an nMOS embodiment, high signals will provide the turn-on voltage – while, as discussed immediately above, in a pMOS embodiment, low signals will provide the turn-on voltage; however, providing waveforms in which one signal is off while the other signal is on will appear in essentially the same way – and, as mentioned above, the Claim 3 usage of "phases that do not overlap" applies here in the same way.

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226. Returning to Claim 4, Figure 4 of the ’593 patent provides an example of what this limitation requires.

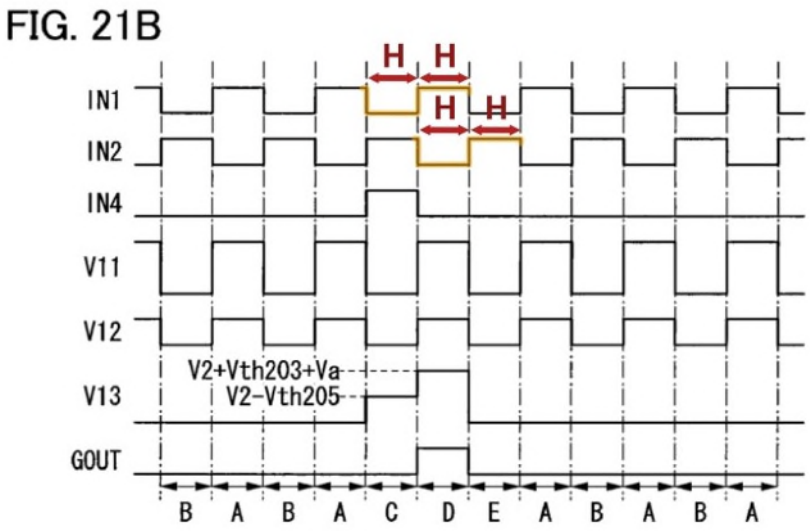
FIG. 4



Ex. 1001, Fig. 4 (annotations added). Signals CLK1 and CLK2 both span two of the time intervals labeled “1H” – and, further, the signals enter a low state (i.e., turn-on) in different, successive intervals:

227. In Kimura, signals are supplied across a series of equal “period[s]” of time A-E. *See* Ex. 1004, ¶ [0016]. This can also be seen graphically via an annotated version of Figure 21B of Kimura:

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Id., Fig. 21B. Both IN2 and IN1 span two of these periods and enter a low state in different, subsequent periods.

228. Thus, Kimura renders obvious this claim of the ’593 patent.

5. Dependent Claim 5

229. As an initial matter, Claim 5 depends from Claim 2, and Claim 2 depends from Claim 1; as was shown above, Claim 1 and Claim 2 of the ’593 patent are disclosed by Kimura.

230. Claim 5 further requires that “the start signal is supplied to overlap the first clock signal.”

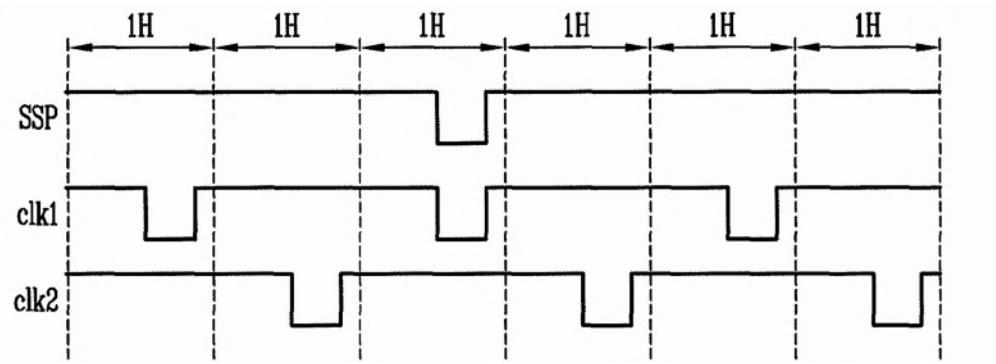
231. Here, in contrast to Claim 3 (discussed above in Section XII.A.3), Claim 5 refers to “overlap.” As was noted earlier in the Claim 3 discussion, the patent provides some guidance regarding this phrase in the specification at 5:16-28 – particularly at 5:21-28:

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> In particular, times when the first and second clock signals CLK1 and CLK2 are supplied, e.g., the first and second clock signals CLK1 and CLK2 have a low level, do not overlap, although times when the first and second clock signals CLK1 and CLK2 are not supplied may *overlap*, e.g., both the first and second clock signals CLK1 and CLK2 may have a high level at the same time. ('593 patent at 5:21-28; emphasis added to highlight the claim language.)

(Note once again that as the '593 patent uses pMOS transistors, a "low level" corresponds to the on/active state, while a "high level" corresponds to the off/inactive state.) In this excerpt, it is stated that an example of "overlap" occurs when the two clock signals "have a high level at the same time;" as this is an example ("e.g."), by implication it can be inferred that "overlap" of two signals occurs when those two signals have the *same* level (i.e., either both high or both low) at the "same time."

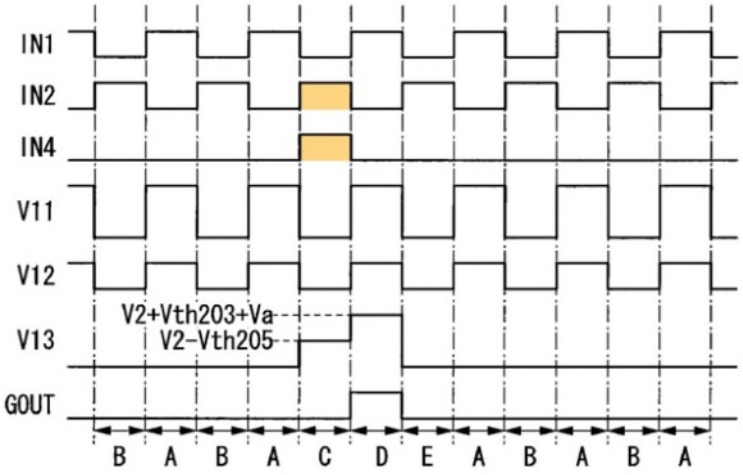
232. In Claim 5, the two signals at issue are "the start signal" and "the first clock signal." As with Claim 3, the situation can be understood by examination of Figure 4 of the '593 patent:



(Annotations added.) Unlike clock signals (which are continuously-running, essentially to infinity in time), the "start signal" (as shown via the annotation above) is a simple activation pulse – which exists only as a signal as the low-state pulse annotated above. As can be seen, the start pulse and the first clock signal (clk1) overlap – which exemplifies what Claim 5 of the '593 patent means by specifying that the start signal and the first clock signal overlap.

233. Returning to Kimura, as shown below, signal IN4 (which includes Kimura's start signal) and signal IN2 (the first clock signal) overlap – and have an active logic-high state during time interval C:

FIG. 21B



Ex. 1004, Fig. 21B (annotations added). Consistent with this annotated diagram, Kimura explains that "[i]n the period C" both "the signal IN2" and "the signal IN4" are "set to an H level." *Id.*, ¶¶ [0255], [0269]. As explained earlier, this timing diagram applies to embodiments in Kimura that use nMOS transistors; thus, "an H

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level" refers to a high logic-level signal – which is a turn-on signal for an nMOS transistor.

234. Thus, Kimura renders obvious this claim of the '593 patent.

6. Dependent Claim 6

235. As an initial matter, Claim 6 depends from Claim 2, and Claim 2 depends from Claim 1; as was shown above, Claim 1 and Claim 2 of the '593 patent are disclosed by Kimura.

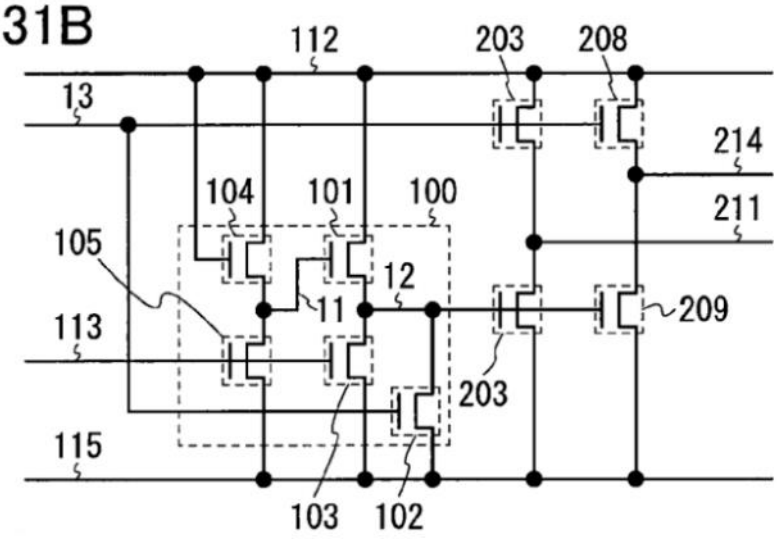
236. Claim 6 further requires that "the first driver includes: a first transistor between the first input terminal and the second node, the first transistor having a gate electrode coupled to the second input terminal; and a second transistor and a third transistor serially positioned between the second node and the first power supply, wherein a gate electrode of the second transistor is coupled to the third input terminal, and wherein a gate electrode of the third transistor is coupled to the first node." This is a verbal form of a topological description of circuitry – which describes the components of the described circuitry, the terminals of those components, and the way that the various terminals of the various components are connected together; further, this claim requires that the "first driver" include "first," "second," and "third" transistors arranged in a particular way.

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237. This claim is taught by Kimura when Figure 27C is modified to include the additional features of Figure 31B – and, as will be discussed below, a POSITA would be motivated to combine these two embodiments of Kimura.

238. According to Kimura, its devices—including that shown in Figure 27C—can be provided with additional transistors 208 and 209 like that in Figure 31B. Ex. 1004, ¶ [0304].

FIG. 31B



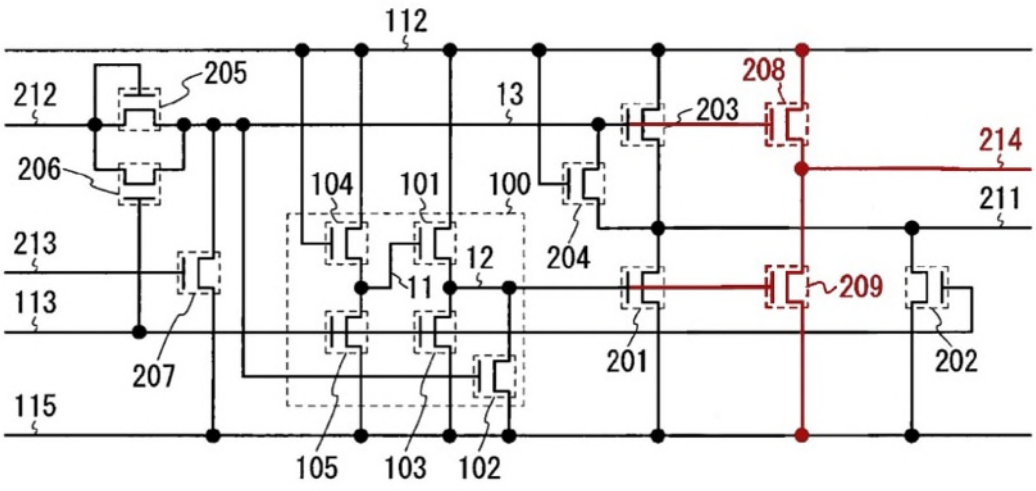
Id., Fig. 31B. As shown in Figure 31B, additional "[t]ransistor 208" has a gate is connected to "node 13," and operates to interconnect "wiring 112" to output "wiring 214." *Id.*, ¶ [0305]. Further, additional "transistor 209" has a "gate connected to the node 12" and interconnects "wiring 115" to output "wiring 214." *Id.* Thus, transistors 208 and 209 are (respectively) controlled by the signals applied to nodes 13 and 12 – and both of these transistors serve to deliver (when activated) output signals to output terminal 214: as can be seen by inspection of Figure 31B, these

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transistors (by one or the other being turned on – while the other transistor is turned off) control the output signal SOUT (at 214) – so that it is either a logic-low or a logic-high.

239. As Kimura further explains, the use of these additional transistors facilitates generation of a "different" output "signal SOUT" that "can be input to a semiconductor device in a different stage as a start pulse." *Id.* The signal SOUT is intended to lower "delay or distortion" in the shift register. *Id.*

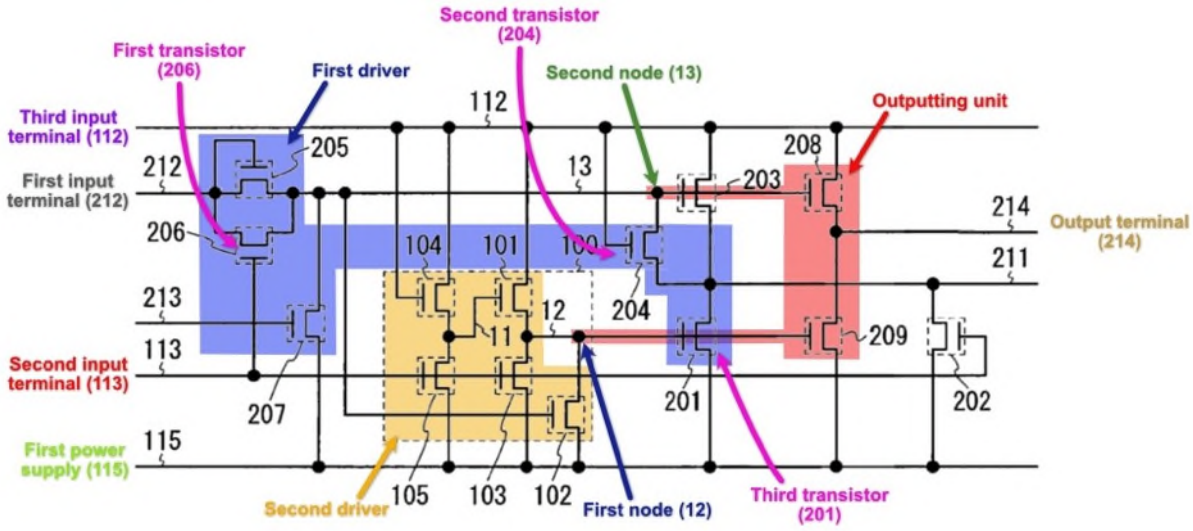
240. When these additional transistors (and their associated wiring) are added to the embodiment of Figure 27C in the manner taught by Kimura (as just discussed), this results in the following circuitry (with the added elements shown in red):



See id., Figs. 27C, 31A-B (annotated and combined).

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241. In this combined embodiment, the second driver remains unchanged from what it is in Figure 27C alone; however, the first driver here expands to include transistor 201, while the outputting unit now comprises transistors 208 and 209 (which, as detailed above, provide an output signal to 214).

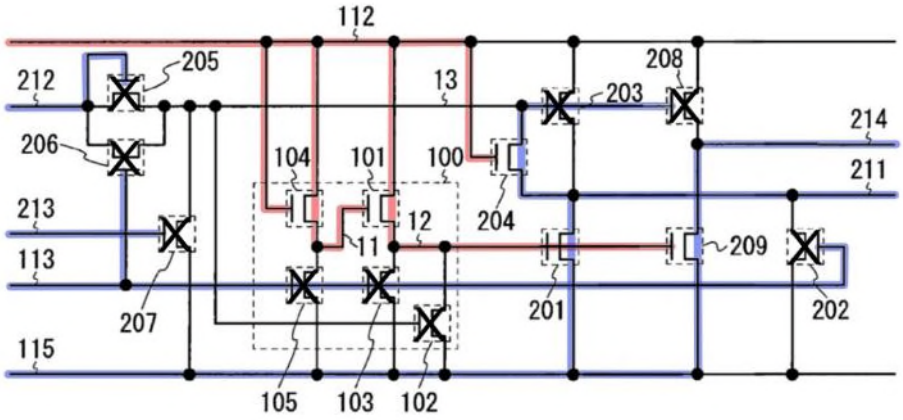


As can be seen, added transistors 208 and 209 now form the device's outputting unit supplying a signal SOUT to wiring 214 (the output terminal); these transistors are controlled by the same node 12 (the first node) and node 13 (the second node) employed by the device of Figure 27C. As can also be seen, the various inputs (112, 113, 212, and 115) also remain the same as they are in Figure 27C.

242. However, while one of the functions of transistor 201 is to control the output to wiring 211, it also operates to connect wiring 115 to node 13 (the second node) via transistor 204. *See* Ex. 1004, Figs. 27C. This allows for the provision of V_1 – which is carried by this wiring to node 13 when the voltage of node 12 and the

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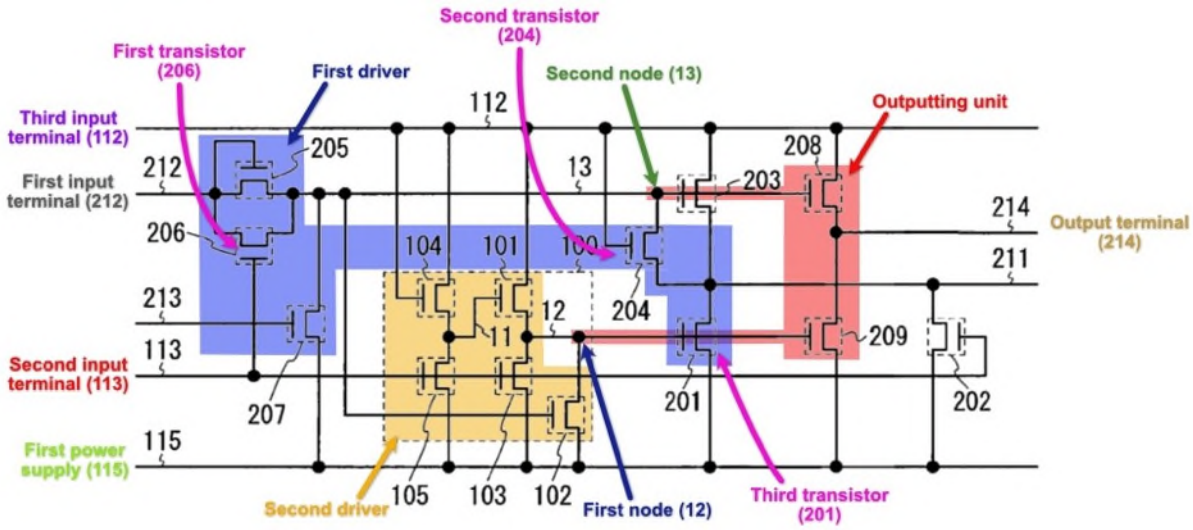
signal IN1 are both high (*i.e.*, during time period A) . *Id.*, Figs. 17B, 21B, 25B, 31C. An example of this is shown below:



Because one of transistor 201's functions is to (along with other transistors) control the voltage on node 13, it clearly should be considered to be part of the first driver. Moreover, while the transistor does—during certain time periods—relay a signal to output wiring 211, it does not do so with respect to output wiring 214; thus, it is clearly not part of the outputting unit that is here responsible for generating output on wiring 214; only transistors 208 and 209 generate such output – as was described above.

243. Thus, when Figure 27C is modified to include additional transistors 208 and 209, it teaches everything that Claim 6 requires. To reprise the annotated figure shown earlier,

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In particular, as shown above, the first driver of Figures 27C and 31B now includes the required "first transistor [206] between the first input terminal [wiring 212] and the second node [13], the first transistor [206] having a gate electrode coupled to the second input terminal [wiring 113]." In addition, this first driver also includes "a second transistor [204] and a third transistor [201] serially positioned between the second node [13] and the first power supply [wiring 115]," that "a gate electrode of the second transistor [204] is coupled to the third input terminal [wiring 112]," and that "a gate electrode of the third transistor [201] is coupled to the first node [12]."

244. Finally, for the reasons cited earlier, a POSITA would have been motivated to apply additional output 214 and transistors 208 and 209 of the embodiment of Figure 31B to the embodiment of Figure 27C – and would have a reasonable expectation that this combination would be successful. Of particular note, as was explained earlier, Kimura itself contemplates the addition of the two

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additional transistors 208 and 209 to its other embodiments (including that shown in Figure 27C). Thus, Kimura itself instructs—and motivates—the combination.

245. Further, Kimura clearly describes the reason for this combination and the motivation for this combination – that incorporation of the two additional transistors improves shift register operation, by inducing the signal distortion to be reduced, and to cause the signal delays inherent in the passing of signals from shift register stage-to-stage to be reduced.

246. Thus, Kimura renders obvious this claim of the ’593 patent.

7. Dependent Claim 7

247. As an initial matter, Claim 7 depends from Claim 2, and Claim 2 depends from Claim 1; as was shown above, Claim 1 and Claim 2 of the ’593 patent are disclosed by Kimura.

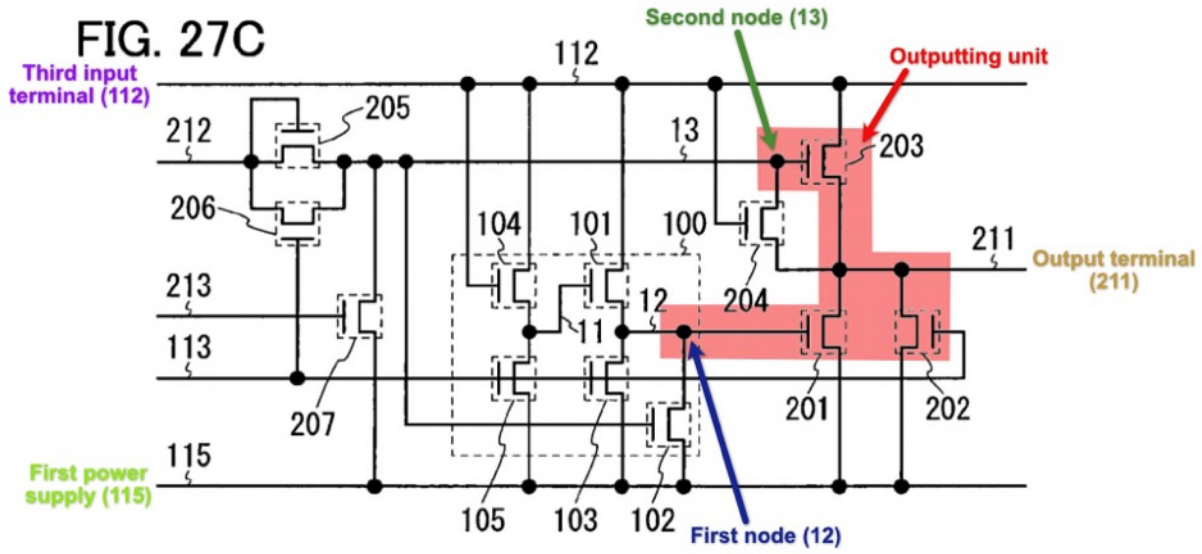
248. Claim 7 further requires:

> wherein the outputting unit includes:
>
> a fourth transistor between the first power supply and the output terminal, the fourth transistor having a gate electrode coupled to the first node;
>
> a fifth transistor between the output terminal and the third input terminal, the fifth transistor having a gate electrode coupled to the second node;
>
> a first capacitor between the second node and the output terminal; and

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a second capacitor between the first node and the first power supply.

Similar to Claim 6 above, this is a verbal form of a topological description of circuitry. Further, as was also the case for Claim 6, how this topological description reads on Kimura here in connection with Claim 7 is best described via revisiting a previously included annotated version of Figure 27C of Kimura:



Ex. 1004, Fig. 27C (annotations added). As can be seen by inspection, this embodiment of Kimura has all of the claim elements of Claim 7 – except for the first capacitor and the second capacitor.

249. However, a POSITA examining this circuitry would reach several conclusions – since these conclusions are well-known in the art.

250. First, a POSITA would recognize that the first node (12) will be electrically isolated whenever all of the transistors which provide electrical access

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to this node (101, 102, 103, 104, and 105) are turned off. In the same way, a POSITA would recognize that the second node (13) will be electrically-isolated whenever all of the transistors which provide electrical access to this node (204, 205, 206, and 207) are turned off.

251. Second, a POSITA would also understand that the amount of charge stored at the node would determine the isolated voltage at that (floating) node – using the simple and well-known equation

$$Q = CV,$$

where Q is the charge on the node, V is the resulting voltage at the node, and C is the capacitance at the node. For example, when there is no capacitor associated with a node, then the capacitance would be supplied only by the wiring and transistors[17] (and the parasitic capacitances of any adjacent transistors) to which the node is connected. However, as the wiring and transistors hold very little charge, they provide very little capacitance. And thus, the resulting voltage value will be based upon a very small amount of charge.

252. This can be problematic, since perturbations in the amount of charge (for example, due to electromagnetic interference (EMI) or interline crosstalk during digital switching events) may cause sizeable changes in the voltage on the node;

[17] All field-effect transistors include small parasitic capacitances; usually, these capacitances are so small that they are not explicitly included in the circuit diagram.

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these types of signal integrity issues are undesirable. Therefore, a POSITA would be motivated to seek methods of making the circuitry of Kimura more robust against a problem of this sort by including further capacitors.

253. In addition, the "isolation" of a node is being provided by turning off all the transistors that provide electrical connection(s) to that node (with the node *not* being isolated when any one of them is turned on). However, as described in Section VII.A.4, a transistor does not turn off perfectly – and some off-state leakage current will be present. If the voltage at the isolated node (e.g., 12 or 13) is defined by a very small amount of charge, then that charge will leak away very quickly via the imperfect off-state of the transistors – and the voltage will change quickly with time, and may even quickly reach the voltage that is its inevitable endpoint.

254. As a POSITA would thus know, the voltage at this node would be made more robust (i.e., it would be able to hold the isolated voltage value more stably against upsets like EMI, and the stored charge (which provides the stored voltage) would take a longer time to discharge away through the imperfect off-state transistors and thus the isolated voltage on the node would be retained for a much longer time) if the capacitance at the node could be increased. This is actually quite easily done – by adding a capacitor to the isolated node, so that the amount of charge used to create the voltage at the node is much larger; as can readily been seen from

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the equation presented above, for the same voltage, a larger capacitance would hold a proportionately larger charge.

255. Thus, a POSITA looking at the circuitry of Kimura would realize that these vulnerabilities exist and that they could be mitigated by adding a properly-connected capacitor at each node. This will make the charge on the isolated node more robust when that node is first charged up and is then electrically isolated from the rest of the circuitry.

256. Thus, it would be a relatively straightforward decision to conclude that the first node (12) and the second node (13) in Kimura should have a capacitor included and connected to each of them – for the reasons just cited above.

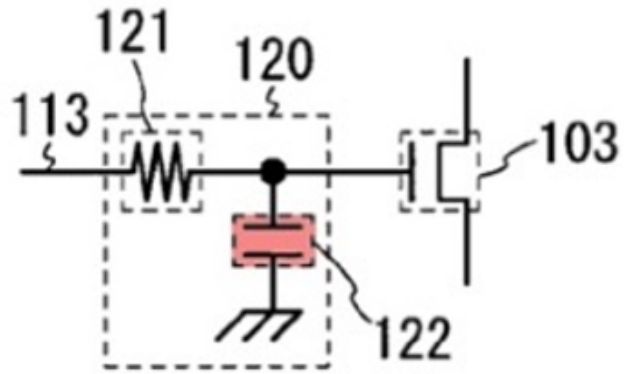
257. Using capacitors to address these problems is something that is well-known in the art – as will be discussed in more detail in Section XII.C.2 and Section XII.E.2. As a brief summary of two notable instances, Jeong provides an example – wherein capacitors are added to a shift register's output transistors (or to any similarly-affected circuitry), so to mitigate the problems described above. *See* Ex. 1007, ¶ [0056]. Another reference – U.S. Patent Publication No. 2007/0263763 A1 to Moon ("Moon") – also explains why one would wish to add capacitors to a shift register circuit (or any similarly-affected circuit), so as to mitigate the problems described above. *See* Ex. 1020, ¶ [0053].

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258. In addition to this knowledge in the art (which would have been well-known to a POSITA), Kimura itself already advises that "[c]apacitors can be additionally provided" along with the transistors in its shift register. Ex. 1004, ¶ [0198].

259. For example, a "capacitor 122" can be connected between wiring 115 and the wiring leading to the gate of a transistor (like transistor 103 in Figure 1A) that generates the circuit's output signal. *Id.*, ¶¶ [0190]-[0191]. An example of this inclusion is provided by Kimura in Figure 9C:

FIG. 9C

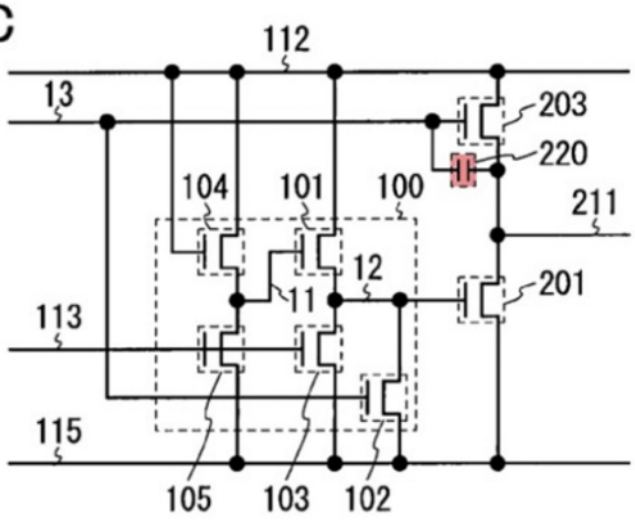


Id., Fig. 9C (annotated). According to Kimura, doing so reduces the "fall time of the signal OUT." *Id.*, ¶¶ [0190]-[0191]. However, a capacitor added in this manner (between node 12 and the power supply wiring 115) will also provide robustness to the node against signal integrity threats, as detailed above.

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260. Additionally, Kimura describes how a "capacitor 220" can be "connected between the node 13" and output "wiring 211." *Id.*, ¶ [0302]. An example of this inclusion is provided by Kimura in Figure 30C:

FIG. 30C



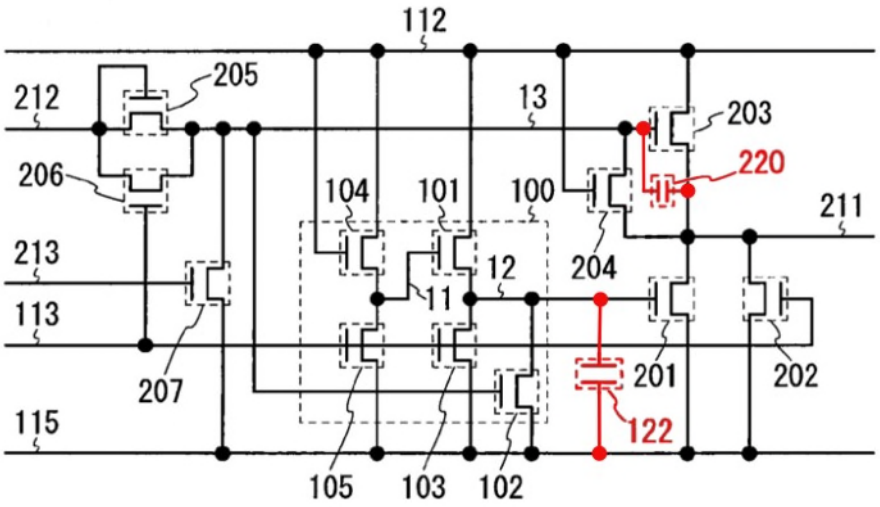
Id., Fig. 30C (annotated). Kimura also explains that inclusion of this capacitor serves to "shorten" "the fall time or rise time" of the output signal. *Id.*, ¶ [0303]. .

261. Using Kimura's teachings (as described above) and the knowledge of a POSITA (also described above), Figure 27C would obviously be modified with the addition of two capacitors for the reasons described above. For instance, an added capacitor like capacitor 122 would add node robustness, while an added capacitor like capacitor 220 would shorten the output signal's rise/fall time. A POSITA would also have had a reasonable expectation of success, not only because Kimura already contemplates the addition of capacitors to its shift register nodes, but also because

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this was commonly and routinely done in the prior art for the reasons discussed above.

262. The addition of the two capacitors is shown below (with the added elements highlighted red). Capacitor 122 is added between node 12 and the power supply wiring 115, while capacitor 220 is added between node 13 and the output wiring 211:



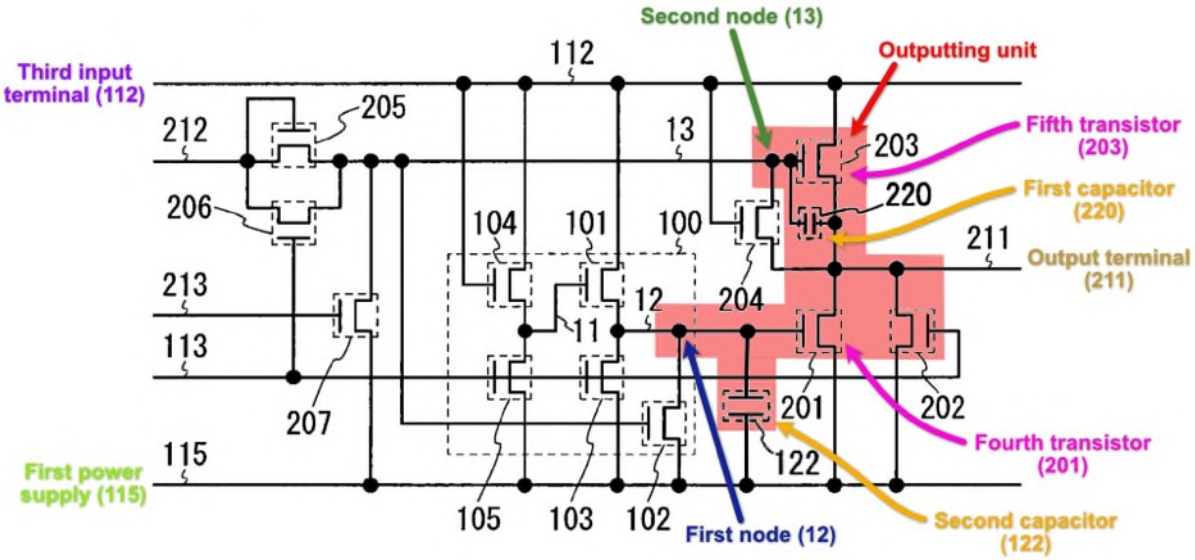
(The added elements are highlighted red).

263. With these modifications, the outputting unit now includes a fourth transistor [201] between the first power supply [wiring 115] and the output terminal [wiring 211], the fourth transistor [201] having a gate electrode coupled to the first node [12]" and "a fifth transistor [203] between the output terminal [wiring 211] and the third input terminal [wiring 112], the fifth transistor [203] having a gate electrode coupled to the second node [13] – as well as a first capacitor [220] between the

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second node [13] and the output terminal [wiring 211], and a second capacitor [122] between the first node [12] and the first power supply [wiring 115].

264. Moreover, the "outputting unit" also now includes "a first capacitor [220] between the second node [13] and the output terminal [wiring 211]," and "a second capacitor [122] between the first node [12] and the first power supply [wiring 115]."



265. Thus, it is my conclusion and opinion that a POSITA would have been motivated to include these capacitors and would have expected the inclusion to be successful.

266. Thus, Kimura renders obvious this claim of the '593 patent.

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8. Dependent Claim 8

267. As an initial matter, Claim 8 depends from Claim 2, and Claim 2 depends from Claim 1; as was shown above, Claim 1 and Claim 2 of the ’593 patent are disclosed by Kimura.

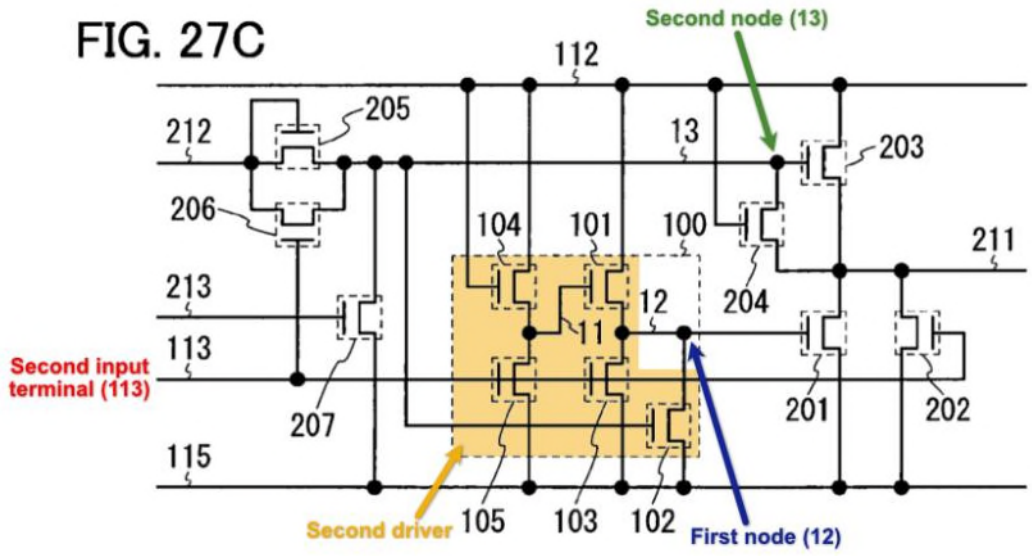
268. Claim 8 further requires:

> a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and
>
> a seventh transistor between the first node and a second power supply, the second power supply having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal.

269. Once again, this is a verbal form of a topological description of circuitry.

270. As an initial matter, the “second driver” of the embodiment depicted in Figure 27C of Kimura was discussed in the evaluation of claim element [1-c], which was discussed in Section XII.A.1.d.

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Ex. 1004, Fig. 27C (annotations added); *see also supra* limit [1-c]. As was explained in that earlier discussion – and as can be seen here – the second driver includes transistors 101-105.

271. However, while none of Figure 27C's transistors are connected in the way the claim requires, Kimura provides a number of design alternatives (in the text of the specification) for use with its stage circuits.

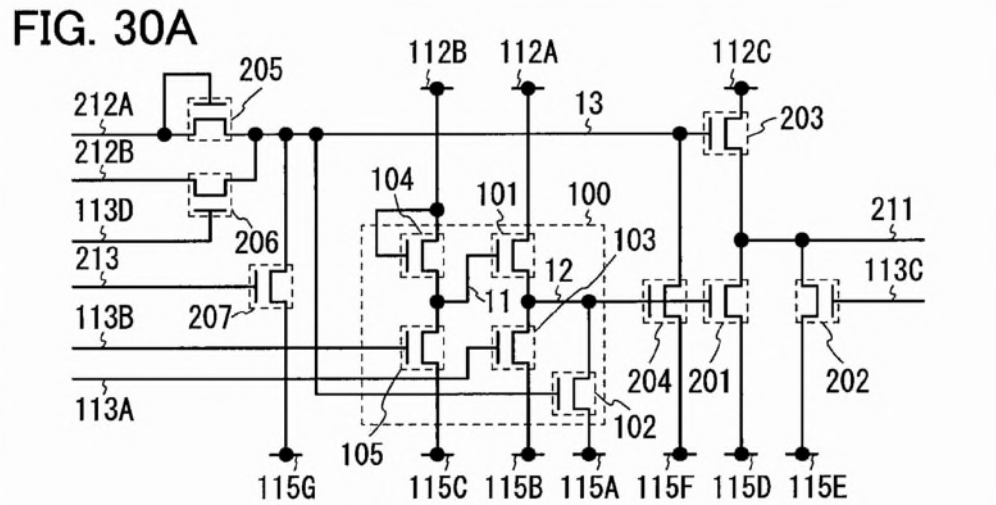
272. For instance, "the first terminal of the transistor 102" can be "connected to the wiring 113" instead of wiring 115. *Id.*, ¶ [0169]. This, according to Kimura, "suppresse[s]" transistor "deterioration." *Id.* (The background of the issues of possible "dielectric breakdown or deterioration of transistors" was briefly discussed in the overview of Kimura provides in Section IX.A.)

273. When transistor 102 is connected to wiring 113, the device of Figure 27C includes the claimed "sixth transistor"; here, transistor 102 is located between

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the "first node" (node 12) and the "second input terminal" (wiring 113) – and in addition, the gate of transistor 102 is coupled to the "second node" (node 13).

274. Also, Kimura explains that its stage circuits can employ "a power supply voltage, reference voltage, ground voltage, ground, or negative power supply voltage." *Id.*, ¶ [0105]. Moreover, Kimura also teaches that the same stage circuit can be provided with multiple different power supply voltages. *See id.*, ¶¶ [0173], [0299]. For instance, in Figure 30A, transistor 105 is connected to a different power supply with a different voltage (wiring 115B) than is output transistor 201 (wiring 115D).



Id., Fig. 30A. The use of more-than-one power supply voltage level (as, among other things at least, a high logic-level or a low logic-level) is a common and well-known practice in circuit design and circuit operation – one which has been known in the art for a considerable period of time (and predates the '593 patent); for example, the main circuitry may use a power supply voltage that is lower than the

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power voltage used with, e.g., the I/O (input/output) drivers – since larger current are often required for signals to be driven out of the circuitry and into external connections; the reason for this use of a larger current was actually explained during the discussion above of Claim 7 (Section XII.A.7), where the issue of delay time in digital switching events was considered. Clearly, all of this would have been known to a POSITA at the time of the '593 patent.

275. When transistor 103 is connected to wiring 115B and transistor 201 is connected to wiring 115D, the device of Figure 27C includes the claimed "seventh transistor": transistor 103 it is located between the "first node" (node 12) and "second power supply" (wiring 115B), and has its gate connected to "second input terminal" (wiring 113).

276. Consistent with this, Kimura explains that wiring 115B can be supplied with a relatively "negative power supply voltage." *Id.*, ¶ [0105]. Similarly, Kimura explains that "an H-level signal can be supplied to the first terminal of transistor 103.[18]" *Id.*, ¶¶ [0162], [0170]. Thus, just as this claim requires, Kimura renders what

[18] The identity of the "first terminal" mentioned here is explained at [0161] with reference to Figure 1A – and, referring to Figure 1A, it is the "lower" terminal of transistor 103 (i.e., the one connected there to the wiring 115); as explained in Section VII.A.1, whether this is terminal is specifically-identified as being either the "source" or the "drain" of the transistor depends on the specific voltages applied to

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this claim requires obvious: transistor 103 receives a negative "second power supply" that has a voltage lower than the positive voltage of the "first power supply."

277. Because Kimura itself identifies these alternatives for use—and considers them acceptable—a POSITA would have been motivated and considered it highly obvious to apply them to the device of Figure 27C; further a POSITA would have had a reasonable expectation of success when doing so.

278. Thus, Kimura renders obvious this claim of the '593 patent.

9. Dependent Claim 14

279. As an initial matter, Claim 14 depends from Claim 1; as was shown above, Claim 1 of the '593 patent is disclosed by Kimura.

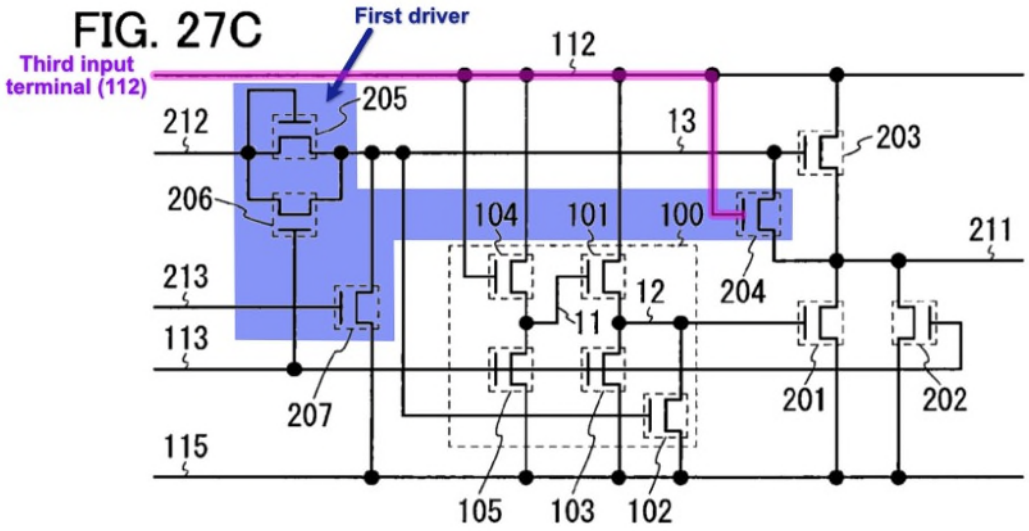
280. Claim 14 further requires that "the transistor controls the voltage of the second node according to the on/off operation thereof."

281. As an initial matter, Claim 14 simply states "the transistor"; the only "transistor" mentioned by name in Claim 1 appears in claim element [1-d] ("the signal of the third input terminal directly controls an on/off operation of *a transistor*, the transistor included in the first driver"; emphasis added) – which was discussed earlier in Section XII.A.2.e.

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the transistor terminals at any given moment in time – with the identification possibly changing in time, even though the circuit topology itself does not change.

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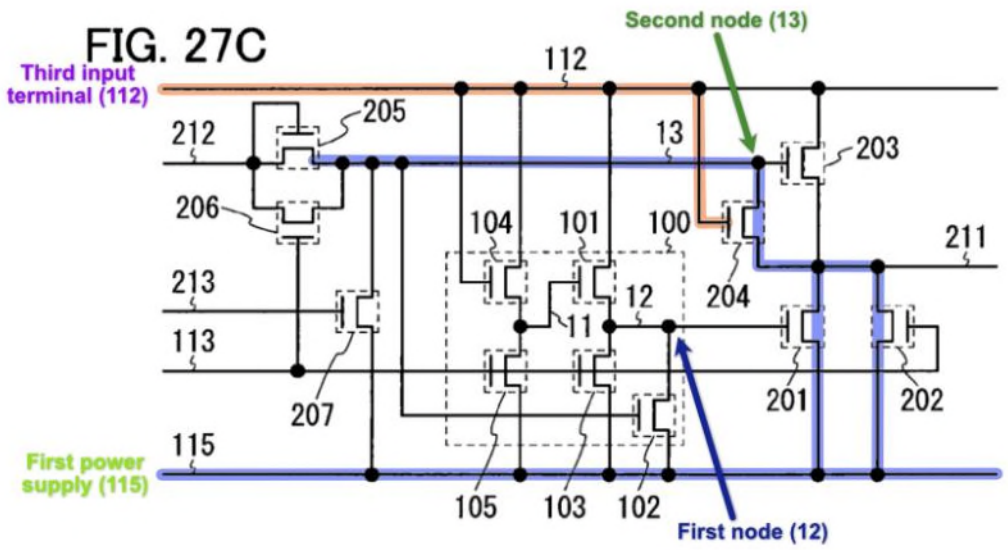


Ex. 1004, Fig. 27C (annotated). Thus, transistor 204 is duly identified as being "the transistor" of Claim 14.

282. Further, as shown above, and as also discussed in the context of claim element [1-d], "the signal of the third input terminal directly controls an on/off operation of a transistor (204). *Id.*, Fig. 27C (annotated). The only additional functionality included in Claim 14 is that "the transistor controls the voltage of the second node," since the second part of the claim was already demonstrated in the discussion of claim element [1-d] (that is, "directly controls an on/off operation of a transistor").

283. This addition in Claim 14 is readily shown by simple examination of the annotated circuit figure presented just above – as the implications of what occurs when transistor 204 is turned on are readily apparent:

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Id., Fig. 27C (annotations added). As can be seen, when a clock signal[19] is applied to the third input terminal such that it turns on transistor 204, when either transistor 201 or transistor 202 is also turned on, the voltage of the first power supply will be passed to the second node. (On the other hand, when the aforementioned clock signal is such that it turns transistor 204 off, this functionality is not available.)

284. Therefore, the transistor (204) controls the voltage of the second node according to the on/off state of that transistor (204).

285. Thus, Kimura renders obvious Claim 14 of the '593 patent.

[19] As shown in the discussion involving Claim 2 (in Section XII.A.2) the third input terminal receives a clock signal.

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10. Independent Claim 15

286. It is my conclusion and opinion that Claim 15 of the ’593 patent is rendered obvious by Kimura.

a. [15-pre]: “An organic light emitting display, comprising:”

287. Regardless of whether or not this preamble language is limiting (and, for the reasons that I discuss below in connection with the Tobita reference it is not), it is taught by Kimura.

288. For example, Kimura explains that its “shift register” is intended for use with a “display device.” Ex. 1004, ¶ [0320]. And, this display can employ “an organic EL element” for its “light emitting layer.” *Id.*, ¶ [0388]. The term “EL” is typical shorthand for “electroluminescent” – and a light-emitting diode (LED) is considered to be a type of electroluminescent element; further, such LEDs are used in displays – such as organic light-emitting displays. Thus, at a bare minimum, the term “organic EL” would at least encompass the term “OLED.”

289. Thus, Kimura renders obvious the preamble of Claim 15 of the ’593 patent.

b. [15-a]: “pixels positioned in regions partitioned by scan lines and data lines;”

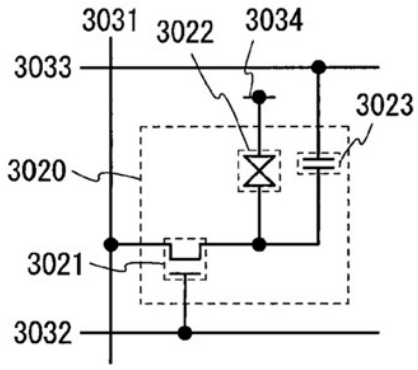
290. Kimura discloses this claim element of Claim 15 of the ’593 patent.

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291. Kimura explains that its display includes a "circuit 1001, a circuit 1002, a circuit 1003, a pixel portion 1004, and a terminal 1005." Ex. 1004, ¶ [0321]. The pixels are arranged in multiple "row[s]" and "columns." *Id.*, ¶ [0349]. The use of rows and columns of pixels is a well-known and commonly-used technique in the structure of displays – and goes back to the earliest development of displays, such as early televisions. Kimura's display—like all such displays—is formed from a matrix of pixels.

292. Figure 33E of Kimura depicts a single "pixel portion." *Id.*, ¶ [0330].

FIG. 33E



Id., Fig. 33E. As Kimura explains, "pixel 3020" is surrounded by and connected to both a "wiring 3031" and "wiring 3032." *Id.*, ¶ [0330-0331]. "A video signal is input … to the wiring 3031." *Id.* Thus, this is the claimed "data line" - as it is responsible for activating certain pixels for purposes of displaying an image. Furthermore, "A scan signal … is input … to the wiring 3032." *Id.*, ¶ [0331]. This is the claimed "scan line" – as it activates the rows of pixels one row at a time.

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293. While Figure 33E shows only one pixel, a POSITA would understand that Kimura's display is formed by an array or matrix of such pixels. Video signal wirings 3031 would be located between the pixel columns. And, scan signal wiring 3032 would be located between the pixel rows.

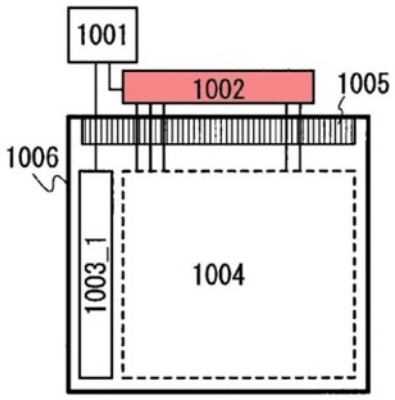
294. Thus, Kimura renders obvious this claim element of Claim 15 of the '593 patent.

c. [15-b]: "a data driver for supplying data signals to the pixels through the data lines; and"

295. Kimura discloses this claim element of Claim 15 of the '593 patent.

296. This can be readily seen by examination of an annotated version of Figure 33A of Kimura:

FIG. 33A



Ex. 1004, Fig. 33A (annotation added). As Kimura explains, the display includes a "circuit 1002" that "functions … as a driver circuit" for "supplying a video signal to the pixel portion 1004." *Id.*, ¶ [0323]. This is the "data driver" of this claim element.

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297. Thus, Kimura renders obvious this claim element of Claim 15 of the ’593 patent.

d. [15-c]: “a scan driver for supplying scan signals to the pixels through the scan lines, the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals and having a first input terminal, a second input terminal, a third input terminal, and an output terminal,”

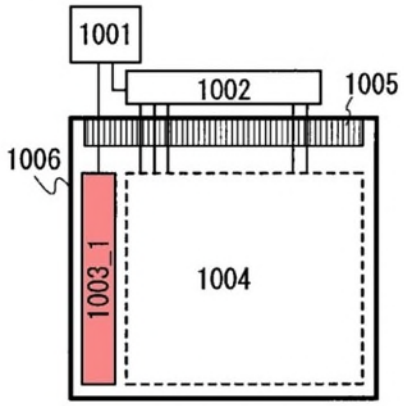
298. Claim element [15-c] is rather long – and thus the analysis will be simpler to explain if this claim element is broken up into sub-elements.

i. [15-c-1]: “a scan driver for supplying scan signals to the pixels through the scan lines”

299. Kimura discloses this claim sub-element of claim element [15-c] of Claim 15 of the ’593 patent.

300. This can be readily seen by further examination of Figure 33A of Kimura:

FIG. 33A



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Ex. 1004, Fig. 33A (annotations added). According to Kimura "circuit 1003_1" operates as a "scan line driver" for "supplying a scan signal … to the pixel portion 1004." *Id.*, ¶ [0324].

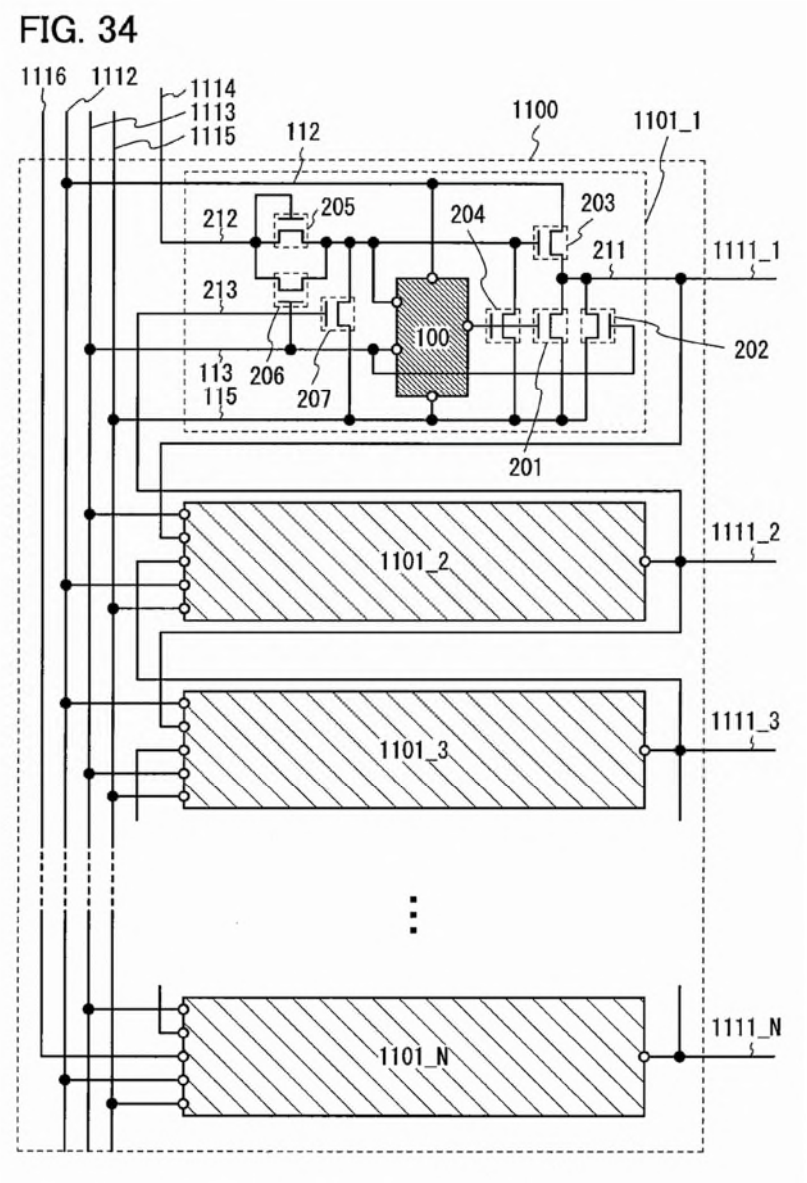
301. Thus, Kimura discloses this claim sub-element of claim element [15-c] of the '593 patent.

ii. [15-c-2]: "the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals"

302. Kimura discloses this claim sub-element of claim element [15-c] of Claim 15 of the '593 patent.

303. This is readily seen via examination of Figure 34 of Kimura – which was already discussed at this level of detail above, in the evaluation of Claim 1 (Section XII.A.1) and of Claim 2 (Section XII.A.2).

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Ex. 1004, Fig. 34. As Kimura explains, a "shift register circuit" like that shown in Figure 34 "can be included in "the circuit 1003_1." *Id.*, ¶ [0333]. Further, this shift register circuit includes a number of stages in the form of "flip-flop circuits 1101_1 to 1101_N." *Id.*, ¶ [0334] – and each of these stages outputs, in turn, signals "GOUT_1" to "GOUT_N" to "wirings 1111_1 to 1111_N." *Id.*, ¶¶ [0335]-[0336].

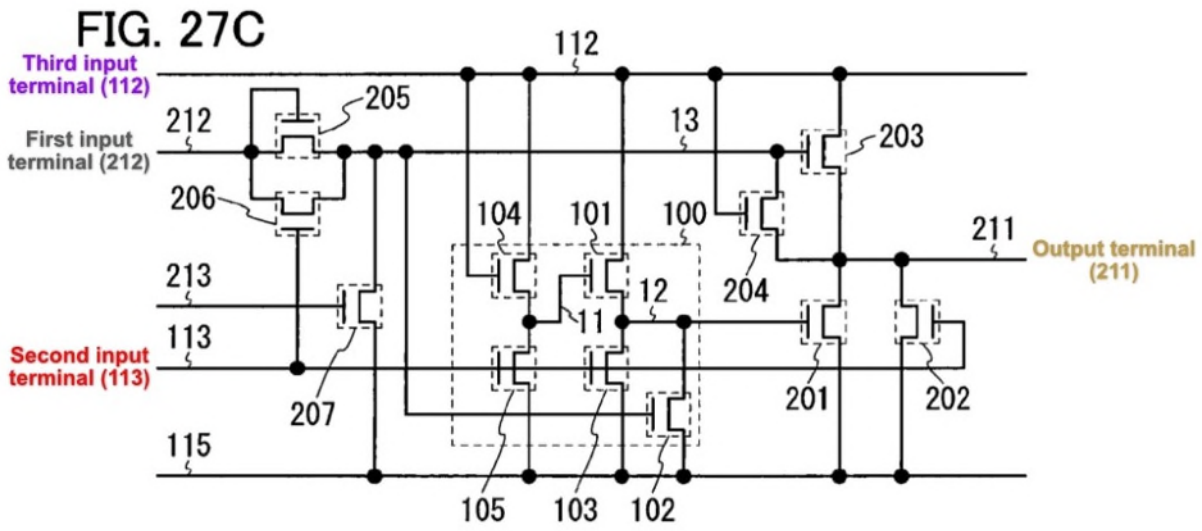
Finally, Kimura notes that any of the circuits of "Embodiments 1 or 2" can be used to form the stages. *Id.*, ¶ [0333].

304. Thus, Kimura discloses this claim sub-element of claim element [15-c] of Claim 15 of the '593 patent.

iii. [15-c-3]: "and having a first input terminal, a second input terminal, a third input terminal, and an output terminal,"

305. This claim sub-element of claim element [15-c] of Claim 15 of the '593 patent is disclosed by Kimura.

306. This claim sub-element is essentially identical to the preamble of Claim 1 of the '593 patent – which was already discussed in detail earlier (at Section XII.A.1.a) – where it was shown that these details are disclosed by Kimura. An annotated figure (Figure 27C from Kimura) from Section XII.A.1.a can be repeated here to reinforce the point.



Ex. 1004, Fig. 27C (annotations added). This exemplary stage circuit of Kimura's shift register has a first input terminal [wiring 212], second input terminal [wiring 113], third input terminal [wiring 112], and output terminal [wiring 211].

307. Thus, Kimura discloses this claim sub-element of claim element [15-c] of Claim 15 of the '593 patent.

iv. Claim Element [15-c] Summary

308. As just demonstrated, Kimura discloses claim sub-elements [15-c-1], [15-c-2], and [15-c-3] of the '593 patent; thus, Kimura discloses claim element [15-c] of Claim 15 of the '593 patent.

e. Preface to claim elements [15-d] – [15-g]

309. Between claim element [15-c] and claim element [15-d], Claim 15 includes the phrase "wherein each of the stage circuits includes:". It is taken here that this is intended to mean that "includes" is stated with regard to the sequential list claim elements which follow for the remainder of Claim 15 – that is, claim elements [15-d], [15-e], [15-f], and [15-g]. Each of these claim elements will be considered in turn.

f. [15-d]: "an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node,"

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310. This claim element is identical to claim element [1-a] of Claim 1 of the ‘593 patent – which was discussed earlier (in Section XII.A.1.b).

311. Thus, Kimura discloses this claim element of Claim 15 of the ‘593 patent.

g. [15-e]: “a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal, and”

312. This claim element is identical to claim element [1-b] of Claim 1 of the ‘593 patent – which was discussed earlier (in Section XII.A.1.c).

313. Thus, Kimura discloses this claim element of Claim 15 of the ‘593 patent.

h. [15-f]: “a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node, wherein”

314. This claim element is identical to claim element [1-c] of Claim 1 of the ‘593 patent – which was discussed earlier (in Section XII.A.1.d).

315. Thus, Kimura discloses this claim element of Claim 15 of the ‘593 patent.

i. [15-g]: “the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver.”

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316. This claim element is identical to claim element [1-d] of Claim 1 of the ‘593 patent – which was discussed earlier (in Section XII.A.1.e).

317. Thus, Kimura discloses this claim element of Claim 15 of the ‘593 patent.

j. Claim 15 Summary

318. As just shown, Kimura discloses each element of Claim 15 of the ‘593 patent; thus, Kimura renders obvious Claim 15 of the ‘593 patent.

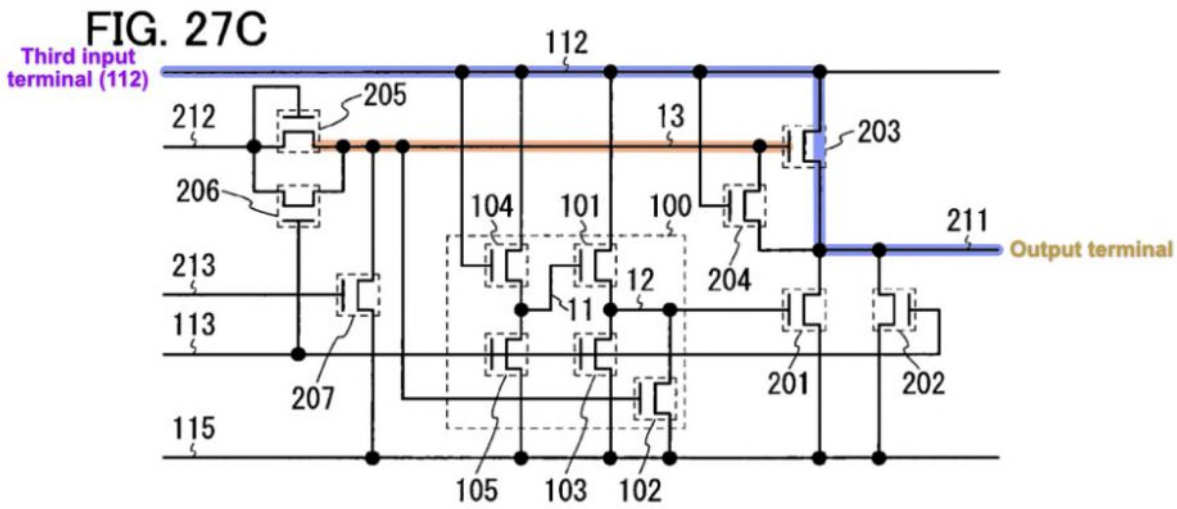
11. Dependent Claim 16

319. As an initial matter, Claim 16 depends from Claim 15; as was shown above, Claim 15 of the ‘593 patent is disclosed by Kimura.

320. Claim 16 further requires “a clock signal supplied to the third input terminal is used as the scan signal.” Kimura discloses this claim of the ‘593 patent.

321. The first part of this claim element (“a clock signal supplied to the third input terminal”) was already discussed earlier (in Section XII.A.1.b.iii) – with respect to claim sub-element [1-a-3] of claim element [1-a] of Claim 1 of the ‘593 patent. An annotated version of Figure 27C of Kimura was provided there for purposes of explanation – and for clarity, that figure will be repeated here.

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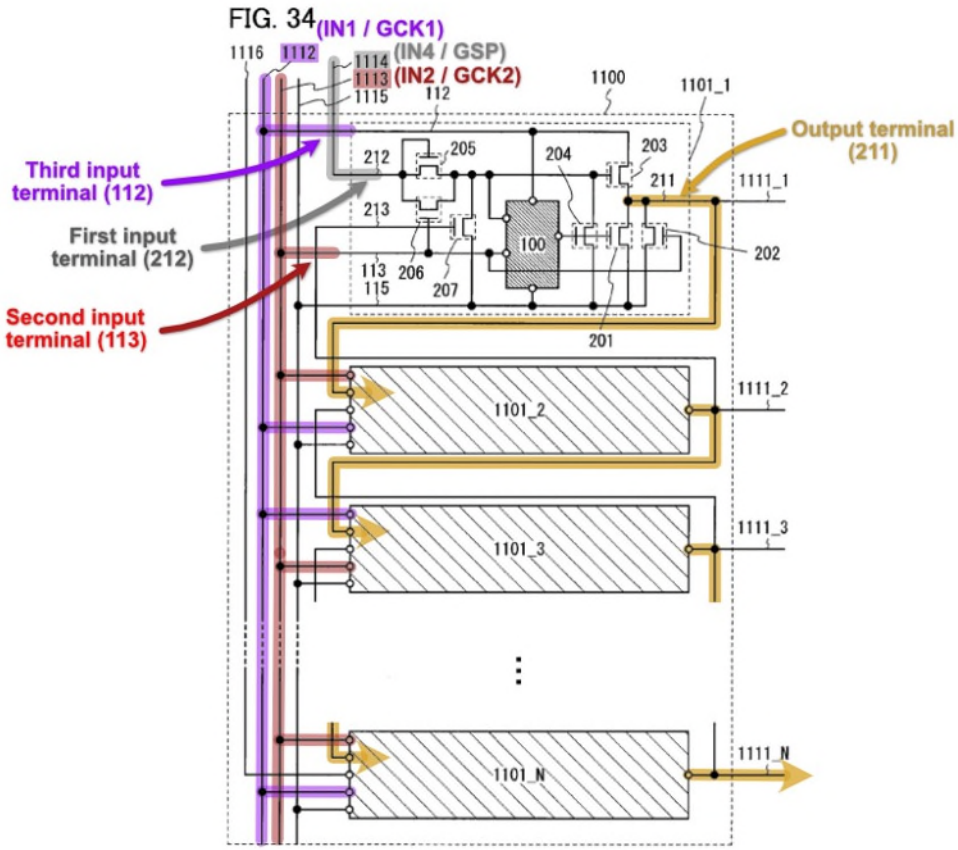
Ex. 1004, Fig. 27C (annotated). As detailed in Section XII.A.1.b.iii, when an appropriate (i.e., turn-on) voltage is applied at the second node (the node labeled 13), transistor 203 will turn on; this will connect the signal of the third input terminal to the node of the output terminal (211) – and thus the signal of the third input terminal is supplied to the output terminal (211).

322. As also discussed earlier (in the evaluation of claim element [1-d], in Section XII.A.1.e) the third input terminal (112) receives a clock signal – since "A signal IN1 is input" to the shift register's "wiring 112" *Id.*, ¶ [0104]; as Kimura describes repeatedly in its various timing diagrams (e.g., Figures 15A – 15C, Figure 17B, Figure 21B, Figure 25B, Figure 31C, and Figure 32B), the signal IN1 is a clock signal – which takes on either a high voltage (i.e., a high logic-level) or a low voltage (i.e., a low logic-level).

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323. Finally, with respect to this clock signal being used as "the scan signal," it was shown above (see the annotated version Figure 27C above) that when transistor 203 is turned on, the input signal that is being applied to the third input terminal (112) is supplied to the output terminal (211).

324. What that signal (at 211) is being used for is made clear via a partial, annotated version of Figure 34 of Kimura:



Id., Fig. 34 (annotations added). As can be seen, the signal at the output terminal 211 is provided to line 1111_1 of the first stage – and 1111_2, 1111_3 … 1111_N of the subsequent stages; these lines (1111_1 – 1111_N) are scan lines, which

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provide scan signals to the pixel array – and thus, the "clock signal applied to the third input terminal is used as the scan signal." In particular, per Kimura, each stage's output signal is employed as a display's "scan signal." *Id.*, ¶ [0324]; Fig. 27C, 34.

325. Thus, Kimura renders obvious this claim of the '593 patent.

12. Dependent Claim 17

326. As an initial matter, Claim 17 depends from Claim 15; as was shown above, Claim 15 of the '593 patent is disclosed by Kimura.

327. Claim 17 further requires that "the first input terminal receives a scan signal of a previous stage circuit or a start signal."

328. This claim is identical to an element of Claim 2 of the '593 patent – which was discussed earlier (in Section XII.A.2).

329. Thus, Kimura renders obvious this claim of the '593 patent.

13. Dependent Claim 18

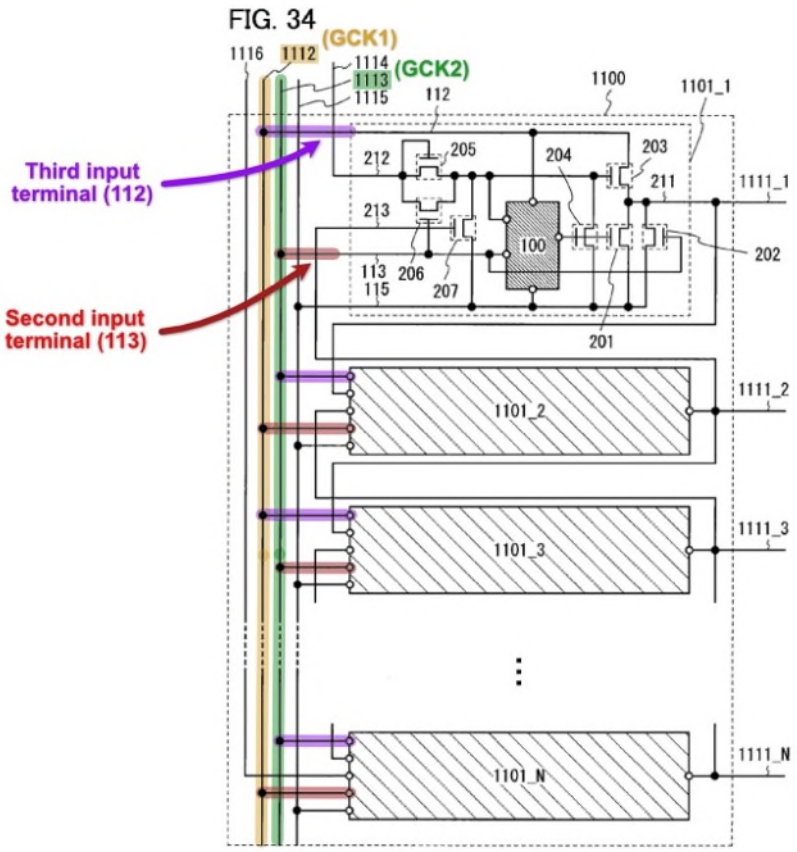
330. As an initial matter, Claim 18 depends from Claim 17, and Claim 17 depends from Claim 15; as was shown above, Claim 15 and Claim 17 of the '593 patent are disclosed by Kimura.

331. Claim 18 further requires "wherein second input terminals of odd stage circuits receive a first clock signal and third input terminals of odd stage circuits receive a second clock signal, and wherein second input terminals of even stage

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circuits receive the second clock signal and third input terminals of even stage circuits receive the first clock signal." In other words, the first clock signal and the second clock signal alternate between the second input terminal and the third terminal along the sequence of stage circuits.

332. First, consider an annotated version of Figure 34 of Kimura:



Ex. 1004, Fig. 34 (annotations added).

333. As shown here, in the odd-numbered stage circuits (*e.g.*, circuits 1101_1, 1101_3, etc.), the second input terminals (wiring 113) receive a first clock signal (GCK2, supplied over wiring 1113) and the third input terminals (wiring 112)

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receive a second clock signal (GCK1, supplied over wiring 1112). As also shown here, the situation with these clock signals and the even-numbered stage circuits (*e.g.*, circuits 1101_2, etc.) is reversed (as compared with the situation with the odd-numbered stage circuits) – with the second input terminals (wiring 113) receiving the second clock signal (GCK1, supplied over wiring 1112) and the third input terminals (wiring 112) receiving the first clock signal (GCK2, supplied over wiring 1113).

334. Kimura explains this operation – stating that in its flip-flop circuits, "in an odd-numbered stage and a flip-flop circuit in an even-numbered stage, portions to which the wiring 112 and the wiring 113 are connected are inversed" *Id.*, ¶ [0335].

335. Thus, Kimura renders obvious this claim of the '593 patent.

14. Dependent Claim 19

336. As an initial matter, Claim 19 depends from Claim 18, which depends from Claim 17, which depends from Claim 15; as was shown above, Claim 15, Claim 17, and Claim 18 of the '593 patent are disclosed by Kimura.

337. Claim 19 further requires that "the first clock signal and the second clock signal have the same period and have phases that do not overlap."

338. This claim is identical to Claim 3 of the '593 patent – which was discussed earlier (in Section XII.A.3).

339. Thus, Kimura renders obvious this claim of the '593 patent.

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15. Dependent Claim 20

340. As an initial matter, Claim 20 depends from Claim 18, which depends from Claim 17, which depends from Claim 15; as was shown above, Claim 15, Claim 17, and Claim 18 of the ’593 patent are disclosed by Kimura.

341. Claim 20 further requires “wherein the first driver includes: a first transistor between the first input terminal and the second node, the first transistor having a gate electrode coupled to the second input terminal; and a second transistor and a third transistor serially positioned between the second node and the first power supply, wherein a gate electrode of the second transistor is coupled to the third input terminal, and wherein a gate electrode of the third transistor is coupled to the first node.”

342. This claim is identical to Claim 6 of the ’593 patent – which was discussed earlier (in Section XII.A.6).

343. Thus, Kimura renders obvious this claim of the ’593 patent.

16. Dependent Claim 21

344. As an initial matter, Claim 21 depends from Claim 18, which depends from Claim 17, which depends from Claim 15; as was shown above, Claim 15, Claim 17, and Claim 18 of the ’593 patent are disclosed by Kimura.

345. Claim 21 further requires “wherein the outputting unit includes: a fourth transistor between the first power supply and the output terminal, the fourth

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transistor having a gate electrode coupled to the first node: a fifth transistor between the output terminal and the third input terminal, the fifth transistor having a gate electrode coupled to the second node: a first capacitor between the second node and the output terminal; and a second capacitor between the first node and the first power supply."

346. This claim is identical to Claim 7 of the '593 patent – which was discussed earlier (in Section XII.A.7).

347. Thus, Kimura renders obvious this claim of the '593 patent.

17. Dependent Claim 22

348. As an initial matter, Claim 22 depends from Claim 18, which depends from Claim 17, which depends from Claim 15; as was shown above, Claim 15, Claim 17, and Claim 18 of the '593 patent are disclosed by Kimura.

349. Claim 22 further requires:

> a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and
>
> a seventh transistor between the first node and a second power supply, the second power supply having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal.

350. This claim is identical to Claim 8 of the '593 patent – which was discussed earlier (in Section XII.A.8).

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351. Thus, Kimura renders obvious this claim of the ’593 patent.

18. Dependent Claim 25

352. As an initial matter, Claim 25 depends from Claim 18, which depends from Claim 17, which depends from Claim 15; as was shown above, Claim 15, Claim 17, and Claim 18 of the ’593 patent are disclosed by Kimura.

353. Claim 25 further requires that “the scan signal of the previous stage circuit or the start signal supplied to the first input terminal overlaps the clock signal supplied to the second input terminal.”

354. Because Claim 25 contains an “or,” it can be satisfied in form of either “the scan signal of the previous stage circuit … overlaps the clock signal supplied to the second input terminal” or “the start signal supplied to the first input terminal overlaps the clock signal supplied to the second input terminal.”

355. The second of these two possible renditions of Claim 25 is nearly-identical to Claim 5 (“… “the start signal is supplied to overlap the first clock signal.”) – which was discussed earlier (in Section XII.A.5).

356. Thus, Kimura renders obvious this claim of the ’593 patent.

B. Ground 2: Shin in Combination with Sasaki Renders Obvious Claims 1-6, 8, 14-20, 22, and 25

362. As will be discussed below, it is my conclusion and opinion that, when viewed and considered in light of the knowledge possessed by a POSITA, Claims 1-

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6, 8, 14-20, 22, and 25 of the ’593 patent are rendered obvious by Shin in combination with Sasaki.

1. Motivation to Combine Shin with Sasaki

363. As will be discussed here, Shin and Sasaki are within the scope of the prior art, are closely-related to each other within that scope, and are highly relevant to the patentability of the ’593 patent’s claims. Further, when viewed and considered in light of the knowledge possessed by a POSITA, the combination of Shin and Sasaki together disclose all the limitations of and render claims 1-6, 8, 14-20, 22, and 25 of the ’593 patent obvious. As will also be discussed here, a POSITA reviewing the prior art would have been motivated to combine Shin and Sasaki – to address deficiencies in the circuitry disclosed by Shin, by adding circuitry disclosed by Sasaki to the circuitry of Shin.

364. With regard to Shin, Shin relates to a “scan driving circuit” for an “organic light emitting display.” Ex. 1005, ¶ [0003]. According to Shin, prior art circuit designs allow significant “static current flows,” which results in undesirable “excessive power consumption.” *Id.*, ¶¶ [0012]-[0015]. The prior art circuitry that is shown in Figure 2 of Shin provides an example of this – as in this circuitry, each stage includes four potential current flow pathways from VDD to ground that may be active during device operation. *Id.*, Figs. 2-3. (In more detail with regard to Figure 2 of Shin, the prior art circuitry described here involves four inverters – where

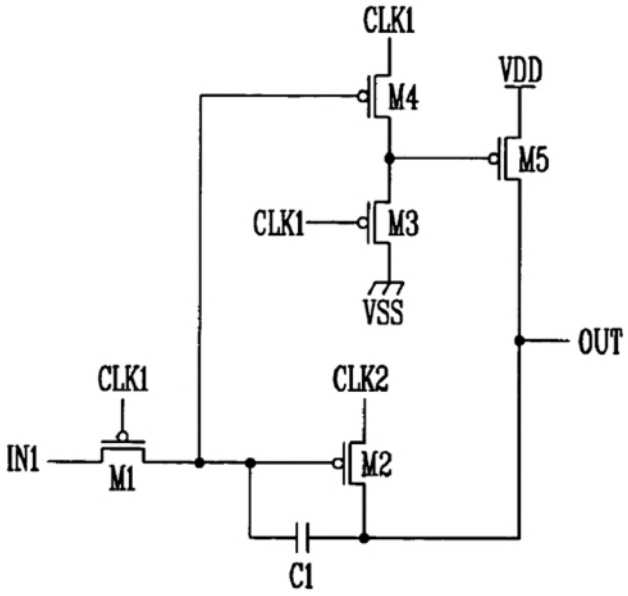
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an inset figure to the right provides a transistor-level (rather than logic-level) depiction of this circuit element; this configuration is what is well-known in the art as being a PMOS inverter, where the transistor M2 (which uses a diode-connected configuration) provides the "load" device of the inverter. It has long been known in the art that PMOS logic circuitry (like its better-known cousin, NMOS logic circuitry) requires a bias current to be flowing through the circuit (from VDD to ground) even when no switching logic operations are occurring – and thus this inverter circuit will be consuming power even when it is, in essence, not doing anything.[20])

365. To address this, Shin proposes a "scan driving circuit" design that "remov[es] a current flow path of a static current from a stage of each unit." Id., ¶ [0016]. Shin provides an example of improved circuitry to address problem in the embodiment disclosed in Figure 11 of Shin:

[20] One of the key reasons that, in mainstream silicon technology, CMOS logic technology replaced NMOS logic technology (nearly 40 years ago) is because NMOS logic circuits consume power even when not engaging in switching operations, while CMOS logic circuits consume power only when engaging in switching operations (and consume nearly no power when such operations are not occurring).

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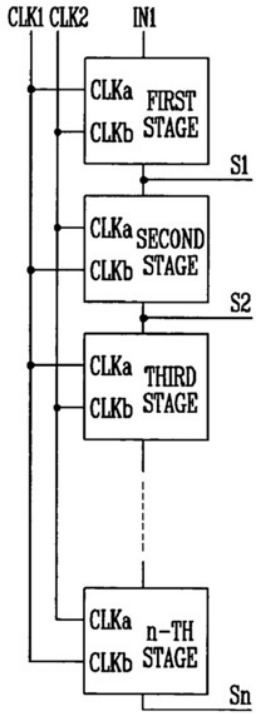


Ex. 1005, Fig. 11. Unlike the prior art circuit that Shin describes in Figure 2, this circuit does not have the PMOS logic inverters that are used in the circuitry of Figure 2 – inverters, which, as detailed above, have an active bias current even when the logic circuitry is inactive (i.e., not engaging in any logic switching events); as that prior art circuity as four such inverters in its architecture, the use of the circuit of Figure 11 does not have the four potential bias current paths from VDD to ground. *See id.*

366. This circuitry provides the same functionality – functioning as a scan driving circuit. According to Shin, the circuit's transistors are turned on or off by the start signal IN1 and the clock signals CLK1 and CLK2 – for purposes of supplying either a "high" or a "low" signal to OUT. *See id.*, ¶¶ [0075], [0099]-[0107]; Fig. 12.

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367. As Shin indicates, a series of such circuits is arranged one after another in a cascade of stages – so as to supply signals to a display's scan lines. This is shown below in Figure 10 (which has been excerpted to focus on the portion of the circuit responsible for generating scan signals):



Id., Fig. 10 (excerpted); *see also* Fig. 4.

368. While Shin's circuitry (described above) is clearly beneficial due to its reduced power consumption (as would have been recognized by a POSITA), it is subject to a potential problem (as would also have been recognized by a POSITA). That is, there is a potential deficiency in this stage circuit of Shin because the node at the gate of M2 could be subject to reversal.

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369. This, however, would have been known in the art, as it was considered (and highlighted) by Sasaki (Ex. 1014).

370. First, it should be briefly noted that, like Shin, Sasaki involves a "shift register" circuit for use with a "display device." Ex. 1014, ¶ [0003].

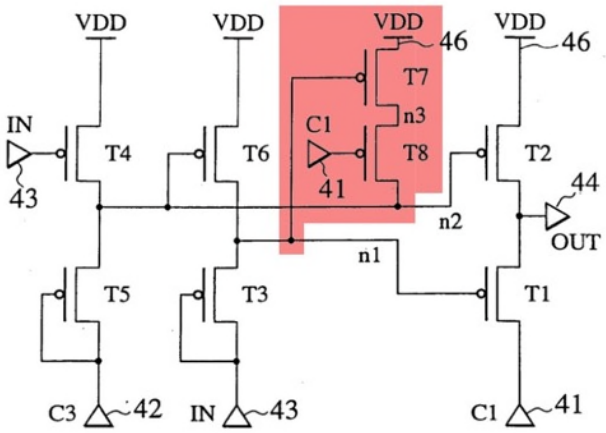
371. Returning to the issue of the potential problem of reversal in the circuitry of Shin, Sasaki's disclosed circuitry includes "transistors" with gates connected to a "control electrode." *Id.*, ¶ [0011]. In the conventional way, this allows the circuit to apply either a logical high or logical low signal to an output terminal. *See id.*, Fig. 4.

372. As Sasaki explains, if either transistor's "control electrode" enters a "floating state" because "the high voltage VDD is not supplied," it is possible that the transistor may be "reversed" (*i.e.*, turned on when it is supposed to be turned off). *Id.*, ¶ [0042]. This can in turn cause an unwanted (particularly in terms of circuit functionality) mixing of high and low signals at the output terminal. *Id.*

373. To address this problem, Sasaki employs an "anti-reversal circuit." *Id.*, ¶ [0042]; Figure 4 provides an example of this "anti-reversal circuit":

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FIG.4



Id., Fig. 4 (annotated).

As Sasaki explains, "The anti-reversal circuit includes a seventh transistor T7 and an eighth transistor T8." *Id.*, ¶ [0042].

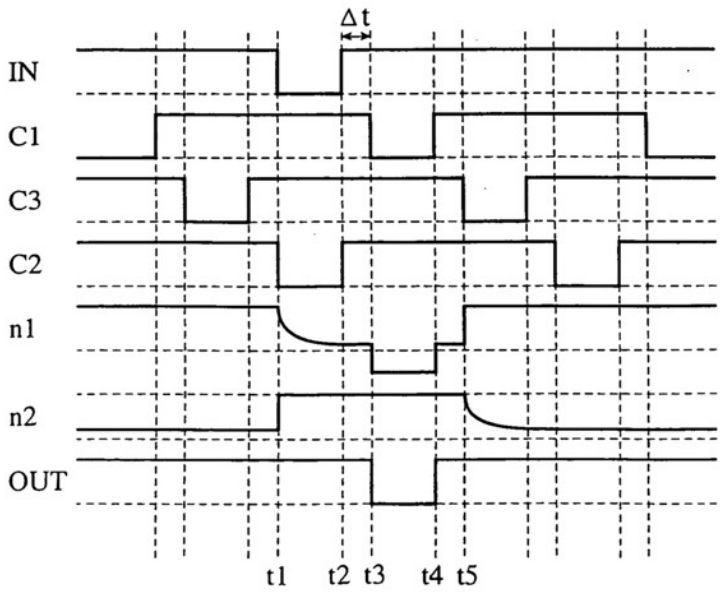
374. The two transistors of the anti-reversal circuit (T7 and T8) are operated so as to keep transistor T2 off – by supplying a high VDD signal to transistor T2's gate when transistor T1 is on and the signal input C1 is supplying a low signal to OUT; this ensures that the high VDD signal is not inadvertently supplied to OUT along with the low signal.

375. The paragraphs below will provide further details regarding the operation and effects of Sasaki's anti-reversal circuit.

376. Figure 5 is a timing diagram which shows when logic-high and logic-low signals are applied to the various input terminals of Sasaki's circuitry:

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FIG.5



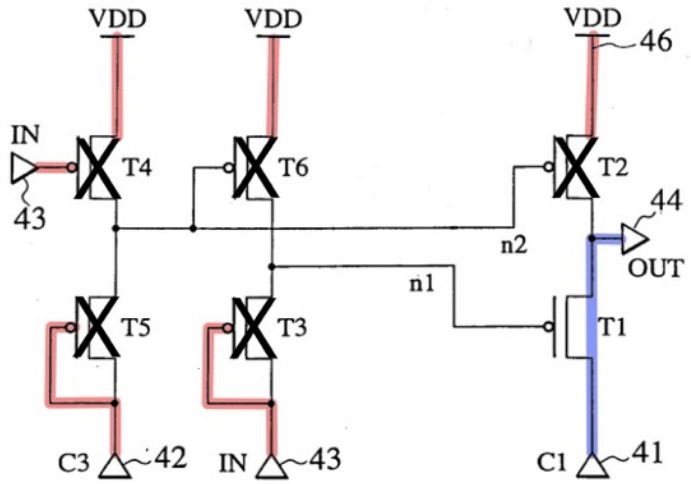
Id., Fig. 5.

377. Further, Sasaki employs p-type transistors – which are turned on by logical low signals (blue below) and turned off by logical high signals (red below).

378. The anti-reversal circuit operates in a manner which ensures that a low signal is supplied to OUT in time period t3-t4. If the anti-reversal circuit were not present—as shown in the modified version of Figure 4 below, where the two transistors of the anti-reversal circuitry are not present—the gate of transistor T2 gate would be have a high signal, which would thus turn transistor T2 off; however, this gate will be subject to a floating potential (provided by the voltage present on node n2) during this period – creating the possibility of reversal, which would improperly supply the high signal from VDD to OUT:

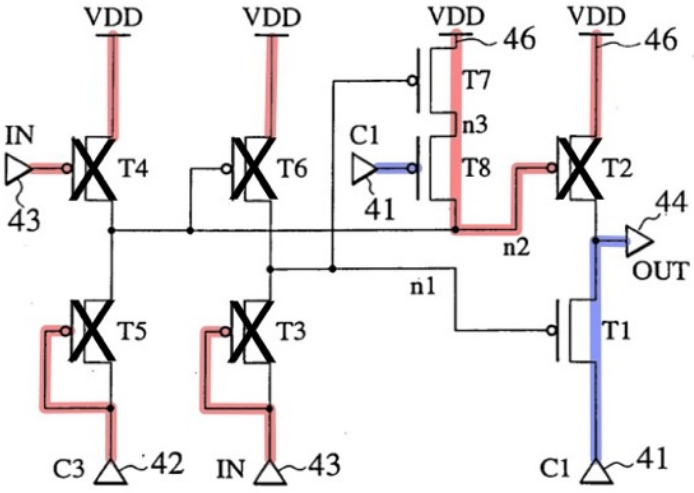
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FIG.4



Id., Fig. 4 (annotated). Transistors T7 and T8 serve to avoid this scenario – by passing a high VDD signal to the gate of transistor T2 during this period, to ensure that transistor T2 stays turned-off:

FIG.4



Id., Fig. 4 (annotated).

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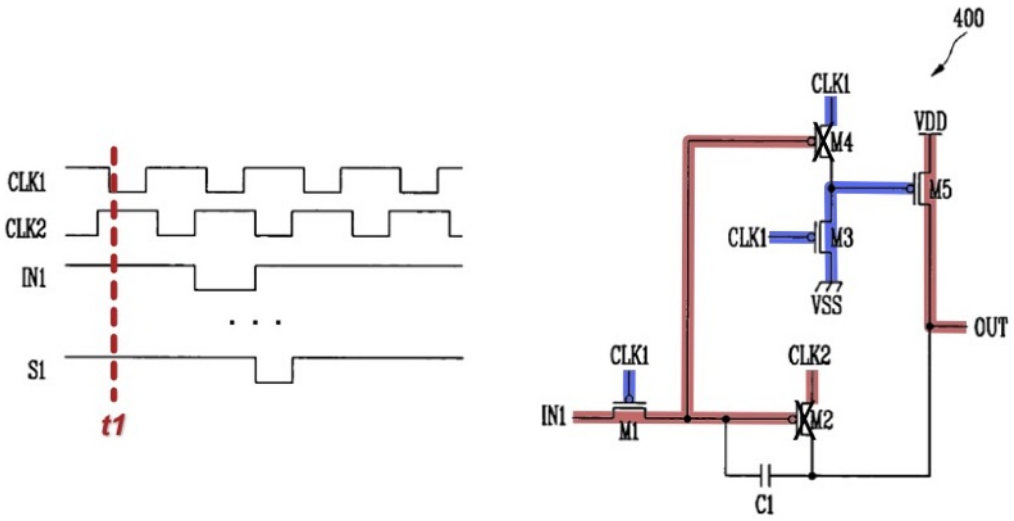
379. As noted above, this is a known problem in the art, and one that would have been obvious upon examination of the circuitry of Shin; further, it is also obvious that Sasaki's circuitry addresses this deficiency in Shin. All of this would be known to a POSITA – and thus, a POSITA would have motivated to combine the circuitry of Shin with circuitry like that exemplified by Sasaki, for the purpose of addressing this problem.

380. The discussion and figures below—created using the timing diagram of Figure 12 of Shin and the circuit diagram of Figure 11 of Shin—provide an example.

381. Shin employs p-type transistors that are turned on by low voltages (again blue) and turned off by high voltages (again red).

382. In the period ***t1***, CLK1 is low, causing transistors M1, M3, and M5 turn on. CLK2 is high, and IN1 is also high – thus turning off transistor M2. A high signal is supplied to OUT from VDD:

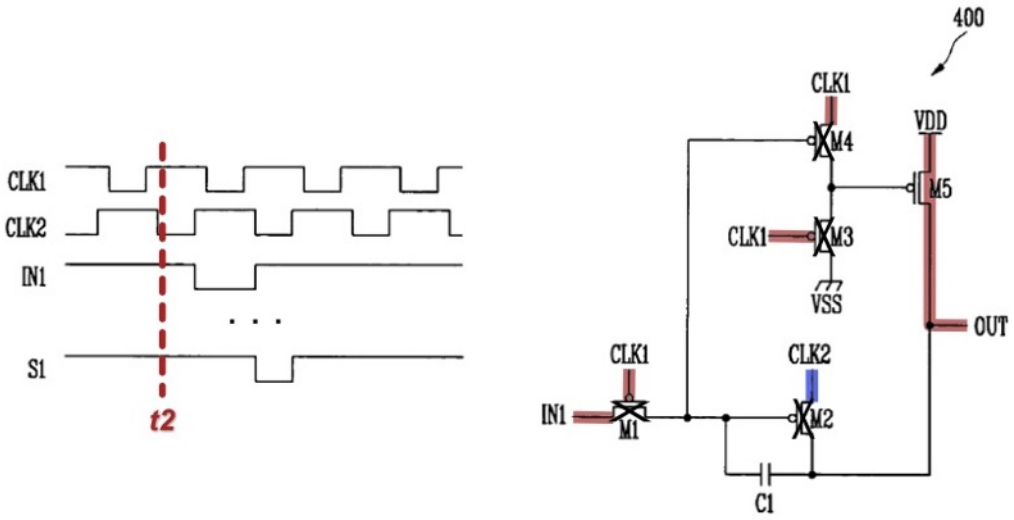
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Id., Figs. 11, 12 (excerpted). As shown, the transistor M2 is turned off by an applied signal; however, as transistor M1 is turned on and is thus connected to the gate of transistor M2, the node that includes the gate of transistor M2 does not have a floating potential.

383. This changes in period ***t2***. Here, CLK1 is high and CLK2 is low – and thus, transistors M1 and M3 – which in the previous period were turned on – are now turned off. Transistor M5 remains turned on, and a high signal continues to be supplied to OUT from VDD:

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Id., Figs. 11, 12 (excerpted).

384. For OUT to be high as intended, however, transistor M2 must remain turned off - as otherwise, a low signal CLK2 will also be supplied to OUT. However, the line leading to the gate of transistor M2 gate is now electrically isolated (i.e., this node is now floating). This creates the possibility of a reversal event; noise (due to, for example electromagnetic interference (EMI), or due to crosstalk from other nearby digital switching events) could result in spurious signals on this floating node - which could, in turn, cause the transistor M2 to inadvertently turn on.

385. It can be noted that while Shin includes a capacitor (C1) that is connected to the gate of transistor M2, this capacitor will not provide adequate anti-reversal protection. This is because in steps subsequent to those described above, this capacitor's charge state is set to a low logic voltage level – which serves to keep transistor M2 turned on after the low-level signal ceases (as this voltage remains on

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the capacitor, as it is connected to a floating node). *See* Ex. 1005, ¶ [0102]. However, in period ***t2***, the capacitor has only been subject to high-level signals, rendering it unable to fully guarantee reversal protection. Moreover, the transition of CLK2 to low in this time period will result in the lowering of the voltage at the gate of transistor M2 - which further minimizes the effect of the capacitor.

386. Indeed, numerous prior art references employ ***both*** capacitors and transistors to control a node voltage. *See, e.g.*, Ex. 1016, Fig. 1A (capacitors 233-234 and transistors 226-227 are all connected to and operate to control the potential of node N226); Ex. 1004, ¶¶ [0286], [0302]-[0303] (both a "transistor 204" and "capacitor 220" control the voltage of node 13).

387. As described in Section IX.C, Sasaki noted that a circuit of this type can be vulnerable to a "reversal" – a problem which Sasaki explicitly identifies for remediation by his disclosed invention(s), in the Abstract:

> In this way, a floating state of the node n2 is avoided, and the voltage level of the node n2 is prevented from being reversed.

Ex. 1014, Abstract.

388. It was for this reason that Sasaki introduced the "anti-reversal circuit" – which is described in both the text of the specification and in the figures.

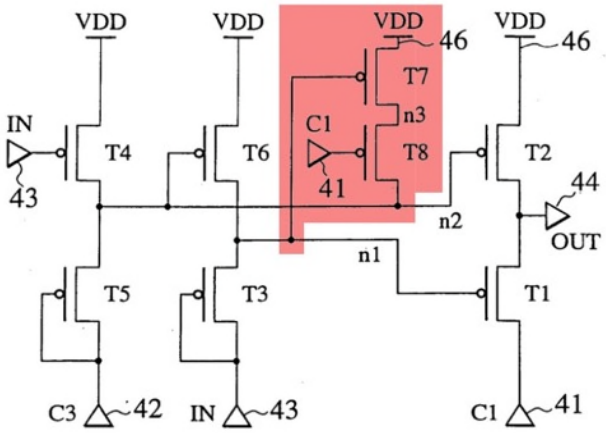
> The anti-reversal circuit prevents a voltage level at the control electrode of the second transistor T2 from being reversed, which is attributable to a floating state of the control electrode of the second transistor T2, where if a

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> voltage level of the first clock signal C1 is reversed in the state where the first transistor T1 is turned on and the second transistor T2 is turned off.

Id., ¶ [0042].

FIG.4



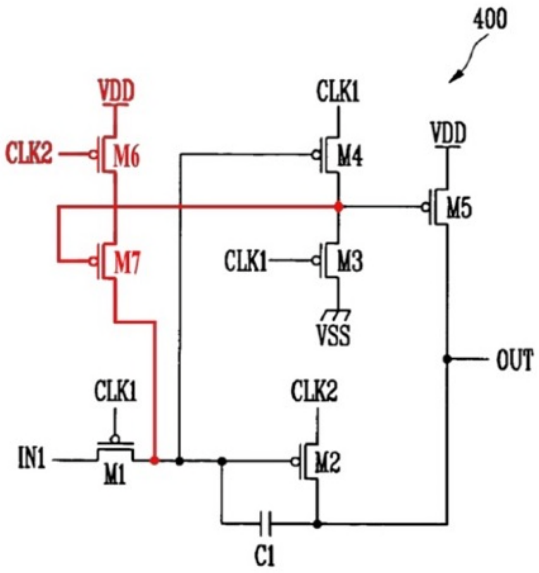
Id., Fig. 4 (annotations added). As was explained earlier, this circuitry was added by Sasaki to make sure that the node is at the expected value before the control sequence stops; without this connection to reset the node, there is a risk that the voltage will be "reversed" from the expected value during the control sequence.

389. The node at the gate of transistor M2 in Shin is subject to this sort of reversal due to fluctuations in the timing and operation of signal CLK2. As will be shown below, in Shin's Figure 11 circuit, there is no way to independently set the node connected to the gate of transistor M2 to a high voltage, so as to ensure that M2 is not turned on unexpectedly. In particular, the operation of the circuit would be disrupted if M2 were to be turned on at a time when CLK2 was low and M5 was intended to be on (so as to provide a high-signal, VDD, to the output). This would

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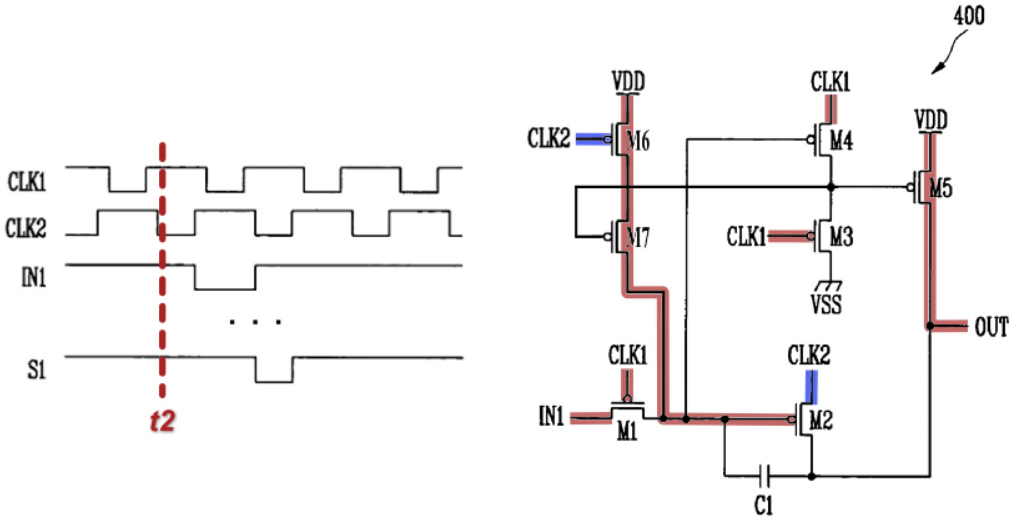
result in conflicting signals on the output – between VDD and a low CLK2. Sasaki's anti-reversal circuit mitigates this specific problem – by connecting the node that might be reversed directly to VDD, through two transistors, where one is controlled by the other node of the output unit and the other is connected to the conflicting input. Thus, Sasaki provides a simple logic circuit that uses the other output node and the input to that other node – and thus provides circuitry that ameliorates the possibility of conflicting outputs.

390. Thus, as these items were known in the art at the time of the '593 patent, a POSITA would have been motivated to remedy the aforementioned deficiency in Shin – by adding Sasaki's anti-reversal circuit to the Figure 11 stage circuit embodiment of Shin. The resulting combined embodiment is readily-assembled, with the following result:



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In the above circuitry, if the gate of M2 is guaranteed (by the added circuitry) to *not* inadvertently go low at a point when the output should be VDD (because if a low value is provided by CLK2, the upper transistor of the anti-reversal circuit will be on – and if M5 is also on at that point, the lower transistor of the anti-reversal circuit will also be on), then this ensures that the node at the gate of M2 is at a high voltage (VDD), and that the low side value of signal CLK2 cannot reach the output. This is shown below:



Other than the application of a high signal to keep transistor M2 turned off during period ***t2***, the rest of Shin's operation remains the same. Further, Sasaki's example *does* employ an anti-reversal circuit – to keep Sasaki's transistor T2 from turning on and inadvertently supplying a high VDD signal to OUT at a time when capacitor C1 is supplying a low signal. *See* Ex. 1014, Fig. 4. However, as already explained, transistor reversal was a well-known issue in the prior art – and as an issue that could occur with different transistors. Because of this, a POSITA would not regard the

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use of an anti-reversal circuit (like that shown in Sasaki) to be limited to just Sasaki's specific example. Further, a POSITA would have understood that Sasaki's anti-reversal circuit is not necessary to keep Shin's transistor M5 turned off. When a low CLK2 signal is supplied to OUT through transistor M2, transistor M5's gate is not floating – but is instead provided with an off signal via a high CLK1 signal applied through transistor M4. *See* Ex. 1005, Figs. 10, 11.

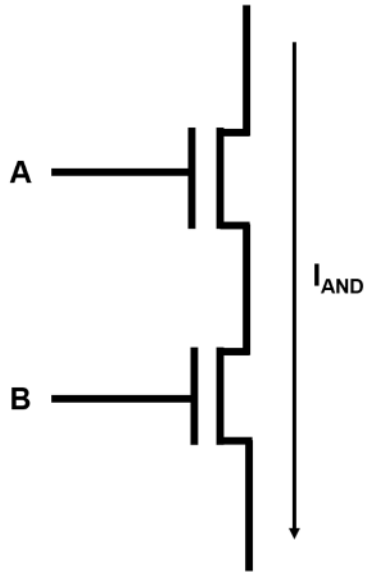
391. A view of the prior art generally reveals that Sasaki's teaching was well-known and obvious – as will be noted in more detail below. Sasaki's anti-reversal circuit consists of two transistors in series – with the gates of the two transistors connected to separate input lines, and no circuit use made of the node between the two transistors in the series configuration. While a configuration of two transistors[21] in series is well-known in the art and can be (and is) used for a wide variety of purposes[22], the particular configuration used in Sasaki's anti-reversal

[21] This configuration was also well-known and commonly used in electronic devices that were precursors to the transistor – such as the vacuum-tube triode and even the relay.

[22] See, for example, J. Miller, "Dependence of the input impedance of a three-electrode vacuum tube upon the load in the plate circuit," Scientific Papers of the Bureau of Standards, 15(351):367–385, 1920 (Ex. 1022) this paper predates the 1947 invention of the transistor, and discusses an application of two vacuum-tube triodes

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circuit provides what amounts to an AND logic functionality – that is, *both* transistors must be turned on for a current to flow through the two transistors.



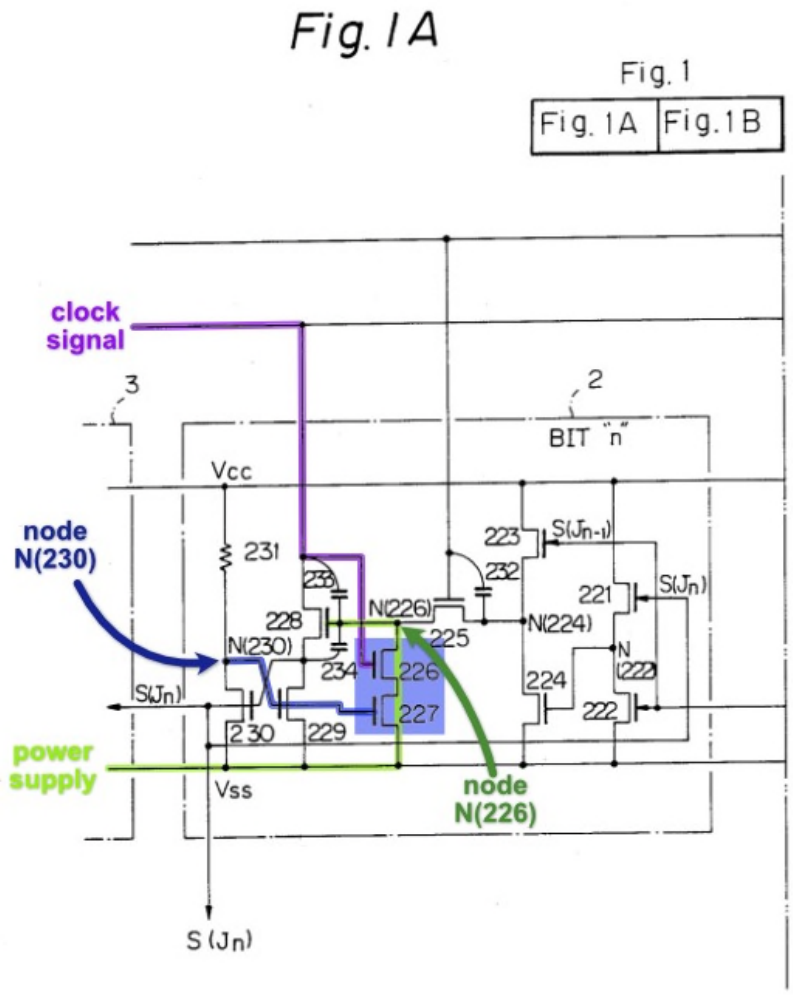
As can readily be seen by inspection, the current I_{AND} will flow only when both transistors have been turned on – by the provision of "on" logic-state signals to the gates of both transistors of the circuit.

392. Numerous instances of circuitry of this type can be found in the art – including in the patent art. For example, U.S. Patent No. 4,720,815 to Ogawa ("Ogawa", Ex. 1016), discloses circuitry of this type, as shown in Figs. 1A and 1B:

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in series – in a manner that is now widely-used in particular types of transistor-based circuits (where "cascoding" is used.)

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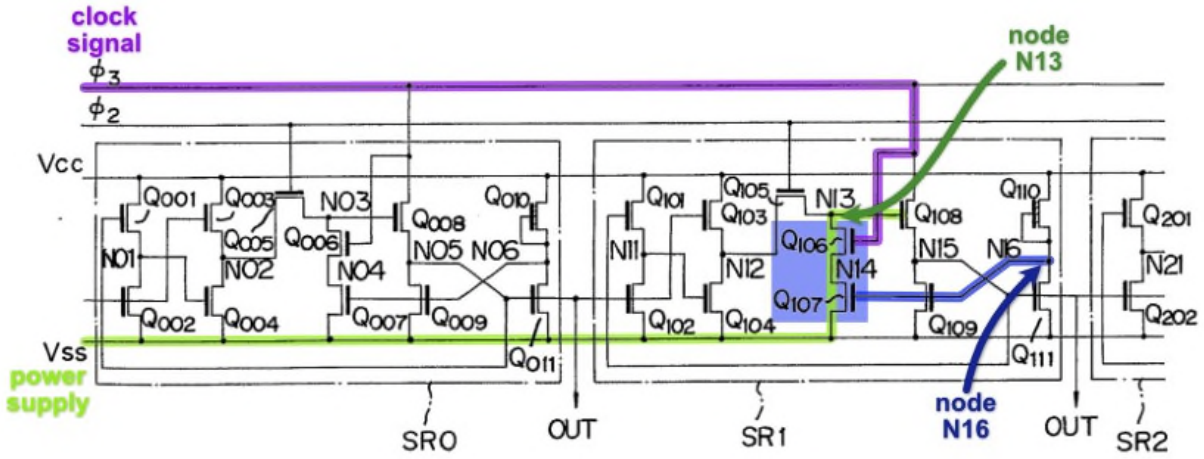


Ex. 1016, Figs. 1A and 1B (annotations added). The circuitry annotated with a blue box is the same as that described just above – where two transistors in series, with their gates connected to different input lines, provide an AND functionality; in this particular case, when (and only when) both transistors 226 and 227 are turned on, a current will flow through the circuitry. (Ogawa also happens to disclose the use of this circuitry in the stage circuits of a shift register; thus, a POSITA familiar with shift-register art – or studying/reviewing it – would be even more likely to know about this circuitry or to find it.)

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393. Ex. 1017 (the Takemae reference) is yet another example teaching a "shift register" with serially arranged transistors Q_{106}-Q_{107} for controlling node N13's potential. Ex. 1017, Abstract, 7:26-35, Fig. 6. More particularly, in this reference's shift register, the voltage of node N13—and thus the gate of transistor Q_{108} attached to the node— can be set by passing a signal through transistor Q_{105}. *See id.* In addition, the node voltage can be further controlled by in-series transistors Q_{106} and Q_{107}, which are located between power supply Vss and node N13. *See id.* Transistor Q_{106} is controlled by clock signal Ø3, while transistor Q_{107} receives a signal from another node N16. *See id.* Thus, the transistors operate to "reset" the "output" to "node N13." *Id.* This is shown below:

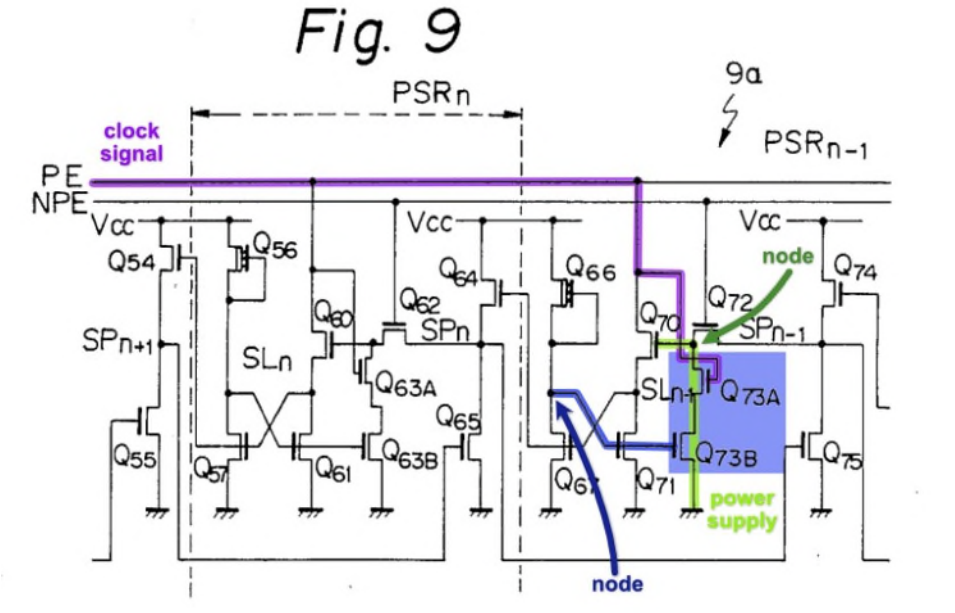
Fig. 6



Id., Fig. 6.

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394. Ex. 1018 (another Ogawa reference) provides one more example. Here, a circuit employs in-series transistors Q_{73A}-Q_{73B} to control the potential of a node leading to transistor Q_{70}. *Id.*, 5:11-17; Fig. 9. The node leading to transistor Q_{70} can be controlled by the signal passing through transistor Q_{72}. *See id.*, 4:49-5:10. Alternatively, the node can be controlled by transistors Q_{73A} and Q_{73B}, which supply a low power supply voltage or ground to the node at certain times. *Id.*, 5:11-17. Transistor Q_{73A} receives "pulse PE," which can be a "clock pulse signal." *Id.*, 4:46-50, Fig. 9. Transistor Q_{73B} receives a signal from another node located between transistors Q_{66} and Q_{67}. *See id.*, Fig. 9. In operation, "transistors Q_{73A} and Q_{73B} prevent the application of" a "high voltage to the gate of the transistor Q_{70}" when this is not intended. *Id.*, 5:11-17. This is shown below:



Id., Fig. 9.

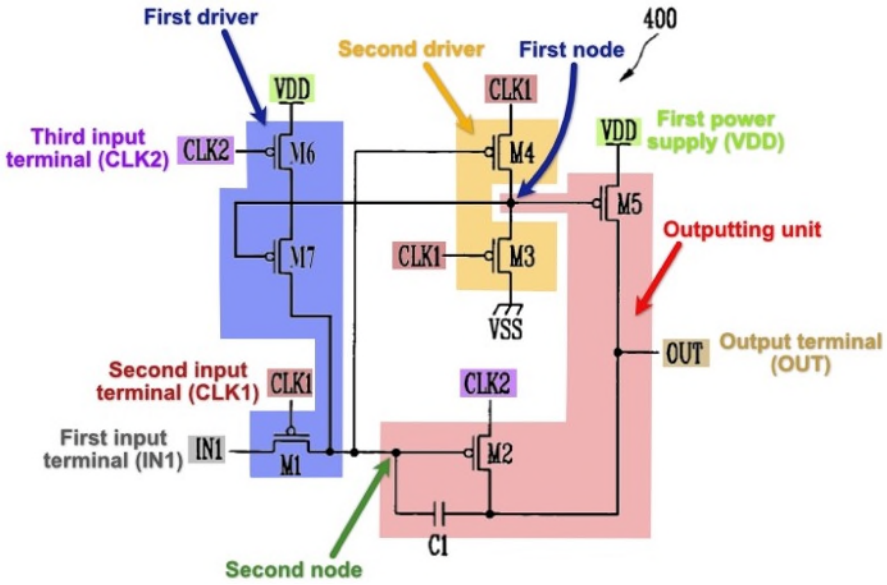
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395. As indicated above, numerous other references in the patent art describe circuitry and functionality of this type; this included (but certainly are not limited to) US Patent Publication No. 2007/0085808A1 (Ex. 1023) at Fig. 4 and US Patent Publication No. 2009/0115792A1 (Ex. 1024) at Fig. 29.

396. Together, these references confirm—just as Sasaki teaches—that it was well-known, routine, and commonplace to integrate transistors that operate as a logical AND, including for purposes of controlling a node's potential by connecting a power supply to the node at a particular time based on signals supplied to the transistors' gates, including (1) a clock signal and (2) a signal from another node. This would have further motivated the use of such a circuit element with Shin, and provided a POSITA with a more than reasonable expectation of success.

397. Finally, before beginning a discussion of the claim-by-claim analysis, it will be helpful to first provide an annotated version of the combined embodiment of Shin's Figure 11 embodiment with Sasaki's anti-reversal circuit – with the annotations indicating the identification of the specific structures recited in the claims of the '593 patent, as mapped to the combined embodiment:

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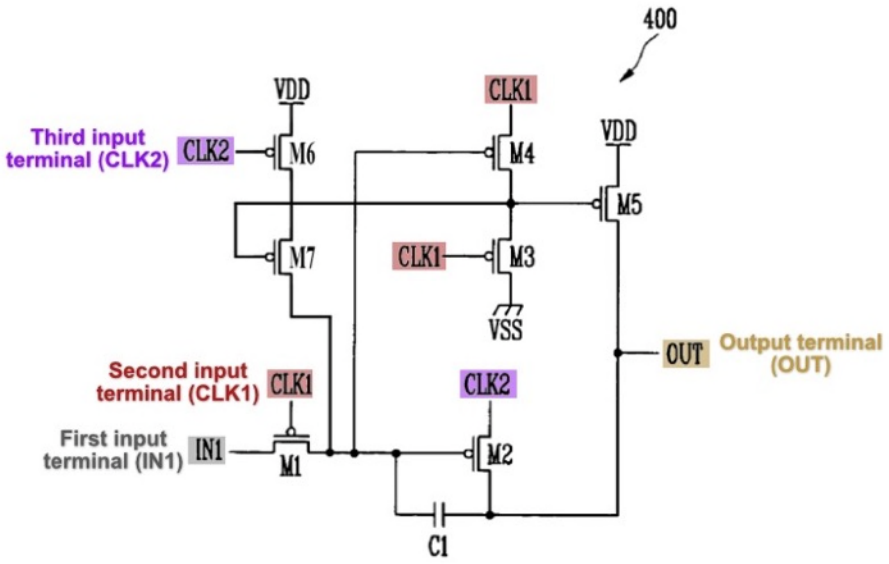
2. Independent Claim 1

398. It is my conclusion and opinion that Claim 1 of the ‘593 patent is rendered obvious by Shin in combination with Sasaki, in view of the knowledge of a POSITA.

a. [1-pre]: “A stage circuit having a first input terminal, a second input terminal, a third input terminal, and an output terminal, the stage circuit comprising:”

399. To the extent that the preamble is limiting, Shin in combination with Sasaki discloses the preamble of Claim 1 of the ’593 patent; this can be seen readily via an annotated version of the combined embodiment of Shin and Sasaki:

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As can be seen in this annotated figure, Shin in combination with Sasaki discloses a first input terminal, a second input terminal, a third input terminal, and an output terminal – all of which are part of a stage circuit.

400. In more detail, according to Shin, the above circuit operates as a stage of a "scan driv[er]" for a "display." Ex. 1005, ¶ [0003]. As shown above, each "stage[]" includes a terminal that "receive[s]" a "first input signal IN1" (the first input terminal), along with "first clock terminal CLKa" (the second input terminal) and "second clock terminal CLKb" (the third input terminal) that respectively receive "first and second clock signals CLK1 and CLK2." *Id.*, ¶¶ [0072]-[0075], [0088]-[0090].

401. Further, an "output line" from each "stage[]" of the "scan drive unit" "provide[s] a selection signal to respective pixels defining" a display's "pixel array."

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Id., ¶¶ [0070], [0072]. This selection signal is generated on "the output line OUT" (the output terminal). *Id.*, ¶ [0089].

402. Thus, Shin in combination with Sasaki discloses the preamble of Claim 1 of the '593 patent.

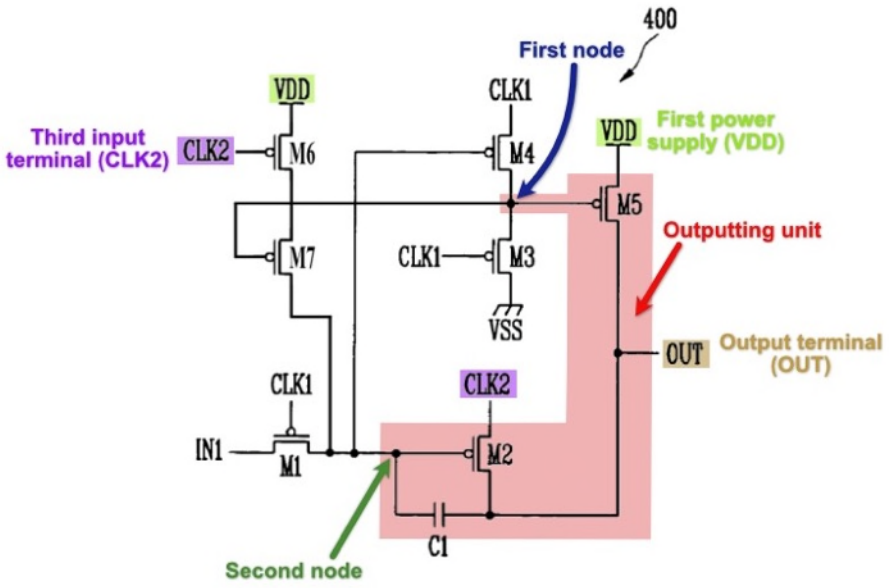
b. [1-a]: "an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node:"

403. Claim element [1-a] is rather long – and thus the analysis will be simpler to explain if this claim element is broken up into sub-elements.

i. [1-a-1]: "an outputting unit having a first node and a second node,"

404. Shin in combination with Sasaki discloses this claim sub-element; this is evident via an annotated version of the combined embodiment presented above:

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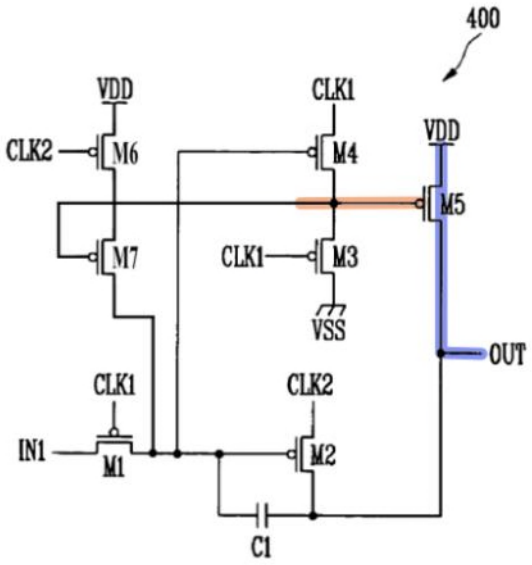
The red boxing identifies the outputting unit, while first node is noted in blue and the second node is noted in green.

405. Thus, Shin in combination with Sasaki discloses this claim sub-element of this claim element of Claim 1 of the ’593 patent.

ii. [1-a-2]: “the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node”

406. Shin in combination with Sasaki discloses this claim sub-element; this is evident via an annotated version of the combined embodiment presented above:

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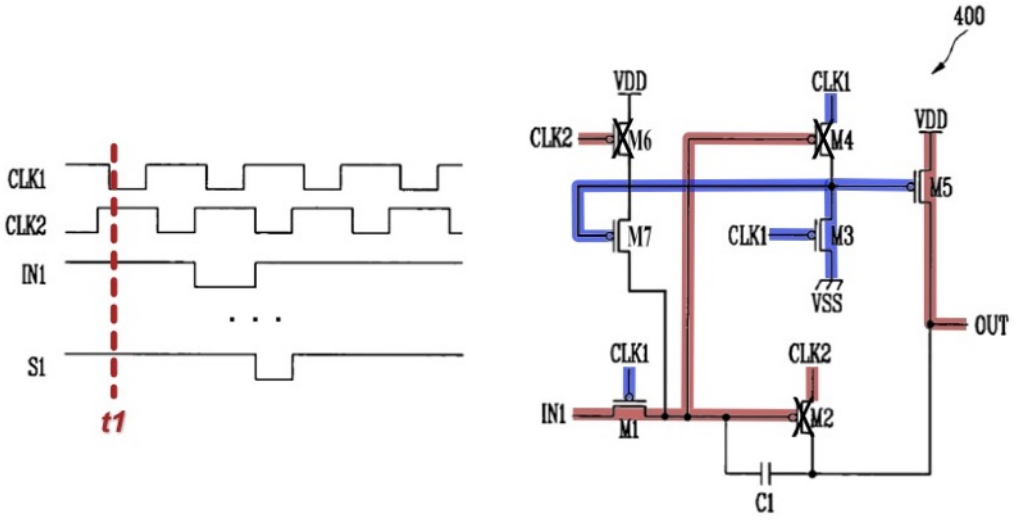


As the annotations show, when an appropriate (i.e., turn-on) voltage is applied at the first node, transistor M5 will turn on; this will connect the first power supply voltage (VDD) to the node of the output terminal ("OUT") – and thus the voltage of the first power supply connection (VDD) is supplied to the output terminal ("OUT"). (On the other hand, when a turn-on voltage is not applied at the first node, transistor M5 will not turn on – and the voltage of the first power supply connection (VDD) is not supplied to the output terminal.)

407. In more detail, Shin explains that in each shift register stage, "PMOS transistor M5 is coupled between a first power supply VDD and the output line OUT." Ex. 1005, ¶ [0089]. Its gate is connected to a "first node N1" (the first node) located between transistors M3 and M4. *Id.* In operation, transistor M5 allows the stage to provide the first power supply voltage (i.e., VDD) to OUT. *See id.*, ¶ [0075].

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408. More particularly, during a "precharge period," input and clock signals are provided such that "first node N1" is supplied with a "low-level signal" opening transistor M5 allowing "first power supply VDD of a high level" to be "output through an output terminal OUT." *Id.*, ¶ [0099]. This is shown below:

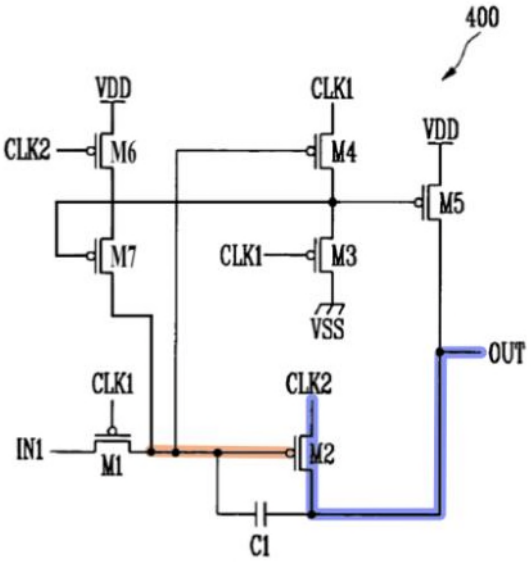


409. Thus, Shin in combination with Sasaki discloses this claim sub-element of this claim element of Claim 1 of the '593 patent.

iii. [1-a-3]: "and a signal of the third input terminal to the output terminal according to a voltage applied to the second node:"

410. Shin in combination with Sasaki discloses this claim sub-element; this is evident via an annotated version of the combined embodiment presented above:

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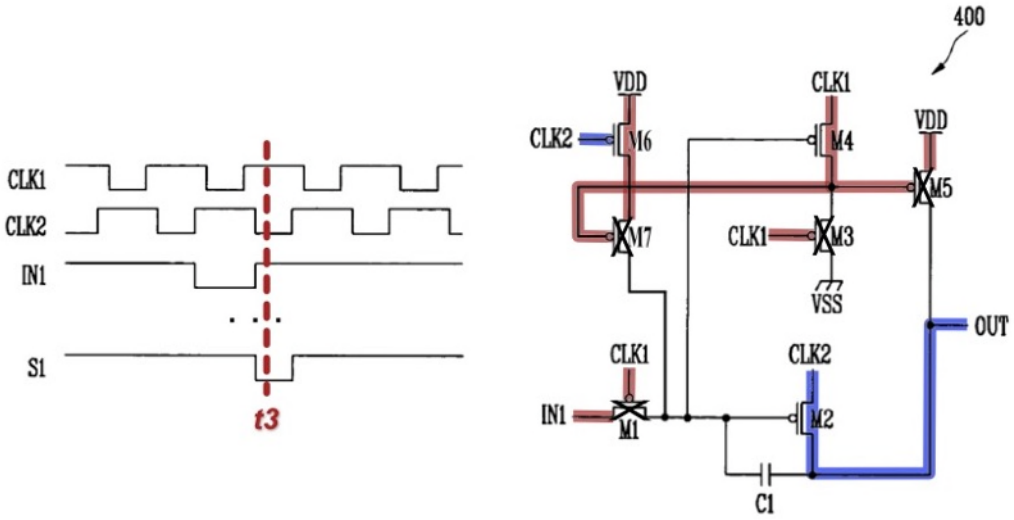
As the annotations show, when an appropriate (i.e., turn-on) voltage is applied at the second node, transistor M2 will turn on; this will connect the signal of the third input terminal ("CLK2") to the node of the output terminal ("OUT") – and thus the signal of the third input terminal ("CLK2") is supplied to the output terminal ("OUT"). (On the other hand, when a turn-on voltage is not applied at the second node, transistor M2 will not turn on – and thus the signal of the third input terminal (CLK2) is not supplied to the output terminal ("OUT").)

411. In more detail, Shin explains that in each shift register stage, a "PMOS transistor M2 is coupled with a second clock terminal" receiving CLK2 (Shin's third output terminal) "and an output line OUT" (the output terminal). Ex. 1005, ¶ [0088]. This transistor's gate is coupled to a point where lines leading to or from the output of transistor M1, capacitor C1, and the gate of transistor M4 intersect (i.e., Shin's

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second node). *Id.* In operation, transistor M2 allows the stage to provide the signal of the third input terminal (CLK2) to OUT. *See id.*, ¶ [0075].

412. More particularly, during an "evaluation period," signals are supplied to turn off transistors M1, M3, M5, and M7. *Id.*, ¶¶ [0099]-[0107]. Capacitor C1 allows "transistor M2" to maintain an open state allowing the "stage [to] output[] a low-level" CLK2 "signal." *Id.*, ¶¶ [0103], [0105]; *see also id.*, Fig. 12. This is shown below:



413. Thus, Shin in combination with Sasaki discloses this claim sub-element of this claim element of Claim 1 of the '593 patent.

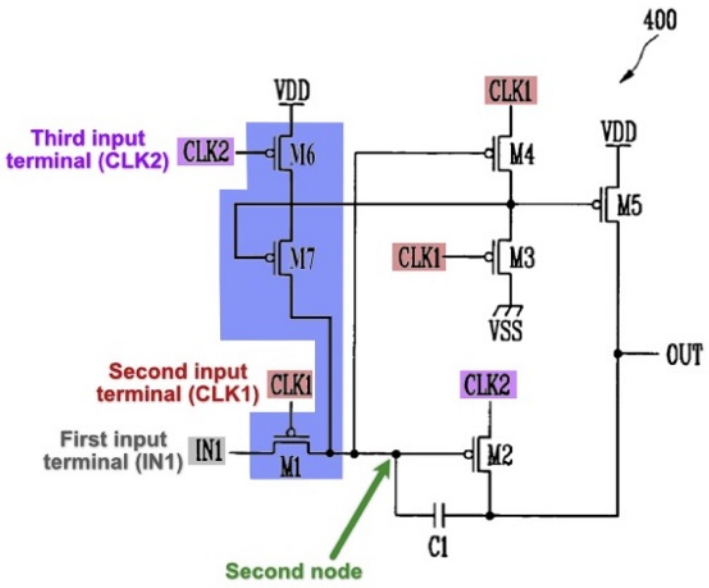
iv. Claim Element [1-a] Summary

414. As just demonstrated, Shin in combination with Sasaki discloses claim sub-elements [1-a-1], [1-a-2], and [1-a-3] of the '593 patent; thus, Shin in combination with Sasaki discloses claim element [1-a] of Claim 1 of the '593 patent.

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c. [1-b]: "a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal; and"

415. Shin in combination with Sasaki discloses this claim element of the '593 patent; this is evident via an annotated version of the combined embodiment presented above:

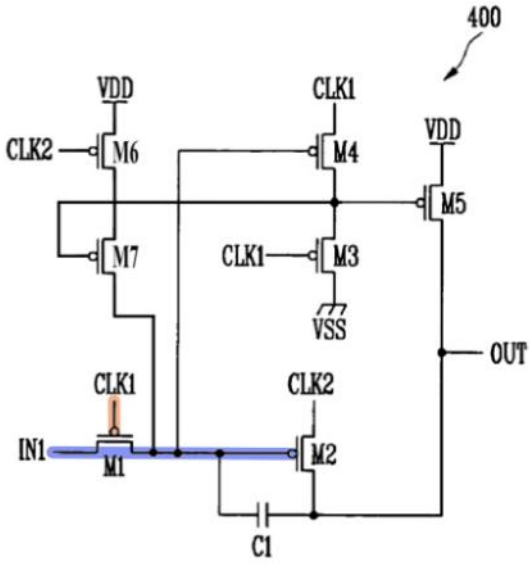


In the figure above, the "first driver" is identified using blue boxing.

416. The voltage on the second node is controlled in accordance with the signals of the first input terminal, the second input terminal, and the third input terminal – as will be shown by the annotations to the following versions of the combined embodiment presented above. As these annotations show, this functionality is implemented in two separate ways – one that combines the first input

terminal and the second input terminal, and a second that uses the third input terminal.

417. The first way, using the first input terminal and the second input terminal, is implemented as described here.

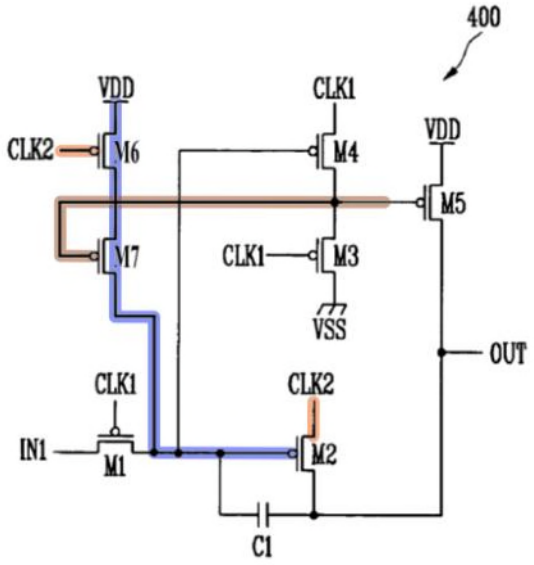


The first way occurs when the second input signal (CLK1) turns on transistor M1; when this occurs, the first input signal (IN1) is transferred to the second node. (On the other hand, when transistor M1 is not turned on, the first input signal (IN1) is not supplied to the second node.)

418. In more detail, transistor M1 is "controlled by the first clock signal CLK1" (the signal supplied by Shin's second input terminal), and operates to "transfer[]" "input signal IN1" (the signal supplied by the first input terminal) to the node (the second node) leading to transistor M2's gate. Ex. 1005, ¶¶ [0088], [0098].

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419. The second way, using the third input terminal, is implemented as described here.



The second way occurs when the input signal (CLK2) at the third input terminal is pulled to a voltage that causes transistor M6 to turn on. If the voltage on the first node is such that it will cause transistor M7 to turn on, then the first power supply voltage (VDD) will be transferred to the second node. (On the other hand, it either CLK2 is such that transistor M6 is turned off or the voltage on the first node is such that transistor M7 is turned off, then the first power supply voltage (VDD) will not be transferred to the second node.)

420. In more detail, transistors M6 and M7 (the anti-reversal circuit added following Sasaki's teachings) supplement transistor M1's operation by receiving an input signal from CLK2 (the signal supplied by Shin's third input terminal) and controlling the potential of the same node for purposes of keeping transistor M2

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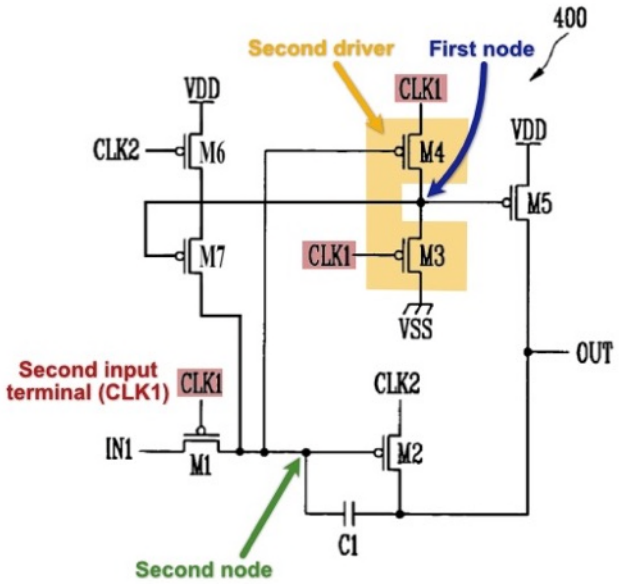
closed when CLK2 is low but OUT is intended to be high. See Ex. 1014, ¶ [0042] and above discussion before element [1-PRE].

421. In overall summation of the discussion above, transistors M1, M6, and M7 together operate to control the voltage of the second node and thus form the claimed first driver.

422. Thus, Shin in combination with Sasaki discloses this claim element of Claim 1 of the ’593 patent.

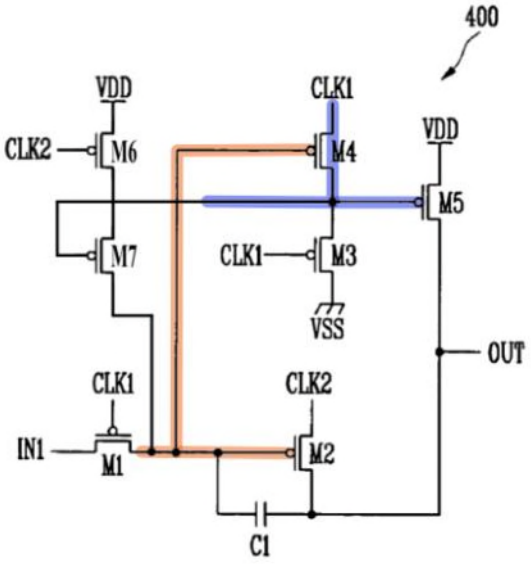
d. [1-c]: “a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node, wherein”

423. Shin in combination with Sasaki discloses this claim element of the ’593 patent; this is evident via an annotated version of the combined embodiment presented above:



In the combined embodiment figure above, the "second driver" is identified using yellow boxing.

424. The voltage on the first node is controlled in accordance with the signal of the second input terminal, and the voltage of the second node – as will be shown by the annotations to the combined embodiment presented above.



When the voltage on the second node is such that transistor M4 is turned on, the second input signal (CLK1) is passed to the first node. (When the voltage on the second node is such that transistor M4 is not turned on, this functionality is not available). Thus, the voltage of the first node is controlled in accordance with the signal of the second input terminal and the voltage of the second node.

425. In more detail and with reference to the two annotated figures presented above, Shin and Sasaki include a "third PMOS transistor M3 … coupled between a second power supply VSS and a first node N1" (Shin's first node). Ex. 1005, ¶

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[0088]. This transistor M3's gate receives input from and is controlled by "the first clock terminal" supplying CLK1 (the second input terminal). *Id.* Further, "[F]ourth PMOS transistor M4 is coupled between the first clock terminal" (the second input terminal) and "the first node N1" (the first node). *Id.* This transistor's gate is connected to the same node (the second node) as the "output terminal of the first PMOS transistor M1." *Id.* Node 1 (the first node) is "coupled" to the "gate terminal" of transistor M5 (the transistor which controls the provision of VDD to OUT). *Id.*

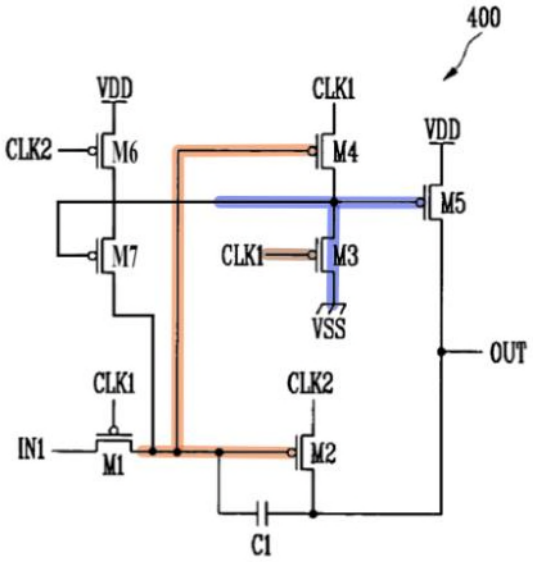
426. In operation, Shin employs CLK1 and the signal received from its second node to control transistors M3 and M4. *See id.* These transistors in turn control the potential of node N1 for purposes of opening/closing transistor M5. *See id.*, ¶¶ [0098]-[0103].

427. Thus, because they collectively control the potential of node N1 (the first node) and receive the required input, transistors M3 and M4 form Shin's second driver.

428. Therefore, Shin in combination with Sasaki discloses this claim element of Claim 1 of the '593 patent.

429. For completeness, it should be noted that there is also a second way that the combined embodiment depicted above can implement this claimed functionality.

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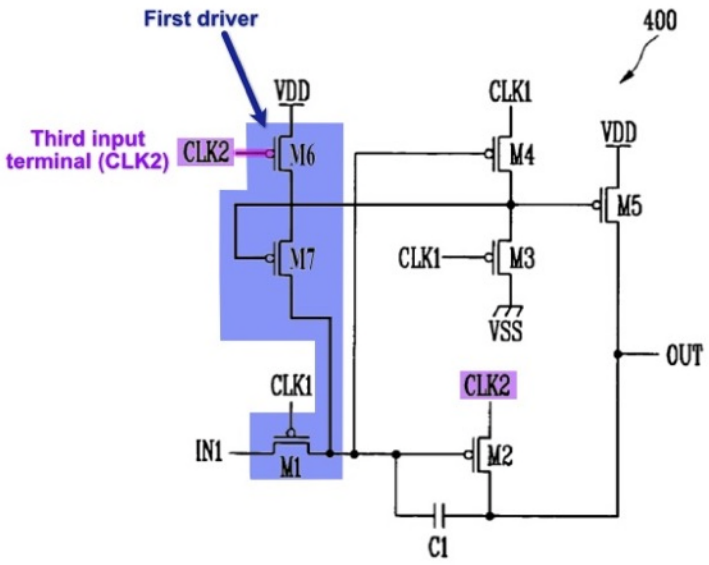
When the voltage on the second node is such that transistor M4 is turned off and when the second input signal turns on transistor M3, then the voltage on the first node will be pulled to the voltage of the second power supply (VSS). (If the voltage on the second node is such that transistor M4 is turned off but the second input signal is such that it does not turn on transistor M3, then this functionality is not available.)

430. Therefore, Shin in combination with Sasaki discloses this claim element of Claim 1 of the ’593 patent.

e. [1-d]: “the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver.”

431. Shin in combination with Sasaki discloses this claim element of the ’593 patent; this is evident via annotated versions of the combined embodiment presented above:

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When a signal applied to the third input terminal (CLK2), this signal directly controls the on/off operation of transistor M6 – which is part of the first driver.

432. Thus, Shin in combination with Sasaki discloses this claim element of Claim 1 of the ’593 patent.

f. Claim 1 Summary

433. As just shown, Shin in combination with Sasaki discloses each element of Claim 1 of the ’593 patent; thus, Shin in combination with Sasaki renders obvious Claim 1 of the ’593 patent.

3. Dependent Claim 2

434. As an initial matter, Claim 2 depends from Claim 1; as was shown above, Claim 1 of the ’593 patent is disclosed by Shin in combination with Sasaki.

435. Claim 2 further requires that “wherein the first input terminal receives an output signal of a previous stage circuit or a start signal, wherein the second input

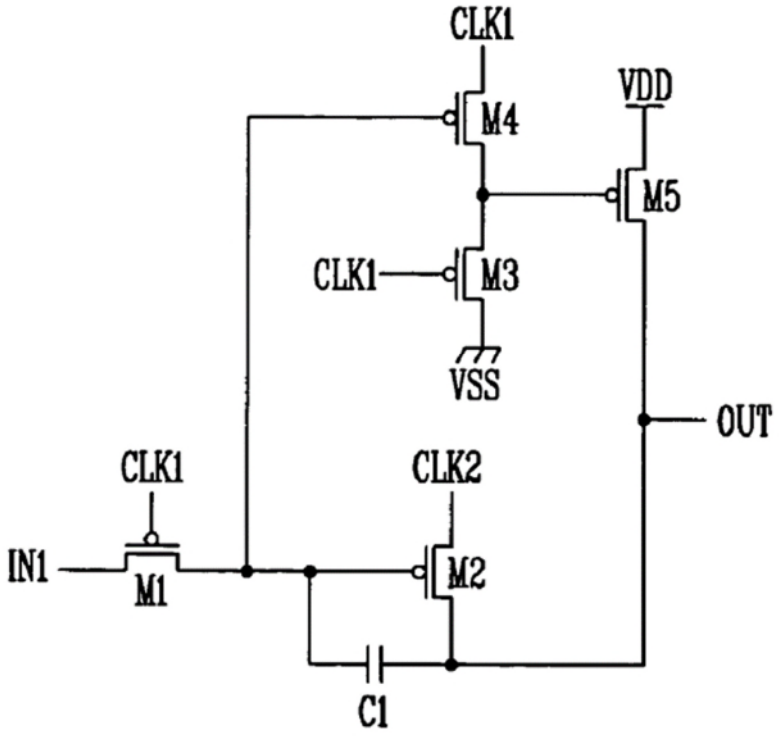
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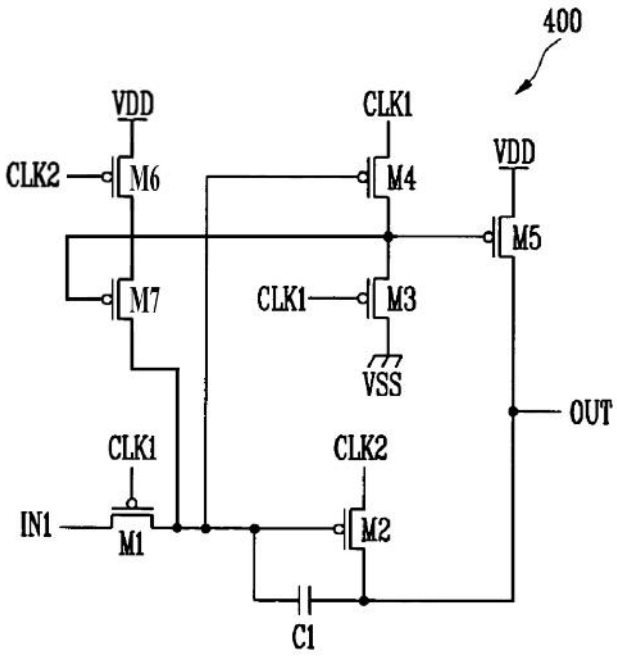
terminal receives a first clock signal, and wherein the third input terminal receives a second clock signal." Shin combined with Sasaki discloses this claim of the '593 patent.

436. As an initial matter, note that the first part of the claim language just cited includes "wherein the first input terminal receives an output signal of a previous stage circuit ***or*** a start signal" (emphasis added). Because of the use of "or," the presence of this claim element term can be shown to be present in Shin and Shin + Sasaki if the first input terminal receives and "an output signal of a previous stage circuit" or "a start signal"; it will be shown next that Shin and Shin + Sasaki discloses the second of these two options.

437. To begin, consider the two stage circuits embodiments of Shin that are under consideration here – Figure 11 of Shin as-is, and the combined embodiment that is formed by combining Shin Figure 11 with Sasaki:

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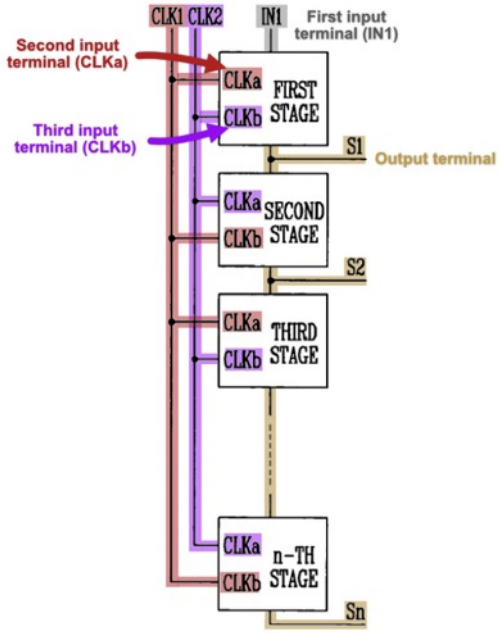




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In both cases, there is first input signal at IN1, a second input signal at the various instances of CLK1, and a third input signal at various instances of CLK2 – along with an output signal at OUT.

438. The higher-level rendition of the shift register architecture described in Shin can be understood via examination of this excerpt from Figure 10 of Shin:



Ex. 1005, Fig. 10 (annotated). What is going on here is explained in the specification of Shin. With regard to the clock signal inputs to the first stage,

> [E]ach stage of the scan drive unit 312 includes a first clock terminal CLKa and a second clock terminal CLKb. First and second phase inverted clock signals CLK1 and CLK2 in which parts of high levels overlap with each other, are supplied to the first clock terminal CLKa and the second clock terminal CLKb, respectively. A first clock signal CLK1 is supplied to the first clock terminal CLKa of odd-numbered stages in the first scan driver 310, and a

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> second clock signal CLK2 is supplied to the second clock terminal CLKb.

Id., ¶ [0074].

Since the first stage is an odd-numbered stage, the "first clock signal CLK1 is supplied to the first clock terminal CLKa" and the "second clock signal CLK2 is supplied to the second clock terminal CLKb." This provides "the second input terminal receives a first clock signal, and wherein the third input terminal receives a second clock signal" of Claim 2. Meanwhile, with regard to the input signal to the first stage,

> Here, a first input signal IN1 is supplied to a first stage included in the scan drive unit 312…

Id., ¶ [0073].

As this is the first stage block of a chain of many stage circuit blocks, the "first input signal IN1 is supplied to a first stage" provides the "first input terminal receives … a start signal" of Claim 2 – as the "first input signal" of Shin is the "start signal" of Claim 2.

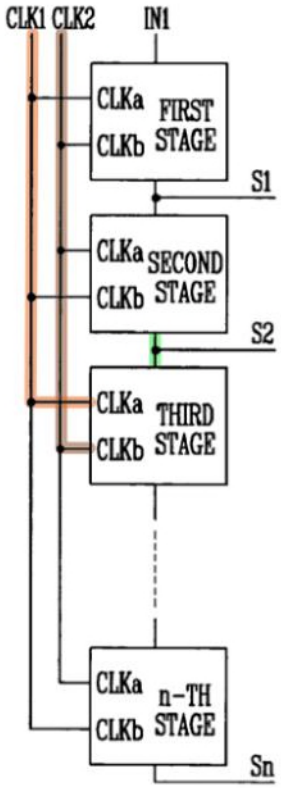
439. Thus, Shin in combination with Sasaki discloses Claim 2 of the '593 patent.

440. For completeness, it can be noted that the other part of the "or" situation discussed at the beginning of this discussion of Claim 2 ("wherein the first input

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terminal receives an output signal of a previous stage circuit ***or*** a start signal") is also present in Shin and Sasaki.

441. This is readily illustrated by first starting with a differently-annotated version of the excerpt of Figure 10 of Shin that was presented above.



Ex. 1005, Fig. 10 (annotated). Since the third stage is also an odd-numbered stage, the excerpt from Shin cited earlier applies here as well:

> [E]ach stage of the scan drive unit 312 includes a first clock terminal CLKa and a second clock terminal CLKb. First and second phase inverted clock signals CLK1 and CLK2 in which parts of high levels overlap with each other, are supplied to the first clock terminal CLKa and the

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> second clock terminal CLKb, respectively. A first clock signal CLK1 is supplied to the first clock terminal CLKa of odd-numbered stages in the first scan driver 310, and a second clock signal CLK2 is supplied to the second clock terminal CLKb.

Ex. 1005, ¶ [0074].

Once again, the "first clock signal CLK1 is supplied to the first clock terminal CLKa" and the "second clock signal CLK2 is supplied to the second clock terminal CLKb" provides "the second input terminal receives a first clock signal, and wherein the third input terminal receives a second clock signal" of Claim 2.

442. However, rather the IN1 start signal provides to the first input terminal of the first stage, the first input signal of the third stage receives the output signal of the previous (second) stage:

> [E]ach stage receives the first input signal IN1 or *an output voltage gi of a previous stage*…

Id., ¶ [0075].

This provides "first input terminal receives an output signal of a previous stage circuit" of Claim 2.

443. Thus, for a second reason, Shin in combination with Sasaki discloses Claim 2 of the '593 patent.

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4. Dependent Claim 3

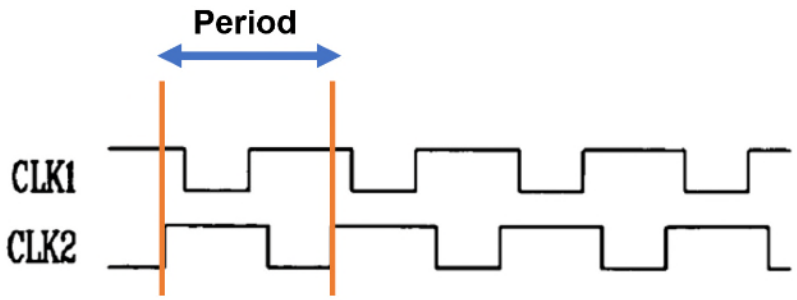
444. As an initial matter, Claim 3 depends from Claim 2, which depends from Claim 1; as was shown above, Claim 1 and Claim 2 of the ’593 patent are disclosed by Shin in combination with Sasaki.

445. Claim 3 further requires that “the first clock signal and the second clock signal have the same period and have phases that do not overlap.”

446. As an initial matter, the meaning of the phrase “do not overlap” (in the context of the ‘593 patent) was explained earlier (in Section XII.A.3).

447. This behavior is depicted as part of Figure 9 of Shin (which is depicted twice below) – and is in two parts.

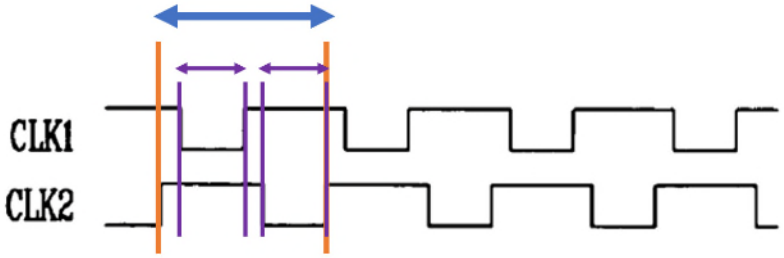
448. The first issue is the period of the two clock signals. As described above, the “period” of a repeating (i.e., recurring) signal is well-known in that art as being the time that it takes for that signal to repeat itself.



Ex. 1005, Fig. 9 (excerpted, with annotations added). As can readily be seen, in this particular instance, the period of the first clock signal (CLK1) and the period of the second clock signal (CLK2) are identical.

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449. The second issue is whether or not the two clock signals "do not overlap" – as per the explanation of Section XII.A.3.



Id. (excerpted with annotation added). As can be seen (via the purple annotations), this is indeed the case for these two waveforms.

450. Thus, Shin and Shin in combination with Sasaki render obvious this claim of the '593 patent.

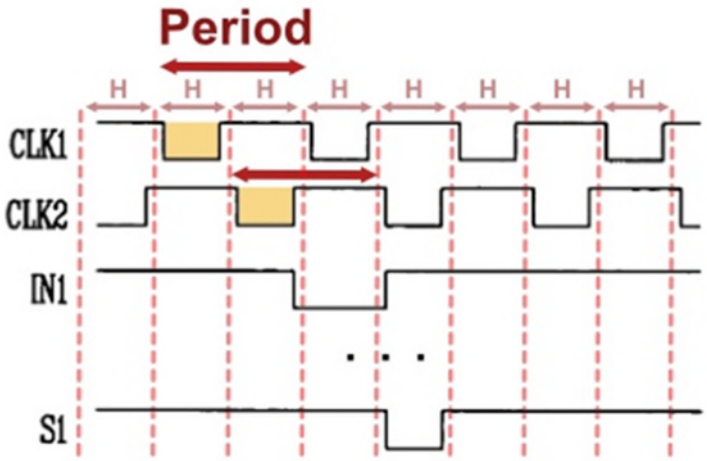
5. Dependent Claim 4

451. As an initial matter, Claim 4 depends from Claim 3, which depends from Claim 2, which depends from Claim 1; as was shown above, Claim 1, Claim 2, and Claim 3 of the '593 patent are disclosed by Shin in combination with Sasaki.

452. Claim 4 further requires that "the first clock signal and the second clock signal have a period equal to two horizontal periods 2H and are supplied in different horizontal periods as low signals."

453. This can be readily-seen via an annotated version of Figure 9 of Shin:

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Ex. 1005, Fig. 9 (excerpted with annotations added); *see also* discussion of ’593 patent in *supra* Section IX.B.4.) Shin’s CLK1 and CLK2 are supplied such that they have a regular, repeating period spanning two time intervals (where on time interval is labeled as “H” in the figure above). Further, CLK1 and CLK2 are low in different, successive time intervals.

454. Thus, Shin and Shin in combination with Sasaki render obvious this claim of the ’593 patent.

6. Dependent Claim 5

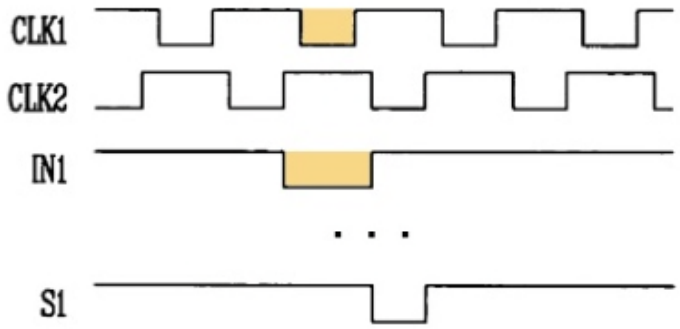
455. As an initial matter, Claim 5 depends from Claim 2, which depends from Claim 1; as was shown above, Claim 1 and Claim 2 of the ’593 patent are disclosed by Shin in combination with Sasaki.

456. Claim 5 further requires that “the start signal is supplied to overlap the first clock signal.”

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457. As an initial matter, the meaning of the phrase "overlap" (in the context of the '593 patent) was explained earlier (in Section XII.A.5).

458. That this is the case can be readily-seen via an annotated version of Figure 9 of Shin:



Ex. 1005, Fig. 9 (excerpted with annotations added). As shown by the orange highlighting, the start signal (the orange-annotated part of the signal IN1) and CLK1 (the first clock signal) overlap.

459. Thus, Shin and Shin in combination with Sasaki render obvious this claim of the '593 patent.

7. Dependent Claim 6

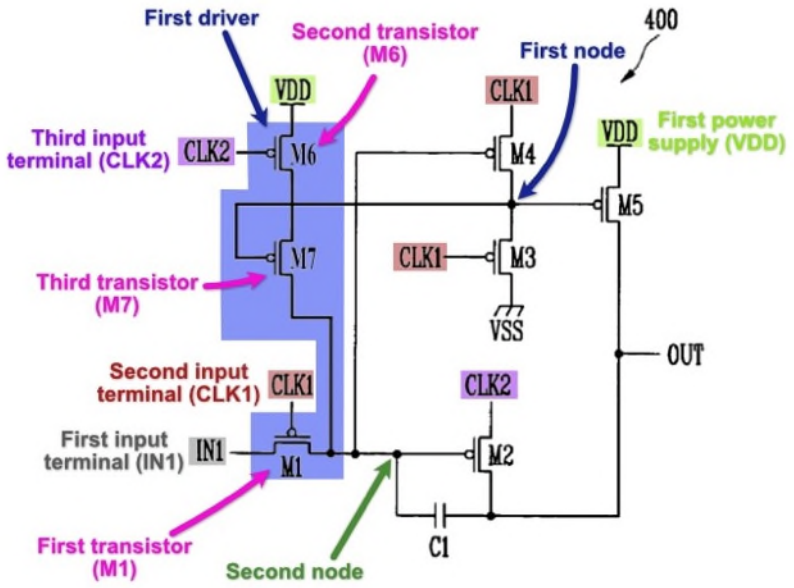
460. As an initial matter, Claim 6 depends from Claim 2, and Claim 2 depends from Claim 1; as was shown above, Claim 1 and Claim 2 of the '593 patent are disclosed by Shin in combination with Sasaki.

461. Claim 6 further requires that "wherein the first driver includes" – followed by four claim elements.

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a. [6-a]: "a first transistor between the first input terminal and the second node, the first transistor having a gate electrode coupled to the second input terminal; and"

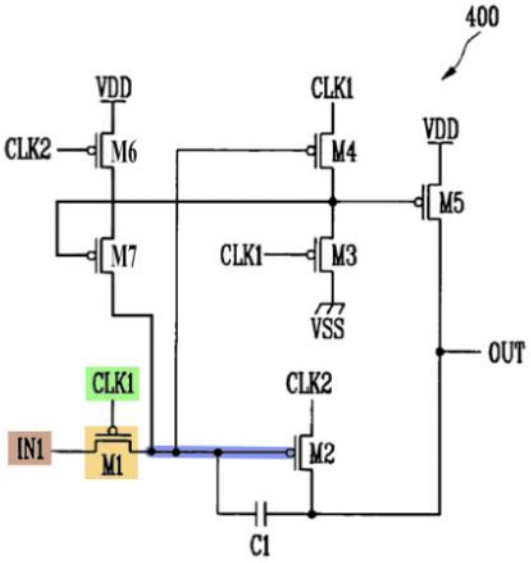
462. This claim element is disclosed by Shin in combination with Sasaki; this can readily be seen in the overall structure of the combined embodiment of Shin and Sasaki that was introduced above:



As the annotations show, this embodiment has a first transistor between the first input terminal and the second node, and the first transistor has a gate electrode coupled to the second input terminal.

463. For clarity with respect to this claim element, this is also evidenced via more-detailed examination of the combined embodiment.

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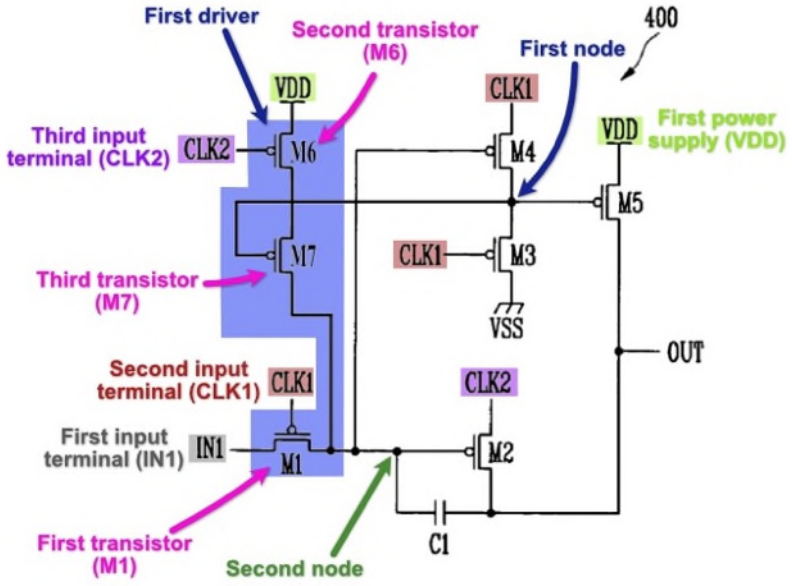
Here, the first transistor is annotated in orange, the first input terminal is annotated in brown, the second node is annotated in blue, and the second input terminal is annotated in green – which, as noted above, shows that this embodiment has a first transistor between the first input terminal and the second node, and shows that the first transistor has a gate electrode coupled to the second input terminal.

464. Thus, Shin in combination with Sasaki discloses this claim element of Claim 6 of the ’593 patent.

b. [6-b]: “a second transistor and a third transistor serially positioned between the second node and the first power supply,”

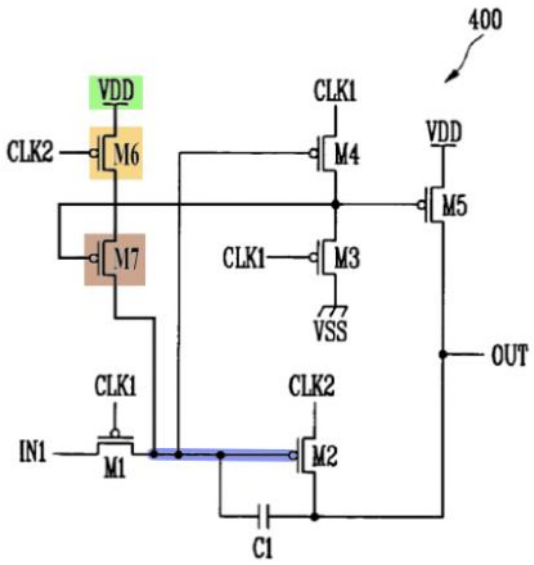
465. This claim element is disclosed by Shin in combination with Sasaki; this can readily be seen in the overall structure of the combined embodiment of Shin and Sasaki that was introduced above:

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As the annotations show, this embodiment has a second transistor and a third transistor serially positioned between the second node and the first power supply.

466. For clarity with respect to this claim element, this is also evidenced via more-detailed examination of the combined embodiment.

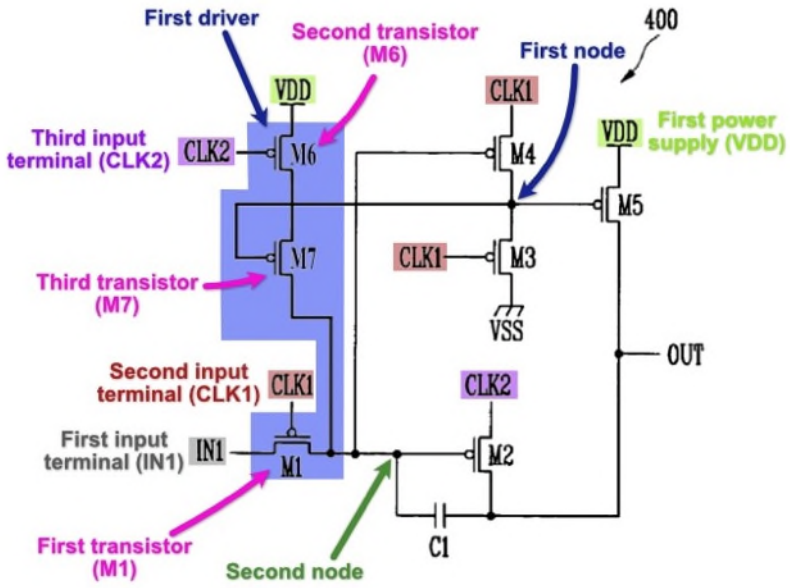


The second transistor is annotated in orange, the third transistor is annotated in brown, the second node is annotated in blue, and the first power supply is annotated in green.

467. Thus, Shin in combination with Sasaki discloses this claim element of Claim 6 of the ’593 patent.

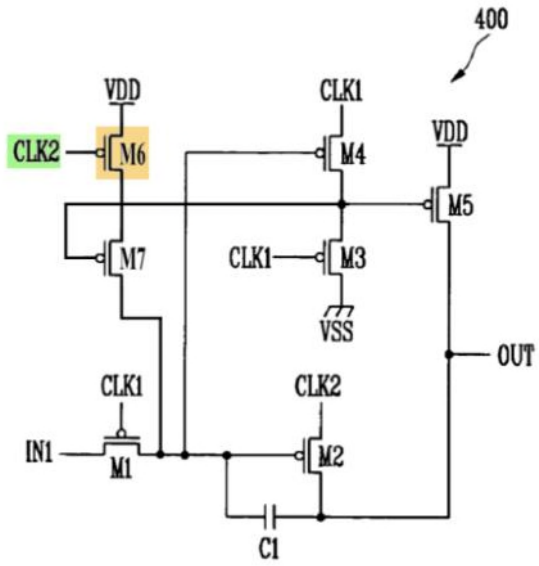
c. [6-c]: “wherein a gate electrode of the second transistor is coupled to the third input terminal, and”

468. This claim element is disclosed by Shin in combination with Sasaki; this can readily be seen in the overall structure of the combined embodiment of Shin and Sasaki that was introduced above:



As the annotations show, in this embodiment, the gate electrode of the second transistor is coupled to the third input terminal.

469. For clarity with respect to this claim element, this is also evidenced via more-detailed examination of the combined embodiment.



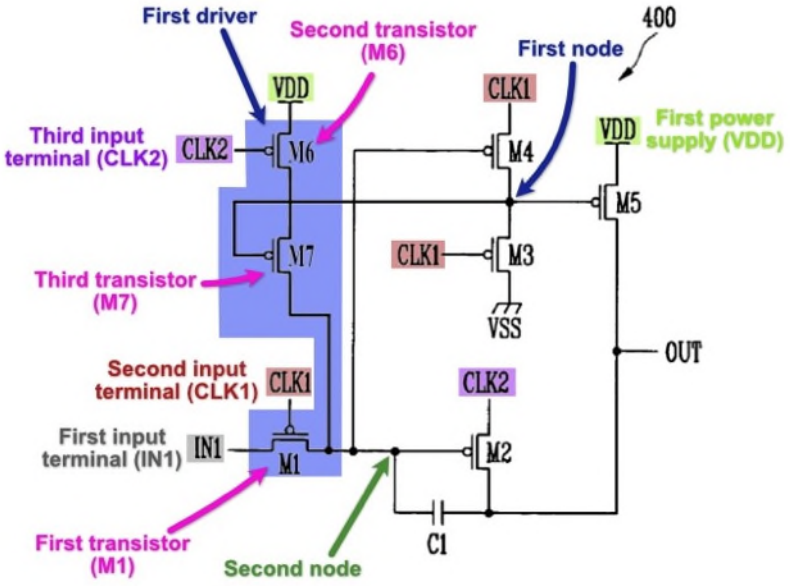
The second transistor is annotated in orange, while the third input terminal is annotated in green.

470. Thus, Shin in combination with Sasaki discloses this claim element of Claim 6 of the ’593 patent.

d. [6-d]: “wherein a gate electrode of the third transistor is coupled to the first node.”

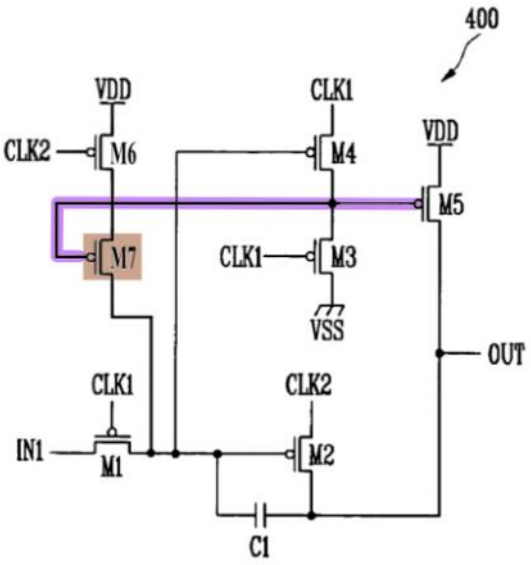
471. This claim element is disclosed by Shin in combination with Sasaki; this can readily be seen in the overall structure of the combined embodiment of Shin and Sasaki that was introduced above:

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As the annotations show, in this embodiment, the gate electrode of the third transistor is coupled to the first node.

472. For clarity with respect to this claim element, this is also evidenced via more-detailed examination of the combined embodiment.



The third transistor is annotated in brown, while the first node is annotated in purple.

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473. Thus, Shin in combination with Sasaki discloses this claim element of Claim 6 of the ’593 patent.

e. Claim 6 Summary

474. As just shown, Shin in combination with Sasaki discloses each element of Claim 6 of the ’593 patent; thus, Shin in combination with Sasaki/ renders obvious Claim 6 of the ’593 patent.

8. Dependent Claim 8

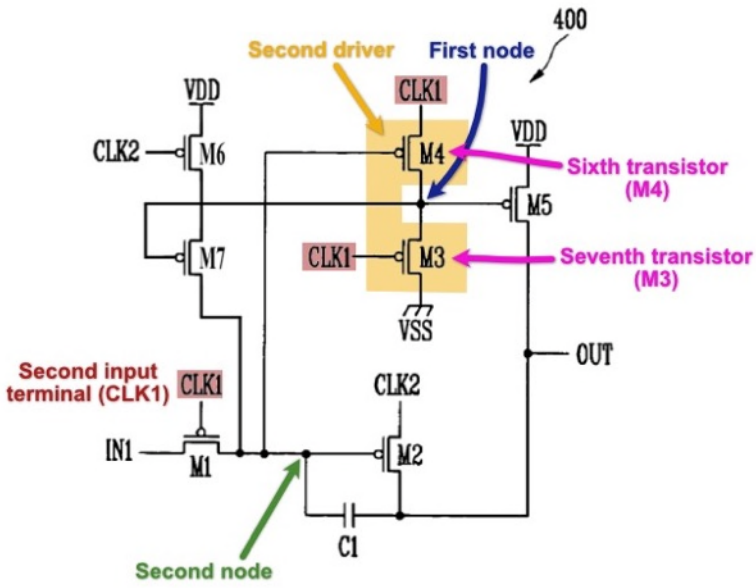
475. As an initial matter, Claim 8 depends from Claim 2, and Claim 2 depends from Claim 1; as was shown above, Claim 1 and Claim 2 of the ’593 patent are disclosed by Shin in combination with Sasaki.

476. Claim 8 further requires that “wherein the second driver includes” – followed by two claim elements.

a. [8-a]: “a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and”

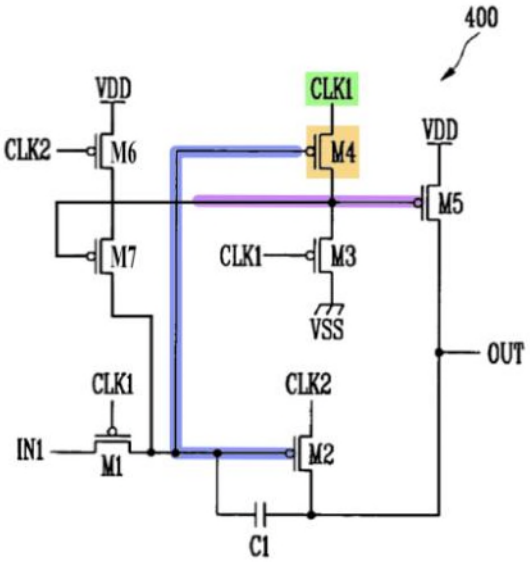
477. This claim element is disclosed by Shin in combination with Sasaki; this can readily be seen in the overall structure of the combined embodiment of Shin and Sasaki that was introduced above:

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As the annotations show, this embodiment has a sixth transistor between the first node and the second input terminal, and the sixth transistor has a gate electrode coupled to the second node.

478. For clarity with respect to this claim element, this is also evidenced via more-detailed examination of the combined embodiment that was presented earlier.

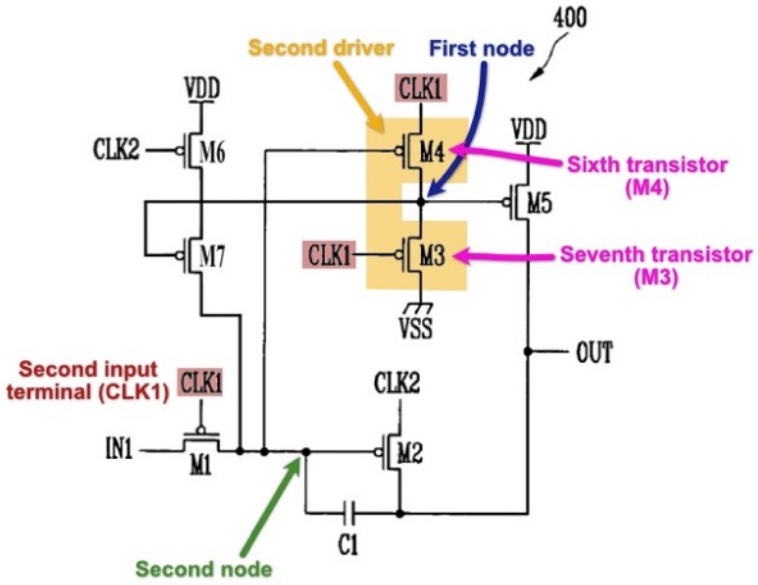


The sixth transistor is annotated in orange, the first node is annotated in purple, the second input terminal is annotated in green, and the second node is annotated in blue.

479. Thus, Shin in combination with Sasaki discloses this claim element of Claim 8 of the ’593 patent.

b. [8-b]: “a seventh transistor between the first node and a second power supply, the second power supply having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal.”

480. This claim element is disclosed by Shin in combination with Sasaki; this can readily be seen in the overall structure of the combined embodiment of Shin and Sasaki that was introduced above:

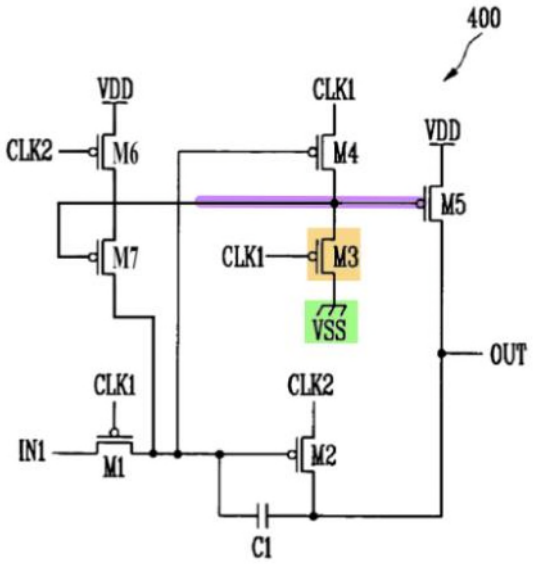


As the annotations show, this embodiment has a seventh transistor between the first node and a second power supply, the second power supply having a lower voltage

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than the first power supply, and the seventh transistor has a gate electrode coupled to the second input terminal.

481. For clarity with respect to this claim element, this is also evidenced via more-detailed examination of the combined embodiment.



The seventh transistor is annotated in orange, the first node is annotated in purple, the second power supply is annotated in green, and second input terminal is annotated in brown.

482. Further, Shin specifies that "the second power supply [has] a lower voltage than the first power supply."

> … a first power supply VDD of a high level…

Ex. 1005, ¶ [0099].

> Furthermore, a negative supply voltage may be applied to the second power supply VSS.

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Id., ¶ [0093].

This description in Shin is consistent with long-known practice in the art for circuitry that is based upon the use of transistors – in which VDD is a positive DC voltage and VSS is either a negative voltage or is simply ground (GND); this would have been known to a POSITA – and a POSITA would also be aware that the circuitry requires at least that VDD be a higher voltage than VSS for the circuitry to function properly. This is a textbook concept. Thus, Shin in combination with Sasaki discloses this claim element of Claim 8 of the ’593 patent.

c. Claim 8 Summary

483. As just shown, Shin in combination with Sasaki discloses each element of Claim 8 of the ’593 patent; thus, Shin in combination with Sasaki renders obvious Claim 8 of the ’593 patent.

9. Dependent Claim 14

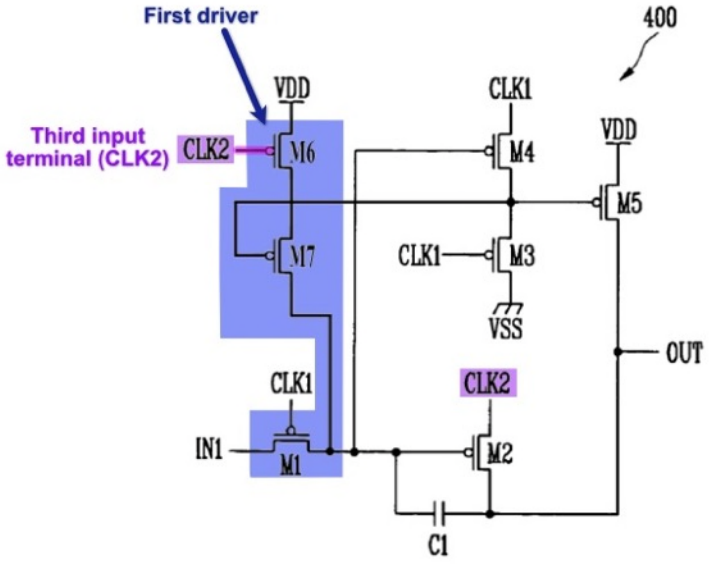
484. As an initial matter, Claim 14 depends from Claim 1; as was shown above, Claim 1 of the ‘593 patent is disclosed by Shin in combination with Sasaki.

485. Claim 14 further requires that “the transistor controls the voltage of the second node according to the on/off operation thereof.”

486. As an initial matter, Claim 14 simply states “the transistor”; the only “transistor” mentioned by name in Claim 1 appears in claim element [1-d} (“the signal of the third input terminal directly controls an on/off operation of *a transistor*,

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the transistor included in the first driver"; emphasis added) – which was discussed earlier in Section XII.B.2.e.



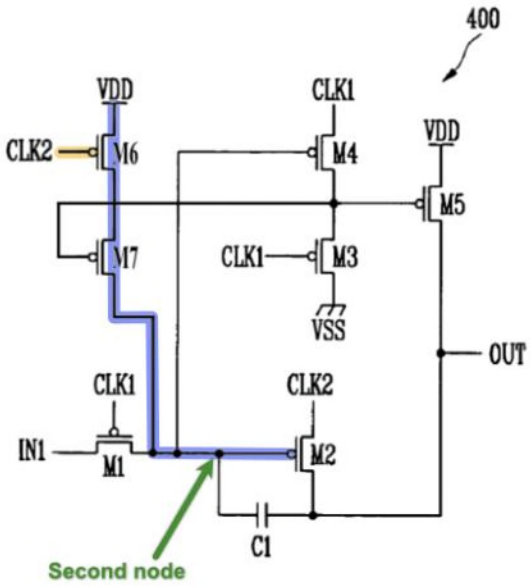
Thus, transistor M6 is duly identified as being "the transistor" of Claim 14.

487. Further, as shown above, "the signal of the third input terminal directly controls an on/off operation of [the] transistor" (here M6).

488. The only additional functionality included in Claim 14 is that "the transistor controls the voltage of the second node," since the second part of the claim was already demonstrated in the discussion of claim element [1-d] (that is, "directly controls an on/off operation of a transistor").

489. This addition in Claim 14 is readily shown by simple examination of the annotated circuit figure presented just above – as the implications of what occurs when transistor M6 is turned on are readily apparent:

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As can be seen, when the CLK2 signal is such that it turns on transistor M6, when transistor M7 is also turned on, the power supply voltage will be passed to the second node. (On the other hand, when the CLK2 signal is such that it turns transistor M6 off, this functionality is not available.)

490. Therefore, the transistor (M6) controls the voltage of the second node according to the on/off state of that transistor (M6).

491. Thus, Shin in combination with Sasaki renders obvious Claim 14 of the ‘593 patent.

10. Independent Claim 15

492. It is my conclusion and opinion that Claim 15 of the ’593 patent is rendered obvious by Shin in combination with Sasaki, in view of the knowledge of a POSITA.

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a. [15-pre]: "An organic light emitting display, comprising:"

493. To the extent that the preamble is limiting (and, for the reasons that I discuss below in connection with the Tobita reference, it is not), Shin in combination with Sasaki discloses the preamble of Claim 15 of the '593 patent.

494. Shin makes it abundantly clear that his inventions are targeted at organic light emitting displays – as is made evident by just a few selected examples.

495. The title of Shin's patent application is "Scan Driving Circuit and Organic Light Emitting Display Using the Same." Further, the Abstract of Shin begins with the sentence "A scan driving circuit and an organic light emitting display using the scan driving circuit are disclosed." In addition, the text part of the specification opens with a "Field of Invention" section, the first paragraph of which is:

> The field of the present invention relates to an organic light emitting display, and more particular to a scan driving circuit used for a current programming type organic light emitting display.

Ex. 1005, ¶ [0003].

Numerous other examples can be found throughout Shin (*see, e.g., id.*, ¶¶ [0016], [0041]-[0042]), but these examples are sufficient for this analysis.

496. Thus, even if the preamble of Claim 15 is limiting, Shin and Sasaki render obvious the preamble of Claim 15 of the '593 patent.

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b. [15-a]: "pixels positioned in regions partitioned by scan lines and data lines;"

497. Shin and Sasaki disclose this claim element of Claim 15 of the '593 patent.

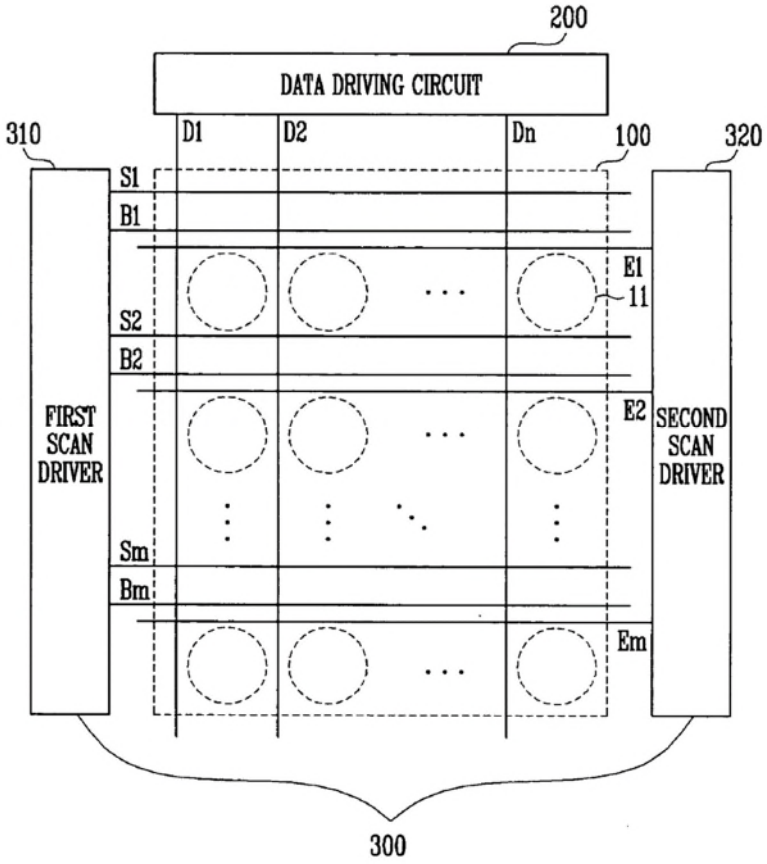
498. As above, Shin provides numerous instances demonstrating this disclosure; for example,

> The display panel 100 includes a plurality of data lines D1 through Dn, a plurality of signal lines S1 to Sm, E1 to Em, B1 to Bm, and a plurality of pixel circuits 11. The plurality of data lines D1 through Dn are arranged in a column direction. The plurality of signal lines S1 to Sm and E1 to Em are arranged in a row direction. The plurality of pixel circuits 11 are arranged in an array.

Ex. 1005, ¶ [0044].

499. Shin also depicts this overall architecture in Figure 4:

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Id., Fig. 4. As can be seen from this Figure and the excerpt from Shin above, the "S" lines (horizontal) are the scan lines, and the "D" lines (vertical) are the data lines.

500. In more detail, as described by Shin, the pixel circuits are separated by horizontal "signal lines S1 to Sm for transferring a selection signal to a select a row of pixels" and vertical "data lines D1 through Dn." *Id.*, ¶¶ [0046]-[0047]. The signal lines are connected to a "scan driving circuit 300," while the data lines are connected to a "data driving circuit 200." *Id.* And, as shown above (in Figure 4 of Shin), pixels 11 are located in the spaces between signal and data lines.

501. Thus, Shin discloses this claim element of Claim 15 of the '593 patent.

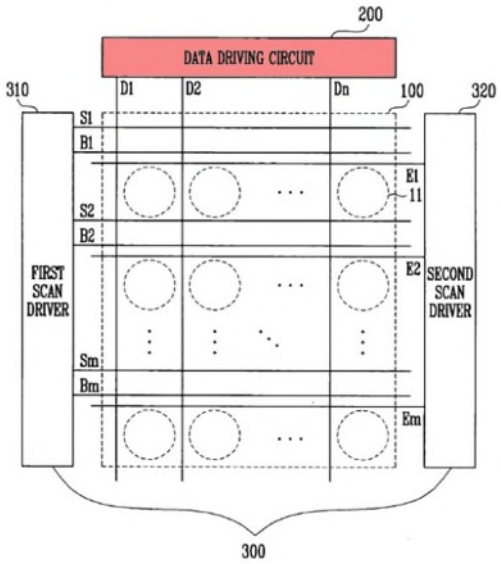
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c. [15-b]: "a data driver for supplying data signals to the pixels through the data lines; and"

502. Shin discloses this claim element of Claim 15 of the '593 patent.

503. Shin explicitly identifies a "data driving circuit" in Figure 4:

FIG. 4



Ex. 1005, Fig. 4 (annotation added).) As Shin explains, the "data lines D1 through Dn" are connected to a "data driving circuit 200" that "applies a data current I_{DATA}" to each of the data lines. *Id.*, ¶ [0047].

504. Thus, Shin discloses this claim element of Claim 15 of the '593 patent.

d. [15-c]: "a scan driver for supplying scan signals to the pixels through the scan lines, the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals and having a first input terminal, a second input terminal, a third input terminal, and an output terminal,"

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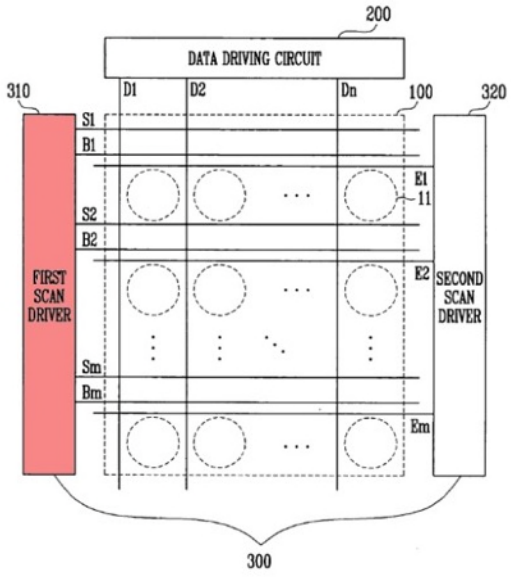
505. My analysis of claim element [15-c] is broken up into sub-elements.

i. [15-c-1]: "a scan driver for supplying scan signals to the pixels through the scan lines"

506. Shin discloses this claim sub-element of claim element [15-c] of Claim 15 of the '593 patent.

507. This can readily be seen by examination of Figure 4 of Shin.

FIG. 4



Ex. 1005, Fig. 4 (annotations added). Shin, in fact, discloses two scan drivers – as can be seen in Figure 4 of Shin. In addition, Shin describes its display as including a "first scan driver 310" that "sequentially applies a selecting signal for selecting a pixel circuit 11 to the selection signal lines S1 to Sm." *Id.*, ¶ [0047].

508. Thus, Shin discloses this claim sub-element of claim [15-c] of Claim 15 of the '593 patent.

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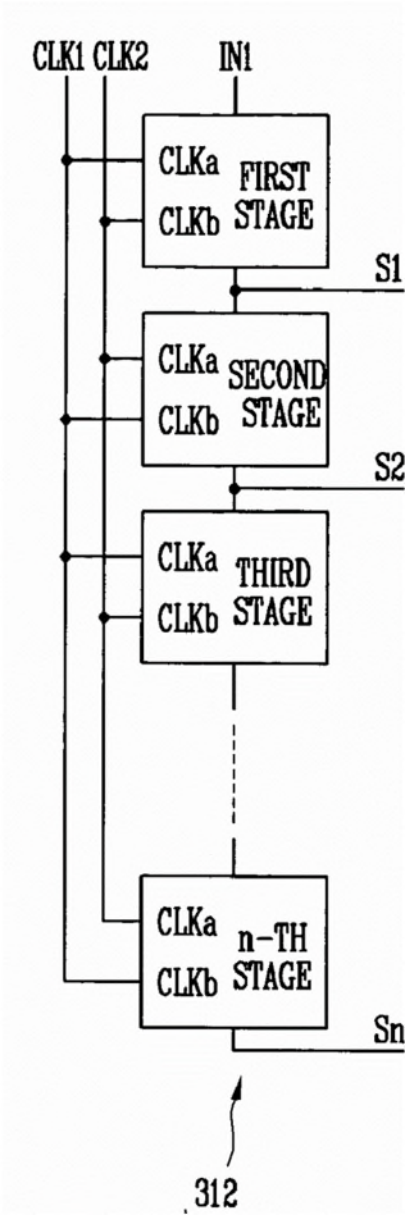
ii. [15-c-2]: "the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals"

509. Shin discloses this claim sub-element of claim element [15-c] of Claim 15 of the '593 patent.

510. Just above, in the discussion of claim sub-element [15-c-1], it was shown – via Figure 4 of Shin – that Shin discloses at least one scan driver. As Shin explains, this "first scan driver" includes a "scan drive unit 312" formed from a series of "stages" that are "coupled" with various "input signal … lines." *Id.*, ¶ [0070]-[0071].

511. As Shin explains (at [0028] and [0031]), Figure 7 and Figure 10 contain a more-detailed, block-level description of a scan driver.

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Id., Figs, 7, 10. As can seem by simple inspection, this depiction shows that a scan driver includes stage circuits – and that these scan circuits are coupled to the previously-identified scan lines (S1, S2, … Sn). As described earlier (in the discussion of Claim 2), each scan line is fed by the output of a corresponding stage circuit. Further, as Shin explains, the "scan drive unit 312" is formed from a series

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of "stages" that are "coupled" with various "input signal … lines." *Id.*, ¶ [0070]-[0071].

512. Thus, Shin discloses this claim sub-element of claim [15-c] of Claim 15 of the '593 patent.

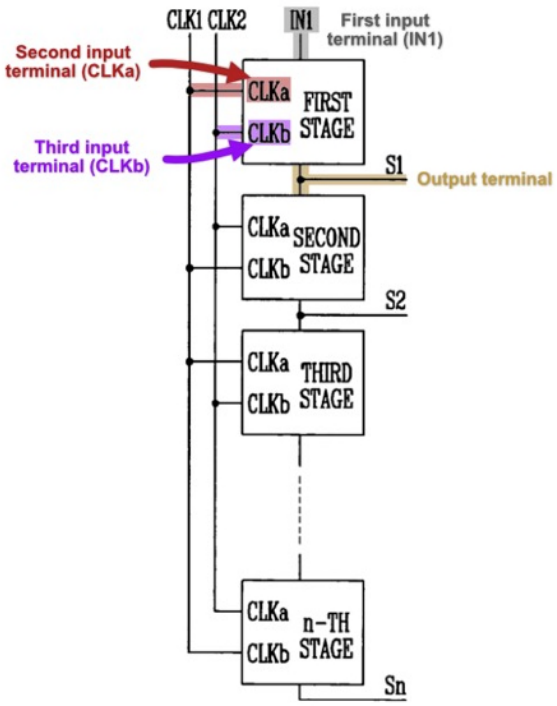
iii. [15-c-3]: "and having a first input terminal, a second input terminal, a third input terminal, and an output terminal,"

513. This claim sub-element of claim element [15-c] of Claim 15 of the '593 patent is disclosed by Shin and Shin in combination with Sasaki.

514. The claim sub-element is essentially identical to the preamble of Claim 1 of the '593 patent – which was already discussed in detail earlier (at Section XII.B.2.a) – where it was shown that these details are disclosed by Shin in combination with Sasaki.

515. However, for clarity, rather than mapping these four terminals of the claim sub-element onto the circuitry-level description (as was done with respect to the preamble of Claim 1), here the four terminals can be identified in the block-level circuitry of Figure 7:

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Ex. 1005, Fig. 7 (annotated). As shown in this annotated version of Figure 7, a "first input signal IN1 is supplied to a first stage included in the scan drive unit 312." *Id.*, ¶ [0073]. The terminal supplying this signal is Shin's first input terminal. Further, "each stage of the scan drive unit 312 includes a first clock terminal CLKa and a second clock terminal CLKb" that receive "[f]irst and second clock signals CLK1 and CLK2…." *Id.*, ¶ [0074]. These are respectively Shin's second input terminal and third input terminal.

516. Finally, each stage includes an "output lin[e]" that is "coupled with … row lines S1 to Sn" to "provide" the pixel "selection signal." *Id.*, ¶ [0072]. This is Shin's output terminal.

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517. Note again that each stage will have the internal structure shown and discussed repeatedly earlier in connection with claim 1 – as was mentioned above.

518. Thus, Shin and Sasaki disclose this claim sub-element of claim element [15-c] of Claim 15 of the ’593 patent.

iv. Claim Element [15-c] Summary

519. As just demonstrated, Shin and Shin in combination with Sasaki discloses claim sub-elements [15-c-1], [15-c-2], and [15-c-3] of the ‘593 patent; thus, Shin and Shin in combination with Sasaki discloses claim element [15-c] of Claim 15 of the ’593 patent.

e. Preface to Claim Elements [15-d] – [15-g]

520. Between claim element [15-c] and claim element [15-d], Claim 15 includes the phrase “wherein each of the stage circuits includes:”. It is taken here that this is intended to mean that “includes” is stated with regard to the sequential list of claim elements which follow for the remainder of Claim 15 – that is, claim elements [15-d], [15-e], [15-f], and [15-g]. Each of these claim elements will be considered in turn.

f. [15-d]: “an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node,”

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521. This claim element is identical to claim element [1-a] of Claim 1 of the ’593 patent – which was discussed earlier (in Section XII.B.2.b).

522. Thus, Shin and Shin in combination with Sasaki discloses this claim element of Claim 15 of the ’593 patent.

g. [15-e]: “a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal, and”

523. This claim element is identical to claim element [1-b] of Claim 1 of the ’593 patent – which was discussed earlier (in Section XII.B.2.c).

524. Thus, Shin and Shin in combination with Sasaki discloses this claim element of Claim 15 of the ’593 patent.

h. [15-f]: “a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node, wherein”

525. This claim element is identical to claim element [1-c] of Claim 1 of the ’593 patent – which was discussed earlier (in Section XII.B.2.d).

526. Thus, Shin and Shin in combination with Sasaki discloses this claim element of Claim 15 of the ’593 patent.

i. [15-g]: “the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver.”

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527. This claim element is identical to claim element [1-d] of Claim 1 of the ‘593 patent – which was discussed earlier (in Section XII.B.2.e).

528. Thus, Shin and Shin in combination with Sasaki discloses this claim element of Claim 15 of the ’593 patent.

j. Claim 15 Summary

529. As shown, Shin in combination with Sasaki discloses each element of Claim 15 of the ’593 patent; thus, Shin in combination with Sasaki render obvious Claim 15 of the ’593 patent.

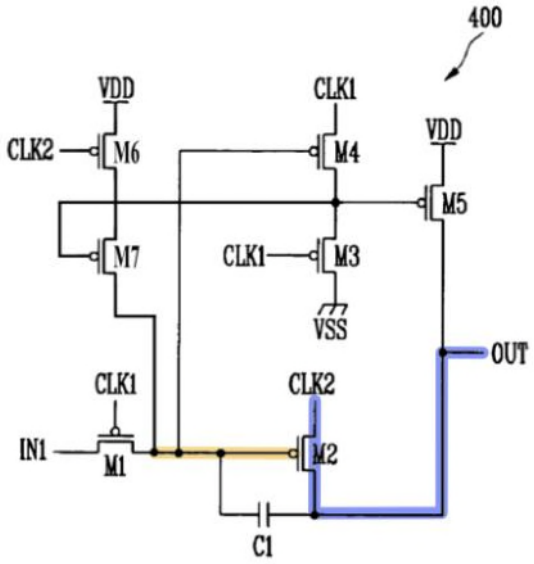
11. Dependent Claim 16

530. As an initial matter, Claim 16 depends from Claim 16; as was shown above, Claim 15 of the ’593 patent is disclosed by Shin in combination with Sasaki.

531. Claim 16 further requires that “a clock signal supplied to the third input terminal is used as the scan signal.”

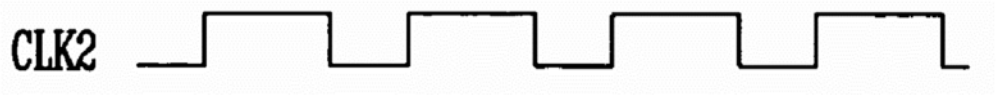
532. The first part of this claim element (“a clock signal supplied to the third input terminal”) was already discussed earlier (in Section XII.B.2.b.iii) – with respect to claim sub-element [1-a-3] of claim element [1-a] of Claim 1 of the ’593 patent. An annotated version of the combined embodiment was provided there for purposes of explanation – and for clarity, that figure will be repeated here.

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As the annotations show, when an appropriate (i.e., turn-on) voltage is applied at the second node, transistor M2 will turn on; this will connect the signal of the third input terminal ("CLK2") to the node of the output terminal ("OUT") – and thus the signal of the third input terminal ("CLK2") is supplied to the output terminal ("OUT"). (On the other hand, when a turn-on voltage is not applied at the second node, transistor M2 will not turn on – and thus the signal of the third input terminal (CLK2) is not supplied to the output terminal ("OUT").) (*See also* Ex. 1005, ¶ [0088].)

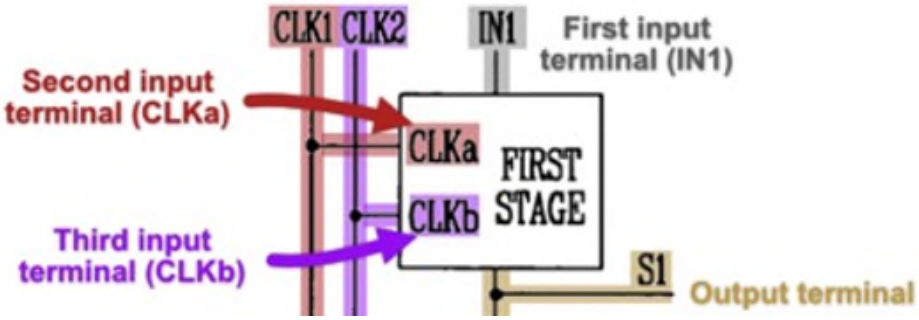
533. As also discussed earlier, the third input terminal receives a clock signal – in particular, the clock signal CLK2, which is depicted in Figure 9 of Shin.



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Id., Fig. 9 (excerpted). As the name itself implies, the signal CLK2 is clearly a clock signal – and, as detailed in the discussion of Claim 2, Shin identifies (e.g., at [0074]) CLK2 as a clock signal.

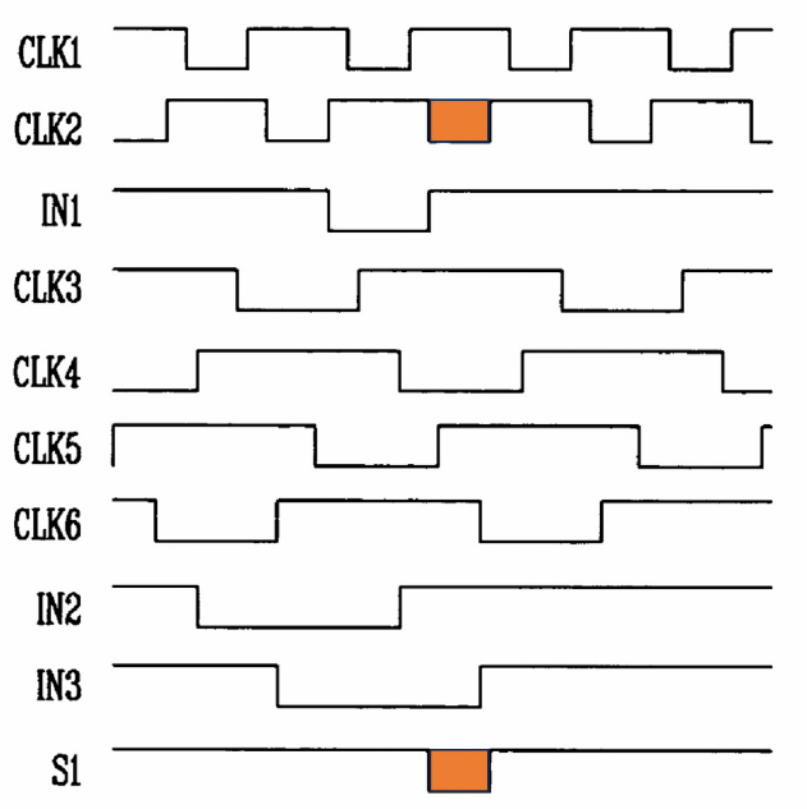
534. Finally, with respect to this clock signal being used as "the scan signal," it was shown above (see the annotated version of the combined embodiment above) that when transistor M2 is turned on, the input signal that is being applied to the third input terminal (which, in this case is the clock signal CLK2) is supplied to the output terminal OUT. What that signal (at OUT) is being used for is made clear via a partial, annotated version of Figure 10 of Shin:



Id., Fig. 10 (excerpted and annotated). As can be seen, the output of the first stage circuit block is being fed to S1. (Note also that each stage circuit block in Figure 10 of Shin feeds the output of its OUT terminal to a scan line of its own (S2, S3 … Sn).) That S1 is a scan lines (as are the lines S2, S3 … Sn) was shown above (in Section XII.B.10.b) with respect to claim element [15-a] (*see also id.*, ¶¶ [0047], [0072]).

535. Further, Figure 9 of Shin shows what use is being made of the clock signal CLK2 (which is being provided to the output terminal).

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Id., Fig. 9 (annotations added). As the annotations show, during the highlighted period, the clock signal supplied to the third input terminal (i.e., CLK2) is used as the scan signal S1. Therefore, the clock signal that is supplied to the third input terminal is passed to the output terminal (OUT), where it is then used as a scan signal.

536. Thus, Shin and Shin in combination with Sasaki render obvious this claim of the ’593 patent.

12. Dependent Claim 17

537. As an initial matter, Claim 17 depends from Claim 15; as was shown above, Claim 15 of the ’593 patent is disclosed by Shin in combination with Sasaki.

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538. Claim 17 further requires that "the first input terminal receives a scan signal of a previous stage circuit or a start signal."

539. This claim is identical to an element of Claim 2 of the '593 patent – which was discussed earlier (in Section XII.B.3).

540. Thus, Shin in combination with Sasaki renders obvious this claim of the '593 patent.

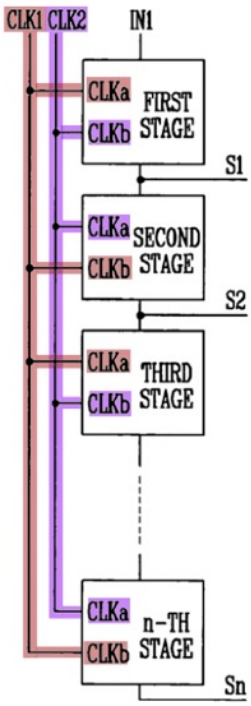
13. Dependent Claim 18

541. As an initial matter, Claim 18 depends from Claim 17, and Claim 17 depends from Claim 15; as was shown above, Claim 15 and Claim 17 of the '593 patent are disclosed by Shin in combination with Sasaki.

542. Claim 18 further requires "wherein second input terminals of odd stage circuits receive a first clock signal and third input terminals of odd stage circuits receive a second clock signal, and wherein second input terminals of even stage circuits receive the second clock signal and third input terminals of even stage circuits receive the first clock signal." In other words, the first clock signal and the second clock signal alternate between the second input terminal and the third terminal along the sequence of stage circuits.

543. First, consider an annotated version of Figure 7 of Shin:

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Ex. 1005, Fig. 7 (annotated). Shin explicitly describes this functionality in the specification:

> Further, each stage of the scan drive unit 312 includes a first clock terminal CLKa and a second clock terminal CLKb. First and second phase inverted clock signals CLK1 and CLK2 in which parts of high levels overlap with each other, are supplied to the first clock terminal CLKa and the second clock terminal CLKb, respectively. A first clock signal CLK1 is supplied to the first clock terminal CLKa of odd-numbered stages in the first scan driver 310, and a second clock signal CLK2 is supplied to the second clock terminal CLKb. In contrast to this, the second clock signal CLK2 is supplied to a first clock terminal CLKa of even-numbered stages, and the first clock signal CLK1 is supplied to a second clock terminal CLKb of the even-numbered stages.

Id., ¶ [0074]; *see also* ¶ [0090].

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As detailed earlier (in, e.g., the discussion of Claim 1 and, e.g., the discussion of claim sub-element [15-c-3]), the top terminal of a stage circuit is the first input terminal, the CLKa terminal is the second input terminal, and the CLKb terminal is the third input terminal.

544. Thus, the second input terminals of odd stage circuits receive a first clock signal and the third input terminals of odd stage circuits receive a second clock signal, and the second input terminals of even stage circuits receive the second clock signal and third input terminals of even stage circuits receive the first clock signal.

545. Thus, Shin and Shin in combination with Sasaki render obvious this claim of the ’593 patent.

14. Dependent Claim 19

546. As an initial matter, Claim 19 depends from Claim 18, which depends from Claim 17, which depends from Claim 15; as was shown above, Claim 15, Claim 17, and Claim 18 of the ‘593 patent are disclosed by Shin and Sasaki.

547. Claim 19 further requires that “the first clock signal and the second clock signal have the same period and have phases that do not overlap.” This behavior is depicted as part of Figure 12 of Shin.

548. This claim is identical to an element of Claim 3 of the ’593 patent – which was discussed earlier (in Section XII.B.4). Thus, Shin in combination with Sasaki renders obvious this claim of the ’593 patent.

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15. Dependent Claim 20

549. As an initial matter, Claim 20 depends from Claim 18, which depends from Claim 17, which depends from Claim 15; as was shown above, Claim 15, Claim 17, and Claim 18 of the ’593 patent are disclosed and Shin and Sasaki.

550. Claim 20 further requires:

> wherein the first driver includes:
>
> a first transistor between the first input terminal and the second node, the first transistor having a gate electrode coupled to the second input terminal; and
>
> a second transistor and a third transistor serially positioned between the second node and the first power supply,
>
> wherein a gate electrode of the second transistor is coupled to the third input terminal, and
>
> wherein a gate electrode of the third transistor is coupled to the first node.

551. This claim is identical to Claim 6 of the ’593 patent – which was discussed earlier (in Section XII.B.7).

552. Thus, Shin in combination with Sasaki renders obvious this claim of the ’593 patent.

16. Dependent Claim 22

553. As an initial matter, Claim 22 depends from Claim 18, which depends from Claim 17, which depends from Claim 15; as was shown above, Claim 15, Claim 17, and Claim 18 of the ’593 patent are disclosed by Shin and Sasaki.

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554. Claim 22 further requires:

> wherein the second driver includes:
>
> a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and
>
> a seventh transistor between the first node and a second power supply, the second power supply having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal.

555. This claim is identical to Claim 8 of the ’593 patent – which was discussed earlier (in Section XII.B.8).

556. Thus, Shin in combination with Sasaki render obvious this claim of the ‘593 patent.

17. Dependent Claim 25

557. As an initial matter, Claim 25 depends from Claim 18, which depends from Claim 17, which depends from Claim 15; as was shown above, Claim 15, Claim 17, and Claim 18 of the ’593 patent are disclosed by Shin in combination with Sasaki.

558. Claim 25 further requires that “the scan signal of the previous stage circuit or the start signal supplied to the first input terminal overlaps the clock signal supplied to the second input terminal.”

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559. Because Claim 25 contains an "or," it can be satisfied in form of either "the scan signal of the previous stage circuit … overlaps the clock signal supplied to the second input terminal" or "the start signal supplied to the first input terminal overlaps the clock signal supplied to the second input terminal."

560. The second of these two possible renditions of Claim 25 is nearly-identical to Claim 5 ("… "the start signal is supplied to overlap the first clock signal.") – which was discussed earlier (in Section XII.B.6).

561. For this reason alone, Shin and Shin in combination with Sasaki render obvious this claim of the '593 patent.

562. For completeness, the first of these two possible renditions of Claim 25 ("the scan signal of the previous stage circuit … overlaps the clock signal supplied to the second input terminal") should also be considered.

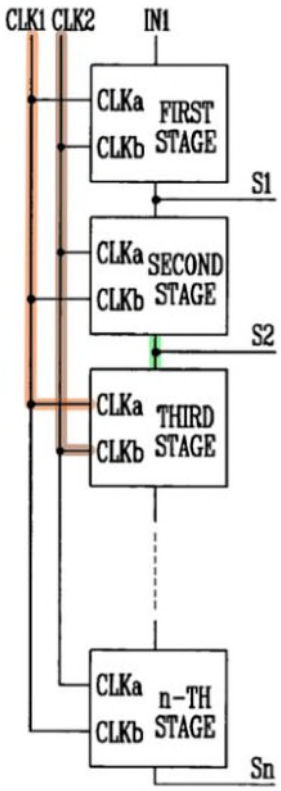
563. Most of what satisfies this rendition of Claim 25 was already provided in the discussion associated with Claim 2 (above, in Section XII.B.3). In particular, it was first shown there that, other than is the case with the first stage, subsequent stages in Shin's stage circuit receive the output signal of the previous stage (which is also the scan signal of that stage) as the input signal at the input terminal of that stage:

> [E]ach stage receives the first input signal IN1 or *an output voltage gi of a previous stage*…

Ex. 1005, ¶ [0075] (emphasis added).

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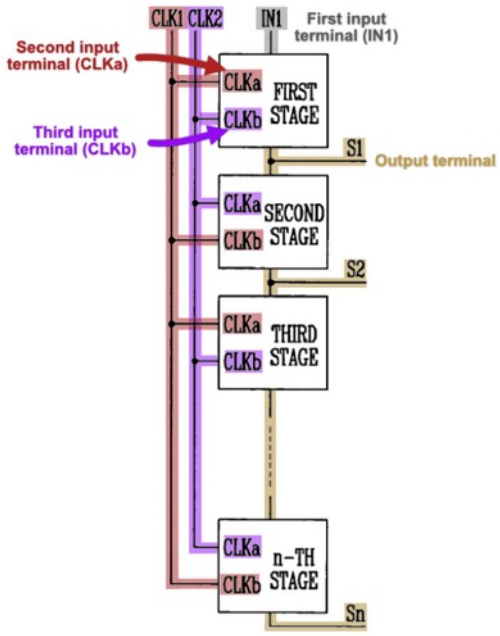
564. Further, it was also shown that with respect to the third stage of the stage circuit, the first input signal of the third stage receives the output signal of the previous (second) stage:



Id., Fig. 10 (annotated). As was detailed earlier, the output of a particular stage and the scan signal of a particular stage are the same thing – as this figure once again makes clear.

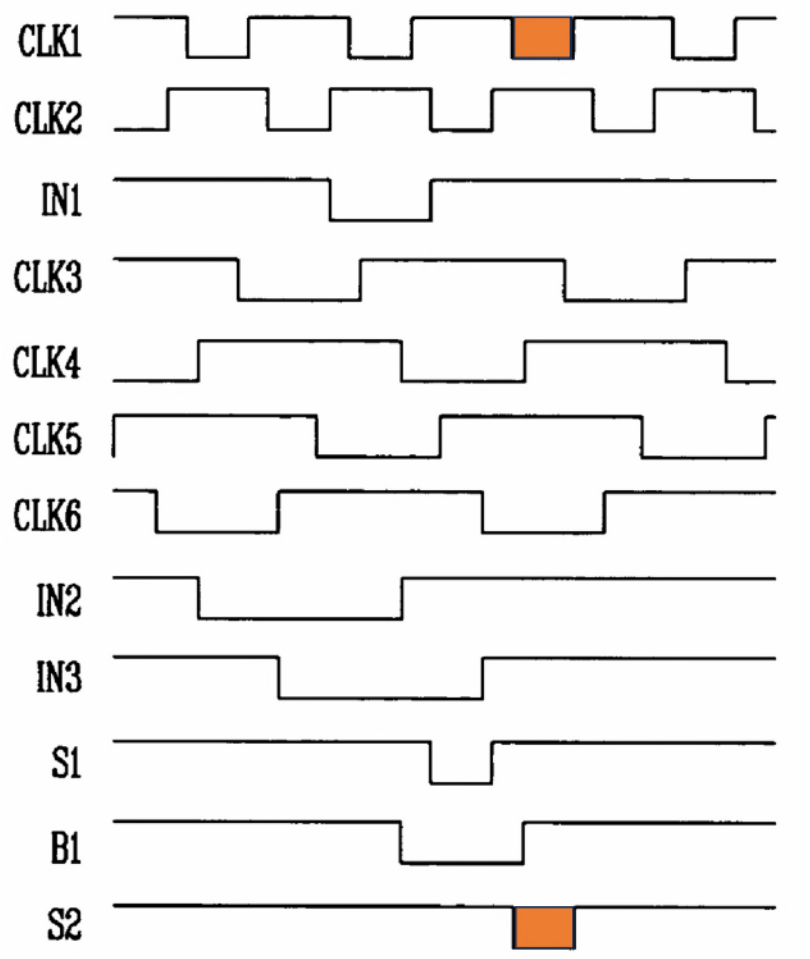
565. In addition, it was also shown earlier (in the discussion of Claim 2) that the second input terminal of the third stage receives the clock signal CLK1:

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Id., Fig. 10 (annotated). The relationship between the clock signal supplied to the second input terminal of the third stage and the scan signal of the previous stage can be elucidated via an examination of an annotated version of Figure 9 of Shin:

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Id., Fig. 9 (annotations added). Note that like the "start signal" (as explained in Section XII.A.3), the "scan signal of the previous stage circuit" (here as part of signal S2) exists only as a pulse with a low (active) voltage. As can readily be seen via the annotations added to this timing diagram, with respect to the third stage, the clock signal (CLK1) overlaps the scan signal of the previous stage circuit (i.e., S2) – as this output signal S2 is supplied by the second stage to the input terminal of the third stage.

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566. Thus, for this additional reason, Shin in combination with Sasaki renders obvious this claim of the ’593 patent.

C. Ground 3: Shin and Sasaki in Combination with Jeong Renders Obvious Claims 7 and 21

567. As will be discussed below, it is my conclusion and opinion that Claims 7 and 21 of the ’593 patent are rendered obvious by Shin and Sasaki, in combination with Jeong and the knowledge of a POSITA.

1. Motivation to Combine Shin and Sasaki with Jeong

568. Before going into the details, some of the generalized aspects of the motivation to combine Jeong with Shin (or Shin in combination with Sasaki) should be considered. I also discuss additional aspects in my specific claim analyses themselves.

569. As an initial matter, Shin and Jeong both involve shift register circuitry that forms the basis of a scan driver used in the operation of active-matrix displays. Thus, a POSITA would have been aware of both of these references, and would have studied the advantages of these two respective designs. Further, field-effect transistors, circuits based on them, and the use of such circuits for the drivers in an active-matrix display, were well known in the art – and had been well known for years prior to 2012. Therefore, a POSITA at the time of the alleged inventions of the ’593 patent would have had extensive knowledge about such circuits and their usage. Accordingly, it would have been sensible for a POSITA to integrate

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compatible circuits, so as to garner respective advantages of two or more references. Further, because the circuit design and circuit operation principles were already well known in the art, such combinations would have yielded predictable results.[23]

570. Further, a POSITA would have been motivated to combine Shin (or Shin combined with Sasaki) with Jeong because, as noted above, both involve the use of shift registers to provide scan drivers for use in pixel-based displays. Both Shin (and Shin combined with Sasaki) and Jeong use field-effect transistors, and in each reference the circuits disclosed use only one species (pMOS) of field-effect transistor. Further, the similarity of the functions and designs of Shin (or Shin in combination with Sasaki) and Jeong would have further confirmed to a POSITA that combining the teachings of these two references would involve straightforward modifications (as discussed just above) – with both predictable outcomes and a reasonable expectation of success.

571. Finally, a POSITA would have observed that Shin's outputting unit (or the outputting unit of Shin in combination with Sasaki) and Jeong's outputting unit

[23] As per some of the references cited in Section VII.A.1, this knowledge predates the '593 patent by an extensive period of time – with one of the references cited going back to 1967.

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share what are essentially the same components in the same configuration, making the combination simple and highly predictable.

2. Dependent Claim 7

572. As an initial matter, Claim 7 depends from Claim 2, and Claim 2 depends from Claim 1; as was shown above (in Sections XII.B.2 and XII.B.3), Claim 1 and Claim 2 of the ’593 patent are rendered obvious by Shin and Sasaki.

573. Claim 7 further requires:

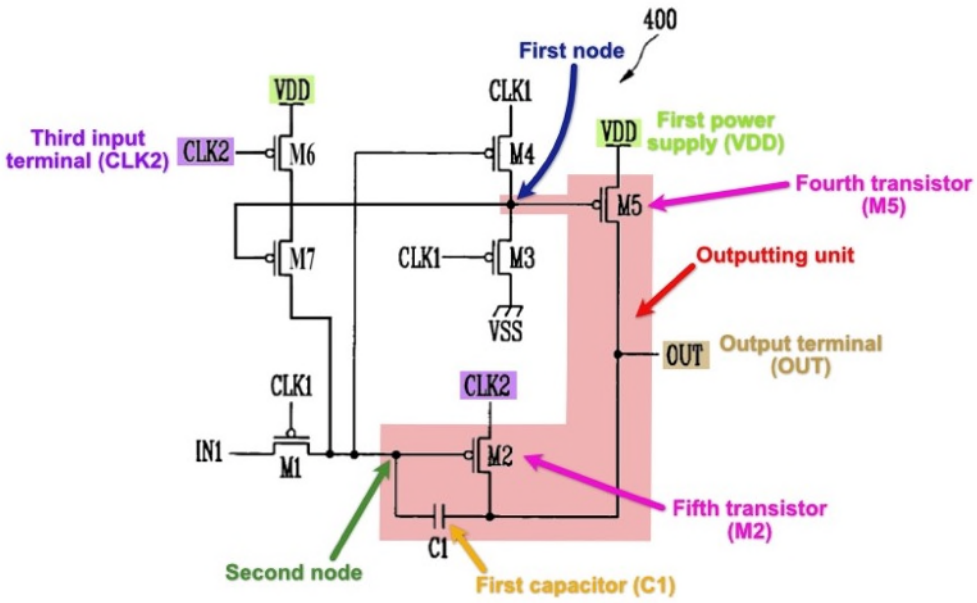
> wherein the outputting unit includes:
>
> a fourth transistor between the first power supply and the output terminal, the fourth transistor having a gate electrode coupled to the first node;
>
> a fifth transistor between the output terminal and the third input terminal, the fifth transistor having a gate electrode coupled to the second node;
>
> a first capacitor between the second node and the output terminal; and
>
> a second capacitor between the first node and the first power supply.

As will be shown here, Shin (or Shin combined with Sasaki) combined with Jeong and the knowledge of a POSITA renders obvious this claim of the ’593 patent.

574. Simple inspection of the circuitry of both Figure 11 of Shin and of the combined embodiment presented above shows that this circuitry contains all of the elements recited in Claim 7, arranged in the configuration that is recited in Claim 7

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– with the exception of the second capacitor, which is not present in these two instances of circuitry.

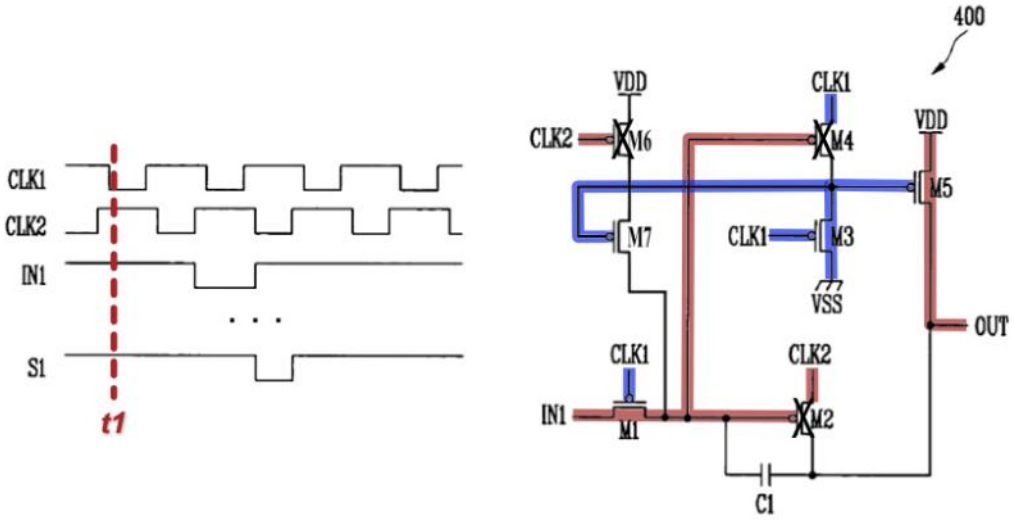


A POSITA examining this circuitry would reach several conclusions – since these conclusions are well-known in the art.

575. First, a POSITA would recognize that the first node will be electrically isolated whenever the two transistors which provide electrical access to this node (M3 and M4) are both turned off.

576. To begin, consider a period in the timing diagram where transistor M3 is turned on and transistor M4 is turned off:

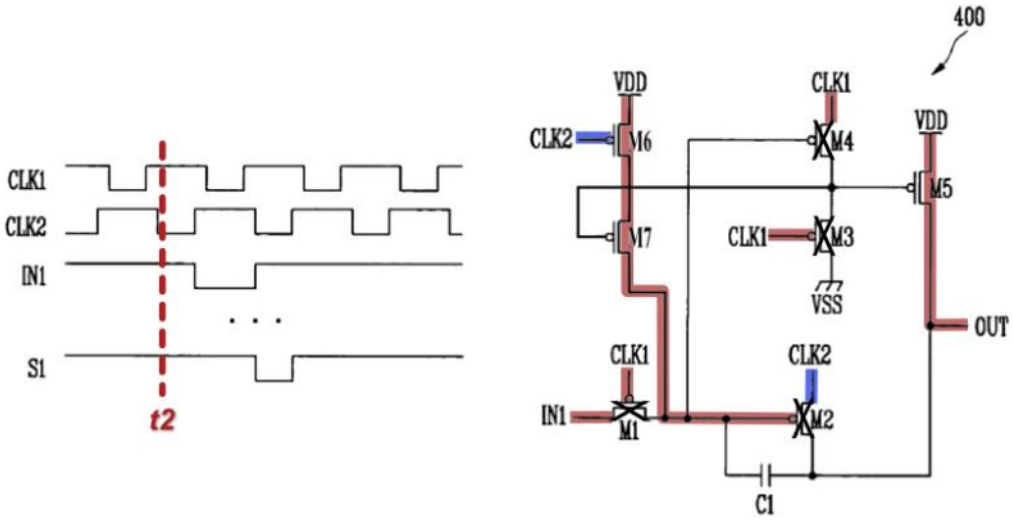
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During the period immediately following time point ***t1***, as just mentioned, transistor M4 is turned off and M3 is turned on; this connects the low power supply voltage VSS to the first node, which (among other things) is connected to the gate transistor M5; in turn, this turns on transistor M5 – which connects the high power supply voltage VDD to the output OUT.

577. Now, consider what happens when transistor M3 is turned off, and transistor M4 remains off:

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During the time period immediately following time period ***t2***, both transistors M3 and M4, as just described, are turned off; this leaves the first node (again, which is connected to the gate of transistor M5) in retention of the low power supply voltage VSS that was supplied to it just before – but now, that node is floating. During this time, Shin still intends for the low power supply voltage on the first node (and on gate of transistor M5) to remain in place – so that transistor M5 continue to be turned on, so that the high power supply voltage VDD will continue to be provided to the output terminal OUT.

578. However, there is a problem with this floating node – and, as a second conclusion that would be reached, a POSITA would also understand that the amount of charge stored at the node would determine the isolated voltage at that node using the simple and well-known equation

$$Q = CV,$$

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where Q is the charge on the node, V is the resulting voltage at the node, and C is the capacitance at the node. For example, if the first capacitor (C1) were not there, then the capacitance would be supplied only by the wiring and transistors[24] to which the node is connected; however, as wiring and transistors (and the parasitic capacitances of any adjacent transistors) hold very little charge, they provide very little capacitance – and thus, the resulting voltage value will be based upon a very small amount of charge.

579. This can be problematic, since perturbations in the amount of charge (for example, due to electromagnetic interference (EMI) or interline crosstalk during digital switching events) may cause sizeable changes in the voltage on the node; these types of signal integrity issues are undesirable. Therefore, a POSITA would be motivated to seek methods of making the circuitry of Shin and Sasaki more robust against a problem of this sort.

580. In addition, the "isolation" of this node is being provided by turning off all the transistors that provide electrical connection(s) to that node when any one of them is turned on – and, as described above, examination of the two instances of circuitry above indicates that there are two such transistors (M3 and M4) that provide electrical connections to the first node, and the first node is isolated when both of

[24] All field-effect transistors include small parasitic capacitances; usually, these capacitances are so small that they are not explicitly included in the circuit diagram.

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these transistors are turned off. However, a transistor does not turn off perfectly – and some off-state leakage current will be present. If the voltage at the isolated first node is defined by a very small amount of charge, then that charge will leak away very quickly via the imperfect off-state of the transistors – and the voltage will change quickly with time, and may even quickly reach the high (VDD) voltage as its inevitable endpoint.

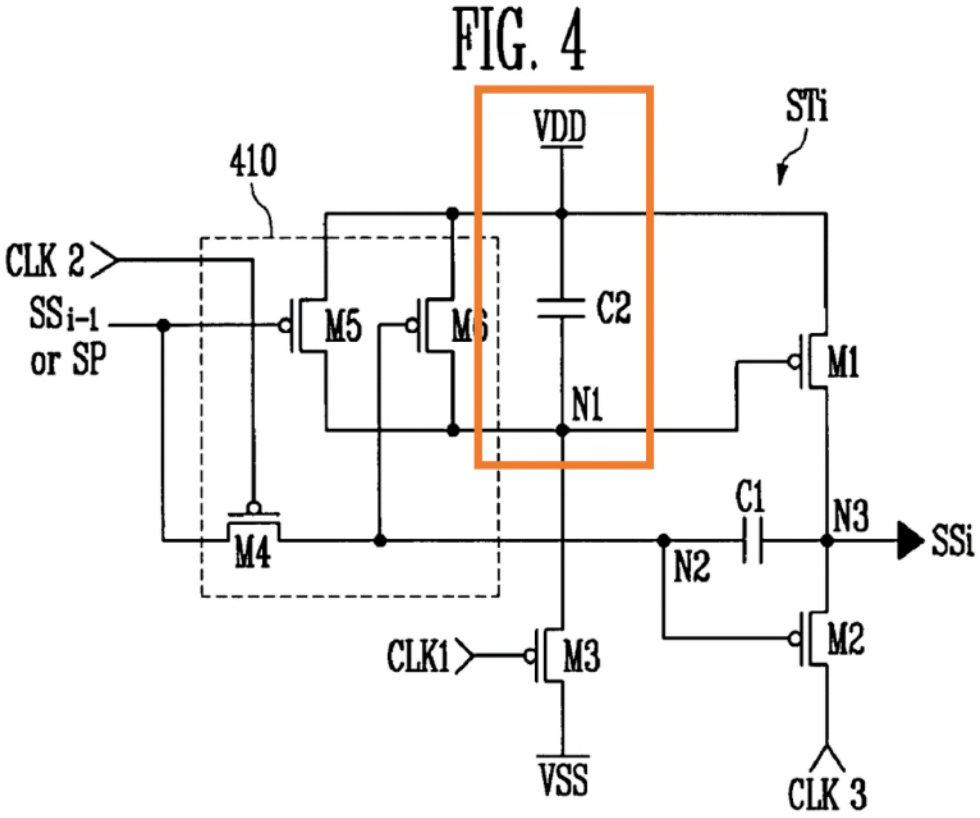
581. As a POSITA would thus know, the voltage at this node would be made more robust (i.e., it would be able to hold the isolated voltage value more stably against upsets like EMI, and would take a long time to charge to a high voltage through the imperfect off-state transistors and thus would retain the isolated voltage much longer) if the capacitance at the node could be increased. This is actually quite easily done – by adding a capacitor to the isolated node, so that the amount of charge used to create the voltage at the node is much larger; as can readily been seen from the equation presented above, for the same voltage, a larger capacitance would hold a proportionately larger charge.

582. Thus, a POSITA looking at the circuitry presented above would realize that these vulnerabilities exist. Thus, it would be a relatively straightforward decision to conclude that the first node in the circuitry presented above should have a capacitor included and connected to it – for the reasons just cited above.

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583. One simple method for adding a capacitor to accomplish this would be to connect that capacitor between the first node (the required connection) and a DC power supply voltage (the optional-location-choice connection).

584. A simple example of this insertion is provided by Jeong, at Figure 4:



Ex. 1007, Fig. 4 (annotation added). As can be seen by inspection, when the transistors M5 and M6 are turned off, the node N1 is electrically isolated – and will retain the charge (and thus the corresponding voltage) that is present there. For the reasons detailed above (i.e., increasing the robustness of the voltage that is present at the node N1), the capacitor C2 is added. As Jeong explains,

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> The second capacitor C2 may be coupled between the first power supply VDD and the first node N1. The second capacitor C2 may *function to reduce a variation of a voltage*, which may be applied to the first power supply VDD or the first node N1.

Id., ¶ [0057] (emphasis added).

This is a description of the enhanced robustness of the voltage present at the node N1, consistent with what was discussed above.

585. In addition, another prior art reference, Moon (Ex. 1020) also explicitly recognizes these vulnerabilities – and explicitly describes the inclusion of two capacitors at the two relevant nodes (Q and QB) to mitigate these problems:

> A first capacitor CQ may be connected between the [second] node Q and an input line of the low-level driving voltage VSS for eliminating noise at the [second] node Q. Similarly, a second capacitor CBQ may be connected between the [first] node QB and the input line of the low-level driving voltage VSS for eliminating noise at the [first] node QB.

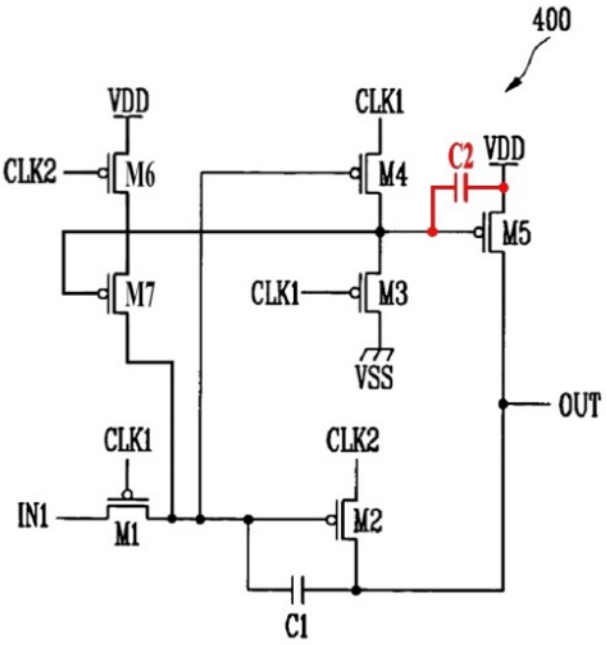
Ex. 1020, ¶ [0053].

586. It is clear from the above discussion (as would be clear to a POSITA) that by "eliminating noise," Moon is referring to increasing the charge on each node by increasing the capacitance at those nodes – to make their charge states more robust against upsets (such as EMI (which, as described above, is a well-known form of noise) and interline crosstalk during digital switching events (which is also a well-known form of noise)). In the same manner as that just shown with respect to Jeong,

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Moon is describing enhanced robustness of the voltage present at the nodes Q and QB, consistent with what was discussed above.

587. As an example, this capacitor could be added to the circuitry of the combined embodiment presented above – in the following manner:



(Highlighted added capacitor in red.) This capacitor is connected between the first node and the first power supply.

588. In operation, capacitor C2 would be charged during the period immediately following time point t1 – a period of time that was discussed above (wherein the lower power supply voltage VSS is provided to the first node in the same way as was described there). When the first node is charged up, the endpoint voltage (VSS) will not change from what was discussed earlier (as long as enough time is allowed for the charging-up of the first node to reach completion). Then,

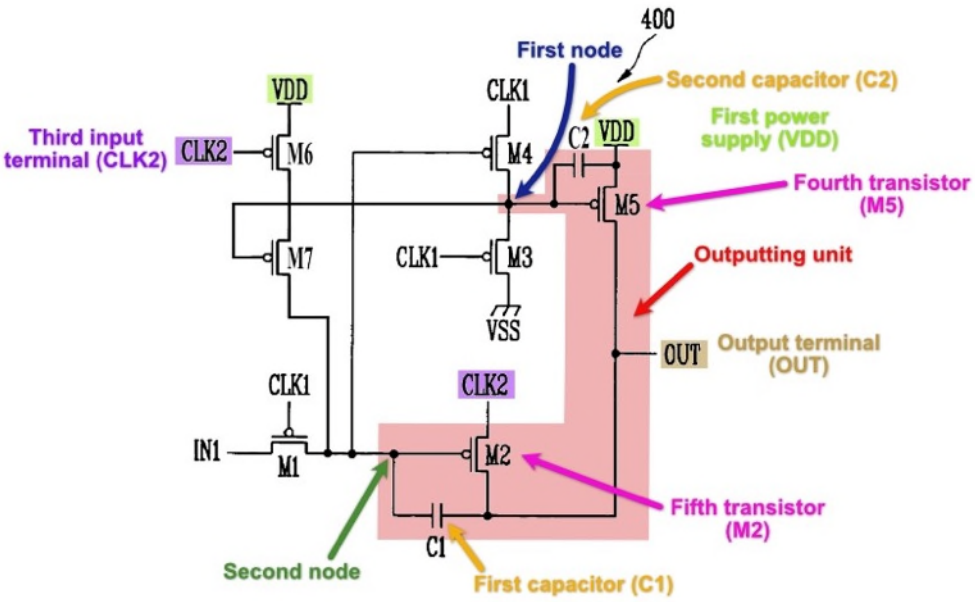
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during the time period immediately following time point t2 (and also discussed above), the second node will be floating – but will retain the voltage VSS at that node; again, this is at least the initial condition of the situation what was also discussed above.

589. However, as per the discussion above regarding the relationship among charge, capacitance, and voltage (i.e., $Q = CV$), here – due to the larger capacitance (C) – the voltage (V – which, here, is the low power supply voltage VSS) will involve a larger amount of charge (Q). Therefore, when the first node is isolated and floating (i.e., when as described above, transistors M3 and M4 are both turned off), the inclusion of capacitor C2 will provide the benefits (in terms of signal integrity and voltage retention) that were discussed above.

590. When this second capacitor is added, the combined embodiment now includes the "second capacitor [C2] between the first node and the first power supply [VDD]" – as required by Claim 7:

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591. Thus, Shin in combination with Sasaki, in view of Jeong and the knowledge of a POSITA, renders obvious this claim of the ’593 patent.

3. Dependent Claim 21

592. As an initial matter, Claim 21 depends from Claim 18, which depends from Claim 17, which depends from Claim 15; as was shown above (in Sections XII.B.10, XII.B.12, and XII.B.13), Claim 15, Claim 17, and Claim 18 of the ‘593 patent are disclosed by Shin in combination with Sasaki.

593. This claim is identical to Claim 7 of the ’593 patent – which was discussed just above (in Section XII.C.2).

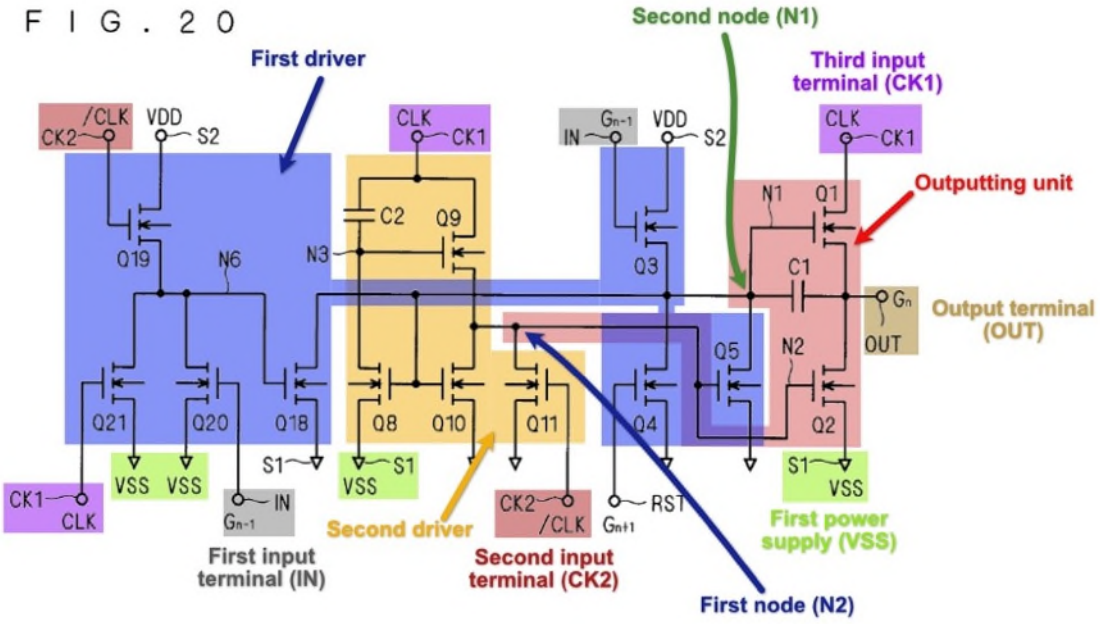
594. Thus, Shin in combination with Sasaki, in view of Jeong and the knowledge of a POSITA, renders obvious this claim of the ’593 patent.

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D. Ground 4: Tobita Renders Obvious Claims 1, 2, and 15-19

595. As will be discussed below, it is my conclusion and opinion that, when viewed and considered in light of the knowledge possessed by a POSITA Claims 1, 2, and 15-19 of the ’593 patent are rendered obvious by Tobita (Ex. 1006).

596. Before beginning a discussion of the analysis, it will be helpful to first provide an annotated version of Figure 20 of Tobita – with the annotations indicating the identification of the specific structures recited in the claims of the ’593 patent, as mapped to Tobita.



1. Independent Claim 1

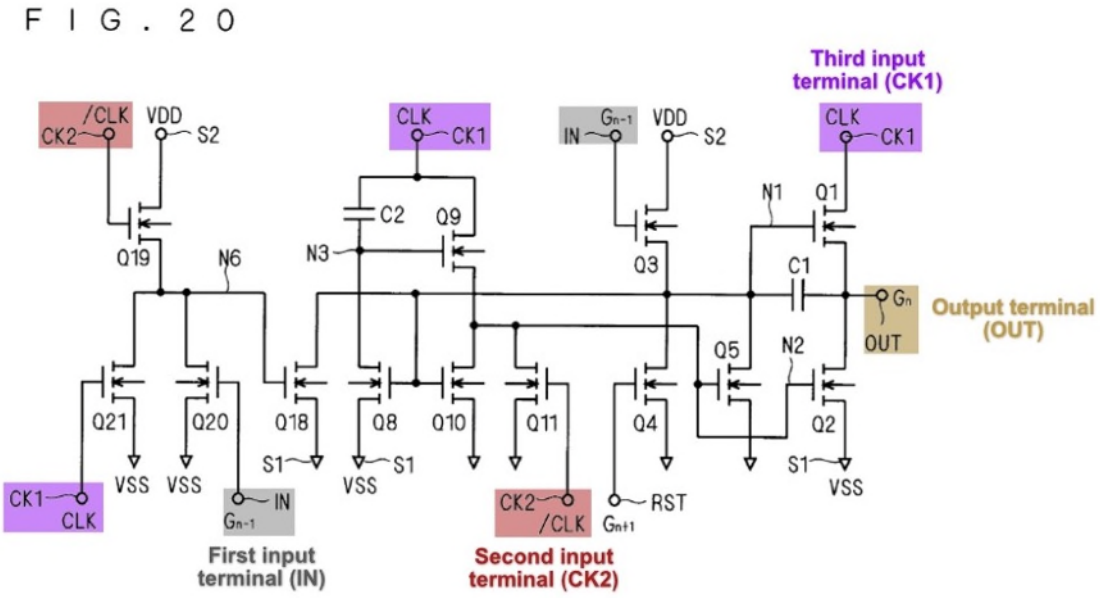
597. It is my conclusion and opinion that Claim 1 of the ’593 patent is rendered obvious by Tobita.

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a. [1-pre]: "A stage circuit having a first input terminal, a second input terminal, a third input terminal, and an output terminal, the stage circuit comprising:"

598. As an initial matter, I will be offering no opinion regarding whether or not the preamble of Claim 1 is limiting. I have been instructed by counsel for Petitioner to offer an opinion as to whether or not the prior art discloses or renders obvious the preamble, regardless of whether or not the preamble is limiting.

599. Tobita discloses the preamble of Claim 1 of the '593 patent; this can be seen readily via annotated versions of Figure 20 of Tobita:



Ex. 1006, Fig. 20 (annotations added).

600. As can be seen in this annotated figure, Tobita discloses a first input terminal, a second input terminal, a third input terminal, and an output terminal – all of which are part of a stage circuit. In more detail, Tobita's circuit includes a "first

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clock terminal CK1," an "input terminal IN," a "second clock terminal CK2," and an "output terminal OUT." *Id.*, ¶¶ [0109], [0111], [0115]; *see also id.*, ¶¶ [0173], [0178] (describing input terminals IN, CK1, and CK2).

601. Thus, Tobita discloses the preamble of Claim 1 of the '593 patent.

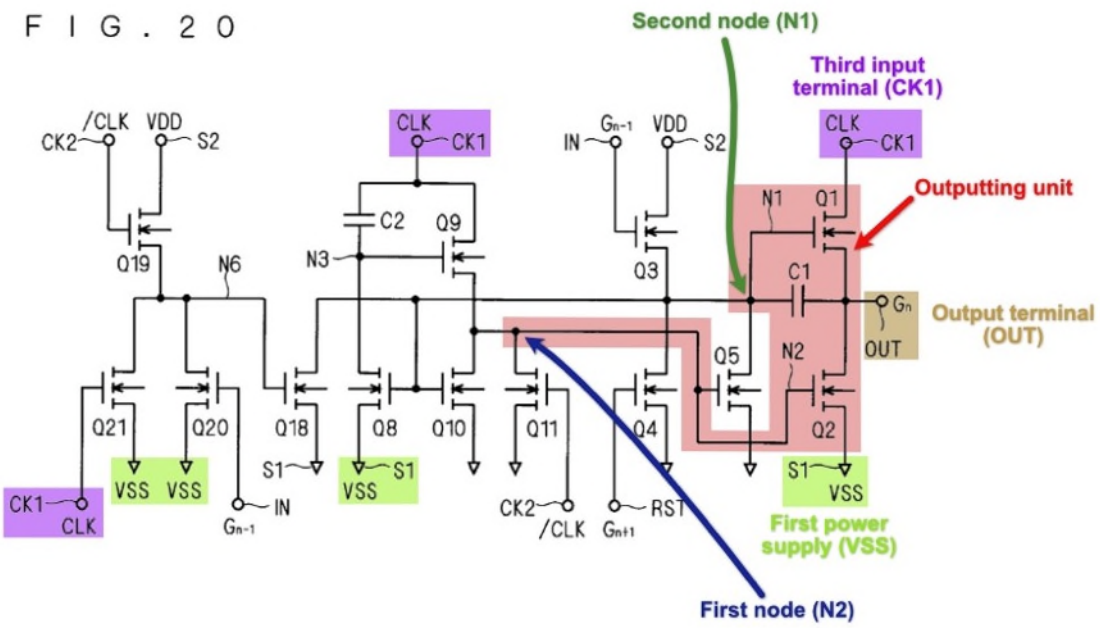
b. [1-a]: "an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node:"

602. Claim element [1-a] is rather long – and thus the analysis will be simpler to explain if this claim element is broken up into sub-elements.

i. [1-a-1]: "an outputting unit having a first node and a second node,"

603. Tobita discloses this claim sub-element; this is evident via an annotated version of Figure 20 of Tobita:

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Ex. 1006, Fig, 29 (annotations added). The node labeled "N2" is the first node, and the node labeled "N1" is the second node – while the "outputting unit" is a shown via the annotation box-bounding in red. In more detail, according to Tobita, the two transistor Q1 and Q2 supply signals to "output terminal OUT" (the claimed output terminal): "Q1 … suppl[ies] the clock signal input to the first clock terminal CK1" (the claimed third input terminal) and "Q2 … suppl[ies] the low supply voltage VSS" (the claimed first power supply). *Id.*, ¶ [0109]. As can be seen in the annotated figure above, the gate electrodes of Q1 and Q2 are connected (respectively) to—and thus controlled by—Tobita's node N1 (the claimed second node) and the node N2 (the claimed first node).

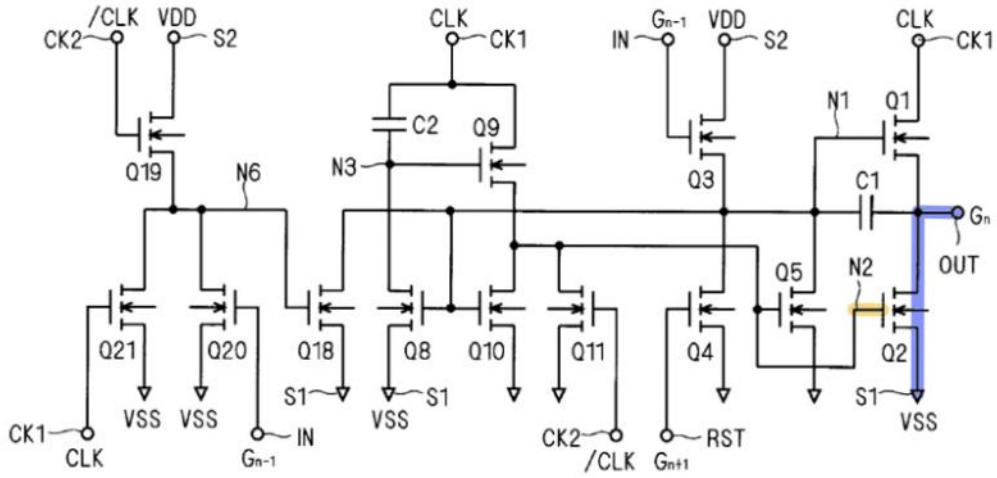
604. Thus, Tobita discloses this claim sub-element of this claim element of Claim 1 of the '593 patent.

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ii. [1-a-2]: "the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node"

605. Tobita discloses this claim sub-element; this is evident via an annotated version of Figure 20 of Tobita:

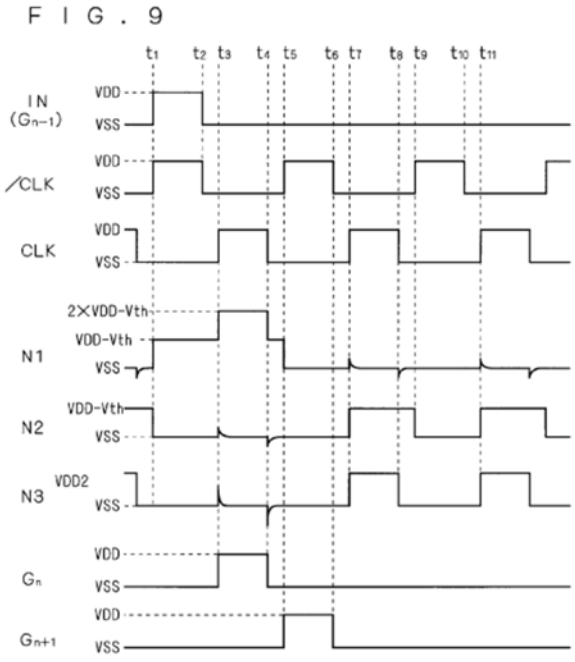
FIG. 20



Ex. 1006, Fig. 20 (annotations added). As the annotations show, when an appropriate (i.e., turn-on) voltage is applied at the first node (the node labeled "N2"), transistor Q2 will turn on; this will connect the first power supply voltage (VSS) to the node of the output terminal ("OUT") – and thus the voltage of the first power supply connection (VSS) is supplied to the output terminal ("OUT"). (On the other hand, when a turn-on voltage is not applied at the first node ("N2"), transistor Q2 will not turn on – and the voltage of the first power supply connection (VSS) is not supplied to the output terminal.)

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606. The functionality described above is confirmed by Tobita's circuit timing diagrams, including the one provided in Figure 9. While Tobita does not include a diagram specific to Figure 20, Tobita does so for Figure 7. Given that Figures 7 and 20 share many common components and functionalities (*compare* Exs. 1006, Figs. 7, 20), a POSITA would have understood that the timing diagram of Figure 9 applies not only to Figure 7 but also Figure 20. *Id.*, ¶¶ [0026]-[0028], [0117], [0195].



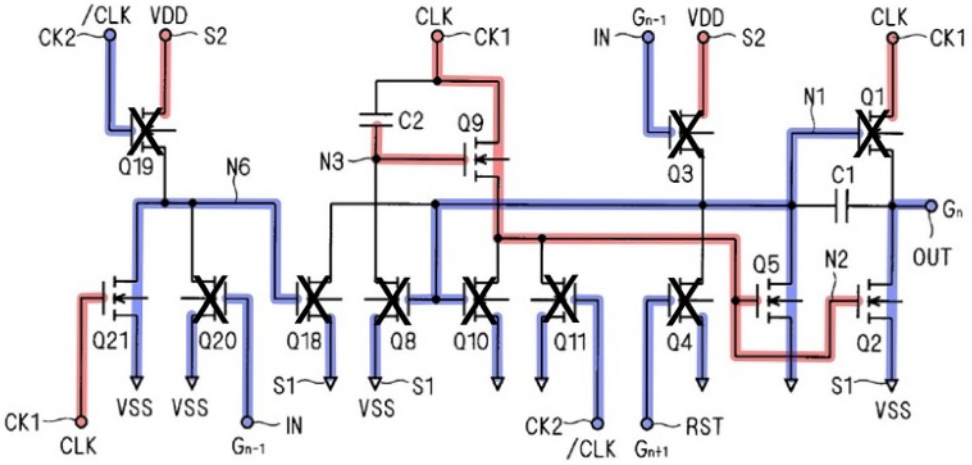
Id., Fig. 9, ¶¶ [0120]-[0137].

607. Figure 20 of Tobita employs n-type transistors, which are turned on by high signals (red below) and turned off by low signals (blue below). In this

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annotated figure, period t_7-to-t_8 is shown – with high signals shown in red and low signals shown in blue:

F I G . 2 0



Ex. 1006, Fig. 20 (annotations added; some transistors are marked with a large "X" to indicate that they are turned off in this situation – while those not so-marked serves to indicate that they are turned on in this situation.) During t_7-to-t_8 (and later period t_8-to-t_9), node N2 is high while node N1 is low. *Id.*, ¶¶ [0131]-[0133]. Q1 is off and the low voltage of VSS is coupled to OUT through Q2. *Id.*, ¶¶ [0132]-[0135].

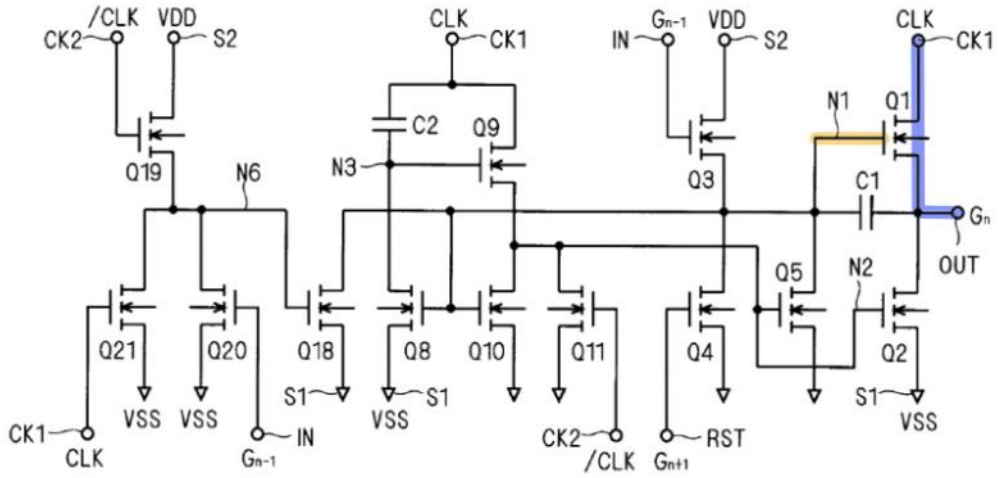
608. Thus, Tobita discloses this claim sub-element of this claim element of Claim 1 of the '593 patent.

iii. [1-a-3]: "and a signal of the third input terminal to the output terminal according to a voltage applied to the second node:"

609. Tobita discloses this claim sub-element; this is evident via an annotated version of Figure 20 of Tobita:

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F I G . 2 0

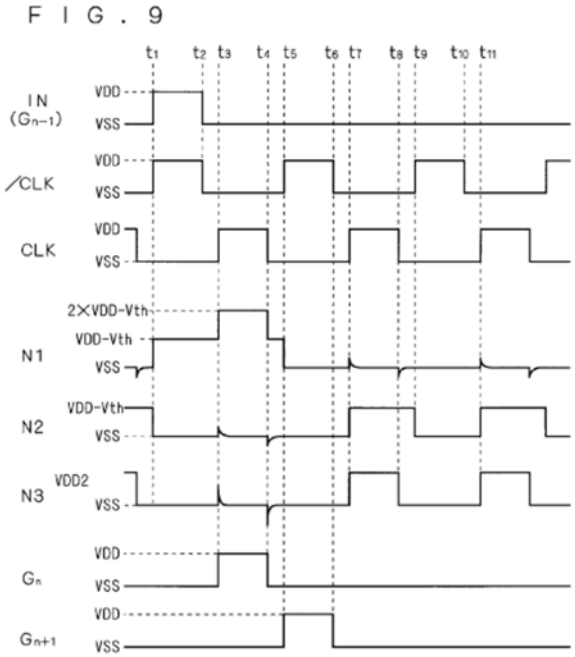


Ex. 1006, Fig. 20 (annotations added). As the annotations show, when an appropriate (i.e., turn-on) voltage is applied at the second node (the node labeled "N1"), transistor Q1 will turn on; this will connect the signal of the third input terminal ("CK1") to the node of the output terminal ("OUT") – and thus the signal of the third input terminal ("CK1") is supplied to the output terminal ("OUT"). (On the other hand, when a turn-on voltage is not applied at the second node ("N1"), transistor Q1 will not turn on – and thus the signal of the third input terminal (CK1) is not supplied to the output terminal ("OUT").)

610. Once again, the functionality described above is confirmed by Tobita's circuit timing diagrams, including the one provided in Figure 9. As described above, while Tobita does not include a diagram specific to Figure 20, Tobita does so for Figure 7. Given that Figures 7 and 20 share many common components and functionalities (*compare* Exs. 1006, Figs. 7, 20), a POSITA would have understood

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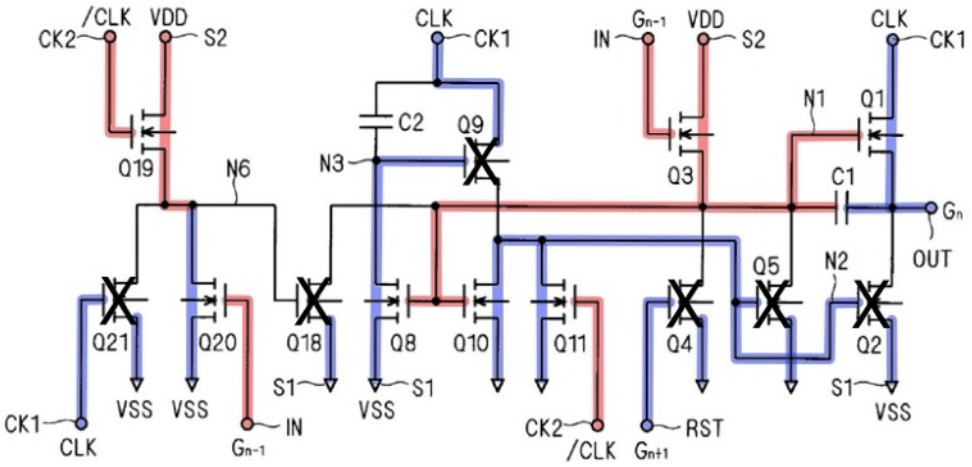
that the timing diagram of Figure 9 applies not only to Figure 7 but also Figure 20. *Id.*, ¶¶ [0026]-[0028], [0117], [0195].



Id., Fig. 9, ¶¶ [0120]-[0137].

611. Figure 20 of Tobita employs n-type transistors, which are turned on by high signals (red below) and turned off by low signals (blue below). In this annotated figure, period t_1-to-t_2 is shown – with high signals shown in red and low signals shown in blue:

F I G . 2 0



Id., Fig. 20 (annotations added; some transistors are marked with a large "X" to indicate that they are turned off in this situation – while those not so-marked serves to indicate that they are turned on in this situation.) During period t_1-to-t_2 (and later periods t_2-to-t_3 and t_3-to-t_4) node N2 is low, turning off transistor Q2. *Id.*, ¶¶ [0120]-[0121]. Node N1 is high, turning on transistor Q1. *Id.* Thus, CLK is transferred to OUT. *Id.*

612. Thus, Tobita discloses this claim sub-element of this claim element of Claim 1 of the '593 patent.

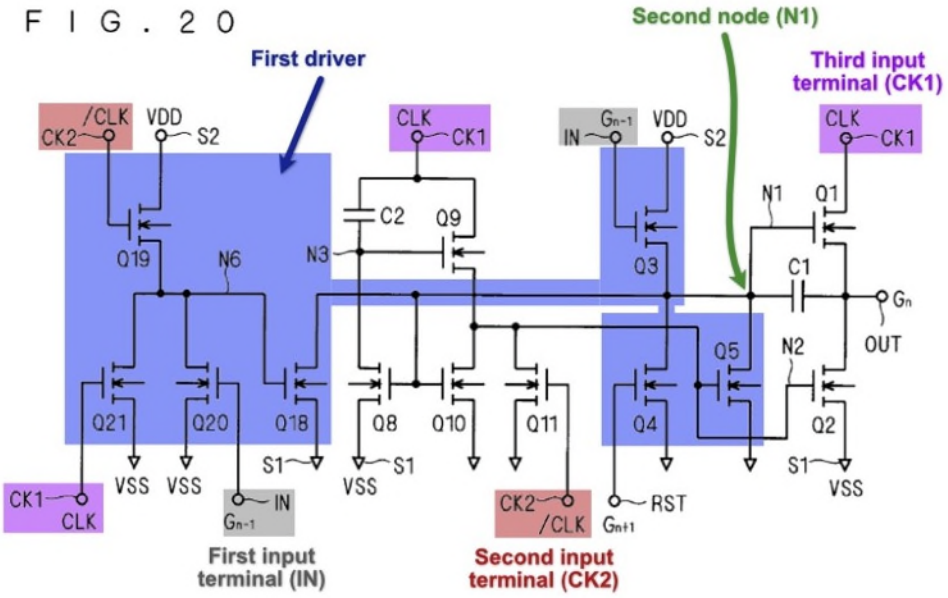
iv. Claim Element [1-a] Summary

613. As just demonstrated, Tobita discloses claim sub-elements [1-a-1], [1-a-2], and [1-a-3] of the '593 patent; thus, Tobita discloses claim element [1-a] of Claim 1 of the '593 patent.

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c. [1-b]: "a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal; and"

614. Tobita discloses this claim element of the '593 patent; this is evident via an annotated version of Figure 20 of Tobita:



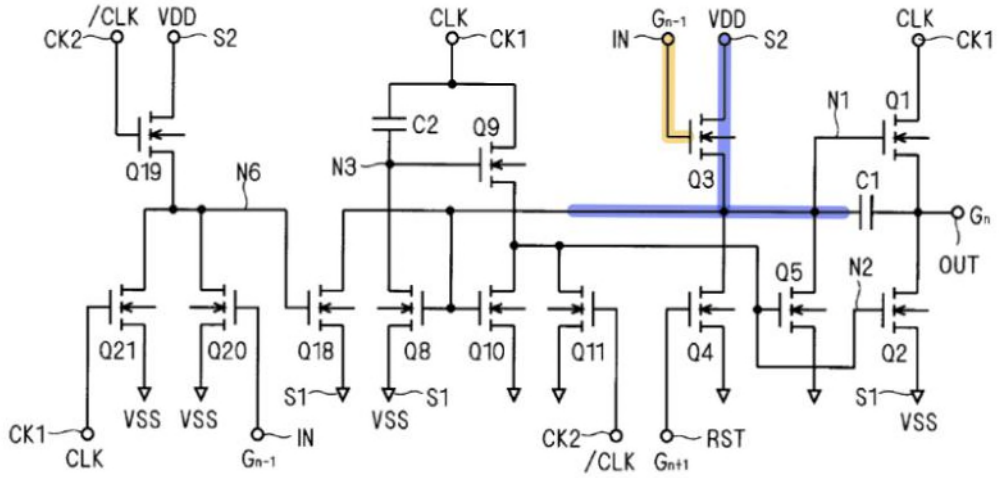
Ex. 1006, Fig. 20 (annotations added); *see also id.*, ¶¶ [0111], [0173]. In the Tobita figure above, the "first driver" is identified using blue box-bounding; as can be seen there are inputs of the first input terminal, the second input terminal, and the third input terminal to the first driver.

615. Further, the voltage on the second node ("N1") is controlled in accordance with the signals of the first input terminal, the second input terminal, and the third input terminal – as will be shown by the annotations to the following versions of Figure 20 of Tobita.

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616. The first driver is able to control the voltage of the second node in accordance with signal of the first input terminal as described here.

F I G . 2 0

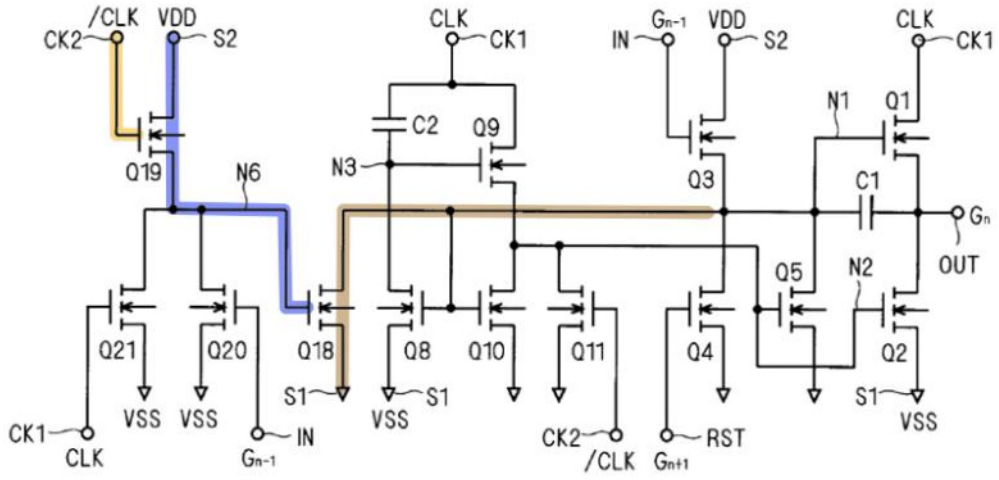


Id., Fig. 20 (annotations added). As shown, when the first input signal (G_{n-1}) at the first input terminal (IN) is pulled to a voltage that causes transistor Q3 to turn on, the second node (N1) is pulled to the high voltage level VDD. (On the other hand, when transistor Q3 is not turned on, the high voltage VDD is not supplied to the second node (N1).) Further, Tobita describes this operation – in which, as outlined above, signal G_{n-1} is received at IN (Tobita's first input terminal) and controls the on/off operation of transistor Q3, which in turn contributes to the control of the voltage of node N1 (the claimed second node) by allowing a high VDD signal to be provided to node N1 during certain periods of operation. *See, e.g.*, *id.*, ¶¶ [0120]-[0121], [0125].

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617. The first driver is able to control the voltage of the second node in accordance with signal of the second input terminal as shown here..

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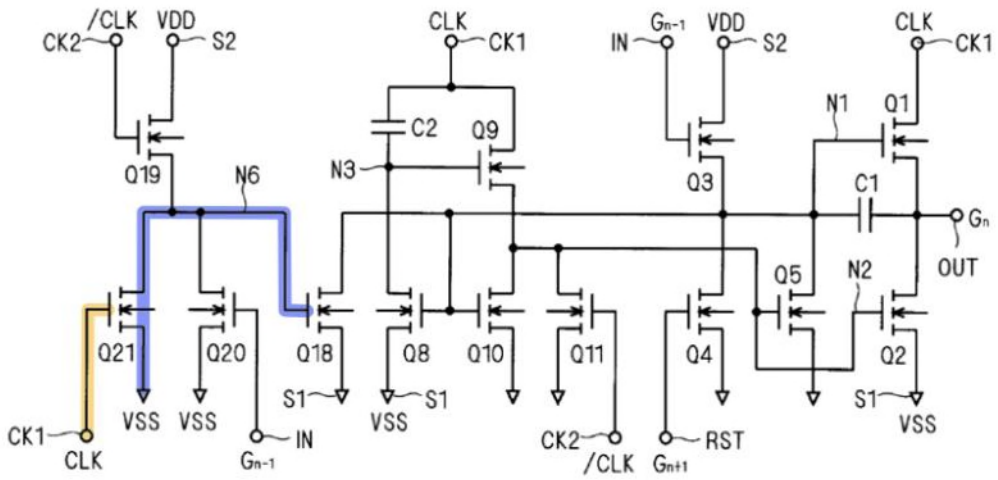


Id., Fig. 20 (annotations added). This occurs when the input signal (/CLK) at the second input terminal (CK2) is pulled to a voltage that causes transistor Q19 to turn on; this will pull the node labeled "N6" to the high (i.e., VDD) voltage level. This will cause transistor Q18 to turn on; when this is done, the second node (N1) is pulled to the low voltage level VSS. (On the other hand, when transistor Q19 is not turned on, the transistor Q18 will not turn on, and the low voltage VSS is not supplied to the second node (N1).)

618. The first driver is able to control the voltage of the second node in accordance with signal of the third input terminal as shown here.

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FIG. 20



Id., Fig. 20 (annotations added). This occurs when the input signal (CLK) at the third input terminal (CK1) is pulled to a voltage that causes transistor Q2 to turn on. This causes the low voltage level VSS to be passed through transistor Q2 to the node labeled "N6," and thus to be passed to the gate of transistor Q18 – which causes transistor Q18 to be turned off.

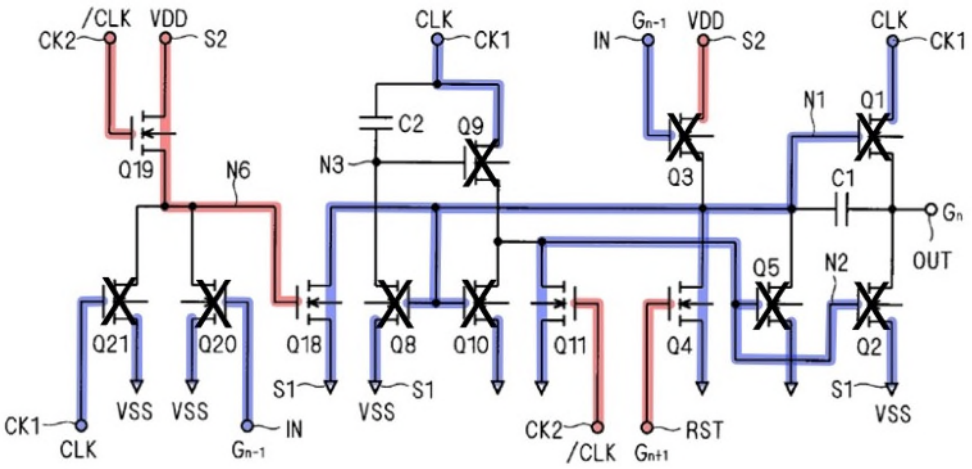
619. Relatedly, note that the second node N1 is coupled to the gate electrodes of transistors Q1, Q8, and Q10. Thus, the second node N1 controls the operation of these transistors, not the other way around.

620. Transistors Q18-Q21—which receive signals from IN (the first input terminal), CK2 (the second input terminal), and CK1 (the third input terminal)—also control the voltage of the node N1 by opening transistor Q18 to allow VSS to be provided to node N1 for purposes of bringing it to a low level. *Id.*, ¶¶ [0172], [0174]-

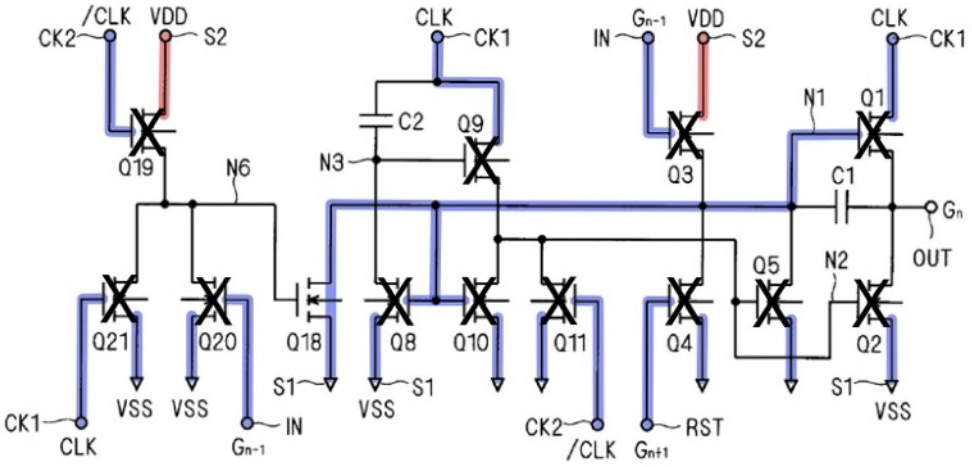
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[0177]. This occurs, for instance, during periods t_5-to-t_6 (top figure) and t_6-to-t_7 (bottom figure):

F I G . 2 0



F I G . 2 0

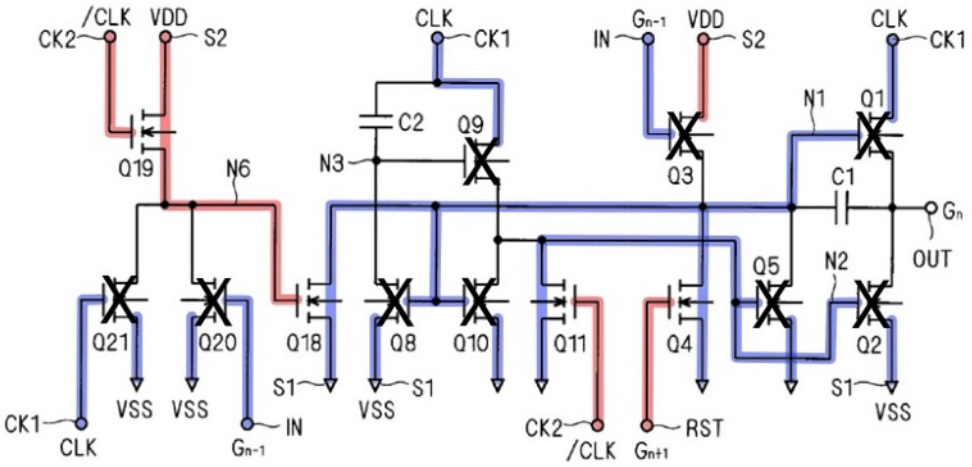


Id., Fig. 20 (annotations added; some transistors are marked with a large "X" to indicate that they are turned off in this situation – while those not so-marked serves to indicate that they are turned on in this situation.)

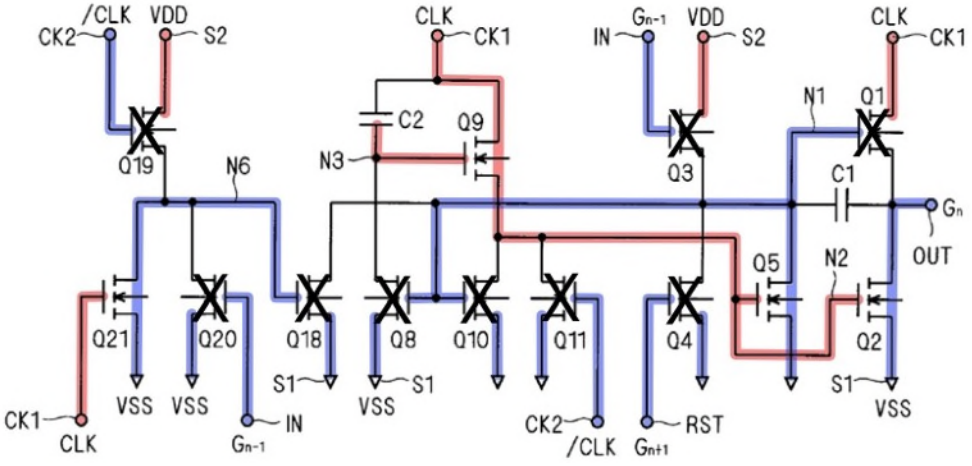
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621. Transistors Q4 and Q5 likewise provide output to and operate to control the potential of node N1 by also providing low VSS signals at appropriate times. *Id.*, ¶¶ [0175]-[0176]. This occurs, for instance, during period t_5-to-t_6 (top figure) and t_7-to-t_8 (bottom figure):

F I G . 2 0



F I G . 2 0



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Id., Fig. 20 (annotations added; some transistors are marked with a large "X" to indicate that they are turned off in this situation – while those not so-marked serves to indicate that they are turned on in this situation.)

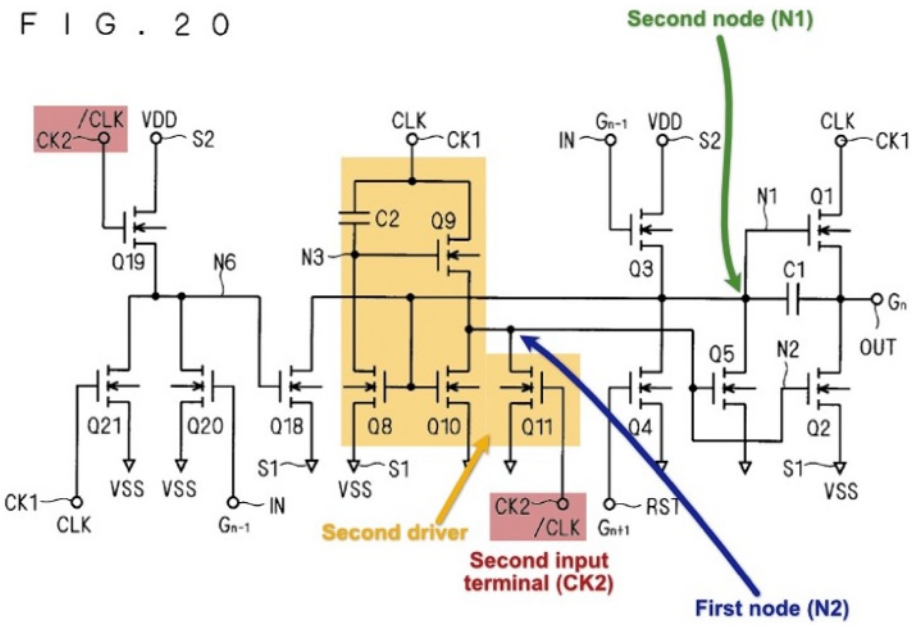
622. While Tobita uses more transistors than does the preferred embodiment of the first driver that is disclosed in the '593 patent, this claim does not limit the number of transistors in the first driver (nor are there limits placed on the number of any other present components). Additionally, while I recognize that certain of transistors Q3-Q5 and Q18-Q21 do not directly provide output to node N1, as mentioned earlier, it is my understanding that Patent Owner has taken the position in the associated ITC action that the claimed "first driver" can indirectly control node voltage(s). *See* Ex. 1009 at 22-23. In any event, as I have explained above, there are multiple transistors in Tobita's "first driver" that do in fact directly provide output to node N1 – including transistors Q3-Q5 and Q18.

623. Thus, Tobita discloses this claim element of Claim 1 of the '593 patent.

d. [1-c]: "a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node, wherein"

624. Tobita discloses this claim element of the '593 patent; this is evident via an annotated version of Figure 20 of Tobita:

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Ex. 1006, Fig. 20 (annotations added; *see also id.*, ¶¶ [0113]-[0114].) In the figure above, the "second driver" is identified using yellow box-bounding. As shown, Tobita's node N2 (the claimed first node) is coupled to gate electrodes and controls operation of transistors Q2 and Q5. *See, e.g., id.*, ¶¶ [0120], [0123]-[0124], [0132], [0134], [0136]. The potential of node N2 is itself controlled by the output of transistors Q8-Q11. *See, e.g., id.*, ¶¶ [0115], [0120]-[0121], [0123]-[0124], [0129]-[0132], [0134], [0136]. Thus, a POSITA would have understood these transistors to constitute the second driver.

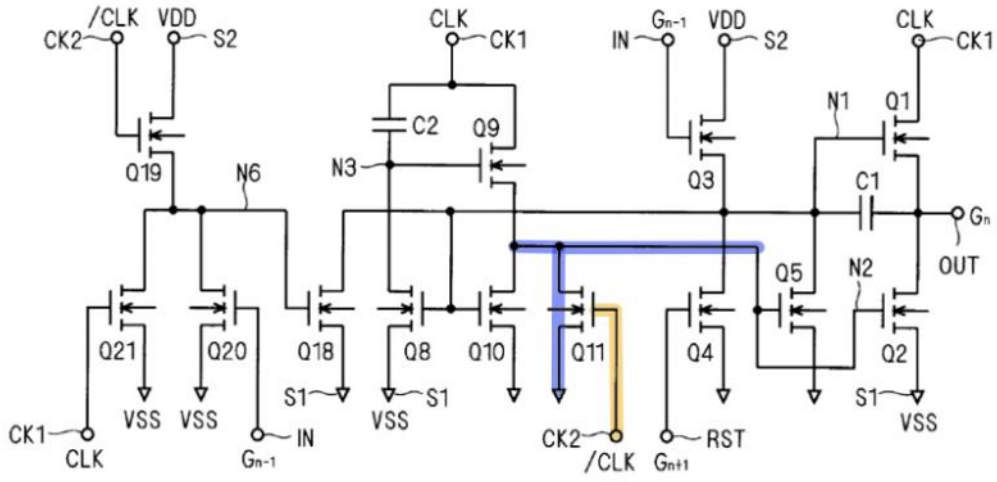
625. In the same way as was explained earlier for the first driver, while Tobita's embodiment of the second driver has more transistors than does the preferred embodiment second driver disclosed in the '593 patent, consistent with Patent Owner's proposed constructions and infringement theories from the related

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ITC Investigation, there is nothing in the claim element limiting the number of transistors in the second driver. Further, the voltage on the first node ("N2") is controlled in accordance with the signal of the second input terminal, and the voltage of the second node – as will be shown by the annotations to the following versions of Figure 20 of Tobita. As these annotations show, this functionality is implemented in at least two separate ways – one for the second input terminal, and one for the second node

626. The second driver is able to control the voltage of the first node in accordance with the signal of the second input terminal as described here.

F I G . 2 0



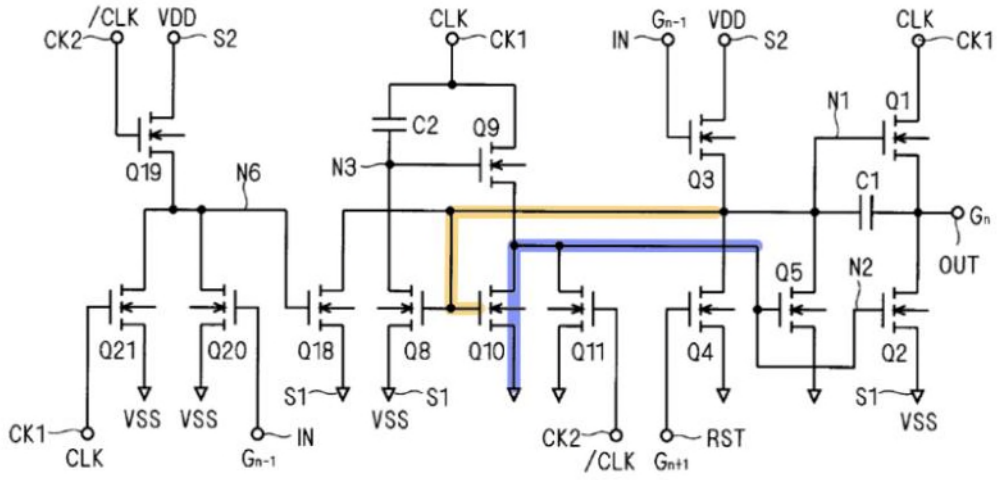
Id., Fig. 20 (annotations added). Transistor Q11 is controlled by the /CLK signal supplied to CK2 (the second input terminal). *Id.* When a voltage is applied to the second input terminal (CK2) that turns on the transistor Q11, Q11 connects the first

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node (N2) to the low voltage rail (VSS) – which pulls the voltage on the first node (N2) to the low rail voltage (VSS). (When transistor Q11 is not turned on, this functionality is not available). Thus, the voltage on the first node is controlled in accordance with the signal of the second input terminal.

627. The second driver is able to control the voltage of the first node in accordance with the voltage of the second node as described here.

F I G . 2 0



Id., Fig. 20 (annotations added). Transistors Q8 and Q10 have their gates connected to and are controlled by node N1 (the claimed second node). *Id.* When the voltage on the second node (N1) is such that it will turn on transistor Q10, the first node (N2) will be connected to the low voltage rail (VSS) through the transistor Q10 – which will serve to pull the voltage on the first node (N2) to the low voltage rail voltage (VSS). (When the voltage on the second node (N1) is such that it will not turn on

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transistor Q10, then this functionality is not available). Thus, the voltage on the first node is controlled in accordance with the voltage of the second node.

628. Relatedly, note that the first node N2 is coupled to the gate electrodes of transistors Q2 and Q5. Thus, the first node N2 controls the operation of these transistors, not the other way around.

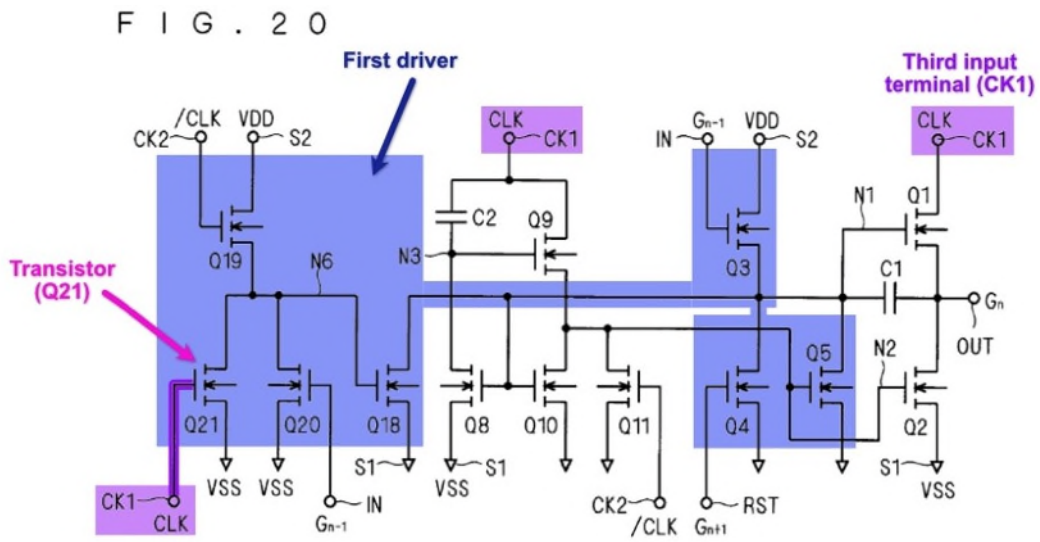
629. It should also be noted that transistor Q9 is controlled by either the VSS signal passing through transistor Q8 when that transistor is turned on – or by the voltage on capacitor C2 (which will vary depending on the capacitor's state of charge and the CLK signal supplied to terminal CK1). This gate voltage is shown as "N3" in figure 9. *See id.*, Fig. 9.

630. Therefore, Tobita discloses this claim element of Claim 1 of the '593 patent.

e. [1-d]: "the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver."

631. Tobita discloses this claim element of the '593 patent; this is evident via annotated versions of Figure 20 of Tobita:

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Ex. 1006, Fig. 20 (annotations added); *see also id.*, ¶ [0086]; [0177].) When a signal (such as CLK) is applied to the third input terminal (CK1), it directly controls the on/off operation of transistor Q21 – which is part of the first driver. In particular, the gate of transistor Q21 (part of Tobita's first driver) is coupled to has its on/off functionality controlled by the signal supplied by CK1 (the third input terminal).

632. Thus, Tobita discloses this claim element of Claim 1 of the '593 patent.

f. Claim 1 Summary

633. As just shown, Tobita discloses each element of Claim 1 of the '593 patent; thus, Tobita renders obvious Claim 1 of the '593 patent.

2. Dependent Claim 2

634. As an initial matter, Claim 2 depends from Claim 1; as was shown above, Claim 1 of the '593 patent is disclosed by Tobita.

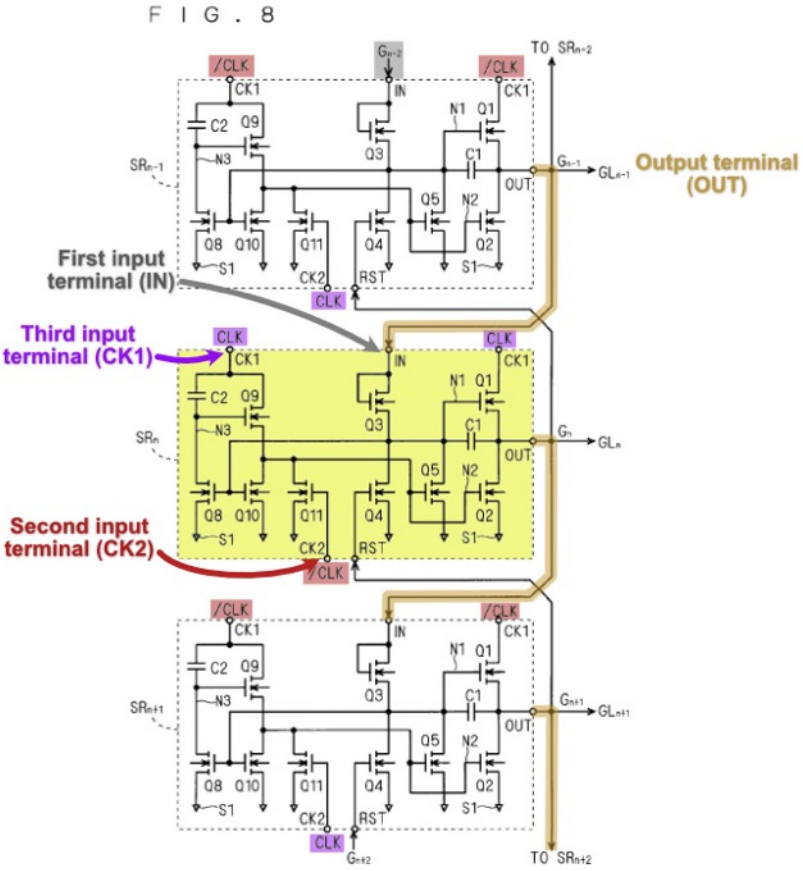
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635. Claim 2 further requires that "wherein the first input terminal receives an output signal of a previous stage circuit or a start signal, wherein the second input terminal receives a first clock signal, and wherein the third input terminal receives a second clock signal." Tobita discloses this claim of the '593 patent.

636. As an initial matter, note that the first part of the claim language just cited includes "wherein the first input terminal receives an output signal of a previous stage circuit ***or*** a start signal" (emphasis added). Because of the use of "or," the presence of this claim element term can be shown to be present in Tobita if the first input terminal receives either "an output signal of a previous stage circuit" or "a start signal"; it will be shown next that Tobita discloses the first of these two options.

637. This item and the remainder of Claim 2 can be shown to be disclosed by Tobita via the examination of an annotated version of Figure 8 of Tobita. As can be seen, Tobita teaches a shift register including stages SR_{n-1}, SR_n, SR_{n+1}, etc.:

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Ex. 1006, Fig. 8 (annotations added); *see also* ¶ [0117].

638. As can be seen from examination of this annotated figure, the middle stage circuit block (SR_n) receives an output signal of a previous stage circuit block at the first input terminal (IN) as its input signal. Also, the second input terminal (CK2) receives a first clock signal (/CLK), and the third input terminal (CK1) receives a second clock signal (CLK); Tobita specifically identifies /CLK and CLK as being clock signals (e.g., "… clock signals CLK and /CLK …" *Id.*, ¶¶ [0095], [0118]. Note in particular that the third stage circuit block (SR_3), like the first stage circuit block (SR_1), is configured so that the second input terminal receives a first

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clock signal and the third input terminal receives a second clock signal. *Id.* As shown, terminal IN (the first input terminal) of stage SR_n receives output signal G_{n-1} of the previous stage circuit SR_{n-1} (that stage's output signal). *Id.* Terminal CK2 of SR_n (the second input terminal) receives /CLK (the claimed first clock signal), and terminal CK1 of SR_n (the third input terminal) receives CLK (the claimed second clock signal). *Id.*

639. Per Tobita, both /CLK and CLK are clock signals. *Id.*, ¶ [0118]

640. Thus, Tobita renders obvious Claim 2 of the '593 patent.

641. For completeness, it can be noted that the other part of the "or" situation discussed at the beginning of this discussion of Claim 2 ("wherein the first input terminal receives an output signal of a previous stage circuit ***or*** a start signal") is also present in Tobita. Figure 8 of Tobita depicts a cascade of shift registers – in which (as just detailed) the first input terminal of a particular stage circuit receives an output signal of the previous stage circuit; however, Figure 8 does not include the initial stage circuit that is present as the first stage circuit in the cascade. However, Tobita notes that in this instance, the first stage circuit would receive a start signal:

> … when the output signal G_{n-1} from the immediately preceding stage (or the start pulse SP in the first stage)…

Id., ¶ [0086].

> Specifically, each of the unit shift registers SR has its input terminal IN connected to the output terminal OUT of a unit shift register SR of the immediately preceding stage,

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> except that the input terminal IN of the unit shift register SR_1 of the first stage receives a start pulse SP as an input signal.

Id., ¶ [0094].

> Starting from that mode, the output signal G_{n-1} from the immediately preceding stage (start pulse SP in the case of the first stage), when raised to the H level, is input to the input terminal IN of the unit shift register SR…

Id., ¶ [0098].

642. Thus, Tobita renders obvious Claim 2 of the ’593 patent.

3. Independent Claim 15

643. It is my conclusion and opinion that Claim 15 of the ’593 patent is rendered obvious by Tobita.

a. [15-pre]: “An organic light emitting display, comprising:”

644. In the earlier considerations of the preamble of Claim 15. with respect to Ground 1 (at Section XII.A.10) and Ground 2 (at Section XII.B.10), it was noted that the issue of whether or not the preamble of Claim 15 is limiting would be considered in slightly more detail when Tobita was assessed. I do so here.

645. As an initial matter, it appears that the preamble of claim 15 is not limiting. The phrase “organic light emitting display” appears to be a simple label. It does not come up again in Claim 15, and is only recited in the preambles of dependent claims 16-28 as “[t]he organic light emitting display as claimed in claim 15” or another claim depending from claim 15.

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646. Regardless, even if limiting, it is my conclusion and opinion that a POSITA would have considered it obvious to employ Tobita with an organic light emitting display for the reasons that will now be considered with specific respect to Tobita.

647. The circuitry disclosed in Tobita is stated as being applied for use with liquid crystal displays (LCDs). As was described in Section VII.B.3, stage circuitry of the type disclosed in the ’593 patent can be employed with more than one type of display technology; the same can be said of Tobita. Indeed, the circuity disclosed by the ’593 patent performs the function of providing sequences of signals to drive the rows of a display. As discussed above, this structure of having rows of pixels in a display that are sequentially driven is well known, and it is common to most display technologies. For example, U.S. Patent Publication No. 2007/0139348A1 (“Lee”) claims an invention comprising stage circuits that can provide scan signals to either LCD or OLED panels. Ex. 1015, claims 1, 14. Thus, a POSITA would have found it obvious that Tobita’s embodiment providing sequential sequencing signals for LCDs could be employed to perform the similar sort of sequential signaling required by an OLED display. This is evident from the similar functionality of the Tobita circuitry as compared to the ’593 circuitry.

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648. Thus, it is my conclusion and opinion that a POSITA would have found it obvious to employ Tobita's circuitry with an OLED – for several interrelated reasons.

649. While Tobita references "a liquid crystal display," this is only an example. Ex. 1006, ¶ [0004]. Thus, a POSITA would have recognized that Tobita's teachings broadly apply to any "display apparatus." *Id.* Further, between Tobita's filing and the effective filing date of the '593 patent (the latter of which is the pertinent date for this obviousness analysis), OLED displays became more commonplace. Thus, Tobita's focus on earlier available LCD (as opposed to OLED) displays is not surprising; however, as Tobita notes (as just described), the teachings of Tobita apply more-generally (and more-broadly) to any "display apparatus" – and thus it would have been obvious to a POSITA that Tobita's teachings applied to more than just LCD displays; rather, as Tobita states, they could be applied to any suitable "display apparatus" – which, as comparison of the architecture of the '593 patent and the architecture of Tobita shows, was clearly the case.

650. Further, when the '593 patent was filed, not only were OLED displays a well-known technology; it was also well-known that OLED displays and LCD displays share features many similar basic features – including pixel matrices, data drivers, and scan drivers. It was also well-known at that time that LCD and OLED displays can employ structurally- and functionally-similar stage circuits. See, e.g.,

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Ex. 1015, claims 1, 14 (already cited above in the same context). It is quite obvious that if the newer OLED displays could be operated using the same supporting circuitry as that which had already been successfully developed for LCD (or other) displays, it would make good engineering sense to use that successful set of circuit architectures as-is with any newer display technologies.

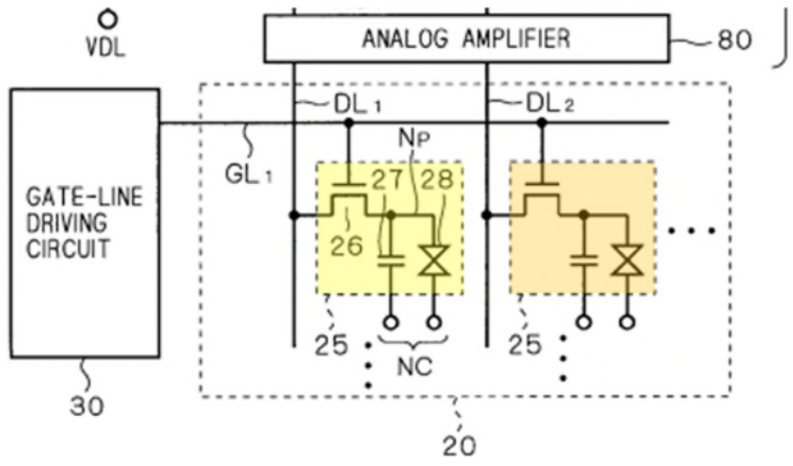
651. Given all of this, a POSITA would have readily understood that Tobita's teachings were applicable to any available type of display – including an OLED display.

652. Thus, even if the preamble of Claim 15 is limiting, Tobita renders obvious the preamble of Claim 15 of the '593 patent.

b. [15-a]: "pixels positioned in regions partitioned by scan lines and data lines;"

653. Tobita discloses this claim element of Claim 15 of the '593 patent.

654. This can readily be seen via an annotated excerpt from Figure 1 of Tobita.



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Ex. 1006, Fig. 1 (excerpted and annotations added). The details of the structures depicted in this figure are provided by Tobita in the specification.

> The liquid crystal array part 20 includes a plurality of pixels 25 arrayed in a matrix. The columns of pixels (hereinafter also referred to as "pixel lines") are respectively provided with gate lines GL_1, GL_2, #. . . (hereinafter also generically referred to as a "gate line GL), and the rows of pixels (hereinafter also referred to as "pixel rows") are respectively provided with data lines DL_1, DL_2, #. . . (hereinafter generically referred to as a "data line DL"). FIG. 1 representatively shows pixels 25 of the first and second rows in the first column and corresponding gate line GL_1 and data lines DL_1 and DL_2.
>
> Each pixel 25 has a pixel switching device 26 disposed between a corresponding data line DL and a pixel node Np, and a capacitor 27 and a liquid crystal display device 28 connected in parallel between the pixel node Np and a common electrode node NC.

Id., ¶¶ [0059]-[0060].

Note that the "gate lines" of Tobita are the same as the "scan lines" of the '593 patent – as Tobita explicitly states (at, e.g., [0004] ("A gate line (scanning line) is provided for each row of pixels") and at [0058] ("… a gate-line driving circuit (scanning-line driving circuit)…"). Note also that, as can be seen in the figure above, the scan lines and the data lines are located between the pixels (yellow/orange boxes) and separate the pixels.

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655. Gate lines—labeled GL_1, GL_2, etc.—are connected to rows of pixels and data lines—labeled DL_1, DL_2, etc.—are connected to columns of pixels. *Id.* Gate lines are the same as scanning lines. *Id.*, ¶ [0004].

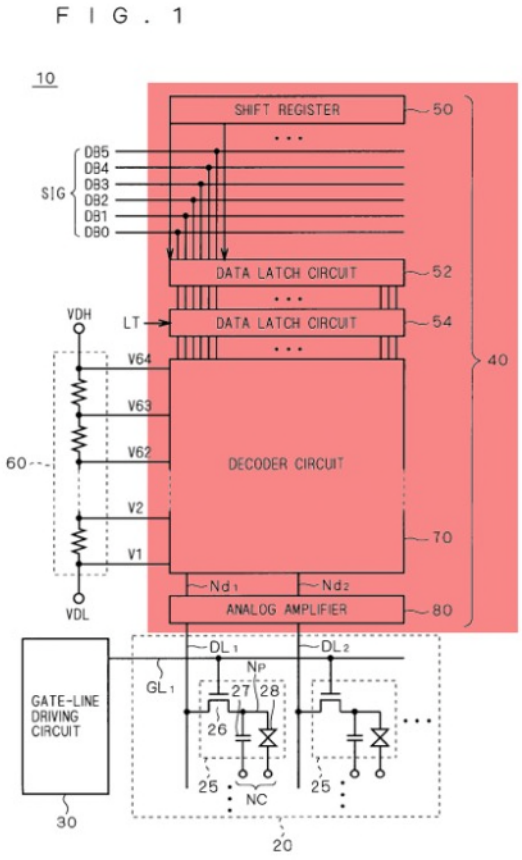
656. Thus, Tobita discloses this claim element of Claim 15 of the ’593 patent.

c. [15-b]: “a data driver for supplying data signals to the pixels through the data lines; and”

657. Tobita discloses this claim element of Claim 15 of the ’593 patent.

658. This can be readily seen by a more-extensive examination of Figure 1 of Tobita.

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Ex. 1006, Fig. 1 (annotations added). The data lines and pixel structures depicted in Figure 1 of Tobita were already explained just above, in the discussion of claim element [15-a] – where, among other things, the lines DL_1, DL_2, … were identified as being data lines. The annotated structure (40) is identified in Tobita as being a "source driver" (e.g., at [0058]). This structure is clearly supplying data signals to the pixels through the data lines; thus, the "source driver" of Tobita is the same thing as the "data driver" of the '593 patent. Furthermore, in Tobita, the source driver 40 is responsible for "output[ting] display voltages set stepwise by a display signal SIG … to the data lines DL." *Id.*, ¶ [0062]; *see also id.*, ¶ [0071].

659. Therefore, Tobita discloses this claim element of Claim 15 of the ‘593 patent.

d. [15-c]: “a scan driver for supplying scan signals to the pixels through the scan lines, the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals and having a first input terminal, a second input terminal, a third input terminal, and an output terminal,”

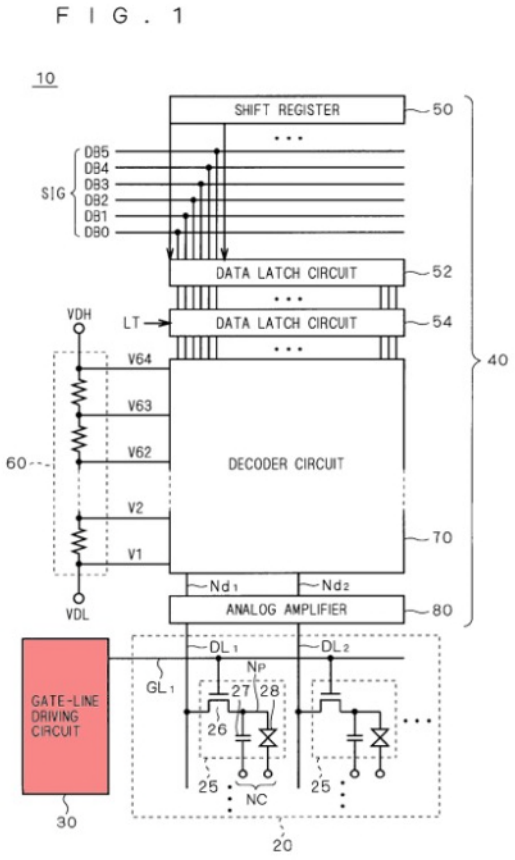
660. Claim element [15-c] is rather long – and thus the analysis will be simpler to explain if this claim element is broken up into sub-elements.

i. [15-c-1]: “a scan driver for supplying scan signals to the pixels through the scan lines”

661. Tobita discloses this claim sub-element of claim element [15-c] of Claim 15 of the ’593 patent.

662. This can readily be seen by examination of Figure 1 of Tobita.

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Ex. 1006, Fig. 1 (annotations added); *see also id.*, ¶ [0058] (where Tobita describes the "gate line driving circuit"). As was explained above, Tobita notes (at, e.g., [0004] and [0058]) that the "gate lines" and the "scan lines" are the same thing under two different names. Therefore, the "gate line driving circuit" of Tobita is the same thing as a "scan line drive circuit" – i.e., it is a scan driver. Further, as was also discussed earlier (in the discussion of claim element [15-a]), the gate/scan driver supplies scan signals to the pixels through the scan lines – as can once again be seen in the annotated figure above.

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663. Thus, Tobita discloses this claim sub-element of claim [15-c] of Claim 15 of the ’593 patent.

ii. [15-c-2]: “the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals”

664. Tobita discloses this claim sub-element of claim element [15-c] of Claim 15 of the ’593 patent.

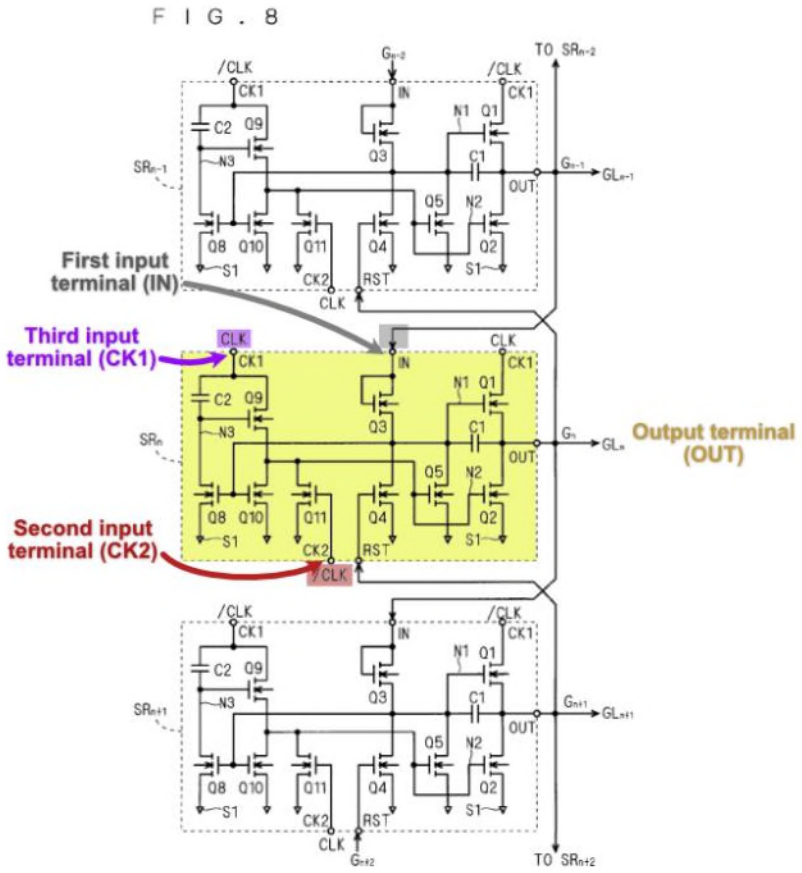
665. Just above, in the discussion of claim sub-element [15-c-1], it was explained how Tobita describes a “gate line driving circuit” (30) that drives the gate lines that drive the pixels (as a row of pixels) of the display – and how the “gate lines” of Tobita are thus the same thing as the “scan lines” of the ‘593 patent. Further, Tobita describes the gate line driving circuit (i.e., the scan driver) as follows:

> The gate-line driving circuit 30 includes a plurality of unit shift registers SR1, SR2, SR3, SR4, # ... connected in cascade (Tobita at [0073]; ellipsis in the original.)

As Tobita also details, this circuit “sequentially drives the gate lines GL_1, GL_2, #. . . in synchronization with the scanning cycle.” *Id.*, ¶ 0071; *see also id.*, ¶ 0061; in addition, as Tobita further details, the scan line drive circuit includes stages of “cascade-connected unit shift registers SR.” *Id.*, ¶ [0167].

666. Tobita describes the inner details of the scan driver in Figure 8.

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Id., Fig. 8 (annotations added; the annotation labels were explained earlier, in the discussion of Claim 2.) As can be seen by inspection of Figure 8 of Tobita, the scan driver includes stage circuits (shift registers) that are coupled to the scan lines (which, as detailed above, Tobita calls "the gate lines"). Further, that each of the stage circuits generates a corresponding scan signal of the scan signals was described earlier – in the discussion associated with Claim 1, where the output characteristics of the shift register circuitry were detailed.

667. Thus, Tobita discloses this claim sub-element of claim element [15-c] of Claim 15 of the '593 patent.

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iii. [15-c-3]: "and having a first input terminal, a second input terminal, a third input terminal, and an output terminal,"

668. This claim sub-element of claim element [15-c] of Claim 15 of the '593 patent is disclosed by Tobita.

669. The claim sub-element is essentially identical to the preamble of Claim 1 of the '593 patent – which was already discussed in detail earlier (at Section XII.D.1.a) – where it was shown that these details are disclosed by Tobita. As I discussed there when addressing claim 1, each unit shift register receives input from IN (the first input terminal), CK2 (the second input terminal), and CK1 (the third input terminal), and outputs a corresponding scan signal G_n to OUT (the output terminal) which is then provided to scan line GL. *See* above discussion of limit [1-pre].

670. Thus, Tobita discloses this claim sub-element of claim element [15-c] of Claim 15 of the '593 patent.

iv. Claim Element [15-c] Summary

671. As just demonstrated, Tobita discloses claim sub-elements [15-c-1], [15-c-2], and [15-c-3] of the '593 patent; thus, Tobita discloses claim element [15-c] of Claim 15 of the '593 patent.

e. Preface to claim elements [15-d] – [15-g]

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672. Between claim element [15-c] and claim element [15-d], Claim 15 includes the phrase "wherein each of the stage circuits includes:". It is taken here that this is intended to mean that "includes" is stated with regard to the sequential list of claim elements which follow for the remainder of Claim 15 – that is, claim elements [15-d], [15-e], [15-f], and [15-g]. Each of these claim elements will be considered in turn.

f. [15-d]: "an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node,"

673. This claim element is identical to claim element [1-a] of Claim 1 of the '593 patent – which was discussed earlier (in Section XII.D.1.b).

674. Thus, Tobita discloses this claim element of Claim 15 of the '593 patent.

g. [15-e]: "a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal, and"

675. This claim element is identical to claim element [1-b] of Claim 1 of the '593 patent – which was discussed earlier (in Section XII.D.1.c).

676. Thus, Tobita discloses this claim element of Claim 15 of the '593 patent.

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h. [15-f]: "a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node, wherein"

677. This claim element is identical to claim element [1-c] of Claim 1 of the '593 patent – which was discussed earlier (in Section XII.D.1.d).

678. Thus, Tobita discloses this claim element of Claim 15 of the '593 patent.

i. [15-g]: "the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver."

679. This claim element is identical to claim element [1-d] of Claim 1 of the '593 patent – which was discussed earlier (in Section XII.D.1.e).

680. Thus, Tobita discloses this claim element of Claim 15 of the '593 patent.

j. Claim 15 Summary

681. As just shown, Tobita discloses each element of Claim 15 of the '593 patent; thus, Tobita renders obvious Claim 15 of the '593 patent.

4. Dependent Claim 16

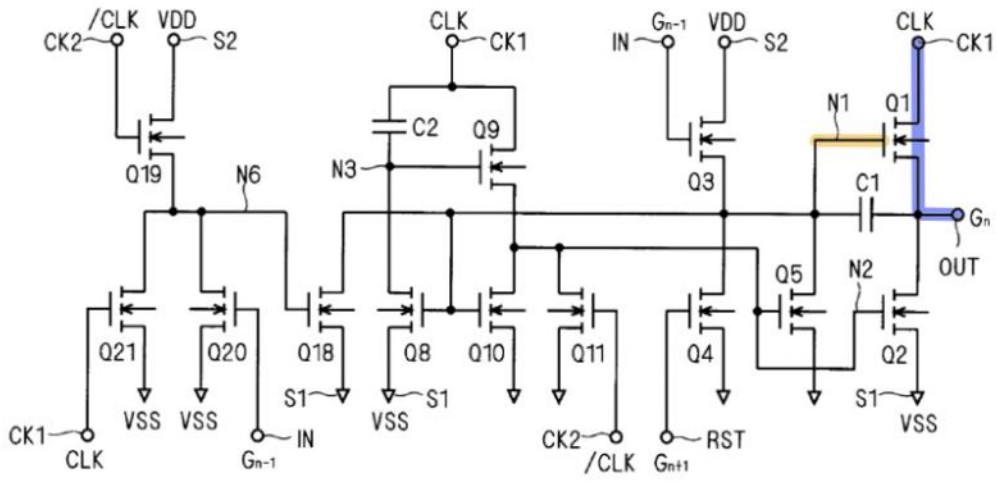
682. As an initial matter, Claim 16 depends from Claim 15; as was shown above, Claim 15 of the '593 patent is disclosed by Tobita.

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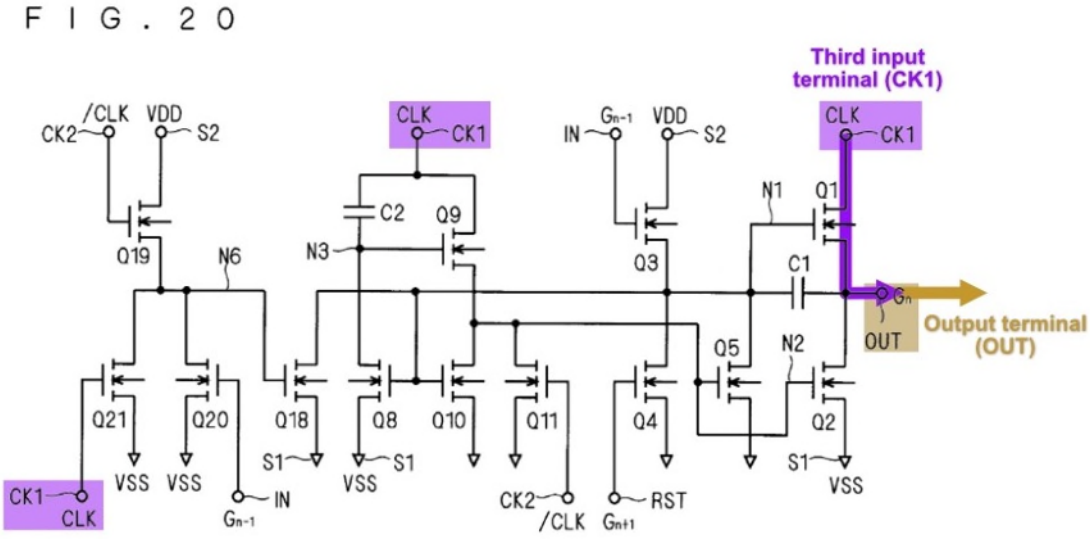
683. Claim 16 further requires "a clock signal supplied to the third input terminal is used as the scan signal." Tobita discloses this claim of the '593 patent.

684. The first part of this claim element ("a clock signal supplied to the third input terminal") was already discussed earlier (in Section XII.D.1.b.iii) – with respect to claim sub-element [1-a-3] of claim element [1-a] of Claim 1 of the '593 patent. An annotated version of Figure 20 of Tobita provided below summarized this:.

F I G . 2 0



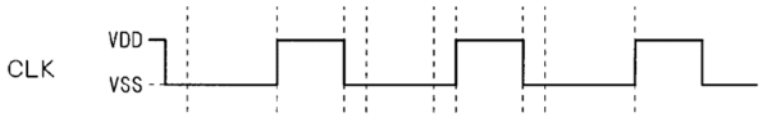
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Ex. 1006, Fig. 20 (annotations added); s*ee also id.*, ¶¶ [0109], [0117], [0122], [0125]-[0126].) As detailed in Section XII.D.1.b.iii, when an appropriate (i.e., turn-on) voltage is applied at the second node (the node labeled "N1"), transistor Q1 will turn on; this will connect the signal of the third input terminal ("CK1") to the node of the output terminal ("OUT") – and thus the signal of the third input terminal ("CK1") is supplied to the output terminal ("OUT"). (On the other hand, when a turn-on voltage is not applied at the second node ("N1"), transistor Q1 will not turn on – and thus the signal of the third input terminal (CK1) is not supplied to the output terminal ("OUT").)

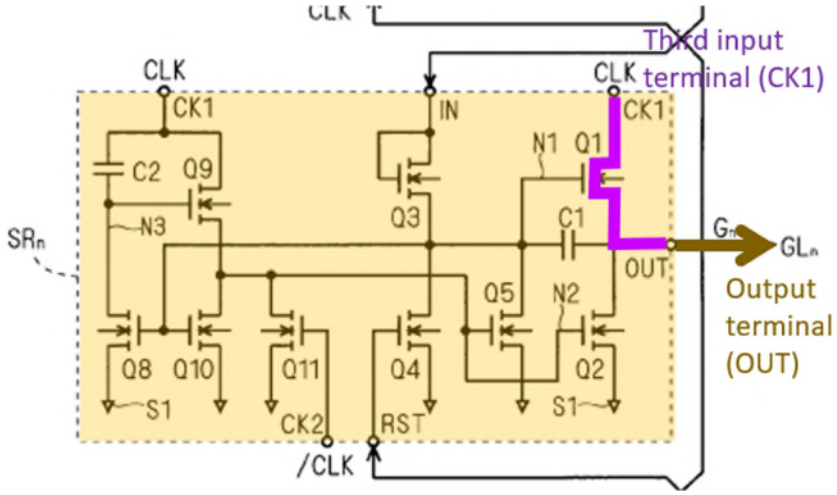
685. As also discussed earlier, the third input terminal (CK1) receives a clock signal – in particular, the clock signal CLK, which is depicted in Figure 9 of Tobita.

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Id., Fig. 9 (exerpted). As the name itself implies, the signal CLK is clearly a clock signal – and, as detailed in the discussion of Claim 2, Tobita identifies (e.g., at [0095]) CLK as a clock signal.

686. Finally, with respect to this clock signal being used as "the scan signal," it was shown above (see the annotated version of Figure 20 of Tobita above) that when transistor Q1 is turned on, the input signal that is being applied to the third input terminal CK1 (which, in this case is the clock signal CLK) is supplied to the output terminal OUT. What that signal (at OUT) is being used for is made clear via a partial, annotated version of Figure 8 of Tobita:

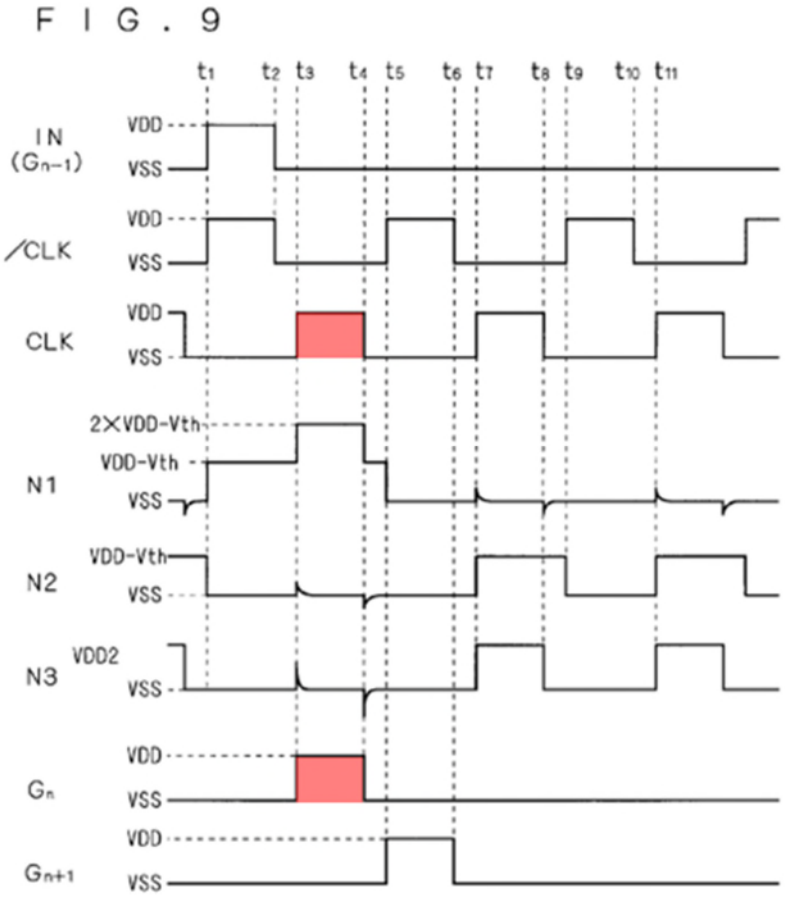


Id., Fig. 8 (excerpted and annotated). As can be seen, the output of the first stage circuit block (SR_n) is being fed to GL_n; as described earlier (in Section XII.D.7.d), the "gate lines" of Tobita are the same thing as the "scan lines" of the '593 patent.

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(Note also that each stage circuit block (SR_{n-1}, SR_n, SR_{n+1}, …) feeds the output of its OUT terminal to a gate/scan line of its own.)

687. Further, Figure 9 of Tobita shows what use is being made of the clock signal CLK (which is being provided to the output terminal).



Ex. 1006, Fig. 9 (annotated). As the annotations show, during the period $t_3 – t_4$, the clock signal supplied to the third input terminal (i.e., CLK) is used as the scan signal (i.e., G_n).

688. Therefore, the clock signal that is supplied to the third input terminal is passed to the output terminal (OUT), where it is then used as a scan signal.

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689. Thus, Tobita renders obvious this claim of the ’593 patent.

5. Dependent Claim 17

690. As an initial matter, Claim 17 depends from Claim 15; as was shown above, Claim 15 of the ’593 patent is disclosed by Tobita.

691. Claim 17 further requires that “the first input terminal receives a scan signal of a previous stage circuit or a start signal.”

692. This claim is identical to an element of Claim 2 of the ’593 patent – which was discussed earlier (in Section XII.D.2).

693. Thus, Tobita renders obvious this claim of the ’593 patent.

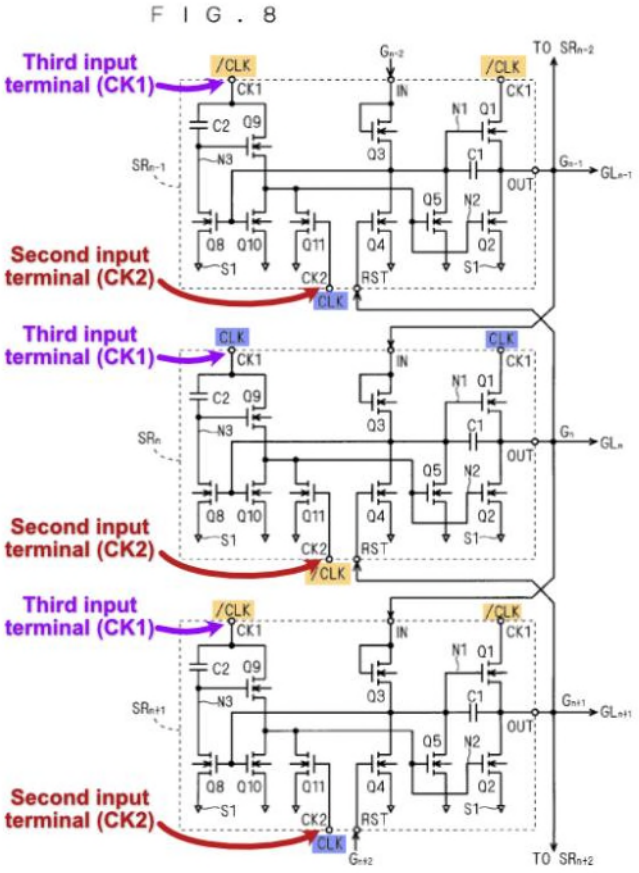
6. Dependent Claim 18

694. As an initial matter, Claim 18 depends from Claim 17, and Claim 17 depends from Claim 15; as was shown above, Claim 15 and Claim 17 of the ’593 patent are disclosed by Tobita.

695. Claim 18 further requires “wherein second input terminals of odd stage circuits receive a first clock signal and third input terminals of odd stage circuits receive a second clock signal, and wherein second input terminals of even stage circuits receive the second clock signal and third input terminals of even stage circuits receive the first clock signal.” In other words, the first clock signal and the second clock signal alternate between the second input terminal and the third terminal along the sequence of stage circuits.

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696. This is readily demonstrated via an annotated version of Figure 8 of Tobita.



Ex. 100, Fig. 8 (annotations added). To simplify the explanation of what is going on, the first clock signal (/CLK) is annotated in red, and its destinations are highlighted in maroon for odd-numbered stage circuits (G_n, …) and orange for even-numbered stage circuits (G_{n-1}, G_{n+1}, …). The second clock signal (CLK) is annotated in purple, and its destinations are highlighted in purple for odd-numbered stage circuits (G_n, …) and light blue for even-numbered stage circuits (G_{n-1}, G_{n+1}, …). As can be seen by inspection, the first clock signal (/CLK) goes to the second input

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terminal (CK2) of the stage circuit SR_n, and to the third input terminal (CK1) of the stage circuits SR_{n-1} and SR_{n+1}; meanwhile the second clock signal (CLK) goes to the third input terminal (CK1) of the stage circuit SR_n, and to the second input terminal (CK2) of the of the stage circuits SR_{n-1} and SR_{n+1}.

697. Tobita, at [0027], describes the stage circuits of Figure 8 as being "connected in a cascade." As was noted earlier, Tobita further describes the meaning of cascade as "The gate-line driving circuit 30 includes a plurality of unit shift registers SR_1, SR_2, SR_3, SR_4, # . . . connected in cascade" (ellipsis in the original); this is also shown in Figure 2 of Tobita (and described at [0073] and [0092] of Tobita), and in Figure 5 of Tobita (and described at [0094] of Tobita).

698. Referring back to Figure 8 (and the annotated version of Figure 8 presented just above), these further explanations of the "cascade" described by Tobita show that the depiction of Figure 8 is an excerpt from a larger cascade of such stage circuits. Further, it is readily understood that if the excerpt were to be (e.g.) expanded from three stage circuits to five stage circuits, so as to include the next stage at the top of the stack in Figure 8 (which would be SR_{n-2}) and the next stage at the bottom of the stack in Figure 8 (which would be SR_{n+2}), the stage circuits SR_{n-2} and SR_{n+2} would be configured exactly as is stage circuit SR_n – with, in particular, the same locations of the inputs of the first clock signal (/CLK) and the second clock signal (CLK) as in stage circuit SR_n.

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699. Therefore, the stage circuits SR_{n-1} and SR_{n+1} (and beyond, in the "cascade") provide the "even stage circuits," while the stage circuits SR_{n-2}, SR_n, and SR_{n+2} (and beyond, in the "cascade") provide the "odd stage circuits." And thus, the second input terminals of odd stage circuits receive a first clock signal and third input terminals of odd stage circuits receive a second clock signal, and the second input terminals of even stage circuits receive the second clock signal and third input terminals of even stage circuits receive the first clock signal.

700. Thus, Tobita renders obvious this claim of the '593 patent.

E. Ground 5: Tobita in Combination with Jeong Renders Obvious Claims 7 and 21

701. As will be discussed below, it is my conclusion and opinion that Claims 7 and 21 of the '593 patent are rendered obvious by Tobita in combination with Jeong and the knowledge of a POSITA.

1. Generalized Motivation to Combine

702. Before going into the details of Ground 5, some of the generalized aspects of the motivation to combine Jeong with Tobita should be considered.

703. As an initial matter, Tobita and Jeong both involve shift register circuitry that forms the basis of a scan driver used in the operation of pixel-matrix displays. Thus, a POSITA would have been aware of both of these references, and would have studied the advantages of these two respective designs. Further, field-

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effect transistors, circuits based on them, and the use of such circuits for the drivers in a pixel-matrix display, were well known in the art – and had been well known for years prior to 2012. Therefore, a POSITA at the time of the alleged inventions of the '593 patent would have had extensive knowledge about such circuits and their usage. Accordingly, it would have been sensible for a POSITA to integrate compatible circuits, so as to garner respective advantages of two or more references. Further, because the circuit design and circuit operation principles were already well known in the art, such combinations would have yielded predictable results.[25]

704. Further, a POSITA would have been motivated to combine Tobita with Jeong because, as noted above, both involve the use of shift registers to provide scan drivers for use in pixel-based displays. Both Tobita and Jeong use field-effect transistors, and in each reference the circuits disclosed use only one species (either nMOS or pMOS) of field-effect transistor. As per the discussion in Section VII.A.2, while Tobita's disclosed circuitry uses nMOS transistors and Jeong's disclosed circuity uses PMOS transistors, the ability to change switching transistors from nMOS to pMOS (or vice versa), along with the operational changes necessary for this change, were well known in the art at the time of the '593 patent. Further, the

[25] As per some of the references cited in Section VII.A, this knowledge predates the '593 patent by an extensive period of time – with one of the references cited going back to 1967.

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similarity of the functions and designs of Tobita and Jeong would have further confirmed to a POSITA that combining the teachings of these two references would involve straightforward modifications (as discussed just above) – with both predictable outcomes and a reasonable expectation of success.

705. Finally, a POSITA would have observed that Tobita's outputting unit and Jeong's outputting unit share what are essentially the same components in the same configuration – and thus Jeong is close enough to Tobita to make the combination of details from Jeong into Tobita a reasonable prospect.

2. Dependent Claim 7

706. As an initial matter, Claim 7 depends from Claim 2, and Claim 2 depends from Claim 1; as was shown above (in Section XII.C), Claim 1 and Claim 2 of the '593 patent are rendered obvious by Tobita.

707. Claim 7 further requires:

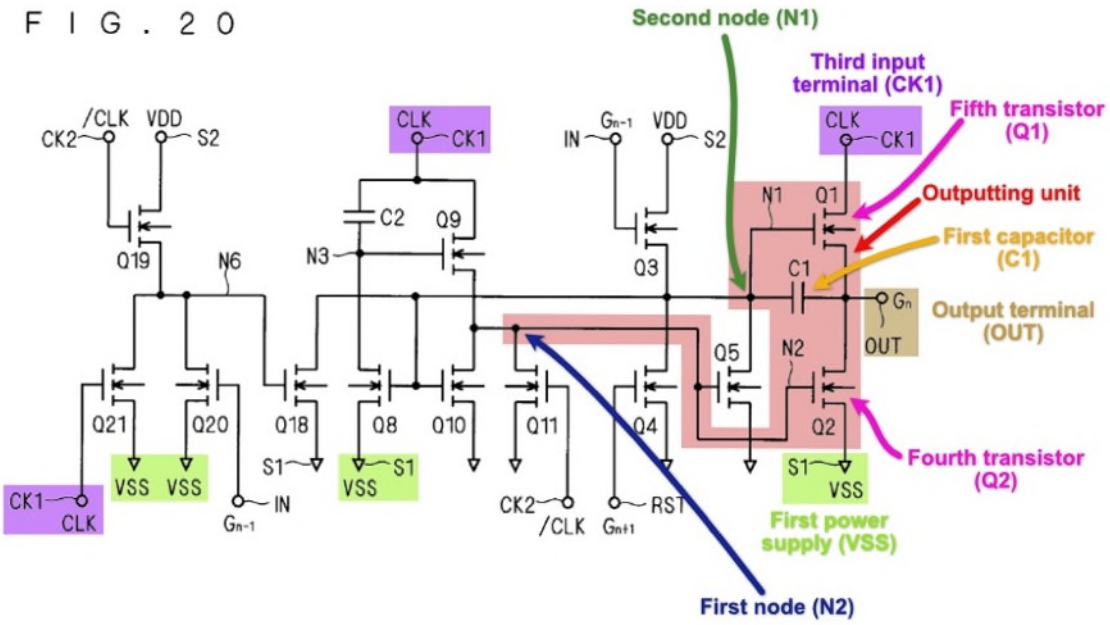
> wherein the outputting unit includes:
>
> a fourth transistor between the first power supply and the output terminal, the fourth transistor having a gate electrode coupled to the first node;
>
> a fifth transistor between the output terminal and the third input terminal, the fifth transistor having a gate electrode coupled to the second node;
>
> a first capacitor between the second node and the output terminal; and

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a second capacitor between the first node and the first power supply.

As will be shown here, Tobita combined with Jeong and the knowledge of a POSITA renders obvious this claim of the '593 patent.

708. Simple inspection of the circuitry of Figure 20 of Tobita shows that this circuitry contains all of the elements recited in Claim 7, arranged in the configuration that is recited in Claim 7 – with the exception of the second capacitor, which is not present in the circuitry of Figure 20 of Tobita.



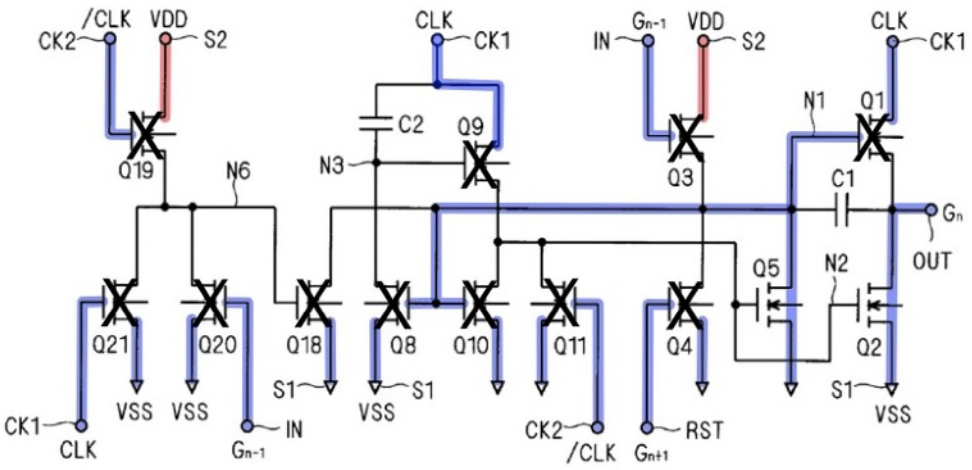
Ex. 1006, Fig. 20 (annotated). A POSITA examining this circuitry would reach several conclusions – since these conclusions are well-known in the art.

709. First, a POSITA would recognize that the first node (N2) that will be electrically isolated whenever the three transistors which provide electrical access to

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this node (Q9, Q10, and Q11) are all turned off. Referring to the earlier discussion regarding Figure 9 of Tobita, this will occur, for instance, during period t_8-to-t_9:

F I G . 2 0



Id., Fig. 20 (annotated).

710. Second, a POSITA would also understand that the amount of charge stored at the node would determine the isolated voltage at that (floating) node – using the simple and well-known equation

$$Q = CV,$$

where Q is the charge on the node, V is the resulting voltage at the node, and C is the capacitance at the node. For example, if the first capacitor (C1) were not there, then the capacitance would be supplied only by the wiring and transistors[26] (and the

[26] All field-effect transistors include small parasitic capacitances; usually, these capacitances are so small that they are not explicitly included in the circuit diagram.

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parasitic capacitances of any adjacent transistors) to which the node is connected; however, as the wiring and transistors hold very little charge, they provide very little capacitance – and thus, the resulting voltage value will be based upon a very small amount of charge.

711. This can be problematic, since perturbations in the amount of charge (for example, due to electromagnetic interference (EMI) or interline crosstalk during digital switching events) may cause sizeable changes in the voltage on the node; these types of signal integrity issues are undesirable. Therefore, a POSITA would be motivated to seek methods of making the circuitry of Tobita more robust against a problem of this sort.

712. In addition, the "isolation" of this node is being provided by turning off all the transistors that provide electrical connection(s) to that node when any one of them is turned on – and, as described above, examination of Figure 20 of Tobita indicates that that there are three such transistors (Q9, Q10, Q11) that provide electrical connections to the first node (N2), and the first node (N2) is isolated when all of these transistors are turned off. However, as described in Section VII.A.4, a transistor does not turn off perfectly – and some off-state leakage current will be present. If the voltage at the isolated first node (N2) is defined by a very small amount of charge, then that charge will leak away very quickly via the imperfect off-

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state of the transistors – and the voltage will change quickly with time, and may even quickly reach the low (VSS) voltage as its inevitable endpoint.

713. As a POSITA would thus know, the voltage at this node would be made more robust (i.e., it would be able to hold the isolated voltage value more stably against upsets like EMI, and would take a long time to drain the charge away through the imperfect off-state transistors and thus would retain the isolated voltage much longer) if the capacitance at the node could be increased. This is actually quite easily done – by adding a capacitor to the isolated node, so that the amount of charge used to create the voltage at the node is much larger; as can readily been seen from the equation presented above, for the same voltage, a larger capacitance would hold a proportionately larger charge.

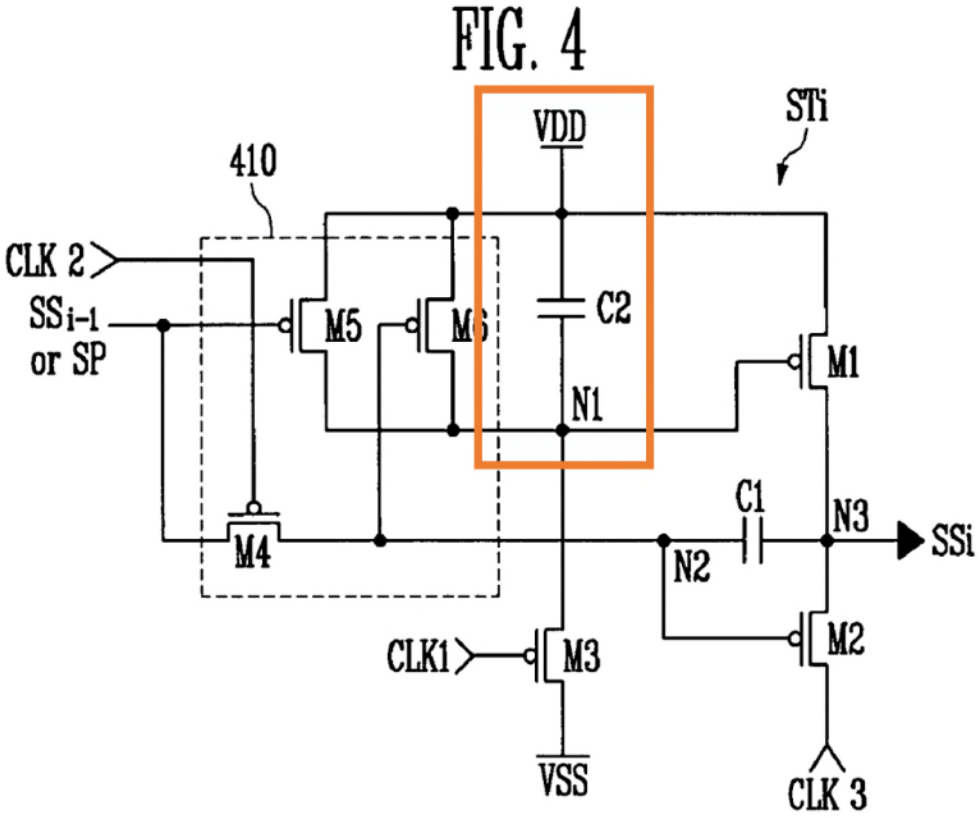
714. Thus, a POSITA looking at the circuitry of Tobita would realize that these vulnerabilities exist. Further, even though Tobita states that the capacitor C1 is included for the purpose of "bootstrapping" the second node (N1), a capacitor at this location in the circuitry can also make the charge on the second node (N1) more robust when that node is charged up and is then electrically isolated from the rest of the circuitry.

715. Thus, it would be a relatively straightforward decision to conclude that the first node (N2) in Tobita should have a capacitor included and connected to it – for the reasons just cited above.

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716. One simple method for adding a capacitor to accomplish this would be to connect that capacitor between the first node (N2) (the required connection) and a DC power supply voltage (the optional-location-choice connection).

717. A simple example of this insertion is provided by Jeong, at Figure 4:



Ex. 1007, Fig. 4 (annotation added). As can be seen by inspection, when the transistors M5 and M6 are turned off, the node N1 is electrically isolated – and will retain the charge (and thus the corresponding voltage) that is present there. For the reasons detailed above (i.e., increasing the robustness of the voltage that is present at the node N1), the capacitor C2 is added. As Jeong explains,

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> The second capacitor C2 may be coupled between the first power supply VDD and the first node N1. The second capacitor C2 may *function to reduce a variation of a voltage*, which may be applied to the first power supply VDD or the first node N1.

Id., ¶ [0057] (emphasis added).

This is a description of the enhanced robustness of the voltage present at the node N1, consistent with what was discussed above.

718. In addition, another prior art reference, Moon (Ex. 1020) also explicitly recognizes these vulnerabilities – and explicitly describes the inclusion of two capacitors at the two relevant nodes (Q and QB) to mitigate these problems:

> A first capacitor CQ may be connected between the [second] node Q and an input line of the low-level driving voltage VSS for eliminating noise at the [second] node Q. Similarly, a second capacitor CBQ may be connected between the [first] node QB and the input line of the low-level driving voltage VSS for eliminating noise at the [first] node QB.

Ex. 1020, ¶ [0053].

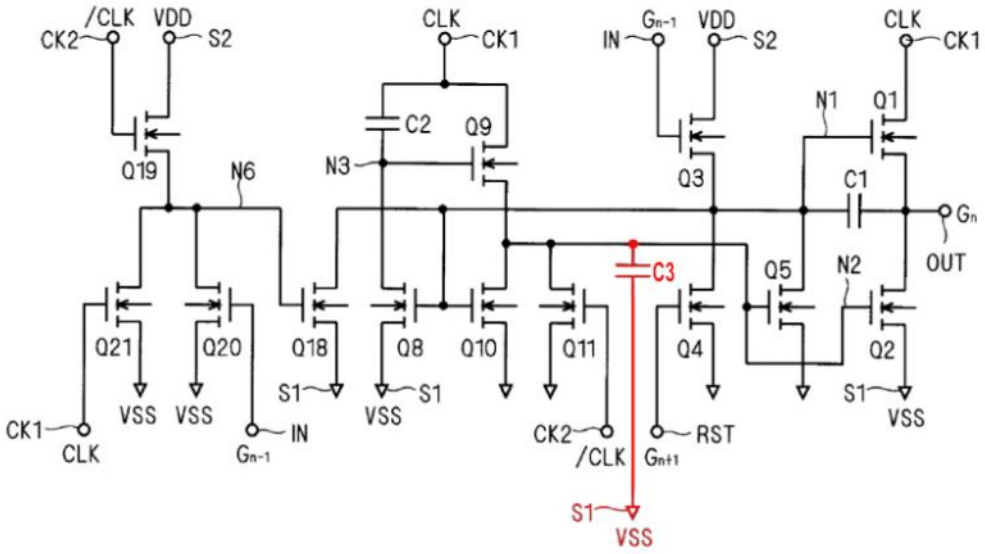
719. It is clear from the above discussion (as would be clear to a POSITA) that by "eliminating noise," Moon is referring to increasing the charge on each node by increasing the capacitance at those nodes – to make their charge states more robust against upsets (such as EMI (which, as described above, is a well-known form of noise) and interline crosstalk during digital switching events (which is also a well-known form of noise)). In the same manner as that just shown with respect to Jeong,

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Moon is describing enhanced robustness of the voltage present at the nodes Q and QB, consistent with what was discussed above.

720. As an example, this capacitor could be added to the circuitry of Figure 20 of Tobita in the following manner:

FIG. 20

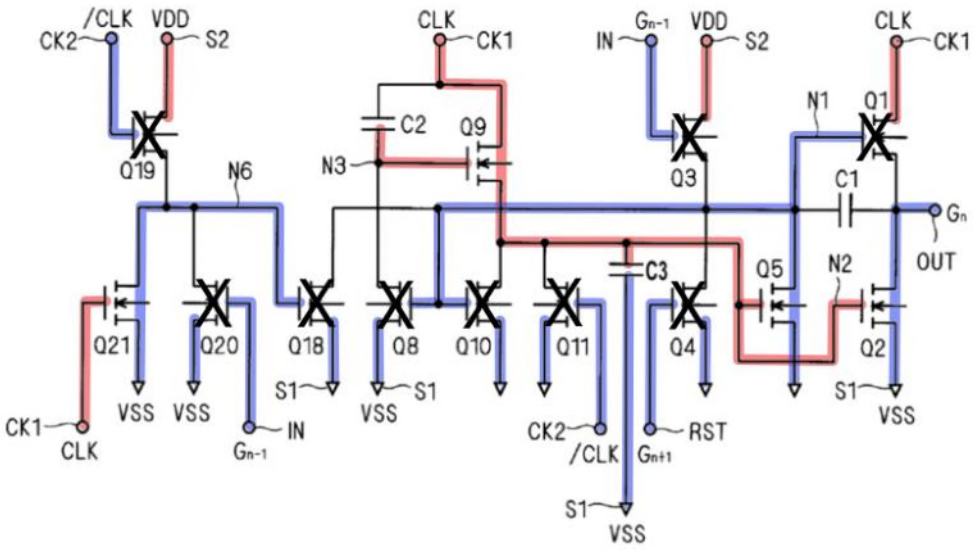


(Highlighted added capacitor in red.) This capacitor is connected between the first node and the first power supply.

721. When the first node (N2) is charged up, the endpoint voltage will not change (as long as enough time is allowed for the charging-up of the first node to reach completion).

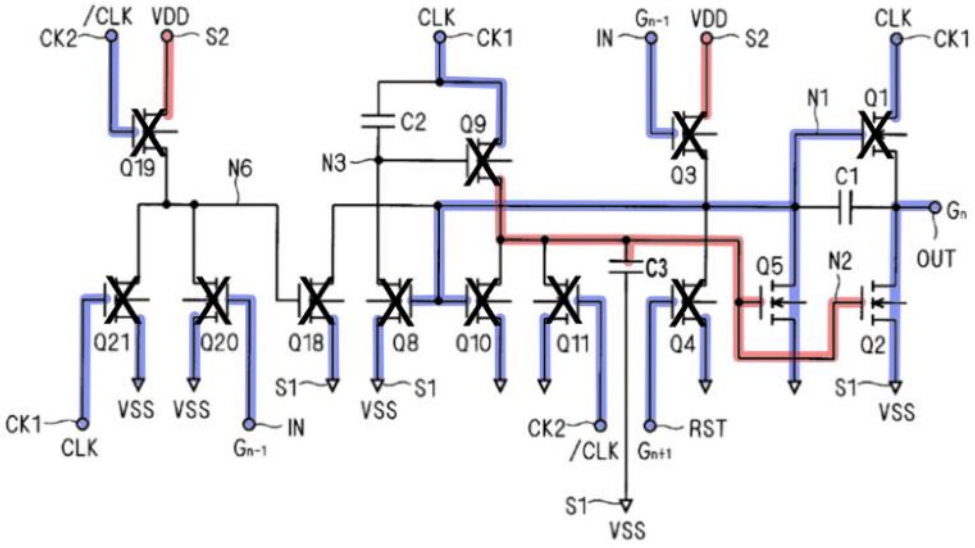
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FIG. 20



However, when the first node is isolated and floating (that is, as described above, when transistors Q9, Q10, and Q11 are all turned off), the situation is somewhat different from that which was present when the capacitor C3 is not included.

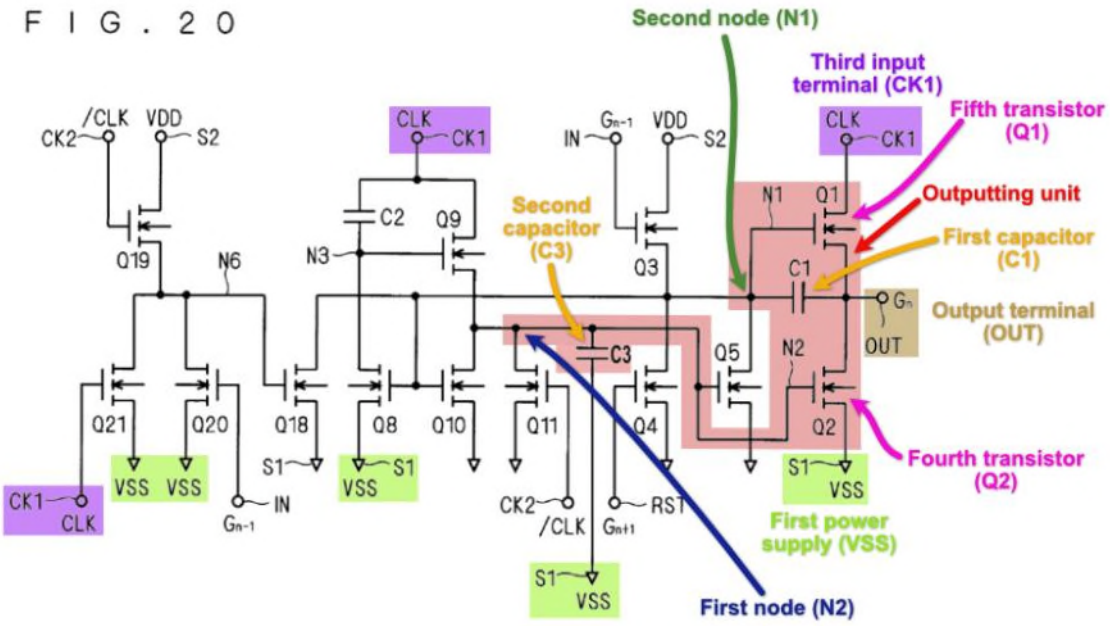
FIG. 20



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As per the discussion above regarding the relationship among charge, capacitance, and voltage (i.e., $Q = CV$), here – due to the larger capacitance (C) – the voltage (V) will involve a larger amount of charge (Q). Therefore, when the first node (N2) is isolated and floating (i.e., when as described above, transistors Q9, Q10, and Q11 are all turned off), the inclusion of capacitor C3 will provide the benefits (in terms of signal integrity and voltage retention) that were discussed above.

722. When this second capacitor is added, the combined embodiment now includes the "second capacitor [C3] between the second node [N1] and the first power supply [VSS]" – as required by Claim 7:



723. Thus, Tobita, in view of Jeong and the knowledge of a POSITA, renders obvious this claim of the '593 patent.

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3. Dependent Claim 21

724. As an initial matter, Claim 21 depends from Claim 18, which depends from Claim 17, which depends from Claim 15; as was shown above (in Section XII.D), Claim 15, Claim 17, and Claim 18 of the ’593 patent are disclosed by Tobita.

725. This claim is identical to Claim 7 of the ’593 patent – which was discussed just above (in Section XII.E.2).

726. Thus, Tobita, in view of Jeong and the knowledge of a POSITA, renders obvious this claim of the ’593 patent.

XIII. SECONDARY CONSIDERATIONS

727. If I later become aware of arguments of any secondary considerations in this proceeding, I may assess those arguments when they arise, in order to reach conclusions and form opinions regarding their correctness or incorrectness; I reserve the right to file supplemental declarations as necessary should such circumstances occur. In any event, it is my conclusion and opinion that, even if Patent Owner proffers evidence of secondary considerations of non-obviousness, such evidence cannot overcome the showing of obviousness through the prior art references that were analyzed in this Declaration.

XIV. CONCLUSION

728. As per the analysis presented above, it is my conclusion and opinion that Claims 1-8, 14-22, and 25 of the ’593 patent are unpatentable. It is thus my

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further conclusion and opinion that IPR proceedings regarding the ’593 patent should be instituted, and that the challenged claims should be cancelled as unpatentable.

729. I am aware that this declaration will be filed as evidence in an IPR proceeding before the PTAB. I am aware that making willfully false statements in my declaration are punishable by fine or imprisonment, or both (under 18 U.S.C. § 1001), and that such actions may compromise the validity of the IPR Petition. All statements herein made by me of my own knowledge are true, and all statements made on information and belief are believed to be true.

730. I declare under penalty of perjury that the foregoing is true and correct. Executed this 6th day of March, 2024 in Fletcher, Vermont.



Daniel Foty, Ph.D.

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APPENDIX A

DANIEL FOTY, Ph.D.

SUMMARY

Dr. Foty has more than 30 years of engineering and management experience in the mainstream of the technology industry. During this time, he has worked in semiconductor physics, device design, process integration, modeling/simulation (process, device, and circuit), circuit design/analysis, and wireless communications. After seven years at the microelectronics unit of IBM, he founded his own consulting firm, Gilgamesh Associates, LLC, which works in very demanding areas of technology design and development such as analog, mixed-signal, RF, signal processing, wireless communications, and ultra-low-power design.

Dr. Foty is also an advisor to the Tallinn University of Technology (Estonia) and the University of Pretoria (South Africa). He is also the author of *MOSFET Modeling with SPICE: Principles and Practice*, the more-recent *Moore's Law: The Untold* Story, and several other books. He has also authored well over 100 journal articles and conference presentations, and is a frequent plenary (keynote) speaker at major international conferences throughout the world. He is also a licensed pilot and aircraft owner, possesses both an instrument rating and a seaplane rating, and is a registered "angel pilot" with Patient Airlift Services.

Expertise

- Analog/Mixed-Signal/RF CMOS
- CMOS Integrated Circuit Design
- IC Modeling/Simulation
- CMOS Technology and Process Integration
- Semiconductor Manufacturing/Fabrication
- Nanotechnology
- Design Automation (EDA) Software
- Semiconductor Memory (DRAM, SRAM, Flash)
- Semiconductor Physics
- RF/Radio Technology, Wireless Networks, and Wireless Communications
- Power Management
- Digital Communications, Signal Integrity, and Electromagnetic Interference
- Cryogenic Electronics

PROFESSIONAL EXPERIENCE

1994 to Present **Gilgamesh Associates, LLC**
President

- Analysis of analog/mixed-signal/RF CMOS circuits
- New technologies in high-speed wireless data communications
- Specialized process-design-kits (PDKs) for circuit design/simulation
- Foundry interfacing for fabless IC design companies
- Professional education via short courses and lectures
- Litigation support in various aspects of the integrated circuit industry

1988 to 1994 **IBM Microelectronics Division**
Scientist/Engineer

- Process integration, device design, semiconductor/IC physics
- Process and device simulation; circuit simulation
- Process and device integration for memory and logic technologies
- Process-design-kits (PDKs) for circuit simulation
- Spearheaded initial IBM foray into OEM foundry market; responsible for all "external customer" PDKs and support/interfacing; business grew from nothing to $66M in revenue in first year.

EDUCATION

Ph.D., Materials Science, University of Vermont, 2001
MS, Electrical Engineering, University of Illinois, 1985
BS, Physics and Chemistry, Bates College, 1983

LITIGATION RELATED EXPERIENCE

Dr. Foty has served as a testifying expert, and provided declarations, expert reports, trial testimony, and arbitration-hearing testimony for cases that have touched on the complete spectrum of semiconductor/electronics engineering issues, electronic design automation software, wireless technology, contract interpretations and business processes, and prior art searches in both patents and the public-domain literature. He has also served as a consulting expert. Dr. Foty has been deposed some thirty times, and has testified at trial six times. Below are matters in which he has written expert reports and given testimony either at deposition, trial, or before an arbitration panel.

Type of Matter:	*Inter Partes* review involving power conversion technology in solar power systems
Law Firm:	Sheridan Ross LLP, Denver, Colorado
Case Name:	SolarEdge Technologies, Ltd. v. Koolbridge Solar, Inc.
Represented:	Patent holder
Case Number:	IPR2022-00007, -00010, -00013
Filing Date:	10/11/2021, 10/11/2021, 10/8/2021
Court:	Patent Trial and Appeal Board
Disposition:	Prepared three declarations supporting the patent holder; deposed; ongoing.
Date:	June 2022 – present.

Type of Matter:	Patent infringement involving wireless communications technology
Law Firm:	Folio Law Group, LLP, Seattle, Washington
Case Name:	Dali Wireless v. Corning
Represented:	Patent holder
Case Number:	6:20-cv-00827-ADA
Filing Date:	10/22/2020
Court:	US District Court District of the Western District of Texas
Disposition:	Prepared an expert report, deposed; ongoing.
Date:	November 2021 – present.

Type of Matter:	Patent infringement involving integrated circuit layout for lithographic control
Law Firm:	Jones Day LLP, Chicago, Illinois
Case Name:	NXP Semiconductors v. Impinj
Represented:	Plaintiff
Case Number:	2:20-cv-01503-RSM-SKV337-TA-1272
Filing Date:	10/7/2020
Court:	US District Court of the Western District of Washington,
Disposition:	Ongoing.
Date:	November 2021 – present.

Type of Matter:	Patent infringement involving integrated circuit technology
Law Firm:	Jones Day LLP, Washington DC (ITC matter)
Case Name:	MediaTek v. NXP Semiconductors
Represented:	Respondent
Case Number:	337-TA-1272
Filing Date:	6/21/2021
Court:	International Trade Commission
Disposition:	Ongoing.
Date:	April 2021 – present.

Type of Matter:	Patent infringement involving portable vehicle battery jump starters
Law Firm:	Fox Rothschild LLP, Philadelphia, Pennsylvania (ITC matter)
Case Name:	The Noco Company v. Deltran Global
Represented:	Respondent
Case Number:	337-TA-1256
Filing Date:	1/19/2021
Court:	International Trade Commission
Disposition:	Prepared an expert report; deposed; plaintiff withdrew complaint against Deltran.
Date:	June 2021 – November 2021.

Type of Matter:	Patent infringement involving integrated circuit technology and signal integrity
Law Firm:	Jones Day LLP, Chicago, Illinois
Case Name:	WSOU v. Xilinx
Represented:	Respondent
Case Number:	1:20-cv-01228-CFC; 1:20-cv-01229-CFC
Filing Date:	09/16/2020
Court:	US District Court District of Delaware
Disposition:	Ongoing.
Date:	April 2021 – present.

Type of Matter:	Patent infringement involving wireless communications technology
Law Firm:	Folio Law Group, LLP, Seattle, Washington
Case Name:	Dali Wireless v. JMA
Represented:	Patent holder
Case Number:	1:19-cv-02367-RGA
Filing Date:	12/30/2019
Court:	US District Court District of Delaware
Disposition:	Settled.
Date:	March 2021 – November 2021.

Type of Matter:	Patent infringement involving wireless communications technology
Law Firm:	Folio Law Group, LLP, Seattle, Washington

Case Name:	Dali Wireless v. Commscope
Represented:	Patent holder
Case Number:	1:19-cv-00952
Filing Date:	5/22/2019
Court:	US District Court District of Delaware
Disposition:	Prepared an expert report; deposed; ongoing.
Date:	March 2021 – present.
Type of Matter:	Patent infringement involving integrated circuit technology (ITC matter)
Law Firm:	Troutman Pepper LLP, Boston, Massachusetts
Case Name:	Tela v. Intel
Represented:	Patent holder
Case Number:	337-TA-1246
Filing Date:	12/18/2020
Court:	International Trade Commission
Disposition:	Settled; this includes all prior disputes between the parties
Date:	March 2021 – April 2021.
Type of Matter:	Patent infringement involving wireless battery charging and discharging
Law Firm:	Feinberg Day Kramer Alberti Limtonkovich & Belloli LLP
Case Name:	Garrity Power Services v. Samsung
Represented:	Patent holder
Case Number:	2:20-cv-00269-JRG
Filing Date:	08/17/2020
Court:	US District Court Eastern District of Texas
Disposition:	Case dismissed by the Court
Date:	October 2020 – March 2022.
Type of Matter:	*Inter Partes* review involving wireless battery charging and discharging
Law Firm:	Spencer Fane LLP, Plano, Texas
Case Name:	Samsung v. Garrity Power Services
Represented:	Patent holder
Case Number:	IPR2021-00389
Filing Date:	12/31/2020
Court:	Patent Trial and Appeal Board
Disposition:	Prepared a declaration; PTAB denied institution.
Date:	October 2020 – July 2021.
Type of Matter:	Patent infringement involving MOS transistor design and MOS transistor manufacturing processes
Law Firm:	Fish & Richardson LLP, Boston, Massachusetts
Case Name:	Innovative Foundry Technologies v. SMIC, Broadcom, Cypress Semiconductor, and Dish Network
Represented:	Respondents

Case Number:	6:19-cv-00719-ADA
Filing Date:	12/20/2019
Court:	US District Court Western District of Texas
Disposition:	Settled
Date:	June 2020 – April 2021.
Type of Matter:	Patent infringement involving digital communications integrated circuit technology
Law Firm:	Morrison & Foerster LLP, Los Angeles, California
Case Name:	Analog Devices v. Xilinx
Represented:	Respondent
Case Number:	1:19-cv-02225-RGA
Filing Date:	12/05/2019
Court:	US District Court District of Delaware
Disposition:	Ongoing.
Date:	April 2020 – present.
Type of Matter:	Patent infringement involving integrated circuit technology
Law Firm:	Pepper Hamilton LLP, Boston, Massachusetts
Case Name:	Intel v. Tela
Represented:	Respondent
Case Number:	3:18-cv-02848-WHO
Filing Date:	05/15/2018
Court:	US District Court Northern District of California
Disposition:	Prepared two expert reports; deposed; matter settled.
Date:	March 2019 – April 2021.
Type of Matter:	Patent infringement involving integrated circuit technology (ITC matter)
Law Firm:	Mintz, Levin, Cohn, Ferris, Glovsky and Popeo, P.C., Boston, Massachusetts
Case Name:	Globalfoundries v. TSMC
Represented:	Patent holder
Case Number:	337-TA-1177
Filing Date:	08/26/2019
Court:	International Trade Commission
Disposition:	Settled.
Date:	August 2019 – October 2019.
Type of Matter:	*Inter Partes* review involving wireless/RF technology
Law Firm:	Jones, Day LLP, Cleveland, Ohio
Case Name:	Intel v. Qualcomm
Represented:	Patent holder
Case Number:	IPR2019-00128, IPR2019-00129, IPR2019-00047, IPR2019-00048, IPR2019-00049
Filing Date:	11/8/2018
Court:	Patent Trial and Appeal Board

Disposition:	Prepared five declarations supporting patent owner responses; deposed; PTAB upheld all challenged claims of the patent as valid.
Date:	June 2019 – July 2020.
Type of Matter:	Patent infringement involving integrated circuit technology
Law Firm:	Pepper Hamilton LLP, Boston, Massachusetts
Case Name:	Tela v. Intel
Represented:	Patent holder
Case Number:	337-TA-1148
Filing Date:	12/19/2018
Court:	International Trade Commission
Disposition:	Prepared two declarations supporting claim construction; prepared an expert report; deposed; testified at the hearing/trial in December 2019.
Date:	March 2019 – December 2019.
Type of Matter:	Patent infringement involving RF/wireless technology
Law Firm:	Quinn Emanuel Urquhart & Sullivan LLP, New York, New York
Case Name:	Qualcomm v. Apple
Represented:	Patent holder
Case Number:	3:17-cv-02402-CAB-MDD
Filing Date:	12/29/2017
Court:	US District Court Southern District of California
Disposition:	Settled.
Date:	January 2018 – December 2018.
Type of Matter:	Patent infringement involving RF/wireless technology
Law Firm:	Quinn Emanuel Urquhart & Sullivan LLP, New York, New York
Case Name:	Qualcomm v. Apple
Represented:	Patent holder
Case Number:	337-TA-1093
Filing Date:	7/7/2017
Court:	International Trade Commission
Disposition:	Prepared two expert reports regarding RF-IC/wireless technology; deposed; testified at the hearing/trial in September 2018.
Date:	January 2018 – September 2018.
Type of Matter:	Patent infringement involving integrated circuit technology and printed-circuit board technology
Law Firm:	Dovel and Luner, LLP, Santa Monica, California
Case Name:	X2Y v. Intel
Represented:	Patent holder
Case Number:	3:18-cv-01394-HZ
Filing Date:	07/25/2018
Court:	US District Court District of Oregon
Disposition:	Prepared a declaration supporting claim construction; deposed; case settled.

Date:	June 2017 – December 2019.
Type of Matter:	Patent infringement involving integrated circuit technology
Law Firm:	Jones, Day LLP, San Francisco, California, and Slater Matsil LLP, Dallas, Texas
Case Name:	IPBridge v. Xilinx
Represented:	Respondent
Case Number:	3:17-cv-06376-JD
Filing Date:	11/01/2017
Court:	US District Court Northern District of California
Disposition:	Settled.
Date:	February 2017 – February 2019.
Type of Matter:	Patent infringement involving analog circuits
Law Firm:	Covington & Burling LLP, San Diego, California
Case Name:	Tessera v. Broadcom
Represented:	Patent holder
Case Number:	1:16-cv-00380-LPS-CJB
Filing Date:	05/23/2016
Court:	US District Court District of Delaware
Disposition:	Settled.
Date:	December 2016 – December 2017.
Type of Matter:	Patent infringement involving integrated circuit design methods and integrated circuit design-automation software
Law Firm:	Jones, Day LLP, Cleveland, Ohio
Case Name:	Synopsys v. ATopTech
Represented:	Patent holder
Disposition:	Prepared an expert report; deposed; matter was suspended when ATopTech filed for Chapter 11 bankruptcy.
Date:	June 2016 – March 2017.
Type of Matter:	Patent infringement involving integrated circuit process/manufacturing technology for wireless communications
Law Firm:	McKool Smith, LLP, Dallas, Texas
Case Name:	Ericsson v. TCL
Represented:	Plaintiff
Disposition:	Prepared an expert report regarding the costs and timelines associated with the development of integrated circuits for wireless communications, and the related difficulties encountered; trial was stayed when an IPR proceeding began, matter has since ended.
Date:	November 2015 – March 2016.
Type of Matter:	*Inter Partes* review involving integrated circuit design methods and integrated circuit design-automation software
Law Firm:	Jones, Day LLP, Cleveland, Ohio
Case Name:	ATopTech v. Synopsys

Represented:	Patent holder
Disposition:	Prepared two declarations; deposed.
Date:	November 2014 – January 2016.
Type of Matter:	*Inter Partes* review involving a semiconductor flash memory technology patent
Law Firm:	Aka Chan LLP, Santa Clara, California
Case Name:	Silicon Motion Technology Corp. v. Phison Electronics Corp.
Represented:	Petitioner
Disposition:	Prepared a declaration; deposed; hearing before the PTAB in September 2014, PTAB ruled completely in Petitioners' favor
Date:	May 2014 – September 2014.
Type of Matter:	Patent infringement involving integrated circuit design
Law Firm:	Bragalone, Conroy, PC, Dallas, Texas
Case Name:	HSM v. Elpida Memory et al. (was HSM v. Fujitsu et al.)
Represented:	Plaintiff
Disposition:	Prepared numerous declarations and two expert reports; deposed; all respondents eventually settled.
Date:	February 2012 – February 2016.
Type of Matter:	Patent infringement involving integrated circuit process/manufacturing technology (ITC matter)
Law Firm:	McKool Smith, LLP, Dallas, Texas
Case Name:	Samsung v. Ericsson
Represented:	Defendant
Disposition:	Was assigned one patent in a larger matter, having done much original engineering work on the technology in question; produced extensive background prior art (having created much of it), demonstrated that the accused technology clearly did not practice the teachings of the patent, and clearly showed that the aforementioned prior art would call the patent's validity seriously into question; plaintiff dropped that patent from the action.
Date:	January 2013 – May 2013.
Type of Matter:	Patent infringement involving integrated circuit design, with a focus on RF-ICs for wireless communications
Law Firm:	Antonelli, Harrington, & Thompson, LLP, Houston, Texas
Case Name:	Semiconductor Ideas to the Market, BV v. Texas Instruments et al.
Represented:	Plaintiff
Disposition:	Prepared a declaration for pre-hearing; major defendant (Qualcomm) settled following this expert's examination of their Confidential Business Information (CBI) in June, 2012; other defendants settled shortly thereafter.
Date:	May 2012 – August 2012.
Type of Matter:	Bond forfeiture proceeding (ITC matter)

Law Firm:	Adduci, Mastriani, & Schaumberg, LLP, Washington, D.C.
Case Name:	Tessera v. Freescale
Represented:	Plaintiff
Disposition:	Following unfavorable ITC ruling, respondent argued that posted bond (pending final disposition) should be returned to them; prepared a declaration for hearing; ITC ruled against respondent, who then agreed to cease litigation and forfeit the bond.
Date:	April 2012 – October 2012.
Type of Matter:	Theft of trade secrets involving integrated circuit design, manufacturing, and characterization technology
Law Firm:	Shore, Chan, Bragalone, and DePumpo, LLP, Dallas, Texas
Case Name:	Xicor v. SST
Represented:	Plaintiff
Disposition:	Prepared a declaration for hearing regarding plaintiff's identification of its trade secrets; following favorable ruling on this, defendant agreed to settle on terms favorable to the plaintiff
Date:	February 2012 – September 2012.
Type of Matter:	Patent infringement in integrated circuit substrates (ITC matter)
Law Firm:	Alston + Bird, LLP, Atlanta, Georgia
Case Name:	X2Y v. Intel
Represented:	Plaintiff
Disposition:	Consulted on technology involved
Date:	August 2011 – August 2012.
Type of Matter:	Theft of trade secrets involving design of power management integrated circuits (ITC enforcement proceeding)
Law Firm:	Alston + Bird, LLP, Menlo Park, California
Case Name:	Richtek v. uPI, and Sapphire Technology
Represented:	Plaintiff
Disposition:	Prepared an expert report and a supplemental expert report; deposed; testified at hearing/trial; subsidiary respondent Sapphire settled and exited the case shortly before trial.
Date:	June 2011 – March 2012; follow-on district/superior court cases temporarily stayed, but pending.
Type of Matter:	Patent infringement in switching power supplies
Law Firm:	McDermott, Will & Emery, LLP, Miami, Florida
Case Name:	Power Integrations, Inc. v. Fairchild Semiconductor International, Inc.
Representing:	Defendant
Disposition:	Presented the tutorial at the Markman hearing in San Jose, California (Northern District of California) in March; matter ongoing, but no longer involved.
Date:	December 2010 – March 2011.

Type of Matter:	Patent infringement in the power management methodologies of portable/mobile device (ITC matter)
Law Firm:	Finnegan, Henderson, Farabow, Garrett & Dunner, LLP, Washington, D.C.
Case Name:	HTC v. Apple
Represented:	Plaintiff
Disposition:	Deposed in March; testified at trial/hearing (ITC) in May; outcome pending.
Date:	November 2010 – May 2011.

Type of Matter:	Theft of trade secrets involving design of power management integrated circuits (ITC matter)
Law Firm:	Alston + Bird, LLP, Menlo Park, California
Case Name:	Richtek v. uPI, AMD, Sapphire Technology, Diamond Multimedia, and XFX Technology
Represented:	Plaintiff
Disposition:	Prepared an expert report and a supplemental expert report; deposed twice (three days total); subsidiary respondents settled and exited the case during May 2010 – July 2010; main respondent uPI agreed on 21 July 2010 to a Consent Order that included a ten-year ban on importation of the accused products to avoid an ITC hearing.
Date:	January 2010 – July 2010; ITC enforcement proceeding opened against uPI and Sapphire, June 2011 – March 2012 (see above); follow-on district/superior court cases temporarily stayed, but pending.

Type of Matter:	Patent infringement and theft of trade secrets involving integrated circuit manufacturing
Law Firm:	Keker and Van Nest, LLP, San Francisco, California
Case Name:	TSMC v. SMIC
Represented:	Plaintiff
Disposition:	Deposed; testified at trial September 2009; jury returned guilty verdict on all 18 counts; parties settled during damages phase of trial.
Date:	July 2007 – September 2009.

Type of Matter:	Theft of Trade Secrets
Law Firm:	Baker & McKenzie, LLP, San Diego, California
Case Name:	Neology Inc. v. B. Roesner et al.
Represented:	Plaintiff
Disposition:	Reviewed materials produced during discovery and found considerable facially-labeled trade secret material in the possession of the defendant. Case Settled
Date:	April 2007 – May 2007

Type of Matter:	Theft of Trade Secrets
Law Firm:	Weil, Gotshal, and Manges, LLP, New York, New York
Case Name:	Synopsys v. Nassda
Represented:	Defendant
Disposition:	Wrote an expert report on behalf of defendant but was not deposed. Case Settled
Date:	September 2003 - August 2004

Type of Matter:	Theft of Trade Secrets
Law Firm:	Howrey, Simon, Arnold & White, LLP, Menlo Park, California
Case Name:	Silvaco, Inc. v. Circuit Semantics, Inc.
Represented:	Defendant
Disposition:	Wrote an expert report on behalf of defendant and was deposed. Case Settled
Date:	February 2003 - September 2003

Type of Matter:	Contract dispute, Copyright Infringement, and Theft of Trade Secret matter involving integrated circuit design tools
Law Firm:	Russo & Hale, LLP, Palo Alto, California
Case Name:	Virtual Silicon Technology, Inc. v. Library Technologies, Inc.,
Represented:	Plaintiff
Disposition:	On behalf of plaintiff, wrote an expert report, was deposed and testified at arbitration hearing. Decision of binding arbitration released in November 2003; all findings-of-fact in favor of the plaintiff.
Date:	December 2002 - November 2003

PUBLICATIONS

Books

1. D. Foty, "Moore's Law: The Untold Story," August 2017.

2. D. Foty, "The Rise and Fall of Classical Athens: A Short History," January 2018.

3. D. Foty, "Thomas Seebeck: His Life and Science," September 2018.

4. D. Foty, "Essential Digital, Analog, and Semiconductor Electronics Technology," Chapter 19 in *Concise Higher Electrical Engineering* (ed. by E. Chikuni, M. Khan, and O. Okoro), Juta Academic, 2008.

5. D. Foty, *MOSFET Modeling with SPICE: Principles and Practice*, Prentice-Hall (now Pearson Education), 1997 (now in its third printing; Vietnamese-language edition published in 2006).

6. Proceedings of the Symposium on Low Temperature Electronics and High Temperature Superconductors (ed. by S. Raider, C. Claeys, D. Foty, T. Kawai, and R. Kirschman) (published in October 1993).

7. Proceedings of the Symposium on Low Temperature Electronic Device Operation (ed. by D. Foty) (published in December 1991).

Guest Journal Editor

1. Guest editor, special issue on Low Voltage/Low Power Design, Analog Integrated Circuits and Signal Processing, December 1999.

Refereed Journal Publications

1. D. Foty, "Nanoscale Electron Devices: Difficulties, Granularities, and Applications" (Invited Paper), Romanian Journal of Information Sciences and Technology, (published by the Romanian Academy of Sciences), January 2009, vol. 12(3), pp. 317 – 338.

2. D. Foty, "An Evaluation of Deep-Submicron CMOS Design Optimized for Operation at 77K" (Invited Paper), Analog Integrated Circuits and Signal Processing vol. 49, pp. 97 – 105 (2006).

3. D. Foty and K. Runge, "What's Ahead in High-Speed Wireless Data Communications? The Future Will Be Better Tomorrow – And Different Than What We've Been Expecting" (Invited Paper), the African Journal of Information and Communications Technology (online publication).

4. S. Terry, J. Rochelle, D. Binkley, B. Blaylock, D. Foty, and M. Bucher, "Comparison of a BSIM3V3 and EKV MOST Model for a 0.5μm Process and Implications for Analog Circuit Design," IEEE Transactions on Nuclear Science vol. NS-50, pp. 915 - 920 (2003).

5. D. Binkley, C. Hopper, S. Tucker, B. Moss, J. Rochelle, and D. Foty, "A CAD Methodology for Optimizing Transistor Current and Sizing in Analog CMOS Design," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems vol. CAD-22, pp. 225 – 237 (2003).

6. D. Foty, "Perspectives on Analytical Modeling of Small Geometry MOSFETs in SPICE for Low Voltage/Low Power CMOS Circuit Design" (Invited Paper), Analog Integrated Circuits and Signal Processing vol. 21, pp. 229 – 252 (1999).

7. D. Foty, "Taking a Deep Look at Analog CMOS," IEEE Circuits and Devices, March 1999, pp. 23 – 28.

8. D. Foty, "MOSFET Modeling for Circuit Simulation: Where Do We Go From Here?," IEEE Circuits and Devices, July 1998, pp. 26 – 31.

9. G. Gildenblat and D. Foty, "Low Temperature Models of Metal-Oxide-Semiconductor Field-Effect Transistors" (Invited Paper), The International Journal of High Speed Electronics and Systems vol. 6, pp. 317 - 373 (1995).

10. D. Foty and E. Nowak, "MOSFET Technology for Low Voltage/Low Power Applications" (Invited Paper), IEEE Micro, June 1994, pp. 68 - 77.

11. D. Foty, P. Wyns, and K. Oughstun, "On the Propagation of Short Optical Pulses in a Linear Dispersive Medium," IEEE Journal of Quantum Electronics vol. 28, pp. 1619 - 1622 (1992).

12. E. Farrell, P. Appino, D. Foty, and T. Linton, "Visual Interpretation of Multi-Dimensional Computations and Transistor Design," IBM Journal of Research and Development vol. 35, pp. 26 - 44 (1991).

13. D. Foty, "Impurity Ionization in MOSFETs at Very Low Temperatures," Cryogenics vol. 30, pp. 1056 - 1063 (1990).

14. D. Cole, E. Buturla, S. Furkay, K. Varahramyan, J. Slinkman, J. Mandelman, D. Foty, O. Bula, A. Strong, J. Park, T. Linton, J. Johnson, M. Fischetti, S. Laux, P. Cottrell, H. Lustig, F. Pileggi, and D. Katcoff, "The Use of Simulation in Semiconductor Technology Development" (Invited Paper), Solid State Electronics vol. 33, pp. 591 - 623 (1990).

15. K. Oughstun, P. Wyns, and D. Foty, "Numerical Determination of the Signal Velocity in Linear Dispersive Pulse Propagation," Journal of the Optical Society of America A vol. 6, pp. 1430 - 1440 (1989).

16. P. Wyns, D. Foty, and K. Oughstun, "Numerical Analysis of the Precursor Fields in Dispersive Pulse Propagation," Journal of the Optical Society of America A vol. 6, pp. 1421 - 1429 (1989).

17. D. Foty, "Thermal Effects in p-Channel MOSFETs at Low Temperatures," IEEE Transactions on Electron Devices vol. 36, pp. 1542 - 1544 (1989).

18. D. Foty and S. Titcomb, "Thermal Effects in n-Channel Enhancement MOSFETs Operated at Cryogenic Temperatures," IEEE Transactions on Electron Devices vol. 34, pp. 107 - 114 (1987).

Refereed Conference Proceedings

1. D. Foty, "Amplification, Feedback, and Sub-Biasing: Applying Analog Techniques to High-Speed, Low-Power Digital CMOS Circuits," *Invited Conference Plenary Lecture,* Proceedings of the 13th International Symposium on Signals, Circuits, and Systems, pp. 123 - 128 (published July 2017).

2. D. Foty, "The Future of 'Moore's Law' – Does It Have One?" *Invited Conference Plenary Lecture,* Proceedings of the 11th International Symposium on Signals, Circuits, and Systems, pp. 1 - 8 (published July 2013).

3. D. Foty, "The Future of 'Moore's Law' – Does It Have One?" *Invited Conference Plenary Lecture*, Proceedings of the 13th Baltic Electronics Conference, pp. 21 – 26 (published October 2012).

4. D. Foty, B. Smith, S. Sinha, and M. Schröter, "Expanding Wireless Bandwidth in a Power-Efficient Way: Developing a Viable mm-Wave Radio Technology," *Invited Conference Plenary Lecture*, Proceedings of the 10th IEEE East-West Design and Test Symposium, pp. 264 - 269 (published September 2012).

5. D. Foty, B. Smith, S. Sinha, and M. Schröter, "The Wireless Bandwidth Crisis and the Need for Power-Efficient Bandwidth," (Invited Paper), Proceedings of the 10th International Symposium on Signals, Circuits, and Systems, pp. 275 - 279 (published July 2011).

6. D. Foty, "Breaking the Entropy Addiction: Understanding Power Consumption and Overcoming It," *Invited Conference Plenary Lecture*, Proceedings of Africon2009, Proceedings on DVD (published September 2009).

7. B.C. Mabuza, S. Sinha and D. Foty, "On-chip Impedance Tuning for mm-wave Applications,"• Proceedings of the South African Conference on Semiconductor and Superconductor Technology, pp. 49 – 53 (published April 2009).

8. D. Foty, S. Sinha, M. Weststrate, C. Coetzee, A. Uys, and E. Sibanda, "mm-Wave Radio Communications Systems: The Quest Continues," *Invited Conference Plenary Lecture*, Proceedings of the International Radio Electronics Forum, pp. 14 – 17 (published October 2008).

9. D. Foty, "Prospects for Nanoscale Electron Devices: Some Little-Recognized Problems," *Invited Conference Plenary Lecture*, Proceedings of the 31st Conference on Semiconductor Physics, pp. 3 – 13 (published October 2008).

10. D. Foty, "Nanoscale Electron Devices: The Untold Technology Story," *Invited Conference Plenary Lecture*, Proceedings of the 11th Baltic Electronics Conference, pp. 59 - 69 (published October 2008).

11. D. Foty**,** "Next-Generation Wireless Networks: A New World, From Bottom to Top," *Invited Conference Keynote Lecture*, Proceedings of Africon2007, Proceedings on DVD (published September 2007).

12. D. Foty, "Next-Generation Wireless Networks: New Building Blocks and New Network Topologies," *Invited Conference Plenary Lecture*, Proceedings of the International Conference on Dependable Systems, Services, and Technologies, pp. 220 - 228 (published April 2007).

13. D. Foty, "Factors in High-Speed Wireless Data Networking – New Ideas and a New Perspective," Invited Conference Plenary Lecture, Proceedings of the East-West Design and Test Workshop, pp. 29 - 38 (published September 2006).

14. D. Foty, "New Directions in Technology for High-Speed Wireless Data Communications," Invited Conference Plenary Lecture, Proceedings of the 13th International Conference on the Mixed Design of Integrated Circuits and Systems, pp. 19 – 27 (published June 2006).

15. D. Foty and G. Gildenblat, "Fundamental Aspects of CMOS Technology: Basics, Implications, and a Roadmap to the Future" (Invited Paper), Proceedings of the International Workshop on System-on-Chip pp. xxx - xxx (published July 2005). (Paper was submitted on time but was inadvertently not included in the Proceedings volume – available upon request.)

16. D. Foty and G. Gildenblat, "Scaling Theory and 'Punctuated Equilibrium' in CMOS Technology," Invited Conference Plenary Lecture, Proceedings of the 7th International Symposium on Signals, Circuits, and Systems, pp. 1 - 8 (published July 2005).

17. D. Foty, "An Evaluation of Deep-Submicron CMOS Design Optimized for Operation at 77K" (Special Session Paper), Proceedings of the 12th International Conference on the Mixed Design of Integrated Circuits and Systems, pp. 939 - 945 (published June 2005).

18. D. Foty, "An Evaluation of Deep-Submicron CMOS Design Optimized for Operation at 77K" (Special Session Paper), Proceedings of the International Symposium on Industrial Electronics, pp. 1139 - 1144 (published June 2005).

19. D. Foty and K. Runge, ""What's Ahead in High-Speed Wireless Data Communications? The Future Will Be Better Tomorrow – And Different Than What We've Been Expecting," Invited Conference Plenary Lecture, Proceedings of the 12th International Conference on Telecommunications, (conference proceedings pages not numbered), (published May 2005).

20. D. Foty and G. Gildenblat, "Fundamental Aspects of CMOS Technology: Basics, Implications, and a Roadmap to the Future," Invited Conference Plenary Lecture, Proceedings of the 8th International Conference CADSM, pp. 21 – 28 (published February 2005).

21. D. Foty, "Perspectives on Scaling Theory and CMOS Technology – Past, Present, and Future" (Invited Paper), Proceedings of the 11th International Conference on Electronics, Circuits, and Systems, pp. 631 – 637 (published December 2004).

22. G. Gildenblat, C. McAndrew, H. Wang, W. Wu, D. Foty, L. Lemaitre and P. Bendix, "Advanced Compact Models: Gateway to Modern CMOS Design" (Invited Paper), Proceedings of the 11th International Conference on Electronics, Circuits, and Systems, pp. 638 – 641 (published December 2004).

23. P. Bendix, D. Foty, and D. Pachura, "Practical Aspects of MOS Transistor Model 'Accuracy' in Modern CMOS Technology" (Invited Paper), Proceedings of the 11th International Conference on Electronics, Circuits, and Systems, pp. 642 - 645 (published December 2004).

24. D. Foty and G. Gildenblat, "CMOS Scaling Theory – Why Our 'Theory of Everything' Still Works, and What That Means For The Future" (Invited Paper), Proceedings of the 12th International Symposium on Electron Devices for Microwave and Optoelectronic Applications, pp. 27 – 38 (published November 2004).

25. D. Foty, "Perspectives on Scaling Theory and CMOS Technology – Punctuated Equilibrium and Evolutionary Biology," Invited Conference Plenary Lecture, Proceedings of the 9th Baltic Electronics Conference, pp. 17- 24 (published October 2004).

26. D. Foty, "Re-Interpreting the MOS Transistor for the 21st Century: Generalized Methods and Their Extension to Nanotechnology," Invited Conference Plenary

Lecture, Nordic VLSI Design Conference (NorChip), pp. 8 - 15 (published November 2003).

27. D. Foty, "Re-Generalizing the MOS Transistor, for Improved Analog Design and Extension to Nanotechnology: New Rules for a New Century," Invited Conference Plenary Lecture, Proceedings of the 4th Electronic Circuits and Systems Conference, pp. 86 - 95 (published September 2003).

28. D. Foty, "Re-Thinking and Re-Generalizing the MOS Transistor: Understanding, CMOS Design, and Extension to Nanotechnology," Invited Conference Plenary Lecture, Proceedings of the 16th European Conference on Circuit Theory and Design, pp. I-16 – I-21 (published September 2003).

29. D. Foty, "Modernizing the Framework for Deep Submicron Design – For CMOS and Beyond," Invited Conference Plenary Lecture, Proceedings of the 10th International Conference on the Mixed Design of Integrated Circuits and Systems, pp. 19 - 24 (published June 2003).

30. S. Terry, J. Rochelle, D. Binkley, B. Blaylock, D. Foty, and M. Bucher, "Comparison of a BSIM3V3 and EKV MOST Model for a 0.5μm Process and Implications for Analog Circuit Design," Proceedings of the IEEE Nuclear Science Symposium, (conference proceedings pages not numbered), (published November 2002).

31. D. Foty, M. Bucher, and D. Binkley, "Re-Interpreting the MOS Transistor Via the Inversion Coefficient and the Continuum of gms/Id," Proceedings of the 9th International Conference on Electronics, Circuits, and Systems, pp. 1179 - 1182 (published September 2002).

32. M. Bucher, D. Kazazis, F. Krummenacher, D. Binkley, D. Foty, and Y. Papananos, "Analysis of Transconductances at All Levels of Inversion in Deep Submicron CMOS," Proceedings of the 9th International Conference on Electronics, Circuits, and Systems, pp. 1183 -1186 (published September 2002).

33. D. Foty, D. Binkley, and M. Bucher, "gm/Id-Based MOSFET Modeling and Modern Analog Design" (Invited Paper), Proceedings of the 9th International Conference on the Mixed Design of Integrated Circuits and Systems, pp. 55 - 58 (published June 2002).

34. D. Foty, D. Binkley, and M. Bucher, "Starting Over: gm/Id-Based MOSFET Modeling as a Basis for Modernized Analog Design Methodologies" (Invited Paper), Proceedings of the International Conference on the Modeling and Simulation of Microsystems, pp. 682 - 685 (published in April 2002).

35. D. Foty, D. Binkley, and M. Bucher, "Measurements and Modeling of MOSFET Inversion Level Over a Wide Range as a Basis for Analog Design," Proceedings of the 15th European Conference on Circuit Theory and Design, pp. I-85 – I-88 (published in August 2001).

36. D. Foty, "MOSFET Modeling for Circuit Simulation: Requiem or Recovery?," Proceedings of the 15th European Conference on Circuit Theory and Design, pp. I-81 – I-84 (published in August 2001).

37. D. Binkley, M. Bucher, and D. Foty, "Design-Oriented Characterization of CMOS Over the Continuum of Inversion Level and Channel Length," Proceedings of the 7th International Conference on Electronics, Circuits, and Systems, pp. 161 – 164 (published in December 2000).

38. D. Foty and E. Nowak, "Performance, Reliability, and Supply Voltage Reduction, with the Addition of Temperature as a Design Variable" (Invited Paper), Proceedings of the 1993 European Solid State Device Research Conference, pp. 943 - 948.

39. D. Foty and E. Nowak, "Performance/Reliability Trade-Off and Optimized nMOSFET Design for 77K CMOS Logic," Proceedings of the Symposium on Low Temperature Electronics and High Temperature Superconductors (ed. by S. Raider), pp. 89 - 95 (published in October 1993).

40. D. Foty, "The Design of Deep Submicron FETs for Low Temperature Operation" (Invited Paper), Proceedings of the Symposium on Low Temperature Electronics and High Temperature Superconductors (ed. by S. Raider), pp. 63 - 77 (published in October 1993).

41. D. Foty, H. Hanafi, P. Agnello, and H. Ho, "Mixed Schottky/p-n Junction Behavior in Diodes Produced by Outdiffusion from Polycrystalline Cobalt Disilicide," Technical Digest of the 1992 International Electron Devices Meeting, pp. 841 - 845.

42. D. Foty, "Low Temperature Electronics and Future Electron Devices" (Invited Paper), Proceedings of the Symposium on Low Temperature Electronic Device Operation (ed. by D. Foty), pp. 13 - 24 (published in December 1991).

43. D. Foty and S. Titcomb, "Freeze-Out and Field Dependent Ionization in MOSFETs at Very Low Temperatures," Proceedings of the Symposium on Low Temperature Electronics and High Temperature Superconductors (ed. by S. Raider), pp. 151 - 160 (published in March 1988).

Articles in Industry Trade Publications

1. D. Foty, "It's Time to Write Off the Past – Vermont Needs an Economic Future," Ethan Allen Institute Newsletter, November 2002. (This article was also published in the Springfield (Vt.) Reporter, the Brandon (Vt.) Bugle, the Brattleboro (Vt.) Reformer, and The Vermont Times.)

2. D. Foty and P. Bendix, "An Executive Guide to MOS Transistor Modeling," Fabless Forum, March 2002.

3. D. Foty, "Radio-Frequency Technology: Easier Said Than Done?," Fabless Forum, September 1999.

4. D. Foty, "A Traveler's Tales – An Essay on Globalization and the Culture of the 'New Economy'," Vermont Business Magazine, September 1998.

5. D. Foty, "MOSFET Modeling for Circuit Simulation: Where Do We Go From Here?," Fabless Forum, March 1998.

Conference Presentations

1. D. Foty, "Amplification, Feedback, and Sub-Biasing: Applying Analog Techniques to High-Speed, Low-Power Digital CMOS Circuits at Dimensions Below 100nm," (Invited Conference Plenary Lecture), presented at the 16th Baltic Electronics Conference, Tallinn, Estonia, 8 October 2018.

2. D. Foty, "Developing Critical Infrastructure – Data-Centric, Next-Generation Communications Networks," (Invited Conference Plenary Lecture), presented at the 2nd Regional African Conference of the International Telecommunications Society, Lusaka, Zambia, 16 March 2018.

3. D. Foty, "Amplification, Feedback, and Sub-Biasing: Applying Analog Techniques to High-Speed, Low Power Digital CMOS Circuits," (Invited Conference Plenary Lecture), presented at the 13th International Symposium on Signals, Circuits, and Systems, Iaşi, Romania, 13 July 2017.

4. D. Foty, "Developing Data-Centric, Next-Generation Communications Networks That Actually Work – and Work Well," (Invited Conference Plenary Lecture), presented at the EAI International Conference for Research, Innovation and Development for Africa, Victoria Falls, Zimbabwe, 21 June 2017.

5. D. Foty, "Amplification, Feedback, and Sub-Biasing: Applying Analog Techniques to High-Speed, Low Power Digital CMOS Circuits," (Invited Conference Plenary Lecture), presented at the 15th Baltic Electronics Conference, Tallinn, Estonia, 3 October 2016.

6. D. Foty, "The Future of 'Moore's Law' – Does It Have One?" (Invited Conference Plenary Lecture), presented at the 12th International Conference on Synthesis, Modeling, Analysis, and Simulation Methods and Applications to Circuit Design, Istanbul, Turkey, 7 September 2015.

7. D. Foty, "Patents, Trade Secrets, Intellectual Property, and Such: What Engineers Need to Know," (Invited Conference Plenary Lecture), presented at the 12th International Symposium on Signals, Circuits, and Systems, Iaşi, Romania, 10 July 2015.

8. D. Foty, "Patents, Trade Secrets, Intellectual Property, and Such: What Engineers Need to Know," (Invited Conference Plenary Lecture), presented at the 14th Baltic Electronics Conference, Laulasmaa, Estonia, 8 October 2014.

9. D. Foty, "The Future of 'Moore's Law' – Does It Have One?" (Invited Conference Plenary Lecture), presented at the 11th International Symposium on Signals, Circuits, and Systems, Iaşi, Romania, 11 July 2013.

10. D. Foty, "The Future of 'Moore's Law' – Does It Have One?" (Invited Conference Plenary Lecture), presented at the 13th Baltic Electronics Conference, Laulasmaa, Estonia, 5 October 2012.

11. D. Foty, B. Smith, S. Sinha, and M. Schröter, "Expanding Wireless Bandwidth in a Power-Efficient Way: Developing a Viable mm-Wave Radio Technology," (Invited Conference Plenary Lecture), presented at the 10th IEEE East-West Design and Test Symposium, Kharkov, Ukraine, 15 September 2012.

12. D. Foty, B. Smith, S. Sinha, and M. Schröter, "Addressing the Problem of Wireless Bandwidth and Power-Efficiency: Prospects for mm-Wave Radio Technology," presented at MASFOR2012, Istanbul, Turkey, 22 June 2012.

13. D. Foty, B. Smith, S. Sinha, and M. Schröter, "Addressing the Emerging Wireless Bandwidth Crisis and the Need for Power-Efficient Bandwidth: Prospects for mm-Wave Radio Technology," (Invited Conference Keynote Lecture), presented at Africon2011, Livingstone, Zambia, 13 September 2011.

14. D. Foty, B. Smith, S. Sinha, and M. Schröter, "The Wireless Bandwidth Crisis and the Need for Power-Efficient Bandwidth," (Invited Paper), presented at the 10th International Symposium on Signals, Circuits, and Systems, Iaşi, Romania, 1 July 2011.

15. D. Foty, "Thomas Johann Seebeck – Two Centuries Later, An Appreciation," (Invited Conference Plenary Lecture – the Thomas Johann Seebeck Memorial Lecture), presented at the 12th Baltic Electronics Conference, Tallinn, Estonia, 4 October 2010.

16. D. Foty, B. Smith, S. Sinha, and M. Schröter, "Next-Generation Wireless Communications Networks - From Chips to Architecture," (Invited Conference Plenary Lecture), presented at the International Association of Science and Technology for Development (IASTED) International Conference on Modeling and Simulation, Gaborone, Botswana, 7 September 2010.

17. D. Foty, "Breaking the Entropy Addiction: Understanding Power Consumption and Overcoming It," (Invited Conference Plenary Lecture), presented at Africon2009, Nairobi, Kenya, 25 September 2009.

18. D. Foty, S. Sinha, M. Weststrate, C. Coetzee, A. Uys, and E. Sibanda, "mm-Wave Radio Communications Systems: The Quest Continues" (Invited Conference Plenary Lecture), presented at the International Radio Electronics Forum, Kharkov, Ukraine, 23 October 2008.

19. D. Foty, "Prospects for Nanoscale Electron Devices: Some Little-Recognized Problems" (Invited Conference Plenary Lecture), presented at the 31st Conference on Semiconductor Physics, Sinaia, Romania, 13 October 2008.

20. D. Foty, "Nanoscale Electron Devices: The Untold Technology Story" (Invited Conference Plenary Lecture), presented at the 11th Baltic Electronics Conference, Laulasmaa, Estonia, 8 October 2008.

21. D. Foty, "Electron Devices in Nanoelectronic Circuits and Systems: Problems and Prospects," *Invited Presentation*, presented at the IEEE Electron Devices Society / Solid State Circuits Society Mini-Colloquium "Nanoelectronic Devices: Present and Perspective," Sinaia, Romania, 14 October 2007.

22. D. Foty, "Next-Generation Wireless Networks: A New World, From Bottom to Top," Invited Conference Keynote Lecture, presented at Africon2007, Windhoek, Namibia, 26 September 2007.

23. D. Foty, "The 'MOS Miracle' – A Behind-the-Scenes Look," Conference tutorial presented at the 8th International Symposium on Signals, Circuits, and Systems, Iaşi, Romania, 11 July 2007.

24. D. Foty, "Next-Generation Wireless Networks: New Building Blocks and New Network Topologies," Invited Conference Keynote Lecture, presented at the International Conference on Dependable Systems, Services, and Technologies, Kirovohrad, Ukraine, 27 April 2007.

25. D. Foty, "Factors in High-Speed Wireless Data Networking – New Ideas and a New Perspective" (Invited Conference Plenary Lecture), presented at the East-West Design and Test Workshop, Sochi, Russia, 18 September 2006.

26. D. Foty, "New Directions in Technology for High-Speed Wireless Data Communications" (Invited Conference Plenary Lecture), presented at the 13th International Conference on the Mixed Design of Integrated Circuits and Systems, Gdynia, Poland, 24 June 2006.

27. D. Foty and G. Gildenblat, "Fundamental Aspects of CMOS Technology: Basics, Implications, and a Roadmap to the Future" (Invited Paper), presented at the International Workshop on System-on-Chip, Banff, Alberta, Canada, 22 July 2005.

28. D. Foty and G. Gildenblat, "Scaling Theory and 'Punctuated Equilibrium' in CMOS Technology" (Invited Conference Plenary Lecture), presented at the 7th International Symposium on Signals, Circuits, and Systems, Iaşi, Romania, 14 July 2005.

29. D. Foty, "An Evaluation of Deep-Submicron CMOS Design Optimized for Operation at 77K" (Special Session Paper), presented at the 12th International Conference on the Mixed Design of Integrated Circuits and Systems, Krakow, Poland, 23 June 2005.

30. D. Foty, "An Evaluation of Deep-Submicron CMOS Design Optimized for Operation at 77K" (Special Session Paper), presented at the International Symposium on Industrial Electronics, Dubrovnik, Croatia, 20 June 2005.

31. D. Foty and K. Runge, "What's Ahead in High-Speed Wireless Data Communications? The Future Will Be Better Tomorrow – And Different Than What We've Been Expecting" (Invited Conference Plenary Lecture), presented at the 12th International Conference on Telecommunications, Cape Town, South Africa, 4 May 2005.

32. D. Foty and G. Gildenblat, "Fundamental Aspects of CMOS Technology: Basics, Implications, and a Roadmap to the Future" (Invited Conference Plenary Lecture), presented at the 8th International Conference CADSM, Polyana, Ukraine, 23 February 2005.

33. D. Foty, "Perspectives on Scaling Theory and CMOS Technology – Past, Present, and Future" (Invited Paper), presented at the 11th International Conference on Electronics, Circuits, and Systems, Tel Aviv, Israel, 15 December 2004.

34. G. Gildenblat, C. McAndrew, H. Wang, W. Wu, D. Foty, L. Lemaitre and P. Bendix, "Advanced Compact Models: Gateway to Modern CMOS Design" (Invited Paper), presented at the 11th International Conference on Electronics, Circuits, and Systems, Tel Aviv, Israel, 15 December 2004.

35. P. Bendix, D. Foty, and D. Pachura, "Practical Aspects of MOS Transistor Model 'Accuracy' in Modern CMOS Technology" (Invited Paper), presented at the 11th International Conference on Electronics, Circuits, and Systems, Tel Aviv, Israel, 15 December 2004.

36. D. Foty and G. Gildenblat, "CMOS Scaling Theory – Why Our 'Theory of Everything' Still Works, and What That Means For The Future" (Invited Paper), presented at the 12th International Symposium on Electron Devices for Microwave and Optoelectronic Applications, Berg-en-Dal, Kruger National Park, South Africa, 8 November 2004.

37. D. Foty, "Perspectives on Scaling Theory and CMOS Technology – Punctuated Equilibrium and Evolutionary Biology" (Invited Conference Plenary Lecture), presented at the 9th Baltic Electronics Conference, Tallinn, Estonia, 4 October 2004.

38. D. Foty, "Re-Interpreting the MOS Transistor for the 21st Century: Generalized Methods and Their Extension to Nanotechnology," (Invited Conference Plenary Lecture), presented at the Nordic VLSI Design Conference (NorChip), Riga, Latvia, 10 November 2003.

39. D. Foty, "Pondering the MOS Transistor in the 21st Century" (Conference Tutorial), presented at the Nordic VLSI Design Conference (NorChip), Riga, Latvia, 9 November 2003.

40. D. Foty, "Re-Generalizing the MOS Transistor, for Improved Analog Design and Extension to Nanotechnology: New Rules for a New Century" (Invited Conference Plenary Lecture), presented at the 4th Electronic Circuits and Systems Conference, Bratislava, Slovakia, 12 September 2003.

41. D. Foty, "Re-Thinking and Re-Generalizing the MOS Transistor: Understanding, CMOS Design, and Extension to Nanotechnology" (Invited Conference Plenary Lecture), presented at the 16th European Conference on Circuit Theory and Design, Krakow, Poland, 2 September 2003.

42. D. Foty, "Modernizing the Framework for Deep Submicron Design – For CMOS and Beyond" (Invited Conference Plenary Lecture), presented at the 10th International Conference on the Mixed Design of Integrated Circuits and Systems, Lodz, Poland, 27 June 2003.

43. D. Foty, M. Bucher, and D. Binkley, "Re-Interpreting the MOS Transistor Via the Inversion Coefficient and the Continuum of gms/Id," presented at the 9th International Conference on Electronics, Circuits, and Systems, Dubrovnik, Croatia, 18 September 2002.

44. D. Foty, and M. Bucher, "New Techniques for Modern Analog Design: CMOS Design Methodologies and the EKV MOSFET Model" (Conference Tutorial), presented at the 9th International Conference on Electronics, Circuits, and Systems, Dubrovnik, Croatia, 15 September 2002.

45. D. Foty, D. Binkley, and M. Bucher, "gm/Id-Based MOSFET Modeling and Modern Analog Design" (Invited Paper), presented at the 9th International Conference on the Mixed Design of Integrated Circuits and Systems, Wrocław, Poland, 20 June 2002.

46. D. Foty and D. Binkley, "MOS Modeling as a Basis for Design Methodologies: New Techniques for Modern Analog Design" (Conference Tutorial), presented at the International Symposium on Circuits and Systems, Scottsdale, Arizona, 26 May 2002.

47. D. Foty, "MOS Modeling, Design Quality, and Modern Analog Design" (Conference Tutorial), presented at the Workshop on Compact Modeling, International Conference on the Modeling and Simulation of Microsystems, San Juan, Puerto Rico, 25 April 2002.

48. D. Foty, D. Binkley, and M. Bucher, "Starting Over: gm/Id-Based MOSFET Modeling as a Basis for Modernized Analog Design Methodologies" (Invited Paper),

presented at the Workshop on Compact Modeling, International Conference on the Modeling and Simulation of Microsystems, San Juan, Puerto Rico, 23 April 2002.

49. D. Foty, "MOS Modeling, Design Quality, and Modern Analog Design" (Conference Tutorial), presented at the International Symposium on Quality Electronic Design, San Jose, California, 18 March 2002.

50. D. Foty, D. Binkley, and M. Bucher, "Measurements and Modeling of MOSFET Inversion Level Over a Wide Range as a Basis for Analog Design," presented at the 15th European Conference on Circuit Theory and Design, Espoo, Finland, 29 August 2001.

51. D. Foty, "MOSFET Modeling for Circuit Simulation: Requiem or Recovery?," presented at the 15th European Conference on Circuit Theory and Design, Espoo, Finland, 29 August 2001.

52. D. Foty and D. Binkley, "MOS Modeling as a Basis for Design Methodologies: New Techniques for Next-Generation Analog Circuit Design" (Conference Tutorial), presented at the 15th European Conference on Circuit Theory and Design, Espoo, Finland, 28 August 2001.

53. D. Foty and D. Binkley, "Re-Connecting MOS Modeling and Circuit Design: New Methods for Design Quality" (Conference Tutorial), presented at the International Symposium on Quality Electronic Design, San Jose, California, 26 March 2001.

54. D. Foty and D. Binkley, "MOS Modeling and Circuit Design: Re-Establishing a Lost Connection" (Conference Tutorial), presented at the Design Automation Conference, Los Angeles, California, 7 June 2000.

55. D. Foty, "A Circuit Designer's Guide to MOS Modeling" (Conference Tutorial), presented at the International Symposium on Circuits and Systems, Geneva, Switzerland, 28 May 2000.

56. D. Foty, "MOS Models as a Factor in the Quality of Electronic Design" (Conference Tutorial), presented at the International Symposium on Quality Electronic Design, San Jose, California, 20 March 2000.

57. D. Foty, "MOS Modeling – A Crucial Circuit Design Activity," presented at Silicon RF-IC: Modeling and Design," Lausanne, Switzerland, 25 February 2000.

58. D. Foty, "An Overview of AC Simulation Aspects of MOS Modeling," presented at the RF MOS Modeling Workshop, Munich, Germany, 16 February 1999.

59. D. Foty, "AC Simulation Aspects of MOS Modeling," presented at Northcon, Seattle, Washington, 22 October 1998.

60. D. Foty, "Effective MOSFET Modeling for SPICE Circuit Simulation" (Conference Tutorial), presented at Northcon, Seattle, Washington, 22 October 1998.

61. D. Foty, "What Every Circuit Designer Needs to Know About MOS Modeling for SPICE Circuit Simulation" (One-Day Short Course), presented at the Electronic Design Automation and Test Conference, Asia, Hsinchu, Taiwan, 15 October 1998.

62. D. Foty, "MOS Modeling of Small Geometry Structures for Circuit Simulation" (Conference Tutorial), presented at the Custom Integrated Circuits Conference, Santa Clara, California, 11 May 1998.

63. D. Foty, "MOS Modeling for Deep Submicron CMOS Circuit Simulation" (Conference Tutorial), presented at the Southeastern Workshop on Mixed-Signal VLSI, Knoxville, Tennessee, 1 April 1998.

64. D. Foty, "MOS Modeling Issues in the Emerging Analog and Low Power Era" (Conference Tutorial), presented at the Electronic Design Automation and Test Conference, Asia, Hsinchu, Taiwan, 28 August 1997.

65. D. Foty, "MOS Modeling Issues in the Emerging Analog and Low Power Era" (Conference Tutorial), presented at the Electronic Design Automation and Test Conference, Asia, Shanghai, China, 22 August 1997.

66. D. Foty, "Aspects of MOS Modeling for Analog/Mixed-Signal Design," presented at the CMP Analog/Mixed-Signal Design Conference, San Jose, California, 22 July 1997.

67. D. Foty, "MOS Modeling and SPICE: Are You an Educated Model Consumer?" (Conference Tutorial), presented at the Custom Integrated Circuits Conference, Santa Clara, California, 5 May 1997.

68. D. Foty, "The SPICE FET Models: Pitfalls and Prospects" (Conference Tutorial), presented at the Design Automation Conference, Las Vegas, Nevada, 5 June 1996.

69. D. Foty and E. Nowak, "Performance, Reliability, and Supply Voltage Reduction, with the Addition of Temperature as a Design Variable" (Invited Paper), presented at the Symposium on Low Voltage-Low Power Integrated Circuits, 1993 European Solid State Device Research Conference, Grenoble, France, 16 September 1993.

70. D. Foty and E. Nowak, "Performance/Reliability Trade-Off and Optimized nMOSFET Design for 77K CMOS Logic," presented at the Symposium on Low Temperature Electronics and High Temperature Superconductors, Honolulu, Hawaii, 20 May 1993.

71. D. Foty, "The Design of Deep Submicron FETs for Low Temperature Operation" (Invited Paper), presented at the Symposium on Low Temperature Electronics and High Temperature Superconductors, Honolulu, Hawaii, 20 May 1993.

72. D. Foty, H. Hanafi, P. Agnello, and H. Ho, "Mixed Schottky/p-n Junction Behavior in Diodes Produced by Outdiffusion from Polycrystalline Cobalt Disilicide," presented at the 1992 International Electron Devices Meeting, San Francisco, California, 16 December 1992.

73. D. Foty, "Low Temperature Electronics and Future Electron Devices (Invited Paper), presented at the Symposium on Low Temperature Electronic Device Operation, Washington, DC, 7 May 1991.

74. D. Foty, "Impurity Ionization in MOSFETs at Very Low Temperatures," presented at the First International Conference on Low Temperature Electronics, Berkeley, California, 24 April 1990.

75. D. Foty and T. Furukawa, "Behavior of an NMOS Trench Isolated Corner Parasitic Device at Low Temperature," presented at the Symposium on Low Temperature Electronics, Materials, and Processing, Hollywood, Florida, 17 October 1989.

76. D. Foty and S. Titcomb, "Freeze-Out and Field Dependent Ionization in MOSFETs at Very Low Temperatures," presented at the Symposium on Low Temperature Electronics and High Temperature Superconductors, Honolulu, Hawaii, 20 October 1987.

Co-Authored Conference Presentations

1. S. Sinha and D. Foty, "SiGe Technology for mm-Wave Applications," (Invited Conference Plenary Lecture), presented at the 13th Baltic Electronics Conference, Tallinn, Estonia, 3 October 2012.

2. B.C. Mabuza, S. Sinha and D. Foty, "On-chip Impedance Tuning for mm-Wave Applications," presented at the South African Conference on Semiconductor and Superconductor Technology, Stellenbosch, South Africa 8 April 2009.

3. S. Terry, J. Rochelle, D. Binkley, B. Blaylock, D. Foty, and M. Bucher, "Comparison of a BSIM3V3 and EKV MOST Model for a 0.5µm Process and Implications for Analog Circuit Design," presented at the IEEE Nuclear Science Symposium, Norfolk, Virginia, 15 November 2002.

4. M. Bucher, D. Kazazis, F. Krummenacher, D. Binkley, D. Foty, and Y. Papananos, "Analysis of Transconductances at All Levels of Inversion in Deep Submicron CMOS," presented at the 9th International Conference on Electronics, Circuits, and Systems, Dubrovnik, Croatia, 18 September 2002.

5. D. Binkley, M. Bucher, and D. Foty, "Design-Oriented Characterization of CMOS Over the Continuum of Inversion Level and Channel Length," presented at the 7th

International Conference on Electronics, Circuits, and Systems, Kaslik, Lebanon, 18 December 2000.

6. G. Gildenblat, M. Bradford, and D. Foty, "A New MOS C-V Simulator for Low Temperature Applications," presented at the Symposium on Low Temperature Electronics and High Temperature Superconductors, Honolulu, Hawaii, 20 May 1993.

Conference Panel Participation

1. Member of Panel Discussion, 2nd Regional African Conference of the International Telecommunications Society, Lusaka, Zambia, 15 March 2018.

2. Member of Panel Discussion, 12th International Conference on Synthesis, Modeling, Analysis, and Simulation Methods and Applications to Circuit Design, Istanbul, Turkey, 7 September 2015.

3. Member of Panel Discussion, Future Wireless Telecommunications, "Telecosm," Lake George, New York, 16 October 2007.

4. Moderator of Panel Discussion, International Workshop on System-on-Chip, Banff, Alberta, Canada, 22 July 2005.

5. Member of Panel Discussion, Custom Integrated Circuits Conference, San Jose, California, 23 September 2003.

6. Co-moderator of Panel Discussion, Fabless Semiconductor Association Modeling Workshop, Santa Clara, California, 9 September 2002.

7. Member of Panel Discussion, Workshop on Compact Modeling, International Conference on the Modeling and Simulation of Microsystems, San Juan, Puerto Rico, 23 April 2002.

8. Member of Panel Discussion, "Vermont's High-Tech Future – Does it Have One?," Room 11, the Statehouse, Montpelier, Vermont, 26 April 2001.

9. Member of Panel Discussion, Fabless Semiconductor Association Quarterly Meeting, San Jose, California, 5 September 1999.

10. Member of Panel Discussion, Fabless Semiconductor Association Modeling Workshop, San Jose California, 24 May 1999.

11. Member of Panel Discussion, Symposium on Low Voltage-Low Power Integrated Circuits at the 1993 European Solid State Device Research Conference, Grenoble, France, 16 September 1993.

12. Member of Panel Discussion, Symposium on Low Temperature Electronics and High Temperature Superconductors, Honolulu, Hawaii, 19 May 1993.

Invited Seminars/Lectures

1. "Digital Semiconductor Electronics: Why It Happened, And Where It's Going," short course hosted by the University of Pretoria, Pretoria, South Africa, 15 August 2011.

2. "The Untold Story of 'Moore's Law': *Why* It Happened," short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Iaşi, Romania, 4 – 5 July 2011.

3. "Some Background Thoughts On mm-Wave Radio Technology," seminar presented at the University of Pretoria, Pretoria, South Africa, 17 August 2010.

4. "Digital Semiconductor-Based Electronics: Why It Became A Juggernaut," short course hosted by the University of Pretoria, Pretoria, South Africa, 16 August 2010.

5. "Some Thoughts On mm-Wave Radio Technology," short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Oradea, Romania, 13 July 2010.

6. "Silicon-Based Semiconductor Electronics – How It Came To Dominate," short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Oradea, Romania, 12 July 2010.

7. "The Powerful Entropy Challenge: Dealing With Power Consumption," presented at the IEEE South Africa Section Meeting, Pretoria, South Africa, 18 August 2009.

8. "Digital CMOS Electronics: The Background Story," short course hosted by the University of Pretoria, Pretoria, South Africa, 17 August 2009.

9. "An Overview of mm-Wave Radio Technology," short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Iaşi, Romania, 13 July 2009.

10. "Modern Electronics: How We Got Here," short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Iaşi, Romania, 13 July 2009.

11. "Prospects for mm-Wave Radio Technology: An Overview," short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Oradea, Romania, 22 July 2008.

12. "Into the NanoSmall: The Unexpected Challenges," short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Oradea, Romania, 22 July 2008.

13. “A Concise History of Modern Electron Devices,” short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Oradea, Romania, 22 July 2008.

14. "Issues In mm-Wave Radio Systems: Prospects and Challenges," short course hosted by the University of Pretoria, Pretoria, South Africa, 8 May 2008.

15. "Prospects for mm-Wave Radio Technology: An Executive Summary for Decision-Makers," presented at the IEEE Region 8 meeting, University of Pretoria, Pretoria, South Africa, 8 May 2008.

16. “The MOS Transistor, On a Tourist Visa,” short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Iaşi, Romania, 16 July 2007.

17. “Semiconductor Electronics: Some Fundamental Background,” short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Iaşi, Romania, 16 July 2007.

18. “The MOS Transistor and CMOS Technology: Past, Present, and Future,” short course hosted by Tallinn University of Technology, Tallinn, Estonia, 13 – 14 November 2006.

19. “New Directions in Technology for High-Speed Wireless Data Communications,” seminar presented at the Universitatea Politehnica Bucureşti, Bucharest, Romania, 28 July 2006.

20. “The MOS Transistor and CMOS Technology: History as a Guide to the Future,” short course hosted at the summer school of the Universitatea Politehnica Bucureşti, held in Braşov, Romania, 25 July 2006.

21. “The Underpinnings of the MOS Transistor and CMOS Technology in the 21st Century - Scaling Theory and New Methods in Analog/RF Design,” short course hosted by l'École Polytechnique de Montréal, Montréal, Québec, Canada; sponsored by ReSMiQ and the local IEEE Solid State Circuits Society chapter, 27 October 2005.

22. “The Underpinnings of the MOS Transistor and CMOS Technology in the 21st Century – Scaling Theory and New Methods in Analog/RF Design,” short course hosted by the Department of Electrical, Electronic, and Computer Engineering, University of Pretoria, Pretoria, South Africa, and sponsored by the IEEE South Africa Section, 9 – 10 May 2005.

23. “What’s Ahead in High-Speed Wireless Data Communications? The Future Will Be Better Tomorrow – And Different Than What We’ve Been Expecting,” seminar presented at the Department of Electrical Engineering, University of Cape Town, Cape Town, South Africa, 7 May 2005.

24. "Low Temperature CMOS: A Bad Idea Whose Time Has (Finally) Come?", seminar presented at the Department of Computer-Aided Design, L'viv Polytechnic National University, L'viv, Ukraine, 28 February 2005.

25. "The Underpinnings of the MOS Transistor and CMOS Technology in the 21st Century – Scaling Theory and New Methods in Analog/RF Design," Full-day "Eurotraining" course, held at the Danish Technical University, Lyngby, Denmark, 27 October 2004.

26. "The Underpinnings of the MOS Transistor and CMOS Technology in the 21st Century – Scaling Theory and New Methods in Analog/RF Design," Full-day "Eurotraining" course, held at the Politechnico di Torino, Turin, Italy, 25 October 2004.

27. "CMOS Scaling and Low Temperature CMOS: A Bad Idea Whose Time Has Come?", seminar presented at the Department of Electrical and Computer Engineering, Oakland University, Auburn Hills, Michigan, 25 March 2004.

28. "Modernizing the Interpretation of the MOS Transistor for the 21st Century: Generalized Methods and Their Extension to Nanotechnology," presented at the IEEE Southeast Michigan Spring Section Meeting, Auburn Hills, Michigan, 24 March 2004.

29. "Re-Interpreting the MOS Transistor for the 21st Century: Generalized Methods and Their Extension to Nanotechnology," seminar presented at Tallinn Technical University, Tallinn, Estonia, 13 November 2003.

30. "Re-Interpreting the MOS Transistor for the 21st Century: Generalized Methods and Their Extension to Nanotechnology," seminar presented at Helsinki University of Technology, Espoo, Finland, 7 November 2003.

31. "A Practical Examination of MOS Transistor Model 'Accuracy' in Modern CMOS Technology," presented at the MOS Arbeitskreis Meeting, Crolles, France, 5 May 2003.

32. "Building a New Framework for Deep Submicron Analog/RF CMOS Design – and Beyond," invited seminar presented at the Department of Electrical Engineering, Columbia University, New York, New York, 25 April 2003.

33. "A New Framework for Deep Submicron Analog/RF CMOS Design – and Beyond," seminar presented at the Department of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, Georgia, 20 March 2003.

34. "Starting Over: Modernizing the Framework for Deep Submicron Analog CMOS Design," seminar presented at the Nokia Research Center, Helsinki, Finland, 29 November 2002.

35. "Modernizing the Framework for Deep Submicron Analog CMOS Design," Distinguished Guest Lecturer, IEEE Baltic Region Meeting (sponsored by Tallinn Technical University), Sagadi, Estonia, 19 – 20 August 2002.

36. "Modernizing the Framework for Deep Submicron Analog CMOS Design," seminar presented at Helsinki University of Technology, Espoo, Finland, 16 August 2002.

37. "gm/Id-Based MOSFET Modeling and Modern Analog Design," presented at the MOS Arbeitskreis Meeting, Ünterpremstatten, Austria, 19 November 2001.

38. "MOS Modeling and Analog Circuit Design," lecture as part of "Practical Aspects of Analog Design," professional short course sponsored by Mead Microelectronics, San Francisco, California, 13 November 2001.

39. "MOS Modeling and Analog Circuit Design," lecture as part of "Transistor-Level Analog IC Design," professional short course sponsored by Mead Microelectronics, Lausanne, Switzerland, 10 October 2001.

40. "Please Stop Imitating Us!' – An Engineer Looks at the (Unstable) State of the Humanities," presented at a meeting of the National Association of Scholars, Burlington,Vermont, 14 July 2001.

41. "Introduction to the Fabless Semiconductor Association (FSA) and the Modeling Committee Activities," presented at the MOS Arbeitskreis Meeting, Munich, Germany, 5 March 2001.

42. "The EKV MOSFET Model: A MOS Model of, by, and for Analog Designers," presented at Broadcom Corp., Irvine, California, 30 November 2000.

43. "Modeling and Simulation for Mixed-Signal IC Design," lecture as part of "Transistor-Level Analog IC Design," professional short course sponsored by Mead Microelectronics, Lausanne, Switzerland, 27 September 2000.

44. "MOS Models as a Factor in the Quality of Electronic Design," presented at the Rockwell Scientific Center, Thousand Oaks, California, 17 March 2000.

45. "MOS Models as a Factor in the Quality of Electronic Design," presented at Micron Technology, Inc., Boise Idaho, 4 March 2000.

46. "Modeling and Simulation for Mixed-Signal IC Design," lecture as part of "Practical Aspects of Analog and Mixed-Signal ICs," professional short course sponsored by Mead Microelectronics, Monterey, California, 3 February 2000.

47. "Modeling and Simulation for Mixed-Signal IC Design," lecture as part of "Transistor-Level Analog IC Design," professional short course sponsored by Mead Microelectronics, Lausanne, Switzerland, 30 September 1999.

48. "AC Simulation Aspects of MOS Modeling," presented at the Fabless Semiconductor Association Modeling Workshop, San Jose, California, 25 May 1999.

49. D. Foty, M. Bucher, and C. Enz, "The EKV MOSFET Model – A MOS Model for the Analog Designer," presented at the Fabless Semiconductor Association Modeling Workshop, San Jose, California, 25 May 1999.

50. Several lectures on MOS device physics, modeling, and analog design, presented at Mentor Graphics, Heliopolis, Cairo, Egypt, 5 – 8 May 1999.

51. "A Brief History of MOS Modeling (or, How We Got In This Mess In the First Place)," presented at Philips Research Laboratories, Eindhoven, The Netherlands, 24 March 1999.

52. "An Overview of MOS Modeling for SPICE Circuit Simulation," presented at Mitel Corporation, Bromont, Québec, Canada, 2 February 1999.

53. "Modeling and Simulation for Mixed-Signal IC Design," lecture as part of "Practical Aspects of Analog and Mixed-Signal ICs," professional short course sponsored by Mead Microelectronics, Monterey, California, 12 December 1998.

54. "MOS Modeling Challenges for Deep Submicron CMOS," lecture presented as part of "Deep Submicron CMOS Design," professional short course sponsored by Mead Microelectronics, Lausanne, Switzerland, 12 October 1998.

55. "Modeling the Temperature-Dependent Characteristics of MOSFETs for Circuit Simulation," presented at the Electronic Parts Selection and Management Workshop, Center for the Analysis of Life-Cycle Engineering, University of Maryland, College Park, Maryland, 17 June 1998.

56. "A Primer on Trench Isolation Technology (or, Why Do Process Engineers Hate Circuit Designers?)," presented at the Fabless Semiconductor Association Modeling Subcommittee Meeting, Opti, Inc., Milpitas, California, 12 May 1998.

57. C. Enz, M. Bucher, and D. Foty, "The EKV MOSFET Model for Analog and Mixed-Mode Circuit Design," satellite broadcast class, National Technological University (hosted by North Carolina State University, Raleigh, North Carolina), 30 April 1998.

58. "MOS Modeling Challenges for Deep Submicron CMOS Circuit Simulation," presented at Digital Equipment Corporation, Hudson, Massachusetts, 13 April 1998.

59. "Challenges for 0.25μm CMOS Circuit Design: Scaling, MOS Modeling, and Complexity," presented at CERN, Geneva, Switzerland, 6 February 1998.

60. "MOS Modeling Challenges for Deep Submicron CMOS," lecture presented as part of "Deep Submicron CMOS Design," professional short course sponsored by Mead Microelectronics, Monterey, California, 11 December 1997.

61. C. Enz, M. Bucher, and D. Foty, "The EKV MOSFET Model for Analog and Mixed-Mode Circuit Design," one-day short course sponsored by the Fabless Semiconductor Association, San Jose, California, 8 November 1997.

62. "MOS Modeling Issues in the Emerging Analog and Low Power Era," presented Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, 27 August 1997.

63. "Current Problems in MOSFET Modeling for Analog Circuit Simulation," presented at Level One Communications, Inc., Sacramento, California, 9 August 1997.

64. Guest lecturer, Centre National pour les Récherches Scientifique (CNRS) Summer Lecture Series, La Londe des Maures, France, 23 – 28 June 1997.

65. "MOSFET Modeling and Analog Circuit Design," presented at the Centre National pour les Récherches Scientifique (CNRS) Summer Lecture Series, La Londe des Maures, France, 27 June 1997.

66. "Benchmarking and Pre-Screening SPICE FET Models for Circuit Simulation Usage," presented at the Fabless Semiconductor Association Modeling Subcommittee Meeting, Adaptec, Inc., Milpitas, California, 6 May 1997.

67. "Benchmarking and Pre-Screening SPICE FET Models for Circuit Simulation Usage," presented at Cirrus Logic, Inc., Fremont, California, 6 May 1997.

68. "MOSFET Modeling and SPICE: Are You an Educated Model Consumer?," presented at Cirrus Logic, Inc., Fremont, California, 6 May 1997.

69. "MOS Modeling and SPICE: Are You an Educated Model Consumer?," satellite broadcast class, National Technological University (hosted by North Carolina State University, Raleigh, North Carolina), 21 April 1997.

70. "An Overview of the SPICE FET Modeling Infrastructure" lecture presented as part of "Modeling and Simulation of MOS Analog ICs," professional short course sponsored by Mead Microelectronics, Lausanne, Switzerland, 18 February 1997.

71. "An Overview of the SPICE FET Modeling Infrastructure" lecture presented as part of "Modeling and Simulation of MOS Analog ICs," professional short course sponsored by Mead Microelectronics, Monterey, California, 12 December 1996.

72. "Analytical MOSFET Modeling and SPICE - Past, Present, and Future", seminar presented at the Department of Electrical Engineering, Ohio State University, Columbus, Ohio, 9 May 1995.

73. "Constraints on CMOS Technology for Low Voltage/Low Power Applications", seminar presented at the Department of Electrical Engineering, Ohio State University, Columbus, Ohio, 8 May 1995.

74. "Submicron FET Design: Physical Considerations and Technological Choices", seminar presented at the Electrical Engineering Department, University of Hawaii, Honolulu, Hawaii, 24 May 1993.

75. "Aspects of the Design of Deep Submicron FETs for CMOS Operation at 300K and 77K", seminar presented at the Department of Electrical Engineering, Pennsylvania State University, University Park, Pennsylvania, 10 November 1992.

PROFESSIONAL AFFILIATIONS & AWARDS

Honorary Member of the Applied Radio Electronics Science Academy of Ukraine

Senior Member, The Institute of Electrical and Electronic Engineers (IEEE); and of the Electron Devices, Lasers and Electro-Optics, Circuits and Systems, and Communications Societies of the IEEE.

Reviewer/evaluator of funding proposals, Natural Science and Engineering Research Council of Canada, 1991 - present.

Reviewer/evaluator of funding proposals, California MICRO program, 2001 - present.

Reviewer/evaluator of funding proposals, National Research Foundation of South Africa, 2007- present.

Industrial and Academic Mentoring

Member of the Advisory Board, Department of Electrical, Electronic & Computer Engineering, University of Pretoria, South Africa, 2012 – present.

Advisor to the Tshwane University of Technology, Pretoria, South Africa, 2007 - present.

Advisor to the University of Pretoria, Pretoria, South Africa, 2005 – present.

Advisor to the Tallinn University of Technology, Tallinn, Estonia, 2004 – present.

Industrial Mentor for "Development and Applications of a New MOS C-V Simulator for the 2 - 300K Temperature Range" (Professor Gennady Gildenblat, Principal Investigator, Department of Electrical Engineering, Pennsylvania State University, University Park, Pennsylvania), funded by the IBM Shared University Research Contract program, calendar year 1992.

Committees/Conferences

1. Member of the Organizing Committee, and Chair of the Track on Electromagnetics and Antennas, Africon 2011, Victoria Falls, Zambia, September 2011.

2. Member of the Organizing Committee, and Chair of the Track on Electron Devices and Circuits, Africon 2009, Nairobi, Kenya, September 2009.

3. Session Chair, 31st International Conference on Semiconductor Physics, Sinaia, Romania, 14 October 2008.

4. Session Chair, Africon 2007, Windhoek, Namibia, 27 September 2007.

5. Session Chair, 13th International Conference on the Mixed Design of Integrated Circuits and Systems, Gdynia, Poland, 24 June 2006.

6. Session Chair, International Workshop on System-on-Chip, Banff, Alberta, Canada, 22 July 2005.

7. Session Chair, 7th International Symposium on Signals, Circuits, and Systems, 4Iaşi, Romania, 15 July 2005.

8. Member of the Scientific Committee, European Conference on Circuit Theory and Design (ECCTD), 2005.

9. Special Session Organizer, 12th International Conference on the Mixed Design of Integrated Circuits and Systems, Krakow, Poland, 22 - 25 June 2005.

10. Special Session Organizer, International Symposium on Industrial Electronics, Dubrovnik, Croatia, 20 – 23 June 2005.

11. Session Chair, 12th International Conference on Telecommunications, Cape Town, South Africa, 4 – 6 May 2005.

12. Session Chair, 11th International Conference on Electronics, Circuits, and Systems, Tel Aviv, Israel, 13 - 15 December 2004.

13. Session Chair, the 12th International Symposium on Electron Devices for Microwave and Optoelectronic Applications, Berg-en-Dal, Kruger National Park, South Africa, 8 - 9 November 2004.

14. Member of the International Program Committee, International Conference on Mixed Design of Integrated Circuits and Systems, 2004 – present.

15. Member of the Technical Program Committee, International Symposium on Signals, Circuits, and Systems, 2004 – present.

16. Special Session Organizer, 11th International Conference on Electronics, Circuits, and Systems, Tel Aviv, Israel, 13 – 15 December 2004.

17. Session Chair, 4th Electronic Circuits and Systems Conference, Bratislava, Slovakia, 11 – 12 September 2003.

18. Member of the Scientific Committee, European Conference on Circuit Theory and Design (ECCTD), 2003.

19. Session Chair, 9th International Conference on Electronics, Circuits, and Systems, Dubrovnik, Croatia, 16 - 18 September 2002.

20. Member, Analog Signal Processing Technical Committee, IEEE Circuits and Systems Society, 2002 – present.

21. Member, Program Committee, Analog Circuits and Signal Processing, International Symposium on Circuits and Systems (ISCAS), 2002 – present.

22. Session Chair, International Symposium on Quality Electronic Design, San Jose, California (ISQED), 18 – 20 March 2002.

23. Chairman, Modeling Subcommittee, Fabless Semiconductor Association, 2001 – 2003.

24. Chairman, Fabless Semiconductor Association Modeling Workshop, 2001 – present.

25. Member of Technical Program Committee, European Conference on Circuit Theory and Design (ECCTD), 2001.

26. Member, IEEE Advisory Committee, 2001 – present.

27. Member of the Organizing Committee, International Symposium on Quality Electronic Design (ISQED), 2000 – 2002.

28. Member of the Modeling Committee, International Symposium on Quality Electronic Design (ISQED), 2000 – 2002.

29. Chairman of the Modeling Committee, International Symposium on Quality Electronic Design (ISQED), 2001.

30. Session Chair, International Symposium on Quality Electronic Design, San Jose, California (ISQED), 26 – 28 March 2001.

31. Lead Organizer, Fabless Semiconductor Association Workshop, 2000 – present.

32. Member of the MOS Arbeitskreis, 2000 – present.

33. Co-Chairman, Modeling Subcommittee, Fabless Semiconductor Association, 1999 – 2000.

34. Member of the Executive Committee, Modeling Subcommittee, Fabless Semiconductor Association, 1998 – present.

35. Member, Modeling Subcommittee, Fabless Semiconductor Association, 1996 – present.

36. Organizer, Symposium on Low Temperature Electronics and High Temperature Superconductors, Honolulu, Hawaii, 16 - 21 May 1993.

37. Organizer, Symposium on the Physics and Fabrication of Semiconductor Nanostructures, Washington DC, 5 - 10 May 1991.

38. Lead Organizer, Symposium on Low Temperature Electronic Device Operation, Washington DC, 5 - 10 May 1991.

39. Co-Chaired the Symposium on Low Temperature Electronics, Materials, and Processing, Hollywood, Florida, 17 October 1989.