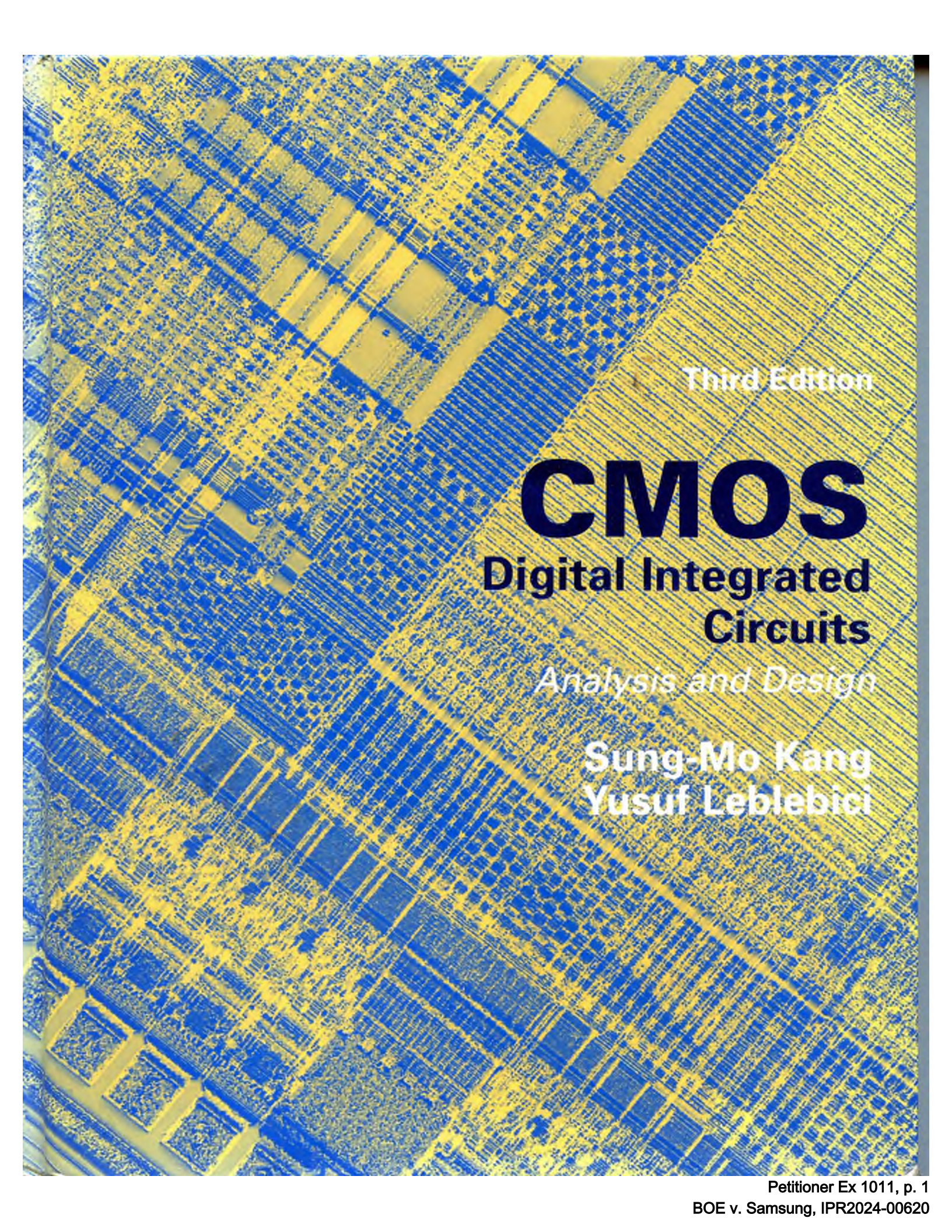


The background of the book cover is a high-magnification micrograph of a silicon chip, showing a complex grid of square and rectangular patterns in shades of blue and yellow. The patterns represent various functional blocks and interconnects of the integrated circuit.

Third Edition

CMOS

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Analysis and Design

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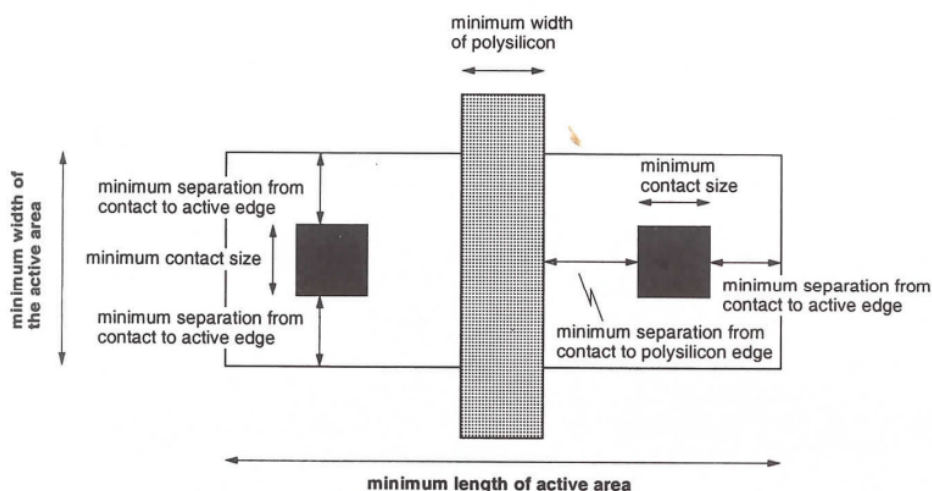


Figure 2.15 Design rules which determine the dimensions of a minimum-size transistor.

area is then determined by the minimum diffusion contact size (which is necessary for source and drain connections) and the minimum separation from diffusion contact to both active area edges. The width of the polysilicon line over the active area (which is the gate of the transistor) is typically taken as the minimum poly width (Fig. 2.15). Then, the minimum overall length of the active area is determined by the following sum: (minimum polysilicon width) + $2 \times$ (minimum poly-to-contact spacing) + $2 \times$ (minimum contact size) + $2 \times$ (minimum spacing from contact to active area edge).

The pMOS transistor must be placed in an n-well region, and the minimum size of the n-well is dictated by the pMOS active area and the minimum n-well overlap over n+. The distance between the nMOS and the pMOS transistor is determined by the minimum separation between the n+ active area and the n-well (Fig. 2.16). The polysilicon gates of the nMOS and the pMOS transistors are usually aligned, so that the gate connections can be made with a single polysilicon line of least possible length. The reason for avoiding long polysilicon connections (as a general layout practice) is the fact that the large parasitic resistance and the parasitic capacitance of polysilicon lines may result in significant RC delays. Thus, even *local* signal connections are preferably made with metal lines as much as possible, and metal-polysilicon contacts are used to provide the electrical connection between the two layers, wherever necessary.

The final step in the mask layout is the local interconnections in metal for the output node, VDD and GND contacts (Fig. 2.17). The dimensions of metal lines in a mask layout are usually dictated by the minimum metal width and the minimum metal separation (between two neighboring lines, on the same level). Notice that in order to be biased properly, the n-well region must also have a VDD contact.

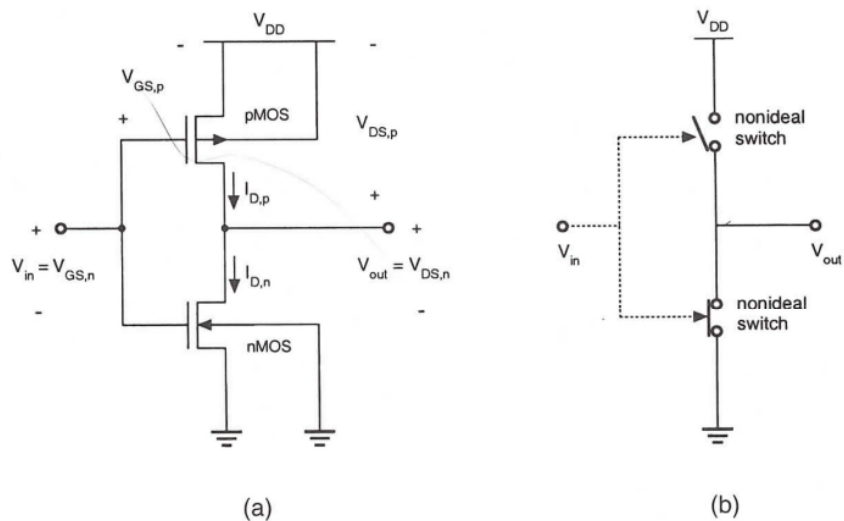


Figure 5.16 (a) CMOS inverter circuit. (b) Simplified view of the CMOS inverter, consisting of two complementary nonideal switches.

nMOS transistor acting as a nonlinear resistor. In this general configuration, the input signal is always applied to the gate of the driver transistor, and the operation of the inverter is controlled primarily by switching the driver. Now, we will turn our attention to a radically different inverter structure, which consists of an enhancement-type nMOS transistor and an enhancement-type pMOS transistor, operating in complementary mode (Fig. 5.16). This configuration is called Complementary MOS (CMOS). The circuit topology is complementary push-pull in the sense that for high input, the nMOS transistor drives (pulls down) the output node while the pMOS transistor acts as the load, and for low input the pMOS transistor drives (pulls up) the output node while the nMOS transistor acts as the load. Consequently, both devices contribute equally to the circuit operation characteristics.

The CMOS inverter has two important advantages over the other inverter configurations. The first and perhaps the most important advantage is that the steady-state power dissipation of the CMOS inverter circuit is virtually negligible, except for small power dissipation due to leakage currents. However, as mentioned earlier, the trend of increasing subthreshold leakage currents in deep sub-micron technologies causes great design challenges. In all other inverter structures examined so far, a nonzero steady-state current is drawn from the power source when the driver transistor is turned on, which results in a significant DC power consumption. The other advantages of the CMOS configuration are that the voltage transfer characteristic (VTC) exhibits a full output voltage swing between 0 V and V_{DD} , and that the VTC transition is usually very sharp. Thus, the VTC of the CMOS inverter resembles that of an ideal inverter.

Since nMOS and pMOS transistors must be fabricated on the same chip side-by-side, the CMOS process is more complex than the standard nMOS-only process. In