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Applicant: **FUJITSU LIMITED, 1015, Kamikodanaka
Nakahara-ku, Kawasaki-shi Kanagawa 211 (JP)**

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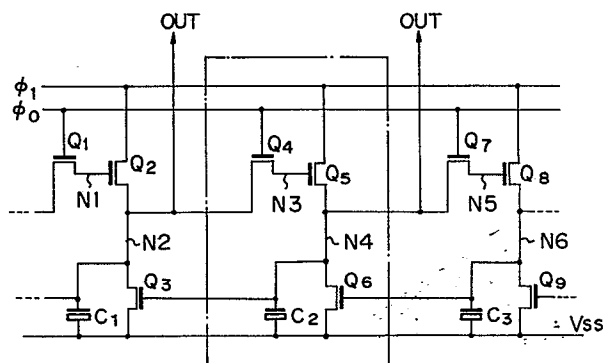
Inventor: **Takemae, Yoshihiro, 303, 8-13-24, Akasaka
Minato-ku, Tokyo 107 (JP)**

Designated Contracting States: **DE FR GB**

Representative: **Sunderland, James Harry et al,
HASLITINE LAKE & CO Hazlitt House 28 Southampton
Buildings Chancery Lane, London WC2A 1AT (GB)**

Shift register.

A shift register having a simple circuit structure and used, for example, in a dynamic RAM device for a refresh operation. The shift register comprises a plurality of circuit stages mutually connected in cascade. Each of the circuit stages comprises: a first transistor (Q_4) for a transfer gate which is turned on and off by a first clock signal (ϕ_0) and to which is input the output signal (OUT) of the previous circuit stage; a second transistor (Q_5) whose gate electrode is connected to the output of the first transistor, whose drain or source electrode receives a second clock signal (ϕ_1) having a different phase from the first clock signal, and whose source or drain electrode outputs an output signal; and a reset means (Q_6 , C_2) for rendering the input portion of the first transistor to a reset condition on the basis of the output signal, thereby sequentially transmitting data through each circuit stage.



stage has a very complex circuit structure and a large number of circuit components. Therefore, the circuit width of each circuit stage on a semiconductor device is relatively large, and it is impossible to use /^{such a} shift register in the above-mentioned memory device.

In view of the problems of the aforementioned conventional shift register, the present invention adopts an idea of constituting each circuit stage in a MIS dynamic-type shift register by using three MIS transistors as base components.

An embodiment of the present invention can simplify the circuit structure of each circuit stage and decrease the number of circuit components used in each circuit stage, thereby decreasing the width of the space occupied by each circuit stage on a semiconductor substrate.

According to the present invention, there is provided a shift register having a plurality of circuit stages connected in cascade and receiving first and second clock signals different in phase from each other for driving the shift register, each of the circuit stages comprising: a first transistor operatively connected to receive an input signal and the first clock signal for transferring the input signal in response to the first clock signal; a second transistor having a gate operatively connected to receive the input signal, a source and a drain, one of the source and drain receiving the second clock signal, the second transistor providing an output signal at the other of the source and drain in response to the input signal and the second clock signal; and a reset means for resetting the input signal applied to the first transistor in response to the output signal, the output signal of the present circuit stage providing the input signal applied to the first transistor of the succeeding stage.

Reference is made, by way of example, to the accompanying drawings in which:

Figure 1 is a block circuit diagram illustrating a memory device which uses a shift register according to the present invention;

5 Figure 2 is an electric circuit diagram illustrating a shift register as an embodiment of the present invention;

Figure 3 is a waveform diagram illustrating the operation of the shift register of Fig. 2;

10 Figures 4 and 5 are electric circuit diagrams each illustrating another embodiment of the present invention and each being a modification of the shift register of Fig. 1;

Figure 6 is an electric circuit diagram illustrating still another embodiment of the present invention; and

15 Figure 7 is a waveform diagram illustrating the operation of the shift register of Fig. 6.

20 Figure 1 illustrates a dynamic memory device wherein a shift register, possibly a ring counter type shift register, is used to sequentially designate a word line connected to memory cells for the purpose of ^arefresh operation. The memory device of Fig. 1 comprises a memory cell array MCA having a plurality of memory cells MC each being connected to a bit line BL and a word line WL, a column decoder CD, a word decoder WD, and the above-mentioned shift register SR. The word decoder comprises a NOR gate NG for decoding address signals and an electronic switch SW for every
25
30 word line WL.

In the memory device of Fig. 1, an access operation such as a readout operation or write-in operation is effected in a state in which the switch SW is positioned so as to connect the output of the NOR gate NG to the corresponding word line WL. The word line WL is selected by a decoded signal, i.e., the output signal of the NOR gate NG, and the bit line BL is
35

selected by the column decoder CD. Thus, the memory cell MC is selected and the access thereto is performed in a known manner.

The switch SW is controlled by^a/refresh enable signal RFE of, for example, a high potential level so as to connect each of the output terminals of the shift register SR to the corresponding word lines. The shift register SR shifts^a/data "1" cyclically, and selects a word line sequentially, thereby refreshing memory cells connected to each word line.

Figure 2 illustrates a structure of a shift register as an embodiment of the present invention used, for example, in the memory device of Fig. 1. In Fig. 2, the circuit portion surrounded by a dot-dash line constitutes a circuit of one stage of the shift register, and comprises three MIS transistors Q_4 , Q_5 , and Q_6 , and one capacitor C_2 .

The shift register of Fig. 2 is controlled by two kinds of clock pulses ϕ_0 and ϕ_1 , and these clock pulses ϕ_0 and ϕ_1 have phases mutually different, for example, by 180° , as shown in Fig. 3. The clock pulse ϕ_1 has an amplitude extending between power supply voltages V_{SS} and V_{CC} . However, the voltage of a low level portion of the clock pulse ϕ_0 is within the range of V_{th} to $2V_{th}$ and is preferably $1.5 V_{th}$, although the voltage of a high level portion thereof is V_{CC} ; where V_{th} is a threshold voltage of the MIS transistors, for example^{that of} Q_4 .

Assume that the potential of an output node N2 of the pre-stage circuit is high, as shown in Fig. 3. At a time t_0 , the transistor Q_4 is turned on in response to the rising of the clock pulse ϕ_0 from a low level, e.g. $1.5 V_{th}$, to a high level.^{Hence} the potential of a node N3 rises to a high level, and the transistor Q_5 is turned on. At a time t_1 , the clock pulse ϕ_0 falls and the clock pulse ϕ_1 rises from a low level, i.e., V_{SS} to a high level, i.e. V_{CC} , so that node N4 rises to a high level because the transistor Q_5 is in^{the}/on-state.

At this time/^(t₁) the potential of the node N3 rises to a higher potential level in response to the potential rise of the clock pulse ϕ_1 due to the bootstrap effect of the transistor Q_5 , so that the node N4 rises to V_{CC} level as well as the clock signal ϕ_1 . When the potential of the node N4 rises, a transistor Q_3 of the preceding stage is turned on, and the potential of an output node N2 of the pre-stage circuit falls to a low level. At this time, the potential of the clock pulse ϕ_0 is at a low level, but since the low level potential of the clock pulse ϕ_0 is 1.5 V_{th} as mentioned before, when the potential of the node N2 becomes lower than $1/2 V_{th}$, the transistor Q_4 is turned on, thereby pulling down the potential of the node N3 rapidly. In this way, transmission of the high level potential from the node N2 to node N4 is effected, and, similarly, the high level potential is sequentially transmitted through each circuit stage. The capacitor C_2 is provided so as to decrease the voltage loss caused when electric charges are transmitted from one stage to a succeeding stage, by rendering the capacitance of the output node N4 sufficiently larger than that of the input circuit, i.e. the node N5 of the succeeding stage. Since the low level voltage of the clock pulse ϕ_0 is 1.5 V_{th} , when, for example, the potential of the node N4 is at a high level and the clock pulse ϕ_0 is at a low level, i.e., 1.5 V_{th} , the potential of the node N5 of the next stage becomes 0.5 V_{th} and it is possible to keep a transistor Q_8 of the succeeding stage in a cut-off state. Therefore, it is possible to maintain the potential of a node N6 at a low level, i.e., V_{SS} . If the low level potential of the clock pulse ϕ_0 is equal to or larger than 2 V_{th} , the potential of the node N6 disadvantageously rises to a value equal to or larger than V_{SS} in response to the rise or fall of the clock pulse ϕ_1 . It is necessary that the low level voltage of the clock pulse ϕ_0 is higher than V_{th} and lower than 2 V_{th} . Considering the variations in characteristics of each MIS

transistor, it is preferable that the low level voltage of the clock pulse ϕ_0 is a value near $1.5 V_{th}$.

Figure 4 illustrates a circuit of one stage of a shift register as another embodiment of the present invention. The circuit of Fig. 4 differs from that of Fig. 2 in that a transistor Q_4' is connected in parallel to the input transfer gate transistor Q_4 , a voltage V_B having a voltage of approximately $1.5 V_{th}$ is applied to the gate of the transistor Q_4' , and the clock pulse ϕ_0 in Fig. 2 is replaced by a clock pulse ϕ_0' . The low level voltage of the clock pulse ϕ_0' is V_{SS} which is the same as that of the clock pulse ϕ_1 , and the clock pulse ϕ_0' has the same waveform as that of a pulse formed by shifting the phase of the clock pulse ϕ_1 by 180° , for example. The other portions of Fig. 4 are the same as those of the circuit of Fig. 2 and are designated by the same reference symbols.

In the circuit of Fig. 4, the parallel circuit of the transistors Q_4 and Q_4' effects the same operation as that of the transistor Q_4 of Fig. 2. That is, when the clock pulse ϕ_0' is low, the transistor Q_4 is turned off and the nodes N2 and N3 are connected only via the transistor Q_4' . Since the voltage V_B of $1.5 V_{th}$ is applied to the gate of the transistor Q_4' , the transistor Q_4' becomes equivalent to the transistor Q_4 when the clock pulse ϕ_0 in the circuit of Fig. 2 is in a low potential level, i.e., $1.5 V_{th}$.

In the circuit of Fig. 4, it is not necessary to strictly regulate the voltage level of the clock pulse ϕ_0' , and it is advantageously possible to enlarge the allowable error of the voltage level of the clock pulse ϕ_0' .

Figure 5 illustrates a circuit of one stage of a shift register as still other embodiment of the present invention. The circuit of Fig. 5 further comprises transistors Q_6' and Q_6'' connected to the transistor Q_6 in the circuit of Fig. 2. The transistors Q_6 and Q_6''

are mutually cross-coupled at the gates and the drains,
and a signal from the output node N6 of the succeeding
stage is input to the drain of the transistor Q_6 ,
i.e., a node N4' via the transistor Q_6 '. The other
5 portions are the same as those of the circuit of Fig. 2
and are designated by the same reference symbols.

In the circuit of Fig. 5, a high level voltage of,
for example, the node N4 is transmitted to the succeeding
stage circuit, and when the output node N6 of the
10 succeeding circuit becomes high, the potential of the
node N4', i.e., the gate of the transistor Q_6 becomes
high, thereby clamping the potential of the node N4
to V_{SS} . When the potential of the succeeding output
node N6 becomes low after the high level voltage of the
15 succeeding output node N6 is transmitted to a further
succeeding stage, the potential of the node N4 is low
and, thus, the potential of the node N4' is still high,
so that the potential of the node N4 is always clamped
to the voltage V_{SS} by the transistor Q_6 . Therefore,
20 by using the circuit of Fig. 5, it is possible to
prevent the node N4 from being in an electrically
floating state when the node N4 is at a low level. It
is also possible to increase the reliability of
operation of a shift register, because the potential of
25 the node N4 does not fluctuate due to noise and so on.

Figure 6 illustrates a shift register as still
another embodiment of the present invention. Each stage
of the shift register, for example, a stage SRL, comprises
eleven MIS transistors Q_{101} , Q_{102} , ---, Q_{111} .
30 The transistor Q_{110} is a depletion type load transistor.
The transistors Q_{101} , ---, Q_{104} constitute an input
circuit and a first reset means for resetting an input
portion/of ^(a node N12) a transistor Q_{105} . The transistors
 Q_{106} and Q_{107} constitute a second reset means which
35 resets ^(a node N13) an output portion/of the transistor Q_{105} . The
transistors Q_{109} , Q_{110} and Q_{111} constitute a
latch circuit which is driven by the output signal of

a transistor Q_{108} . In the circuit of Fig. 6, nodes N05, N15, --- correspond to the nodes N2, N4, --- of the circuit of Fig. 2. Clock pulses ϕ_2 and ϕ_3 are pulses having a phase difference of, for example, 180° .

5 The high potential level of both clock pulses ϕ_2 and ϕ_3 is V_{CC} , and the low potential level of both clock pulses ϕ_2 and ϕ_3 is V_{SS} .

Operation of the shift register of Fig. 6 is described with reference to Fig. 7. Before a time t_0 ,
10 data "1" is stored at a circuit stage SR0, and the potential of the node N05 is high. At this time a node N12 is already charged to a high potential level by the turned on transistor Q_{103} .

At the time t_0 , the potential of the clock
15 pulse ϕ_3 changes from high to low. Thereby, a current flows from the node N05 to a clock line ϕ_3 via the transistor Q_{008} , and the potential of the node N05 changes from high to low, i.e., the output signal of the circuit stage SR0 becomes "0". In response to the
20 change of the potential of the node N05 to low, the transistor Q_{011} is turned off, and the potential of a node N06 changes from low to high.

At a time period approximately between times t_1 and t_2 , the potential of the clock pulse ϕ_2 changes
25 from low to high, a high level signal is transmitted from a node N12 to a node N13 via the turned on transistor Q_{105} , so that the potential of the node N13 becomes high. Thereafter, the clock pulse ϕ_2 again changes from high to low.

30 At a time t_3 , the clock pulse ϕ_3 changes from low to high. Since the potential of the node N13 is high, the potential of the node N15 is pulled up to high via the turned on transistor Q_{108} , and the output data of the circuit stage SR1 becomes "1". When the
35 potential of the node N15 becomes high, the transistor Q_{101} is turned on, and the potential of a node N11 becomes high. Thereby, the transistor Q_{104} is turned

on, and the node N12 is reset from high to low.

5 In the circuit stage SR0, since the potential of the node N6 is high, the transistor Q₀₀₇ is turned on. The transistor Q₀₀₆ is also turned on because of the high potential level of the clock pulse ϕ_3 . Therefore, the potential of the node N03 is reset to low, and the transmission of data "1" from the circuit stage SR0 to the circuit stage SR1 is performed (completed).

10 As mentioned above, according to the present invention, it is possible to constitute a ^{shift register, for example a} ring counter type shift register by using a very simple circuit structure, and to considerably reduce the width occupied by each circuit stage on a semiconductor substrate. Therefore, it becomes very advantageous to dispose the
15 shift register parallel to a decoder as mentioned before.

CLAIMS

1. A shift register having a plurality of circuit stages connected in cascade and receiving first and second clock signals different in phase from each other for driving the shift register, each of said circuit
5 stages comprising:

a first transistor operatively connected to receive an input signal and said first clock signal for transferring the input signal in response to said first clock signal;

10 a second transistor having a gate operatively connected to receive said input signal, a source and a drain, one of said source and drain receiving said second clock signal, said second transistor providing an output signal at the other of said source and drain in
15 response to said input signal and said second clock signal; and

a reset means for resetting said input signal applied to said first transistor in response to said output signal, the output signal of the
20 circuit stage providing the input signal applied to the first transistor of a succeeding/^{circuit}stage of the shift register

2. A shift register according to claim 1, wherein said reset means comprises a third transistor which is
connected /^{in series with} said second transistor and which
25 is turned on and off by the output of the succeeding circuit stage.

3. A shift register according to claim 2, wherein each of said circuit stages comprises a capacitor
connected/ⁱⁿparallel with said third transistor.

30 4. A shift register according to claim 1, wherein said reset means comprises a third transistor connected in series with said second transistor, a fourth transistor cross-coupled with said third transistor, and a fifth transistor which is connected in series
35 with said fourth transistor and which is turned on and off by an output signal of the succeeding circuit stage.

5. A shift register according to claim 4, wherein each of said circuit stages comprises a capacitor connected to said third transistor.

6. A shift register according to any preceding claim, wherein the phases of said first clock signal and said second clock signal differ from each other approximately by 180 degrees.

7. A shift register according to any preceding claim, wherein the voltage level of said first clock signal reciprocates between a power supply voltage and a voltage within the range of V_{th} and $2V_{th}$.

8. A shift register according to any one of claims 1 to 6, wherein each of said circuit stages further comprises a further transistor which is connected in parallel with said first transistor and whose gate receives a bias voltage within the range of V_{th} to $2V_{th}$, where V_{th} is the threshold voltage of said first transistor.

9. A shift register according to claim 1, wherein each of said circuit stages further comprises a latch circuit driven by the output signal of said second transistor for storing the output signal, and said reset means comprises a first reset means for resetting the input signal applied to said first transistor after said latch circuit has stored the output signal and a second reset means for resetting the input signal at said gate of said second transistor depending on the data stored in said latch circuit and in response to said second clock signal.

[illegible][illegible]

Fig. 3

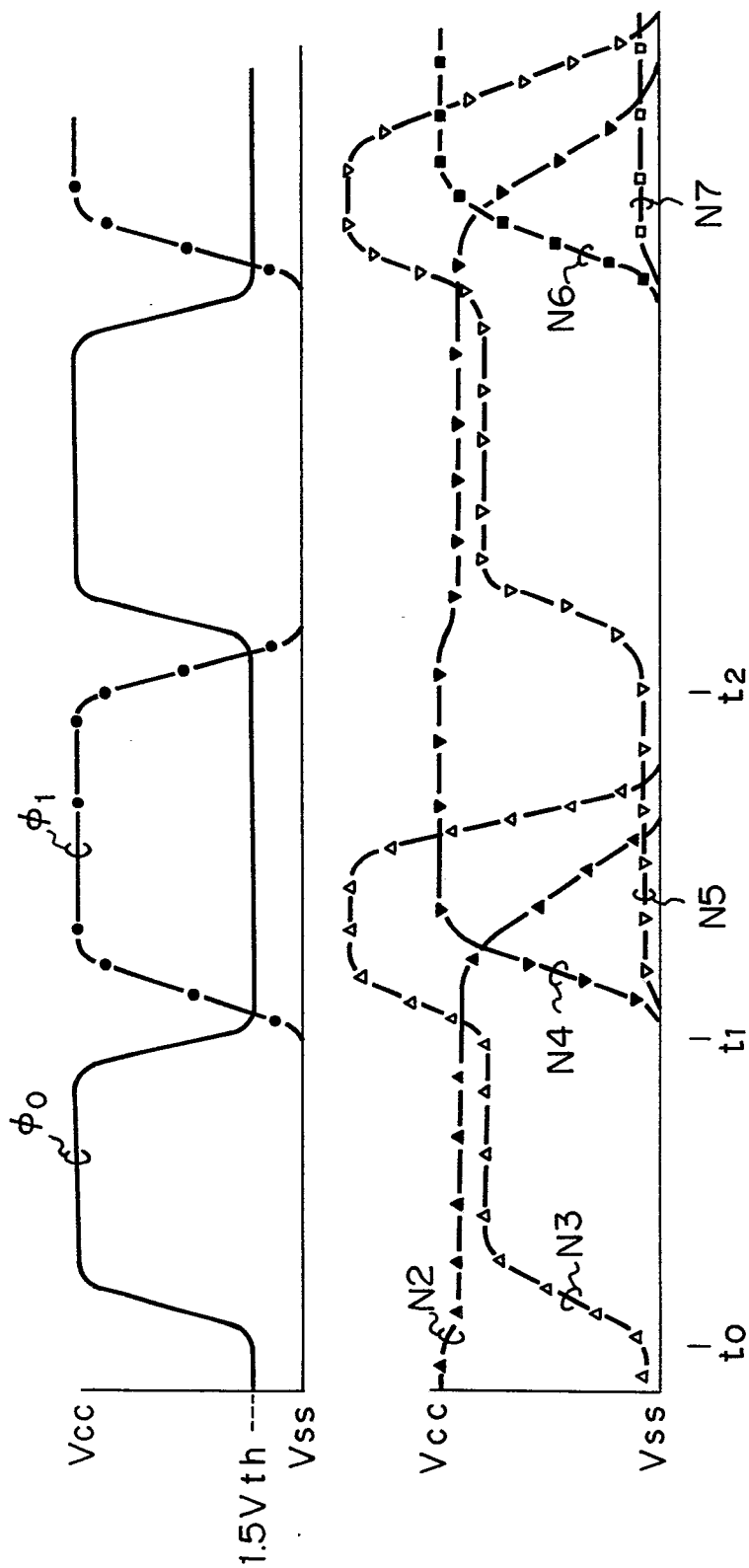


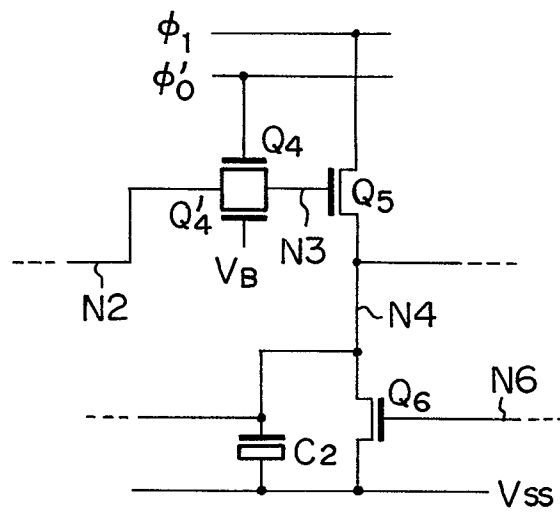
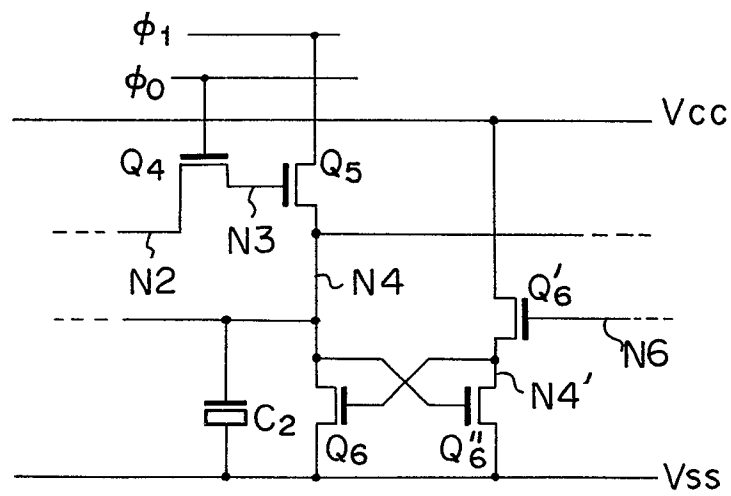
Fig. 4*Fig. 5*

Fig. 6

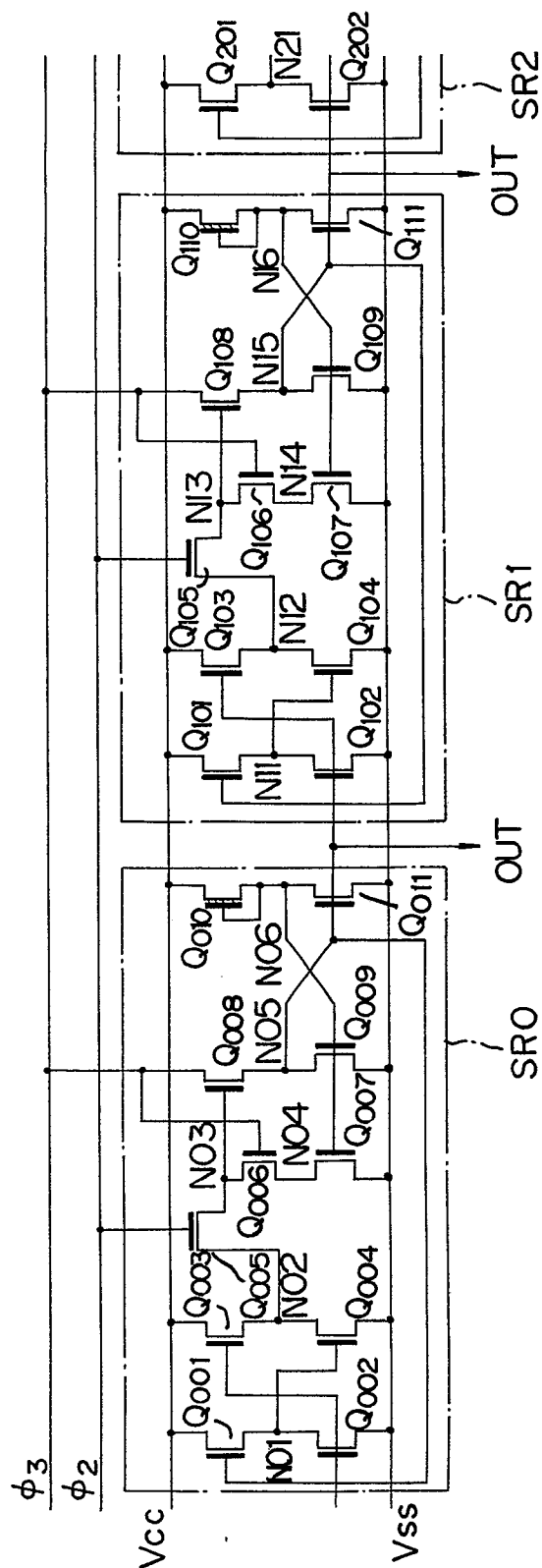
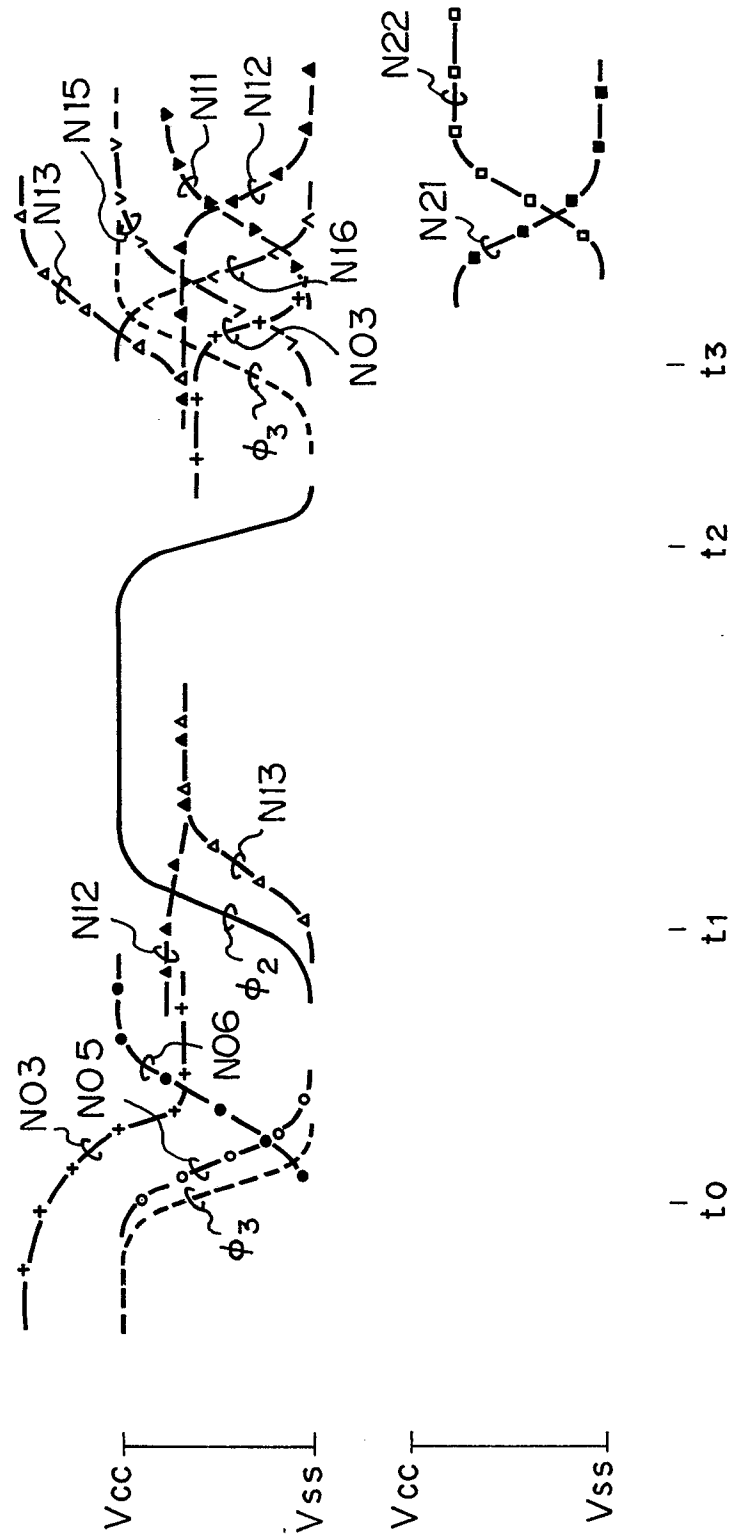


Fig. 7



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