

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MIANYANG BOE OPTOELECTRONICS TECHNOLOGY CO., LTD.;
WUHAN CHINA STAR OPTOELECTRONICS SEMICONDUCTOR DISPLAY
TECHNOLOGY CO., LTD.; TIANMA MICROELECTRONICS CO., LTD.;
AND VISIONOX TECHNOLOGY, INC.,
Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.
Patent Owner.

Case IPR2024-00620
U.S. Patent No. 9,330,593

PATENT OWNER'S PRELIMINARY RESPONSE

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PATENT OWNER'S EXHIBIT LIST

Exhibit	Description
Ex. 2001	Order Amending Schedule, Inv. No. 337-TA-1351
Ex. 2002	Notice of Prior Art, Inv. No. 337-TA-1351
Ex. 2003	Westlaw Company Investigator Report for Mianyang BOE
Ex. 2004	Assignment for U.S. Patent Application No. 15/031,174
Ex. 2005	Assignment for U.S. Patent Application No. 15/031,174
Ex. 2006	Assignment for U.S. Patent Application No. 16/097,538
Ex. 2007	Assignment for U.S. Patent Application No. 15/562,853
Ex. 2008	Assignment for U.S. Patent Application No. 16/968,978
Ex. 2009	Assignment for U.S. Patent Application No. 16/622,918
Ex. 2010	Westlaw Company Investigator Report for TCL Technology Group
Ex. 2011	Westlaw Company Investigator Report for China Star Wuhan
Ex. 2012	May 18, 2017 References Cited by Examiner for U.S. Patent Application No. 15/031,174
Ex. 2013	March 12, 2019 References Cited by Examiner for U.S. Patent Application No. 15/562,853
Ex. 2014	February 2, 2023 References Cited by Examiner for U.S. Patent Application No. 16/968,978
Ex. 2015	May 4, 2022 References Cited by Examiner for U.S. Patent Application No. 16/622,918
Ex. 2016	May 14, 2020 References Cited by Examiner for U.S. Patent Application No. 16/097,538
Ex. 2017	U.S. Patent No. 9,236,377

Ex. 2018	Claim Construction Order, Inv. No. 337-TA-1351
Ex. 2019	Declaration of Dr. Andrew Wolfe, Ph.D.
Ex. 2020	Notice of Allowance for U.S. Patent No. 9,330,593
Ex. 2021	Curriculum Vitae of Andrew Wolfe, Ph.D.

I. Introduction

Petitioner challenges claims 1-8, 14-22, and 25 of U.S. Patent No. 9,330,593 (Ex. 1001, the “’593 Patent”) in its current petition, which is the second petition Petitioner has filed challenging the same claims of the same patent, and asserts many of the same prior art references asserted in its first petition. Petitioner withdrew its previous petition, then waited more than seven months from filing its first petition to file the current petition, gaining in the interim the benefit of analyzing Patent Owner’s validity contentions in a parallel ITC proceeding, and taking those contentions into account before filing the current petition. Discretionary denial is thus appropriate under 35 U.S.C. § 314(a) and the *General Plastic* factors, factors which Petitioner does not even address in its Petition.

Petitioner advances five different grounds based on five different references and alleges only obviousness of the challenged claims. Only one of these grounds, Ground 1 based on U.S. Patent Publication No. 2011/0057190A1 (Ex. 1004, “Kimura”), purports to challenge each of the challenged claims. As to that ground, Petitioner picks and chooses from various embodiments and argues for modifications having no support in Kimura and that, on the contrary, contradict other teachings of Kimura on which Petitioner seeks to rely.

Petitioner’s other grounds are similarly flawed, conjuring problems that do not exist so that Petitioner can implement solutions that do not apply, all the while

ignoring established principles that undercut Petitioner's proposed modifications and combinations. Simply put, there is no rationale or basis for Petitioner's obviousness arguments. Rather, the Petition presents a flawed effort to reconstruct the inventions of the '593 Patent through hindsight. For these reasons as well, the Board should deny institution.

II. The Board Should Exercise Its Discretion to Deny the Petition Under 35 U.S.C. § 314.

Applying *General Plastic*, discretionary denial under 35 U.S.C. § 314(a) is appropriate because each factor favors denial: (1) this Petition challenges the same claims as a previous petition by the Petitioner; (2) when filing its previous petition, Petitioner knew, or should have known, of the prior art asserted in this petition; (3) Petitioner revised its invalidity grounds between the first and second petitions after having studied the Patent Owner's position and responses; (4) at least seven months elapsed between the time the petitioner learned of (or should have learned of) the prior art asserted in the second petition and the filing of the second petition; (5) Petitioner fails to explain the time elapsed between the filings of the two petitions; (6) the Board's resources would be more fairly expended on initial petitions, rather than follow-on petitions from the same petitioner; and (7) the current proceeding will conclude significantly later than other proceedings between the Parties. *See General Plastic Industrial Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 at 16 (PTAB Sept. 6, 2017) (precedential).

On July 26, 2023, Petitioner filed a Petition for *Inter Partes* Review seeking to cancel claims 1-9, 14-23, and 25 of the '593 Patent. *See* IPR2023-01221, Paper 1 (the “First Petition”). The First Petition asserted four grounds for unpatentability based on four prior art references:

1. Chung (U.S. Patent Publication No. 2013/0285888A1);
2. Kim (U.S. Patent Publication No. 2013/0127807A1);
3. Tobita (U.S. Patent Publication No. 2008/0101529A1); and
4. Jeong (U.S. Patent Publication No. 2008/0062097A1).

Id. at 5. The Board issued its Notice of Filing Date accorded on August 28, 2023, setting a deadline of November 28, 2023 for Patent Owner’s preliminary response. IPR2023-01221, Paper 8.

Just weeks before that deadline, on November 8, 2023, Petitioner filed an unopposed motion to terminate the First Petition. Petitioner’s motion argued that “dismissal of this [First Petition] would promote efficiency and minimize unnecessary costs,” and “that termination of the IPR proceeding [wa]s appropriate as both Congress and federal courts have expressed a strong interest in encouraging settlement in litigation.” IPR2023-01221, Paper 9, at 2-3.

On March 6, 2024, over seven months after the First Petition, Petitioner filed a second petition. Paper 1 (the “Second” or “Current Petition”). This Petition

challenges a subset of the claims challenged in the First Petition,¹ and drops Chung and Kim as references in favor of three new prior art references: Kimura (U.S. Pub. 2011/0057190A1), Shin (U.S. Pub. 2007/0063950A1), and Sasaki (U.S. Pub. 2005/0185752A1). *Id.* at 4. Specifically, the Second Petition asserts grounds of unpatentability based on:

1. Kimura;
2. Shin in view of Sasaki;
3. Shin in view of Sasaki, and further in view of Jeong;
4. Tobita; and
5. Tobita in view of Jeong.

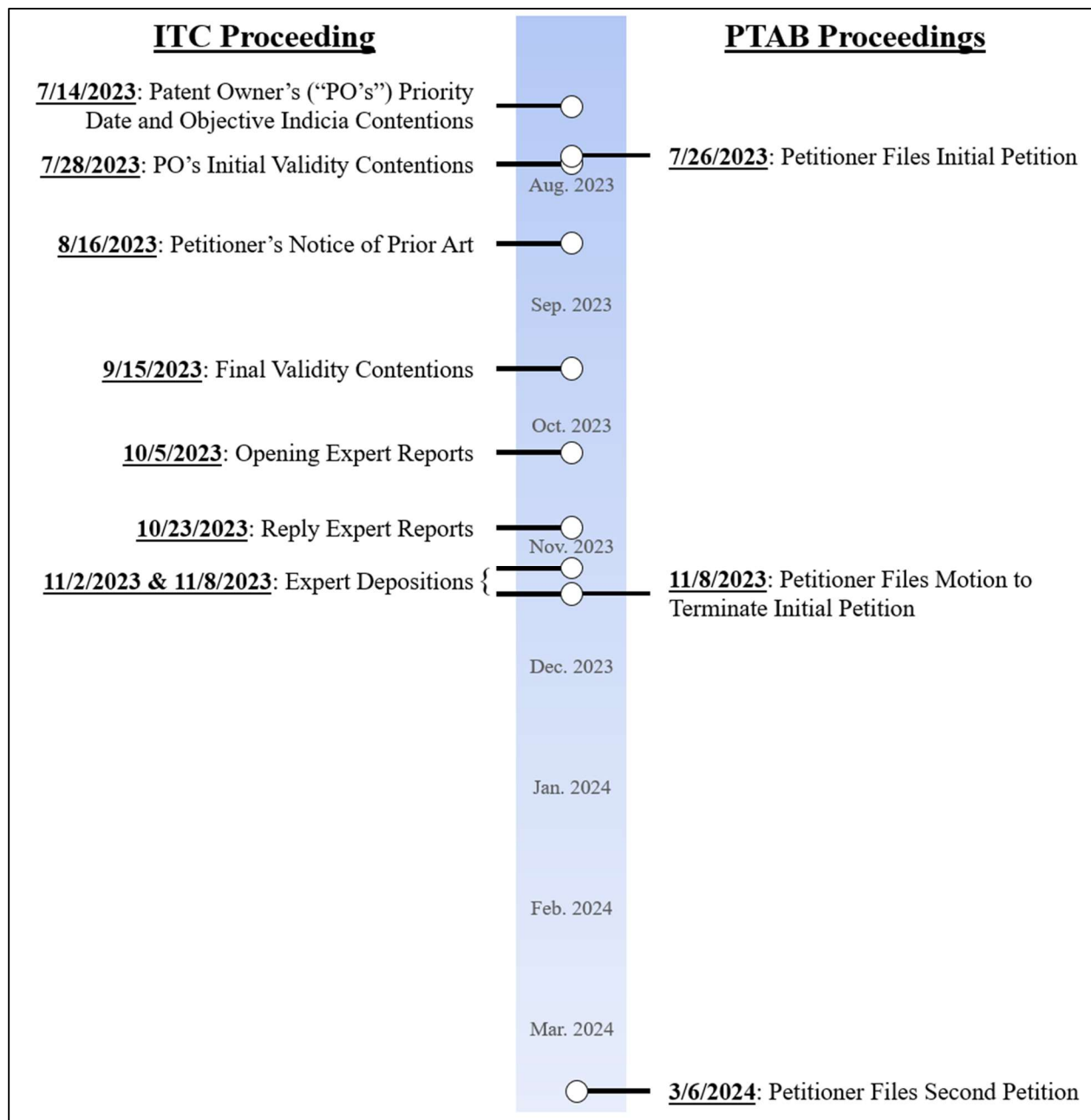
Id. at 4-5.

Contrary to the reasons Petitioner expressed to the Board in its motion to terminate its First Petition, Petitioner now claims it withdrew that the First Petition “to avoid a dispute regarding the ’593 patent’s date of invention.” *Id.* at 6. Notably, given that the first proceeding was terminated prior to Patent Owner’s Preliminary response, no issue as to priority dates was raised in that proceeding.

However, between the filing of the First and Second Petitions, Petitioner has had the benefit of analyzing Patent Owner’s validity positions in a parallel

¹ The Current Petition seeks cancellation of claims 1-8, 14-22, and 25. The First Petition sought cancellation of all of those claims, as well as claim 9.

proceeding before the International Trade Commission between Petitioner Mianyang BOE and Patent Owner Samsung Display, and involving the same patent, ITC Inv. No. 337-TA-1351 (the “ITC Proceeding”). There, Patent Owner has served validity contentions, priority date and objective indicia contentions, opening expert reports, rebuttal expert reports, and expert witness statements. Patent Owner’s final validity contentions, served between the filing of the First and Second Petitions, address all of the references asserted in the First Petition. Furthermore, both parties’ respective experts were deposed and trial is set to begin in just over two weeks from the filing of this response. The relevant milestones in the ITC and PTAB proceedings are summarized below.



See Ex. 2001 at 2-4.

Accordingly, in the ITC Proceeding Petitioner obtained information regarding Patent Owner's validity positions, which apparently compelled them to withdraw and refashion their unpatentability theories before the Board. This is the

type of gamesmanship that the Board warned against in *General Plastic*. Petitioner addresses below the *General Plastic* factors, all of which weigh in favor of the Board exercising its discretion to deny Petitioner’s serial petition.

A. Petitioner Seeks to File Its Serial Petition to Revise Its Grounds After Assessing Patent Owner’s Contentions (Factor 3).

A motivating principle for *General Plastic* is to avoid giving Petitioner the ability to leverage the Patent Owner’s positions for additional bites at the apple. *General Plastic*, IPR2016-01357, Paper 19 at 17 n.14 (collecting cases detailing how adjudicating serial petitions with shifting prior art is inefficient, unfair, incentivizes harassment, and is an abuse of process). This principle underlies factor 3, which evaluates “whether at the time of filing of the second petition the petitioner already received the patent owner’s preliminary response to the first petition or received the Board’s decision on whether to institute review in the first petition.” *Id.* at 16.

Although no preliminary response or decision on institution was filed for the First Petition, this nevertheless presents a manifest case of such abuse. Petitioner has done what *General Plastic* seeks to deter—materially change its unpatentability grounds in a follow-on petition after having had the benefit of studying Patent Owner’s responsive positions on Petitioner’s prior art theories. *See Valve Corp. v. Elec. Scripting Prods., Inc.*, IPR2019-00062, Paper 11 at 13 (PTAB

April 2, 2019) (precedential) (use of materials from related proceeding as a guide to preemptively address anticipated arguments “implicates the fairness concerns discussed in *General Plastic* and favors denying institution”).

Here, Petitioner Mianyang BOE apparently reviewed Patent Owner’s validity contentions, recognized its First Petition was flawed, and then withdrew its Petition to seek out additional prior art in an attempt to correct those deficiencies. Although Petitioner now claims that it withdrew its First Petition to avoid a priority date dispute, the timeline casts doubt on this new explanation. Petitioner would have been aware since before the First Petition that at least one prior art reference, Chung, was not prior art, in view of Patent Owner’s July 14, 2023 contentions in the ITC. If Petitioner were concerned about this priority issue, it is unclear why it would have relied on Chung in its First Petition. Accordingly, it is perhaps more plausible that Petitioner withdrew its First Petition in response to flaws Patent Owner identified in Petitioner’s prior art theories.

Yet regardless of whether Petitioner revised its grounds based on the weaknesses of its theories or based on perceived priority concerns, Petitioner relied on the benefit of receiving and studying the Patent Owner’s contentions, expert

reports, expert deposition transcripts, and briefing to do so.² This raises precisely the type of fairness considerations that underlie *General Plastic*. Moreover, the *General Plastic* factors are “non-exhaustive” and merely “serve to act as a baseline of factors.” *General Plastic* at 16, 18 (emphasizing that “additional factors may arise in other cases”).

B. Petitioner Should Have Raised Its New Challenges Earlier (Factors 1, 2 and 4).

Petitioner could have, and should have, filed the Current Petition over seven months ago. The Current Petition challenges a subset of the claims challenged in the First Petition and Petitioner either knew, or should have known, of all of the prior art asserted in the Current Petition. Finally, Petitioner provides no justification for its delay in asserting that prior art. Therefore, factors 1, 2, and 4 of *General Plastic* weigh in favor of discretionary denial.

Factor 1 of *General Plastic* looks at “whether the same petitioner previously filed a petition directed to the same claims of the same patent.” *General Plastic*, IPR2016-01357, Paper 19 at 16. This is the case here—every claim challenged in

² Even still, the Petition is inexplicably silent regarding the objective evidence of nonobviousness for the ’593 Patent that Petitioner provided to Petitioner BOE in the ITC proceeding.

the Current Petition was also challenged in the First Petition. *Compare* Paper 1 at 1 *with* IPR2023-01221, Paper 1 at 1.

Factor 2 of *General Plastic* looks at “whether at the time of filing of the first petition the petitioner knew of the prior art asserted in the second petition or should have known of it.” *Valve*, IPR2019-00062, Paper 11, at 10 (precedential). The inquiry looks not only at actual knowledge, but also at whether the prior art relied on in the Current Petition “could have been found with reasonable diligence.” *Id.* at 10-11 (determining that factor 2 favored denial where petitioner could have found the relevant prior art references through reasonable diligence). Factor 4 considers “the length of time that elapsed between the time the petitioner learned of the prior art asserted in the second petition and the filing of the second petition.” *Apple Inc. v. Uniloc 2017 LLC*, IPR2020-00854, Paper 9 at 10 (PTAB Oct. 28, 2020) (precedential).

The Second Petition fails to provide any information on when Petitioner first became aware of the prior art, nor does it explain why Petitioner waited seven months before filing a petition on the current grounds. Petitioner’s failure to address factors 2 and 4, or to otherwise provide any explanation for this delay, weighs against institution. *See id.* at 9-11 (determining that factors 2 and 4 weigh against institution where Petitioner failed to explain Petitioner’s first awareness of the asserted prior art).

Furthermore, any explanation by Petitioner would be unavailing because Petitioner either knew, or should have known, of all of the asserted prior art as of the filing of the First Petition. Two weeks prior to the First Petition, Petitioner filed its initial invalidity contentions in the ITC Proceeding, asserting Shin. Both Tobita and Jeong were asserted in the First Petition. IPR2023-01221, Paper 1 At 5. And Petitioner should have known of Sasaki and Kimura as of the filing of the First Petition.

Petitioner's filings in the ITC Proceeding demonstrate that Petitioner could have found Sasaki with reasonable diligence. Indeed, just a few weeks after the filing of the First Petition, Petitioner identified Sasaki in a Notice of Prior Art that it served in the ITC Proceeding. Ex. 2002 at 11. The same is true for Kimura, which was cited by Examiners as prior art in five different U.S. patent applications involving applicants related to Petitioner prior to July 2023.³ Moreover, on June 9,

³ BOE Technology Group Co., Ltd. is the parent company of petitioner, Mianyang BOE Optoelectronics Technology Co., Ltd., as well as the assignee for U.S. Patent Application Nos. 15/031,174, 16/097,538, 15/562,853, and 16/968,978. *See* Ex. 2003 at 4 (showing corporate relationship); Exs. 2004-2008 (patent assignments to BOE Technology Group Co., Ltd.). Shenzhen China Star Optoelectronics Semiconductor Display Technology Co., Ltd. ("China Star Shenzhen") is the

2023, almost two months before the First Petition, Petitioner filed IPR2023-00941 against another of Patent Owner's patents, asserting U.S. Pat. Pub. 2003/0132931, a patent publication that shares a common inventor and assignee with Kimura. Additionally, it is clear that Petitioner has extensively studied Kimura's inventions, as Petitioner's Notice of Prior Art in the ITC Proceeding lists 29 pieces of prior art authored by Dr. Kimura. *See generally* Ex. 2002.

C. Petitioner Fails to Justify Its Serial Petitions (Factor 5).

With respect to factor 5, Petitioner provides no explanation for the time elapsed between the filings of multiple petitions directed to the same claims of the same patent. Regarding its previous petition, Petitioner states only that:

Finally, while petitioner did file another IPR petition challenging the claims of the '593 patent, it withdrew that petition before both the filing of Patent Owner's preliminary response and the Board's

assignee of U.S. patent application no. 16/622,918. Ex. 2009. China Star Shenzhen was acquired by TCL Technology Group, Ex. 2010 at 20, which is petitioner Wuhan China Star Optoelectronics Semiconductor Display Technology Co., Ltd.'s parent company. Ex. 2011 at 7. Kimura was cited by the Examiner in an office action in each of those five patent applications. Exs. 2012-2015 (citing Kimura), Ex. 2016 (citing U.S. Patent No. 9,236,377, Ex. 2017, which was previously published as Kimura).

statutory deadline for issuing an institution decision. *See* IPR2023-01221, Paper 10. Petitioner did so to avoid a dispute regarding the '593 patent's date of invention: unlike certain of the references in the prior petition, the references here all qualify as prior art under pre-AIA 102(b). Thus, this is not a case where there are multiple IPRs challenging the same patent: only this IPR is at issue.

Paper 1 at 6. While Petitioner provides a purported reason for withdrawing the First Petition, Petition fails to account for the time elapsed between the filing of the two petitions. *See Apple*, IPR2020-00854, Paper 9 at 11 (concluding that the fifth *General Plastic* factor weighed against institution where petitioner provided no explanation for the time between petitions).

Furthermore, Petitioner's explanation for withdrawing its First Petition is contradictory and inadequate. Petitioner represented to the PTAB in moving to terminate its First Petition that it was doing so for "efficiency" purposes and in view of "a strong interest in encouraging settlement." IPR2023-01221, Paper 9 at 1-2. Ignoring its prior written representation to the Board, Petitioner now claims it withdrew its previous petition not for the reasons it provided, but because the First Petition relied on references that postdate Patent Owner's date of conception. Paper 1 at 6. But even this new explanation is questionable, as noted above for Factor 3.

D. Denying Institution is Efficient (Factors 6 and 7)

The sixth and seventh *General Plastic* factors are “‘the finite resources of the Board’ and ‘the requirement under 35 U.S.C. § 316(a)(11) to issue a final determination not later than 1 year after the date on which the Director notices institution of review.’ . . . The sixth and seventh factors are efficiency considerations.” *Valve*, IPR2019-00062, Paper 11 at 15 (precedential) (internal citations omitted).

The Board should not expend its finite resources to endorse Petitioner’s second bite at the apple. *See General Plastic*, IPR2016-01357, Paper 19 at 21 (non-precedential) (“multiple, staggered petition filings . . . are an inefficient use of the *inter partes* review process and the Board’s resources”). This is particularly so here, where Petitioner does not even attempt to address the efficiency concerns that stem from its serial petitions. *See generally* Paper 1 (failing to address efficiency concerns or otherwise explain Petitioner’s decisions). Moreover, Petitioner’s new explanation for withdrawing its First Petition suggests that its serial filings resulted from its own errors. *See General Plastic*, IPR2016-01360, Paper 12 at 9 (PTAB Nov. 14, 2016) (non-precedential) (denying institution because petition “seek[ing] to remedy . . . [Petitioner’s] own error . . . imposes an unnecessary burden on the Patent Owner and the Board”). Petitioner admits that certain references in the First Petition did not qualify as prior art references, Paper 1 at 6 (“*unlike* certain of the

references in the prior petition, the references here all qualify as prior art”) (emphasis added), yet Patent Owner made Petitioner aware that at least certain of the art in its petition was not prior art to the ’593 Patent 14 days *before* the First Petition was filed.

Considering the schedules of related proceedings further supports denial. In June, 2023, Petitioners filed four Petitions for *Inter Partes* Review, challenging the other patents at issue in the ITC Proceeding.⁴ If instituted, the Current Petition would be almost nine months behind the other four Patent Office proceedings challenging the other patents in the ITC Proceeding. By the time an institution decision is due in this case, September 21, 2024, the oral argument for the other four proceedings will be well underway. Furthermore, trial in the ITC Proceeding would have concluded and the Parties will be under two months away from a ruling on the merits, including the validity of the challenged claims. Therefore, by the time a Final Written Decision is due in this proceeding, all of the other disputes between the Parties will have been resolved, and any appeals well under way. For these reasons, judicial economy would be best served in letting the current

⁴ Petitioner filed IPR2023-00941 on June 9, 2023, IPR2023-00987 and IPR2023-00988, and IPR2023-01075 on June 21, 2023.

proceedings conclude instead of creating a laggard parallel proceeding, further delaying resolution of the controversies between the Parties.

III. Claim Construction

Patent Owner notes that on September 11, 2023, the Administrative Law Judge in the related ITC Proceeding, Investigation No. 337-TA-1351, issued a claim construction order construing certain claim terms of the '593 Patent. Ex. 2018 at 15-37.

For purposes of this Preliminary Response, however, Patent Owner does not believe that any specialized constructions are necessary. Petitioner fails to establish a reasonable likelihood of prevailing under any claim interpretation.

IV. Level of Ordinary Skill in the Art

Patent Owner proposes that a POSITA with regard to the '593 Patent would have had a relevant technical degree in Electrical Engineering, Computer Engineering, Materials Science, Physics, or the like, and experience in active matrix display design and electroluminescence. *See* Ex. 2019, ¶ 36. Patent Owner notes that, in the related ITC Proceeding, the Administrative Law Judge agreed with and adopted Patent Owner's proposal. Ex. 2018 at 12 (explaining, among other things, the '593 Patent is "directed to active matrix display technologies for organic light-emitting diode displays" and "[i]t is therefore reasonable to expect

one of skill to have specific experience with active matrix display circuitry and electroluminescence”).

Petitioner has proposed a POSITA would have had “a Bachelor’s degree in electrical engineering or similar discipline, along with 2–3 years of circuit design/analysis experience.” Pet. at 5.

Petitioner’s definition is incorrect, as it entails only general “circuit design” experience with no experience in active matrix display design and electroluminescence, the subject matter of the ’593 Patent. The ’593 Patent is directed to active-matrix organic light-emitting diode (AMOLED) displays and solving problems specific to those displays, including improving scan-on time and reducing the physical footprint of the scan circuitry required to program each row of pixels. Ex. 2019, ¶ 38. Important aspects and considerations of the pixel circuit design are unique to the context of active matrix display design and to electroluminescent displays. *Id.* For example, the signal timings generated by the scan driver and provided to the pixel circuits are specialized to AMOLED displays.

Petitioner’s definition does not accurately reflect the experience of those working in the field of the ’593 Patent—Petitioner’s definition does not include *any* experience in display design. Ex. 2019, ¶ 39. Indeed, Petitioner’s misreading of the art appears to result from a lack of appreciation of active matrix display-related technology. For example, Kimura’s disclosures relating to the GOUT and

SOUT signals are specific to the display context, and make clear that these signals serve different functions within the scan driver and pixel array. *See, e.g.*, Kimura ¶¶ [0304]-[0305]. Petitioner’s misapplication of these teachings underscores how a proper understanding of active matrix and electroluminescent displays is critical to understand the content of the prior art. *See, e.g.*, Section V.3, below.

Because Petitioner’s definition fails to include any experience with active matrix display design and electroluminescence, it fails to reflect the background and knowledge of a POSITA. Ex. 2019, ¶¶ 38-39. Petitioner’s expert, Dr. Foty, does not qualify as a person of ordinary skill in the art under the proper definition and accordingly lacks qualification to opine on matters requiring the perspective of a person of ordinary skill.

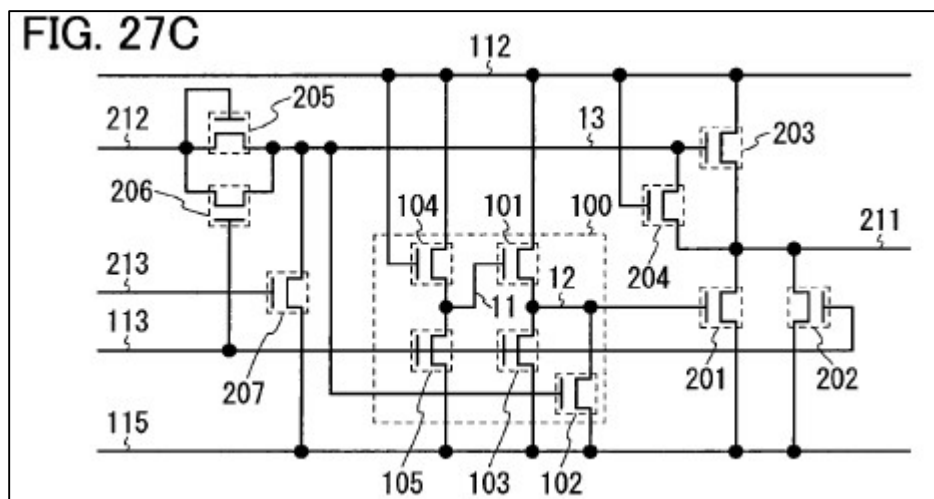
V. Petitioner Has Not Established a Reasonable Likelihood of Prevailing as to Any Challenged Claim.

A. Petitioner Has Not Shown That Kimura Renders Obvious Any Challenged Claim.

The Petition’s arguments as to Kimura all begin with Figure 27C. However, Kimura’s Figure 27C circuit more closely resembles the prior art stage circuits upon which the ’593 Patent’s inventions improved, than the actual claimed inventions.

In particular, the ’593 Patent teaches that its inventions provide a reduction of necessary transistors and signal lines, which led to improvements in

manufacturability, efficiency, and speed. *See, e.g., '593 Patent*, 9:12-26. The '593 Patent specifically criticizes prior art stage circuits having “at least ten transistors” as well as prior art stage circuits requiring additional input signals beyond “first and second clock signals,” and a start pulse or output of a prior stage. *Id.* As shown below, Kimura’s Figure 27C includes 12 transistors (elements 101, 102, 103, 104, 105, 201, 202, 203, 204, 205, 206, and 207) and requires at least 4 input signals (elements 112, 212, 213, 113).



Petitioner provides no reason why a POSITA would choose to start with this design as opposed to any other. As Petitioner acknowledges, “Kimura includes numerous embodiments.” Pet. at 10. Kimura further describes multiple circuit variations within many of its embodiments. For example, Figures 27A-C are described as depicting circuit diagrams of Kimura’s second embodiment, but each of these Figures includes different transistors connected in different ways. *See,*

e.g., Kimura at ¶¶ [0283]-[0287] (describing the different transistors and corresponding connections in the circuits of Figs. 27A, 27B, and 27C).

Petitioner's arguments require the specific configuration and connections shown in Figure 27C to arrive at the challenged claims. Pet. at 10. However, nothing in Kimura teaches or suggests any particular advantages of the specific configuration of transistors and connections depicted in Figure 27C as opposed to any of the other configurations of Kimura's embodiments. Instead, Kimura simply lists numerous potential alternative configurations of its embodiments. *See, e.g.*, Kimura at ¶ [0289] ("In the structures illustrated in...FIGS. 27A to 27C...the second terminal of the transistor 207 can be connected to a wiring that is different from the node 13.... Alternatively, the first terminal of the transistor 207 can be connected to a wiring which is different from the wiring 115...."); *see also, e.g.*, Kimura at ¶¶ [0287], [0291], [0297] (listing other possible alternatives). Kimura provides no explanation as to why the permutation of options Kimura lists were implemented as shown in Figure 27C, let alone provide any reason as to why that particular configuration is advantageous.

Indeed, Petitioner concedes as much, in acknowledging that "Figure 27C does not itself mention all of the depicted transistors, inputs, and outputs," and thus presenting its arguments "in terms of obviousness." Pet. at 15. But Petitioner points to nothing to explain why it would have been obvious for a POSITA to look to the

specific configuration of Fig. 27C as opposed to any of Kimura's numerous other configurations. As Patent Owner's expert explains, a POSITA would have had no reason to do so. Ex. 2019, ¶¶ 43-45. Additionally, and as discussed in greater detail below, while Petitioner asserts that a POSITA would have looked "elsewhere" in Kimura for description of elements not discussed in the context of Figure 27C, Pet. at 15, Kimura's description of Figure 27C is inconsistent with its description of certain of its other Figures and embodiments, including with respect to the timing diagram upon which Petitioner and its expert rely.

Accordingly, as Patent Owner's expert explains, a POSITA would not have looked to Figure 27C as Petitioner contends, and in any event would not have had a reasonable expectation of success in implementing Figure 27C. Ex. 2019, ¶ 45.

1. Petitioner's Application of Kimura Is Flawed.

While Petitioner states that its arguments are based on Kimura's Figure 27C circuit, Pet. at 10, it points to portions of Kimura directed to different circuits and configurations in an attempt to arrive at the requirements of the challenged claims. Notably, Petitioner relies on a timing diagram that is *inconsistent* with the Figure 27C circuit, including disclosures relating to transistor 204 that Petitioner relies upon as purportedly teaching the very point of novelty that led to the allowance of the claims.

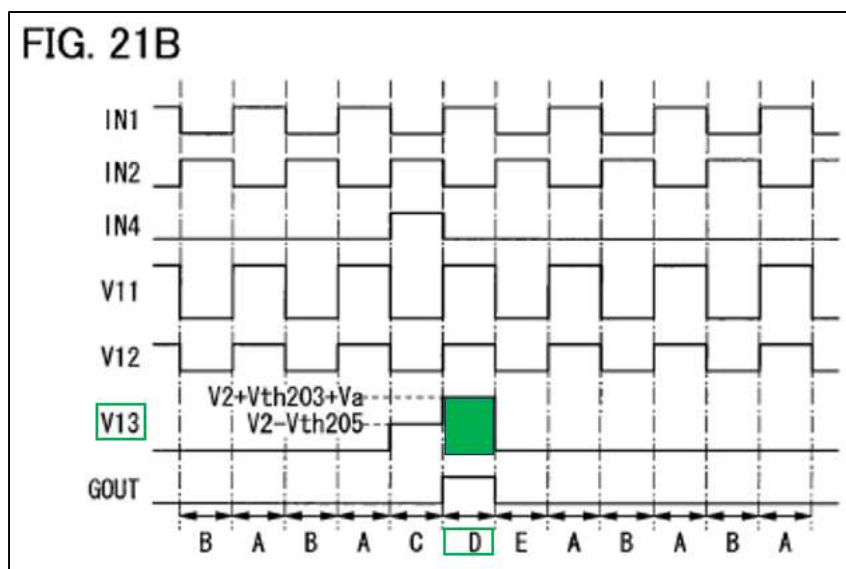
For example, claim elements [1-A] and [15-D] are directed to “an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node.”

While the Petition points to Figure 27C for these limitations, Petitioner’s citations to Kimura to show how the identified elements in Figure 27C satisfy the requirements of these limitations refer to *different* circuits in Kimura. *See, e.g.*, Pet. at 18 (citing discussions related to Figs. 18A, 19A, 19B, *e.g.*, Kimura ¶¶ [0253]-[0256]). Beyond the bare assertion that a POSITA would have understood that components of Figure 27C not discussed with respect to Figure 27C would be “connected” and “function” in the same way “discussed elsewhere,” Pet. at 15, Petitioner provides no explanation as to why a POSITA would look to these different Figures and circuits to understand the operation of Figure 27C’s circuit. Ex. 2019, ¶¶ 47-50.

Petitioner also relies on the timing diagram in Figure 21B for claim elements [1-A] and [15-D]. Pet at 19. Petitioner acknowledges that this timing diagram “is not specific to the device of Figure 27C,” but asserts that a POSITA would have understood that because Figure 27C “includes the same input and output lines and many of the same transistors as Kimura’s other circuits,” and that the Figure 27C

circuit “would (or at least obviously could) be supplied with input signals in the same manner and with the same timing.” Pet. at 19.

However, Kimura’s description of Figure 27C demonstrates that it is *not* compatible with the timings shown in Figure 21B. Ex. 2019, ¶¶ 47-50. Specifically, Kimura explains that for the circuit shown in Figure 27C, “in a period D, the potential of the node 13 can be *lowered*.” Kimura ¶ [0286] (emphasis added). Contrary to this description, however, during period D shown in (annotated) Figure 21B below, the potential of node 13 (V13) is depicted to be at its *highest* level:



Petitioner and its expert do not address this discrepancy, or attempt to explain why a POSITA would nevertheless understand Figure 21B’s timings to be compatible with the Figure 27C circuit. As discussed below, this discrepancy between the timing diagram that Petitioner asserts would apply to Figure 27C’s

circuit and Kimura’s description of the operation of Figure 27C’s circuit would not allow a POSITA to draw conclusions as to whether the Figure 27C circuit satisfies the requirements of the claims. Ex. 2019, ¶¶ 48-50.

2. Kimura Does Not Teach or Suggest Claim Elements [1-D]/[15-G].

Claim elements [1-D] and [15-G] require that “the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver.”

Petitioner must rely on transistor 204 as the claimed transistor in the “first driver,” because it is the only transistor in Figure 27C that, according to Petitioner, has its “on/off operation” “directly control[led]” by the “signal of the third input terminal,” as these claim elements require. Pet. at 24. However, the “first driver” must also control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal,” as set forth in claim elements [1-B]/[15-E]. With respect to how the identified “first driver” allegedly “control[s] the voltage of the second node in accordance with” the signal of the third input terminal, Petitioner also relies on transistor 204.

Specifically, Petitioner points to Kimura’s description that transistor 204 has its gate “connected to wiring 112” (the identified third input terminal), and Petitioner alleges that transistor 204 thus “controls” the voltage node 13 by lowering its potential, citing to the portion of Kimura previously discussed

(Kimura ¶ [0286]). But Kimura provides no further explanation of this lowering, or how it occurs, and Petitioner has identified nothing to suggest that this lowering would meet the requirement of the claims that the first driver “control[s] the voltage of the second node in accordance with” the signal of the third input terminal. Ex. 2019, ¶ 52. For example, Petitioner does not suggest that transistor 204 “controls” the voltage of node 13 in accordance with the signal of the identified third input terminal such that transistor 203 (which has its gate connected to node 13) turns on or off. *Id.* Moreover, the timing diagram Petitioner points to does not reflect a lowered potential of node 13 at all, it reflects a *raised* potential, as explained above. Ex. 2019, ¶ 53.

For at least these reasons, as Patent Owner’s expert explains, no reliable conclusion can be drawn, and a POSITA would not have understood transistor 204 to meet this claim element. Ex. 2019, ¶¶ 52-54. This is of particular significance because claim element [1-D] was identified by the Examiner as a point of novelty in allowing the claims. Ex. 2020 at 7.

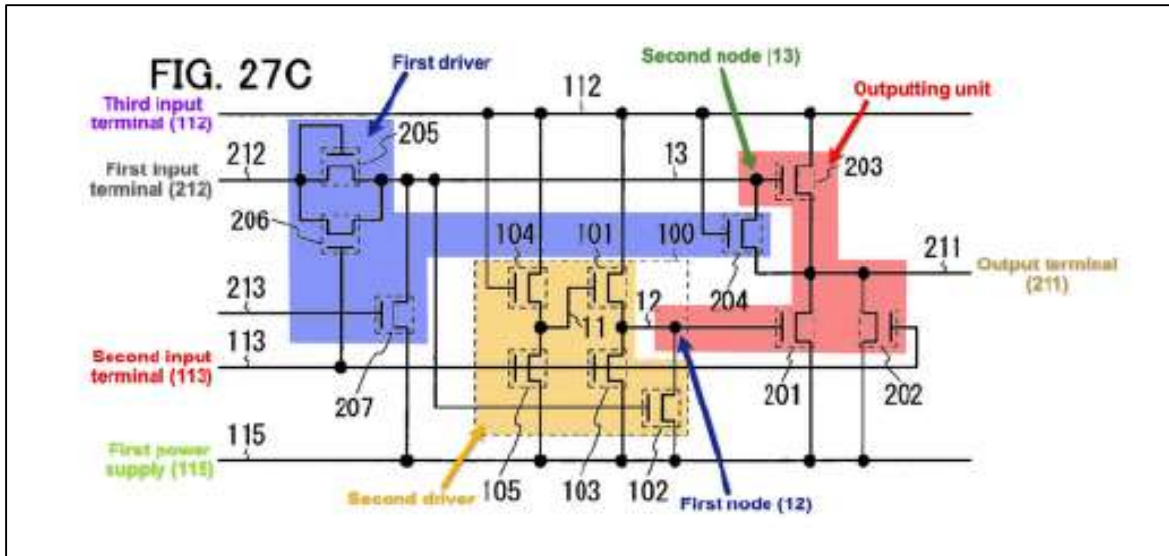
Accordingly, a POSITA would not have looked to Figure 27C and, absent timings, would further not have had a reasonable expectation of success in implementing Figure 27C’s circuit. Ex. 2019, ¶ 54.

3. Kimura Does Not Teach or Suggest Claim Elements [1-A]/[15-D] and [6-B]/[20-B].

Claim elements [1-A] and [15-D] require “an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node.”

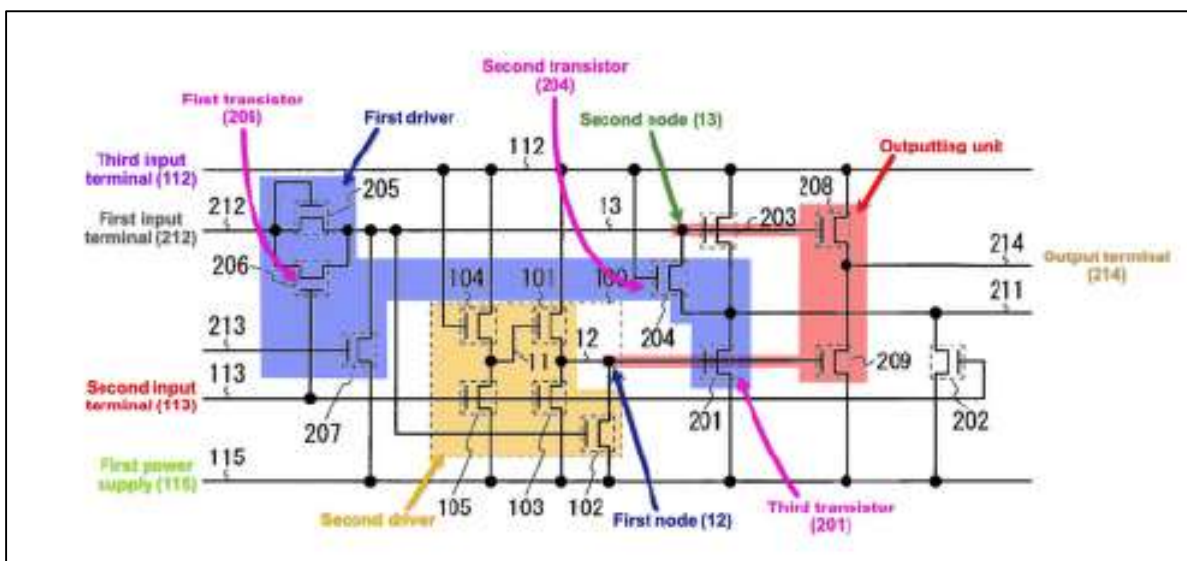
For claims 1 and 15, Petitioner identifies transistor 201 as part of the “outputting unit.” However, that reading of Figure 27C would not meet the requirements of claims 6 and 20, including claim elements [6-B]/[20-B], which require “a second transistor and a third transistor serially positioned between the second node and the first power supply.” Acknowledging this tension, Petitioner is forced to modify its identification of which circuit elements in Figure 27C are part of the claimed “outputting unit” and “first driver” as compared to what it presented for independent claims 1 and 15. Petitioner provides no explanation for its changed analysis, and none exists other than, in hindsight, to realign its reading of the circuit in order to arrive at the requirements of claims 6 and 20.

As shown below, for claims 1 and 15, Petitioner identifies transistors 204, 205, 206, and 207 as part of the “first driver,” and transistors 201, 202, and 203 as part of the “outputting unit.”



Pet. At 15 (annotating Fig. 27C for claims 1 and 15).

In contrast, for claims 6 and 20, Petitioner identifies transistor 201 as part of the “first driver,” and proposes to add two additional transistors, 208 and 209, which it now identifies as the “outputting unit” for these claims (Petitioner no longer asserts that transistor 203 is part of either the “first driver” or “outputting unit”).



Pet. at 31 (annotating composite of Fig. 27C and Fig. 31B for claims 6 and 20).

Petitioner suggests that transistor 201 “operates to connect wiring 115 to node 13 via transistor 204.” Pet. at 30. However, neither the Petition nor Dr. Foty’s declaration suggest that transistor 201 would operate differently as between Figure 27C and the composite Figure 27C and Figure 31B on which Petitioner relies for claims 6 and 20. Similarly, neither Petitioner nor Dr. Foty provides any explanation for why this transistor should be considered part of the “outputting unit” for claims 1 and 15, but part of the “first driver” for claims 6 and 20. This is unsurprising, as no reason exists beyond modifying Figure 27C in a hindsight-driven attempt to arrive at the requirements of claims 6 and 20 that the “first driver” include “a second transistor and a third transistor serially positioned between the second node and the first power supply.” Ex. 2019, ¶¶ 55-68.

As reflected above, transistors 201 and 204 are located in the same positions in both Figure 27C and Petitioner’s modified composite of Figures 27C and 31B, and thus transistor 201 could also be identified as part of the “first driver” under Petitioner’s theory for claims 1 and 15. However, in Figure 27C, if transistor 201 were identified as part of the first driver, the alleged “outputting unit” would not “supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node” as Petitioner suggests. In particular, for that limitation of claims 1 and 15, Petitioner relies upon the same transistor 201, which

has its gate connected to the alleged “first node,” to satisfy this requirement of the “outputting unit.” Pet. at 17-18. If transistor 201 were instead identified as part of the “first driver,” there would be no element in the “outputting unit” that would allow for the “outputting unit” to “supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node” as the claims require. Ex. 2019, ¶ 60.

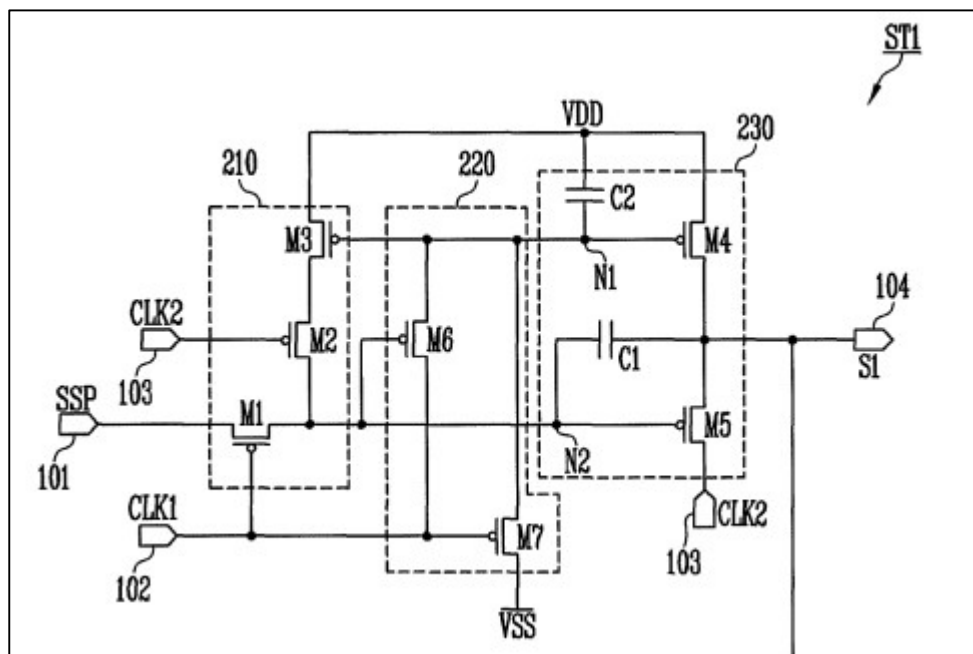
Needing to identify transistor 201 as part of the “first driver” to satisfy the requirements of claims 6 and 20, Petitioner turns to Figure 31B and proposes to add two additional transistors and an additional “output” signal line to Figure 27C, so that Petitioner can identify these additional circuit elements as the new “outputting unit,” and identify transistor 201 as part of the “first driver” instead. This proposed modification results in a stage circuit having 14 transistors and at least 4 input signals. Pet. at 30-31; Ex. 2019, ¶ 61.

Petitioner suggests that a POSITA would have made these modifications because it would “improve display operation, particularly when a large number of stages are employed.” Pet. at 32. Neither Petitioner nor Dr. Foty addresses the significant detriments of adding two additional transistors and an additional signal line to each stage circuit in a display. Contrary to Petitioner’s suggestion, these detriments are only exacerbated where a large number of stages are employed, as this would increase the total number of additional circuit elements that must be

added. Ex. 2019, ¶ 62. Indeed, as described above, the '593 Patent explains that its invention allows for a reduction in the number of transistors and signal lines, and describes specific benefits associated with these reductions. *See, e.g.*, '593 Patent, 9:12-26. A POSITA would not have added these circuit elements and incurred these significant downsides absent clear benefits, and Petitioner's bare claim of "improve[d] display operation" is plainly insufficient. Pet. at 32. Indeed, Kimura itself describes that when "[t]he number of transistors is reduced," "layout area can be decreased" and "power consumption can be reduced." Kimura [0301].

Petitioner does not explain how the modified circuit it proposes for dependent claims 6 and 20 would meet the requirements of their independent claims 1 and 15, respectively, under Petitioner's shifted analysis of Figure 27C's circuit. In any event, even under that shifted analysis, Petitioner's modified circuit fails to teach or suggest the requirements of claims 6 and 20, because the elements Petitioner identifies as part of the new "outputting unit" do not provide scan signals to the output terminal 211 previously identified for claim 1. Ex. 2019, ¶¶ 63-68. Transistors 208 and 209 instead control the provision of signal SOUT to wiring 214. As Petitioner acknowledges, "the signal SOUT is not output to the wiring 211 but can be input to a semiconductor device in a different stage as a start pulse." Kimura ¶ [0304]. Petitioner acknowledges that the SOUT signal is a "different" signal than GOUT. Pet. At 29.

As Petitioner acknowledged for claim 1, GOUT is the signal that is output to the scan lines that provide scan signals to the rows of pixel circuits. Kimura at [0304]; Pet. at 29. The '593 Patent makes clear that the “output terminal” provides an output scan signal to the pixel circuits via scan lines. For example, as shown in Figure 3, the output terminal 104 connects to the scan lines S_n , which provide output scan signals to the pixel circuits.



'593 Patent, Fig. 3 (excerpted); see also, *e.g.*, *id.* Fig. 1. This is further illustrated by the language of claim 15, which recites “a scan driver for supplying scan signals to the pixels through the scan lines, the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal

of the scan signals.”⁵ Thus, the “output terminal” connects the stage circuits to scan lines that are in turn connected to the pixel circuits. *See also, e.g.,* ’593 Patent, 7:46-48 (“In this case, the output terminal 104 outputs the second clock signal CLK2 as a scan signal to the scan line S1”); *id.* at 8:15-17 (“In practice, the stages ST repeat the above-described processes to sequentially output the scan signals to the scan lines.”).

Accordingly, transistors 208 and 209, which control the output of SOUT to wiring 214, do not satisfy the requirements of the “outputting unit” of claim 1. Similarly, wiring 214 does not satisfy claim 1’s requirements of the “output terminal.” Ex. 2019, ¶¶ 63-68.

⁵ The ’593 Patent explains that the output of a previous stage can be provided into a subsequent stage as an input, as is the case with Kimura’s GOUT, but unlike the ’593 Patent’s embodiments, SOUT is provided only to the subsequent stage of the scan driver, and is not also provided to the scan lines that connect to the pixel circuits. In any event, even if SOUT and GOUT were together considered to be the output signal, then transistors 201 and 203 (which control GOUT, i.e., the output signal to wiring 211) would still need to be part of the “outputting unit,” not the “first driver.”

4. Kimura Does Not Teach or Suggest Claim Elements [7-C]/[21-C] and [7-D]/[21-D].

Claim elements [7-C] and [21-C] require that the “outputting unit” include “a first capacitor between the second node and the output terminal.” Claim elements [7-D] and [21-D] require that the “outputting unit” include “a second capacitor between the first node and the first power supply.” The circuit shown in Figure 27C, on which Petitioner relies for independent claims 1 and 15, does not include any capacitors, let alone capacitors in the alleged “outputting unit.” Petitioner thus must seek to add two capacitors to Figure 27C to arrive at the requirements of claims 7 and 21.

Petitioner argues that a POSITA would have added two capacitors to Kimura’s Figure 27C to arrive at these requirements of claims 7 and 21. Petitioner’s assertion that “[c]apacitors can be added in various places” belies the hindsight-driven theory the Petition advances for these claims. Pet. at 32; Ex. 2019, ¶¶ 70-72.

Petitioner looks to other embodiments of Kimura that include capacitors, and asserts that a POSITA would have added those capacitors to Kimura’s Figure 27C. Pet. at 32. In particular, Petitioner looks to Figure 9C and Figure 30C, and asserts that capacitors in these other embodiments “can be used with any of Kimura’s devices, including that in Figure 27C.” Pet. at 33. Petitioner cites in support to Kimura ¶ [0304], but this paragraph says *nothing* about capacitors, let alone adding

capacitors to other embodiments of Kimura, Figure 27C or otherwise. Indeed, Kimura never suggests that these capacitors from different embodiments can or should be added to Figure 27C. Ex. 2019, ¶¶ 70-72.

Petitioner's application of these capacitors is further inconsistent with Kimura's description of the embodiments from which Petitioner proposes to take the capacitors. Ex. 2019, ¶¶ 72-74. For example, Kimura describes that the embodiment of Figure 9C is directed to a "circuit 120" that can be added to circuit 100 in Figures 1A, 6A-6F, 7A-7E, and 8A-8F to delay the provision of signal IN2 in those circuits. Kimura ¶ [0190]. Kimura never discusses adding circuit 120 to other embodiments, and indeed, no circuit 120 appears in Kimura's Figure 27C. Additionally, in Figure 9C, circuit 120 consists of a resistor 121 in addition to capacitor 122. Petitioner seeks to add only capacitor 122 to Figure 27C, and ignores Kimura's disclosures that circuit 120 must include "at least a capacitance component and a resistance component." Kimura ¶ [0191]. Thus, not only does Kimura not suggest adding this capacitor to Kimura's Figure 27C, but Petitioner further seeks to add it in a manner contrary to Kimura's teachings. Petitioner makes no effort to show how a circuit with a resistor and a capacitor could or would be added to its base figure, Figure 27C. Ex. 2019, ¶ 72.

Petitioner's proposed modifications are also inconsistent with Kimura's focus on preventing or reducing transistor deterioration, and its explanation that

reducing the time during which certain transistors are on will reduce deterioration of those transistors. *See, e.g.*, Kimura ¶ [0228] (“Thus in a period during which the transistor 201 is on can be shortened. Accordingly, deterioration of the transistor can be suppressed.”); *see also id.* Abstract, ¶ [0008]. For example, in Petitioner’s proposed modification, the capacitor 122 is connected to the gate of transistor 201, which will prolong its on time, rather than shorten it. Pet. at 34; Ex. 2019, ¶ 73. Similarly, Petitioner proposes to connect capacitor 220 to the gate of transistor 203. Additionally, Kimura describes that due to the addition of capacitor 220 “the potential of the node 13 is likely to rise in the bootstrap operation.” Kimura ¶ [0303]. Petitioner fails to explain why a POSITA would look to modify Figure 27C, which describes *lowering* the potential of node 13, to include a capacitor that Kimura states will *raise* the potential of that node during the bootstrap operation. *See, e.g.*, Kimura ¶ [0286]; Ex. 2019, ¶ 74.

Petitioner also asserts that “Kimura itself contemplates that the capacitors can be employed” and that the “device’s output signal is improved when the capacitors are used.” Pet. at 34. Setting aside that, as discussed above, Kimura does not teach or suggest adding capacitors to Figure 27C, and that Petitioner seeks to add them in a manner inconsistent with Kimura’s description of the embodiments in which they are provided, Petitioner again overlooks the significant detriments that would be incurred by adding two capacitors to a stage circuit. As Patent

Owner's expert explains, capacitors take up significant circuit area, and this, along with the necessary connections to other circuit elements would have to be taken into account in designing a modified stage circuit. Ex. 2019, ¶ 75.

Petitioner's generalized assertions that these capacitors could be added to Figure 27C would not provide a POSITA sufficient motivation to incur these detriments. Petitioner's citations to Jeong, a different reference disclosing different circuits, with no further explanation, for the proposition that capacitors "improve robustness of, reduce[] variation of voltage applied to, and can stabilize operation of certain of a shift register's output transistors" fare no better. Pet. at 34. Petitioner provides no rationale for why these generalized considerations would motivate a POSITA to add two capacitors from different embodiments of Kimura to Figure 27C, let alone connect them within Figure 27C in the specific ways Petitioner suggests. As Patent Owner's expert explains, a POSITA would not have made these modifications, and Petitioner's arguments are nothing more than a hindsight-driven attempt to arrive at claims 7 and 21. Ex. 2019, ¶ 76.

5. Kimura Does Not Teach or Suggest Claim Elements [8-A]/[22-A] and [8-B]/[22-B].

Claim elements [8-A] and [22-A] require that the second driver include "a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node." Claim elements [8-B] and [22-B] similarly require that the second driver include "a seventh transistor

between the first node and a second power supply, the second power supply having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal.”

Petitioner concedes that “none of Figure 27C’s transistors are connected in the way the claim requires,” and proposes modifications to Figure 27C in order to arrive at these claims. Pet. at 35. Notably, unlike the modifications Petitioner must make for other challenged claims, Petitioner does not even attempt to depict how the modifications it proposes would be made, or explain how the resulting circuit would operate. Pet. at 35-36; Ex. 2019, ¶¶ 77-78. Petitioner suggests that Kimura states that these modifications “can be” made. Pet at 35-36. Petitioner cites to no disclosure of Kimura teaching that any of these modifications could be made to Figure 27C. *Id.* Petitioner also provides no rationale for making these modifications, instead suggesting that the needed changes would be a “design alternative.” *Id.*; *see also* Ex. 2019, ¶¶ 78-83.

Petitioner has failed to show that these modifications would result in an operable circuit, let alone identify a sufficient basis for a POSITA to have made these modifications with a reasonable expectation of success. Ex. 2019, ¶¶ 78-83. As one example, Petitioner asserts that “‘the first terminal of the transistor 102’ can be ‘connected to the wiring 113’ instead of wiring 115,” and that with this modification, transistor 102 is the claimed sixth transistor. Pet. at 35-36. But

Petitioner cites in support to a portion of Kimura describing Figure 7C, not Figure 27C. Kimura ¶ [0169] (“FIG. 7C illustrates a structure where the first terminal of the transistor 102 is connected to the wiring 113”); see also *id.* ¶ [0168] (listing only Figs. 1A, 6A-6F, and 7A-7 as structures in which “the first terminal of the transistor 102 can be connected to a wiring which is different from the wiring 115”). Notably, in the Figure 7C configuration, transistor 102 has its gate connected to wiring 114, not node 13 (the identified “second node”) as required by claims 8 and 22. Petitioner fails to explain this discrepancy, let alone point to any disclosure in Kimura that suggests that transistor 102 would still have its gate connected to the identified “second node” when its first terminal is connected to wiring 113 instead of wiring 115. Ex. 2019, ¶¶ 79-80.

Petitioner’s theory also requires, in addition to changing the connections of the transistors in Figure 27C in ways not supported by Kimura, adding an additional power supply line to Figure 27C. Petitioner provides no explanation whatsoever for this proposed modification. Pet. at 36. Petitioner simply suggests that “Kimura also teaches that the same device can be provided with multiple different power supply voltages.” *Id.* For claims 1 and 15 Petitioner identifies wiring 115 as the “first power supply.” Pet. at 18. For claims 8 and 22, Petitioner points to a different embodiment (Figure 30A) and suggests that wiring 115b in that embodiment would satisfy the “second power supply” limitation of those

claims. Petitioner does not explain what would be the “first power supply” in its proposed modification, explain what voltages would be provided by the identified “first” and “second” power supplies, or explain how the resulting modified circuit would function. Ex. 2019, ¶¶ 81-82.

For example, Petitioner suggests that Kimura describes (for other embodiments) that wiring 115 “can be provided with multiple different power supply voltages.” Pet. at 36. Petitioner points to Figure 30A, and asserts that for that embodiment Kimura teaches that “transistor 103 is connected to a different power supply with a different voltage (wiring 115B) than output transistor 201 (wiring 115D).” Pet. at 36. But with respect to Figure 30A, Kimura explains that “the voltage V_1 can be supplied to the wirings 115A to 115E.” Kimura ¶ [0299]. Ex. 2019, ¶¶ 81-82. Petitioner similarly fails to point to anything in Kimura that would teach or suggest connecting transistor 203 (the identified “seventh transistor”) to a “second power supply having a lower voltage than the first power supply,” as Petitioner suggests. Pet. at 36.

Finally, as with its other proposed modifications, Petitioner entirely ignores the significant downsides of adding multiple additional circuit elements and modified connections that would be incurred. Ex. 2019, ¶ 83. Indeed, Petitioner ignores Kimura’s teachings that reducing power sources results in improved reliability and yield, and reduces manufacturing costs. Kimura ¶ [0196]; Ex. 2019,

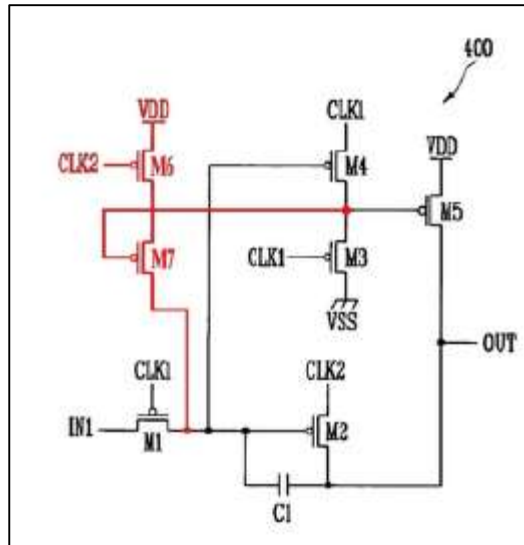
¶ 83. This further undercuts Petitioner’s unsupported theory that a POSITA would nevertheless seek to add a power supply to arrive at the requirements of claims 8 and 22.

B. Petitioner Has Not Shown That Shin in View of Sasaki or Shin in View of Sasaki and Jeong Renders Obvious Any Challenged Claim.

In a hindsight-driven attempt to arrive at the claims, Petitioner proposes to take a portion of a circuit taught by Sasaki and apply it to a specific node in a separate circuit taught by Shin. As Patent Owner’s expert explains, Petitioner’s arguments require making significant modifications that a POSITA would not have had a reason to make. Ex. 2019, ¶ 84. Petitioner additionally dismisses without explanation teachings in Shin that would obviate the only identified rationale Petitioner provides for modifying Shin. Moreover, Petitioner seeks to apply Sasaki’s circuitry to Shin in a manner that is inconsistent with Sasaki’s teachings. For all of these reasons a POSITA would not have been motivated to combine Shin and Sasaki and would not have had a reasonable expectation of success in so doing.

1. Shin Already Addresses the Purported Issue for Which Petitioner Proposes to Add Circuitry from Sasaki.

As shown below, Petitioner proposes to take two transistors from Sasaki (red) and apply them to Shin’s Figure 11:



Pet. at 50. All of Petitioner’s arguments relating to this Ground require combining these elements of Shin and Sasaki in the specific manner shown above. *See, e.g.*, Pet. at 53.

The only rationale Petitioner provides for adding these additional transistors (and connecting them in the specific manner, with the specific inputs shown above) is the unsupported assertion that a POSITA “would have recognized that Shin’s scan driving circuit is subject to a problem like that identified by Sasaki.” Pet. at 47. The purported problem involves reversal (i.e., switching from an intended level to an opposite level) of a particular node, for which Sasaki provides these additional circuit elements. But Petitioner’s hindsight-driven assertion is belied by Shin’s disclosures. Indeed, Shin already contains circuitry, namely capacitor C1, which Shin explains will mitigate concerns of reversal at the node to which Petitioner proposes to add these additional circuit elements. Ex. 2019, ¶ 86.

In particular, Sasaki teaches, as Petitioner acknowledges, that the reversal for which it is concerned may occur when a particular node is in a “floating state,” or in other words a state in which the node does not have a signal voltage supplied to it. Sasaki ¶ [0042]; Pet. at 46. However, Shin explains that when that the node to which Petitioner proposes to provide Sasaki’s “anti-reversal” circuit (i.e., the node connected to the gate of transistor M2) might be in a “floating state” Shin’s capacitor C1 maintains the intended voltage on that node. *See, e.g.*, Shin ¶ [0107] (“a voltage of the capacitor C1 remains unchanged, and thus the second transistor M2 continues to be turned-on”). Ex. 2019, ¶¶ 85-88.

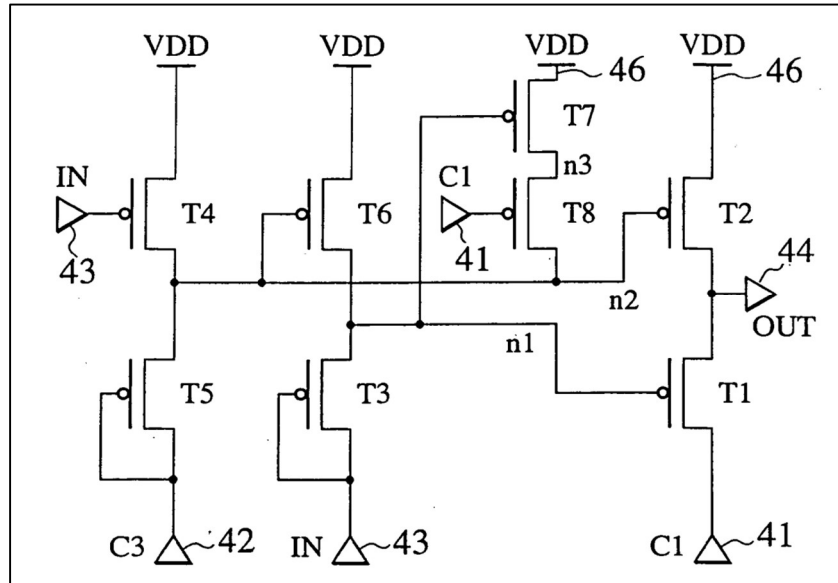
Petitioner tacitly acknowledges this hole in its rationale, yet provides only the bare, unsupported conclusion that “a POSITA would have recognized that this capacitor is not sufficient by itself to address Shin’s anti-reversal problem.” Pet. at 49. Petitioner’s bare assertion is contradicted by Shin’s disclosures, which teach that C1 is sufficient to maintain the voltage on the gate of M2. *Id.*; Ex. 2019, ¶ 88. As Patent Owner’s expert explains, there is nothing in Shin that states or would suggest to a POSITA that capacitor C1 is “not robust enough” to carry out the specific function for which Shin teaches it is provided, or that, in addition to capacitor C1, two additional transistors would be necessary, or even helpful, to perform that same function. Ex. 2019, ¶ 89.

Petitioner’s argument also fails to address the numerous reasons why a POSITA would *avoid* adding additional circuit elements. Adding additional elements to a circuit design will increase the footprint of the circuit, as prior art cited by Dr. Foty confirms. *See, e.g.*, Ex. 1006 at ¶ [0015], [0107] (describing “concern for increased circuit area”). Additionally, as the ’593 Patent explains, adding elements to a circuit may increase complexity, decrease stability, and lower process yield. Ex. 1001 at 9:12-26. Also, as Patent Owner’s expert explains, any added circuit elements will require input signals and associated timings for those signals. Ex. 2019, ¶¶ 89-91. The timings of existing circuit elements may also be impacted by the addition of new circuit elements. In addition, the driver that provides certain input signals may need to be modified to provide any additional or altered timings to enable the modified circuit to function properly. Each of these factors are among the specific benefits provided by the inventions of the ’593 Patent. Petitioner takes none of these concerns into account with its generalized assertions that a POSITA would mix and match teachings of various references simply because they are directed to stage circuits or that general concepts were “well known.”

2. Petitioner Applies Sasaki’s Circuitry Inconsistently with Sasaki’s Teachings.

Petitioner’s argument also relies on misapplying Sasaki’s teachings. Sasaki’s “anti-reversal” circuit is directed specifically at the potential reversal of Sasaki’s

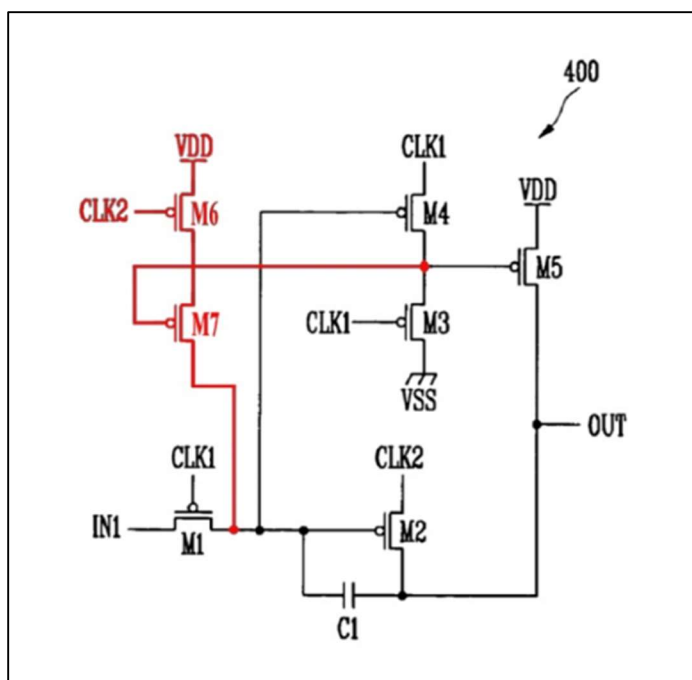
node n2 that Sasaki explains may be subject to reversal at a specific time in the operation of Sasaki's circuit. *See, e.g.,* Ex. 1003 at ¶ 388. Figure 4 of Sasaki depicts a stage circuit according to a first embodiment of Sasaki. Transistors T7 and T8 form the “anti-reversal” circuit.



Node n2 in Sasaki is connected to the gate of transistor T2, which controls whether the high voltage VDD is provided to the output terminal. Sasaki explains that reversal of the node n2 could result in the high voltage supply VDD being erroneously provided to the output terminal when a low value is intended. Ex. 1014 at ¶ [0048]. Sasaki explains that this can lead to unintended distortion of the output signal. Ex. 1014 at ¶ [0048] (describing that with no anti-reversal circuit, if node n2 is reversed “transistor T2 starts conducting and the high voltage VDD is supplied to the output terminal 44 through the second transistor T2[,]” resulting in a “distorted” output waveform.).

As Sasaki explains, it is reversal of this specific node at the identified point in the operation of the circuit at which Sasaki teaches that reversal would be particularly problematic. Sasaki repeatedly describes potential distortion when the intended output signal is low and VDD is erroneously provided to the output terminal. *See, e.g.*, Ex. 1014 ¶ [0051] (“As a result, the output signal OUT at the low level without distortion will be supplied to the output terminal 44.”); *see also id.* at ¶¶ [0055], [0059], [0061], [0064], [0066]. In contrast, Sasaki does not describe potential distortion when the intended output signal is high and CLK2 is erroneously provided (i.e., if reversal of Sasaki’s node n1 were to occur). Ex. 2019 ¶¶ 92-94.

The equivalent node to Sasaki’s node n2 in Shin is the node connected to the gate of transistor M5, because this node in Shin, like node n2 in Sasaki, controls whether the high voltage VDD is provided to the output terminal. Ex. 2019, ¶ 95. However, contrary to the teachings of Sasaki, Petitioner does not propose to add the “anti-reversal circuit” to this node in Shin. Ex. 2019, ¶ 96. Instead, Petitioner incorporates Sasaki’s “anti-reversal” circuit to the *opposite* node, i.e., the node at the gate of transistor M2 that controls whether the clock signal CLK2 is provided to the output terminal.



Pet. at 50; *see also id.* (“In operation, added transistors M6 and M7 operate to supply a high VDD signal to transistor M2’s gate to prevent the transistor from opening and inadvertently supplying a low CLK2 signal to OUT at a time when the circuit’s output is intended to be high”).

Notably, and as Patent Owner’s expert explains, the node to which Dr. Foty seeks to add Sasaki’s “anti-reversal” circuit does not have the same operational concerns that Sasaki describes in explaining why its “anti-reversal” circuit is provided. Ex. 2019, ¶¶ 96-97. Sasaki describes the purpose of the “anti-reversal” circuit as being to prevent reversal of the node that controls whether the high voltage VDD is provided to the output, because reversal of that node could lead to the high voltage VDD distorting the intended low value output. *See, e.g.,* RX-0095 ¶ [0051]. In contrast, the node in Shin to which Petitioner applies Sasaki’s “anti-

reversal” circuit does not control whether VDD is provided to the output terminal. Petitioner’s argument thus rests entirely on a misapplication of Sasaki’s teachings.

3. Shin in View of Sasaki and Further in View of Jeong Does Not Render Obvious Claim Elements [7-D] and [21-D].

Claim elements [7-D] and [21-D] require that the “outputting unit” include “a second capacitor between the first node and the first power supply.” Petitioner acknowledges that its proposed combination of Shin and Sasaki does not include the second capacitor required by claim elements [7-D] and [21-D], and proposes to further combine Shin and Sasaki with Jeong. Pet. at 74.

The only rationale Petitioner provides as to why a POSITA would seek to add an additional circuit element to the composite circuit of Shin as modified by Petitioner to include Sasaki’s “anti-reversal” circuit is an unsupported reference to potential “electromagnetic interference or other perturbances,” and a conclusory, unsupported assertion that “[a] POSITA would have understood that this problem would be eliminated by including another capacitor.” Pet. at 77.

Contrary to Petitioner’s unsupported assertions, nothing in Shin or Sasaki suggests any operational issue with Shin or Sasaki’s circuitry that would motivate adding a capacitor. Ex. 2019, ¶¶ 99-103. Indeed, while Petitioner acknowledges that Shin already has a capacitor C1, and suggests this means a POSITA would have naturally added another capacitor, in reality this demonstrates that Shin was

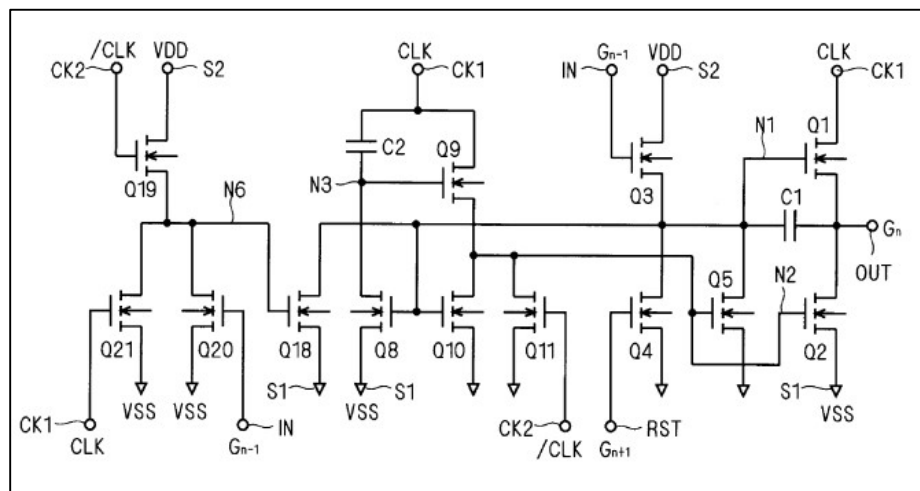
familiar with the generalized concerns Petitioner points to, yet intentionally added a capacitor (C1) where it was needed, and did not add a capacitor where it was not. Ex. 2019, ¶ 101. Moreover, Petitioner's arguments that Shin's inclusion of capacitor C1 are inconsistent with its arguments that capacitor C1 is insufficient for its intended purpose. *Id.* Petitioner's citation to Jeong's teachings relating to different circuits similarly do not manufacture a rationale sufficient to motivate a POSITA to add an additional capacitor to a scan driver stage circuit.

Petitioner and its expert additionally overlook the detriments to adding additional circuit elements to a scan driver stage circuit, detriments with which a POSITA would have been well aware. Ex. 2019, ¶ 103. For example, a different reference relied upon by Petitioner describes that capacitors detrimentally add significant circuit area. *See, e.g.,* Tobita ¶ [0015]. A POSITA would have been familiar with such detriments and would not have sought to add additional circuit elements absent a clear and specific reason to do so. Petitioner provides no such reason. The generalized concerns Petitioner suggests could possibly arise would not overcome the known issues and disadvantages associated with adding circuit elements like capacitors to scan driver stage circuits. Ex. 2019, ¶ 103.

C. Petitioner Has Not Shown That Tobita or Tobita in View of Jeong Renders Obvious Any Challenged Claim.

Tobita is directed to a scan driver shift register for a liquid crystal display. Tobita ¶ [0004]. Tobita describes a problem with conventional shift registers

comprised of amorphous silicon TFTs, in which degraded driving capability occurred because “a-Si TFT tends to have its threshold voltage shifted in the positive direction when the gate electrode is continuously positive-biased.” Tobita ¶ [0010]. Tobita describes that other approaches to addressing this issue required additional capacitive elements with “large capacitance” which led to “increases [in] the circuit area.” Tobita ¶ [0015]. Accordingly Tobita describes an approach intended to “control an increase in circuit area of a shift register while preventing malfunctions” Tobita ¶ [0016]. Ex. 2019, ¶¶ 104-105.

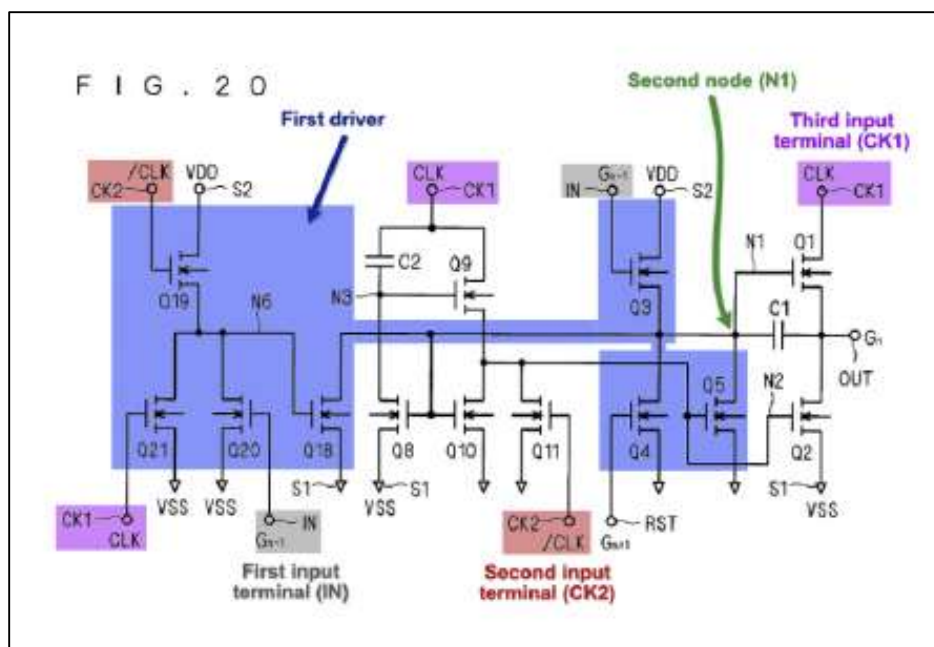


display's backlight. Tobita ¶ [0170]. OLED displays do not have backlights, and thus are not susceptible to backlight leakage current, as a POSITA would have understood. Ex. 2019, ¶ 106. Petitioner and its expert do not explain why a POSITA would nevertheless look to Tobita for implementing an OLED scan driver stage circuit.

Additionally, like the embodiment of Kimura Petitioner relies upon, Tobita's eighth embodiment includes many more transistors and input signals than the embodiments of the '593 Patent and is accordingly more similar to the conventional stage circuits distinguished by the '593 Patent. *Id.* Petitioner again fails to explain why a POSITA would nevertheless look to such an embodiment for application in an OLED display.

1. Tobita Does Not Teach or Suggest Claim Element [1-B]/[15-E].

Claim limitations [1-B] and [15-E] require a “first driver” that “control[s] the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal.” As shown below, Petitioner identifies portions of Tobita's Figure 20 encompassing seven different transistors (blue) as purportedly satisfying this limitation. Pet. at 84.



As noted above, Tobita explains that its eighth embodiment is directed to a particular issue with optical leakage current that may arise at a specific point in time in the operation Tobita’s seventh embodiment. Tobita ¶¶ [0170], [0171]; Ex. 2019, ¶ 109. Tobita explains that this optical leakage may occur when Q3 is not diode-connected, but instead has its drain connected to VDD, as it is in both the seventh and eighth embodiments. Tobita ¶¶ [0170], [0171], Figs. 19, 20. As Tobita describes, in this configuration, when node N1 is in a high impedance state, optical leakage current may flow from VDD to node N1 “under the influence of external light incident into the display or backlit light of a display panel” Tobita ¶ [0170]. Tobita thus provides its eighth embodiment, with its additional four transistors Q18, Q19, Q20, and Q21, to address this specific concern relating to optical leakage current. *Id*; see also Ex. 2019, ¶ 109.

Tobita is clear that in Figure 20, transistors Q19, Q20, and Q21 are provided to determine the voltage of node N6, not node N1 (the identified second node). Tobita ¶¶ [0172]–[0178]; *see also* Ex. 2019, ¶¶ 109-111. In particular, Tobita explains that transistors Q19 and Q20 operate as an “inverter circuit,” with node N6 “serving as the output node of the inverter circuit.” Tobita ¶ [0174]. Tobita also explains that Q21 operates to keep this output node “at the L level” at a particular period of operation of the stage circuit. Tobita ¶ [0177].

Accordingly, Q19, Q20, and Q21 (which Petitioner has identified as part of the “first driver”) do not control the voltage of the identified second node (N1) as this claim element requires, because they instead control the voltage of a different node, N6. Ex. 2019, ¶¶ 110-111. Indeed, the voltage on node N6 is not passed to the node N1. Instead the voltage on node N6 is passed to the gate of another transistor, Q18, to turn that transistor ON and OFF. Transistors Q19, Q20, and Q21 may thus control the voltage of node N6 in accordance with the signals of the identified input terminals (CK1, CK2, and IN), but they do not control the voltage of node N1 in accordance with the signals of those input terminals. Ex. 2019, ¶ 111.

Petitioner tacitly admits that these transistors do not control the voltage of node N1 as required by the claims in acknowledging that “certain of Tobita’s transistors do not directly provide output to node N1.” Pet. at 85. Petitioner

suggests that despite this, the identified “first driver” meets this limitation based on a mischaracterization of Patent Owner’s arguments in the related ITC Proceeding. Pet. at 85. In the ITC, Patent Owner noted that the first capacitor C1 “charges the voltage corresponding to turn on and off of the fifth transistor.” Ex. 1009, 22-23, quoting ’593 Patent, 5:56-59.

But the “first driver” must still “control[]” the voltage of the second node “in accordance with signals of the first input terminal, the second input terminal, and the third input terminal.” Ex. 2019, ¶ 107. And as shown above, transistors Q19-Q21, which Petitioner places within the identified “first driver” may control the voltage of node N6 “in accordance with” the signals of the identified “second” and “third” input terminals, but they do not control the voltage of the identified second node (N1) in accordance with those signals. Ex. 2019, ¶ 111.

2. Tobita In View of Jeong Does Not Teach or Suggest Claim Elements [7-D]/[21-D].

Claim elements [7-D]/[21-D] require that the “outputting unit” includes “a second capacitor between the first node and the first power supply.” Petitioner admits that the identified “outputting unit” in Tobita does not include the claimed second capacitor. Pet. at 95. Petitioner thus proposes to add an additional capacitor from a different reference, Jeong, to arrive at this claim element.

Notably, Petitioner does not identify any operational issues with the embodiment of Tobita on which it relies, instead making unsupported assertions

that Tobita's circuit "could experience" unintended "voltage variation." Pet. at 97; *see also* Ex. 2019, ¶ 113. As Patent Owner's expert explains, a POSITA would not simply assume that there could possibly be such issues, and any generic concerns would not motivate a POSITA to add a capacitor to Tobita's circuit. Ex. 2019, ¶ 113. A given circuit will be specifically designed for its intended purpose, and a POSITA would not haphazardly add circuit elements without clear objectives or benefits. *Id.*

Indeed, Tobita explains that capacitors add significant circuit area, Tobita ¶ [0015], and Tobita is directed to reducing circuit area where possible. *Id.* Neither the generalized and unsupported concerns Petitioner identifies, nor Jeong's teachings relating to a capacitor in a different circuit would provide sufficient motivation for a POSITA to add an additional capacitor to Tobita's circuit. Ex. 2019, ¶¶ 113-114. Moreover, Tobita includes a capacitor, C1, in the identified "outputting unit," yet does not include the additional capacitor Petitioner proposes to add. Tobita, Fig. 20. Thus, Tobita was familiar with the generalized concerns Petitioner points to, yet intentionally added a capacitor (C1) where it was needed, and did not add a capacitor where it was not. This further confirms that the generic considerations Petitioner advances (of which Tobita's author would have been similarly aware) would not motivate a POSITA to add a capacitor to Tobita as

Petitioner suggests, let alone connect it in the specific way Petitioner does, which is necessary to arrive at the claims. Ex. 2019, ¶ 114.

VI. Conclusion

For all of the foregoing reasons, Patent Owner respectfully submits that institution should be denied.

Date: June 21, 2024

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), I certify that the present paper contains 11,516 words based on the word count indicated by the word-processing program used to generate the paper and excluding those portions exempted by 37 C.F.R. §§ 42.24(a) and (b).

Date: June 21, 2024

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6, I hereby certify that the foregoing Patent Owner's Preliminary Response and accompanying exhibits were served by electronic mail on the following counsel of record for petitioner:

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