



UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MIANYANG BOE OPTOELECTRONICS TECHNOLOGY CO., LTD.;
WUHAN CHINA STAR OPTOELECTRONICS SEMICONDUCTOR DISPLAY
TECHNOLOGY CO., LTD.; TIANMA MICROELECTRONICS CO., LTD.;
AND VISIONOX TECHNOLOGY, INC.,
Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.
Patent Owner.

Case IPR2024-00620
U.S. Patent No. 9,330,593

PATENT OWNER'S RESPONSE

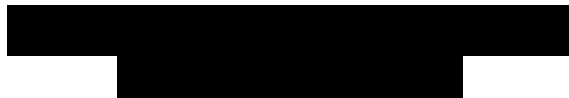




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PATENT OWNER'S EXHIBIT LIST

Exhibit	Description
Ex. 2001	Order Amending Schedule, Inv. No. 337-TA-1351
Ex. 2002	Notice of Prior Art, Inv. No. 337-TA-1351
Ex. 2003	Westlaw Company Investigator Report for Mianyang BOE
Ex. 2004	Assignment for U.S. Patent Application No. 15/031,174
Ex. 2005	Assignment for U.S. Patent Application No. 15/031,174
Ex. 2006	Assignment for U.S. Patent Application No. 16/097,538
Ex. 2007	Assignment for U.S. Patent Application No. 15/562,853
Ex. 2008	Assignment for U.S. Patent Application No. 16/968,978
Ex. 2009	Assignment for U.S. Patent Application No. 16/622,918
Ex. 2010	Westlaw Company Investigator Report for TCL Technology Group
Ex. 2011	Westlaw Company Investigator Report for China Star Wuhan
Ex. 2012	May 18, 2017 References Cited by Examiner for U.S. Patent Application No. 15/031,174
Ex. 2013	March 12, 2019 References Cited by Examiner for U.S. Patent Application No. 15/562,853
Ex. 2014	February 2, 2023 References Cited by Examiner for U.S. Patent Application No. 16/968,978
Ex. 2015	May 4, 2022 References Cited by Examiner for U.S. Patent Application No. 16/622,918
Ex. 2016	May 14, 2020 References Cited by Examiner for U.S. Patent Application No. 16/097,538
Ex. 2017	U.S. Patent No. 9,236,377

Exhibit	Description
Ex. 2018	Claim Construction Order, Inv. No. 337-TA-1351
Ex. 2019	Declaration of Dr. Andrew Wolfe, Ph.D. (in support of Patent Owner Preliminary Response)
Ex. 2020	Notice of Allowance for U.S. Patent No. 9,330,593
Ex. 2021	Curriculum Vitae of Andrew Wolfe, Ph.D.
Ex. 2022	Declaration of Derek Andros
Ex. 2023	Declaration of Jared Frisch
Ex. 2024	Teardown Photos of Samsung Galaxy S22Ultra Product
Ex. 2025	Teardown Photos of MobileSentry Product
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Ex. 2039	Teardown Photos of Wholesale Gadget Parts Product
Ex. 2040	Teardown Photos of Parts4LCD Product
Ex. 2041	Teardown Photos of DFW Cellphone and Parts Product
Ex. 2042	Declaration of Aris Silzars, Ph.D.
Ex. 2043	Declaration of Adam Fontecchio, Ph.D.
Ex. 2044	[REDACTED] – [REDACTED] Declaration of Kwangsae Lee
Ex. 2045	<i>Samsung Display Co., Ltd. v. BOE Tech. Co., Ltd. et al.</i> , Case No. 2-23-cv-00309, Compl. (E.D. Tex. June 26, 2023).
Ex. 2046	Mengtor AMOLED Display Claim Chart
Ex. 2047	[REDACTED] – [REDACTED] Declaration of Hwan-Soo Jang
Ex. 2048	[REDACTED] – [REDACTED] [REDACTED]
Ex. 2049	Jason Gutierrez, <i>CES is over – where are the bezel-less phones?</i> , Android Authority (2013)
Ex. 2050	Jin Huh, <i>A New Small Sized Integrated Scan & Emission Driver for Compact AMOLED Displays</i> , SID 2012 Digest (2012)
Ex. 2051	United States Patent Application Publication No. 2013/0169609
Ex. 2052	United States Patent No. 9,620,061
Ex. 2053	United States Patent No. 11,227,549
Ex. 2054	Suzanne Kantra, <i>Review of the Samsung Galaxy S4</i> , Techlicious (2013)
Ex. 2055	Tony Fletcher, <i>Samsung Galaxy S4 announced and here’s the photos</i> ,



Exhibit	Description
	<i>specs and videos</i> , WireFresh (2013)
Ex. 2056	Chuong Nguyen, <i>Samsung Galaxy S4 Review</i> , GottaBeMobile (2013)
Ex. 2057	[REDACTED] – [REDACTED] Samsung Galaxy S22Ultra AMOLED Display Claim Chart
Ex. 2058	[REDACTED] – [REDACTED] [REDACTED]
Ex. 2059	[REDACTED] – [REDACTED] Declaration of Dr. Andrew Wolfe, Ph.D. in Support of Patent Owner Response
Ex. 2060	Transcript of December 5, 2024 Deposition of Daniel Foty, Ph.D. (Rough) (redacted)
Ex. 2061	Transcript of June 24, 2024 Deposition of Daniel Foty, Ph.D. (redacted)



I. Introduction

Petitioner advances five different grounds based on five different references and alleges only obviousness of the challenged claims. Only one of these grounds, Ground 1 based on U.S. Patent Publication No. 2011/0057190A1 (Ex. 1004, “Kimura”), purports to challenge each of the challenged claims. As the Board noted in the institution decision (“ID”), Petitioner picks and chooses from various embodiments and relies upon teachings of Kimura that contradict one another.

In particular, while Petitioner’s Ground 1 is based on the circuit of Kimura’s Figure 27C, Petitioner purports to rely on a timing diagram directed to different embodiment of Kimura, which does not apply to the Figure 27 circuit and is inconsistent with Kimura’s discussion of the operation the Figure 27C circuit. Indeed, Petitioner’s declarant, Dr. Foty, admitted in deposition that this timing diagram does not reflect the operation of the Fig. 27C circuit. Ex. 2060, 25:10-15. The Petition relies on Dr. Foty’s mixing and matching of various aspects of different Kimura embodiments, when Dr. Foty further admits he is unaware of [or is unable to identify] any supporting disclosure or teaching from Kimura but instead “assumes” different embodiments are compatible simply because they are all directed, at a high-level, to stage circuits. *See, e.g., id.*, 32:3-33:17. Petitioner’s flawed analysis is fatal to its theories as to Kimura.



Petitioner's other grounds are similarly flawed. As the Board recognized in the ID, Petitioner's proposed combination of Shin and Sasaki both ignores the express teachings of Shin and manufactures a purported problem with its circuitry so that it can implement a "solution" from Sasaki that is both unnecessary to the circuit of Shin and inconsistent with Sasaki's own teachings.

Additionally, Petitioner's theories regarding Tobita are fundamentally flawed. The challenged claims require "a first driver to control the voltage of the second node in accordance with signals of" three different input terminals, including "the third input terminal." As Dr. Foty confirmed in deposition, however, Petitioner does not (and cannot) argue that the alleged first driver in Tobita actually controls the voltage of the second node in accordance with the signal of the third input terminal. Ex. 2060, 71:10-15. Petitioner and Dr. Foty instead can argue only that the alleged first driver turns off a transistor, and that this prevents a different signal from being provided to the second node. *Id.* But as Dr. Foty admitted and Dr. Wolfe confirms, turning off this transistor does not change or impact the voltage on the second node. *Id.*; Ex. 2059, ¶115. The voltage on the second node is not controlled in accordance with the third input signal.

Thus, Petitioner's Tobita arguments do not rely on a theory that some other circuit element may have an impact on the voltage of the claimed second node in addition to first driver, which was the issue addressed during claim construction at

[REDACTED]

the ITC and referenced by the Board in its ID. Yet the claim limitation was never interpreted by any party at the ITC to suggest that the first driver itself is not required to control the voltage of the second node in accordance with each of the signals of the first, second, and third input terminals, nor would such an interpretation accord with the claim language and intrinsic evidence. Significantly, as Dr. Foty conceded, under his interpretation—on which the Petition relies—the operation of any circuit element within Tobita’s circuit would constitute “control in accordance with” the circuit’s input signals. Ex. 2060, 72:6-73:3. Petitioner’s theories as to Tobita are flawed.

Finally, robust evidence of objective indicia reinforces non-obviousness and further refutes Petitioner’s theories. Before the ’593 Patent’s inventions there was significant demand for AMOLED displays for mobile devices and a need for reduction in the bezel space surrounding the active display area. The ’593 Patent addressed these problems, allowing for significant reductions in the bezel, and satisfying a long-felt need. The inventions have also been widely copied, including by other display manufacturers that tried but failed to develop their own scan driver stage circuits for AMOLED displays.

II. Level of Ordinary Skill in the Art

Patent Owner proposes that POSITAs for the ’593 Patent would have had a relevant degree in Electrical Engineering, Computer Engineering, Materials

[REDACTED]

Science, Physics, or the like, and 2-3 years of experience in active-matrix display design and electroluminescence.¹ Ex. 2059, ¶39. Patent Owner notes that, in the related ITC Proceeding, the ALJ agreed with and adopted Patent Owner’s proposal that experience with active-matrix display circuitry and electroluminescence is required. Ex. 2018, 12 (explaining, among other things, the ’593 Patent is “directed to active matrix display technologies for organic light-emitting diode displays” and “[i]t is therefore reasonable to expect one of skill to have specific experience with active-matrix display circuitry and electroluminescence”). Before the ITC, the amount of that experience was not specified, but Dr. Wolfe explains it would be 2-3 years.

Petitioner has proposed POSITAs would have had “a Bachelor’s degree in electrical engineering or similar discipline, along with 2-3 years of circuit design/analysis experience.” Pet., 5. For purposes of the ID, the Board adopted Petitioner’s definition. ID, 10.

Patent Owner respectfully submits that Petitioner’s definition is incorrect, as it entails only general “circuit design” experience with no experience in active-

¹ The Board noted that Patent Owner’s proposed definition in its preliminary response does not quantify the amount of experience required. ID at 10. Patent Owner has clarified its proposal here to require 2-3 years of experience.

[REDACTED]

matrix display design and electroluminescence, the subject matter of the '593 Patent. The '593 Patent is directed to active-matrix organic light-emitting diode (AMOLED) displays and solving problems specific to those displays, including improving scan-on time and reducing the physical footprint of the scan circuitry required to program each row of pixels. Ex. 2059, ¶41. Important aspects and considerations of the stage circuit design are unique to the context of active-matrix display design and to electroluminescent displays. *Id.* For example, the signal timings generated by the scan driver and provided to the pixel circuits are specialized to AMOLED displays. *Id.* While the Board noted that claim 1 “does not include any limitations directed to ‘active matrix displays’ or any other particular type of display,” ID, 10, other claims include limitations directed to aspects of active-matrix displays and specifically recite OLED displays. For example, claim 15 recites “[a]n organic light emitting display” comprising “a scan driver for supplying scan signals to the pixels through the scan lines,” which reflects an active-matrix display in which each pixel circuit is provided a scan signal through the scan line. Ex. 2059, ¶41. Moreover, claim 15 additionally recites “an organic light emitting display,” as well as other signal lines connected to the pixel circuit. *Id.* Consistent with these claims, the “Background” of the '593 Patent explains that “[a] typical light emitting display supplies currents corresponding to data signals to OLEDs *using transistors formed in pixels so that the OLEDs may*


emit light,” ’593 Patent, 1:30-33 (emphasis added), which is describing active-matrix display technology, and the “Field” specifically refers to “a stage circuit and an organic light emitting display using the same,” id., 1:17-18. See also id., 9:24-26 (“[S]tages according to embodiments, and an organic light emitting display using the same, improve stability and reduce complexity.”); id., Title (“Stage Circuit and Organic Light Emitting Display Using the Same”).

Petitioner’s definition does not accurately reflect the experience of those working in the field of the ’593 Patent—Petitioner’s definition does not include *any* experience in display design, much less OLED display design. Ex. 2059, ¶42. Indeed, Petitioner’s misreading of the art appears to result from a lack of appreciation of display-related technology. For example, Kimura’s disclosures relating to the GOUT and SOUT signals are specific to the display context, and make clear that these signals serve different functions within the scan driver and pixel array. *See, e.g.,* Kimura ¶¶[0304]-[0305]. Petitioner’s misapplication of these teachings underscores how a proper understanding of active matrix and electroluminescent displays is critical to understand the content of the prior art. *See, e.g.,* Section IV.A.4, below.

Because Petitioner’s definition fails to include any experience with active-matrix display design and electroluminescence, let alone any display design experience, it fails to reflect the background and knowledge ofPOSITAs. Ex. 2059,

[REDACTED]

¶42. Petitioner’s expert, Dr. Foty, does not qualify as a person of ordinary skill in the art under the proper definition and accordingly lacks qualification to opine on matters requiring the perspective of a person of ordinary skill.

III. Claim Construction

For purposes of this proceeding, Patent Owner does not believe that any specialized constructions are necessary. Petitioner fails to show unpatentability under any claim interpretation.

As the Board noted in its ID, the ALJ in the related ITC Proceeding, Investigation No. 337-TA-1351, issued a claim construction order construing certain claim terms of the ’593 Patent. Ex. 2018, 15-37. The Board found, for purposes of the ID, that consistent with the construction for limitation 1[b]/15[e] in the ITC, controlling the voltage of the second node does not require the voltage of the second node to be determined by the first driver alone. DI, 10-12. This limitation is further addressed in Section IV.C, *infra*, with respect to Petitioner’s Grounds relying on the Tobita reference.

IV. Petitioner Has Not Established a *Prima Facie* Case of Obviousness as to Any Challenged Claim.

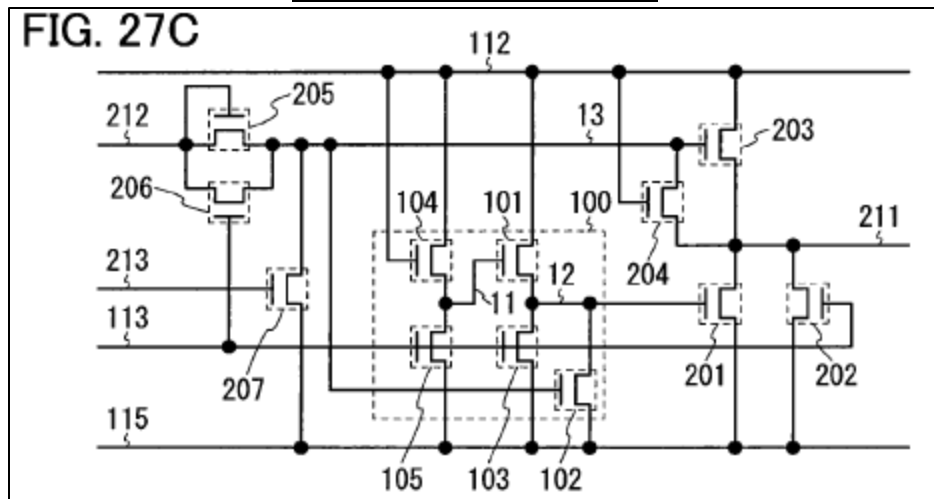
A. Kimura Does Not Render Obvious Any Challenged Claim.

As the Board stated, “Petitioner’s analysis includes inconsistencies that are not sufficiently explained.” DI, 25. Among other issues, Petitioner cites to Kimura’s description of different circuits from different embodiments, and alleges

[REDACTED]

that they could be connected in similar ways, yet provides no explanation as to the specific arrangement contemplated nor how those components would operate. Dr. Foty conceded that Kimura provides no teaching to suggest combining these elements in the way Petitioner suggests, and that his opinions were based on an assumption. Ex. 2060, 30:11-35:20 (“Q. Where does Kimura say that it doesn’t change the inputs [from] the Figure 21A circuit to the 27C circuit?...A. I don’t believe he may say that explicitly but it is basically the same circuit...”)(objections omitted); *see also, e.g., id.* 35:22-36:17 (acknowledging that as between the Figure 21A circuit and Figure 27C circuit there are additional inputs and transistors). Additionally, and as the Board noted in the ID, Petitioner relies upon a timing diagram that is inconsistent with other teachings of Kimura that Petitioner also purports to rely upon. As Dr. Wolfe further explains, these inconsistencies undermine and are fatal to Petitioner’s arguments. ID, 25-26; Ex. 2059, ¶48.

Petitioner’s arguments regarding Kimura all begin with Figure 27C, shown below.



As Patent Owner previously explained, Petitioner provides no reason why POSITAs would choose to start with this design as opposed to any other. As Petitioner acknowledges, “Kimura includes numerous embodiments.” Pet., 10. Kimura further describes multiple circuit variations within many of its embodiments. For example, Figures 27A-C are described as depicting circuit diagrams of Kimura’s second embodiment, but each includes different transistors connected in different ways. *See, e.g.*, Kimura, ¶¶[0283]-[0287] (describing the different transistors and corresponding connections in the circuits of Figs. 27A, 27B, and 27C).

Petitioner’s arguments require the specific configuration and connections shown in Figure 27C to arrive at the challenged claims. Pet., 10. However, nothing in Kimura teaches or suggests any particular advantages of the specific configuration of transistors and connections depicted in Figure 27C as opposed to any other embodiment. Kimura simply lists numerous potential alternative



configurations of its embodiments. *See, e.g.*, Kimura, ¶[0289] (“In the structures illustrated in...FIGS. 27A to 27C...the second terminal of the transistor 207 can be connected to a wiring that is different from the node 13.... Alternatively, the first terminal of the transistor 207 can be connected to a wiring which is different from the wiring 115....”); *see also, e.g.*, Kimura, ¶¶[0287], [0291], [0297] (listing other possible alternatives). Kimura provides no explanation as to why the permutation of options Kimura lists were implemented as shown in Figure 27C, let alone provide any reason as to why that particular configuration is advantageous. Ex. 2059, ¶¶46-48.

Petitioner concedes as much, acknowledging that “Figure 27C does not itself mention all of the depicted transistors, inputs, and outputs,” and thus presenting its arguments “in terms of obviousness.” Pet., 15. But Petitioner points to nothing to explain why it would have been obvious for POSITAs to look to the specific configuration of Fig. 27C. As Patent Owner’s expert explains, POSITAs would have had no reason to do so. Ex. 2059, ¶¶46-48. Additionally, and as discussed below, while Petitioner asserts that POSITAs would have looked “elsewhere” in Kimura for description of elements not discussed in the context of Figure 27C, Pet., 15, Kimura’s description of Figure 27C is inconsistent with its description of certain of its other Figures and embodiments, including with respect to the timing diagram upon which Petitioner and its expert rely. Petitioner’s declarant, Dr. Foty,


confirmed that there is no express teaching in Kimura to use the Figure 21B timings with the Figure 27C circuit, and that Figure 21B's timings would not work absent additional changes that are also not disclosed in Kimura. Ex. 2060, 30:11-35:20; 35:22-36:17; *see also* Ex. 2059, ¶¶50-53.

Additionally, Kimura's Figure 27C circuit more closely resembles the prior art stage circuits upon which the '593 Patent's inventions improved. The '593 Patent teaches that its inventions provide a reduction of necessary transistors and signal lines, which led to improvements in manufacturability, efficiency, and speed. *See, e.g.*, '593 Patent, 9:12-26. The '593 Patent specifically criticizes prior art stage circuits having "at least ten transistors" as well as prior art stage circuits requiring additional input signals beyond "first and second clock signals," and a start pulse or output of a prior stage. *Id.* As shown below, Kimura's Figure 27C includes 12 transistors (elements 101, 102, 103, 104, 105, 201, 202, 203, 204, 205, 206, and 207) and requires at least 4 input signals (elements 112, 212, 213, 113).

Accordingly, as Patent Owner's expert explains, POSITAs would not have looked to Figure 27C as Petitioner contends, and in any event would not have had made the modifications Petitioner asserts, nor had a reasonable expectation of success in implementing Figure 27C according to Petitioner's theories. Ex. 2059, ¶48.



1. Petitioner's Application of Kimura Is Flawed.

While Petitioner states that its arguments are based on Kimura's Figure 27C circuit, Pet., 10, it points to portions of Kimura directed to different circuits and configurations in an attempt to arrive at the requirements of the challenged claims. Notably, as the Board observed, Petitioner relies on a timing diagram that is *inconsistent* with the Figure 27C circuit, including disclosures relating to transistor 204 that Petitioner relies upon as purportedly teaching the very point of novelty that led to the allowance of the claims. ID, 25-27.

Claim elements [1-A] and [15-D] are directed to “an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node.”

Petitioner points to Figure 27C for these limitations, but its citations to Kimura to show how the identified elements in Figure 27C purportedly satisfy the requirements of these limitations refer to *different* circuits in Kimura. *See, e.g.*, Pet., 18 (citing discussions related to Figs. 18A, 19A, 19B, *e.g.*, Kimura ¶¶[0253]-[0256]). The Board pointed out this additional discrepancy in Petitioner's theories. ID, 25 (noting that Petitioner and Dr. Foty do “not explain sufficiently why a different arrangement of such components would yield the same results.”). Indeed,

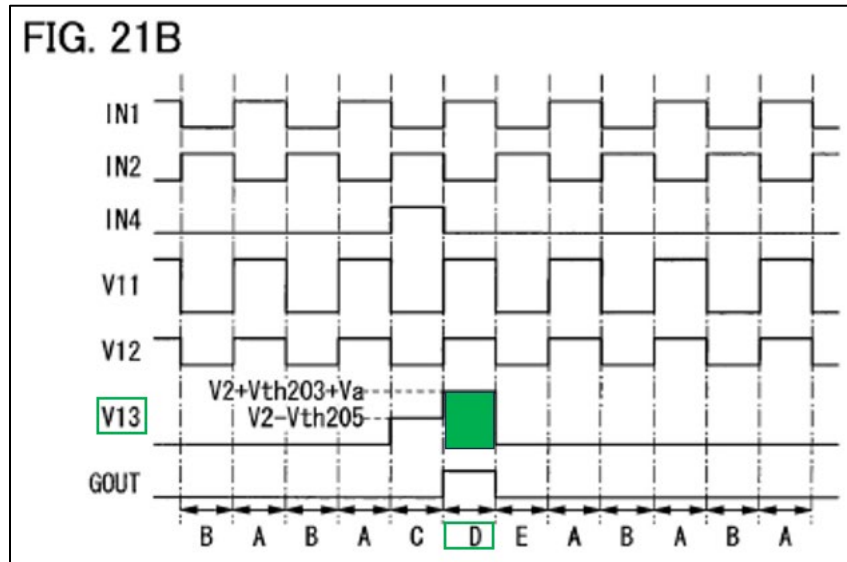
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beyond the bare assertion that POSITAs would have understood that components of Figure 27C not discussed with respect to Figure 27C would be “connected” and “function” in the same way “discussed elsewhere,” Pet., 15, Petitioner provides no explanation as to why POSITAs would allegedly look to these different Figures and circuits to understand the operation of Figure 27C’s circuit. Ex. 2059, ¶¶46-48.

As previously noted, Petitioner also relies on the timing diagram in Figure 21B for claim elements [1-A] and [15-D]. Pet., 19. Petitioner acknowledges that this timing diagram “is not specific to the device of Figure 27C,” but asserts that POSITAs would have understood that because Figure 27C “includes the same input and output lines and many of the same transistors as Kimura’s other circuits,” and that the Figure 27C circuit “would (or at least obviously could) be supplied with input signals in the same manner and with the same timing.” Pet., 19.

However, as the Board observes, ID, 25-26, Kimura’s description of Figure 27C demonstrates that it is *not* compatible with the timings shown in Figure 21B. Ex. 2059, ¶52. Petitioner’s declarant, Dr. Foty, admitted at deposition that the Figure 21B timings are provided with respect to Figure 21A, and that the Figure 27C circuit includes additional inputs and transistors not accounted for in the Figure 21B timings. Ex. 2060, 30:11-35:20; 35:22-36:17. It is thus unsurprising that while Kimura explains that for the circuit shown in Figure 27C, “in a period D, the potential of the node 13 can be *lowered*,” Kimura ¶[0286] (emphasis added),

during period D shown in (annotated) Figure 21B below, the potential of node 13 (V13) is depicted to be at its *highest* level:



Petitioner and its expert do not address this discrepancy, or attempt to explain why POSITAs would nevertheless understand Figure 21B’s timings to be compatible with the Figure 27C circuit. They are not. Ex. 2059, ¶¶50-53. This discrepancy between the timing diagram Petitioner asserts would apply to Figure 27C’s circuit and Kimura’s description of the operation of Figure 27C’s circuit would not allow POSITAs to draw conclusions as to whether the Figure 27C circuit satisfies the requirements of the claims. Ex. 2059, ¶¶52-53.

2. Kimura Does Not Teach or Suggest Claim Elements [1-D]/[15-G].

Claim elements [1-D] and [15-G] require that “the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver.”



Petitioner must rely on transistor 204 as the claimed transistor in the “first driver,” because it is the only transistor in Figure 27C that, according to Petitioner, has its “on/off operation” “directly control[led]” by the “signal of the third input terminal,” as these claim elements require. Pet., 24. However, the “first driver” must also control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal,” as set forth in claim elements [1-B]/[15-E]. With respect to how the identified “first driver” allegedly “control[s] the voltage of the second node in accordance with” the signal of the third input terminal, Petitioner also relies on transistor 204.

Specifically, Petitioner points to Kimura’s description that transistor 204 has its gate “connected to wiring 112” (the identified third input terminal), and Petitioner alleges that transistor 204 thus “controls” the voltage node 13 by lowering its potential, citing to the portion of Kimura previously discussed (Kimura ¶[0286]). But Kimura provides no further explanation of this lowering, or how it occurs, and Petitioner has identified nothing to suggest that this lowering would meet the requirement of the claims that the first driver “control[s] the voltage of the second node in accordance with” the signal of the third input terminal. Ex. 2059, ¶55. For example, Petitioner does not suggest that transistor 204 “controls” the voltage of node 13 in accordance with the signal of the identified third input terminal such that transistor 203 (which has its gate

[REDACTED]

connected to node 13) turns on or off. *Id.* Moreover, the timing diagram Petitioner points to does not reflect a lowered potential of node 13 at all, it reflects a *raised* potential, as explained above. Ex. 2059, ¶56.

For at least these reasons, as Dr. Wolfe explains, no reliable conclusion can be drawn, and POSITAs would not have understood transistor 204 to meet this claim element. Ex. 2059, ¶¶55-57. This is of particular significance because claim element [1-D] was identified by the Examiner as a point of novelty in allowing the claims. Ex. 2020, 7.

Accordingly, POSITAs would not have looked to Figure 27C and, absent timings, would not have been motivated to make the modifications Petitioner asserts, and would not have had a reasonable expectation of success in implementing Figure 27C's circuit. Ex. 2059, ¶57.

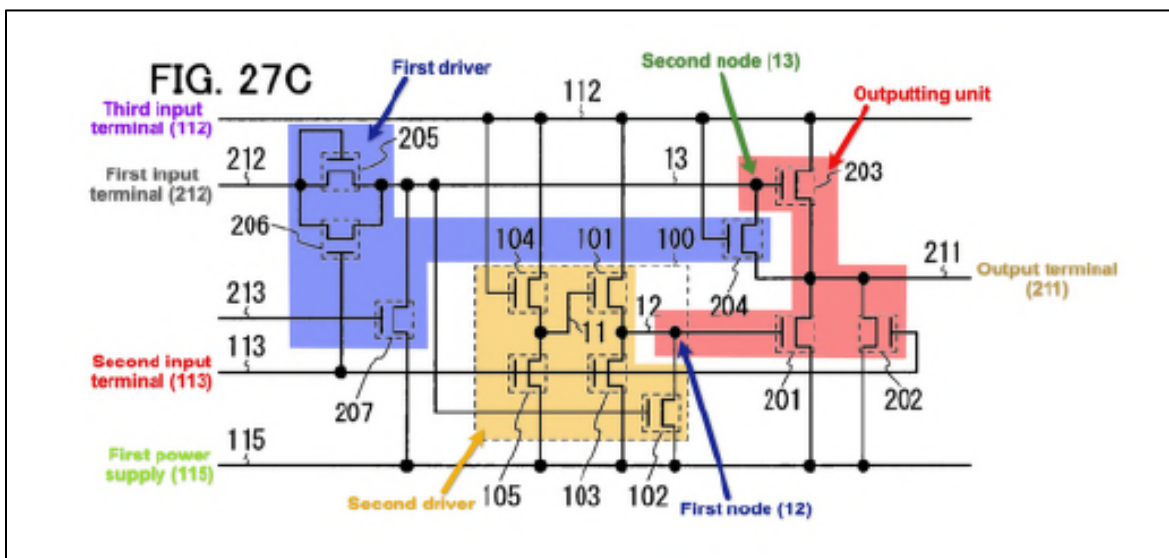
3. Kimura Does Not Teach or Suggest Claim Elements [1-A]/[15-D] and [6-B]/[20-B].

Claim elements [1-A] and [15-D] require “an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node.”

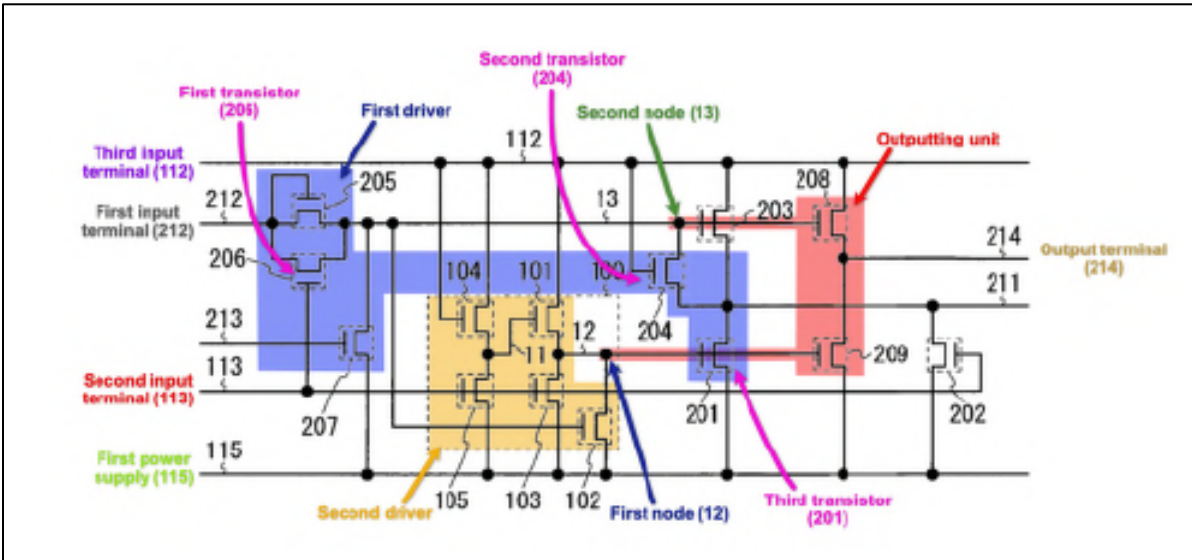
For claims 1 and 15, Petitioner identifies transistor 201 as part of the “outputting unit.” However, that reading of Figure 27C would not meet the

requirements of claims 6 and 20, including claim elements [6-B]/[20-B], which require “a second transistor and a third transistor serially positioned between the second node and the first power supply.” Acknowledging this tension, Petitioner is forced to modify its identification of which circuit elements in Figure 27C are part of the claimed “outputting unit” and “first driver” as compared to what it presented for independent claims 1 and 15. Petitioner provides no explanation for its changed analysis, and none exists other than, in hindsight, to realign its reading of the circuit in order to arrive at claims 6 and 20.

As shown below, for claims 1 and 15, Petitioner identifies transistors 204, 205, 206, and 207 as part of the “first driver,” and transistors 201, 202, and 203 as part of the “outputting unit.”



Pet., 15 (annotating Fig. 27C for claims 1 and 15).



Pet., 31 (annotating composite of Fig. 27C and Fig. 31B for claims 6 and 20).

Petitioner suggests that transistor 201 “operates to connect wiring 115 to node 13 via transistor 204.” Pet., 30. However, neither the Petition nor Dr. Foty’s declaration suggest that transistor 201 would operate differently as between Figure 27C and the composite Figure 27C and Figure 31B on which Petitioner relies for claims 6 and 20. Similarly, neither Petitioner nor Dr. Foty provides any explanation for why this transistor should be considered part of the “outputting unit” for claims 1 and 15, but part of the “first driver” for claims 6 and 20. This is



unsurprising, as no reason exists beyond modifying Figure 27C in a hindsight-driven attempt to arrive at the requirements of claims 6 and 20 that the “first driver” include “a second transistor and a third transistor serially positioned between the second node and the first power supply.” Ex. 2059, ¶58-71.

As reflected above, transistors 201 and 204 are located in the same positions in both Figure 27C and Petitioner’s modified composite of Figures 27C and 31B, and thus transistor 201 could also be identified as part of the “first driver” under Petitioner’s theory for claims 1 and 15. However, in Figure 27C, if transistor 201 were identified as part of the first driver, the alleged “outputting unit” would not “supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node” as Petitioner suggests. In particular, for that limitation of claims 1 and 15, Petitioner relies upon the same transistor 201, which has its gate connected to the alleged “first node,” to satisfy this requirement of the “outputting unit.” Pet., 17-18. If transistor 201 were instead identified as part of the “first driver,” there would be no element in the “outputting unit” that would allow for the “outputting unit” to “supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node” as the claims require. Ex. 2059, ¶63.

Needing to identify transistor 201 as part of the “first driver” to satisfy the requirements of claims 6 and 20, Petitioner turns to Figure 31B and proposes to



add two additional transistors and an additional “output” signal line to Figure 27C, so that Petitioner can identify these additional circuit elements as the new “outputting unit,” and identify transistor 201 as part of the “first driver” instead. This proposed modification results in a stage circuit having 14 transistors and at least 4 input signals. Pet., 30-31; Ex. 2059, ¶64.

Petitioner suggests that POSITAs would have made these modifications because it would “improve display operation, particularly when a large number of stages are employed.” Pet., 32. Neither Petitioner nor Dr. Foty addresses the significant detriments of adding two additional transistors and an additional signal line to each stage circuit. Contrary to Petitioner’s suggestion, these detriments are only exacerbated where a large number of stages are employed, as this would increase the total number of additional circuit elements. Ex. 2059, ¶65. As someone with display experience would readily understand, a display has hundreds if not thousands of rows of pixels. *Id.*

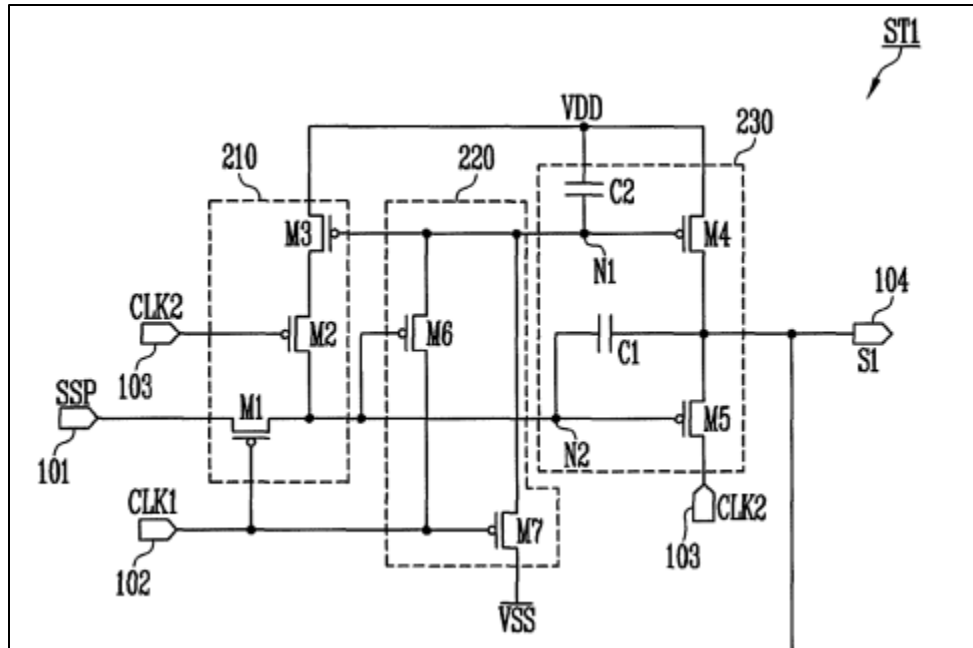
Indeed, as described above, the ’593 Patent explains that its invention allows for a reduction in the number of transistors and signal lines, and describes specific benefits associated with these reductions. *See, e.g.,* ’593 Patent, 9:12-26. POSITAs would not have added these circuit elements and incurred these significant downsides absent clear benefits, and Petitioner’s bare claim of “improve[d] display operation” is plainly insufficient. Pet., 32. Kimura itself describes that when “[t]he



number of transistors is reduced,” “layout area can be decreased” and “power consumption can be reduced.” Kimura ¶[0301].

Petitioner does not explain how the modified circuit it proposes for dependent claims 6 and 20 would meet the requirements of their independent claims 1 and 15, respectively, under Petitioner’s shifted analysis of Figure 27C’s circuit. Even under that shifted analysis, Petitioner’s modified circuit fails to teach or suggest the requirements of claims 6 and 20, because the elements Petitioner identifies as part of the new “outputting unit” do not provide scan signals to the output terminal 211 previously identified for claim 1. Ex. 2059, ¶¶66-71. Transistors 208 and 209 instead control the provision of signal SOUT to wiring 214. As Petitioner acknowledges, “the signal SOUT is not output to the wiring 211 but can be input to a semiconductor device in a different stage as a start pulse.” Kimura ¶[0304]. Petitioner acknowledges that the SOUT signal is a “different” signal than GOUT. Pet., 29.

As Petitioner acknowledged for claim 1, GOUT is the signal that is output to the scan lines that provide scan signals to the rows of pixel circuits. Kimura, ¶[0304]; Pet., 29. The ’593 Patent makes clear that the “output terminal” provides an output scan signal to the pixel circuits via scan lines. For example, as shown in Figure 3, the output terminal 104 connects to the scan lines Sn, which provide output scan signals to the pixel circuits.



'593 Patent, Fig. 3 (excerpted); see also, *e.g.*, *id.* Fig. 1. This is further illustrated by the language of claim 15, which recites “a scan driver for supplying scan signals to the pixels through the scan lines, the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals.”² Thus, the “output terminal” connects the stage circuits to

² The '593 Patent explains that the output of a previous stage can be provided into a subsequent stage as an input, as is the case with Kimura's GOUT, but unlike the '593 Patent's embodiments, SOUT is provided only to the subsequent stage of the scan driver, and is not also provided to the scan lines that connect to the pixel circuits. In any event, even if SOUT and GOUT were together considered to be the output signal, then transistors 201 and 203 (which control GOUT, i.e., the output

[REDACTED]

scan lines that are in turn connected to the pixel circuits. *See also, e.g.,* '593 Patent, 7:46-48 (“In this case, the output terminal 104 outputs the second clock signal CLK2 as a scan signal to the scan line S1”); *id.*, 8:15-17 (“In practice, the stages ST repeat the above-described processes to sequentially output the scan signals to the scan lines.”).

Accordingly, transistors 208 and 209, which control the output of SOUT to wiring 214, do not satisfy the requirements of the “outputting unit” of claim 1. Similarly, wiring 214 does not satisfy claim 1’s requirements of the “output terminal.” Ex. 2059, ¶¶66-71.

4. Kimura Does Not Teach or Suggest Claim Elements [7-C]/[21-C] and [7-D]/[21-D].

Claim elements [7-C] and [21-C] require that the “outputting unit” include “a first capacitor between the second node and the output terminal.” Claim elements [7-D] and [21-D] require that the “outputting unit” include “a second capacitor between the first node and the first power supply.” The circuit shown in Figure 27C, on which Petitioner relies for independent claims 1 and 15, does not include any capacitors, let alone capacitors in the alleged “outputting unit.”

signal to wiring 211) would still need to be part of the “outputting unit,” not the “first driver.”


Petitioner thus must seek to add two capacitors to Figure 27C to arrive at the requirements of claims 7 and 21.

Petitioner argues that POSITAs would have added two capacitors to Kimura's Figure 27C to arrive at these requirements of claims 7 and 21. Petitioner's assertion that "[c]apacitors can be added in various places" belies the hindsight-driven theory the Petition advances for these claims. Pet., 32; Ex. 2059, ¶¶73-75.

Petitioner looks to other embodiments of Kimura that include capacitors, and asserts that POSITAs would have added those capacitors to Kimura's Figure 27C. Pet., 32. In particular, Petitioner looks to Figure 9C and Figure 30C, and asserts that capacitors in these other embodiments "can be used with any of Kimura's devices, including that in Figure 27C." Pet., 33. Petitioner cites in support to Kimura ¶[0304], but this paragraph says *nothing* about capacitors, let alone adding capacitors to other embodiments of Kimura, Figure 27C or otherwise. Indeed, Kimura never suggests that these capacitors from different embodiments can or should be added to Figure 27C. Ex. 2059, ¶¶73-75.

Petitioner's application of these capacitors is further inconsistent with Kimura's description of the embodiments from which Petitioner proposes to take the capacitors. Ex. 2059, ¶¶75-77. For example, Kimura describes that the embodiment of Figure 9C is directed to a "circuit 120" that can be added to circuit

[REDACTED]

100 in Figures 1A, 6A-6F, 7A-7E, and 8A-8F to delay the provision of signal IN2 in those circuits. Kimura ¶[0190]. Kimura never discusses adding circuit 120 to other embodiments, and indeed, no circuit 120 appears in Kimura’s Figure 27C. Additionally, in Figure 9C, circuit 120 consists of a resistor 121 in addition to capacitor 122. Petitioner seeks to add only capacitor 122 to Figure 27C, and ignores Kimura’s disclosures that circuit 120 must include “at least a capacitance component and a resistance component.” Kimura ¶[0191]. Thus, not only does Kimura not suggest adding this capacitor to Kimura’s Figure 27C, but Petitioner further seeks to add it in a manner contrary to Kimura’s teachings. Petitioner makes no effort to show how a circuit with a resistor and a capacitor could or would be added to its base figure, Figure 27C. Ex. 2059, ¶75.

Petitioner’s proposed modifications are also inconsistent with Kimura’s focus on preventing or reducing transistor deterioration, and its explanation that reducing the time during which certain transistors are on will reduce deterioration of those transistors. *See, e.g.*, Kimura ¶[0228] (“Thus in a period during which the transistor 201 is on can be shortened. Accordingly, deterioration of the transistor can be suppressed.”); *see also id.* Abstract, ¶[0008]. For example, in Petitioner’s proposed modification, the capacitor 122 is connected to the gate of transistor 201, which will prolong its on time, rather than shorten it. Pet., 34; Ex. 2059, ¶76. Similarly, Petitioner proposes to connect capacitor 220 to the gate of transistor 203.

[REDACTED]

Additionally, Kimura describes that due to the addition of capacitor 220 “the potential of the node 13 is likely to rise in the bootstrap operation.” Kimura ¶[0303]. POSITAs would not look to modify Figure 27C, which describes *lowering* the potential of node 13, to include a capacitor that Kimura states will *raise* the potential of that node during the bootstrap operation. *See, e.g.*, Kimura ¶[0286]; Ex. 2059, ¶77.

Petitioner also asserts that “Kimura itself contemplates that the capacitors can be employed” and that the “device’s output signal is improved when the capacitors are used.” Pet., 34. Setting aside that, as discussed above, Kimura does not teach or suggest adding capacitors to Figure 27C, and that Petitioner seeks to add them in a manner inconsistent with Kimura’s description of the embodiments in which they are provided, Petitioner again overlooks the significant detriments that would be incurred by adding two capacitors to a stage circuit. As Dr. Wolfe explains, capacitors take up significant circuit area, and this, along with the necessary connections to other circuit elements would have to be taken into account in designing a modified stage circuit. Ex. 2059, ¶78.

Petitioner’s generalized assertions that it is possible to add these capacitors to Figure 27C would not provide POSITAs sufficient motivation to incur these detriments. Petitioner’s citations to Jeong, a different reference disclosing different circuits, with no further explanation, for the proposition that capacitors “improve

[REDACTED]

robustness of, reduce[] variation of voltage applied to, and can stabilize operation of certain of a shift register's output transistors" fare no better. Pet., 34. Petitioner provides no rationale for why these generalized considerations would motivate POSITAs to add two capacitors from different embodiments of Kimura to Figure 27C, let alone connect them within Figure 27C in the specific ways Petitioner suggests. They would not.

Dr. Foty also suggests that a POSITA would seek to add capacitors to prevent leakage current. Ex. 1003, ¶253. However, in a parallel proceeding Dr. Foty conceded that, unless a reference specifically discusses leakage current issues, POSITAs would assume the reference to teach a "functional process, which produces good transistors, not transistors that have a failure mechanism type of leakage." Ex. 2061, 58:4-11. Dr. Foty points to no teaching in Kimura that suggests leakage current is a concern.

As Dr. Wolfe explains, POSITAs would not have made these modifications, and Petitioner's arguments are nothing more than a hindsight-driven attempt to arrive at claims 7 and 21. Ex. 2059, ¶79. Indeed, the Board noted as much with respect to Petitioner's proposed combination of Jeong with Tobita. ID, 57-59.

5. Kimura Does Not Teach or Suggest Claim Elements [8-A]/[22-A] and [8-B]/[22-B].

Claim elements [8-A] and [22-A] require that the second driver include "a sixth transistor between the first node and the second input terminal, the sixth



transistor having a gate electrode coupled to the second node.” Claim elements [8-B] and [22-B] similarly require that the second driver include “a seventh transistor between the first node and a second power supply, the second power supply having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal.”

Petitioner concedes that “none of Figure 27C’s transistors are connected in the way the claim requires,” and proposes modifications to Figure 27C in order to arrive at these claims. Pet., 35. Notably, unlike the modifications Petitioner must make for other challenged claims, Petitioner does not even attempt to depict how the modifications it proposes would allegedly be made, or explain how the resulting circuit would operate. Pet., 35-36; Ex. 2059, ¶¶80-81. Petitioner suggests that Kimura states that these modifications “can be” made. Pet., 35-36. Petitioner cites to no disclosure of Kimura teaching that any of these modifications could be made to Figure 27C. *Id.* Petitioner also provides no rationale for making these modifications, instead suggesting that the needed changes would be a “design alternative.” *Id.*; *see also* Ex. 2059, ¶¶81-86.

Petitioner has failed to show that these modifications would result in an operable circuit, let alone identify a sufficient basis for POSITAs to have made these modifications with a reasonable expectation of success. Ex. 2059, ¶¶81-86. As one example, Petitioner asserts that “‘the first terminal of the transistor 102’

[REDACTED]

can be ‘connected to the wiring 113’ instead of wiring 115,” and that with this modification, transistor 102 is the claimed sixth transistor. Pet., 35-36. But Petitioner cites in support to a portion of Kimura describing Figure 7C, not Figure 27C. Kimura ¶[0169] (“FIG. 7C illustrates a structure where the first terminal of the transistor 102 is connected to the wiring 113”); *see also id.* ¶[0168] (listing only Figs. 1A, 6A-6F, and 7A-7 as structures in which “the first terminal of the transistor 102 can be connected to a wiring which is different from the wiring 115). Notably, in the Figure 7C configuration, transistor 102 has its gate connected to wiring 114, not node 13 (the identified “second node”) as required by claims 8 and 22. Petitioner fails to explain this discrepancy, let alone point to any disclosure in Kimura that suggests that transistor 102 would still have its gate connected to the identified “second node” when its first terminal is connected to wiring 113 instead of wiring 115. Ex. 2059, ¶¶82-83.

Petitioner’s theory also requires, in addition to changing the connections of the transistors in Figure 27C in ways not supported by Kimura, adding an additional power supply line to Figure 27C. Petitioner provides no explanation whatsoever for this proposed modification. Pet., 36. Petitioner simply suggests that “Kimura also teaches that the same device can be provided with multiple different power supply voltages.” *Id.* For claims 1 and 15, Petitioner identifies wiring 115 as the “first power supply.” Pet., 18. For claims 8 and 22, Petitioner points to a



different embodiment (Figure 30A) and suggests that wiring 115b in that embodiment would satisfy the “second power supply” limitation of those claims. Petitioner does not explain what would be the “first power supply” in its proposed modification, explain what voltages would be provided by the identified “first” and “second” power supplies, or explain how the resulting modified circuit would function. Ex. 2059, ¶¶84-85

For example, Petitioner suggests that Kimura describes (for other embodiments) that wiring 115 “can be provided with multiple different power supply voltages.” Pet., 36. Petitioner points to Figure 30A, and asserts that for that embodiment Kimura teaches that “transistor 103 is connected to a different power supply with a different voltage (wiring 115B) than output transistor 201 (wiring 115D).” Pet., 36. But with respect to Figure 30A, Kimura explains that “the voltage V_1 can be supplied to the wirings 115A to 115E.” Kimura ¶[0299]. Ex. 2059, ¶¶84-85. Petitioner similarly fails to point to anything in Kimura that would teach or suggest connecting transistor 203 (the identified “seventh transistor”) to a “second power supply having a lower voltage than the first power supply,” as Petitioner suggests. Pet., 36.

Finally, as with its other proposed modifications, Petitioner entirely ignores the significant downsides of adding multiple additional circuit elements and modified connections that would be incurred. Ex. 2059, ¶86. Indeed, Petitioner

[REDACTED]

ignores Kimura’s teachings that reducing power sources results in improved reliability and yield, and reduces manufacturing costs. Kimura ¶[0196]; Ex. 2059, ¶86. This further undercuts Petitioner’s unsupported theory that POSITAs would nevertheless seek to add a power supply to arrive at the requirements of claims 8 and 22. POSITAs would not have had motivation to make these modifications, or had a reasonable expectation of success in so doing. Ex. 2059, ¶¶85-86.

B. Neither Shin in View of Sasaki nor Shin in View of Sasaki and Jeong Renders Obvious Any Challenged Claim.

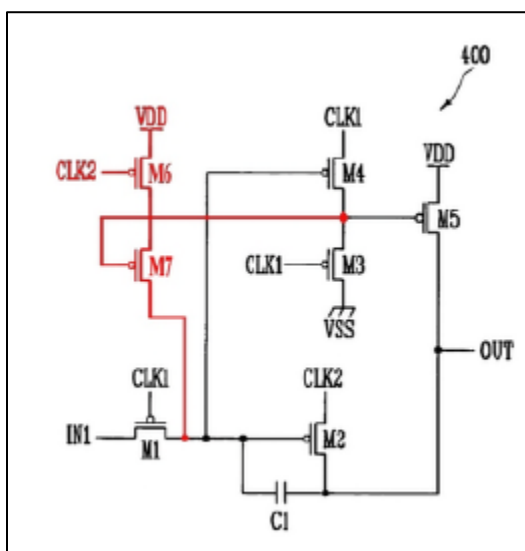
As the Board noted, Petitioner’s sole rationale for combining Shin and Sasaki rests upon an alleged “lack of robustness” in Shin’s circuit. ID, 36. As the Board noted, “Petitioner’s allegations are theoretical at best.” ID, 36. Indeed, Petitioner can point to nothing in either Shin or Sasaki that suggests that Shin’s circuit is not sufficiently “robust,” let alone any reason for POSITAs to add multiple additional circuit elements to Shin’s circuit. As Dr. Wolfe explains, Petitioner’s arguments require making significant modifications that POSITAs would not have had a reason to make. Ex. 2059, ¶87. Petitioner additionally dismisses without explanation teachings in Shin that would obviate the only identified rationale Petitioner provides for modifying Shin. Moreover, Petitioner seeks to apply Sasaki’s circuitry to Shin in a manner that is inconsistent with Sasaki’s teachings. Dr. Foty confirmed this during his deposition. Ex. 2060, 54:13-55:2. For all of these reasons POSITAs would not have been motivated to combine

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Shin and Sasaki and would not have had a reasonable expectation of success in so doing.

1. Shin Already Addresses the Purported Issue for Which Petitioner Proposes to Add Circuitry from Sasaki.

Petitioner proposes to take two transistors from Sasaki (red) and apply them to Shin's Figure 11:



Pet., 50. All of Petitioner's arguments relating to this Ground require combining these elements of Shin and Sasaki in the specific manner shown above. *See, e.g.*, Pet., 53.

The only rationale Petitioner provides for adding these additional transistors (and connecting them in the specific manner, with the specific inputs shown above) is the unsupported assertion that POSITAs "would have recognized that Shin's scan driving circuit is subject to a problem like that identified by Sasaki." Pet., 47.

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The purported problem involves reversal (i.e., switching from an intended level to an opposite level) of a particular node, for which Sasaki provides these additional circuit elements. But Petitioner’s hindsight-driven assertion is belied by Shin’s disclosures, as the Board noted. ID, 36. In particular, Shin already contains circuitry, namely capacitor C1, which Shin explains will mitigate concerns of reversal at the node to which Petitioner proposes to add these additional circuit elements. Ex. 2059, ¶89.

As Petitioner acknowledges, the reversal for which Sasaki is concerned may occur when a particular node is in a “floating state,” or in other words a state in which the node does not have a signal voltage supplied to it. Sasaki ¶[0042]; Pet., 46. However, Shin explains that when that the node to which Petitioner proposes to provide Sasaki’s “anti-reversal” circuit (i.e., the node connected to the gate of transistor M2) might be in a “floating state” Shin’s capacitor C1 maintains the intended voltage on that node. *See, e.g.*, Shin ¶[0107] (“a voltage of the capacitor C1 remains unchanged, and thus the second transistor M2 continues to be turned-on....”). Ex. 2059, ¶¶88-91.

Petitioner tacitly acknowledges this gaping hole in its rationale, yet provides only the bare conclusion that “a POSITA would have recognized that this capacitor is not sufficient by itself to address Shin’s anti-reversal problem.” Pet., 49. Petitioner’s assertion is contradicted by Shin’s disclosures, which teach that C1 is

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sufficient to maintain the voltage on the gate of M2. *Id.*; Ex. 2059, ¶91. As Dr. Wolfe explains, there is nothing in Shin that states or would suggest to POSITAs that capacitor C1 is “not robust enough” to carry out the specific function for which Shin teaches it is provided, or that, in addition to capacitor C1, two additional transistors would be necessary, or even helpful, to perform that same function. Ex. 2059, ¶92,

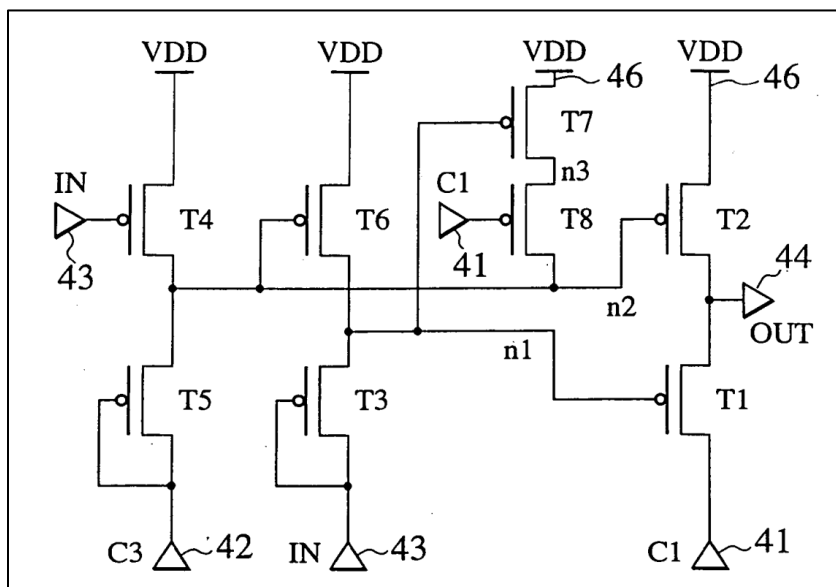
Petitioner’s argument also fails to address the numerous reasons POSITAs would *avoid* adding additional circuit elements, as the Board again observed. ID, 36-37 (“These known concerns, which Petitioner does not address, tend to undermine Petitioner’s rationale for the combination.”). Adding elements to a circuit design will increase the footprint of the circuit, as prior art cited by Dr. Foty confirms. *See, e.g.*, Ex. 1006, ¶¶[0015], [0107] (describing “concern for increased circuit area”).

Additionally, as the ’593 Patent explains, adding elements to a circuit may increase complexity, decrease stability, and lower process yield. Ex. 1001, 9:12-26. Also, as Dr. Wolfe explains, any added circuit elements will require input signals and their associated timings. Ex. 2059, ¶¶92-94. The timings of existing circuit elements may also be impacted by the added elements. In addition, the driver that provides certain input signals may need to be modified to provide any additional or altered timings to enable the modified circuit to function properly. Each of these

factors are among the specific benefits provided by the inventions. Petitioner ignores these concerns with its generalized assertions that POSITAs would mix and match teachings of various references simply because they are directed to stage circuits or that general concepts were “well known.”

2. Petitioner Applies Sasaki's Circuitry Inconsistently with Sasaki's Teachings.

Petitioner's argument also relies on misapplying Sasaki's teachings. Sasaki's “anti-reversal” circuit is directed specifically at the potential reversal of Sasaki's node n2 that Sasaki explains may be subject to reversal at a specific time in the operation of Sasaki's circuit. *See, e.g.*, Ex. 1003, ¶388. Figure 4 of Sasaki depicts a stage circuit according to a first embodiment of Sasaki. Transistors T7 and T8 form the “anti-reversal” circuit.

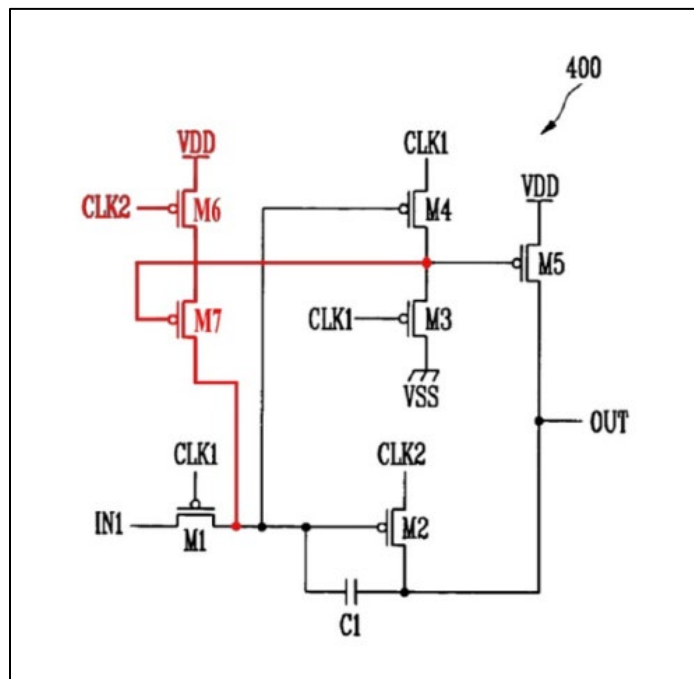




Node n2 in Sasaki is connected to the gate of transistor T2, which controls whether the high voltage VDD is provided to the output terminal. Sasaki explains that reversal of the node n2 could result in the high voltage supply VDD being erroneously provided to the output terminal when a low value is intended. Ex. 1014, ¶[0048]. Sasaki explains that this can lead to unintended distortion of the output signal. Ex. 1014, ¶[0048] (describing that with no anti-reversal circuit, if node n2 is reversed “transistor T2 starts conducting and the high voltage VDD is supplied to the output terminal 44 through the second transistor T2[,]” resulting in a “distorted” output waveform.).

As Sasaki explains, it is reversal of this specific node at the identified point in the operation of the circuit at which Sasaki teaches that reversal would be particularly problematic. Sasaki repeatedly describes potential distortion when the intended output signal is low and VDD is erroneously provided to the output terminal. *See, e.g.*, Ex. 1014 ¶[0051] (“As a result, the output signal OUT at the low level without distortion will be supplied to the output terminal 44.”); *see also id.*, ¶¶[0055], [0059], [0061], [0064], [0066]. In contrast, Sasaki does not describe potential distortion when the intended output signal is high and CLK2 is erroneously provided (i.e., if reversal of Sasaki’s node n1 were to occur). Ex. 2059, ¶¶95-97.

The equivalent node to Sasaki's node n2 in Shin is the node connected to the gate of transistor M5, because this node in Shin, like node n2 in Sasaki, controls whether the high voltage VDD is provided to the output terminal. Ex. 2059, ¶¶95-96. However, contrary to the teachings of Sasaki, Petitioner does not propose to add the "anti-reversal circuit" to this node in Shin. Ex. 2060, 54:13-55:2; *see also* Ex. 2059, ¶¶95-100. Instead, Petitioner incorporates Sasaki's "anti-reversal" circuit to the *opposite* node, i.e., the node at the gate of transistor M2 that controls whether the clock signal CLK2 is provided to the output terminal.



Pet., 50; *see id.* ("In operation, added transistors M6 and M7 operate to supply a high VDD signal to transistor M2's gate to prevent the transistor from opening and inadvertently supplying a low CLK2 signal to OUT at a time when the circuit's output is intended to be high").



Notably, and as Dr. Wolfe explains, the node to which Dr. Foty seeks to add Sasaki’s “anti-reversal” circuit does not have the same operational concerns that Sasaki describes in explaining why its “anti-reversal” circuit is provided. *See* Ex. 2059, ¶¶99-100. Sasaki describes the purpose of the “anti-reversal” circuit as being to prevent reversal of the node that controls whether the high voltage VDD is provided to the output, because reversal of that node could lead to the high voltage VDD distorting the intended low value output. *See, e.g.,* RX-0095 ¶[0051]. In contrast, the node in Shin to which Petitioner applies Sasaki’s “anti-reversal” circuit does not control whether VDD is provided to the output terminal. Ex. 2060, 54:13-55:2; *see also* Ex. 2059, ¶¶99-100. Petitioner’s argument thus rests entirely on a misapplication of Sasaki’s teachings.

3. Shin in View of Sasaki and Further in View of Jeong Does Not Render Obvious Claim Elements [7-D] and [21-D].

Claim elements [7-D] and [21-D] require that the “outputting unit” include “a second capacitor between the first node and the first power supply.” Petitioner acknowledges that its proposed combination of Shin and Sasaki does not include the second capacitor required by claim elements [7-D] and [21-D], and proposes to further combine Shin and Sasaki with Jeong. Pet., 74.

The only rationale Petitioner provides as to why POSITAs would purportedly seek to add an additional circuit element to the composite circuit of

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Shin as modified by Petitioner to include Sasaki's "anti-reversal" circuit is an unsupported reference to potential "electromagnetic interference or other perturbances," and a conclusory, unsupported assertion that "[a] POSITA would have understood that this problem would be eliminated by including another capacitor." Pet., 77. These fail.

Contrary to Petitioner's unsupported assertions, nothing in Shin or Sasaki suggests any operational issue with Shin or Sasaki's circuitry that would motivate adding a capacitor. Ex. 2059, ¶¶102-106. Indeed, while Petitioner acknowledges that Shin already has a capacitor C1, and suggests this means POSITAs would have naturally added another capacitor, in reality this demonstrates that Shin was familiar with the generalized concerns Petitioner points to, yet intentionally added a capacitor (C1) where it was needed, and did not add a capacitor where it was not. Ex. 2059, ¶104. Moreover, Petitioner's arguments regarding Shin's inclusion of capacitor C1 are inconsistent with its arguments that capacitor C1 is insufficient for its intended purpose. *Id.* Petitioner's citation to Jeong's teachings relating to different circuits similarly do not manufacture a rationale sufficient to motivate POSITAs to add an additional capacitor. As noted above, while Dr. Foty also suggests that a POSITA would seek to add capacitors to prevent leakage current, Ex. 1003, ¶580, this is inconsistent with his prior deposition testimony, Ex. 2061, 58:4-11.

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Petitioner and its expert additionally overlook the detriments to adding additional circuit elements to a scan driver stage circuit, detriments with which POSITAs would have been well aware. Ex. 2059, ¶106. For example, a different reference relied upon by Petitioner describes that capacitors detrimentally add significant circuit area. *See, e.g.,* Tobita ¶[0015]. POSITAs would have been familiar with such detriments and would not have sought to add additional circuit elements absent a clear and specific reason to do so. Petitioner provides no such reason. The generalized concerns Petitioner suggests could possibly arise would not overcome the known issues and disadvantages associated with adding circuit elements like capacitors to stage circuits. Ex. 2059, ¶106.

C. Neither Tobita nor Tobita in View of Jeong Renders Obvious Any Challenged Claim.

Patent Owner agrees with the Board's articulation in the institution decision that limitation [1-B]/[15-E] does not require the voltage of the second node to be determined solely by the first driver alone. For clarity, and as discussed below, Patent Owner notes that, by the plain terms of the claim language, the first driver must be involved in controlling the voltage of the second node, and must do so in accordance with each of the recited signals (i.e., the signals of the first, second, and third input terminals) in independent claims 1 and 15. Patent Owner reads the Board's articulation in the institution decision to be consistent with this understanding. Applying its construction, the Board found that:

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Patent Owner's arguments about transistors Q19, Q20, and Q21 not directly controlling node N1 (i.e., the 'second node') do not necessarily undermine Petitioner's showing. Based on the present record, Petitioner shows sufficiently for institution that Tobita's transistors Q19-Q21 (i.e., part of the 'first driver') indirectly control the voltage of the node N1 by opening transistor Q18 to allow VSS to be provided to node N1 for purposes of bringing it to a low level.

ID, 51.

However, Patent Owner respectfully submits that Petitioner's theory goes beyond the question of whether other circuit elements may have an impact on the voltage of the second node. That was the claim construction issue before the ITC, which the Board referenced in adopting its construction. ID, 12-13. There, *Petitioner BOE* argued that no other circuit element could have *any* impact on the voltage of the node. Ex. Ex. 2018 at 30 ("Respondents contend that '[a] POSITA would not understand the driver to 'control' the voltage of a node if something other than the driver's output is able to override that output and change the node's voltage...."). In response, Patent Owner noted that the specification shows that other circuit elements, e.g., a capacitor, may impact the voltage of the node in addition to the driver. *Id.* at 32.

Petitioner's theory instead relies upon using the signals of the first, second, and third input terminals to apply a voltage to an unclaimed node, which itself then turns on a transistor that allows a different signal to be provided to the alleged



second node. Such an argument is distinct from the claim construction issues raised at the ITC and fails to satisfy the claims.

Petitioner's theory additionally fails for a fundamental reason. The claims require that the "first driver" controls the voltage of the "second node" in accordance with the signals of the first, second, and third input terminals. Petitioner alleges that the transistors it identifies as part of the first driver turn on transistor Q18 to allow a low signal to be passed to the alleged second node. However, with respect to the signal of the third input terminal—contrary to its explanation in the Petition—Petitioner's theory relies upon the *absence* of any input by the first driver. When the signal of the third input terminal turns on the identified transistor in the first driver (Q21), it causes transistor Q18 to turn off, and no longer provide any signal to the identified second node. Ex. 1003, ¶618. Petitioner's expert admitted during deposition that this will not change the voltage that is already on the second node. Ex. 2060, 71:10-16. As Dr. Wolfe explains, this lack of a signal does not itself change or otherwise control the voltage of the second node. Ex. 2059, ¶115. Indeed, Tobita confirms that the operation of the circuit formed by transistors Q19-Q21 does not alter the output waveform relative to other embodiments that do not include these transistors. Tobita ¶[0177].

Finally, Tobita is directed to a scan driver shift register for a liquid crystal display. Tobita ¶[0004]. Tobita describes a problem with conventional shift

[REDACTED]

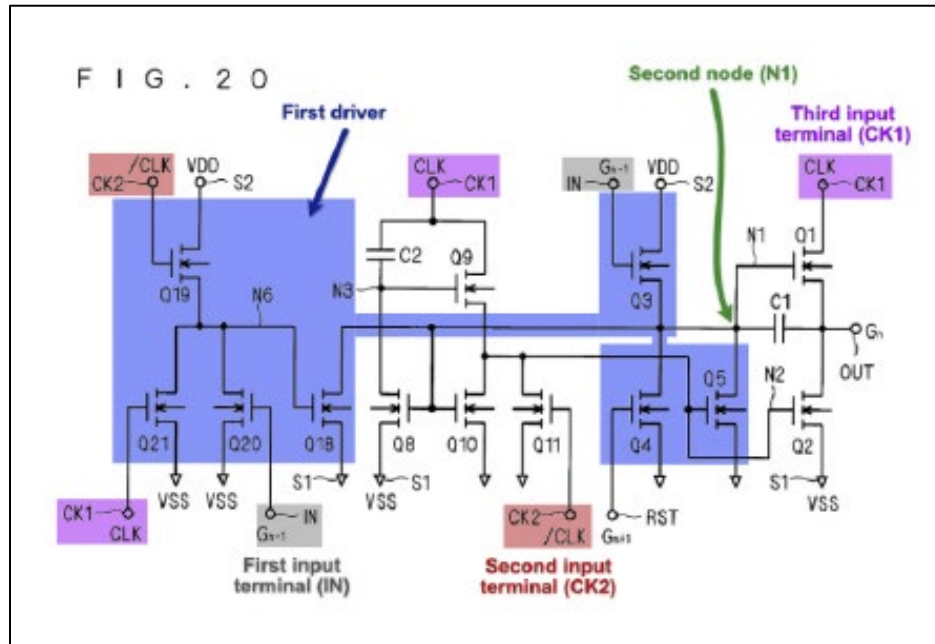
registers comprised of amorphous silicon TFTs, in which degraded driving capability occurred because “a-Si TFT tends to have its threshold voltage shifted in the positive direction when the gate electrode is continuously positive-biased.” Tobita ¶[0010]. Tobita describes that other approaches required additional capacitive elements with “large capacitance” which led to “increases [in] the circuit area.” Tobita ¶[0015]. Accordingly Tobita “control[s] an increase in circuit area of a shift register while preventing malfunctions...” Tobita ¶[0016]; Ex. 2059, ¶¶107-108.

Tobita’s eighth embodiment, on which Petitioner relies, is directed to solving a problem with optical leakage current that may predominantly arise due to the display’s backlight. Tobita ¶[0170]. OLED displays do not have backlights, and thus are not susceptible to backlight leakage current, as POSITAs would have understood. Ex. 2059, ¶109. As Dr. Wolfe further explains, POSITAs would not have looked to a reference directed to liquid crystal displays, let alone an embodiment that adds significant additional circuitry to account for a problem with incident light such as that from backlight leakage for an OLED stage circuit. *Id.*

1. Tobita Does Not Teach or Suggest Claim Element [1-B]/[15-E].

Claim limitations [1-B] and [15-E] require a “first driver” that “control[s] the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal.” Petitioner identifies

portions of Tobita's Figure 20 (blue) as purportedly satisfying this limitation. Pet., 84.



However, Tobita is clear that in Figure 20, transistors Q19, Q20, and Q21 are provided to determine the voltage of node N6, not node N1 (the identified second node). Tobita ¶¶[0172]-[0178]; *see also* Ex. 2059, ¶112. Tobita explains that transistors Q19 and Q20 operate as an “inverter circuit,” with node N6 “serving as the output node of the inverter circuit.” Tobita ¶[0174]. Tobita also explains that Q21 operates to keep this output node “at the L level” at a particular period of operation of the stage circuit. Tobita ¶[0177]. Tobita explains that transistors Q19-Q21, which are only added to previous embodiments to address the optical leakage issue noted above, do not “affect the operation of the unit shift register SR_n of outputting the output signal G_n .” *Id.* In other words, Tobita explains


that these transistors do *not* affect the output signal, which is instead controlled by nodes N1 and N2 in Tobita's stage circuit. *Id.*; Ex. 2059, ¶¶112, 120.

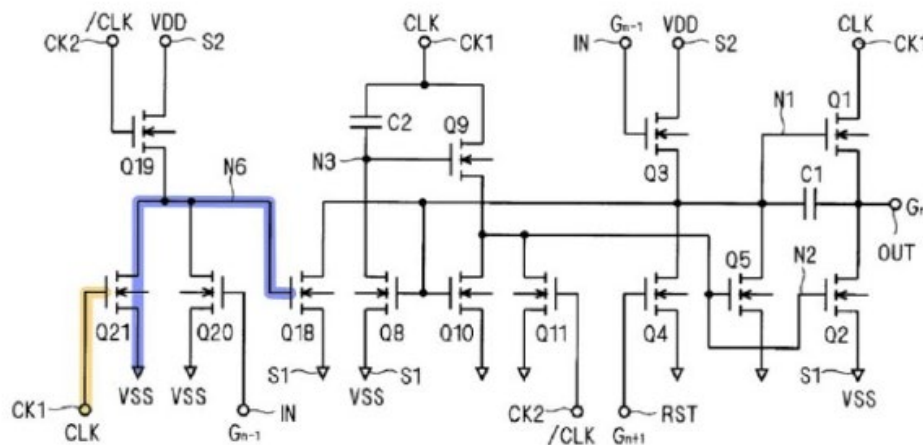
Accordingly, Q19, Q20, and Q21 (which Petitioner has identified as part of the "first driver") do not control the voltage of the identified second node (N1) as this claim element requires; they instead control the voltage of a different node, N6, and the voltage on node N6 is not passed to the node N1. Ex. 2059, ¶¶113-114. Instead the voltage on node N6 is passed to the gate of another transistor, Q18, to turn that transistor ON and OFF. Transistors Q19, Q20, and Q21 may thus control the voltage of *node N6* in accordance with the signals of the identified input terminals (CK1, CK2, and IN), but they do not control the voltage of node N1 in accordance with the signals of those input terminals. Ex. 2059, ¶¶113-114. Dr. Foty acknowledged during his deposition that these transistors control the voltage of node N6. Ex. 2060, 60:5-9; 62:21-63:8.

Independent of this, Petitioner's theory fails for an additional, fundamental reason. Even under Petitioner's theory, the identified "first driver" does not control the voltage of the second node in accordance with the signal of the third input terminal. Specifically, Petitioner asserts that "[t]ransistors Q18-Q21...control the voltage of the node N1 by, *e.g.*, bringing it to a low level." Pet., 84-85. However, in asserting that these transistors purportedly control the voltage of N1 in accordance with the signal of the third input terminal, Petitioner's declarant, Dr.

[REDACTED]

Foty, does not opine that the first driver brings the voltage of node N1 to a low level based on the operation of transistor Q21. Instead, he opines that the signal of the third input terminal (CK1) causes transistor Q21 to turn ON, which allows VSS to be passed to the gate of transistor Q18, which turns transistor Q18 **OFF**. Ex. 1003, ¶618.³ This is further shown in Dr. Foty’s annotated version of Figure 20, excerpted below:

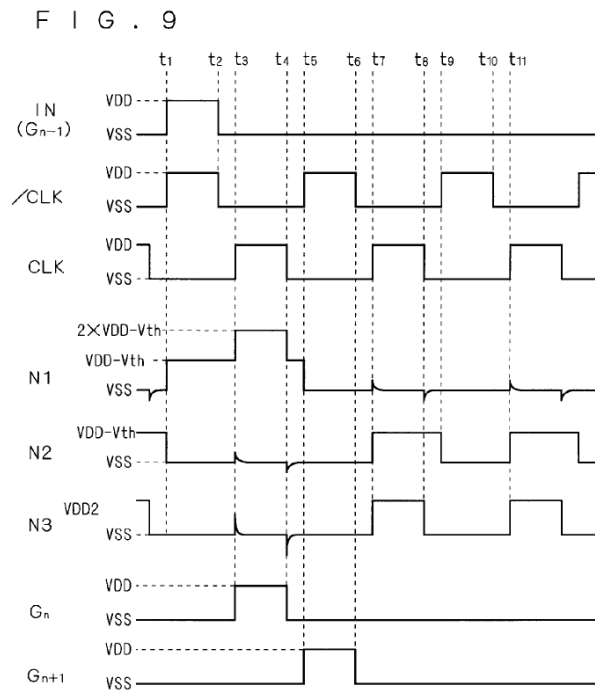
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However, turning transistor Q18 **OFF** does not bring node N1 “to a low level” as Petitioner asserts. Ex. 2059, ¶¶115-119. Turning off transistor Q18 only causes VSS to no longer be provided through transistor Q18 to node N1. Ex. 1003, ¶618. As Dr. Foty admitted, simply turning off transistor Q18 will **not** change the

³ Q18 is an NMOS transistor; accordingly, applying a low signal VSS turns Q18 OFF. See Ex. 1003, ¶611.

voltage of the node N1. Ex. 2060, 71:10-16; *see also* Ex. 2059, ¶115. This is further confirmed by the timings shown in Tobita's Figure 9, on which Dr. Foty relies. Ex. 1003, ¶610; *see* Ex. 2059, ¶¶115-118. During the time period identified by Dr. Foty in which CLK is high and transistor Q21 turns on (t7-t8), the voltage of N1 remains at a low level:



Thus, turning off transistor Q18 does *not* control the voltage on node N1, either directly or indirectly. Ex. 2059, ¶¶115-118. Because the voltage on N1 is not controlled by the alleged first driver in Tobita's eighth embodiment in accordance with the signal of the third input terminal (CK1), Petitioner's theory necessarily fails.

[REDACTED]

Finally, Petitioner's and Dr. Foty's overbroad application of the claim language is inconsistent with the teachings of the '593 Patent. Indeed, Dr. Foty testified during deposition that under the interpretation he uses, turning transistor Q21 on would purportedly control not only node N6 and N1 in accordance with the signal of the third input terminal but would also control the node at the output terminal in accordance with that signal by setting into motion a cascade of effects that culminates in the voltage on the node at the output terminal being set. Ex. 2060, 70:6-72:5 (discussing number of transistors that may be in a "transistor path" to provide a signal to a node, and explaining that "[t]he claim merely says in accordance with, so if you have cause and effect, I don't see any reason that accordance limits the number of transistors that could be there"); *id.* 72:6-73:3.

This overbroad interpretation would render the "in accordance with" language of the claim meaningless. The '593 Patent is clear that the first driver controls the *voltage of the second node*. The '593 Patent does not teach, for example, that the first driver controls the voltage of the output terminal nor does it attribute any subsequent operation of the claimed stage circuit to the first driver, as Petitioner and Dr. Foty would read the claims. This reading would render meaningless the "in accordance with" language because it would ascribe any operation of the circuit back to the first driver. Ex. 2059, ¶119. Petitioner's theories fail for this additional reason.

2. Tobita In View of Jeong Does Not Teach or Suggest Claim Elements [7-D]/[21-D].

Claim elements [7-D]/[21-D] require that the “outputting unit” includes “a second capacitor between the first node and the first power supply.” Petitioner admits that the identified “outputting unit” in Tobita does not include the claimed second capacitor. Pet., 95. Petitioner proposes to add an additional capacitor from an unrelated reference, Jeong. As the Board found, “Petitioner’s rationale for adding a capacitor to Tobita’s circuit is based on hypothetical concerns.” ID, 58. As Dr. Wolfe explains, POSITAs would not have modified Tobita as Petitioner suggests. Ex. 2059, ¶¶122-123.

Petitioner does not identify any operational issues with the embodiment of Tobita on which it relies, instead making unsupported assertions that Tobita’s circuit “could experience” unintended “voltage variation.” Pet., 97; *see also* Ex. 2059, ¶122. As Dr. Wolfe explains, POSITAs would not simply assume that there could possibly be such issues, and any generic concerns would not motivate POSITAs to add a capacitor to Tobita’s circuit. Ex. 2059, ¶122. A given circuit will be specifically designed for its intended purpose, and POSITAs would not haphazardly add circuit elements without clear objectives or benefits. *Id.*

Indeed, Tobita explains that capacitors add significant circuit area, Tobita ¶¶[0015]-[0017], and Tobita is directed to reducing circuit area where possible. *Id.* Neither the generalized and unsupported concerns Petitioner identifies, nor Jeong’s



teachings relating to a capacitor in a different circuit would provide sufficient motivation for POSITAs to add an additional capacitor to Tobita's circuit. Ex. 2059, ¶¶122-123. Moreover, Tobita includes a capacitor, C1, in the identified "outputting unit," yet does not include the additional capacitor Petitioner proposes to add. Tobita, Fig. 20. Thus, Tobita was familiar with the generalized concerns Petitioner points to, yet intentionally added a capacitor (C1) where it was needed, and did not add a capacitor where it was not. This further confirms that the generic considerations Petitioner advances (of which Tobita's author would have been similarly aware) would not motivate POSITAs to add a capacitor to Tobita as Petitioner suggests, let alone connect it in the specific way Petitioner does, which is necessary to arrive at the claims. Ex. 2059, ¶¶122-123. As noted above, while Dr. Foty also suggests that a POSITA would seek to add capacitors to prevent leakage current, Ex. 1003, ¶712, this is inconsistent with his prior deposition testimony, Ex. 2061, 58:4-11.

V. Objective Indicia of Non-obviousness

Petitioner's obviousness theories are further undercut by real-world, objective evidence of non-obviousness. *See* Ex. 2059, ¶¶124-151.

A. The inventions satisfied long-felt needs and succeeded where others had failed.

With the increasing use of smartphones in the early 2010s, there was a significant and growing need for AMOLED displays suitable for mobile devices,

[REDACTED]

and in turn a need for scan driver stage circuit designs that would allow for a reduction in the non-active bezel spaces (also known as “dead space”) around displays. Ex. 2059, ¶¶126-137. As one industry commentator noted, “[a]n idea that ha[d] long been passed around [wa]s to create a phone ... without a bezel[,]” since “removing the bezel would utilize the entire surface area of the [smartphone] device.” Ex. 2049, 2. Because the stage circuits are located along the side bezels of the display, “small sized [scan] drivers [we]re required to reduce the [bezel] area and to implement compact and high density displays.” Ex. 2050, 1.

Developing AMOLED displays with narrow bezels proved especially difficult because of the high complexity of stage circuits being proposed. Ex. 2059, ¶¶129-130. For instance, the ’593 Patent discusses the problem of “conventional stage circuits” which used “a plurality of transistors, e.g., at least ten transistors” that led to process yield deterioration, stability reduction, and greater circuit complexity. Ex. 1001, 9:12-26. Likewise, researchers at Hydis Technologies observed that “conventional” scan driver stage circuits “need[] a plurality of ... signal lines” which “causes a problem of enlarging a dead space of a display device, resulting in the display having bigger size than originally planned.” Ex. 2051, ¶¶[0013]-[0014].

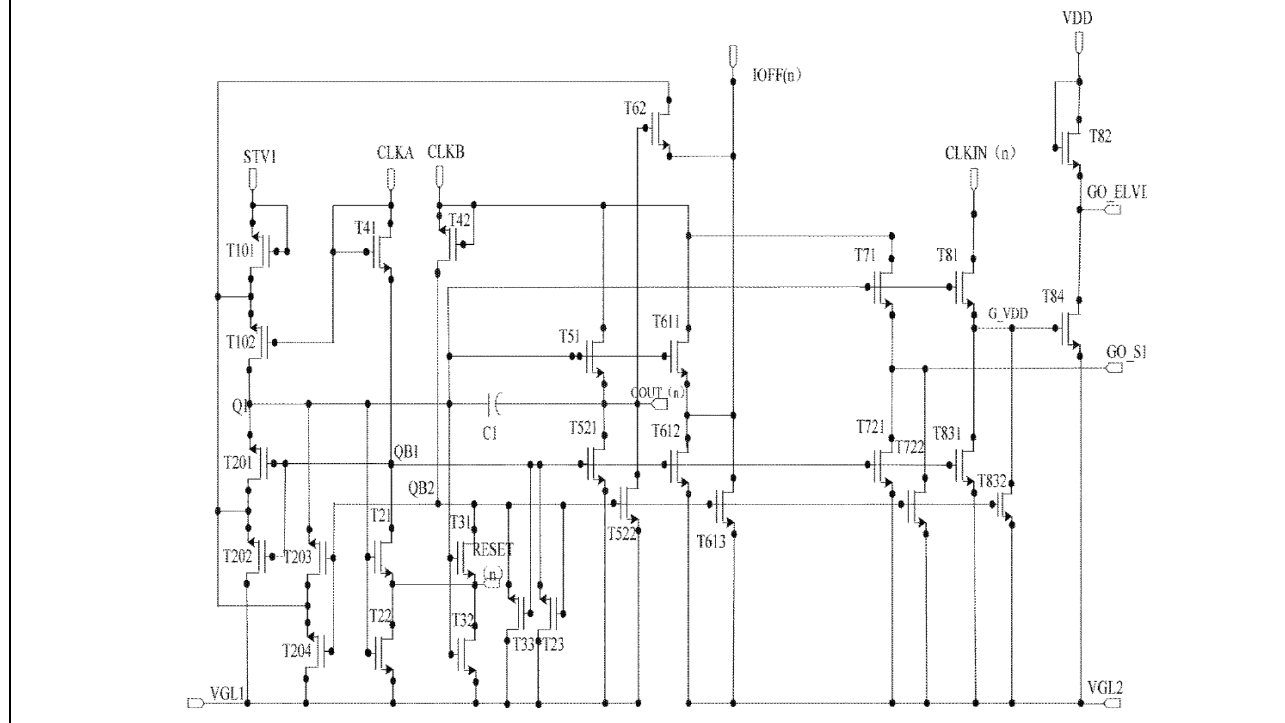
Over the years, display manufacturers and researchers proposed many stage circuits in an attempt to answer the industry’s demand for AMOLED displays with

[REDACTED]

narrower bezels. Ex. 2059, ¶¶133-136. The wide-ranging efforts by others to develop alternative stage circuits, without success, supports non-obviousness. This includes the stage circuits disclosed in Petitioner's cited references, such as Kimura (assigned to Semiconductor Energy Laboratory and published in March 2011) and Tobita (assigned to Mitsubishi Electric and published in May 2008). E Ex. 2059, ¶¶133. In fact, the many years between the publication dates of Petitioner's cited references (e.g., Shin (Ex. 1005, published in 2007), Sasaki (Ex. 1014, published in 2005), and Jeong (Ex. 1007, published in 2008)) and the inventions of the '593 Patent, when many groups were actively attempting to solve the long-felt needs, itself underscores the claimed inventions' nonobviousness. *See Leo Pharm. Prods., Ltd. v. Rea*, 726 F.3d 1346, 1359 (Fed. Cir. 2013).

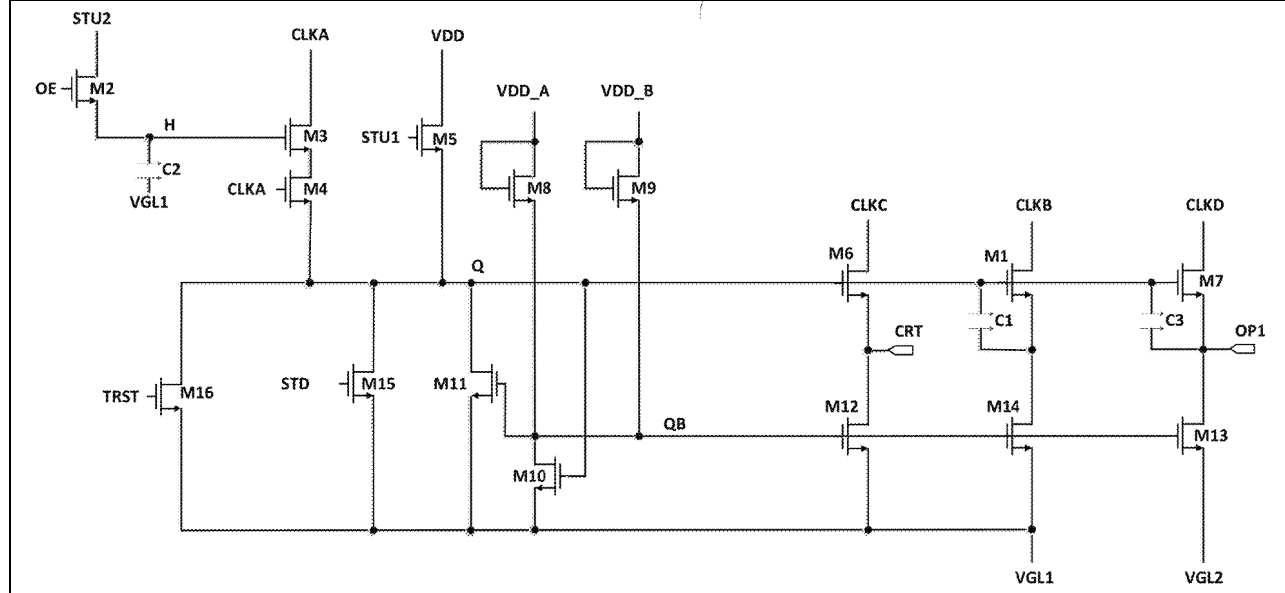
Continued research after the '593 Patent also failed to result in successful scan driver stage circuit structures. *See In re Cyclobenzaprine Hydrochloride Extended-Release Capsule Pat. Litig.*, No. 09-MD-2118, 2010 WL 3766530, at *1-2 (D. Del. Sept. 21, 2010) (“[F]ailure of others after a patent's issue date may be more persuasive than failures that occur before.”). For example, Petitioner BOE proposed a scan driver circuit in 2017 with over 25 transistors and at least three clock signal lines. Ex. 2059, ¶¶134-136.

Ex. 2052, Fig. 3



In January 2022, Petitioner BOE and Hefei BOE proposed another scan driver stage circuit—this time with 4 clock signals and 16 transistors.

Ex. 2053, Fig. 4



[REDACTED]

SDC implemented the claimed inventions of the '593 Patent for the first time in the AMOLED display for the Galaxy S4, which received wide acclaim. Ex. 2059, ¶138; Ex. 2044, ¶7; *see* Ex. 2054, 1-2 (praising Galaxy S4 for its “incredibly small bezel” which is “0.03 inches narrower than the Samsung Galaxy S III”); Ex. 2055, 2; Ex. 2056, 4.

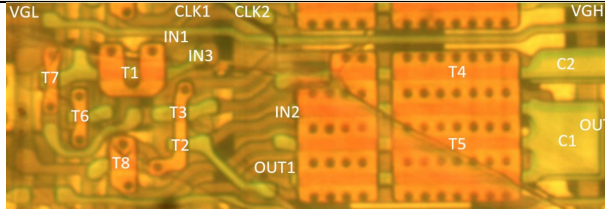
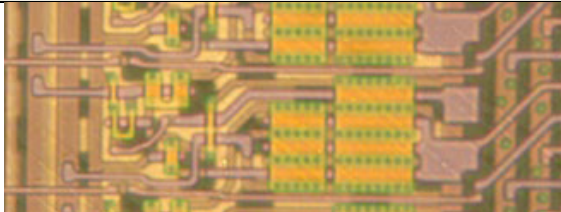
B. Copying further confirms non-obviousness.

Widespread copying further supports non-obviousness. Ex. 2059, ¶¶139-144. Copying is evident from teardowns of commercially available AMOLED display products. These teardowns show that other companies are not just infringing, but have fashioned near identical replicas of SDC’s scan driver stage circuits down to the physical layout and shapes of the circuit elements. Ex. 2059, ¶¶140-144. As Dr. Wolfe explains, the stage circuits in these AMOLED products are so similar,



including in their physical layout, to the patented stage circuits in SDC's products that they can only be reasonably explained by the deliberate copying of SDC's commercially available AMOLED products by persons with access to those products or SDC confidential technical information. Ex. 2059, ¶143. This indicates the makers of these products "had access to, and borrowed from" SDC's patented technology. *Institut Pasteur v. Focarino*, 738 F.3d 1337, 1346, 1348 (Fed. Cir. 2013).

For example, BOE copied SDC's scan driver stage circuits in commercializing AMOLED displays for products such as the iPhone. Ex. 2059, ¶140. The stage circuit in Mianyang BOE's AMOLED display for the iPhone 12 copies SDC's patented stage circuit, as illustrated below in the side-by-side annotated comparison of teardown images of stage circuits in a SDC AMOLED display (Galaxy S22Ultra) (Ex. 2024, 8) and a Mianyang BOE AMOLED display (iPhone 12) (Ex. 2045, 32).

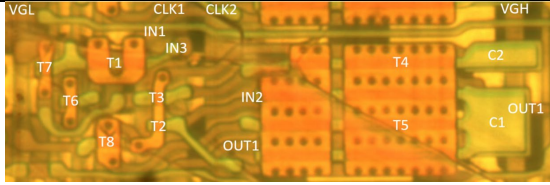
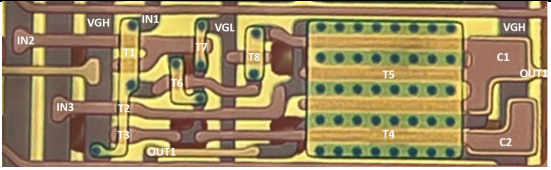
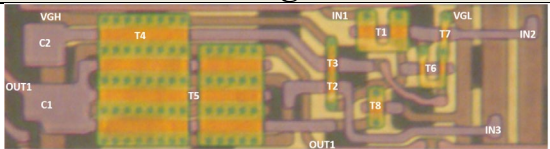
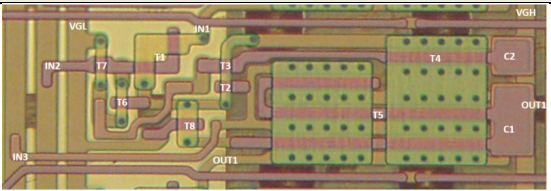
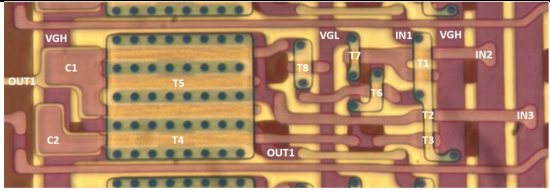
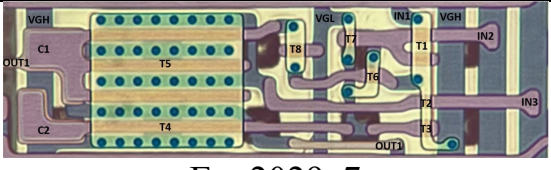
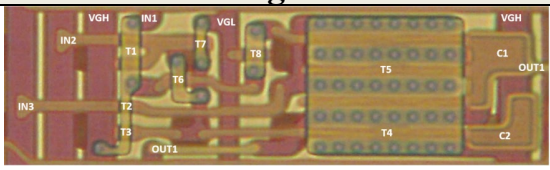
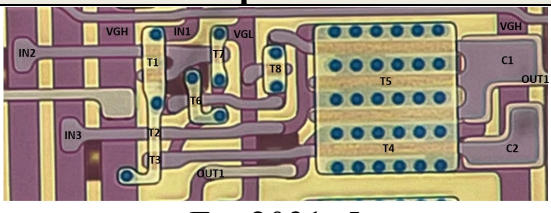
SDC AMOLED (Galaxy S22Ultra)	Mianyang BOE AMOLED (iPhone 12)
	
Ex. 2024, 8	Ex. 2045, 32

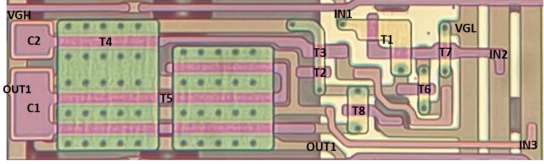
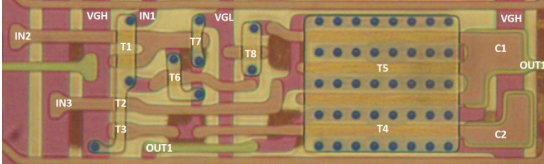
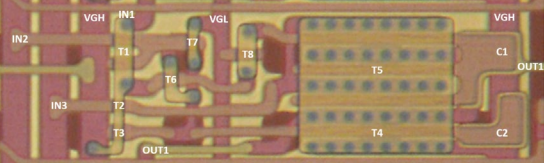
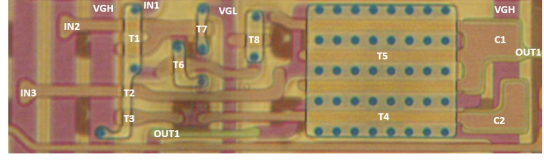
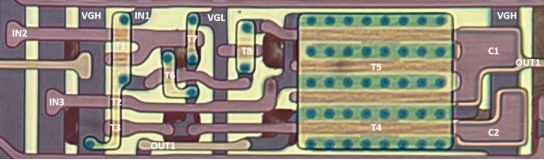
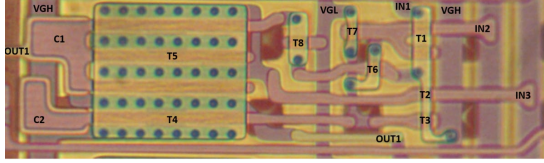
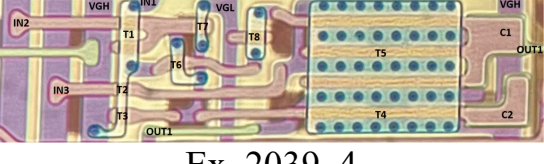
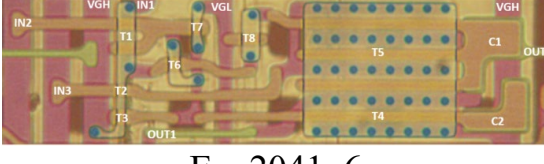
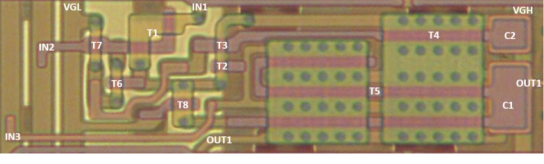
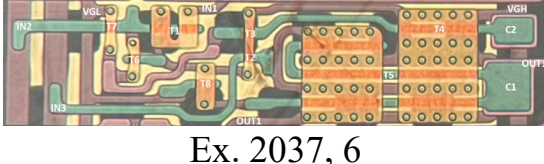
Further, BOE’s patent filings demonstrate it tried to develop its own stage circuits (Exs. 2052-2053). Yet to commercialize AMOLED displays, BOE resorted to copying SDC. Ex. 2059, ¶¶140-141. The failure of its own efforts, coupled with its copying, strongly support nonobviousness.

The widespread copying is further apparent from samples of AMOLED displays sold by numerous vendors of replacement AMOLED displays for mobile phones. Again, these not only infringe the claims (*see, e.g.*, Ex. 2046 (chart mapping claims to Mengtor AMOLED Display)⁴; Section V.C’s claim chart), they are so similar to those of SDC, down to their physical layouts and shapes of circuit elements, that they show copying. Ex. 2059, ¶¶142-144. Exemplary teardown

⁴ The scan driver stage circuit used in the Mengtor product is representative of the circuits used in all of the replacement display products discussed herein. The products all practice the claims for the same reasons. Ex. 2059, ¶144.

images of such products are shown below alongside a teardown image of the patented SDC stage circuit incorporated in the Galaxy S22Ultra smartphone.

SDC AMOLED (Galaxy S22Ultra)  Ex. 2024, 8	MobileSentrix  Ex. 2025, 9
Mengtor  Ex. 2026, 5	Phone LCD Parts  Ex. 2027, 5
Mobile Defenders  Ex. 2028, 6	Injured Gadgets  Ex. 2029, 7
Gadgetfix  Ex. 2030, 5	Group Vertical  Ex. 2031, 5

eTech Parts Plus  Ex. 2032, 4	Parts4Cells  Ex. 2033, 4
SEGMobile  Ex. 2034, 4	Captain Mobile Parts  Ex. 2035, 4
Repairs Universe  Ex. 2036, 5	Fixez  Ex. 2038, 6
Wholesale Gadget Parts  Ex. 2039, 4	DFW Cellphone and Parts  Ex. 2041, 6
Parts4LCD  Ex. 2040, 5	SourcelyPlus  Ex. 2037, 6

C. There is a strong nexus between the objective indicia and the claimed inventions.

A strong nexus exists between the objective evidence and the claimed inventions. “[A] nexus analysis need not be limited to a discussion of only novel



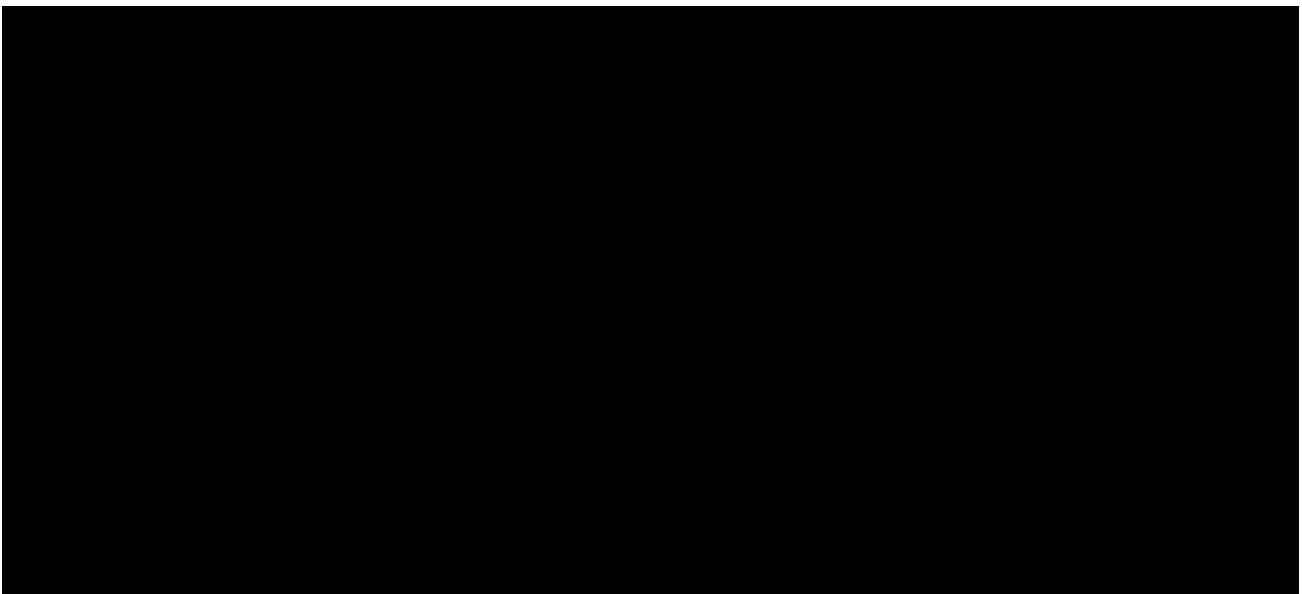
features. It is instead important to consider ‘the invention as a whole,’ rather than on a ‘limitation-by-limitation’ basis.” *Volvo Penta of the Americas v. Brunswick Corp.*, 81 F.4th 1202, 1212 (Fed. Cir. 2023).

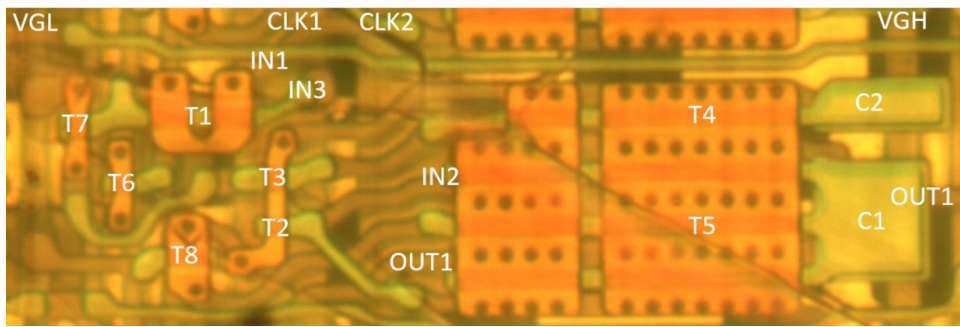
The ’593 Patent’s inventions allow for reductions in “dead space” around a display through a structure that decreases the number of required signal lines. Ex. 2059, ¶¶145-147. The ’593 Patent’s circuits do not require an initialization signal for each stage by having the output of one stage lead to the input of the next. Ex. 1001, 4:61-8:17, Fig. 3. For instance, the claims recite “a first input terminal” (e.g., claims 1, 15) that “receives an output signal of a previous stage circuit” (claim 2) or “receives a scan signal of a previous stage circuit” (claim 17). Moreover, the ’593 Patent’s stage circuits only use two clock signals. Ex. 1001, 4:61-8:17, Fig. 3. The claims recite, for example, a “second input terminal” (e.g., claims 1, 15) which “receives a first clock signal” (claim 2), and a “third input terminal” (e.g., claims 1, 15) which “receives a second clock signal” (claim 2). *See also, e.g.*, claim 18 (“third input terminals of odd stage circuits receive a second clock signal ... third input terminals of even stage circuits receive the first clock signal”). By reducing the number of input signals compared to conventional designs, these circuits improve timing, reduce complexity, including the overall footprint of the circuit, and improve stability. *See* Ex. 1001, 9:12-26.

[REDACTED]

Implementing the scan driver stage circuits of the '593 Patent, SDC successfully introduced AMOLED displays with significantly narrowed bezels, beginning with the display for the Galaxy S4. Ex. 2059, ¶138; Ex. 2044, ¶7. This unique advantage flows from practicing the inventions.

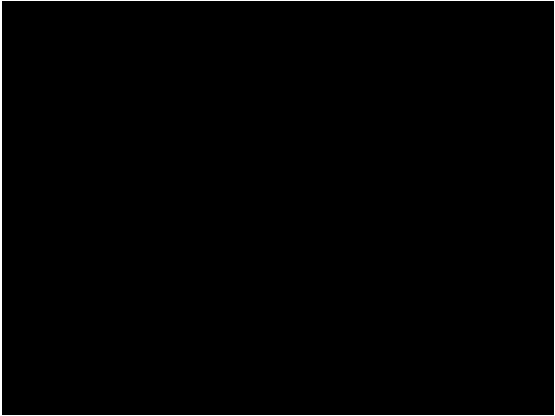
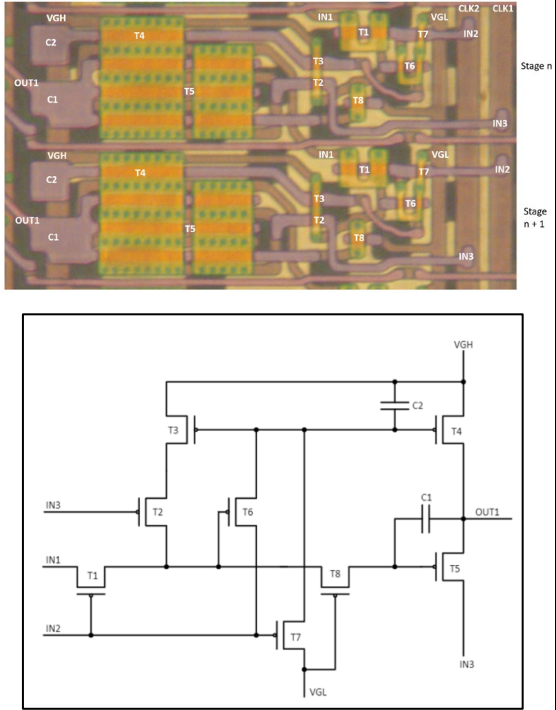
Since its introduction by SDC, the scan driver stage circuit of the '593 Patent has been widely adopted in AMOLED displays for flagship mobile devices, including every Galaxy and iPhone model that has used AMOLED displays. Ex. 2059, ¶¶148-151; Ex. 2044, ¶7. For example, Dr. Wolfe explains that the AMOLED display used in the Galaxy S22 ULTRA product practices all challenged claims. Ex. 2059, ¶¶148-151; Ex. 2044, ¶¶3-9; Ex. 2057 (claim chart mapping claims to AMOLED display in Galaxy S22 ULTRA); Ex. 2058 ([REDACTED]). The circuit diagram and teardown image of the stage circuit used in this product are reproduced below:





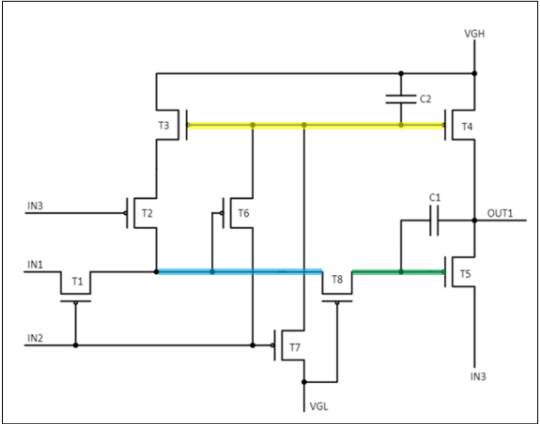
Ex. 2024, 8

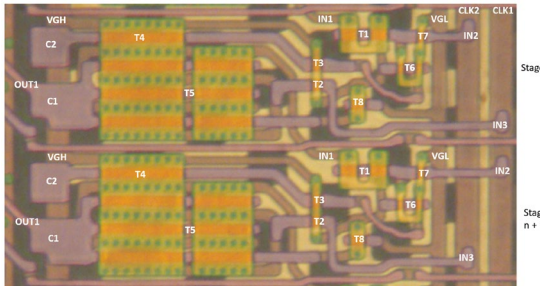
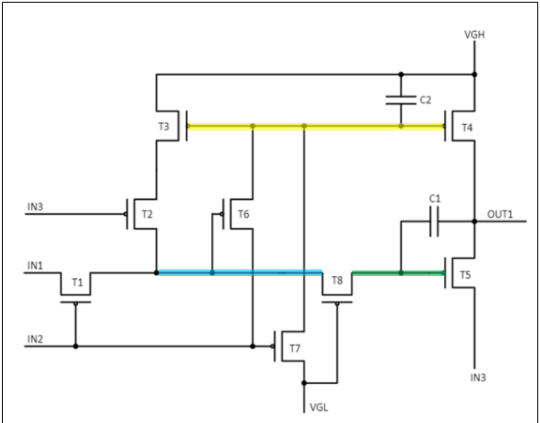
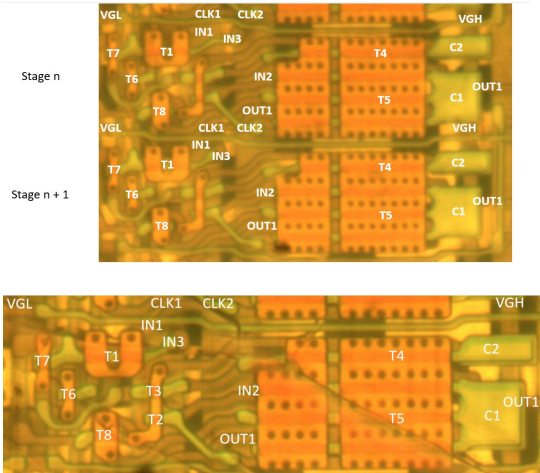
The scan driver stage circuits of the '593 Patent have also been widely copied, as discussed in Section V.B. Ex. 2059, ¶¶139-144. The below chart illustrates how the SDC AMOLED display used in the Galaxy S22 Ultra product (left column) and copycat displays, *e.g.*, Mengtor (right column), practice the claims. The stage circuits used in the Galaxy S22 Ultra and the Mengtor displays are the same. Ex. 2059, ¶144.

Claim	Galaxy S22ULTRA / Mengtor	
1[pre]	The Galaxy S22Ultra and Mengtor products contain a stage circuit having a first input terminal ([REDACTED]) a second input terminal ([REDACTED]) a third input terminal ([REDACTED]) and an output terminal ([REDACTED]) as Dr. Wolfe explains. Ex. 2057, 2; Ex. 2046, 2-4.	
		
	Ex. 2058, 55.	Ex. 2026, 5; Equivalent scan driver stage circuit for Mengtor AMOLED Display (“Mengtor Equivalent Circuit”)

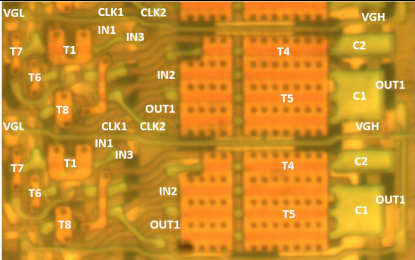
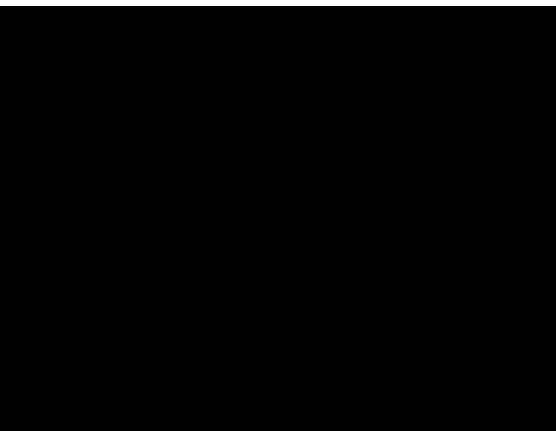
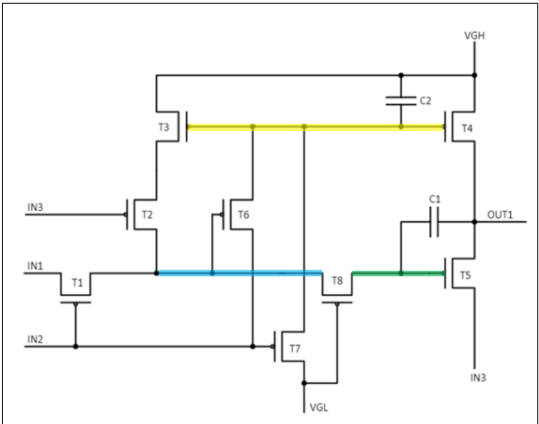
Claim	Galaxy S22ULTRA / Mengtor	
<u>1[b]</u>	The Galaxy S22Ultra and Mengtor products contain a first driver (T1, T2, and T3) to control the voltage of the second node (see 1[a], above), in accordance with signals of the first input terminal ([REDACTED]) the second input terminal ([REDACTED]) and the third input terminal ([REDACTED]) Ex. 2057, 5; Ex. 2046, 8-9. Ex. 2035, 55	
<u>1[c]</u>	The Galaxy S22Ultra and Mengtor products contain a second driver (T4 and T5 / T6 and T7) to control the voltage of the first node (see 1[a], above) in accordance with the signal of the second input terminal ([REDACTED]) and the voltage of the second node (see 1[a], above). Ex. 2057, 6; Ex. 2046, 10-11. Ex. 2035, 55	



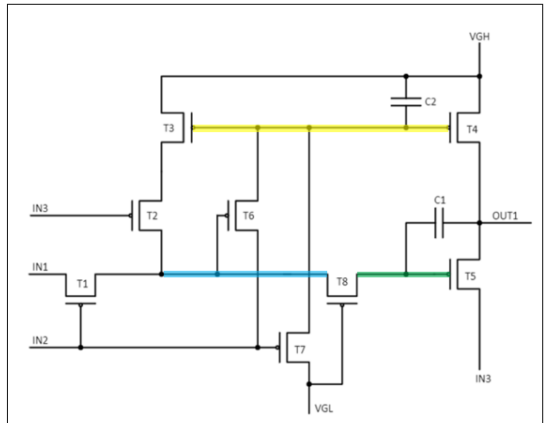
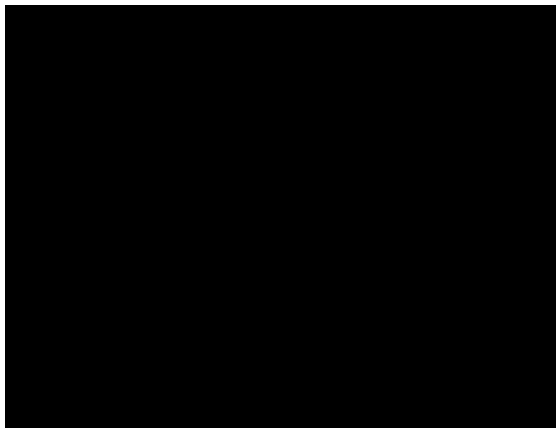
Claim	Galaxy S22ULTRA / Mengtor	
1[d]	The Galaxy S22Ultra and Mengtor products contain a stage circuit wherein the signal of the third input terminal ([REDACTED]) directly controls an on/off operation of a transistor (T3/T2), the transistor included in the first driver (T1, T2, and T3). Ex. 2057, 7; Ex. 2046, 12-13.	
	 Ex. 2035, 55	

Claim	Galaxy S22ULTRA / Mengtor
2[a]	The Galaxy S22Ultra and Mengtor products contain the stage circuit as claimed in claim 1, wherein the first input terminal () receives an output signal () of a previous stage circuit (stage n+1) or a start signal. Ex. 2057, 8-11; Ex. 2046, 14-15.    Ex. 2035, 54-55; Ex. 2026, 5;

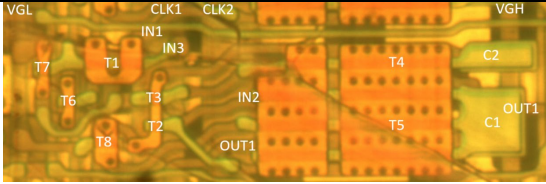
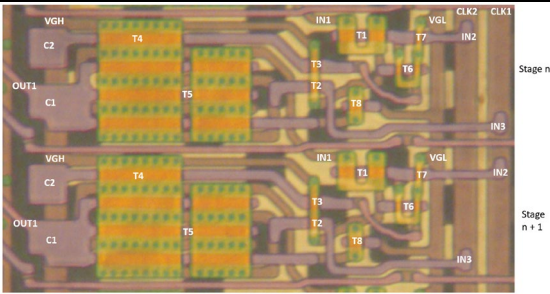
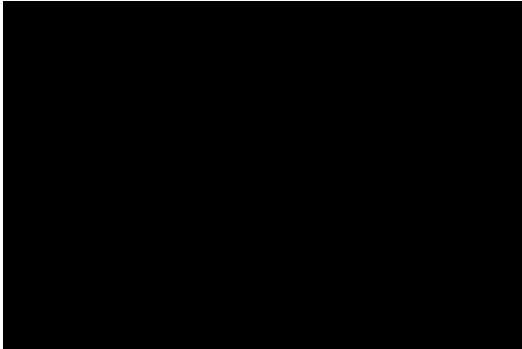
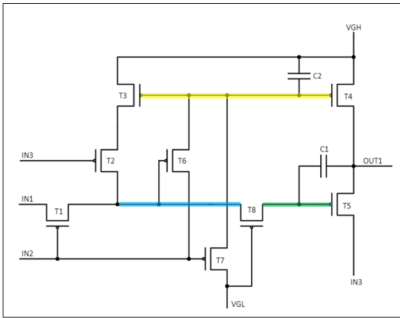


Claim	Galaxy S22ULTRA / Mengtor	
	Ex. 2024, 8	
2[b]	The Galaxy S22Ultra and Mengtor products contain the stage circuit as claimed in claim 1, wherein the second input terminal receives a first clock signal ([REDACTED] Ex. 2057, 12-13; Ex. 2046, 16-17.	
	 Stage n Stage n + 1 Ex. 2035, 54-55; Ex. 2024, 8	

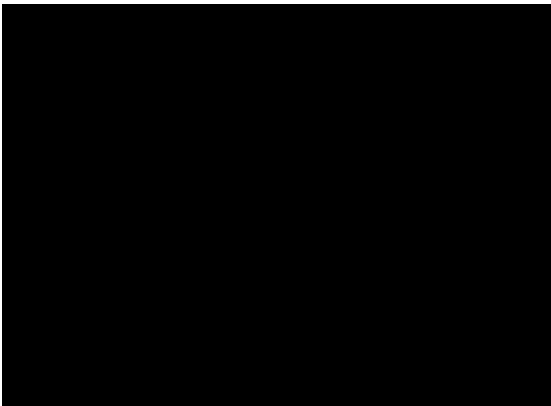
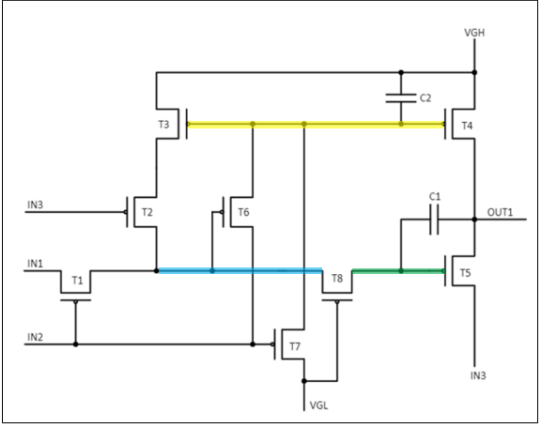
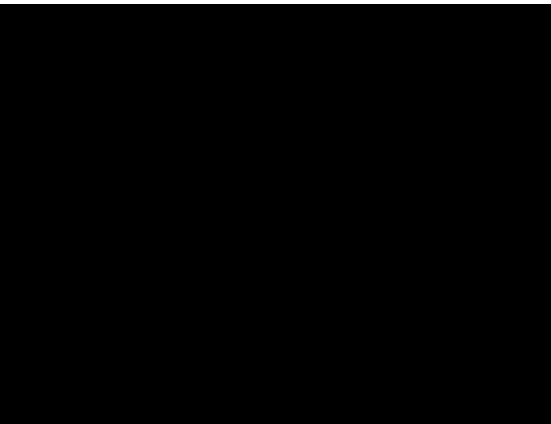
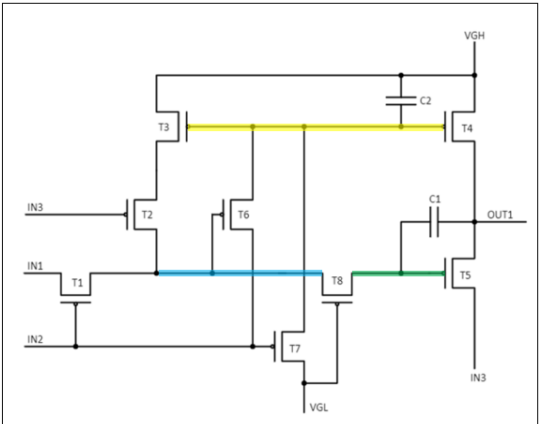
Claim	Galaxy S22ULTRA / Mengtor
<u>2</u>[c]	The Galaxy S22Ultra and Mengtor products contain the stage circuit as claimed in claim 1, wherein the third input terminal receives a second clock signal ([REDACTED] Ex. 2057, 14-15; Ex. 2046, 18-19. Ex. 2035, 54-55; Ex. 2024, 8
<u>3</u>	The Galaxy S22Ultra and Mengtor products contain the stage circuit as claimed in claim 2, wherein the first clock signal ([REDACTED] and the second clock signal ([REDACTED] have the same period and have phases that do not overlap. Ex. 2057, 16-17; Ex. 2046, 20. Ex. 2058, 63; <i>see id.</i>, 64-65.

Claim	Galaxy S22ULTRA / Mengtor
<u>4</u>	The Galaxy S22Ultra and Mengtor products contain the stage circuit as claimed in claim 3, wherein the first clock signal ([REDACTED]) and the second clock signal ([REDACTED]) have a period equal to two horizontal periods 2H and are supplied in different horizontal periods as low signals. Ex. 2057, 18; Ex. 2046, 21. [REDACTED] Ex. 2058, 63; <i>see id.</i>, 64-65.
<u>5</u>	The Galaxy S22Ultra and Mengtor products contain the stage circuit as claimed in claim 2, wherein the start signal ([REDACTED]) is supplied to overlap the first clock signal ([REDACTED]) Ex. 2057, 19; Ex. 2046, 22. See, e.g., Ex. 2058, 63-65 ([REDACTED]).
<u>6[a]</u>	The Galaxy S22Ultra and Mengtor products contain the stage circuit as claimed in claim 2, wherein the first driver includes: a first transistor (T1) between the first input terminal ([REDACTED]) and the second node (see 1[a], above), the first transistor (T1) having a gate electrode coupled to the second input terminal ([REDACTED]) Ex. 2057, 20-21; Ex. 2046, 23. 



Claim	Galaxy S22ULTRA / Mengtor	
	 Ex. 2058, 55; Ex. 2024, 8	 Ex. 2026, 5
6[b]	The Galaxy S22Ultra and Mengtor products contain a second transistor (T3/T2) and a third transistor (T2/T3) serially positioned between the second node (see 1[a], above) and the first power supply ( Ex. 2057, 22; Ex. 2046, 24.	
	 Ex. 2058, 55.	



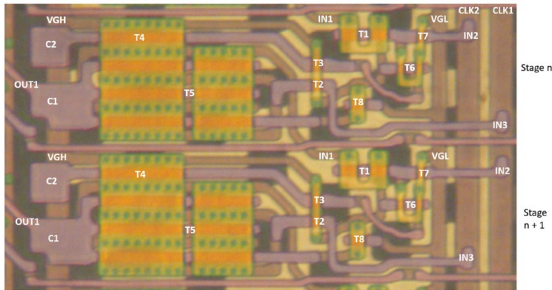
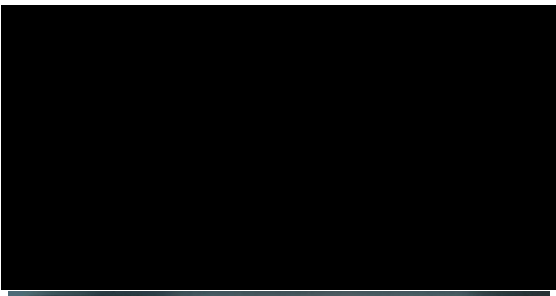
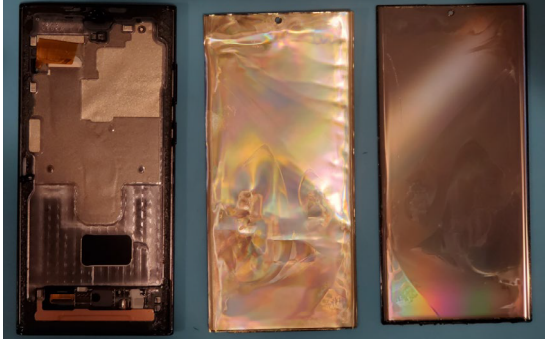
Claim	Galaxy S22ULTRA / Mengtor	
6[c]	The Galaxy S22Ultra and Mengtor products contain a stage circuit wherein a gate electrode of the second transistor (T3/T2) is coupled to the third input terminal ([REDACTED] Ex. 2057, 23; Ex. 2046, 25.  Ex. 2058, 55.	
6[d]	The Galaxy S22Ultra and Mengtor products contain a stage circuit wherein a gate electrode of the third transistor (T2/T3) is coupled to the first node (see 1[a], above). Ex. 2057, 24; Ex. 2046, 26.  Ex. 2058, 55.	

Claim	Galaxy S22ULTRA / Mengtor	
7[a]	The Galaxy S22Ultra and Mengtor products contain the stage circuit as claimed in claim 2, wherein the outputting unit includes: a fourth transistor (T6/T4) between the first power supply ([REDACTED] and the output terminal ([REDACTED] the fourth transistor (T6/T4) having a gate electrode coupled to the first node (see 1[a], above). Ex. 2057, 25; Ex. 2046, 27. Ex. 2058, 55. See also id., 39.	
7[b]	The Galaxy S22Ultra and Mengtor products contain a fifth transistor (T7/T5) between the output terminal ([REDACTED] and the third input terminal ([REDACTED] the fifth transistor (T7/T5) having a gate electrode coupled to the second node (see 1[a], above). Ex. 2057, 26; Ex. 2046, 28. Ex. 2058, 55.	

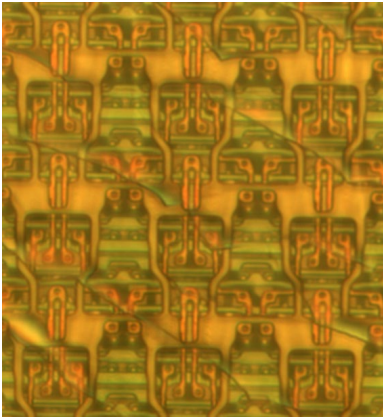
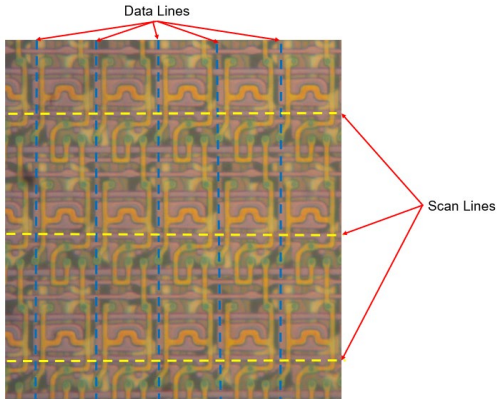
Claim	Galaxy S22ULTRA / Mengtor	
7[c]	The Galaxy S22Ultra and Mengtor products contain a first capacitor ([REDACTED]) between the second node (see 1[a], above) and the output terminal ([REDACTED]) Ex. 2057, 27; Ex. 2046, 29. Ex. 2058, 55.	
7[d]	The Galaxy S22Ultra and Mengtor products contain a second capacitor ([REDACTED]) between the first node (see 1[a], above) and the first power supply ([REDACTED]) Ex. 2057, 28; Ex. 2046, 30. Ex. 2058, 55.	



Claim	Galaxy S22ULTRA / Mengtor	
8[a]	The Galaxy S22Ultra and Mengtor products contain the stage circuit as claimed in claim 2, wherein the second driver includes: a sixth transistor (T4/T6) between the first node (see 1[a], above) and the second input terminal ([REDACTED] the sixth transistor (T4/T6) having a gate electrode coupled to the second node (see 1[a], above). Ex. 2057, 29; Ex. 2046, 31. Ex. 2058, 55.	
8[b]	The Galaxy S22Ultra and Mengtor products contain a seventh transistor (T5/T7) between the first node (see 1[a], above) and a second power supply ([REDACTED] the second power supply ([REDACTED] having a lower voltage than the first power supply ([REDACTED] the seventh transistor (T5/T7) having a gate electrode coupled to the second input terminal ([REDACTED] Ex. 2057, 30-31; Ex. 2046, 32.	

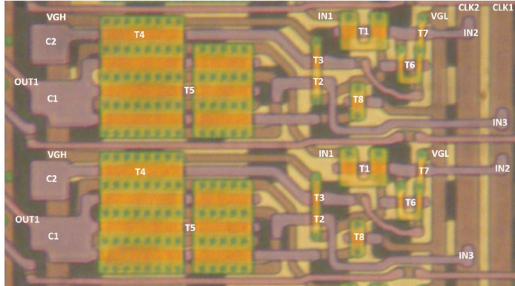
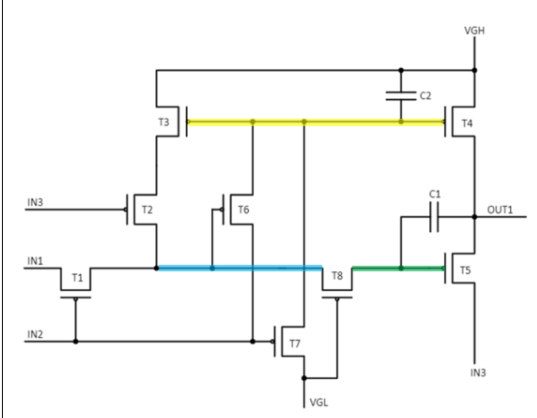
Claim	Galaxy S22ULTRA / Mengtor	
	Ex. 2058, 39 (showing [REDACTED] having lower voltage than [REDACTED] 55.	
<u>14</u>	The Galaxy S22Ultra and Mengtor products contain the stage circuit as claimed in claim 1, wherein the transistor (T3) controls the voltage of the second node (see 1[a], above) according to the on/off operation thereof. Ex. 2057, 32; Ex. 2046, 33.	
	 Ex. 2058, 55.	 Ex. 2026, 5
<u>15[pre]</u>	The Galaxy S22Ultra and Mengtor products contain an OLED display. Ex. 2057, 33-34; Ex. 2046, 34.	
	 	

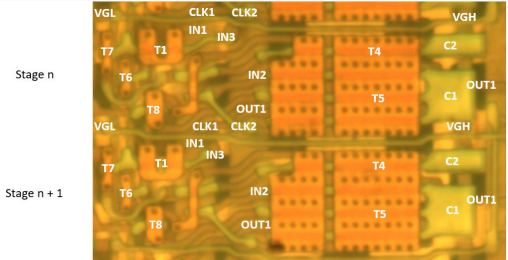
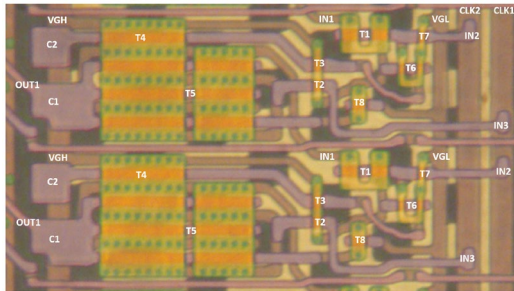
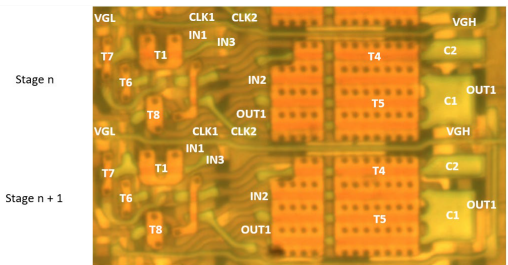
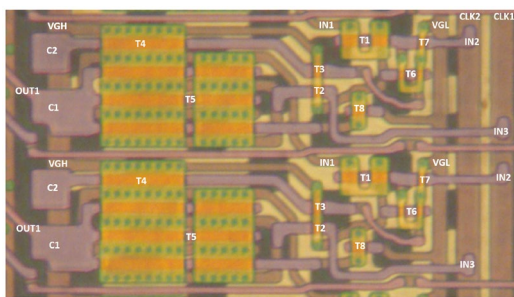


Claim	Galaxy S22ULTRA / Mengtor	
	Ex. 2058, 40; Ex. 2024, 6	Ex. 2026, 3-4
<u>15[a]</u>	The Galaxy S22Ultra and Mengtor products contain pixels positioned in regions partitioned by scan/data lines. Ex. 2057, 35; Ex. 2046, 35.	
	 Ex. 2024, 7.	 Ex. 2026, 5
<u>15[b]</u>	The Galaxy S22Ultra and Mengtor products contain a data driver for supplying data signals to the pixels through the data lines. Ex. 2057, 36; Ex. 2046, 36.	
	 Ex. 2024, 7.	 Ex. 2026, 7

Claim	Galaxy S22ULTRA / Mengtor	
15[c]	The Galaxy S22Ultra and Mengtor products contain a scan driver for supplying scan signals to the pixels through the scan lines, the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals and having a first input terminal ([REDACTED]) a second input terminal ([REDACTED]) a third input terminal ([REDACTED]) and an output terminal ([REDACTED]) wherein each of the stage circuits includes. Ex. 2057, 37-39; Ex. 2046, 37-39.	
	Ex. 2058, 54-55; Ex. 2024, 8	Ex. 2026, 5
15[d]-[g]	See analysis for 1[a]-[d], above.	



Claim	Galaxy S22ULTRA / Mengtor	
<u>16</u>	The Galaxy S22Ultra and Mengtor products contain the OLED display as claimed in claim 15, wherein a clock signal supplied to the third input terminal is used as the scan signal. Ex. 2057, 44; Ex. 2046, 44.	 Stage n Stage n + 1  Ex. 2035, 55 Ex. 2026, 5
<u>17</u>	See 2[a], above. Ex. 2057, 45; Ex. 2046, 45.	

Claim	Galaxy S22ULTRA / Mengtor	
18[a]	The Galaxy S22Ultra and Mengtor products contain the OLED display as claimed in claim 17, wherein second input terminals () of odd stage circuits (Stage n) receive a first clock signal and third input terminals () of odd stage circuits (Stage n) receive a second clock signal. Ex. 2057, 46; Ex. 2046, 46.  Ex. 2024, 8.  Ex. 2026, 5	
18[b]	The Galaxy S22Ultra and Mengtor products contain an OLED display as claimed in claim 17, wherein second input terminals () of even stage circuits (Stage n+1) receive the second clock signal and third input terminals () of even stage circuits (Stage n+1) receive the first clock signal. Ex. 2057, 47; Ex. 2046, 47.  Ex. 2024, 8.  Ex. 2026, 5	
19-21, 25	See analysis for claims 4-8. Ex. 2057, 48-59; Ex. 2046, 48.	

See also Ex. 2043, ¶3.

[REDACTED]

The objective evidence is commensurate with the scope of the challenged claims. A scan driver stage circuit having the unique benefits of '593 Patent's invention was unattainable in the prior art, as exemplified by the failures over the years to develop a suitable scan driver circuit that would reduce "dead space" and be widely adopted in commercial AMOLED displays.

VI. Conclusion

The Board should find the challenged claims patentable.

Date: December 12, 2024

Respectfully submitted,

By /David A. Garr

David A. Garr

Registration No.: 74,932

Scott C. Weidenfeller

Registration No.: 54,531

Counsel for Patent Owner

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), I certify that the present paper contains 13,996 words based on the word count indicated by the word-processing program used to generate the paper and excluding those portions exempted by 37 C.F.R. §§ 42.24(a) and (b).

Date: December 12, 2024

/David A. Garr /
David A. Garr
Registration No.: 74,932

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6, I hereby certify that the foregoing Patent Owner's Preliminary Response and accompanying exhibits were served by electronic mail on the following counsel of record for petitioner:⁵

K. Patrick Herman (P52PTABDocket@orrick.com)
Richard F. Martinelli (RFMPTABDocket@orrick.com)
Xiang Wang (XW0PTABDocket@orrick.com)
ORRICK, HERRINGTON & SUTCLIFFE, LLP

Date: December 12, 2024

/David A. Garr /
David A. Garr
Registration No.: 74,932

⁵ As discussed in Patent Owner's Motion to Seal and for Entry of Protective Order (being filed concurrently with this document), in order to ensure compliance with the restrictions on disclosure of NCT Information outside of the United States, Patent Owner is filing the unredacted confidential Patent Owner's Response and confidential exhibits as "Board and Filing Party Only." Patent Owner is serving these confidential materials on Counsel for Petitioner who are located in the United States and have signed acknowledgement letters pursuant to the proposed Protective Order.