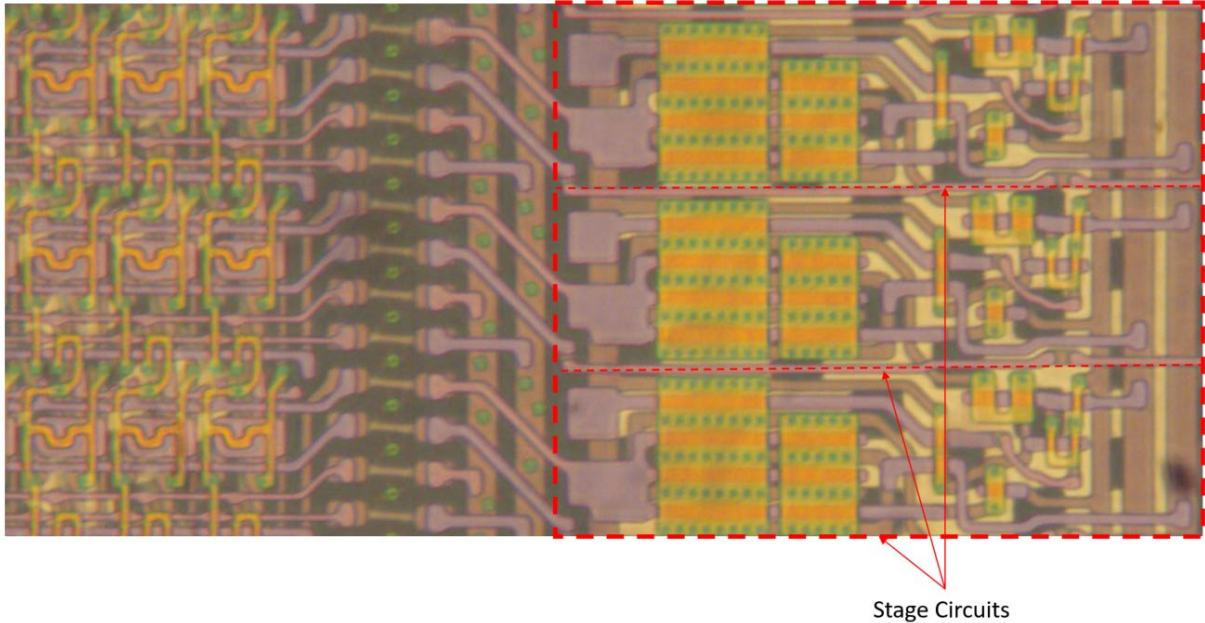
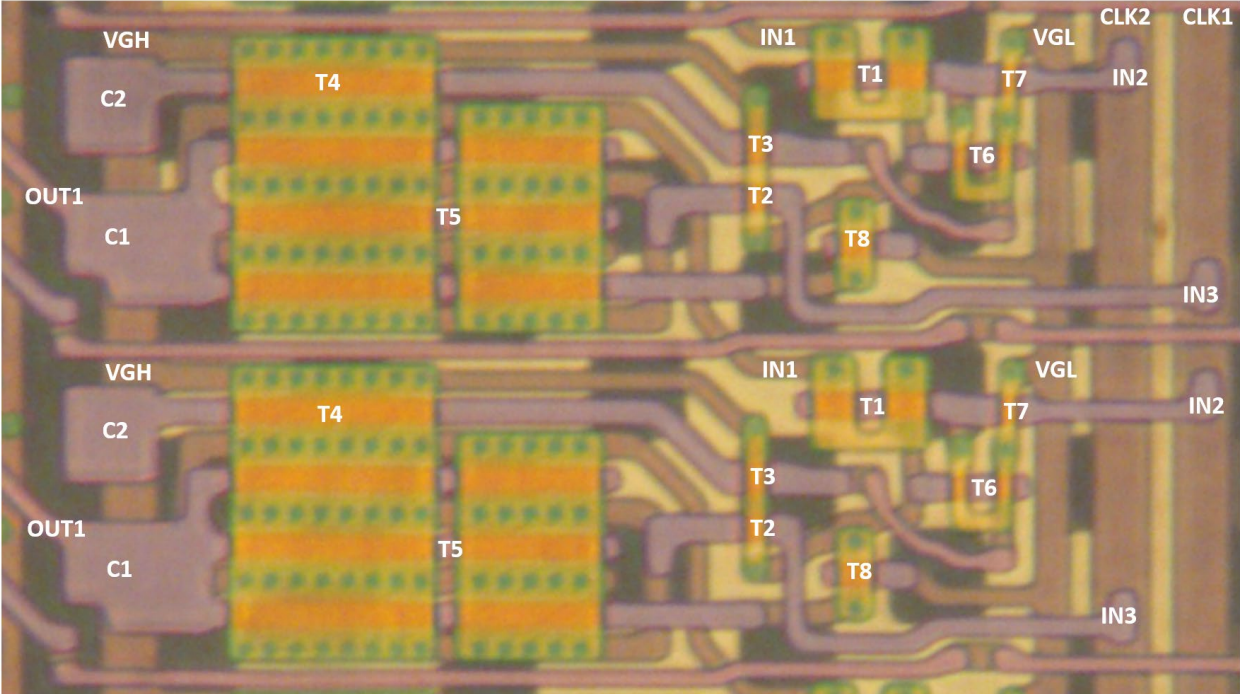
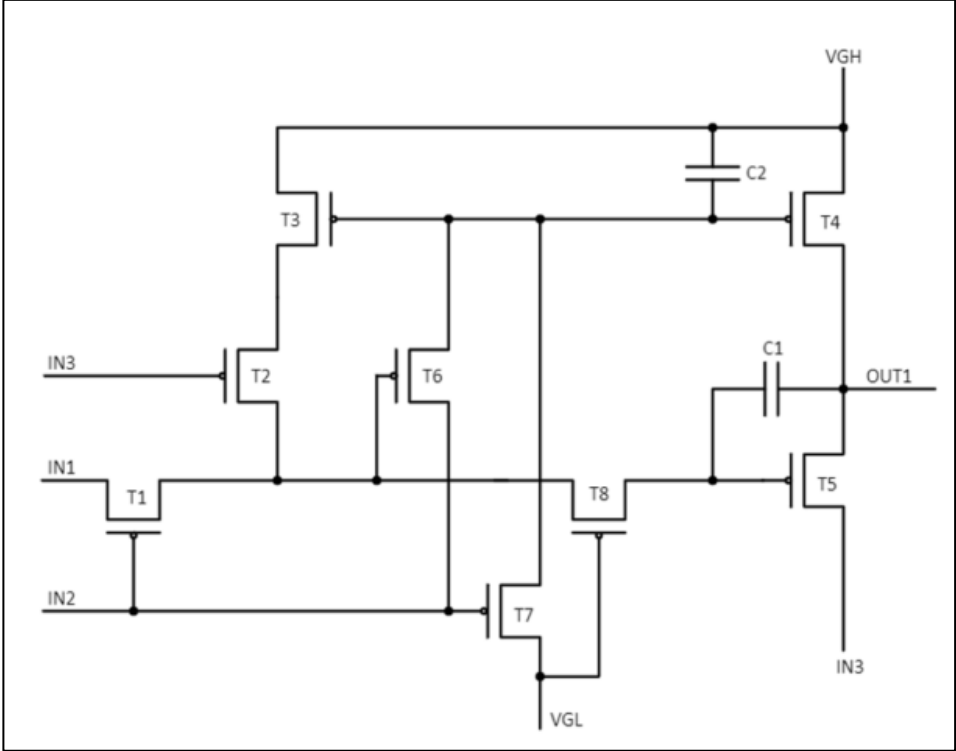


EXHIBIT 2046

CLAIM CHART: AMOLED DISPLAY IN MENGTOR PRODUCT

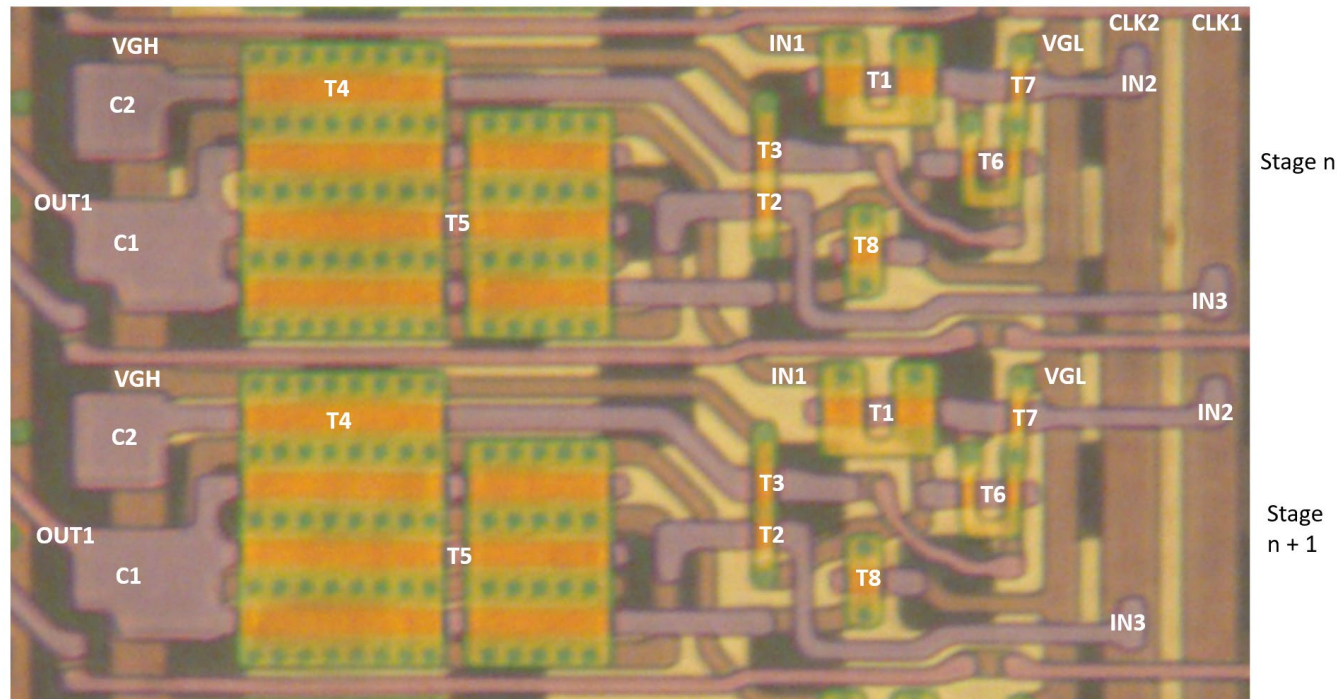
U.S. Patent No. 9,330,593	Mengtor Product
1[preamble] A stage circuit having a first input terminal, a second input terminal, a third input terminal, and an output terminal, the stage circuit comprising:	As shown in the image below, the Mengtor Product contains a scan driver with a plurality of stage circuits (red dashed lines).  Stage Circuits Annotated Exhibit 2026 at 6 (Mengtor Teardown Images)

U.S. Patent No. 9,330,593	Mengtor Product
1[preamble] A stage circuit having a first input terminal, a second input terminal, a third input terminal, and an output terminal, the stage circuit comprising: (<i>cont'd</i>)	As shown in the annotated image below, a stage circuit of the Mengtor Product has a first input terminal (e.g., IN1), a second input terminal (e.g., IN2), a third input terminal (e.g., IN3), and an output terminal (e.g., OUT1).  Stage n Stage n + 1 Annotated Exhibit 2026 at 6 (Mengtor Teardown Images)

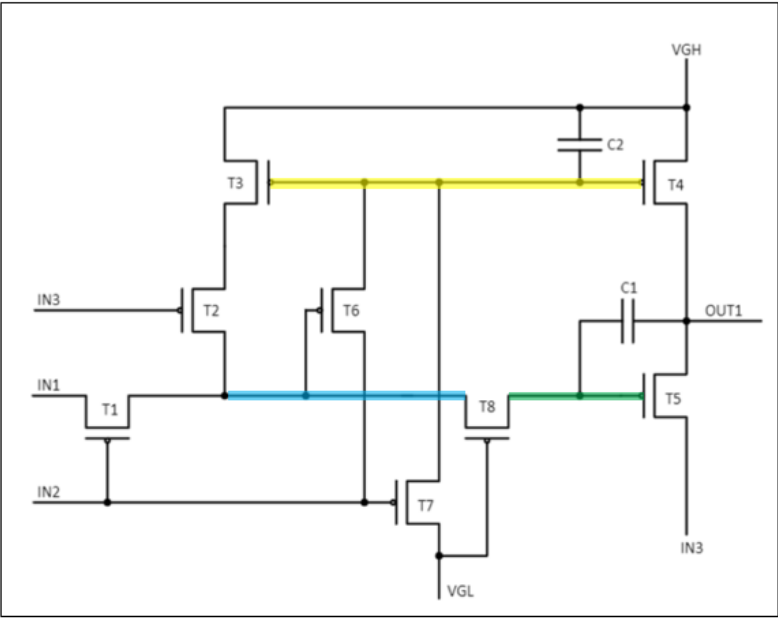
U.S. Patent No. 9,330,593	Mengtor Product
1[preamble] A stage circuit having a first input terminal, a second input terminal, a third input terminal, and an output terminal, the stage circuit comprising: (<i>cont'd</i>)	The figure below is a representative circuit diagram of the one stage of the scan driver stage circuit of the Mengtor Product (“Mengtor Equivalent Circuit”): 

1[a] an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node;

The Mengtor Product contains a stage circuit that has an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node. As shown in the annotated image below, the outputting unit comprises at least transistors **T4** and **T5** and capacitors **C1** and **C2**. The outputting unit has a first node between the gates of transistors **T3** and **T4** and a second node between the gate of transistor **T5** and the output of the first driver (*see claim element 1[b], below*)).



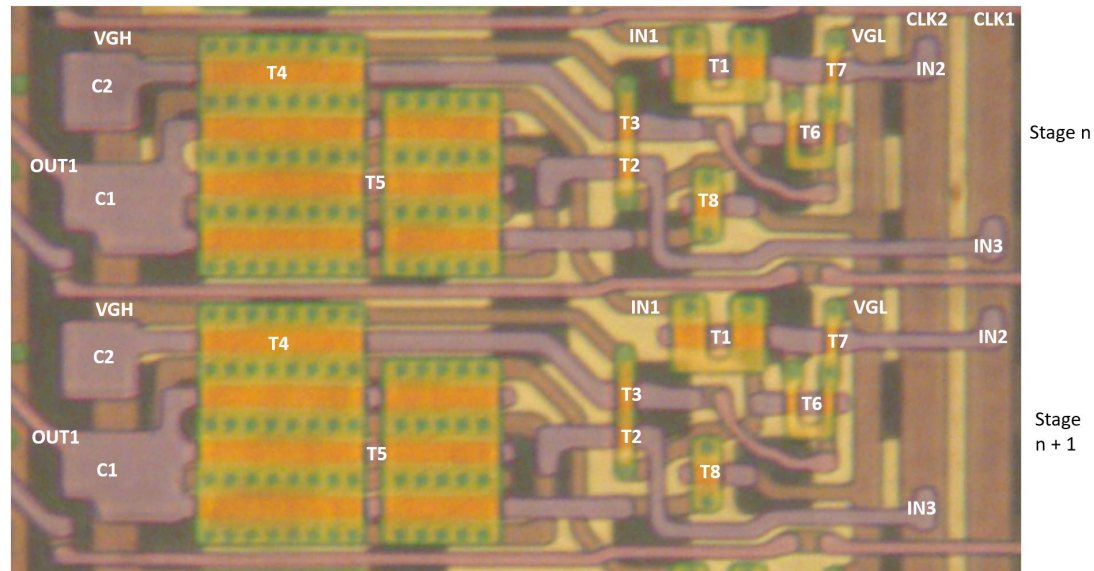
Annotated Exhibit 2026 at 6 (Mengtor Teardown Images)

U.S. Patent No. 9,330,593	Mengtor Product
	For example, in the annotated Mengtor Equivalent Circuit below, the first node is a point or area of interconnection between the gates of transistors T3 and T4 in the region highlighted in yellow. The second node is a point or area of interconnection between the output of the first driver and the source of transistor T8 in the region highlighted in blue (or can also be between the drain of transistor T8 and the gate of transistor T5 in the region highlighted in green). 

U.S. Patent No. 9,330,593	Mengtor Product
1[a] an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node; (<i>cont'd</i>)	Mengtor Equivalent Circuit As shown in the annotated circuit diagram above, the outputting unit supplies the voltage of a first power supply (e.g., VGH) to the output terminal (e.g., OUT1), according to a voltage applied to the first node, and a signal of the third input terminal (e.g., IN3) to the output terminal (e.g., OUT1) according to a voltage applied to the second node. For example, as shown in the annotated circuit diagram above, transistors T4 and T5 supply a voltage to OUT1 depending upon the voltage between the gates of transistors T3 and T4 and the voltage between the gate of transistor T5 and the output of the first driver (<i>see</i> claim element 1[b], below). VGH is coupled to an electrode of transistor T4, such that when a voltage is applied to the node between the gates of transistors T3 and T4, transistor T4 is turned on and VGH is supplied to OUT1. OUT1 is coupled to an electrode of transistor T5 such that when a voltage is applied to a node between the gate of transistor T5 and the output of the first driver, transistor T5 is turned on and IN3 is supplied to OUT1.

1[b] a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal; and

The Mengtor Product contains a stage circuit that has a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal. As shown in the annotated image below, the stage circuit contains a first driver comprising at least transistors **T1**, **T2**, and **T3**. The first input terminal (e.g., **IN1**) is coupled to an electrode of transistor **T1**. The second input terminal (e.g., **IN2**) is coupled to the gate electrode of transistor **T1**. The third input terminal (e.g., **IN3**) is coupled to the gate electrode of transistor **T2**. The signals of the first input terminal (e.g., **IN1**), the second input terminal (e.g., **IN2**), and third input terminal (e.g., **IN3**) control the voltage of the second node (*see* claim element 1[a], above) based on the respective voltages applied at the gate electrodes of transistors **T1**, **T2**, and **T3**.

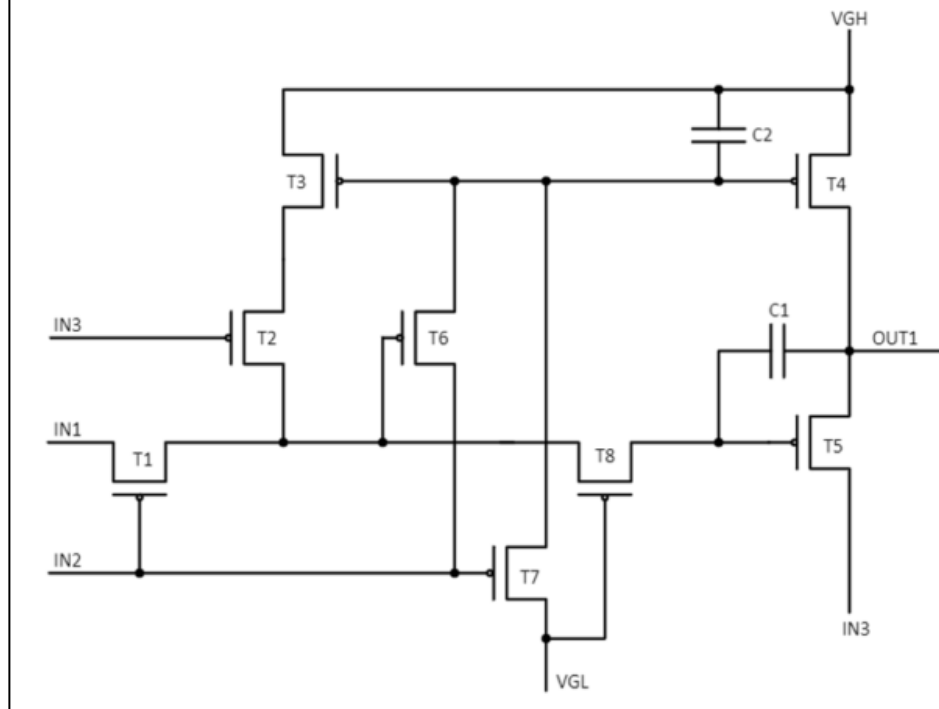


Annotated Exhibit 2026 at 6 (Mengtor Teardown Images)

For example, as shown in the annotated image above, **IN1** is coupled to transistor **T1**, and the gate electrodes of transistor **T1** are coupled to **IN2**. The transistors **T2** and **T3** are coupled in series to the drain of transistor **T1**, and **IN3** is coupled to the gate electrode of transistor **T2**. The signals applied to **IN1**, **IN2**, and **IN3** control the voltage between the output of the first driver and the gate of transistor **T5**.

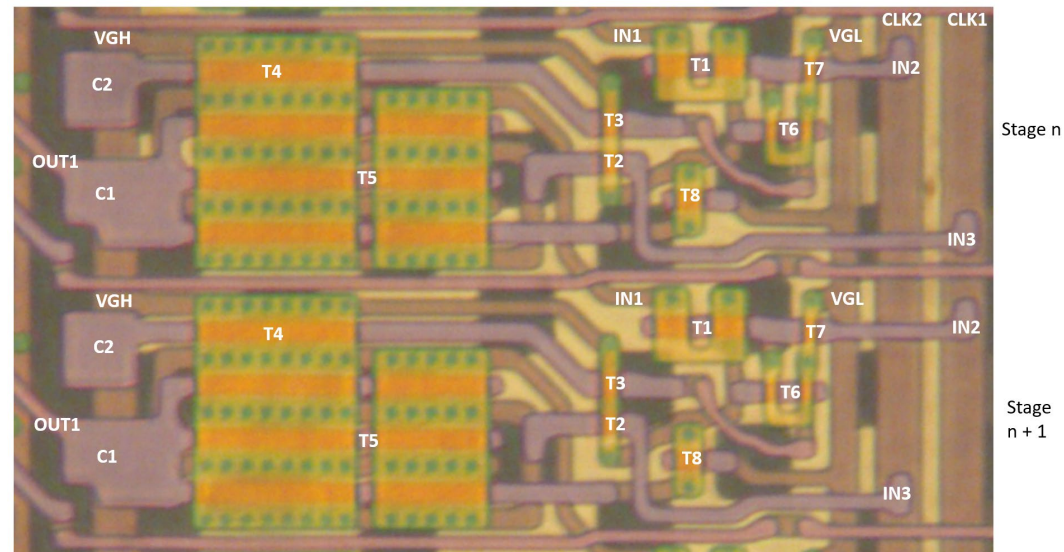
U.S. Patent No.
9,330,593

Mengtor Product



1[c] a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node,

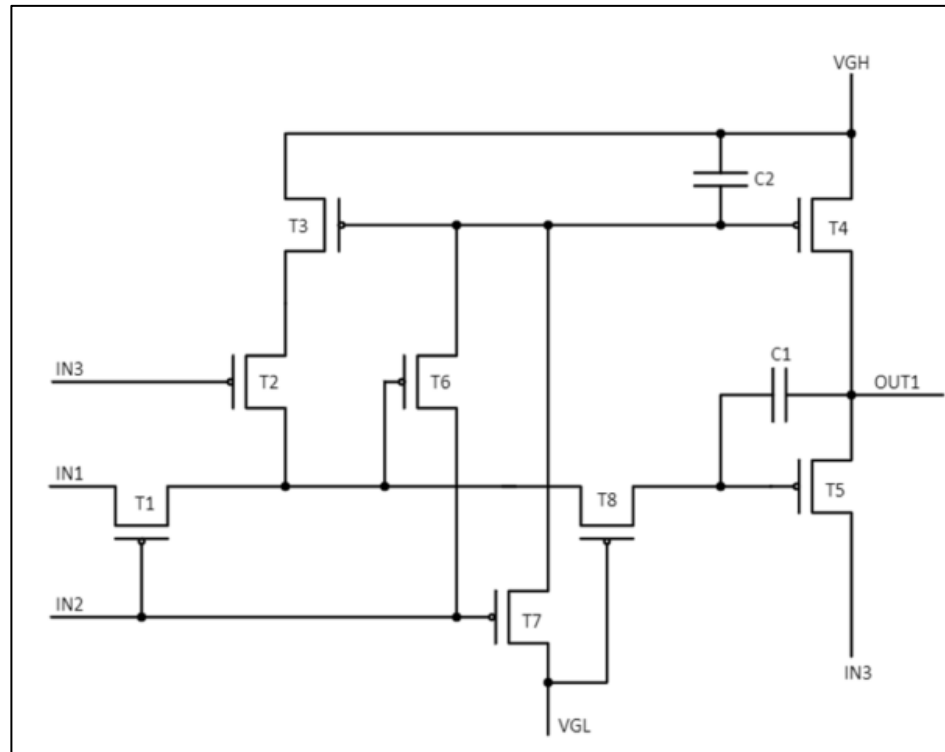
The Mengtor Product contains a stage circuit that has a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node. As shown in the annotated image below, the stage circuit contains a second driver comprising at least transistors **T6** and **T7**. The signal of the second input terminal (e.g., **IN2**) is applied to the gate electrode of transistor **T7**, which controls the voltage of the first node (e.g., the voltage between the gates of transistors **T3** and **T4**). The voltage of the second node (e.g., the voltage between the gate electrode of transistor **T5** and the output of the first driver) is applied to the gate electrode of transistor **T6**, which controls the voltage of the first node (e.g., the voltage between the gate electrodes of transistors **T3** and **T4**).



Annotated Exhibit 2026 at 6 (Mengtor Teardown Images)

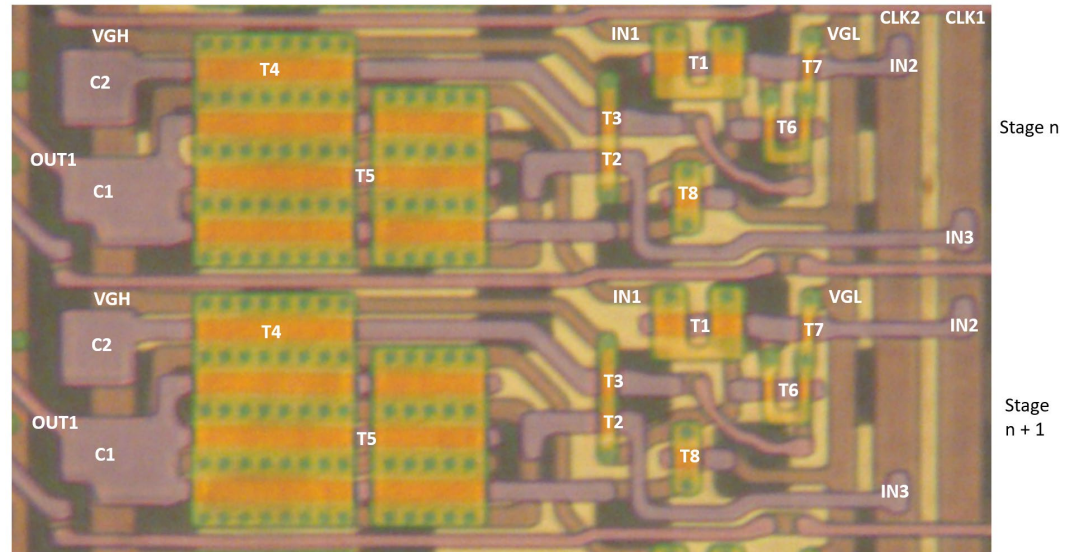
For example, as shown in the annotated image above, **IN2** is coupled to the gate of transistor **T7**, which is coupled between **VGL** and the node between the gates of transistors **T3** and **T4**. The signal at **IN2** controls whether **VGL** is applied between the gates of transistors **T3** and **T4**. The transistor **T6** is coupled between the gates of transistors **T3** and **T4** and **IN2**, and the voltage at the output of the first driver is coupled to the gate of transistor **T6**, thereby controlling when transistor **T6** is on. When

transistor **T6** is on, it couples the node between the gates of transistors **T3** and **T4** to the signal present on **IN2**.



1[d] wherein the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver.

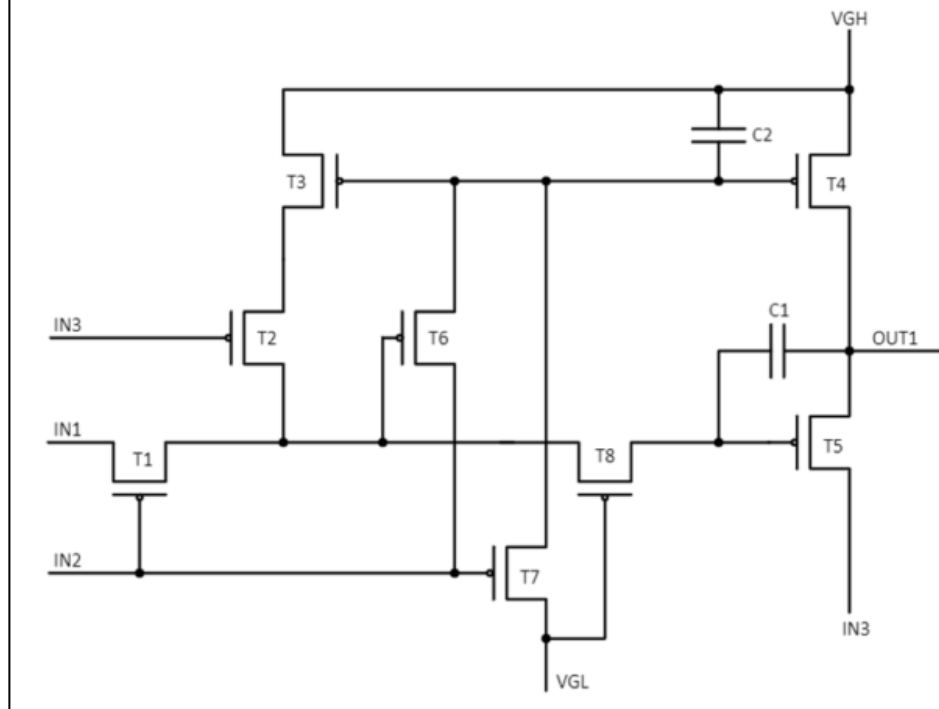
The Mengtor Product contains a stage circuit in which the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver. As shown in the annotated image below, the third input terminal (e.g., **IN3**) is coupled to the gate electrode of transistor **T2** and the signal of the third input terminal directly controls the on/off operation of transistor **T2**. As described above for claim element 1[b], transistor **T2** is included in the first driver.



Annotated Exhibit 2026 at 6 (Mengtor Teardown Images)

U.S. Patent No.
9,330,593

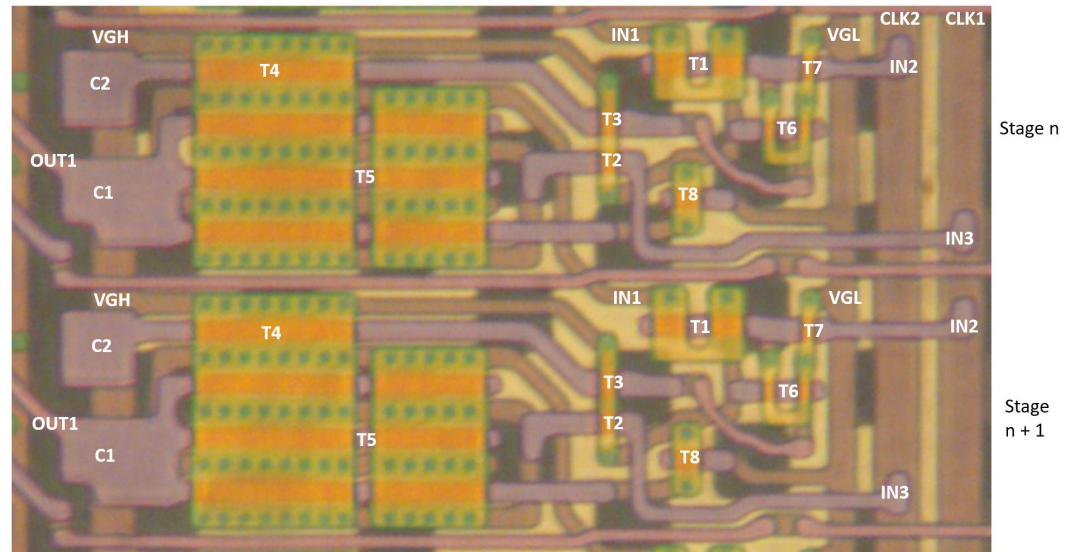
Mengtor Product



2[a] The stage circuit as claimed in claim 1,
wherein the first input terminal receives an output signal of a previous stage circuit or a start signal,

The Mengtor Product contains a stage circuit in which the first input terminal receives an output signal of a previous stage circuit or a start signal.

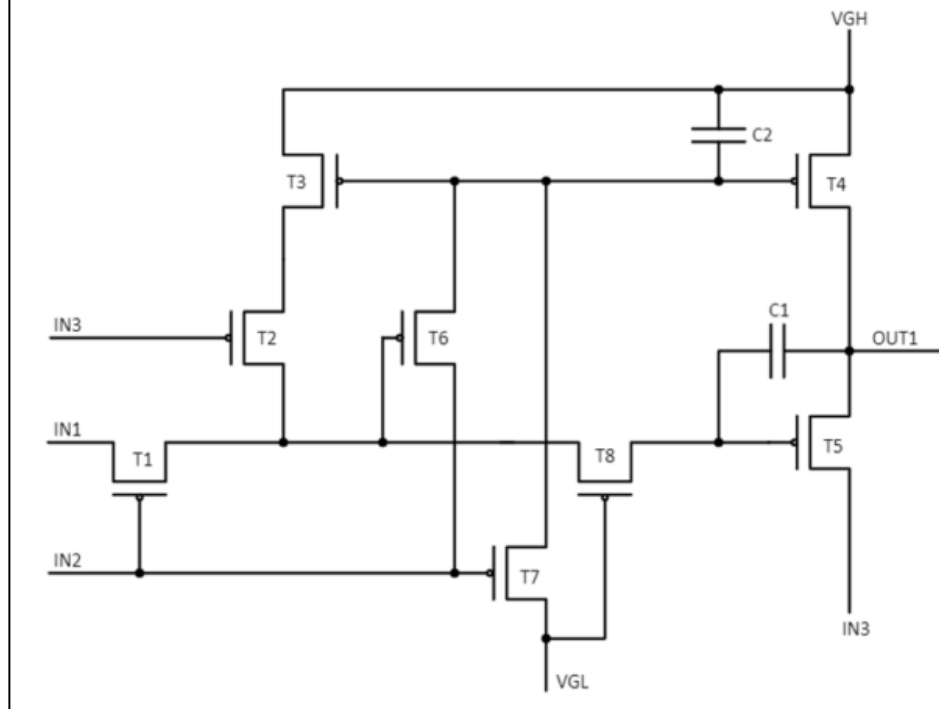
For example, as shown in the annotated image below, the first input terminal of stage $n+1$ receives an output signal of the previous stage, stage n :



Annotated Exhibit 2026 at 6 (Mengtor Teardown Images)

U.S. Patent No.
9,330,593

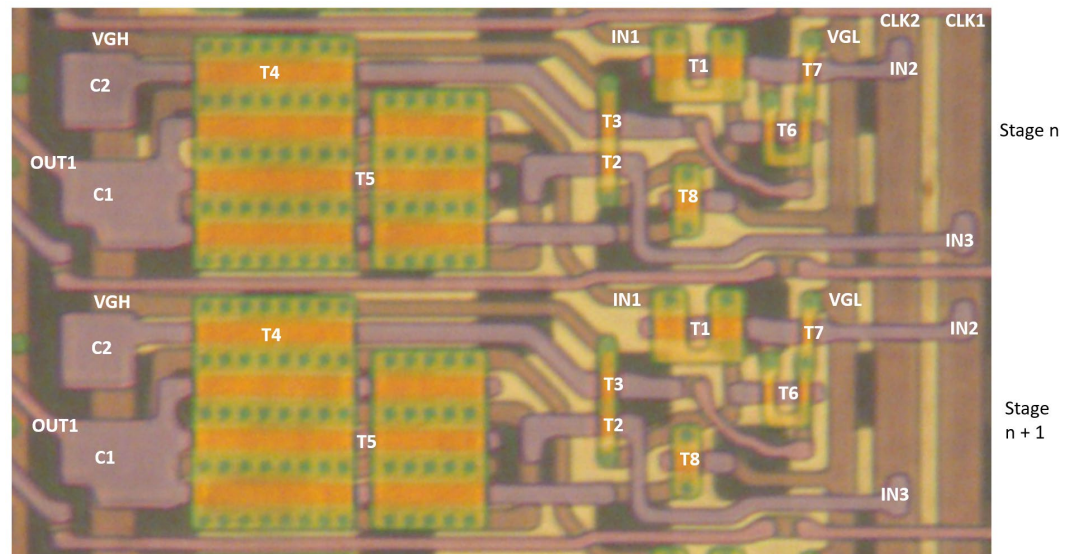
Mengtor Product



2[b] wherein the second input terminal receives a first clock signal, and

The Mengtor Product contains a stage circuit in which the second input terminal receives a first clock signal.

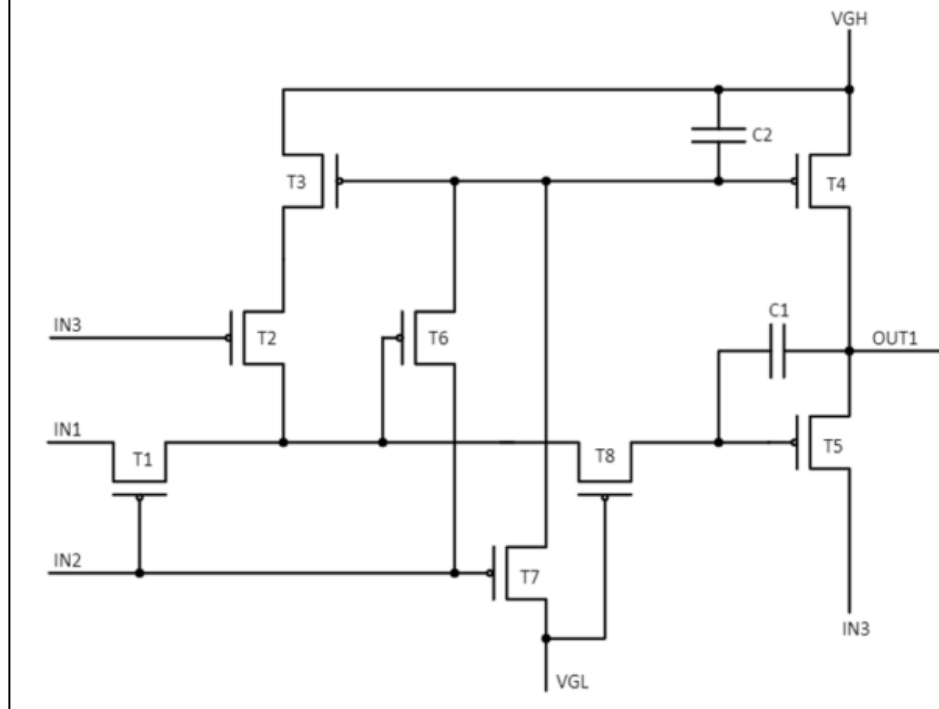
For example, as shown in the annotated image below, the second input terminal IN2 receives a first clock signal, CLK2:



Annotated Exhibit 2026 at 6 (Mengtor Teardown Images)

U.S. Patent No.
9,330,593

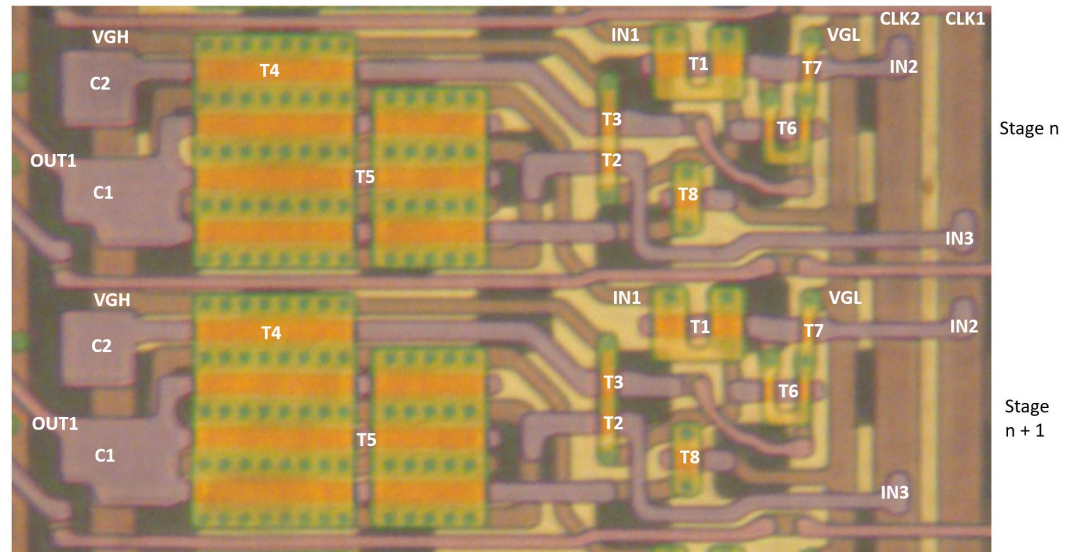
Mengtor Product



2[c] wherein the third input terminal receives a second clock signal.

The Mengtor Product contains a stage circuit in which the third input terminal receives a second clock signal.

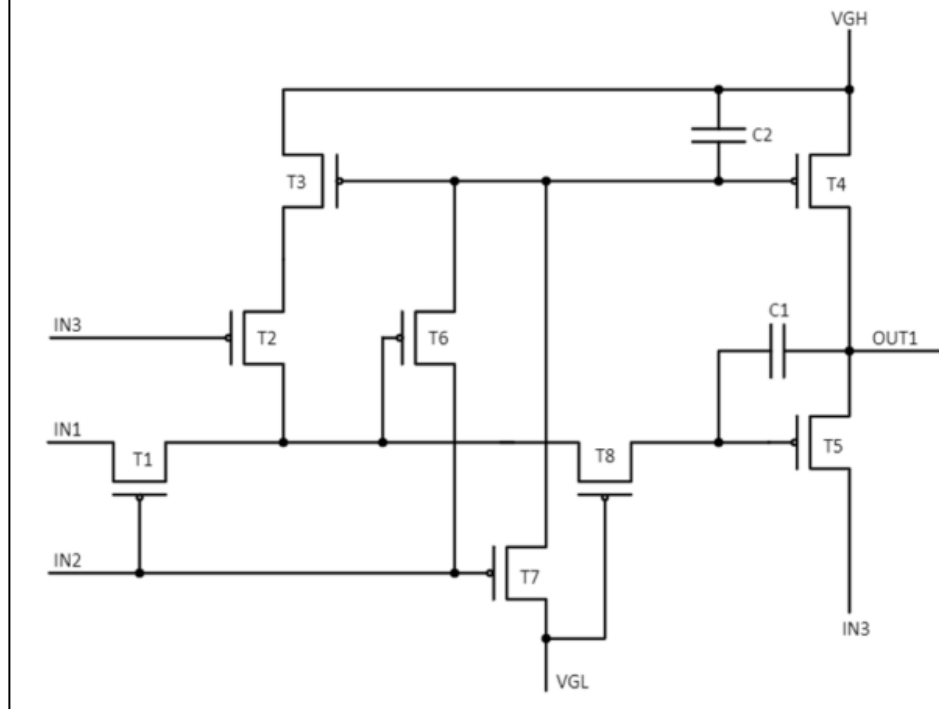
For example, as shown in the annotated image below, the third input terminal IN3 receives a second clock signal, CLK1:



Annotated Exhibit 2026 at 6 (Mengtor Teardown Images)

U.S. Patent No.
9,330,593

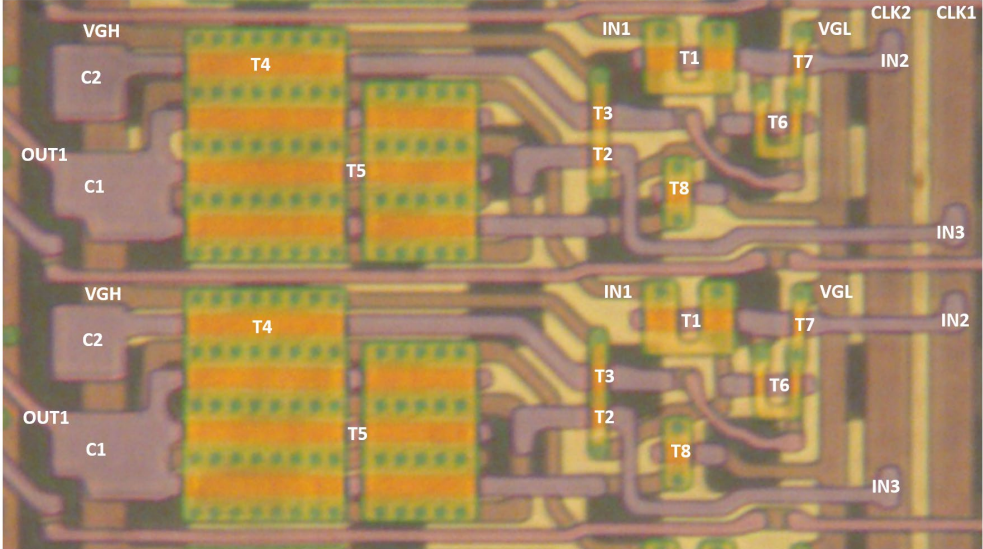
Mengtor Product

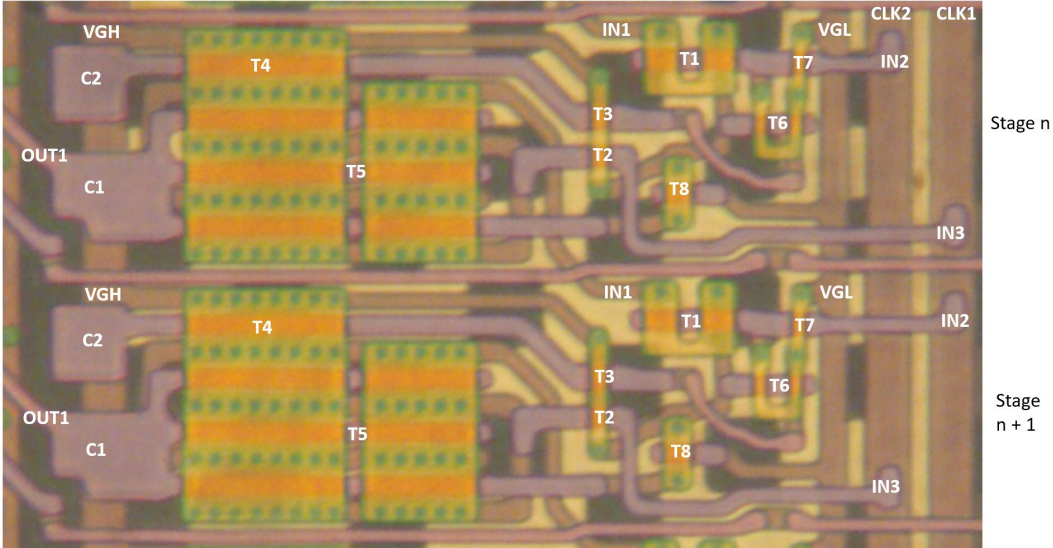


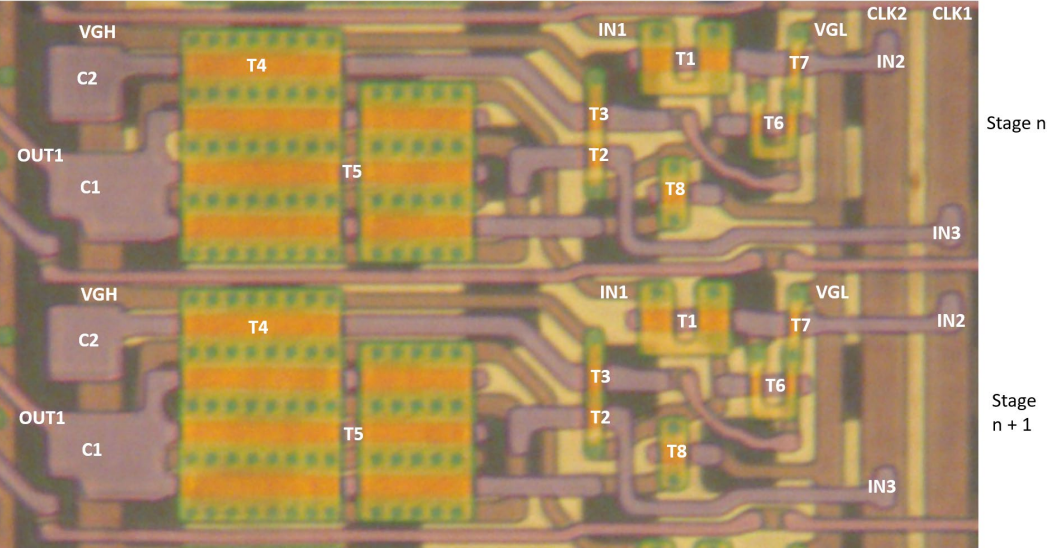
U.S. Patent No. 9,330,593	Mengtor Product
[3] The stage circuit as claimed in claim 2, wherein the first clock signal and the second clock signal have the same period and have phases that do not overlap.	The Mengtor Product contains a stage circuit in which the first clock signal and the second clock signal have the same period and have phases that do not overlap. This is a similar structure to the scan driver stage circuit structure in the AMOLED display used in the Samsung Galaxy S22 ULTRA Product. <i>See</i> Exhibit 2024; Exhibit2057; Exhibit 2058. CLK1 and CLK2 therefore have the same period and phases that do not overlap.

U.S. Patent No. 9,330,593	Mengtor Product
[4] The stage circuit as claimed in claim 3, wherein the first clock signal and the second clock signal have a period equal to two horizontal periods 2H and are supplied in different horizontal periods as low signals.	The Mengtor Product contains a stage circuit in which the first clock signal and the second clock signal have a period equal to two horizontal periods 2H and are supplied in different horizontal periods as low signals This is a similar structure to the scan driver stage circuit structure in the AMOLED display used in the Samsung Galaxy S22 ULTRA Product. <i>See</i> Exhibit 2024; Exhibit2057; Exhibit 2058. The first clock signal and the second clock signal therefore have a period equal to two horizontal periods 2H and are supplied in different horizontal periods as low signals.

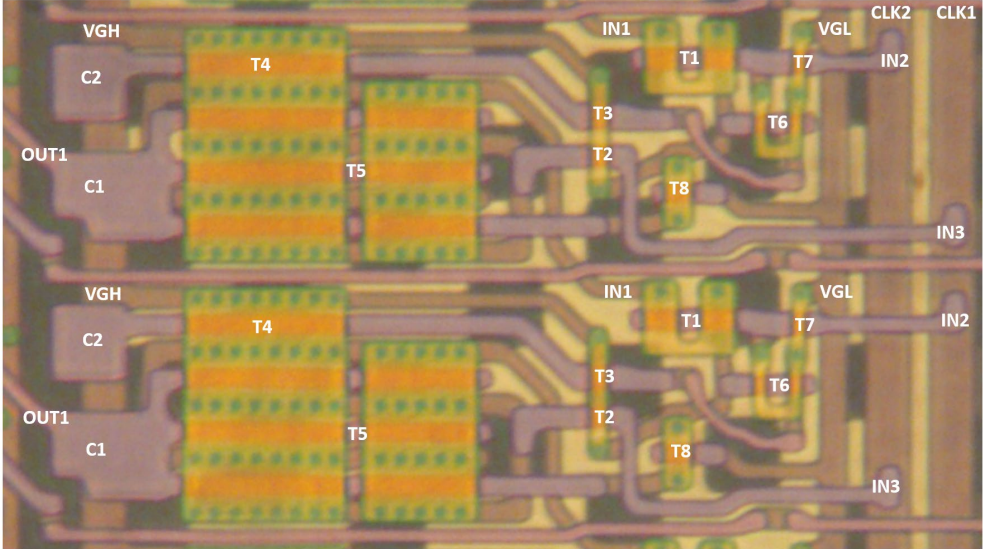
U.S. Patent No. 9,330,593	Mengtor Product
[5] The stage circuit as claimed in claim 2, wherein the start signal is supplied to overlap the first clock signal.	The Mengtor Product contains a stage circuit in which the start signal is supplied to overlap the first clock signal. This is a similar structure to the scan driver stage circuit structure in the AMOLED display used in the Samsung Galaxy S22 ULTRA Product. <i>See</i> Exhibit 2024; Exhibit2057; Exhibit 2058. The start signal is therefore supplied to overlap the first clock signal.

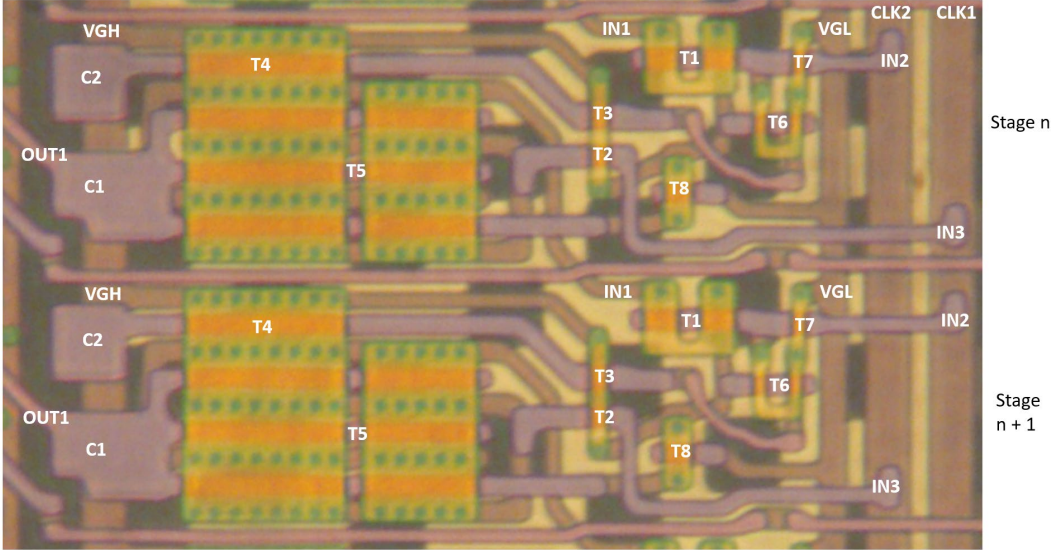
U.S. Patent No. 9,330,593	Mengtor Product
[6a] The stage circuit as claimed in claim 2, wherein the first driver includes: a first transistor between the first input terminal and the second node, the first transistor having a gate electrode coupled to the second input terminal; and	The Mengtor Product contains a stage circuit wherein the first driver includes a first transistor between the first input terminal and the second node, the first transistor having a gate electrode coupled to the second input terminal. For example, as shown in the annotated image below, the first driver includes at least transistors T1, T2, and T3. Transistor T1 is a first transistor between the first input terminal (e.g., IN1) and the second node (<i>see</i> claim elements 1[a], 1[b], above). Transistor T1 has a gate electrode coupled to the second input terminal (e.g., IN2).  Annotated Exhibit 2026 at 6 (Mengtor Teardown Images)

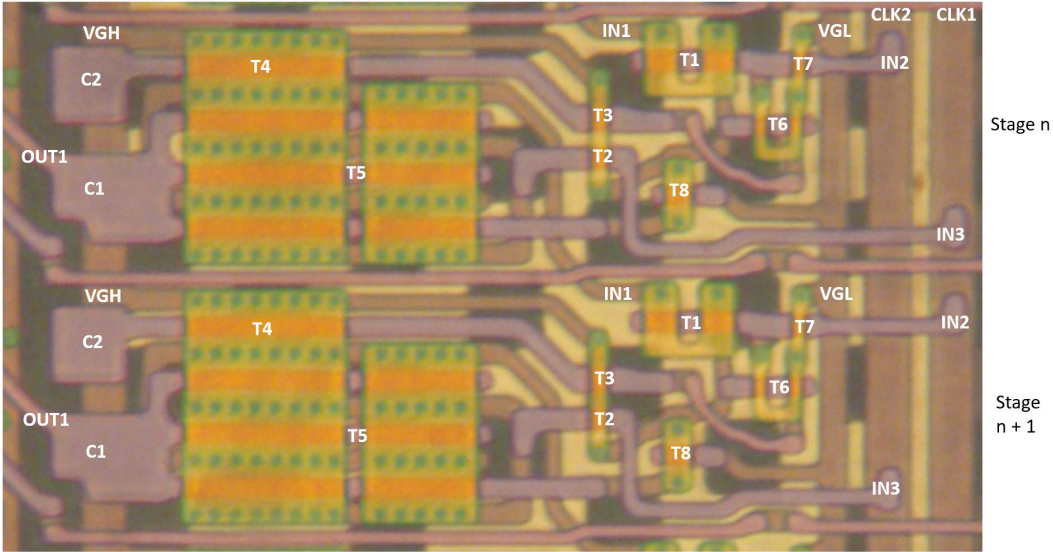
U.S. Patent No. 9,330,593	Mengtor Product
[6b] a second transistor and a third transistor serially positioned between the second node and the first power supply,	The Mengtor Product contains a stage circuit wherein the first driver includes a second transistor and a third transistor serially positioned between the second node and the first power supply. For example, as shown in the annotated image below, the first driver includes at least transistors T1, T2, and T3. Transistors T2 and T3 are second and third transistors serially positioned between the second node (<i>see</i> claim elements 1[a], 1[b], above) and the first power supply (e.g., VGH).  Annotated Exhibit 2026 at 6 (Mengtor Teardown Images)

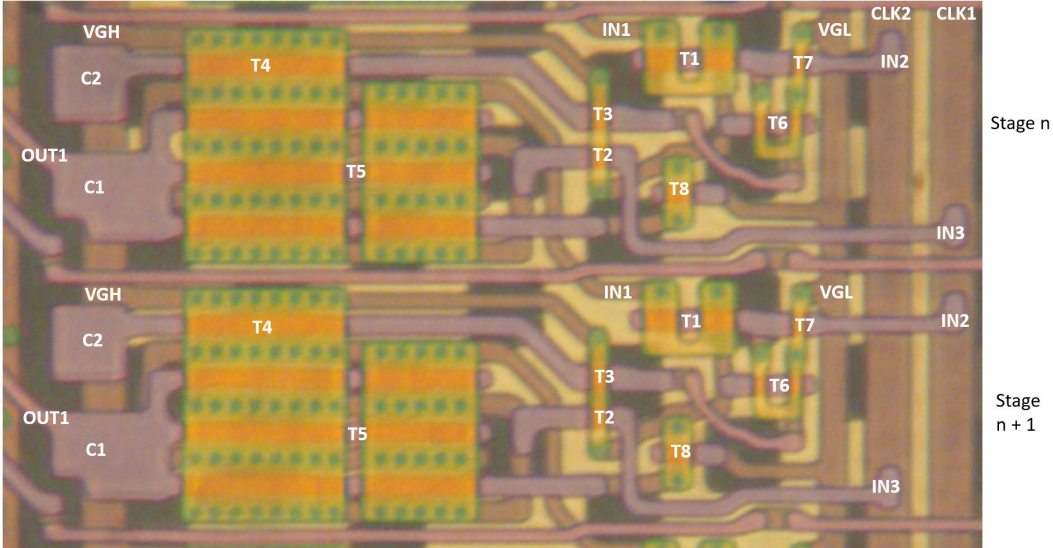
U.S. Patent No. 9,330,593	Mengtor Product
[6c] wherein a gate electrode of the second transistor is coupled to the third input terminal, and	The Mengtor Product contains a stage circuit wherein the first driver includes a second transistor and a third transistor serially positioned between the second node and the first power supply, wherein a gate electrode of the second transistor is coupled to the third input terminal. For example, as shown in the annotated image below, a gate electrode of the second transistor (e.g., T2) is coupled to the third input terminal (e.g., IN3).  Annotated Exhibit 2026 at 6 (Mengtor Teardown Images)

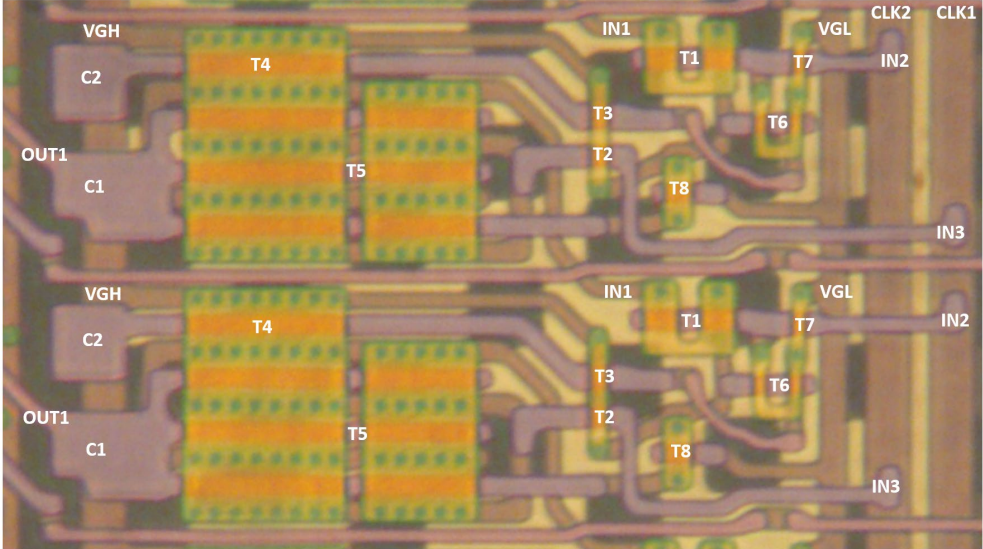
U.S. Patent No. 9,330,593	Mengtor Product
[6d] wherein a gate electrode of the third transistor is coupled to the first node.	The Mengtor Product contains a stage circuit wherein the first driver includes a second transistor and a third transistor serially positioned between the second node and the first power supply, wherein a gate electrode of the third transistor is coupled to the first node. For example, as shown in the annotated image below, a gate electrode of the third transistor (e.g., T3) is coupled to the first node (<i>see</i> claim element 1[a], above). Annotated Exhibit 2026 at 6 (Mengtor Teardown Images)

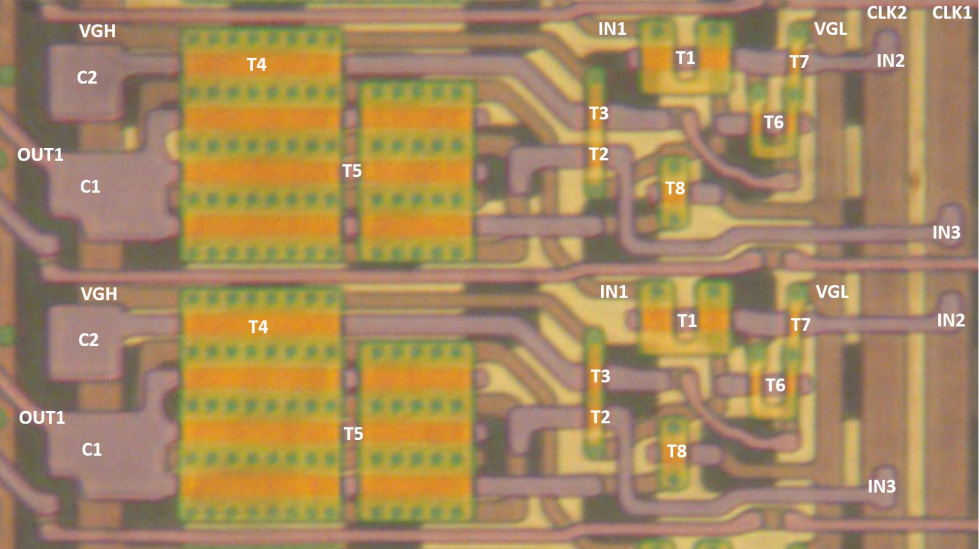
U.S. Patent No. 9,330,593	Mengtor Product
[7a] The stage circuit as claimed in claim 2, wherein the outputting unit includes: a fourth transistor between the first power supply and the output terminal, the fourth transistor having a gate electrode coupled to the first node;	The Mengtor Product contains a stage circuit wherein the outputting unit includes a fourth transistor between the first power supply and the output terminal, the fourth transistor having a gate electrode coupled to the first node. For example, as shown in the annotated image below, the outputting unit includes at least transistors T4, and T5, and capacitors C1 and C2. Transistor T4 is a fourth transistor between the first power supply (e.g., VGH), and the output terminal (e.g., OUT1). Transistor T4 has a gate coupled to the first node (<i>see</i> claim element 1[a], above).  Annotated Exhibit 2026 at 6 (Mengtor Teardown Images)

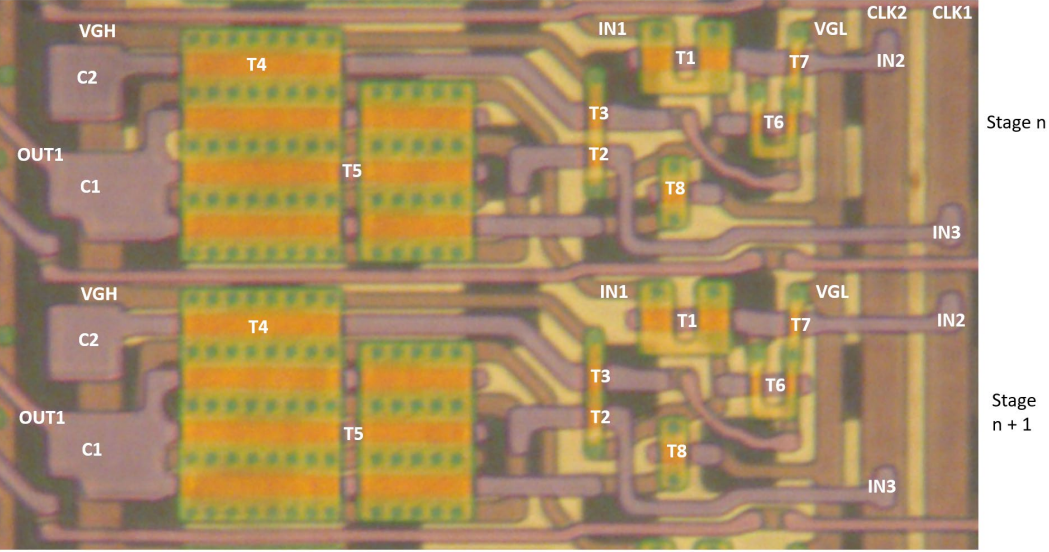
U.S. Patent No. 9,330,593	Mengtor Product
[7b] a fifth transistor between the output terminal and the third input terminal, the fifth transistor having a gate electrode coupled to the second node;	The Mengtor Product contains a stage circuit wherein the outputting unit includes a fifth transistor between the output terminal and the third input terminal, the fifth transistor having a gate electrode coupled to the second node. For example, as shown in the annotated image below, the outputting unit includes at least transistors T4, and T5, and capacitors C1 and C2. Transistor T5 is a fifth transistor between the output terminal (e.g., OUT1) and the third input terminal (e.g., IN3). Transistor T5 has a gate electrode coupled to the second node (<i>see</i> claim elements 1[a], 1[b] above).  Annotated Exhibit 2026 at 6 (Mengtor Teardown Images)

U.S. Patent No. 9,330,593	Mengtor Product
[7c] a first capacitor between the second node and the output terminal; and	The Mengtor Product contains a stage circuit wherein the outputting unit includes a first capacitor between the second node and the output terminal. For example, as shown in the annotated image below, the outputting unit includes at least transistors T4, and T5, and capacitors C1 and C2. Capacitor C2 is a first capacitor between the second node (<i>see</i> claim elements 1[a], 1[b] above), and the output terminal (e.g., OUT1).  Annotated Exhibit 2026 at 6 (Mengtor Teardown Images)

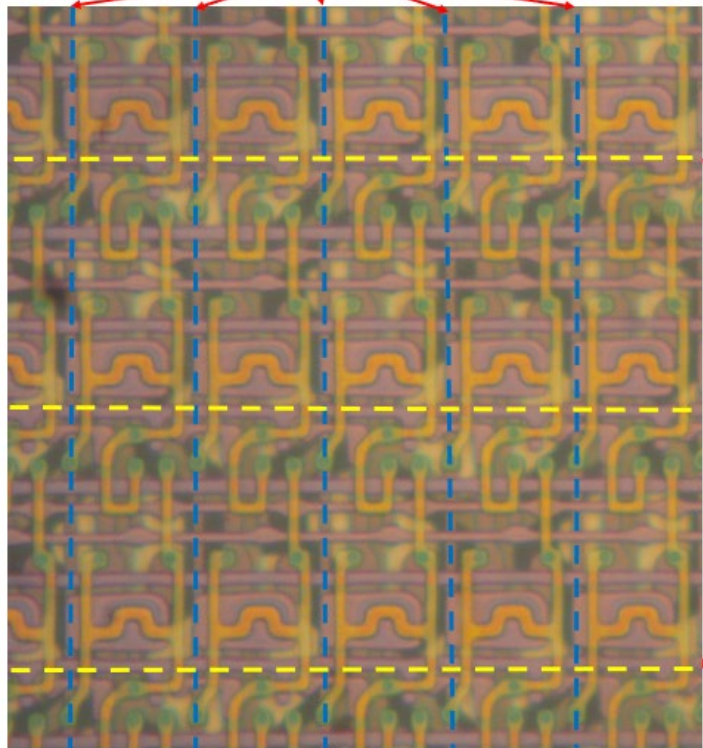
U.S. Patent No. 9,330,593	Mengtor Product
[7d] a second capacitor between the first node and the first power supply.	The Mengtor Product contains a stage circuit wherein the outputting unit includes a second capacitor between the first node and the first power supply. For example, as shown in the annotated image below, the outputting unit includes at least transistors T4, and T5, and capacitors C1 and C2. Capacitor C1 is a second capacitor between the first node (<i>see</i> claim element 1[a], above) and the first power supply (e.g., VGH).  Annotated Exhibit 2026 at 6 (Mengtor Teardown Images)

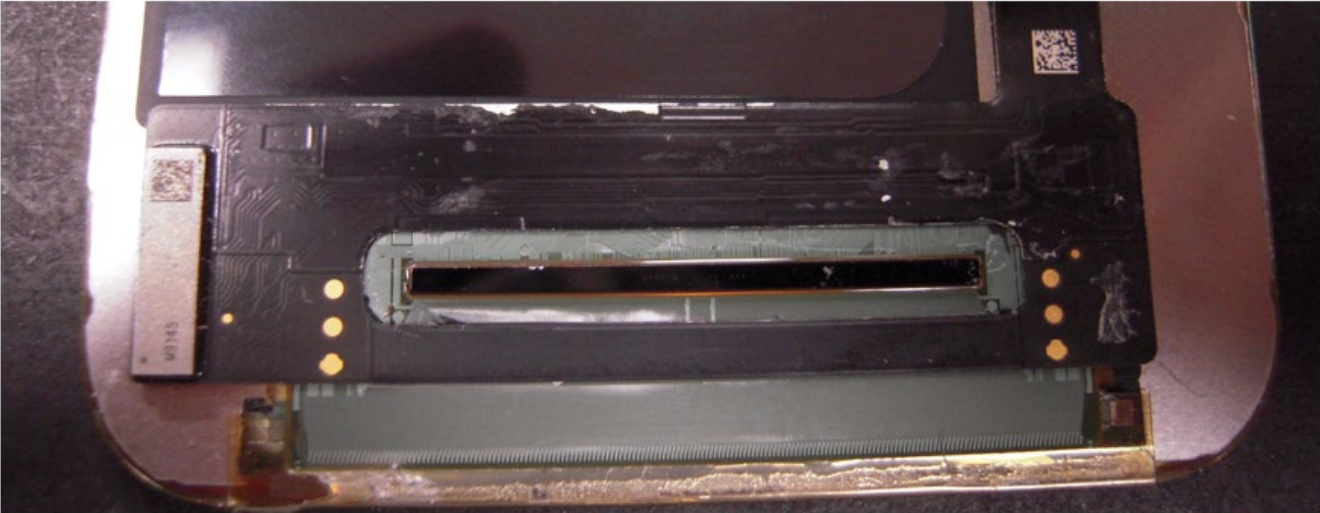
U.S. Patent No. 9,330,593	Mengtor Product
[8a] The stage circuit as claimed in claim 2, wherein the second driver includes: a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and	The Mengtor Product contains a stage circuit wherein the second driver includes a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node. For example, as shown in the annotated image below, second driver includes at least transistors T6, and T7. Transistor T6 is a sixth transistor between the first node (<i>see</i> claim element 1[a], above), and the second input terminal (e.g., IN2). Transistor T6 has a gate electrode coupled to the second node (<i>see</i> claim element 1[a], above).  Annotated Exhibit 2026 at 6 (Mengtor Teardown Images)

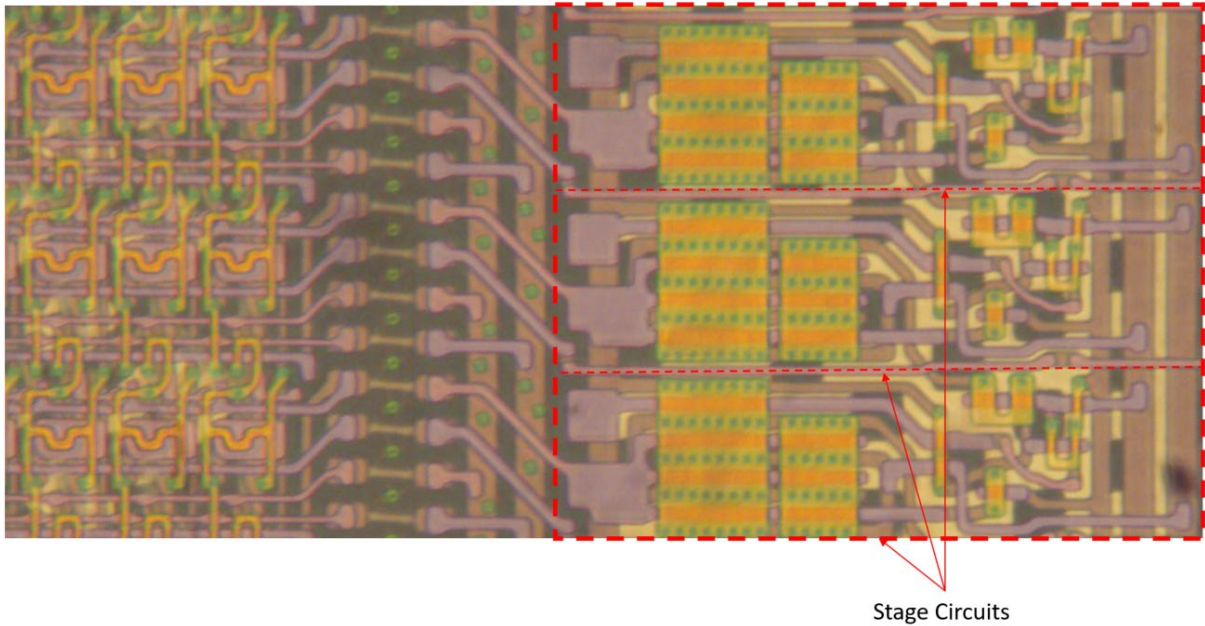
U.S. Patent No. 9,330,593	Mengtor Product
[8b] a seventh transistor between the first node and a second power supply, the second power supply having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal.	The Mengtor Product contains a stage circuit wherein the second driver includes a seventh transistor between the first node and a second power supply, the second power supply having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal. For example, as shown in the annotated image below, second driver includes at least transistors T6 and T7. Transistor T7 is a seventh transistor between the first node (<i>see</i> claim element 1[a], above), and a second power supply (e.g., VGL). Transistor T7 has a gate electrode coupled to the second input terminal (e.g., CLK2).  Annotated Exhibit 2026 at 6 (Mengtor Teardown Images)

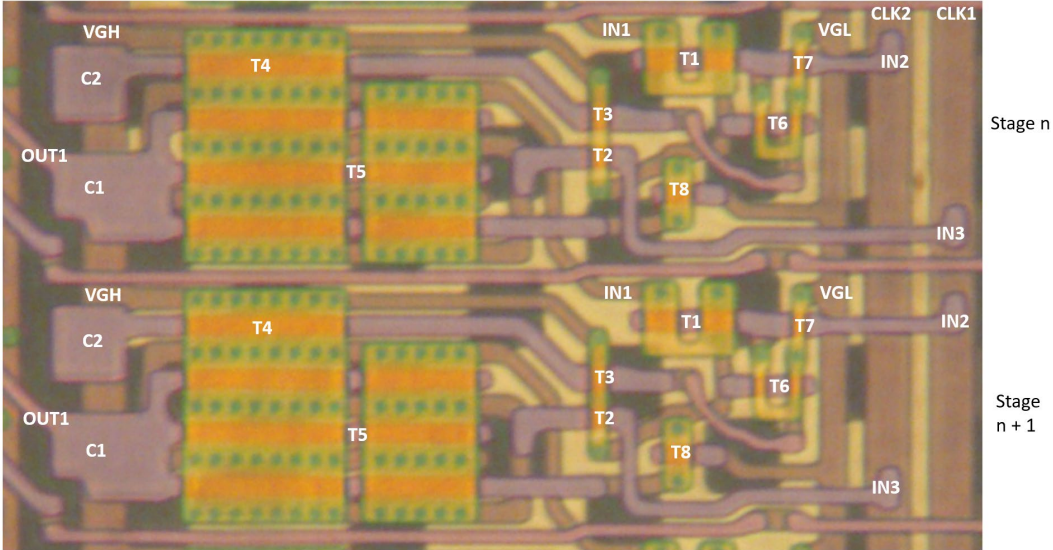
U.S. Patent No. 9,330,593	Mengtor Product
[14] The stage circuit as claimed in claim 1, wherein the transistor controls the voltage of the second node according to the on/off operation thereof.	The Mengtor Product contains a stage circuit wherein the transistor controls the voltage of the second node according to the on/off operation thereof. As shown in the annotated image below, transistor T3 controls the voltage of the second node (<i>see</i> claim element 1[a], above) according to its on/off operation.  Annotated Exhibit 2026 at 6 (Mengtor Teardown Images)

U.S. Patent No. 9,330,593	Mengtor Product
15[preamble] An organic light emitting display, comprising:	The Mengtor Product comprises an organic light-emitting diode (“OLED”) display:  Exhibit 2026 at 3–4 (Mengtor Teardown Images)

U.S. Patent No. 9,330,593	Mengtor Product
15[a] pixels positioned in regions partitioned by scan lines and data lines;	The Mengtor Product has pixels positioned in regions partitioned by scan lines and data lines. As shown, in the annotated image below, the Mengtor Product has a plurality of scan lines and a plurality of data lines. As shown, for example, in the annotated image below, pixels are positioned in regions partitioned by scan lines and data lines. Data Lines  Scan Lines Annotated Exhibit 2026 at 5 (Mengtor Teardown Images)

U.S. Patent No. 9,330,593	Mengtor Product
15[b] a data driver for supplying data signals to the pixels through the data lines; and	The Mengtor Product has a data driver for supplying data signals to the pixels through the data lines. The data driver of the Mengtor Product is shown in the image below:  Exhibit 2026 at 7 (Mengtor Teardown Images)

U.S. Patent No. 9,330,593	Mengtor Product
15[c] a scan driver for supplying scan signals to the pixels through the scan lines, the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals and having a first input terminal, a second input terminal, a third input terminal, and an output terminal, wherein each of the stage circuits includes:	The Mengtor Product has a scan driver for supplying scan signals to the pixels through the scan lines, the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals and having a first input terminal, a second input terminal, a third input terminal, and an output terminal. As shown in the annotated image below, the Mengtor Product has a scan driver that includes a plurality of stage circuits (red dashed lines), and scan lines coupled to the stage circuits on which the corresponding scan signals generated by the stage circuits are supplied to the pixel circuits (green dashed lines).  Stage Circuits Annotated Exhibit 2026 at 6 (Mengtor Teardown Images)

U.S. Patent No. 9,330,593	Mengtor Product
15[c] a scan driver for supplying scan signals to the pixels through the scan lines, the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals and having a first input terminal, a second input terminal, a third input terminal, and an output terminal, wherein each of the stage circuits includes: (<i>cont'd</i>)	As shown in the annotated image below, a stage circuit of the Mengtor Product has a first input terminal (e.g., IN1), a second input terminal (e.g., IN2), a third input terminal (e.g., IN3), and an output terminal (e.g., OUT1).  The image shows two identical stage circuits, labeled 'Stage n' and 'Stage n + 1', arranged vertically. Each stage circuit contains several labeled components: input terminals IN1, IN2, and IN3; output terminal OUT1; control lines VGH and VGL; clock lines CLK1 and CLK2; and transistors T1, T2, T3, T4, T5, T6, T7, and T8. The components are interconnected in a complex pattern, with some components highlighted in yellow and others in green. The labels are placed around the circuit components for identification. Annotated Exhibit 2026 at 6 (Mengtor Teardown Images) The figure below is a representative circuit diagram of the stage circuit of the Mengtor Product:

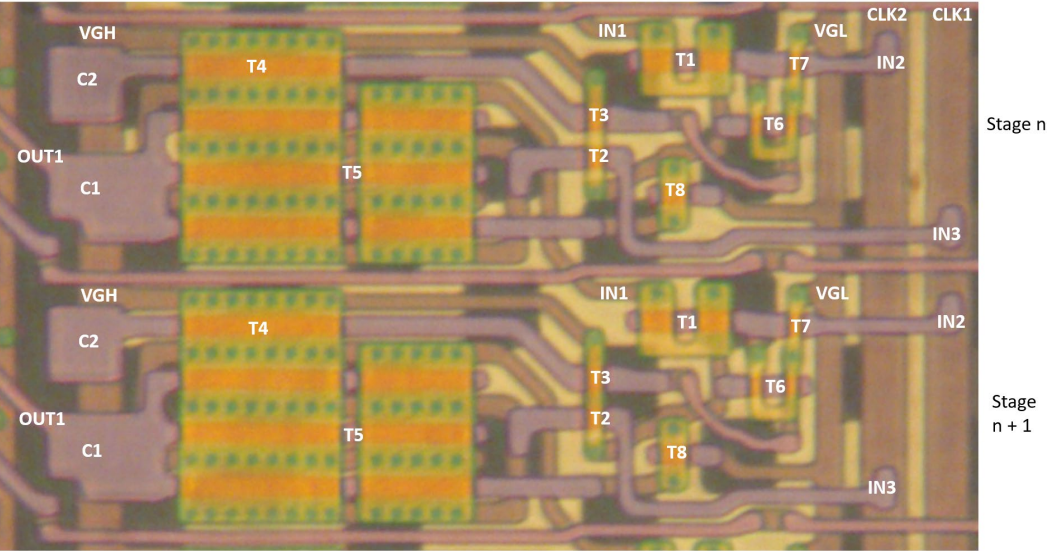
U.S. Patent No. 9,330,593	Mengtor Product
15[c] a scan driver for supplying scan signals to the pixels through the scan lines, the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals and having a first input terminal, a second input terminal, a third input terminal, and an output terminal, wherein each of the stage circuits includes: (<i>cont'd</i>)	Mengtor Equivalent Circuit

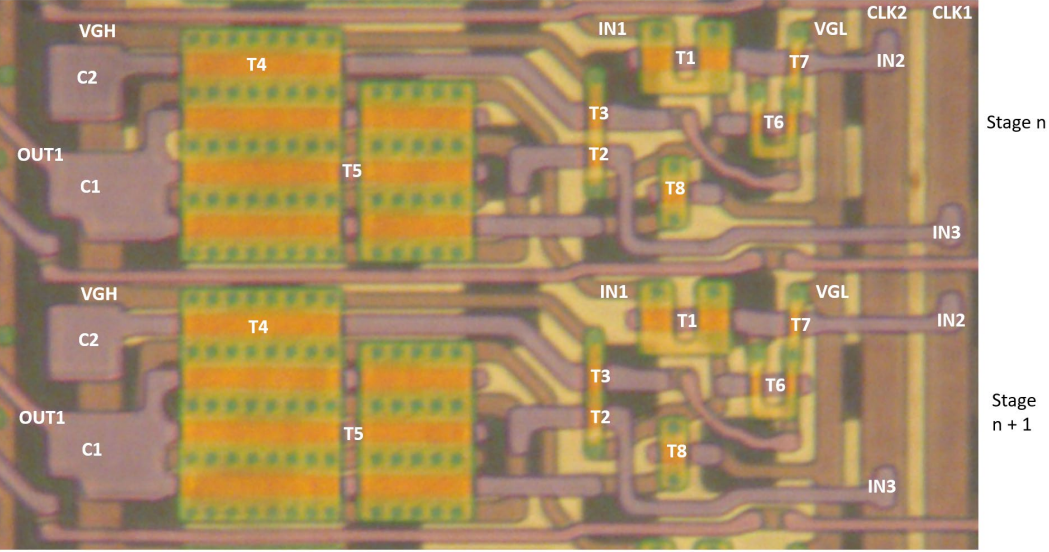
U.S. Patent No. 9,330,593	Mengtor Product
15[d] an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node,	<i>See element 1[a], above.</i>

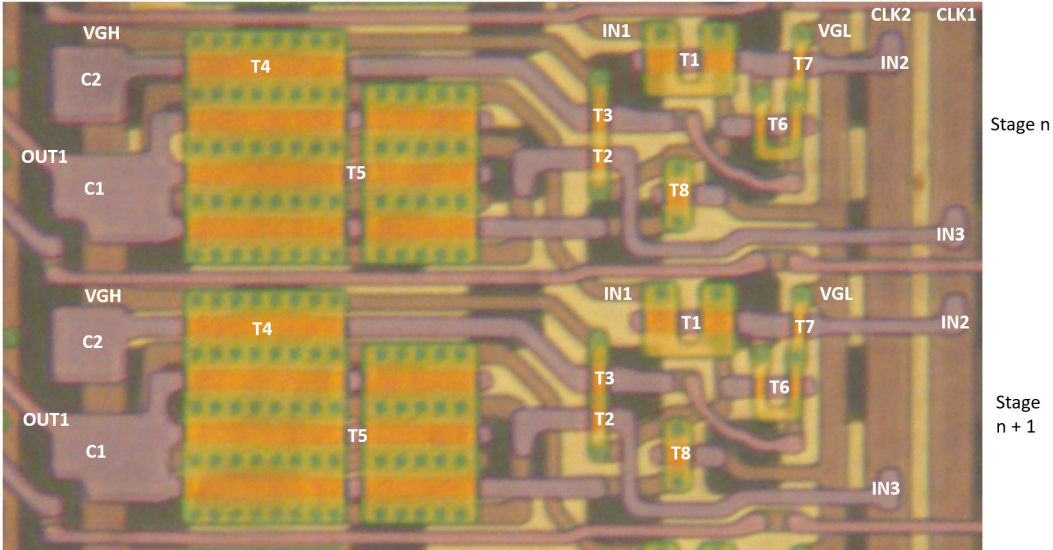
U.S. Patent No. 9,330,593	Mengtor Product
15[e] a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal, and	<i>See element 1[b], above.</i>

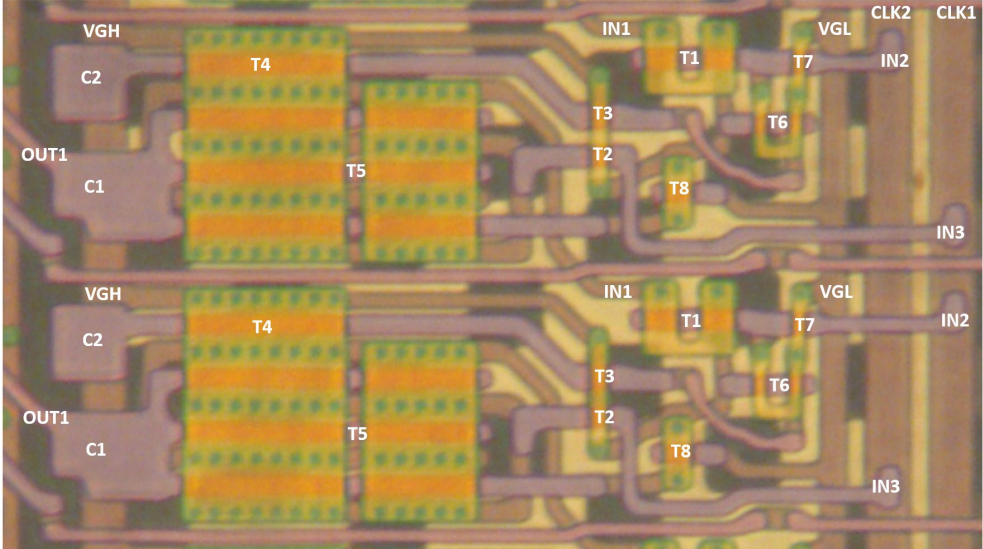
U.S. Patent No. 9,330,593	Mengtor Product
15[f] a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node,	<i>See element 1[c], above.</i>

U.S. Patent No. 9,330,593	Mengtor Product
15[g] wherein the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver.	<i>See element 1[d], above.</i>

U.S. Patent No. 9,330,593	Mengtor Product
[16] The organic light emitting display as claimed in claim 15, wherein a clock signal supplied to the third input terminal is used as the scan signal.	The Mengtor Product comprises an organic light-emitting diode display wherein a clock signal supplied to the third input terminal is used as the scan signal. For example, as shown in the annotated image below, transistors T4 and T5 supply a voltage to OUT1 depending upon the voltage between the gates of transistors T3 and T4 and the voltage between the gate of transistor T5 and the output of the first driver (<i>see</i> claim element 1[b], above). VGH is coupled to an electrode of transistor T4, such that when a voltage is applied to the node between the gates of transistors T3 and T4, transistor T4 is turned on and VGH is supplied to OUT1. OUT1 is coupled to an electrode of transistor T5 such that when a voltage is applied to a node between the gate of transistor T5 and the output of the first driver, transistor T5 is turned on and the clock signal supplied to IN3 is supplied to OUT1.  Annotated Exhibit 2026 at 6 (Mengtor Teardown Images)

U.S. Patent No. 9,330,593	Mengtor Product
[17] The organic light emitting display as claimed in claim 15, wherein the first input terminal receives a scan signal of a previous stage circuit or a start signal.	The Mengtor Product comprises an organic light-emitting diode display wherein the first input terminal receives a scan signal of a previous stage circuit or a start signal. For example, as shown in the annotated image below, the first input terminal of stage n+1 receives a scan signal (e.g., OUT1) of the previous stage circuit, stage n:  Annotated Exhibit 2026 at 6 (Mengtor Teardown Images)

U.S. Patent No. 9,330,593	Mengtor Product
[18a] The organic light emitting display as claimed in claim 17, wherein second input terminals of odd stage circuits receive a first clock signal and third input terminals of odd stage circuits receive a second clock signal, and	The Mengtor Product comprises an organic light-emitting diode display wherein second input terminals of odd stage circuits receive a first clock signal and third input terminals of odd stage circuits receive a second clock signal. For example, as shown in the annotated image below, the second input terminals (e.g., IN2) of odd stage circuits (e.g., stage n, below) receive a first clock signal (e.g., CLK2), and third input terminals (e.g., IN3) of odd stage circuits (e.g., stage n, below) receive a second clock signal (e.g., CLK1):  Annotated Exhibit 2026 at 6 (Mengtor Teardown Images)

U.S. Patent No. 9,330,593	Mengtor Product
[18b] wherein second input terminals of even stage circuits receive the second clock signal and third input terminals of even stage circuits receive the first clock signal.	The Mengtor Product comprises an organic light-emitting diode display wherein second input terminals of even stage circuits receive the second clock signal and third input terminals of even stage circuits receive the first clock signal. For example, as shown in the annotated image below, the second input terminals (e.g., IN2) of even stage circuits (e.g., stage n+1, below) receive the second clock signal (e.g., CLK1), and third input terminals (e.g., IN3) of even stage circuits (e.g., stage n+1, below) receive the first clock signal (e.g., CLK2):  Annotated Exhibit 2026 at 6 (Mengtor Teardown Images)

U.S. Patent No. 9,330,593	Mengtor Product
[19] The organic light emitting display as claimed in claim 18, wherein the first clock signal and the second clock signal have the same period and have phases that do not overlap.	<i>See element 3, above.</i>

U.S. Patent No. 9,330,593	Mengtor Product
[20a] The organic light emitting display as claimed in claim 18, wherein the first driver includes: a first transistor between the first input terminal and the second node, the first transistor having a gate electrode coupled to the second input terminal; and	<i>See element 6[a], above.</i>

U.S. Patent No. 9,330,593	Mengtor Product
[20b] a second transistor and a third transistor serially positioned between the second node and the first power supply,	<i>See element 6[b], above.</i>

U.S. Patent No. 9,330,593	Mengtong Product
[20c] wherein a gate electrode of the second transistor is coupled to the third input terminal, and	<i>See element 6[c], above.</i>

U.S. Patent No. 9,330,593	Mengtong Product
[20d] wherein a gate electrode of the third transistor is coupled to the first node.	<i>See element 6[d], above.</i>

U.S. Patent No. 9,330,593	Mengtor Product
[21a] The organic light emitting display as claimed in claim 18, wherein the outputting unit includes: a fourth transistor between the first power supply and the output terminal, the fourth transistor having a gate electrode coupled to the first node;	<i>See element 7[a], above.</i>

U.S. Patent No. 9,330,593	Mengtor Product
[21b] a fifth transistor between the output terminal and the third input terminal, the fifth transistor having a gate electrode coupled to the second node;	<i>See element 7[b], above.</i>

U.S. Patent No. 9,330,593	Mengtor Product
[21c] a first capacitor between the second node and the output terminal; and	<i>See element 7[c], above.</i>

U.S. Patent No. 9,330,593	Mengtor Product
[21d] a second capacitor between the first node and the first power supply.	<i>See element 7[d], above.</i>

U.S. Patent No. 9,330,593	Mengtor Product
[22a] The organic light emitting display as claimed in claim 18, wherein the second driver includes: a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node; and	<i>See element 8[a], above.</i>

U.S. Patent No. 9,330,593	Mengtor Product
[22b] a seventh transistor between the first node and a second power supply, the second power supply having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal.	<i>See element 8[b], above.</i>

U.S. Patent No. 9,330,593	Mengtor Product
[25] The organic light emitting display as claimed in claim 18, wherein the scan signal of the previous stage circuit or the start signal supplied to the first input terminal overlaps the clock signal supplied to the second input terminal.	<i>See element 5, above.</i>