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A New Small Sized Integrated Scan & Emission Driver for Compact AMOLED Displays

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Abstract

A new small sized integrated scan driver for small sized and high definition LCD and AMOLED display is proposed in this paper. By introducing a new simple circuit, the number of output buffers (n) of a scan driver shares only one shift register. Therefore, the number of total shift registers is reduced by 1/n and thus total area for scan driver is significantly reduced by 40 %. By applying the proposed circuit, a new small sized scan & emission driver is also proposed. This driver can precisely control the initial time for sampling of threshold voltage of DTFT in a pixel. The proposed drivers were verified by SPICE simulation by using LTPS P-type TFT models.

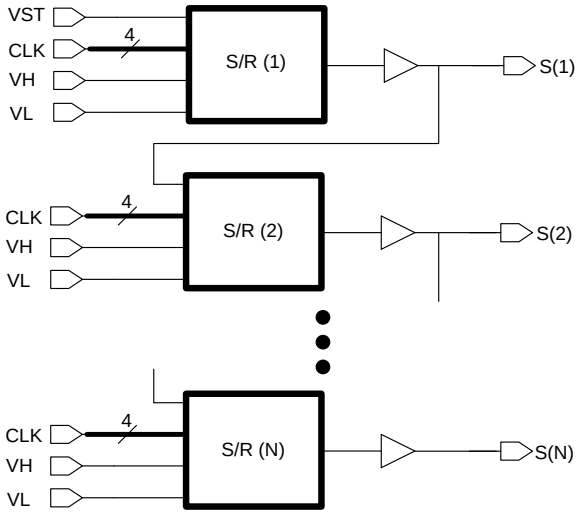
1. Introduction

Smartphones have drawn a great attention in recent year as the most popular hand-held consumer electronic device and users of the smartphone are rapidly increasing even though mobile phones are still used in the world. With the development of internet, various application programs and contents, and social network services (SNS) such as Twiter and Facebook, the number of the smartphone users are expected to continuously increase in all ages.

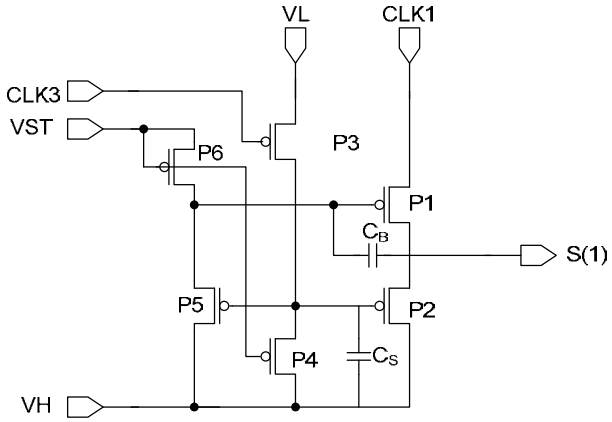
To process many tasks such as a e-mailing, a web searching, a real time information sharing and a social contacting through SNS, and to increase readability, displays for smartphones require not only much larger size but also much higher resolution than those of displays for mobile-phones. For example, the size of smartphones recently released is more than 3 or 4 inches and the higher resolutions of 960 x 640 or 1280 x 780 have been adopted for some products [1]-[2]. Most of the smartphones employ very high density displays over 300 *ppi* (pixel per inch). Therefore, it becomes more challenge to integrate peripheral drivers within a limited small area on a panel. Though they have been implemented by using low temperature poly-silicon TFT (LTPS TFT) process [3] or advanced solid phase crystallization TFT (A-SPC TFT) process [4], it is still difficult to implement the drivers in a limited area because process design rules of these processes are still in a range of several μm. In addition, a bezel of a panel is also getting narrowed for design of compact displays. Furthermore, AMOLED displays require more peripheral drivers such as a scan driver and an emission driver. Therefore, small sized drivers are required to reduce the area and to implement compact and high density displays.

The new small sized scan driver for high resolution and compact LCDs and AMOLED displays was proposed in [5]. However, this paper just conceptually showed the structures of small sized scan driver.

In this paper, the structures and its operation of the proposed small sized scan driver were dealt in detail. By making several buffers share a shifter register (S/R), the number of shifter registers could be reduced by 1/*k*, here *k* is the number of buffers and thus the total area for scan driver was reduced by 40%. A new small sized scan & emission driver is also proposed. The proposed driver can precisely control the initial time for sampling of threshold voltage of DTFT in a pixel. The proposed drivers were verified by SPICE simulation by using LTPS P-type TFT.



(a) Conventional scan driver block diagram with shifter register (S/R) and buffer



(b) Unit cell circuit of a conventional scan driver

Figure 1. Conventional scan driver for LCDs and AMOLED displays implemented with LTPS TFTs [3].

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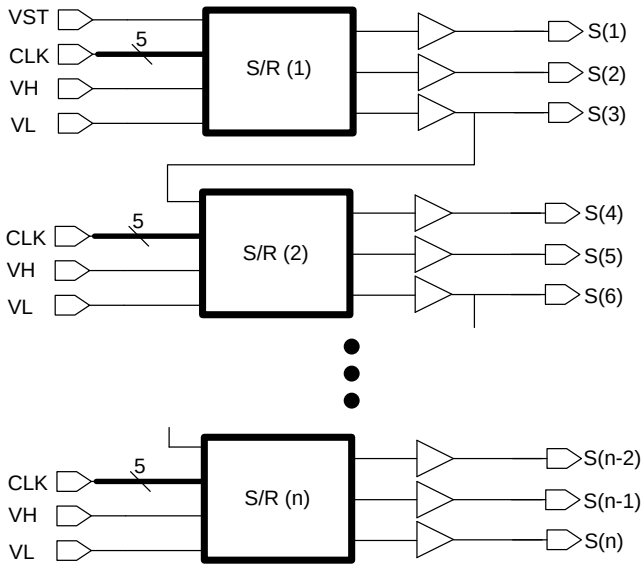
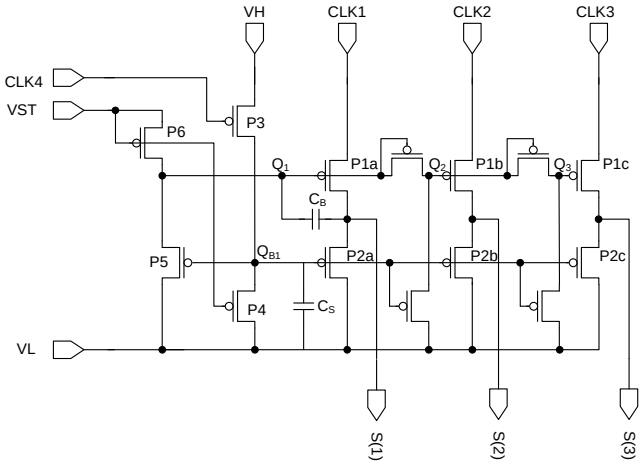
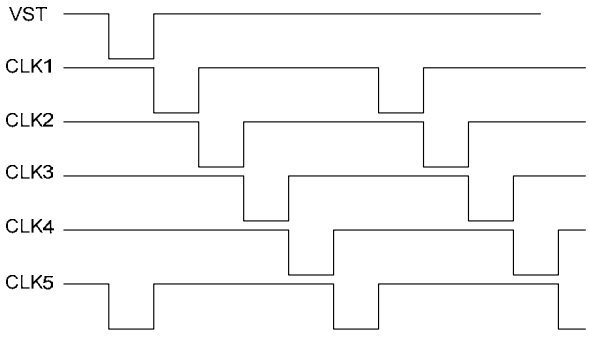


(a) The proposed scan driver block diagram with shared S/R and buffer



(b) Unit cell circuit of the proposed scan driver

(c)



(d) Timing diagram of input clocks

Figure 2. The proposed small sized scan driver and its timing diagram.

2. Small Sized Scan Driver

A conventional scan driver is shown in Fig. 1 [3]. The scan driver is composed of S/R and buffers as shown in Fig. 1 (a) and it is comprised of P-type LTPS TFTs and two storage capacitors as shown in Fig. 1 (b).

In the conventional scan driver, each buffer, which is composed of P1 and P2 in Fig. 1 (b), is connected to its own shift register one by one and thus the number of shifter registers *N* is determined by the number of scan lines. Each driver also has two large capacitors C_B and C_S ranging several tens or hundreds *fF* for complete operations for bootstrapping and maintaining stored charges, respectively. In contrast, in the proposed scan driver in Fig. 2 [], several buffers composed of P1a ~P1c and P2a~P2c share only one shift register as shown in Fig. 2 (a): the S/R (1) composed of TFTs P3~P6 drivers three buffers by introducing additional two P-TYPE diode PD1 and PD2 and two switches PS1 and PS2. As a result, the proposed scan driver can reduce two shift registers and four capacitors. The total number of shifter registers *n* is given by as follows.

$$n = \frac{N_s}{k} \tag{1}$$

Here, N_s is the number of scan lines and *k* is the number of buffers that share S/R. The number of clocks is required as follow.

$$\text{the \# of CLKs} = k + 2 \tag{2}$$

2.1 Operations of the scan driver

The operation of the proposed scan driver in Fig. 2 (b) is as follows, here *VL* is a low voltage level and *VH* is a high voltage level of clocks.

(1) When VST is *VL*, all gate nodes of the upper side TFTs, P1a ~P1c, become *VL* and PD1 and PD2 are on while P2a-P2c are off.

(2) When VST is *VH* and CLK1 is *VL*, then CLK1 is completely passing to the output S(1) without any distortion. All gates nodes of the buffers are still retaining their previous voltages until CLK4 becomes low.

(3) Therefore, CLK2 and CLK3 are successively passing to the outputs S(2) and S(3).

(4) After that, CLK4 becomes low and the voltages of all gates of the output buffers are reversed: P1a~P1c are *VH* and P2a~P2c are *VL*.

The capacitor C_B is required to pass the low voltage *VL* of a clock by bootstrapping and C_S is necessary to store charges until being refreshed.

2.2 Area reduction of the proposed scan driver

As shown in Fig. 1, conventional scan driver requires at least two capacitors C_B and C_S and these capacitors, which are made between two parallel metals for gate and source/drain (S/D), occupy large area because of their large capacitance ranging from several tens to hundreds *fF* for normal operations. There are also

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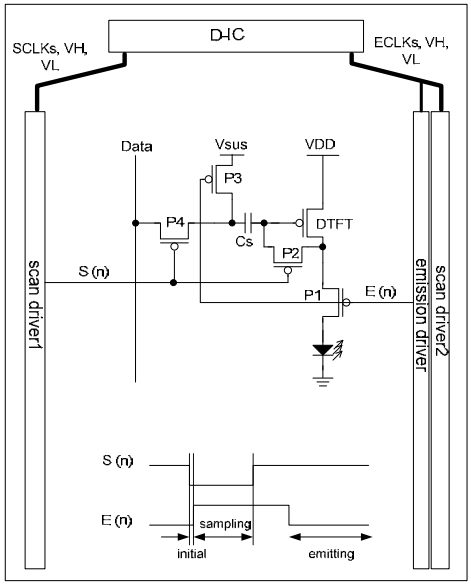
many TFTs in S/R that are not fully shown in Fig. 1. For examples, to prevent floating nodes from discharging due to a leakage current, all TFTs should be implemented dual gate structures or additional switches are inserted in series with each TFT. Therefore, the area for S/R cannot be neglected.

2.3 Precise integrated scan and emission drivers

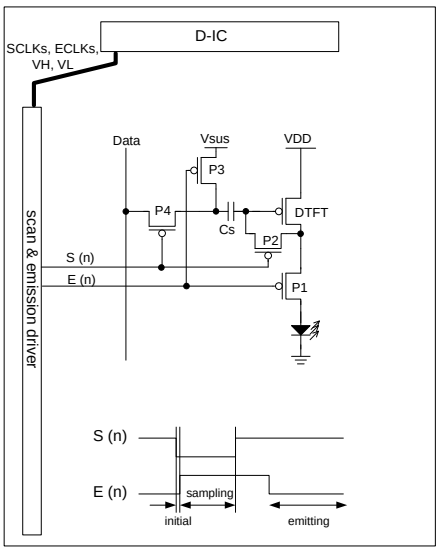
A conventional voltage pixel circuit [6]is shown in Fig. 3. The circuit operation is divided in two mode, V_{TH} sampling mode and emitting mode. For accurate V_{TH} sampling, a small initial time between the scan driver output and emission driver output, S (*n*) and E (*n*), is required as shown in Fig. 3. If S3 is off before S2 is on, the drain voltage of DTFT goes up much greater than *VDD*-V_{TH} and thus C_S cannot store correct V_{TH}. However, if the initial time is a little long, it reduces a contrast ratio of a display. Therefore, the initial time should be controllable and optimized.

To precisely control the initial time, another scan driver with different clocks ECLKs is required for emission driver as shown in Fig. 3. However, it requires an additional area for scan driver2 and additional ECLKs, *VH*, and *VL* also increase the number of pads of D-IC. In addition, this driver consumes additional power.

To solve the problems, unified scan and emission driers which are based on the proposed circuit in Fig. 2. are proposed as shown in Fig. 4. The scan & emission driver consists of an S/R P3~P6, a buffer $P1_a$ and $P2_a$ for S (n), a buffer $P2_b$ and $P2_b$ for emission driver and a buffer $P1_c$ and $P2_c$, a charge pump P7 and P8 and some capacitors C_{B1}, C_{B2}, and C_S. the two buffers $P1_a$, $P2_a$, $P2_b$, and $P2_b$ share the same S/R, but each buffer is separated by a diode PD and different clocks, SCLKs and ECLKs, are supplied to each buffer. In contrast to Fig. 3 (a), the proposed driver reduces the number of ECLKs by two. By changing the timing of SCLKs and ECLKs, the initial time can be controlled.

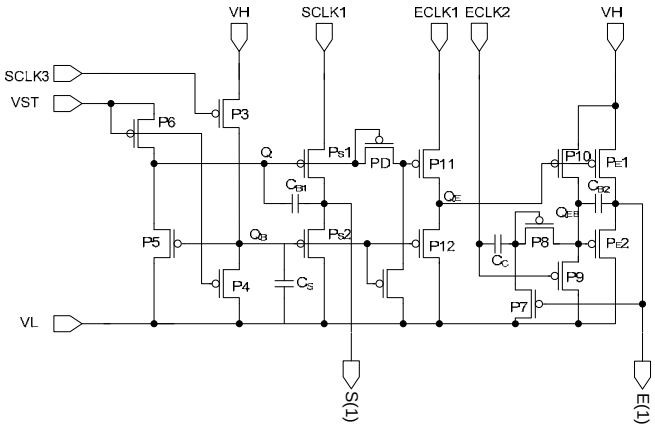


(a) AMOLED display with a separated conventional scan driver and a emission driver

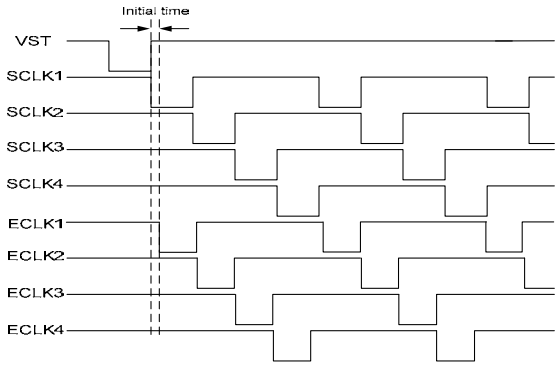


(b) AMOLED display with a proposed scan & emission driver

Figure 3. Example of AMOLED displays with conventional peripheral driver (a) and the proposed scan & emission driver (b).



(a) The proposed scan & emission driver



(b) Timing diagrams of the proposed scan & emission driver

Figure 4. The proposed scan & emission driver and its timing diagram.

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3. Simulation Results

The operation of the proposed scan driver is verified by SPICE simulations. The electrical characteristics of LTPS TFT were modeled by using the RPI LTPS TFT model of SMART SPICE. For SPICE simulations, *VH* and *VL* are 10 *V* and -8 *V*, respectively. The gate width and length of all switches of S/R are 6 μm and 6 μm. CS and CB are roughly determined as 100 *fF*, and Cc in Fig. 4 (b) is selected as 50 *fF*. The loads of the scan driver are modeled with a resistance and a capacitance, 2 $k\Omega$ and 30 *pF*. The *W/L* of buffer TFTs for *S*(*n*), Ps1 and Ps2, are selected as 80 μm/6 μm and 40 μm/10 μm, while the W/L of buffer TFTs for E(n), Pe1 and Pe2, are all 80 μm/6 μm.

Fig. 5 shows the results of the transient simulation of the proposed small sized scan driver for the condition that V_{TH} = -2 V. Here, *S*(1)-*S*(9) are the output waveforms of the scan driver, *Q*(1) - *Q*(9) are the waveforms of *Q* of each S/R, and $Q_B(1)$ - $Q_B(10)$ are the waveforms of Q_B of each S/R. It can be seen that *Q*(*n*) is well enough low so the each PCLK can pass out without any distortion, whereas $Q_B(n)$ well maintains its voltage *VH* for passing each PCLK to the output and then it keeps *VL* for a frame period.

Fig. 6 shows the simulation results of the proposed scan & emission driver. The initial time is set by the space between SCLKs and ECLKs, respectively. The results show that the proposed scan driver is well operated in a different range of initial time, from 0 to 2 μs. Fig. 6 (c) shows the voltage of Q_E and Q_{EB}. The low voltage of Q_{EB} is much lower than -8V due to the charge pump.

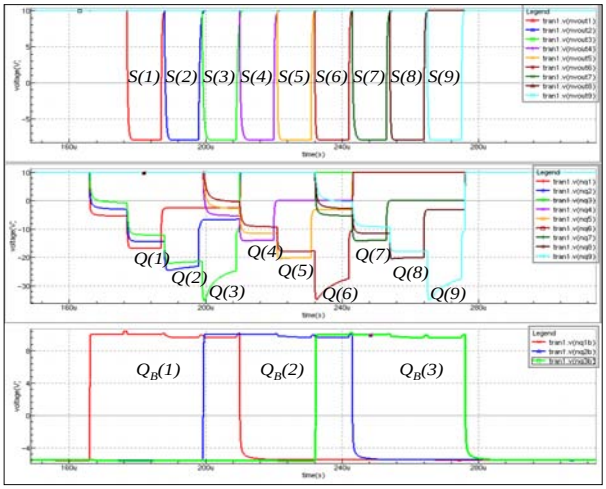
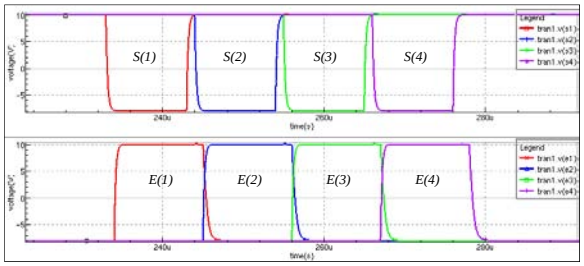
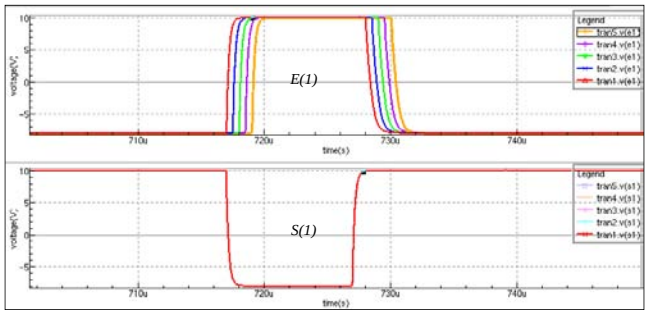


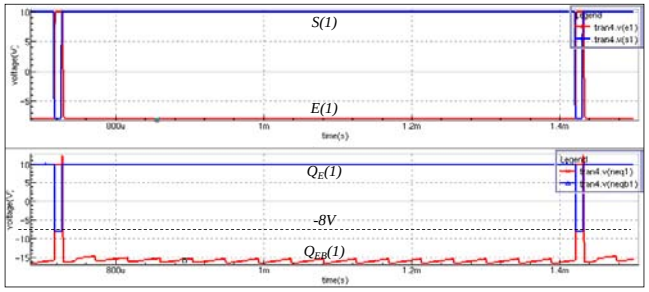
Figure 5. The simulation results of the proposed small sized scan driver.



(a) The simulation results of *S*(*n*) and *E*(*n*)



(b) The simulation results of initial time, 0~2μs, 0.5μs step



(c) The simulation results of charge pump for Q_{EB}

Figure 6. The simulation results of the proposed scan & emission driver.

4. Conclusion

A new scan driver and a scan & emission driver are proposed and verified in this paper. By introducing a simple circuit the proposed scan driver can reduce the area for a scan driver. Furthermore, the proposed scan and emission driver can control the initial time for driving AMOLED. As a result, it is expected that the proposed drivers can be employed for compact AMOLED displays.

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5. References

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