

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MIANYANG BOE OPTOELECTRONICS TECHNOLOGY CO., LTD.;
WUHAN CHINA STAR OPTOELECTRONICS SEMICONDUCTOR DISPLAY
TECHNOLOGY CO., LTD.; TIANMA MICROELECTRONICS CO., LTD.;
AND VISIONOX TECHNOLOGY, INC.,
Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.
Patent Owner.

Case IPR2024-00620
U.S. Patent No. 9,330,593

DECLARATION OF ANDREW WOLFE, PH.D.
IN SUPPORT OF THE PATENT OWNER RESPONSE

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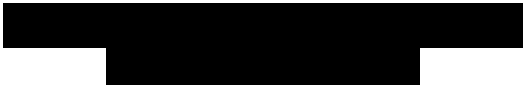
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I, Andrew Wolfe, Ph.D., declare and state, to the best of my knowledge, understanding, and belief, as follows:

1. I have been retained as a technical consultant on behalf of Samsung Display Co., Ltd. (“Samsung Display” or “Patent Owner”). I have been asked to consider whether certain of the references, and combinations of the references, listed as Exhibits 1004-1007 and 1014 below teach or suggest the limitations recited in claims 1-8, 14-22, and 25 of U.S. Patent No. 9,330,593 (Ex. 1001, the “’593 Patent”). I have also been asked to consider the state of the art and the prior art available before the time of the alleged invention of the ’593 Patent. My opinions are provided in this declaration.

2. To the best of my knowledge, I have no financial interest in Patent Owner. To the best of my knowledge, I have no financial interest in the Petitioners or any real party in interest. To the extent any mutual funds or other investments that I own have a financial interest in the Petitioner, the real parties in interest, the Patent Owner, or the ’593 Patent, I am not aware of, nor do I have control over, any financial interest that would affect or bias my judgment.

3. I am being compensated at my standard consulting rate for my time. My compensation is in no way contingent on the results of these or any other proceedings relating to the ’593 Patent.



I. BACKGROUND AND QUALIFICATIONS

4. My name is Andrew Wolfe. My complete qualifications and professional experience are described in my curriculum vitae, a copy of which is provided as Exhibit 2021. The following is a brief summary of my relevant qualifications and professional experience.

5. I am the founder and sole employee of Wolfe Consulting. Through Wolfe Consulting, I provide technical and business analysis to businesses on processor technology, computer systems, display technology, consumer electronics, software, design tools, data security, cryptography, and intellectual property issues. I have more than thirty years' experience developing products, researching, consulting, and teaching in those fields. In that time, I have worked as a computer architect, computer system designer, and as an executive in the PC and electronics business. I have also taught at some of the world's leading institutions in those fields, including Stanford University, Princeton University, Carnegie Mellon University, and Santa Clara University.

6. In 1985, I earned a B.S.E.E. degree in Electrical Engineering and Computer Science from the Johns Hopkins University. In 1987, I received a M.S. degree in Electrical and Computer Engineering from Carnegie Mellon University. In 1992, I received a Ph.D. degree in Computer Engineering from Carnegie Mellon University. My doctoral dissertation proposed a new approach for the architecture

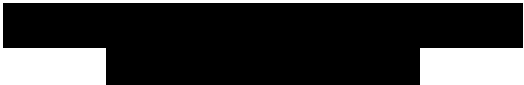
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of a computer processor. My undergraduate Senior Project involved characterizing and filtering noise and interference in capacitive touchscreens.

7. In 1983, I began designing touch sensors, microprocessor-based computer systems, and I/O (input/output) cards for personal computers as a senior design engineer for Touch Technology, Inc. During the course of my design projects with Touch Technology, I designed I/O cards for PC-compatible computer systems, including the IBM PC-AT, to interface with interactive touch-based computer terminals that I designed for use in public information systems. I continued designing and developing related technology as a consultant to the Carroll Touch division of AMP, Inc., where in 1986 I designed one of the first custom touch-screen integrated circuits. I designed the touch/pen input system for the Linus WriteTop, which many believe to be the first commercial tablet computer.

8. From 1986 through 1987, I designed and built a high-performance computer system at Carnegie Mellon University. From 1986 through 1988, I also developed the curriculum and supervised the teaching lab for the processor design courses.

9. In 1989, I worked as a senior design engineer for ESL-TRW Advanced Technology Division. I designed and built a bus interface and memory controller for a workstation-based computer system and worked on the design of a multiprocessor system.



10. At the end of 1989, along with some partners, I reacquired the technology I had developed at Touch Technology and at AMP and founded The Graphics Technology Company. As an officer and a consultant, I managed engineering development activities at that company and personally developed dozens of interactive graphics and interactive video computer systems over the next seven years.

11. I have consulted, formally and informally, for a number of processor design companies. In particular, I have served on the technical advisory boards for two media processor design companies, BOPS, Inc., where I chaired the board, and Siroyan Ltd. I served in a similar role for three networking chip companies, Intellon, Inc., Comsilica, Inc., and Entridia, Inc. and one 3D game accelerator company, Ageia, Inc. I have also served as a technology advisor to Motorola and to several venture capital funds in the U.S. and Europe. Currently, I am a director of Turtle Beach Corporation, providing guidance in its development of premium audio peripheral devices and user-input devices for a variety of commercial electronic products.

12. From 1991 through 1997, I served on the Faculty of Princeton University as an Assistant Professor of Electrical Engineering. At Princeton, I taught undergraduate and graduate-level courses in Computer Architecture, Advanced Computer Architecture, Display Technology, and Microprocessor Systems courses

[REDACTED]

as well as conducting sponsored research in the area of computer systems and related topics. I also was a principal investigator for DOD research in video technology and a principal investigator for the New Jersey Center for Multimedia Research. I worked on research proposals with Princeton's Center for Photonics and Optoelectronic Materials and taught classes on the use of thin-film transistors for active-matrix displays. From 1999 through 2002, I also taught the Computer Architecture course to both undergraduates and graduate students at Stanford University several times as a Consulting Professor. At Princeton, I received several teaching awards, both from students and from the School of Engineering. I have also taught advanced microprocessor architecture to industry professionals in IEEE and ACM sponsored seminars. I am currently a lecturer at Santa Clara University teaching courses on Microprocessor Systems, Real-time Embedded Systems, and Mechatronics.

13. From 1997 through 2002, I held a variety of executive positions at a publicly-held PC graphics company originally called S3, Inc. and later called Sonicblue Inc. These included Chief Technology Officer, Vice President of Systems Integration Products, Senior Vice President of Business Development, and Director of Technology. I also directed the display technology research group. At the time I joined S3, it supplied graphics accelerators for more than 50% of the PCs sold in the United States. As CTO, I led the development and introduction of more than 30 new

[REDACTED]

consumer electronics products. I was also part of a team that developed the Frontpath Progear tablet computer in 2000.

14. I have published more than 50 peer-reviewed papers in computer architecture and computer systems design. I have also chaired IEEE and ACM conferences in microarchitecture and integrated circuit design. I am a named inventor on at least fifty-seven U.S. patents and thirty-seven foreign patents including patents using TFT transistors and patents claiming OLED devices.

15. I have been the invited keynote speaker at the ACM/IEEE International Symposium on Microarchitecture and at the International Conference on Multimedia. I have also been an invited speaker on various aspects of technology or the PC industry at numerous industry events including the Intel Developer's Forum, Microsoft Windows Hardware Engineering Conference, Microprocessor Forum, Embedded Systems Conference, Comdex, and Consumer Electronics Show as well as at the Harvard Business School and the University of Illinois Law School. I have been interviewed on subjects related to computer graphics and video technology and the electronics industry by publications such as the Wall Street Journal, New York Times, LA Times, Time, Newsweek, Forbes, and Fortune as well as CNN, NPR, and the BBC. I have also spoken at dozens of universities including MIT, Stanford, University of Texas, Carnegie Mellon, UCLA, University of Michigan, Rice, and Duke.

[REDACTED]

16. Additional details of my education and work experience, awards and honors, and publications that may be relevant to the opinions I have formed are set forth in my CV (Exhibit 2021).

17. In summary, I have extensive familiarity with fields involving active-matrix displays and electroluminescence. I am familiar with what the state of this field was at the relevant time up to the time that the '593 Patent was filed.

II. MATERIALS REVIEWED

18. I am not an attorney and offer no legal opinions, but in my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person skilled in the art.

19. In preparing this declaration, I reviewed the '593 Patent, including the claims of the patent in view of the specification, and I have reviewed the prosecution history of the '593 Patent and numerous prior art and technical references from the time of the alleged invention. More specifically, I have reviewed each of the following:

Exhibit	Description
Ex. 1001	U.S. Patent No. 9,330,593 (the "'593 patent")
Ex. 1002	Prosecution History of U.S. Patent No. 9,330,593
Ex. 1003	Declaration of Dr. Daniel Foty
Ex. 1004	U.S. Patent Publication No. 2011/057190A1 ("Kimura")

Exhibit	Description
Ex. 1005	U.S. Patent Publication No. 2007/0063950A1 (“Shin”)
Ex. 1006	U.S. Patent Publication No. 2008/0101529A1 (“Tobita”)
Ex. 1007	U.S. Patent Publication No. 2008/0062097A1 (“Jeong”)
Ex. 1008	Excerpts from <i>Analog Integrated Circuit Design</i> , David A Johns et al., John Wiley & Sons, Inc., 1997
Ex. 1009	Complainant’s Opening Claim Construction Brief, <i>In the Matter of Certain Active Matrix Organic Light-Emitting Diode Display Panels and Modules for Mobile Devices, and Components Thereof</i> , Inv. No. 337-TA-1351
Ex. 1010	Excerpts from <i>Physics and Technology of Semiconductor Devices</i> , A. Grove, John Wiley & Sons, 1967
Ex. 1011	Excerpts from <i>CMOS Digital Integrated Circuits: Analysis and Design</i> , (third edition), S. Kang et al., McGraw-Hill, 2003
Ex. 1012	Docket from <i>Samsung Display Co., Ltd. v. BOE Technology Co., Ltd.</i> , E.D. Tex. 2-23-cv-00309
Ex. 1013	U.S. Patent Publication No. 2003/0132931A1 (“Kimura”)
Ex. 1014	U.S. Patent Publication No. 2005/0185752A1 (“Sasaki”)
Ex. 1015	U.S. Patent Publication No. 2007/0139348A1 (“Lee”)
Ex. 1016	U.S. Patent No. 4,720,815 (“Ogawa”)
Ex. 1017	EP 0 138 406 A2 (“Takemae”)
Ex. 1018	U.S. Patent No. 4,740,922 (“Ogawa II”)
Ex. 1019	Excerpts from Wolf, “Silicon Processing for the VLSI Era: Volume 2 – Process Integration” (1990)

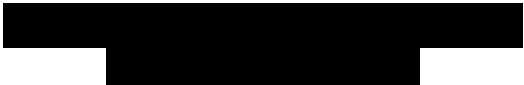
Exhibit	Description
Ex. 1020	U.S. Patent Publication No. 2007/0263763 A1 to Moon (“Moon”)
Ex. 1022	J. Miller, “Dependence of the input impedance of a three-electrode vacuum tube upon the load in the plate circuit,” Scientific Papers of the Bureau of Standards, 15(351), pp. 367–385 (1920)
Ex. 1023	US Patent Publication No. 2007/0085808A1 (“Lee”)
Ex. 1024	US Patent Publication No. 2009/0115792A1 (“Otoose”)
Ex. 2018	Claim Construction Order, Inv. No. 337-TA-1351
Ex. 2020	Notice of Allowance for U.S. Patent No. 9,330,593
Ex. 2024	Teardown Photos of Samsung Galaxy S22 Ultra Product
Ex. 2025	Teardown Photos of MobileSentry Product
Ex. 2026	Teardown Photos of Mengtor Product
Ex. 2027	Teardown Photos of Phone LCD Parts Product
Ex. 2028	Teardown Photos of Mobile Defenders Product
Ex. 2029	Teardown Photos of Injured Gadgets Product
Ex. 2030	Teardown Photos of Gadgetfix Product
Ex. 2031	Teardown Photos of Group Vertical Product
Ex. 2032	Teardown Photos of eTech Parts Plus Product
Ex. 2033	Teardown Photos of Parts4Cells Product
Ex. 2034	Teardown Photos of SEGMobile Product
Ex. 2035	Teardown Photos of Captain Mobile Parts Product
Ex. 2036	Teardown Photos of Repairs Universe Product

Exhibit	Description
Ex. 2037	Teardown Photos of Sourcely Plus Product
Ex. 2038	Teardown Photos of Fixez Product
Ex. 2039	Teardown Photos of Wholesale Gadget Parts Product
Ex. 2040	Teardown Photos of Parts4LCD Product
Ex. 2041	Teardown Photos of DFW Cellphone and Parts Product
Ex. 2042	Declaration of Aris Silzars, Ph.D.
Ex. 2043	Declaration of Adam Fontecchio, Ph.D.
Ex. 2044	 Declaration of Kwangsae Lee
Ex. 2045	<i>Samsung Display Co., Ltd. v. BOE Tech. Co., Ltd. et al.</i> , Case No. 2-23-cv-00309, Compl. (E.D. Tex. June 26, 2023).
Ex. 2046	Mengtor AMOLED Display Claim Chart
Ex. 2047	 Declaration of Hwan-Soo Jang
Ex. 2048	
Ex. 2049	Jason Gutierrez, <i>CES is over – where are the bezel-less phones?</i> , Android Authority (2013)
Ex. 2050	Jin Huh, <i>A New Small Sized Integrated Scan & Emission Driver for Compact AMOLED Displays</i> , SID 2012 Digest (2012)

Exhibit	Description
Ex. 2051	United States Patent Application Publication No. 2013/0169609
Ex. 2052	United States Patent No. 9,620,061
Ex. 2053	United States Patent No. 11,227,549
Ex. 2054	Suzanne Kantra, <i>Review of the Samsung Galaxy S4</i> , Techlicious (2013)
Ex. 2055	Tony Fletcher, <i>Samsung Galaxy S4 announced and here's the photos, specs and videos</i> , WireFresh (2013)
Ex. 2056	Chuong Nguyen, <i>Samsung Galaxy S4 Review</i> , GottaBeMobile (2013)
Ex. 2057	– Samsung Galaxy S22 Ultra AMOLED Display Claim Chart
Ex. 2058	–

III. SUMMARY OF OPINIONS

20. As I explain below, it is my opinion that the references relied upon in the Petition in view of the knowledge of a person of ordinary skill in the art (“POSITA”) do not render obvious any challenged claim. It is also my opinion that objective indicia of non-obviousness further support the non-obviousness of the challenged claims.



IV. RELEVANT LEGAL STANDARDS

21. I am not an attorney. For the purposes of this declaration, I have been informed about certain aspects of the law that are relevant to forming my opinions. I have been informed as follows:

22. I have been informed that a party challenging a claim's patentability in an *inter partes* review bears the burden to show by a preponderance of the evidence that the claim is unpatentable in view of the prior art. I understand that a "preponderance" means "more likely than not."

23. I have been informed that a patent claim is "obvious" in view of the prior art if the differences between the claim and the prior art are such that the subject matter as a whole would have been obvious to a POSITA at the time of the claimed invention.

24. I have been informed that the factors to be considered in analyzing whether a claim was obvious are: (i) the scope and content of the prior art; (ii) the differences between the prior art and the claims; (iii) the level of ordinary skill in the pertinent art; and (iv) any asserted objective indicia of non-obviousness.

25. I have been informed that objective indicia of non-obviousness (which I am informed are sometimes also referred to as secondary considerations of non-obviousness) refers to certain real-world facts that tend to show that a patent claim was not obvious at the time of the claimed invention. I have also been informed that

[REDACTED]

this evidence may include, among other things, whether the claimed invention satisfied a long-felt but unmet need; whether other failed to develop a solution to the long-felt need; whether the claimed invention or a product having the attributes of the claimed invention was praised or recognized by others; and whether others copied the claimed invention.

26. I have been informed that this type of evidence demonstrates non-obviousness because it shows that others working in the field would have been motivated to create a product having the attributes of the claimed invention if they had had the necessary inventive skill to do so. I also understand that such objective indicia must be considered from the perspective of a POSITA.

27. I have been informed that it is appropriate to consider objective indicia if there is a nexus, or connection, between the claimed invention and the objective indicia. I have also been informed that a nexus may be shown when the objective evidence is attributed to the specific product that embodies the invention disclosed and claimed in the patent.

28. I have been informed that where, as here, an obviousness defense is based on a combination of prior art references, a patent claim is not obvious unless a POSITA would have been motivated to combine or modify prior art elements to obtain the invention as set forth in the claim with a reasonable expectation of success.

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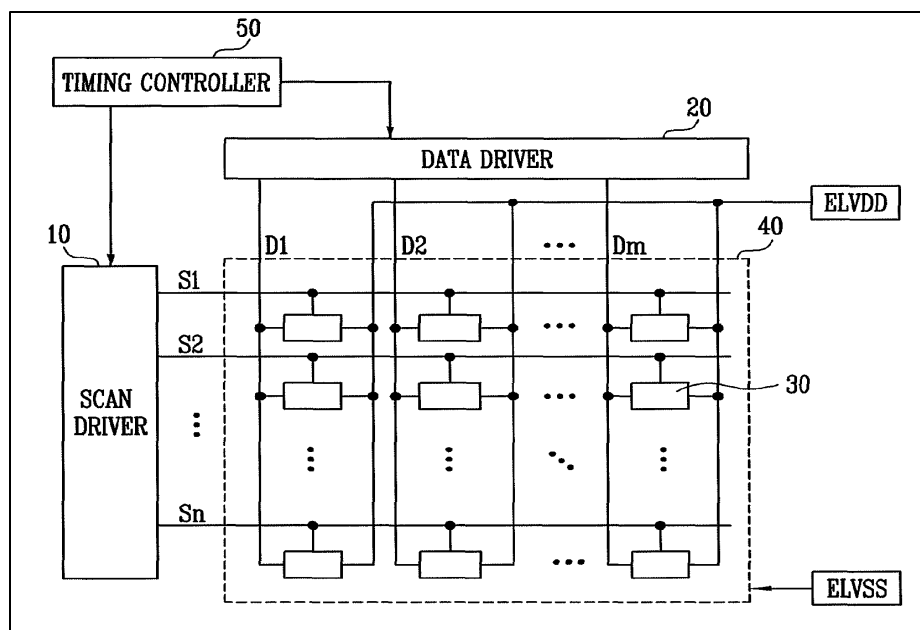
I understand that a motivation to combine prior art references can come from the references themselves or from the understanding of a POSITA.

29. I have been informed that references must be considered in their entirety from the view of a POSITA at the time of the invention, but that viewing the art through hindsight is impermissible.

30. I have been informed that in considering obviousness, it is relevant to consider whether the prior art includes references that “teach away” from the claimed invention. I understand that a reference teaches away from the claimed invention if a POSITA, reading the reference, would be discouraged from following the path of the claimed invention or would be led in a divergent direction.

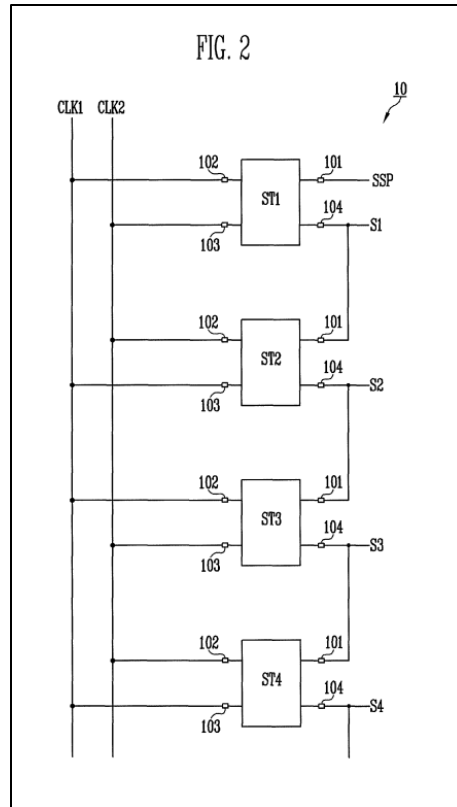
V. OVERVIEW OF U.S. PATENT NO. 9,330,593

31. The '593 Patent relates to a novel stage circuit for an AMOLED display. In an AMOLED display, the rows of pixels in the display are typically provided scan signals by a scan driver, which is made up of a plurality of stage circuits. As the '593 Patent explains, “[c]onventional organic light emitting display[s] include[] a data driver for supplying data signals to data lines, a scan driver for sequentially supplying scan signals to scan lines, and a pixel unit including a plurality of pixels coupled to the scan lines and the data lines.” '593 Patent at 1:34–38. Figure 1 of the '593 Patent depicts this structure:

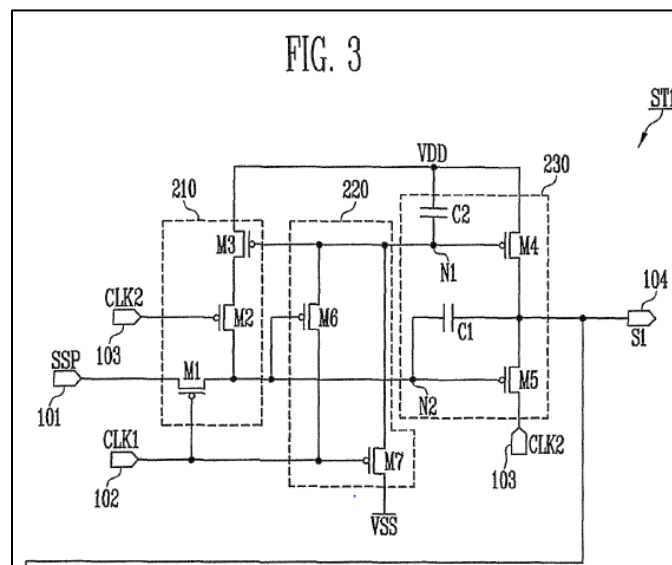


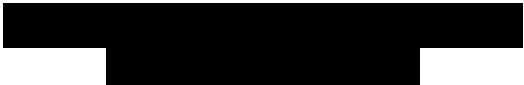
32. As shown in Figure 1, scan lines S1 through Sn are connected to a row of pixels each, respectively. The pixels are selected row by row through scan signals provided by the scan driver to the scan lines, in order for each row of pixels to receive data signals: “[t]he pixels included in the pixel unit are selected when the scan signals are supplied to the scan lines to receive the data signals from the data lines.” ’593 Patent at 1:39–41.

33. As shown in Figure 2, below, the scan driver typically includes one stage circuit for each row of pixels, with each stage circuit connected to the corresponding scan line.



34. In the example of Figure 2, stage circuit ST1 is connected to scan line S1, stage circuit ST2 is connected to scan line S2, and so on. Each stage circuit, in turn, may comprise a number of transistors and capacitors. For example, Figure 3 below depicts an exemplary stage circuit ST1:





35. As shown in Figure 3, the stage circuit is comprised of transistors M1-M7 and capacitors C1-C2. The stage circuit receives clock signal inputs CLK1 and CLK2, as well as a start pulse signal SSP, and provides a scan signal output to output terminal 104 to the scan line S1. This exemplary circuit represents stage circuit ST1 in Figure 2, but the remaining stage circuits have the same components and topology.

36. As the '593 Patent explains, its inventions reduce the number of necessary transistors and input signals:

[E]mbodiments provide stages having a reduced number of transistors and that output scan signals only using first and second clock signals. In contrast, conventional stage circuits includes [*sic*] at least ten transistors . . . and/or require[d] use of [an] initializing signal in addition to the first and second clock signals.

'593 Patent at 9:12–18. This reduction allows for improved manufacturability and circuit stability. *See, e.g.*, '593 Patent at 9:18–20 (“[w]hen [the] number of transistors in a stage increases, process yield deteriorates, so that stability of driving is deteriorated.”); '593 Patent at 9:20–22 (“[w]hen more initializing signals are required, there is less time for supplying scan signals, thereby reducing stability”).

37. In the stage circuit of the '593 Patent, the output of one stage (e.g., ST1) is provided as an input to the next stage (e.g., ST2), and thus an additional initialization signal for each subsequent stage can be omitted. Additionally, as shown for example in Figure 3, the '593 Patent's stage circuit requires only two clock signal

inputs, and less than ten transistors. This yields the benefits the '593 Patent describes in improving timing, reducing complexity, and increasing stability of the circuit. '593 Patent at 9:12–26.

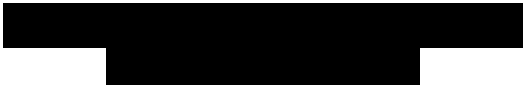
VI. LEVEL OF ORDINARY SKILL IN THE ART

38. I am informed that factors to be considered in determining the level of ordinary skill in the art include: (1) the types of problems encountered in the art; (2) the prior art solutions to those problems; (3) the rapidity with which innovations are made; (4) the sophistication of technology; and (5) the educational level of active workers in the field.

39. Using these factors, in my opinion, a person of ordinary skill in the art (“POSITA”) with regard to the '593 Patent would have had a relevant technical degree in Electrical Engineering, Computer Engineering, Materials Science, Physics, or the like, and 2-3 years of experience in active matrix display design and electroluminescence.

40. I understand that the Petitioner has proposed that a POSITA in the field of the '593 Patent would have had a Bachelor's degree in electrical engineering or similar discipline, along with 2-3 years of circuit design/analysis experience.” Pet. at 5.

41. I do not agree with the Petitioner's proposal, because it does not require any experience in active matrix display design or electroluminescence, which are the



subject matter of the '593 Patent. As explained above, the '593 Patent is directed to AMOLED displays and solving problems specific to those displays, including improving scan-on time and reducing the physical footprint of the scan circuitry required to program each row of pixels. There are aspects of circuit design that are unique to the context of active-matrix display design, and to the context of electroluminescent displays, as opposed to general circuit design. For example, the signal timings generated by the scan driver and provided to the pixel circuits are specialized to AMOLED displays. Claim 15 of the '593 Patent recites elements, including, for example, “a scan driver for supplying scan signals to the pixels through the scan lines,” as well as a “data driver for supplying data signals to the pixels through the data lines,” that are directed to these aspects of active-matrix displays. Claim 15 further recites “an organic light emitting display,” which is directed to electroluminescence. In addition, the “Background” of the '593 Patent explains that “[a] typical light emitting display supplies currents corresponding to data signals to OLEDs using transistors formed in pixels so that the OLEDs may emit light.” '593 Patent, 1:30-33. The use of pixel circuits comprising transistors for individual pixels is indicative of an active-matrix display. Similarly the “Field” refers to “a stage circuit and an organic light emitting display using the same.” '593 Patent, 1:17-18; *see also* '593 Patent, 9:24-26, Title.

[REDACTED]

42. Petitioner’s definition, which relates only to general “circuit design” does not accurately reflect the unique aspects of, and design considerations that go into, active matrix displays, and as such it does not reflect the experience of those working in the field or the technology of the ’593 Patent. Indeed, this is evident even from the alleged prior art relied upon by Petitioner. For example, the disclosures from Kimura relating to the GOUT and SOUT signals are specific to the display context, and make clear that these signals serve different functions within the scan driver and pixel array. *See, e.g.,* Kimura ¶¶ [0304]-[0305]. Because Petitioner’s proposed definition fails to include any experience with active matrix display design and electroluminescence, in my opinion it fails to reflect the background and knowledge of a person of ordinary skill in the art.

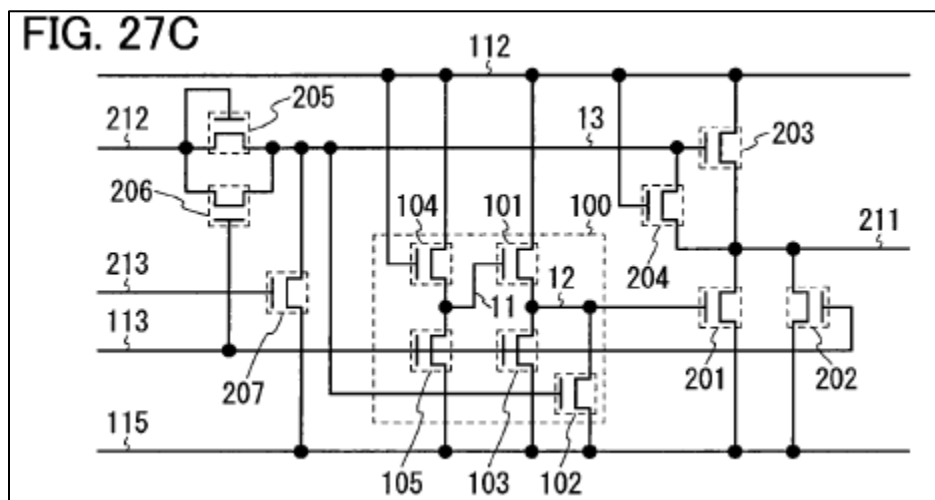
VII. CLAIM CONSTRUCTION

43. After reviewing the specification and the prosecution history, I do not believe that any constructions other than the plain and ordinary meaning of the claim terms of the ’593 Patent are necessary at this stage of the current proceeding. I have also reviewed the ALJ’s Markman Order in the parallel ITC investigation and believe my opinions are consistent with those constructions. Additionally, I understand that the Board found that for purposes of the institution decision, for limitation [1-B]/[15-E], controlling the voltage of the second node does not require the voltage of the second node to be determined by the first driver alone. As

discussed below, I do not believe that any of Petitioner's grounds render obvious the challenged claims.

VIII. KIMURA DOES NOT RENDER OBVIOUS THE CHALLENGED CLAIMS.

44. Dr. Foty relies on the circuit of Figure 27C, shown below, for his analysis of Kimura:



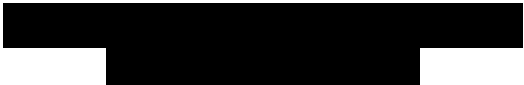
45. This circuit includes 12 transistors (101, 102, 103, 104, 105, 201, 202, 203, 204, 205, 206, and 207), as well as at least 4 input signals (112, 212, 213, and 113). *See also e.g.* Kimura at [286]-293]. The Figure 27C circuit is thus like the prior art circuits that the '593 Patent improved upon. As the '593 Patent explains, its inventions allowed for reducing the number of transistors in each stage, and also reduced the number of necessary signal lines. For example, the '593 Patent teaches that prior art stage circuits had "at least ten transistors," and required first and second clock signals in addition to a start pulse (which could be provided as a separate input signal, or as the output from a previous stage circuit). '593 Patent, 9:12-26. The '593

[REDACTED]

Patent explains that the reduction in number of transistors and input signals led to improvements in manufacturing, as well as improved efficiency and speed of the stage circuit. '593 Patent, 9:12-26.

46. It also bears mention that Kimura teaches a large number of embodiments, as well as different circuit configurations of those embodiments. As one example, Figures 7A-C are each referred to as showing the second embodiment, but each is a different circuit with different connections between certain elements. *See, e.g.*, Kimura at ¶¶ [0283]-[0287] (describing the different transistors and corresponding connections in the circuits of Figs. 27A, 27B, and 27C). A POSITA would have no reason to look to the Figure 27C embodiment as opposed to any other, and neither the Petition nor Dr. Foty provide any reason why a POSITA would have thought to start with the Figure 27C circuit.

47. Additionally, the specific connections of circuit elements in the Figure 27C circuit are necessary for Dr. Foty's arguments as to how Kimura meets the requirements of the challenged claims. But Kimura does not provide any basis for starting with the Figure 27C circuit or recommend the specific circuit elements and configuration of that circuit as opposed to any other embodiment or circuit configuration. Kimura simply lists numerous possibilities of ways to connect various elements. *See, e.g.*, Kimura at ¶ [0289] ("In the structures illustrated in...FIGS. 27A to 27C...the second terminal of the transistor 207 can be connected to a wiring that



is different from the node 13.... Alternatively, the first terminal of the transistor 207 can be connected to a wiring which is different from the wiring 115....”); *see also*, *e.g.*, Kimura at ¶¶ [0287], [0291], [0297] (listing other possible alternatives). Kimura provides no explanation as to why the permutation of options were implemented as shown in Figure 27C, or give a POSITA a reason to expect that configuration to be favorable or advantageous.

48. In my opinion, a POSITA would have had no reason to look to the Figure 27C circuit as opposed to any other. This is underscored by the fact that, as I explain in greater detail below, the timing diagram that Dr. Foty and the Petition rely upon as operative for the Figure 27C circuit is not consistent with the operation of the circuit described in Kimura. For this additional reason, a POSITA would not have looked to the Figure 27C circuit, or, absent disclosed timings, had a reasonable expectation of success in implementing that circuit in the manner that Dr. Foty and the Petition suggest.

A. The Petition Misinterprets Kimura.

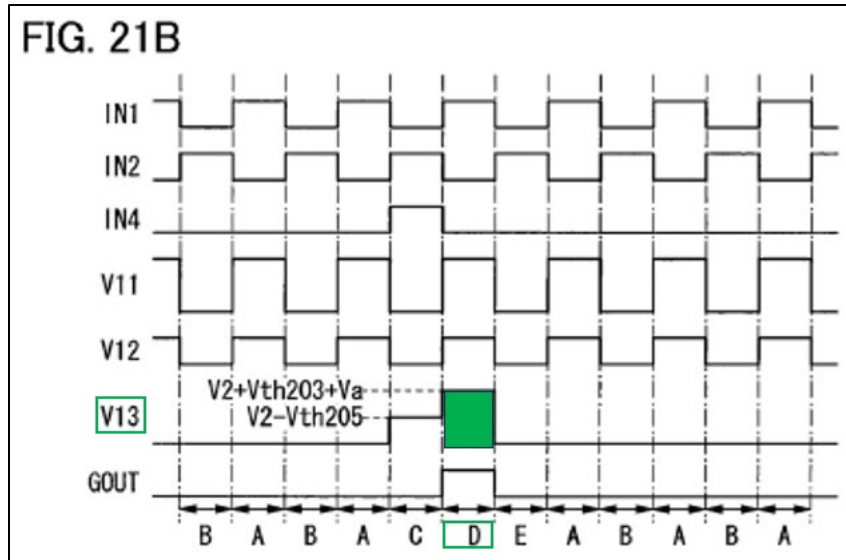
49. Claim elements [1-A] and [15-D] are directed to “an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node.”

[REDACTED]

50. Dr. Foty and the Petition point to Figure 27C for these limitations, but the citations provided do not reflect a discussion of the Figure 27C circuit, but instead refer to different circuits taught by Kimura. *See, e.g.*, Ex. 1003, ¶¶ 156-164; Pet. at 18 (citing discussions related to Figs. 18A, 19A, 19B, e.g., Kimura ¶¶ [0253]-[0256]). Neither Dr. Foty or the Petition provide a reason why a POSITA would look through the disclosures of Kimura relating to other circuits and embodiments in order to understand the operation of the Figure 27C circuit.

51. Notably, Dr. Foty and the Petition point to the timings provided in Figure 21B as part of the analysis for claim elements [1-A] and [15-D]. Pet at 19. Dr. Foty acknowledges that this timing diagram is not “specific to the device of Figure 27C,” but asserts that a POSITA would have understood that the timings of Figure 21B would still apply to the Figure 27C circuit because that circuit “would be supplied with input signals in the same manner and with the same timing.” Ex. 1003, ¶ 160; *see also* Pet. at 19.

52. However, Kimura’s description of Figure 27C shows that it is not compatible with the timings shown in Figure 21B. Kimura explains that for the circuit shown in Figure 27C, “in a period D, the potential of the node 13 can be lowered.” Kimura ¶ [0286]. Contrary to this description, however, during period D shown in (annotated) Figure 21B below, the potential of node 13 (V13) is depicted to be at its highest level:



53. Dr. Foty does not address this discrepancy or explain why a POSITA would still understand Figure 21B's timings to be compatible with the Figure 27C circuit. In my opinion, they would not. The timings shown in Figure 21B are inconsistent with Kimura's discussion of transistor 204 in Figure 27C, and do not show the lowered potential on which Dr. Foty and the Petition rely. Figure 21B also shows fewer input signals than 27C requires. Moreover, Dr. Foty has not identified which claim limitation corresponds to each signal in Figure 21B under his theory. Ex. 1003 at ¶ 160.

B. Kimura Does Not Teach or Suggest Claim Elements [1-D]/[15-G].

54. Claim elements [1-D] and [15-G] require that “the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver.”



55. Dr. Foty and the Petition point to transistor 204 as meeting this limitation, because, under their theory, it is the only transistor in the Figure 27C circuit that has its “on/off operation” “directly control[led]” by the “signal of the third input terminal” as required by the claim. Ex. 1003, ¶ 188. Dr. Foty also relies upon this same transistor for the requirements of claim elements [1-B]/[15-E], that the “first driver” must also control the voltage of the second node “in accordance with signals of the first input terminal, the second input terminal, and the third input terminal.” In particular, Dr. Foty and the Petition point to the portion of Kimura that describes that transistor 204 has its gate “connected to wiring 112” (which Dr. Foty identifies as the “third input terminal”). Dr. Foty further states that because of this connection, transistor 204 “controls” the voltage of node 13 by lowering its potential, as Kimura describes in ¶ [0286]. But Kimura provides no other explanation of how this lowering occurs. Dr. Foty also does not explain how this lowering would satisfy the requirement that the first driver “control[s] the voltage of the second node in accordance with” the signal of the third input terminal. For example, Dr. Foty does not appear to suggest that transistor 204 “controls” the voltage of node 13 in accordance with the signal of wiring 112 (the identified third input terminal) to turn on or off transistor 203 (the transistor that has its gate connected to node 13) which controls whether the signal of wiring 112 is provided to wiring 211.

[REDACTED]

56. Additionally, the timing diagram in Figure 21B that Dr. Foty points to as applying to the Figure 27C circuit does not reflect a lowered potential of node 13. In fact, Figure 21B shows that during the referenced point in the operation of the Figure 27C circuit (period D) the potential of node 13 is at its *highest* potential. See Kimura Fig. 21B and ¶ [0286].

57. A POSITA would thus not understand the Figure 21B timings to apply to the Figure 27C circuit, and Kimura provides no further explanation from which to determine how to drive the circuit to achieve the alleged lowered potential. Accordingly, a POSITA would not have looked to the Figure 27C circuit, nor would they have had a reasonable expectation of success in implementing that circuit without timings.

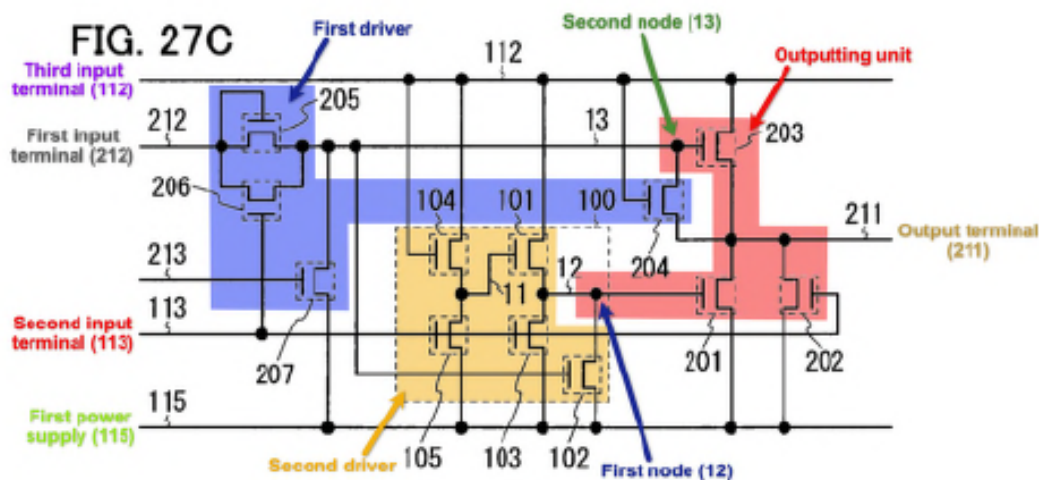
C. Kimura Does Not Teach or Suggest Claim Elements [1-A]/[15-D] and [6-B]/[20-B].

58. Claim elements [1-A] and [15-D] require “an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node.”

59. Dr. Foty identifies transistor 201 as part of the “outputting unit” in his analysis of claim 1. But for claims 6 and 20, which require “a second transistor and a third transistor serially positioned between the second node and the first power

supply,” Dr. Foty must instead place transistor 201 in the “first driver,” along with other changes to the identified elements in the “outputting unit” and “first driver.” There is no apparent reason for this other than to arrive at the separate limitations of the dependent claims, but neither Dr. Foty nor the Petition explain how the modified identification would read on the requirements of the independent claims on which these dependent claims depend.

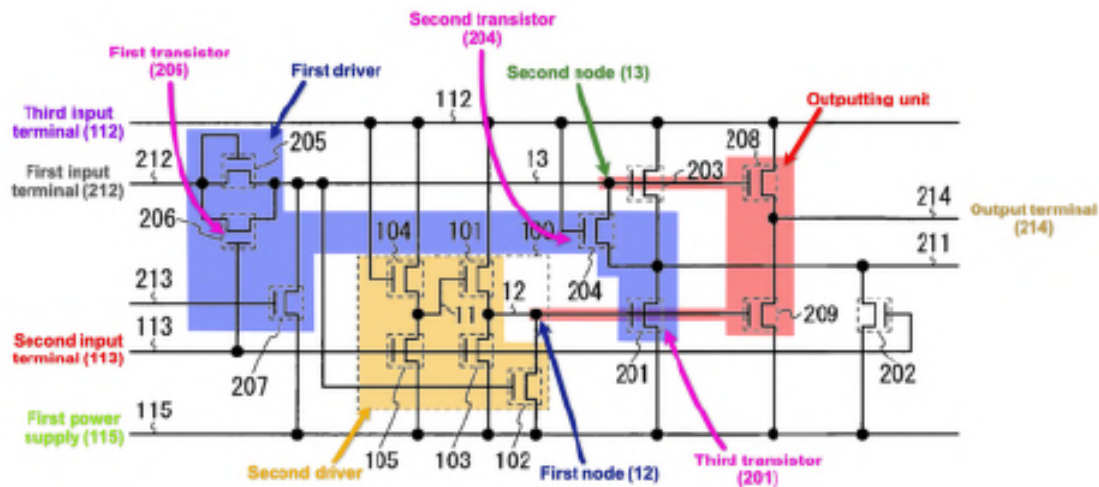
60. To illustrate, for claims 1 and 15, Dr. Foty identifies transistors 204, 205, 206, and 207 as part of the “first driver,” and transistors 201, 202, and 203 as part of the “outputting unit.”



Pet. at 15 (annotating Fig. 27C for claims 1 and 15); Ex. 1003 at ¶ 145.

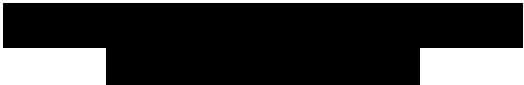
61. In contrast, for claims 6 and 20, which depend on claims 1 and 15 respectively, Dr. Foty identifies transistor 201 as part of the “first driver,” and purports to add two additional transistors, 208 and 209, which he now identifies as

part of the “outputting unit.” Dr. Foty no longer identifies transistors 203 and 202 as part of either the “first driver” or “outputting unit” under this modified analysis.



Pet. at 31 (annotating composite of Fig. 27C and Fig. 31B for claims 6 and 20); Ex. 1003 at ¶ 241.

62. Dr. Foty states that transistor 201 “operates to connect wiring 115 to node 13 (the second node) via transistor 204.” Ex. 1003 at ¶ 242. However, neither Dr. Foty nor the Petition suggest that transistor 201 would operate any differently if the additional transistors from Figure 31B were added. Dr. Foty also does not explain why this transistor should be considered part of the “outputting unit” for claims 1 and 15, but part of the “first driver” for claims 6 and 20. In my opinion it should not be, because it controls whether signals are provided to the output terminal 211, in both the Figure 27C circuit as well as the composite Figure 27C and Figure 31B circuit Dr. Foty creates.



63. As shown in the Figures above, transistors 201 and 204 are located in the same positions in both Figure 27C and the composite of Figures 27C and 31B. Accordingly, transistor 201 could (and should) be identified as part of the “first driver” under Petitioner’s theory for claims 1 and 15. However, in Figure 27C, if transistor 201 were identified as part of the first driver, the alleged “outputting unit” would not “supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node” as Dr. Foty suggests. In particular, for that limitation of claims 1 and 15, Dr. Foty relies upon the same transistor 201, which has its gate connected to the alleged “first node,” to satisfy this requirement of the “outputting unit.” Ex. 1003, ¶ 175. If transistor 201 were instead identified as part of the “first driver,” there would be no element in the “outputting unit” that would allow for the “outputting unit” to “supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node” as the claims require.

64. Dr. Foty and the Petition instead add a different purported “outputting unit” to Figure 27C in the form of two additional transistors and an additional “output” signal line in Figure 31B. Dr. Foty points to these elements as the new “outputting unit,” and identifies transistor 201 as part of the “first driver” instead. Ex. 1003 ¶ 243. It bears mention that this proposed modification results in a stage circuit now having 14 transistors and at least 4 input signals.

[REDACTED]

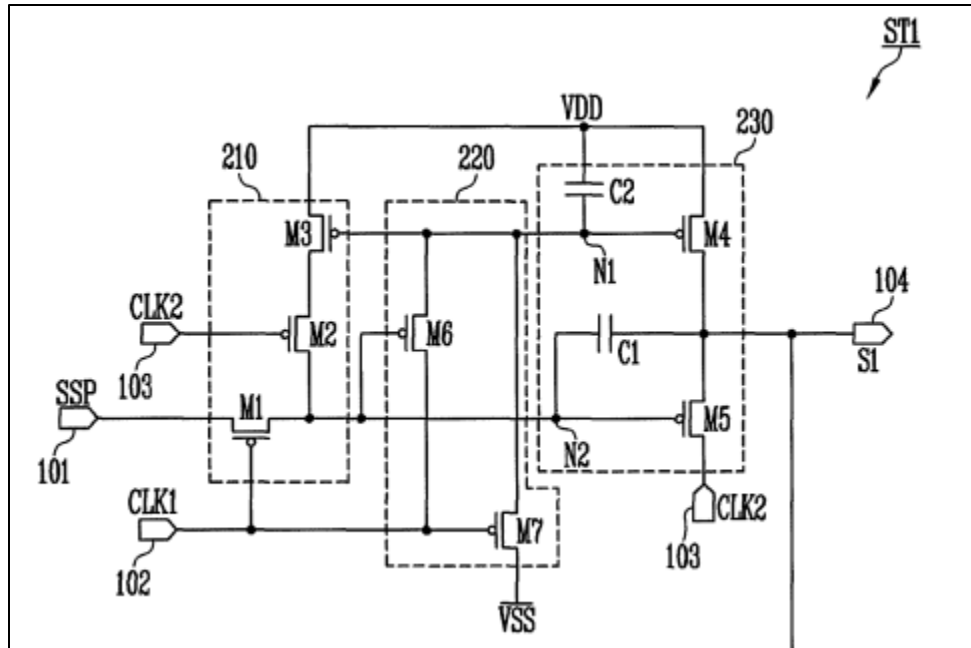
65. Dr. Foty suggests that a POSITA would have made these modifications because they would have improved “shift register operation.” Ex. 1003, ¶ 245. He does not elaborate further as to why providing two additional transistors to the stage circuit would improve its operation, or address the detriments of adding additional circuit elements a POSITA would have been familiar with. Moreover, his argument underscores a problem of scale with adding additional circuit elements to a stage circuit. In particular, a display will typically have one stage circuit for each row of pixels in the display, which is used to generate the scan signal provided to the corresponding row of pixels. Where a large number of stages are used, each of those stages must have the additional transistors and signal lines added. Thus, the larger number of stages only serves to compound the additional complexity, which further exacerbates the problems of manufacturability and efficiency a POSITA would recognize come with adding circuit elements to an existing design. Dr. Foty does not address these concerns, but a POSITA would have been well aware of them and taken them into account when designing a stage circuit. For example, as described above, the ’593 Patent explains that its invention allows for a reduction in the number of transistors and signal lines, and describes specific benefits associated with these reductions. *See, e.g.*, ’593 Patent, 9:12-26. A POSITA would not have added these circuit elements and incurred these significant downsides absent clear benefits. Indeed, Kimura itself describes that when “[t]he number of transistors is reduced,”

[REDACTED]

“layout area can be decreased” and “power consumption can be reduced.” Kimura ¶ [0301].

66. Additionally, Dr. Foty does not explain how the modified circuit he proposes for dependent claims 6 and 20 would meet the requirements of independent claims 1 and 15, under this shifted analysis. But in any event, even under that shifted analysis, the modified circuit does not meet the requirements of claims 6 and 20, because the elements identified as part of the new “outputting unit” do not provide scan signals to the output terminal 211 previously identified for claim 1. Transistors 208 and 209 instead control the provision of signal SOUT to wiring 214. As Dr. Foty acknowledges, “the signal SOUT is not output to the wiring 211 but can be input to a semiconductor device in a different stage as a start pulse.” Kimura ¶ [0304]. Dr. Foty acknowledges that the SOUT signal is a “different” signal than GOUT. Ex. 1003 at ¶ 239.

67. As Dr. Foty acknowledged for claim 1, GOUT is the signal that is output to the scan lines that provide scan signals to the rows of pixel circuits. Kimura ¶ [0304]; Ex. 1003 at ¶ 143. The ’593 Patent makes clear that the “output terminal” provides an output scan signal to the pixel circuits via scan lines 211. For example, as shown in Figure 3, the output terminal 104 connects to the scan lines Sn, which provide output scan signals to the pixel circuits.

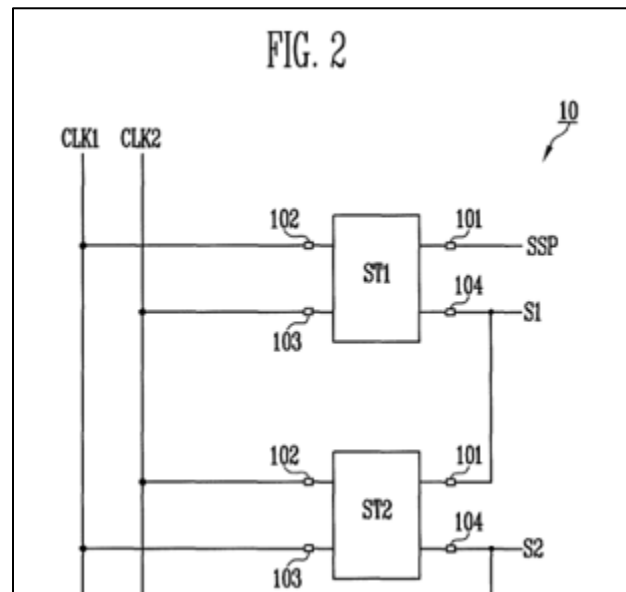


'593 Patent, Fig. 3 (excerpted); *see also, e.g.,* '593 Patent, Fig. 1.

68. This is further illustrated by the language of claim 15, which recites “a scan driver for supplying scan signals to the pixels through the scan lines, the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals.” Thus, the “output terminal” connects the stage circuits to scan lines that are in turn connected to the pixel circuits. *See also, e.g.,* '593 Patent, 7:46-48 (“In this case, the output terminal 104 outputs the second clock signal CLK2 as a scan signal to the scan line S1”); '593 Patent, 8:15-17 (“In practice, the stages ST repeat the above-described processes to sequentially output the scan signals to the scan lines.”).

69. Additionally, while the '593 Patent explains that the output of a previous stage can be provided as an input to a subsequent stage, in the embodiments

of the '593 Patent the same signal is provided to both the output terminal (and thereby to the pixels via the scan lines) as well as to the subsequent stage as an input. This is shown, for example, in the excerpt of Figure 2, below, which shows that the same signal provided to the output terminal 104 of stage ST1 is also provided to the input terminal 101 of the subsequent stage ST2.



'593 Patent, Fig. 2; see also '593 Patent, Fig. 3.

70. In contrast, Kimura's GOUT is provided only to the scan lines, while the different SOUT signal is provided only to the subsequent stage (and not to the scan lines). Thus, even if SOUT and GOUT were considered to collectively be the output signal, transistors 201 and 203 would be part of the "outputting unit" rather than the "first driver," because those transistors control the provision of GOUT to wiring 211. Kimura ¶ [0304]; Figs. 27C, 31B.

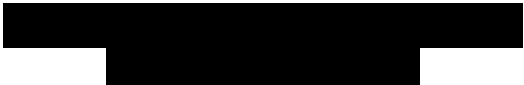
[REDACTED]

71. Accordingly, transistors 208 and 209, which control the output of SOUT to wiring 214, do not satisfy the requirements of the “outputting unit” of claim 1. Similarly, wiring 214 does not satisfy claim 1’s requirements of the “output terminal.”

D. Kimura Does Not Teach or Suggest Claim Elements [7-C]/[21-C] and [7-D]/[21-D].

72. Claim elements [7-C] and [21-C] require that the “outputting unit” include “a first capacitor between the second node and the output terminal.” Claim elements [7-D] and [21-D] require that the “outputting unit” include “a second capacitor between the first node and the first power supply.” The circuit shown in Figure 27C, on which Dr. Foty relies for independent claims 1 and 15, does not include any capacitors, let alone capacitors in the alleged “outputting unit.”

73. Dr. Foty and the Petition assert that a POSITA would have added two capacitors to Kimura’s Figure 27C to arrive at these requirements of claims 7 and 21. Ex. 1003 at ¶ 248. As an initial matter, I do not agree with the Petition’s assertion that “[c]apacitors can be added in various places.” Pet. at 32. A POSITA would not add circuit elements like capacitors to a circuit design absent clear benefits, and would consider the detriments I mentioned previously as part of the analysis of whether to modify a design to add additional circuit elements. For example, and as discussed below, it was known that adding capacitors increases circuit footprint. In my opinion, the additional capacitors cannot be viewed as anything but hindsight.



74. Dr. Foty looks to Figure 9C and Figure 30C, and asserts that Kimura “advises that ‘[c]apacitors can be additionally provided’ along with the transistors in its shift register.” Ex. 1003 at ¶ 258. Dr. Foty cites to Kimura ¶ [0198], but this paragraph says nothing about adding capacitors to Figure 27C. Kimura ¶ [0198] (“In the structures illustrated in FIG. 1A, FIGS. 6A to 6F, FIGS. 7A to 7E, FIGS. 9A and 9B, and FIGS. 11A and 11B, the transistors can be replaced with capacitors. For example, the capacitors can be additionally provided without elimination of the transistors.”). This does not suggest that these capacitors from different embodiments can or should be added to Figure 27C. Nor is there any explanation of how the timing or operation of the proposed design would not substantially change due to the addition of these capacitors and the delays they induce.

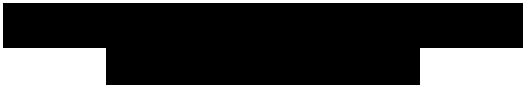
75. Dr. Foty’s application of these capacitors is also inconsistent with Kimura’s description of the embodiments from which he proposes to take the capacitors. For example, Kimura describes that the embodiment of Figure 9C is directed to a “circuit 120” that can be added to circuit 100 in Figures 1A, 6A-6F, 7A-7E, and 8A-8F to delay the provision of signal IN2 in those circuits. Kimura ¶ [0190]. Kimura never discusses adding circuit 120 to other embodiments, and indeed, no circuit 120 appears in Kimura’s Figure 27C. Additionally, in Figure 9C, circuit 120 consists of a resistor 121 in addition to capacitor 122. Dr. Foty only takes the capacitor from Figure 9C, which is contrary to Kimura’s disclosures that circuit 120

[REDACTED]

must include “at least a capacitance component and a resistance component.” Kimura ¶ [0191]. Thus, not only does Kimura not suggest adding this capacitor to Kimura’s Figure 27C, but Dr. Foty further seeks to add it in a manner contrary to Kimura’s teachings. Dr. Foty makes no effort to show how a circuit with a resistor and a capacitor could or would be added to its base figure, Figure 27C.

76. Additionally, Dr. Foty does not appear to take into account Kimura’s emphasis on reducing transistor deterioration. *See, e.g.*, Kimura, Abstract (“A semiconductor device including a circuit which does not easily deteriorate”); ¶ [0008] (“Alternatively, in the semiconductor device further including a seventh transistor, deterioration of the first to seventh transistors is suppressed.”). For example, Kimura describes that reducing transistor on time may “suppress” transistor deterioration. *See, e.g.*, Kimura ¶ [0228] (“Thus in a period during which the transistor 201 is on can be shortened. Accordingly, deterioration of the transistor can be suppressed.”). In Dr. Foty’s proposed modification, capacitor 122 is connected to the gate of transistor 201. Ex. 1003 at ¶ 248. This will serve to prolong the on time of transistor 201, rather than reduce it.

77. Dr. Foty similarly proposes to connect capacitor 220 to the gate of transistor 203. Ex. 1003 at ¶ 248. This is also inconsistent with Kimura’s description of Figure 27C, which, as described above Kimura states will reduce the potential of node 13. Kimura ¶ [0286]. In contrast, in describing Figure 30C (the configuration



from which Dr. Foty proposes to take capacitor 220), Kimura states that the presence of capacitor 220 will serve to raise the potential of node 13 during the bootstrap operation. Kimura ¶ [0303] (“the potential of the node 13 is likely to rise in the bootstrap operation.”). Dr. Foty does not address this discrepancy or explain why a POSITA would look to Figure 27C for lowering the potential of node 13, yet seek to modify Figure 27C to include a capacitor that Kimura states will raise the potential of that same node. In my opinion, a POSITA would not.

78. The Petition asserts that “Kimura itself contemplates that the capacitors can be employed” and that the “device’s output signal is improved when the capacitors are used.” Pet. at 34. Setting aside that, as discussed above, Kimura does not teach or suggest adding capacitors to Figure 27C, and that the Petition adds them in a manner inconsistent with Kimura’s teachings, Petitioner and Dr. Foty again overlook the significant detriments that would be incurred by adding two capacitors to a stage circuit. Capacitors take up significant circuit area, and this, along with the necessary connections to other circuit elements would have to be taken into account in designing a modified stage circuit. Generalized assertions that these capacitors could be added to Figure 27C would not provide a POSITA sufficient motivation to incur these detriments.

79. Dr. Foty’s citations to Jeong and Moon, different references disclosing different circuits, with no further explanation, that he alleges would “solve”

[REDACTED]

generalized concerns such as EMI or crosstalk, Ex. 1003 at ¶ 257, with which a POSITA would have already been familiar and taken into account in the design stage, similarly fail to provide an adequate motivation.

E. Kimura Does Not Teach or Suggest Claim Elements [8-A]/[22-A] and [8-B]/[22-B].

80. Claim elements [8-A] and [22-A] require that the second driver include “a sixth transistor between the first node and the second input terminal, the sixth transistor having a gate electrode coupled to the second node.” Claim elements [8-B] and [22-B] similarly require that the second driver include “a seventh transistor between the first node and a second power supply, the second power supply having a lower voltage than the first power supply, the seventh transistor having a gate electrode coupled to the second input terminal.”

81. Dr. Foty concedes that “none of Figure 27C’s transistors are connected in the way the claim requires,” and proposes modifications to Figure 27C in order to arrive at these claims. Ex. 1003 at ¶ 271. Dr. Foty does not even attempt to depict how the modifications it proposes would be made or explain how the resulting circuit would operate. Ex. 1003 at ¶¶ 271-278. Dr. Foty suggests that Kimura teaches that these modifications “can be” made, but cites to no disclosure of Kimura teaching that any of these modifications could be made to Figure 27C. Ex. 1003 at ¶¶ 271-278. Dr. Foty also provides no rationale for making these modifications, instead

[REDACTED]

suggesting that the needed changes would be a “design alternative.” Ex. 1003 at ¶ 271.

82. Dr. Foty does not explain why a POSA would seek to make these changes to the connections of the transistors in Figure 27C, let alone explain how the resulting circuit would operate. The proposed modifications are also inconsistent with Kimura’s descriptions. For example, Dr. Foty states that “the first terminal of the transistor 102’ can be ‘connected to the wiring 113’ instead of wiring 115,” and that with this modification, transistor 102 is the claimed sixth transistor. Ex. 1003 at ¶¶ 272-273. Dr. Foty points to a description in Kimura that refers to Figure 7C as the basis for connecting transistor 102 to wiring 113 instead of wiring 115. Kimura ¶ [0169] (“FIG. 7C illustrates a structure where the first terminal of the transistor 102 is connected to the wiring 113”); *see also* Kimura ¶ [0168] (listing only Figs. 1A, 6A-6F, and 7A-7 as structures in which “the first terminal of the transistor 102 can be connected to a wiring which is different from the wiring 115”).

83. However, in the Figure 7C configuration, transistor 102 has its gate connected to wiring 114. In contrast, claims 8 and 22 require that the gate of the “sixth transistor” is connected to the “second node,” which Dr. Foty has identified as node 13. Dr. Foty does not cite any portion of Kimura that suggests that in modifying transistor 102 to be connected to wiring 112 instead of wiring 115 (as



Kimura describes for Figure 7C) that the gate of transistor 102 would be connected to node 13 rather than wiring 114 (as it is in Figure 7C).

84. Dr. Foty's theory also requires, in addition to changing the connections of the transistors in Figure 27C as he concedes, adding an additional power supply line to Figure 27C. Dr. Foty provides no explanation whatsoever for this proposed modification. Ex. 1003 at ¶¶ 274-278. Dr. Foty simply suggests that "Kimura also teaches that the same stage circuit can be provided with multiple different power supply voltages." Ex. 1003 at ¶ 274. For claims 1 and 15 Dr. Foty and Petitioner identify wiring 115 as the "first power supply." Ex. 1003 at ¶ 152; Pet. at 18. For claims 8 and 22, Dr. Foty points to a different embodiment (Figure 30A) and suggests that wiring 115b in that embodiment would satisfy the "second power supply" limitation of those claims. Ex. 1003 at ¶¶ 274-275. Dr. Foty does not explain what would be the "first power supply" in the proposed modification, explain what voltages would be provided by the purported "first" and "second" power supplies, or explain how the resulting modified circuit would function.

85. As one example, Dr. Foty points to Figure 30A (not Figure 27C), and suggests that in that Figure, "transistor 105 is connected to a different power supply with a different voltage (wiring 115) than its output transistor 201 (wiring 115D)." Ex. 1003 at ¶ 274. But Kimura explains for Figure 30A that "the voltage V_1 can be supplied to the wirings 115A to 115E." Kimura ¶ [0299]. Dr. Foty points to nothing

[REDACTED]

in Kimura to suggest that these wirings would be connected to different power supplies, let alone any reason for a POSITA to provide an additional power supply. Dr. Foty suggests that “[t]he use of more-than-one power supply voltage level” is “a common and well-known practice in circuit design and circuit operation,” but provides no reason why a POSITA would seek to use multiple power supplies when Kimura teaches that a single power supply (i.e., to supply the voltage V_1 which Kimura explains can be provided to both 115B and 115D) will suffice. Ex. 1003 at ¶ 274. Dr. Foty similarly fails to point to any disclosure in Kimura that would suggest that these multiple power supplies would provide the voltage levels required by the claims (i.e., a second power supply having a lower voltage than the first power supply).

86. Finally. Dr. Foty does not take into account the downsides incurred by adding multiple additional circuit elements and modified connections between them. For example, Dr. Foty does not address Kimura’s teachings that reducing power sources results in improved reliability and yield and reduces manufacturing costs. Kimura ¶ [0196].

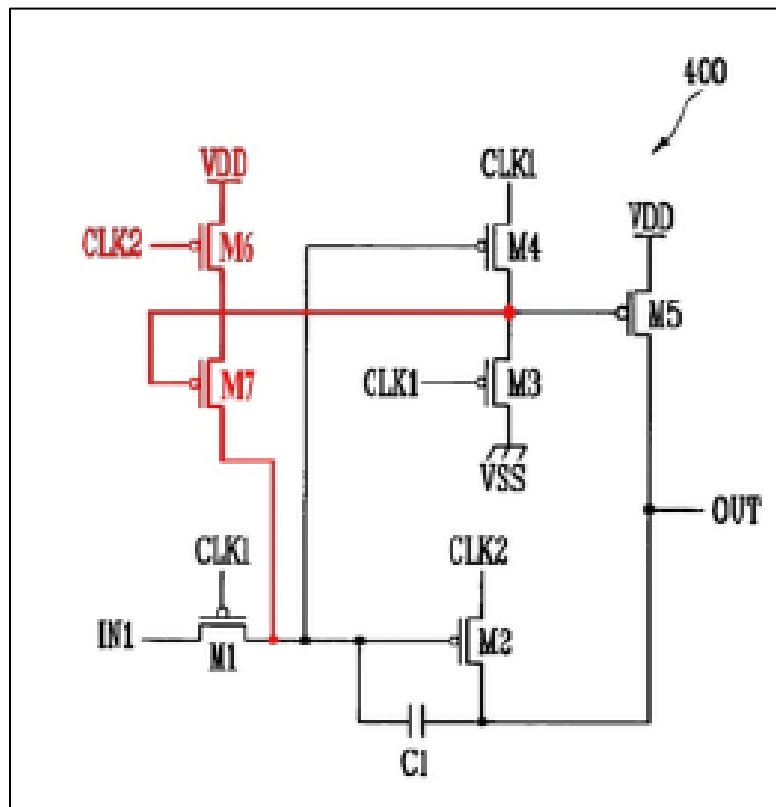
IX. SHIN IN VIEW OF SASAKI DOES NOT RENDER OBVIOUS ANY CHALLENGED CLAIM.

87. Dr. Foty’s analysis of the combination of Shin and Sasaki relies upon a composite circuit taking elements from Shin and elements from Sasaki, that is not taught or suggested by either reference. Taking these circuit elements and connecting

them in the specific ways required to arrive at the claims would have involved significant modifications that a POSITA would not have sought to make. Further, Shin already addresses the only reason Dr. Foty provides as to why a POSITA would have thought to modify Shin, and instead seeks to modify Shin in a way that is further inconsistent with Sasaki's teachings. In my opinion a POSITA would not have made these modifications, which appear to be nothing more than a hindsight-driven attempt to arrive at the claims.

A. Shin Already Addresses the Purported Issue for Which Petitioner Proposes to Add Circuitry from Sasaki.

88. As shown below, Dr. Foty takes two transistors from Sasaki (red) and apply them to Shin's Figure 11:



[REDACTED]

Ex. 1003 at ¶ 390. All of Dr. Foty’s arguments regarding the Shin and Sasaki combination require combining these elements in this exact way. *See, e.g.*, Ex. 1003 at ¶ 390; Pet. at 53.

89. The only rationale Dr. Foty provides for adding these additional transistors (and connecting them in the specific manner, with the specific inputs shown above) is the unsupported assertion that there is “a potential deficiency in this stage circuit of Shin, because the node at the gate of M2 could be subject to reversal.” Ex. 1003 at ¶ 368; *see also, e.g.*, Pet. at 47. Dr. Foty asserts that a POSITA would have been aware of this “potential” issue and would have looked to Sasaki to address it. Dr. Foty is incorrect, because Shin already addresses this purported issue with its capacitor C1. Dr. Foty has not identified any reason why C1 is inadequate.

90. As Dr. Foty acknowledges, Sasaki explains that the reversal it is concerned with occurs when the node n2 may be in a floating state. Ex. 1003 at ¶ 372. In other words, when no signal voltage is being supplied to the node, there is a possibility for voltage of the node to switch from the intended level to a different level. Sasaki ¶ [0042]. Thus, the reversal that Dr. Foty describes may occur when a node is in a “floating” state. And Dr. Foty suggests that a POSITA would realize that Shin is susceptible to this issue and would look to Sasaki to add two additional transistors to Shin’s circuit to address this “potential” issue.

[REDACTED]

91. But this overlooks that Shin already contains a capacitor, C1, which is connected to the gate of transistor M2, and addresses the “potential” issue of reversal due to a node in a floating state. Specifically, Shin explains that when the node at the gate of transistor M2 is in a floating state, the capacitor C1 maintains the intended voltage of that node. *See, e.g.*, Shin ¶ [0107] (explaining that when “a gate terminal of the second transistor M2 is in a floating state, a voltage of the capacitor C1 remains unchanged, and thus the second transistor M2 continues to be turned-on”).

92. Dr. Foty tacitly admits that Shin already addresses the floating state of the node at the gate of transistor M2 with its capacitor C1, but seeks to dismiss Shin’s teachings by asserting, without citation, that “this capacitor will not provide adequate anti-reversal protection.” Ex. 1003 at ¶ 385. Dr. Foty appears to overlook Shin’s express teaching, as described above, that capacitor C1 maintains the intended voltage of the node in question when it is in a floating state. *See, e.g.*, Shin ¶ [0107]. Dr. Foty contends that in certain time periods C1 may be “unable to fully guarantee reversal protection.” Ex. 1003 at ¶ 385. But this is contradicted again by Shin’s provision of capacitor C1 and its teaching that C1 is sufficient to maintain the intended level at the gate of transistor M2. *See, e.g.*, Shin ¶ [0107]. Given that transistor M1 is enabled by a clock, the maximum time for which C1 must maintain its signal is known at design time and can easily be guaranteed. Dr. Foty points to nothing beyond generalized references to electromagnetic interference or crosstalk

[REDACTED]

in support for his theory that Shin's circuit may still be susceptible to reversal. But these are considerations that a POSITA would take into account in designing a circuit, and Shin teaches a circuit including a capacitor C1 that it teaches addresses such concerns. And Dr. Foty points to nothing in Shin that suggests that its capacitor C1 would be insufficient for this purpose. Moreover, he does not show that the additional transistors would be a meaningful improvement as the operation of M7 is still tied to the timing of CLK1.

93. In my opinion, these generalized concerns would not motivate a POSITA to add two additional transistors to a stage circuit. A POSITA would look to Shin and understand that its capacitor C1 is sufficient for its stated purpose. The generalized concerns Dr. Foty points to would not be sufficient for a POSITA to incur the significant costs in both manufacturing and circuit complexity that stem from adding two additional transistors to a stage circuit. As a POSITA would have understood, adding additional elements to a circuit design will increase the footprint of the circuit. Indeed, prior art cited by Dr. Foty confirms as much. *See, e.g.*, Ex. 1006 at ¶ [0015], [0107] (describing "concern for increased circuit area").

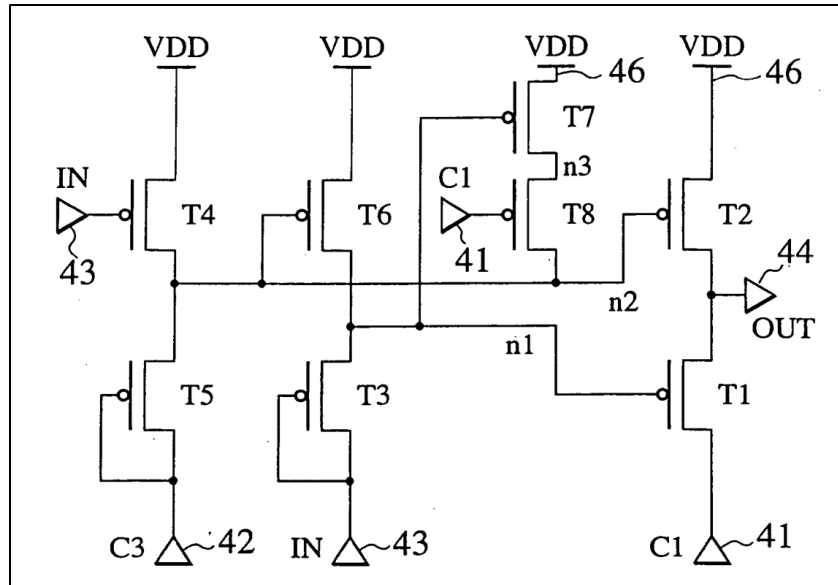
94. As the '593 Patent explains, adding elements to a circuit may increase complexity, decrease stability, and lower process yield. Ex. 1001 at 9:12-26. Any added circuit elements will require input signals and associated timings for those signals, and the timings of existing circuit elements may also be impacted. In

[REDACTED]

addition, the driver that provides certain input signals may need to be modified to provide any additional or altered timings to enable to modified circuit to function properly. Each of these factors are among the specific benefits provided by the inventions of the '593 Patent. Moreover, as previously discussed, changing the design of the stage circuit does not simply require adding two additional transistors, but two additional transistors to every stage circuit in the scan driver. Dr. Foty does not address these concerns, which would have further counseled a POSITA to not make the significant changes Dr. Foty suggests, particularly where Shin already teaches that its capacitor C1 solves the purported problem Dr. Foty raises.

B. Petitioner Applies Sasaki's Circuitry Inconsistently with Sasaki's Teachings.

95. Additionally, Dr. Foty also seeks to apply Sasaki's "anti-reversal" circuit in a way that is not consistent with Sasaki. Specifically, Sasaki is concerned with reversal of a particular node (its node n2), that Sasaki explains may be subject to reversal at a specific point in time in the operation of Sasaki's circuit. That is the point in time where a low voltage is intended to be provided as an output. *See, e.g.*, Ex. 1003 at ¶ 388. In Figure 4 of Sasaki, shown below, transistors T7 and T8 make up the "anti-reversal" circuit.



96. As shown in Figure 4, the node n2 is connected to the gate of transistor T2. Transistor T2 in turn controls whether the high voltage supply VDD is provided to the output terminal. As Sasaki explains, this is why it is concerned with reversal of node n2 at this particular time, because reversal at this time could cause the high voltage supply VDD to be provided to the output terminal instead of the intended low voltage from C1. Ex. 1014 at ¶ [0048]. Sasaki explains that the erroneous provision of VDD at this point in time can lead to unintended distortion of the output signal. Ex. 1014 at ¶ [0048] (describing that with no anti-reversal circuit, if node n2 is reversed “transistor T2 starts conducting and the high voltage VDD is supplied to the output terminal 44 through the second transistor T2[,]” resulting in a “distorted” output waveform.).

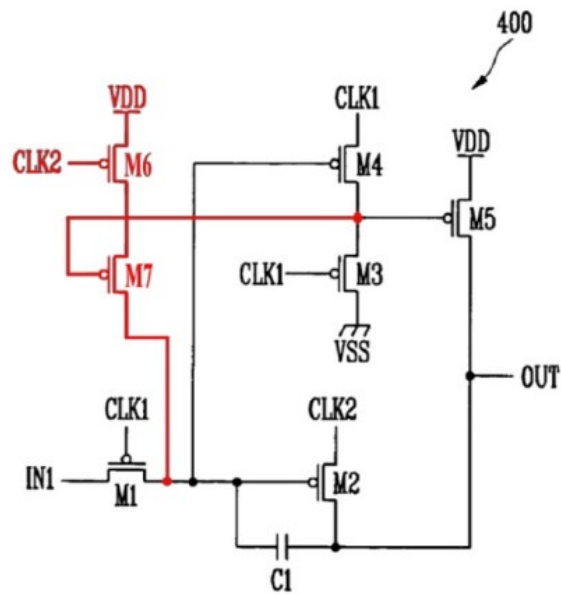
97. In fact, Sasaki repeatedly describes potential distortion when the intended output signal is low and VDD is erroneously provided to the output

[REDACTED]

terminal. *See, e.g.*, Ex. 1014 ¶ [0051] (“As a result, the output signal OUT at the low level without distortion will be supplied to the output terminal 44.”); *see also* Ex. 1014 at ¶¶ [0055], [0059], [0061], [0064], [0066]. Notably, Sasaki does not describe potential distortion in the opposite scenario (i.e., when the intended output signal is VDD but CLK2 is low and erroneously provided).

98. In Shin, the node connected to the gate of transistor M5 is the counterpart to Sasaki’s node n2, because that is the node in Shin that controls whether the high voltage supply VDD is provided to the output terminal. *See, e.g.*, Shin, Fig. 11. Thus, a POSITA looking at Shin and considering the issue of reversal raised by Sasaki would look at the node connected to the gate of transistor M5 as the node for which reversal may cause problematic output distortion.

99. But Dr. Foty does not apply the “anti-reversal” circuit of Sasaki to the node connected to the gate of transistor M5. Instead, he provides it to the opposite node (i.e., the node that controls whether the clock signal CLK2 is provided to the output terminal).



100. Importantly, this node (i.e., the node connected to the gate of transistor M2) does not have the same concern Sasaki describes for its node n2. As discussed above, Sasaki describes that the purpose of its “anti-reversal” circuit is to prevent distorted output due to providing a high signal when a low signal is intended. *See, e.g., Ex. 1014 ¶ [0051]*. But the node Dr. Foty connects the “anti-reversal” circuit to in Shin does not allow the high voltage VDD to be provided to the output terminal. Thus, reversal of this node would not cause the distortion for which Sasaki provides its “anti-reversal” circuit. A POSITA would thus have recognized that, in addition to capacitor C1 solving the “potential” issue Dr. Foty raises, providing the “anti-reversal” circuit as Dr. Foty suggests would be inconsistent with Sasaki’s teachings, and not provide the benefits Sasaki claims through its “anti-reversal” circuit.

[REDACTED]

X. SHIN IN VIEW OF SASAKI AND FURTHER IN VIEW OF JEONG DOES NOT RENDER OBVIOUS ANY CHALLENGED CLAIM.

101. Dr. Foty and the Petition propose to combine Shin and Sasaki with Jeong for claims 7 and 22. In particular, these claims require an additional capacitor in the claimed “outputting unit” that Dr. Foty acknowledges neither Shin nor Sasaki teaches or suggests. In my opinion, a POSITA would not have made the further modifications necessary to the composite circuit of Shin and Sasaki that Dr. Foty proposes in order to arrive at the further requirements of these claims.

A. Shin in View of Sasaki and Further in View of Jeong Does Not Render Obvious Claim Elements [7-D] and [21-D].

102. Claim elements [7-D] and [21-D] require that the “outputting unit” include “a second capacitor between the first node and the first power supply.” Dr. Foty acknowledges that his proposed combination of Shin and Sasaki does not include the second capacitor required by claim elements [7-D] and [21-D] and seeks to add a capacitor from Jeong to meet this requirement. Ex. 1003 at ¶ 574.

103. The only rationale Dr. Foty provides as to why a POSITA would seek to add an additional circuit element to the composite circuit of Shin as modified by Petitioner to include Sasaki’s “anti-reversal” circuit is potential “perturbations” due to EMI or crosstalk, and that a POSITA would seek to add additional circuit elements to make the composite Shin and Sasaki circuit “more robust.” Ex. 1003 at ¶ 579. As I previously explained, these sorts of generalized concerns would not motivate a

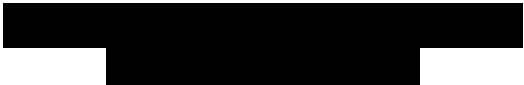
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POSITA to add additional circuit elements (and incur the additional costs previously noted).

104. Additionally, contrary to Dr. Foty's assertions, nothing in Shin or Sasaki suggests any operational issue with Shin or Sasaki's circuitry that would cause a POSITA to seek to add an additional capacitor. Notably, Shin intentionally added a capacitor (C1) where it was needed and did not add a capacitor where it was not. Additionally, Dr. Foty's arguments regarding why a POSITA would add an additional capacitor to the node at the gate of M5 is inconsistent with his argument that capacitor C1 would be insufficient for its stated purpose, such that a POSITA would seek to add two additional transistors in addition to capacitor C1.

105. In sum, the generalized concerns Dr. Foty notes would not be sufficient to cause a POSITA to look to add an additional capacitor, let alone connect it in the specific way Dr. Foty does in order to arrive at the requirements of the claims. Dr. Foty's citations to Jeong, which teaches a different circuit with different circuit elements and connections, would similarly not motivate a POSITA to add additional circuit elements to the composite Shin and Sasaki circuit Dr. Foty creates.

106. Dr. Foty also overlooks the detriments to adding additional circuit elements to a scan driver stage circuit, detriments with which a POSITA would have been well aware. For example, Tobita, on which Dr. Foty relies for other grounds, describes that capacitors detrimentally add significant circuit area. *See, e.g.,* Tobita

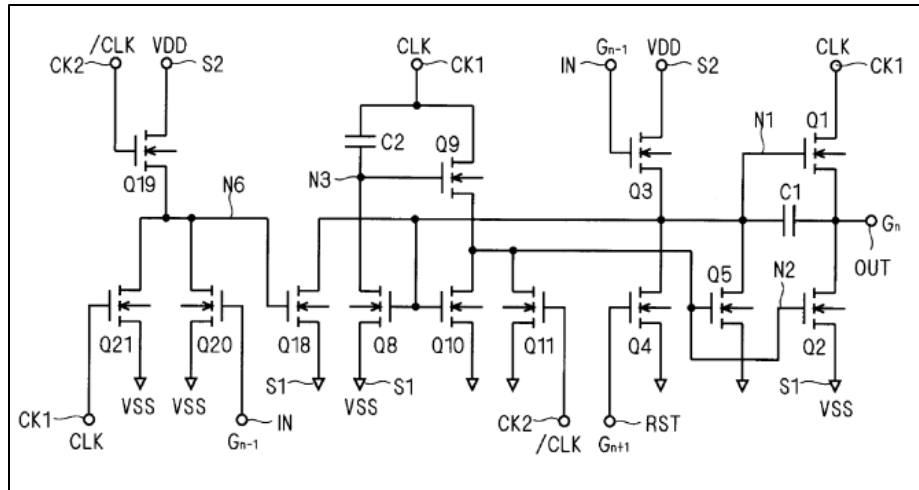


¶ [0015]. A POSITA would have been familiar with such detriments and would not have sought to add additional circuit elements absent a clear and specific reason to do so.

XI. TOBITA DOES NOT RENDER OBVIOUS ANY CHALLENGED CLAIM.

107. Tobita is directed to a scan driver shift register for a liquid crystal display. Tobita ¶ [0004]. Tobita describes an issue with conventional shift registers made of amorphous silicon TFTs, where degraded driving capability occurred because “a-Si TFT tends to have its threshold voltage shifted in the positive direction when the gate electrode is continuously positive-biased.” Tobita ¶ [0010]. Tobita describes that other approaches to addressing this issue required additional capacitive elements with “large capacitance” which led to “increases [in] the circuit area.” Tobita ¶ [0015]. Accordingly Tobita describes an approach intended to “control an increase in circuit area of a shift register while preventing malfunctions” Tobita ¶ [0016].

108. Tobita has 36 Figures and includes 21 different “preferred embodiments.” Dr. Foty relies on the eighth embodiment, which is shown in Figure 20:

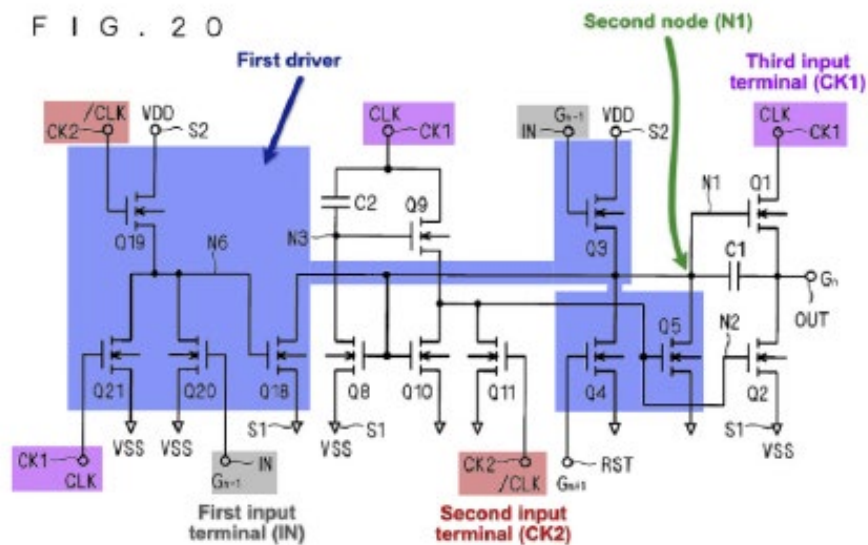


109. As an initial matter, Dr. Foty provides no explanation of why a POSITA would start with this embodiment as opposed to any other. Additionally, like Kimura's Figure 27C circuit, the eighth embodiment of Tobita includes many more transistors and input signals than the claimed invention of the '593 Patent. Moreover, Tobita's eighth embodiment addresses an issue specific to optical leakage current, which will more predominantly arise in a display that has a backlight (like an LCD), and thereby increase the amount of incident light. Tobita ¶ [0170]. In contrast, OLED displays do not have backlights, and so have no backlight leakage and are thus far less susceptible to the issue to which Tobita's eighth embodiment is directed. For these threshold reasons, a POSITA would not have looked to Tobita's eighth embodiment for implementing an OLED stage circuit.

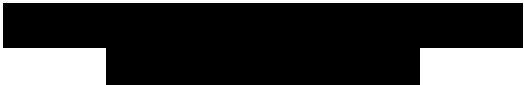
A. Tobita Does Not Teach or Suggest Claim Element [1-B]/[15-E].

110. Claim limitations [1-B] and [15-E] require a “first driver” that “control[s] the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal.”

111. As shown below, Dr. Foty identifies portions of Tobita’s Figure 20 encompassing seven different transistors (blue) as making up the claimed “first driver.” Ex. 1003 at ¶ 596.

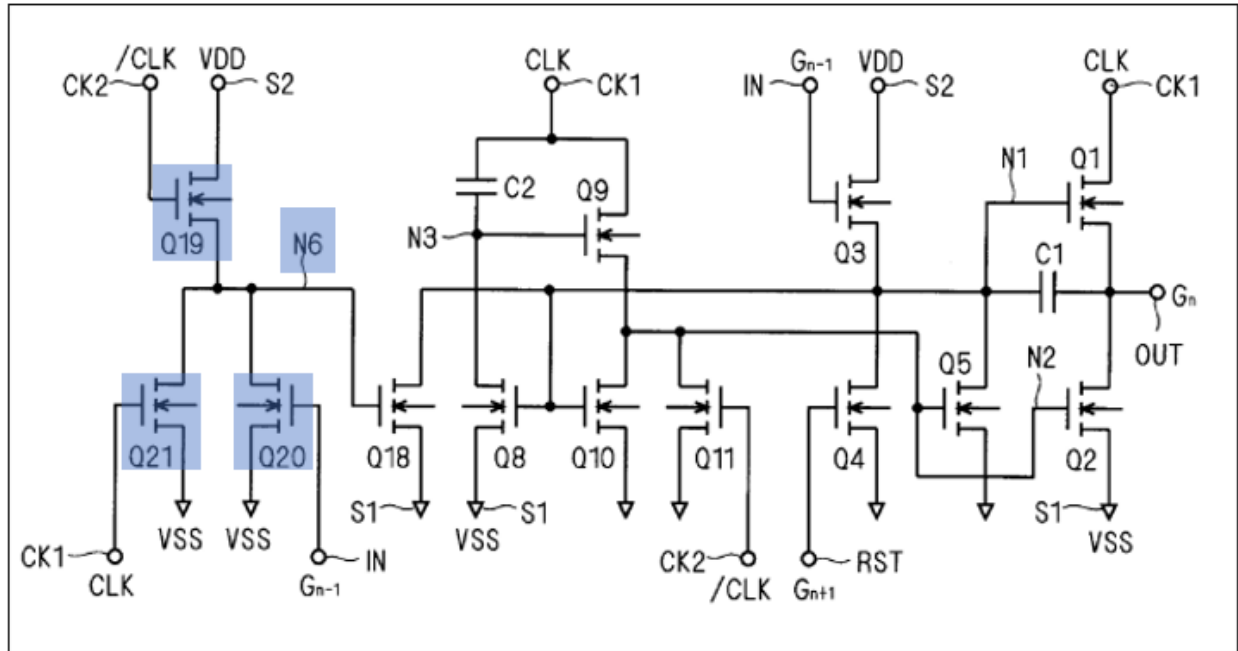


112. As mentioned previously, Tobita explains that its eighth embodiment is directed to preventing optical leakage current that may arise at a specific point in time in the operation of other of Tobita’s embodiments. Tobita ¶¶ [0170], [0171]. Tobita explains that this optical leakage may occur when Q3 is not diode-connected, but instead has its drain connected to VDD, as it is in both the seventh and eighth



embodiments. Tobita ¶¶ [0170], [0171], Figs. 19, 20. As Tobita describes, in this configuration, when node N1 is in a high impedance state, optical leakage current may flow from VDD to node N1 “under the influence of external light incident into the display or backlit light of a display panel” Tobita ¶ [0170]. To address this issue, in the eighth embodiment of Tobita, four additional transistors Q18, Q19, Q20, and Q21, are provided to prevent such leakage. Tobita ¶ [0170].

113. As Tobita makes clear, transistors Q19, Q20, and Q21 are provided to control the voltage of node N6. Tobita ¶¶ [0172]–[0178]. This is a different node than Tobita’s node N1, which Dr. Foty identifies as the claimed “second node.” Ex. 1003 at ¶ 596. More specifically, Tobita explains that transistors Q19 and Q20 operate as an “inverter circuit,” with node N6 “serving as the output node of the inverter circuit.” Tobita ¶ [0174]. Tobita also explains that Q21 operates to keep this output node “at the L level” at a particular period of operation of the stage circuit. Tobita ¶ [0177]. In other words, these transistors operate to control the voltage of the node N6. This can be further seen in Figure 20, as each of these transistors are connected to the node N6.

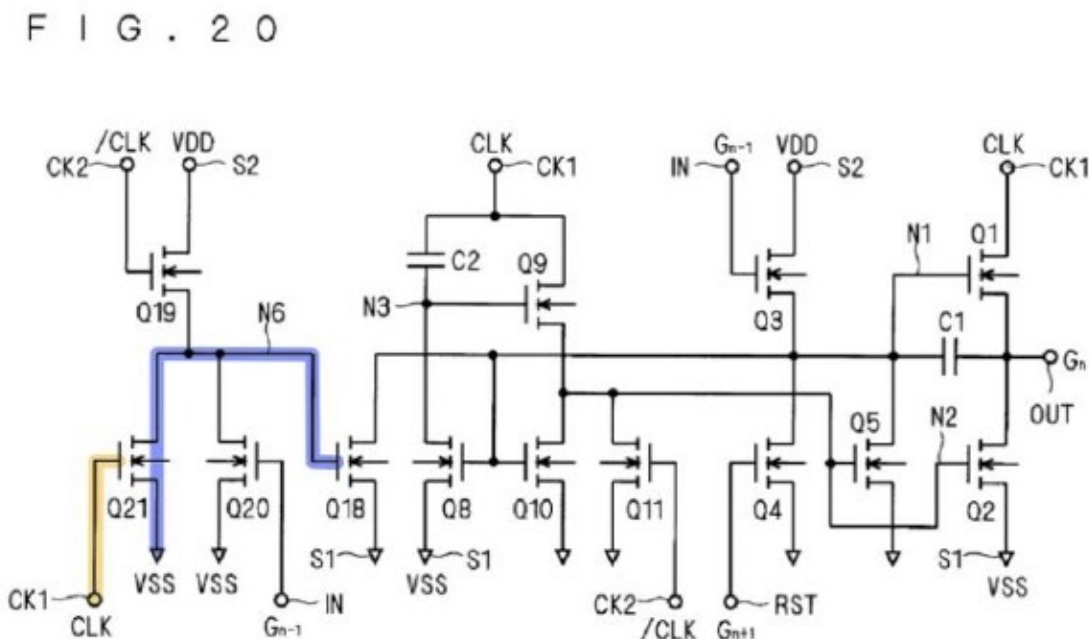


114. This means that transistors Q19, Q20, and Q21 do not control the voltage of the identified second node (N1) as this claim element requires, but rather a different node, node N6. Additionally, the voltage on node N6 is not passed to the node N1. Instead, the voltage on node N6 is passed to the gate of another transistor, Q18, to turn that transistor ON and OFF. Transistors Q19, Q20, and Q21 may thus control the voltage of node N6 in accordance with the signals of the identified input terminals (CK1, CK2, and IN), but they do not control the voltage of node N1 in accordance with the signals of those input terminals.

115. Additionally, the Petition's suggestion that transistors Q18-Q21 receive signals from the first, second, and third input terminals and "control the voltage of the node N1 by, e.g., bringing it to a low level," is not accurate. As reflected in Dr. Foty's analysis, this may be the case for transistors Q18-Q20, and the signals of the

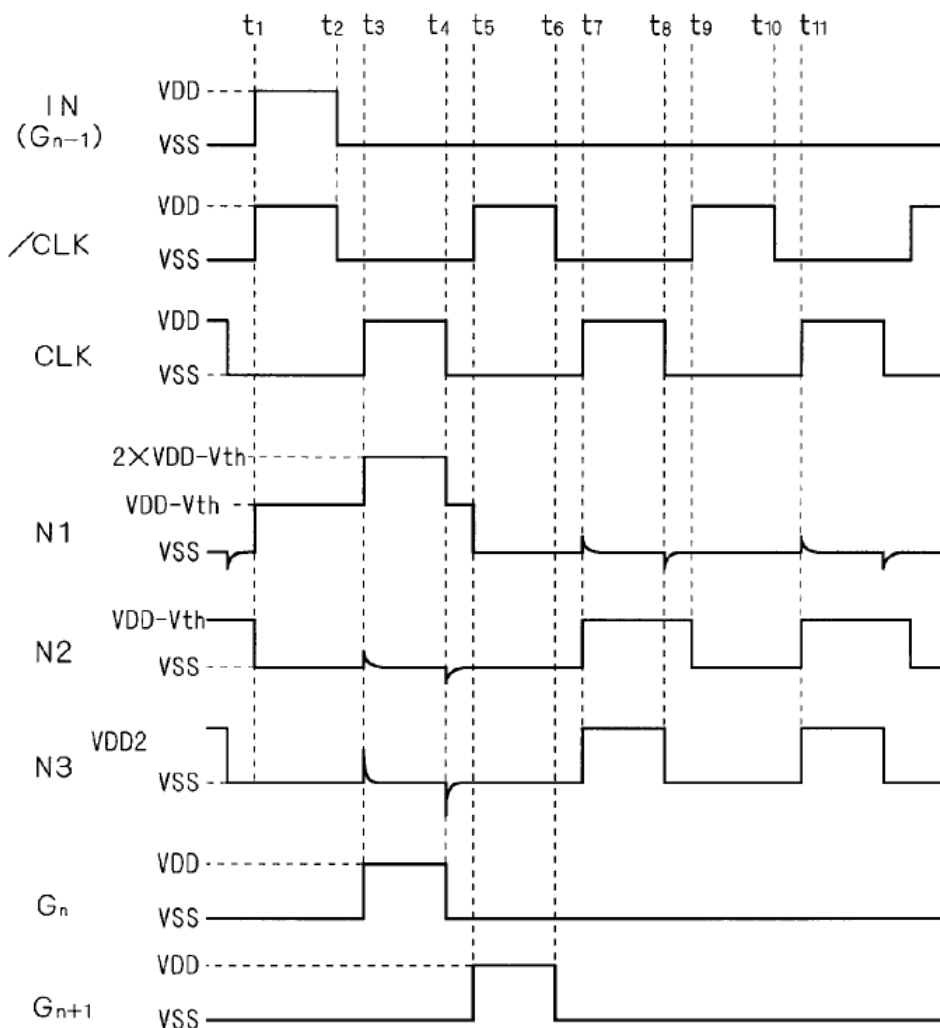
first and second input terminals. Ex. 1003 at ¶¶ 616-622. However, for the signal of the third input terminal, Dr. Foty points to transistor Q21 turning OFF. Ex. 1003 at ¶¶ 618-620. This does not control the voltage of the node N1 by bringing it to a low level. In fact, turning OFF transistor Q21 simply prevents VSS from being provided to the node N1 through transistor Q18, but the voltage of the node N1 remains the same.

116. This is shown, for example, in Dr. Foty's annotation of Figure 20, which reflects that when Q18 turns OFF because of the low signal provided to node N6, no signal is provided to node N1 through Q18:



117. This is further reflected in the timing diagram of Figure 9 of Tobita, on which Dr. Foty relies, which shows that during the time period when Q18 turns ON (period t7-to-t8), the voltage of node N1 remains at a low level.

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118. In my opinion, causing a transistor to turn OFF and thereby prevent a signal from being provided to a node, where the voltage of the node itself does not change, is not controlling the voltage of that node according to the '593 Patent. For example, the Patent teaches that the “first driver” controls the voltage of the second

[REDACTED]

node in accordance with the first, second, and third input terminals. *See, e.g., '593 Patent, 5:63-6:21.* In each case, the signals of the first, second, and third input terminals operate along with the transistors that make up the first driver to allow particular signals to be provided to the second node to change the voltage of the node. *See, e.g., '593 Patent, 6:41-8:17.*

119. Additionally, the '593 Patent does not suggest that because the first driver provides a signal to the second node, and the voltage on the second node causes other signals to pass through the circuit to the output terminal, that the first driver controls the voltage of the *output terminal* in accordance with the signals provided to the first driver. Such an interpretation would read any meaning out of the “control...in accordance with...” language, as it would allow for attributing any and all operational states of the circuit to initial inputs.

120. Finally, as I explained above, Tobita teaches that its eighth embodiment adds transistors Q18-Q21 to address a potential issue with optical leakage. Tobita teaches that, relative to other embodiments that do not include these transistors, Tobita's eighth embodiment provides the same output waveform. Specifically, Tobita explains that these transistors do not “affect the operation of the unit shift register SR_n of outputting the output signal G_n .” Tobita ¶ [0177]. This makes sense, as it is transistors Q1 and Q2 that allow signals to be provided to the output terminal, and those transistors have their gates connected to nodes N1 and N2, respectively,

[REDACTED]

rather than the separate node N6 that Tobita teaches is controlled by transistors Q19-Q21.

XII. TOBITA IN VIEW OF JEONG DOES NOT RENDER OBVIOUS ANY CHALLENGED CLAIM.

121. Claim elements [7-D]/[21-D] require that the “outputting unit” includes “a second capacitor between the first node and the first power supply.” Dr. Foty acknowledges that the identified “outputting unit” in Tobita does not include the claimed second capacitor. Ex. 1003 at ¶ 708. Dr. Foty proposes to add an additional capacitor from a different reference, Jeong, to arrive at this claim element.

122. As an initial matter, Dr. Foty does not identify any operational issues with the embodiment of Tobita on which he relies in support for his argument that a POSITA would understand to add an additional capacitor to Tobita. Ex. 1003 at ¶ 709. He instead makes similar arguments based on generalized concerns regarding EMI or crosstalk and suggests a POSITA would seek to add Jeong’s capacitor to make Tobita more “robust.” I have previously explained why these generalized concerns would not provide sufficient motivation to a POSITA to add additional circuit elements. A POSITA would not simply assume that there could possibly be such issues. Moreover, a given circuit will be specifically designed for its intended purpose, and a POSITA would not haphazardly add circuit elements without clear objectives or benefits.

[REDACTED]

123. In fact, Tobita explains that capacitors add significant circuit area, and Tobita is directed to reducing circuit area where possible. Tobita ¶ [0015]. Neither the generalized and unsupported concerns Dr. Foty identifies, nor Jeong’s teachings relating to a capacitor in a different circuit would provide sufficient motivation for a POSITA to add an additional capacitor to Tobita’s circuit. Moreover, Tobita includes a capacitor, C1, in the identified “outputting unit,” yet does not include the additional capacitor Petitioner proposes to add. Tobita, Fig. 20. This further confirms that the generic considerations Petitioner advances (of which Tobita’s author would have been similarly aware) would not motivate a POSITA to add a capacitor to Tobita as Petitioner suggests, let alone connect it in the specific way Petitioner does, which is necessary to arrive at the claims.

XIII. OBJECTIVE INDICIA OF NON-OBVIOUSNESS FOR THE ’593 PATENT

124. Samsung Display’s counsel has asked me to provide an opinion as to whether the non-obviousness of the challenged claims of the ’593 Patent is supported by objective indicia of non-obviousness.

125. It is my opinion, based on my review of the evidence discussed in this declaration, that the non-obviousness of the challenged claims of the ’593 Patent is supported by extensive real-world objective evidence including longstanding technical needs, failure of others, industry praise, and widespread copying of

[REDACTED]

the '593 Patent's scan driver stage circuits. It is also my opinion that the objective evidence is sufficiently tied to the challenged claims.

1. Longstanding Technical Needs and Failure of Others

126. By the time of the inventions of the '593 Patent, there was a longstanding technical need for scan driver stage circuits for AMOLED displays for mobile devices with reduced sizes (i.e. footprints) such that the non-active “bezel” or “dead space” area around the active-area of the display could be narrowed. This need for more compact scan driver stage circuits continued to increase with the growing use of smartphones, which incorporated AMOLED displays that serve as *the* user interface capability for consumers. For example, researchers at the Department of Electrical Engineering at the Korea Advanced Institute of Science & Technology (“KAIST”) explained in a 2012 Society for Information Display article as follows:

Smartphones have drawn a great attention in recent year[s] as the most popular hand-held consumer electronic device and users of the smartphone are rapidly increasing . . . the number of the smartphone users are expected to continuously increase in all ages [A] bezel of a panel is also getting narrowed for design of compact displays. Furthermore, AMOLED displays require more peripheral drivers such as a scan driver . . . [t]herefore, ***small sized [scan] drivers are required to reduce the area and to implement compact and high density displays.***

Ex. 2050 at 1 (emphasis added).

127. By the time of the inventions of the '593 Patent, consumers and industry commentators were demanding smartphone devices with small bezels or “bezel free displays.” As reported by Android Authority in January 2013:

An idea that ha[d] long been passed around is to create a phone that has a true edge-to-edge display; a phone without a bezel. Almost the entire interaction with the phone occurs directly on the screen, so removing the bezel would utilize the entire surface area of the device. Creating a bezel-less phone would dramatically change the look and feel of a device, but *why hasn't it been done yet?*

Ex. 2049 at 2 (emphasis added).

128. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

129. It was understood by the time of the '593 Patent that designing AMOLED display scan driver stage circuits with small footprints would be difficult because the circuits proposed by that time were highly complex, requiring numerous

[REDACTED]

circuit components such as transistors, capacitors, and input signal lines. The '593 Patent describes the state of the prior art and the problems associated with complex scan driver stage circuits:

[C]onventional stage circuits include[d] a plurality of transistors, e.g., at least ten transistors, to supply the scan signals and/or require use of initializing signal in addition to the first and second clock signals. When a number of transistors in a stage increases, process yield deteriorates, so that stability of driving is deteriorated. When more initializing signals are required, there is less time for supplying scan signals, thereby reducing stability. When a number of transistors is increased and/or more initializing signals are required, complexity increases.

Ex. 1001 at 9:15-24.

130. Likewise, researchers at Hydis Technologies Co., Ltd. observed problems with conventional scan driver stage circuits and their complex structures which led to increased “dead space” around the displays:

[T]he conventional shift register needs a plurality of thin film transistors and signal lines to improve the off-characteristics. This causes a problem of enlarging a dead space of a display device, resulting in the display having bigger size than originally planned and modifying a structure of the gate driving circuit . . . Thus, as the number of transistors increases for changing the order of supplying the signal to the gate line, the conventional shift register exacerbates the foregoing problems.

Ex. 2051 at ¶¶[0013]-[0014].

131. The '593 Patent's inventions satisfied the long-felt need by creating scan driver stage circuits that allowed for a significant reduction in the space required for those circuits. [REDACTED]

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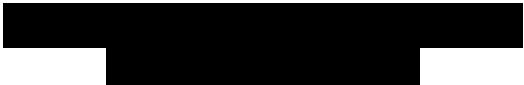
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Ex. 2048 at 14.

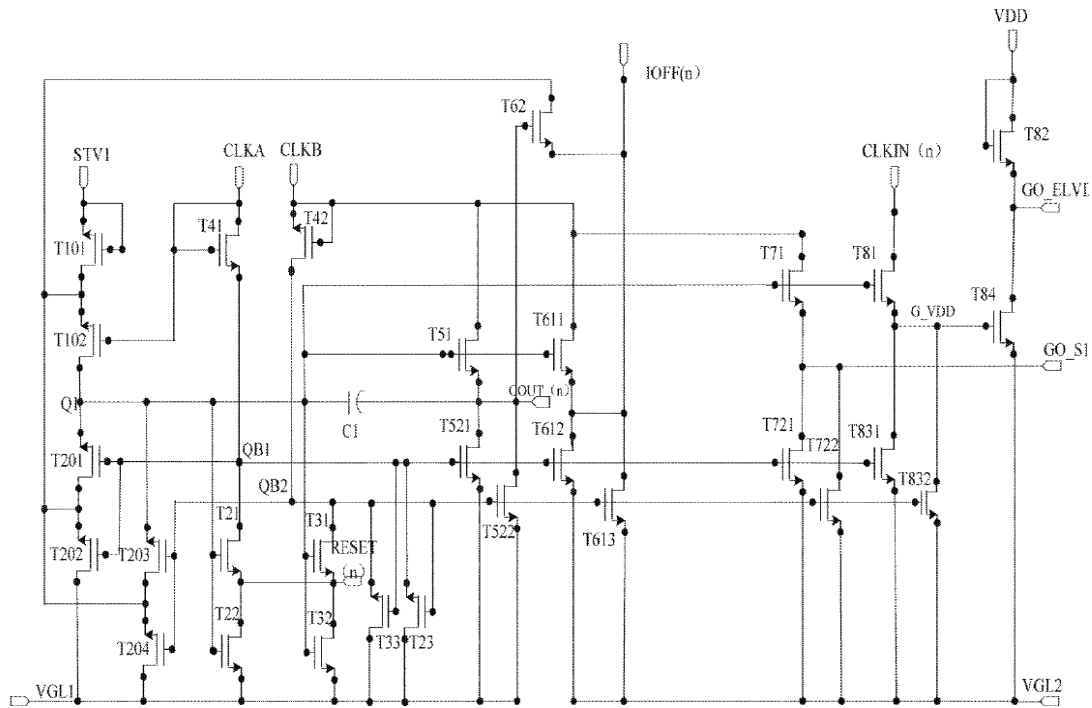
132. The specification of the '593 Patent explains that its inventions “provide stages having a reduced number of transistors and that output scan signals only using first and second clock signals,” which “improve stability and reduce complexity.” Ex. 1001, 9:12-26. The '593 Patent inventions achieve this by using only two clock signals and by having the output of one stage lead to the input of the



next (such that a separate initialization signal for each stage is not required). *See, e.g.,* Ex. 1001 at 4:61–8:17, Fig. 3. By reducing the number of input signals as compared to conventional designs, these circuits improve timing, reduce complexity, including the overall footprint of the circuit, and improve stability. Ex. 1001 at 9:12–26 (’593 Patent’s stage circuits as “improv[ing] stability and reduc[ing] complexity”).

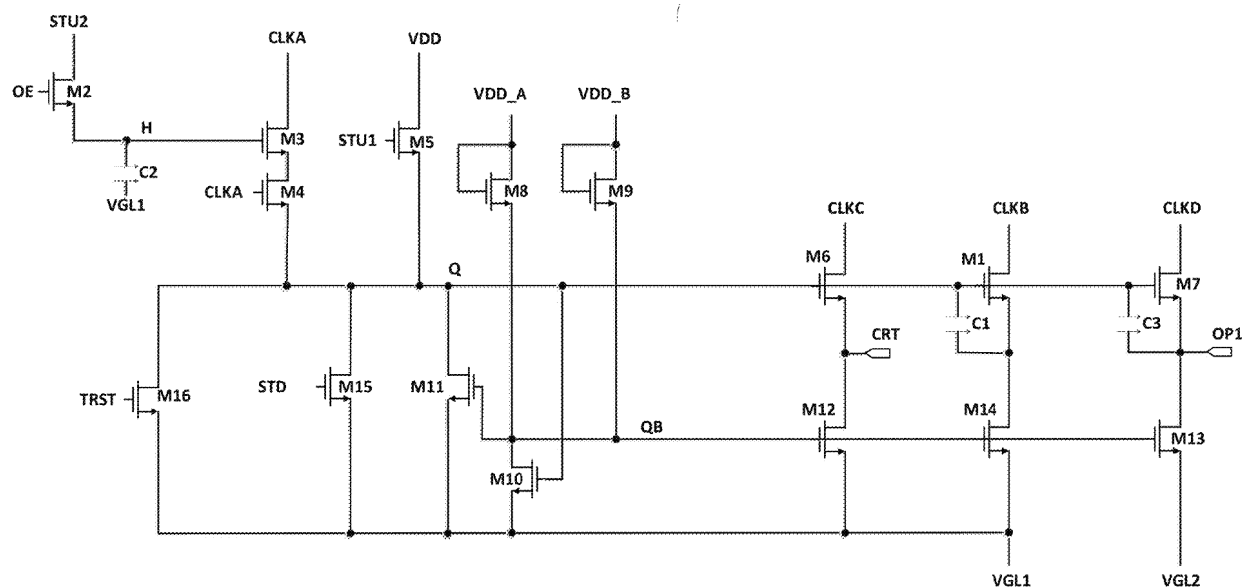
133. The inventions of the ’593 Patent are significant because of the history of failures by other researchers and display manufacturers to propose scan driver stage circuits in an attempt to meet the long-felt technical need for AMOLED displays with narrower bezels. This includes the prior art scan driver stage circuits discussed by Dr. Foty, such as Kimura (originally assigned to Semiconductor Energy Laboratory and published in March 2011), Tobita (originally assigned to Mitsubishi Electric Corporation and published in May 2008), Shin (originally assigned to Samsung SDI and published March 2007), Sasaki (originally assigned to Toshiba and published in June 2008), and Jeong (originally assigned to Samsung SDI and published in March 2008).

134. Companies continued to search for potential solutions even after the inventions of the ’593 Patent, but were ultimately unsuccessful. For example, Petitioner BOE proposed a scan driver stage circuit in 2017 with over 25 transistors and at least three clock signal lines.



Ex. 2052 (Petitioner BOE's U.S. Patent No. 9,620,061).

135. In January 2022, Petitioner BOE and Hefei BOE Joint Technology Co., Ltd. proposed a different scan driver stage circuit—this time with 4 clock signals and 16 transistors.



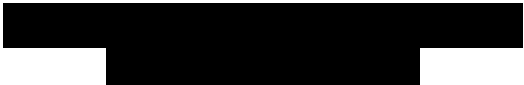
Ex. 2053 (Petitioner BOE's U.S. Patent No. 11,227,549).

136. I have not seen any indication that the many alternative scan driver stage circuits described above were successfully implemented in mass-produced AMOLED displays, despite the extensive amount of research and development work concerning alternative circuits. Instead, every product I have considered, including AMOLED displays used in mobile devices such as the Galaxy series products, uses the '593 Patent's innovative scan driver stage circuits.

137. Accordingly, it is my opinion that extensive real-world evidence establishes that—despite failures of others—long-felt needs were satisfied by the '593 Patent's inventions, which allowed for the successful reduction in dead space around displays through the compact scan driver stage circuits practicing the claimed inventions.

2. Industry Praise and Widespread Copying

138. Samsung Display successfully introduced AMOLED displays with significantly narrowed bezels, beginning with the AMOLED display for the Samsung Galaxy S4, which was the first AMOLED display to implement the scan driver stage circuits of the '593 Patent. Ex. 2044 (Declaration of Kwangsae Lee) at ¶ 7. Numerous publications at the time of the Galaxy S4's launch praised the display for its skinny bezels, which was enabled by the inventions of the '593 Patent.

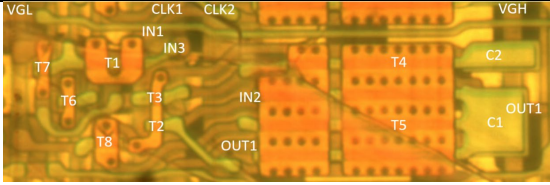
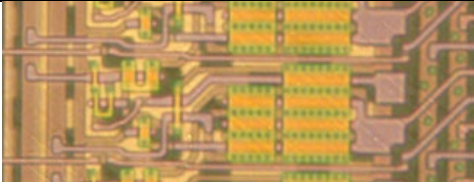
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- Ex. 2056 (Nguyen) noted that “[w]hen you’re looking at the Galaxy S4, the thing that strikes you instantly is the . . . super skinny side bezels.”
 - Ex. 2055 (Fletcher) said “[a]ttractively, the Galaxy S4 has a very narrow bezel, surrounding a five-inch display sporting a high-def and iPhone-besting 1920x1080 pixel resolution (441 ppi).”
 - Ex. 2054 (Kantara) praised the Galaxy S4 for its “gorgeous 5-inch display that has an incredibly small bezel” and specifically noted that its “ultra-thin bezel [was] 0.03 inches narrower than the Samsung Galaxy S III.”

139. I have also reviewed evidence indicating that numerous display manufacturers—including Petitioner Mianyang BOE—copied Samsung Display’s patented scan driver stage circuits and replicated Samsung Display’s AMOLED displays.

140. For example, Petitioner Mianyang BOE Mianyang BOE’s copying is particularly clear from the below side-by-side annotated comparison of teardown images of scan driver stage circuits in a Samsung Display AMOLED display (Galaxy S21) and a Mianyang BOE AMOLED display (iPhone 12). The teardown image of the scan driver stage circuit of Mianyang BOE’s AMOLED display (used in the iPhone 12) comes from complaint filed by Samsung Display against Mianyang BOE in the Eastern District of Texas. *See* Ex. 2045 (*Samsung Display Co., Ltd. v.*

[REDACTED]

BOE Tech. Co., Ltd. et al., Case No. 2-23-cv-00309, Compl. (E.D. Tex. Jun. 26, 2023)).

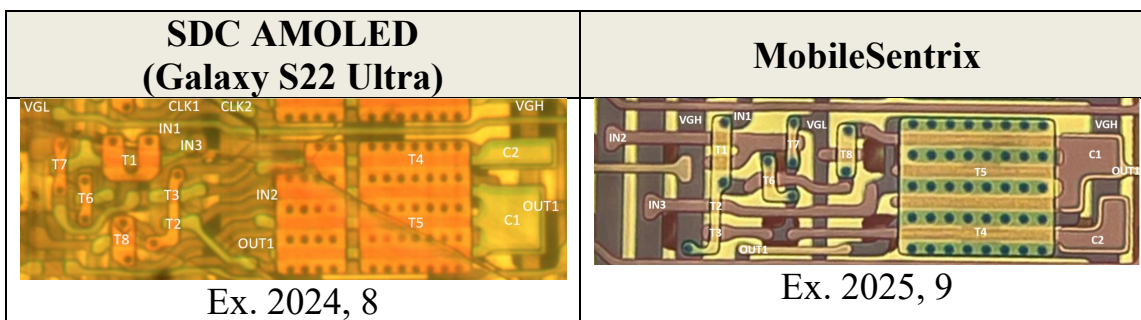
Samsung Display AMOLED (Galaxy S22 ULTRA)	Mianyang BOE AMOLED (iPhone 12)
 Ex. 2024 at 8	 Scan Driver Stage Circuit from BOE's AMOLED Display (Ex. 2045 at Fig. 28)

141. In fact, public patent documents show that Mianyang BOE had proposed alternative scan driver stage circuits over the years: (Ex. 2052 (U.S. Patent No. 9,620,061); Ex. 2053 (U.S. Patent No. 11,227,549)). Despite its attempt at independent circuit design, Mianyang BOE adopted—apparently through copying—Samsung Display’s patented scan driver stage circuits in order to mass-produce AMOLED displays for mobile devices.

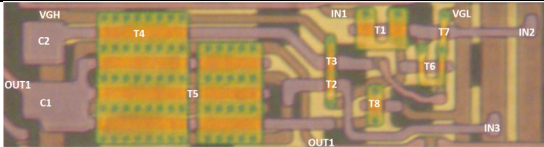
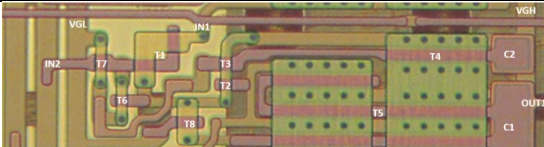
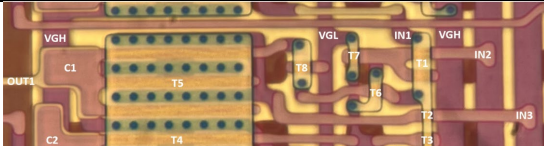
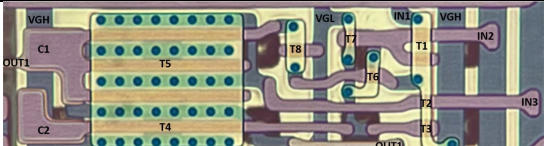
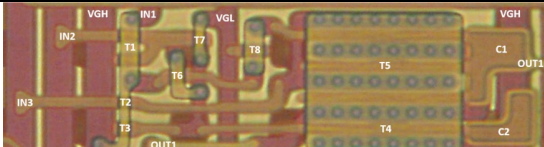
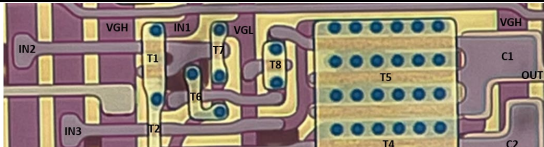
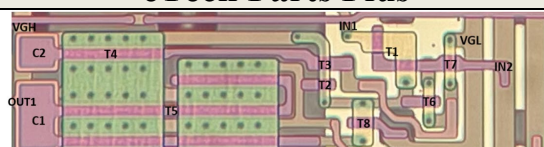
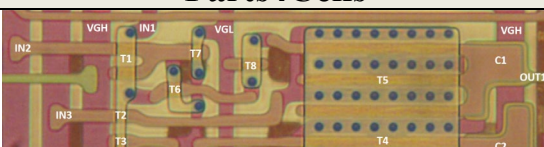
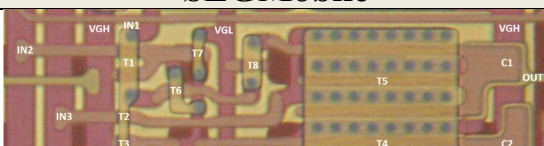
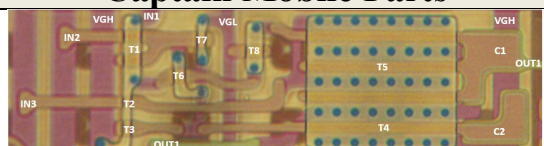
142. I also reviewed teardown photographs obtained from a number of AMOLED displays sold by replacement display vendors MobileSentry (Ex. 2025); Mobile Defenders, LLC (Ex. 2028); Injured Gadgets, LLC (Ex. 2029); Group Vertical, LLC (Ex. 2031); Fixez.com (Ex. 2038); Repairs Universe, LLC (Ex. 2036); SEGMobile.com (Ex. 2034); Sourcely Plus LLC (Ex. 2037); eTech Parts, LLC (Ex. 2032); Parts4Cells, Inc. (Ex. 2033); Wholesale Gadget Parts, Inc. (Ex. 2039); Captain Mobile Parts, Inc. (Ex. 2035); DFW Cellphone and Parts (Ex. 2041); Phone

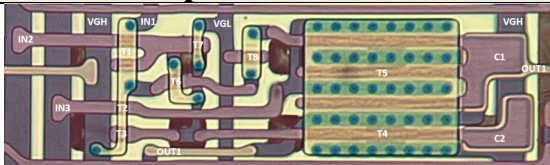
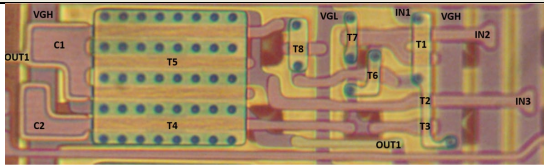
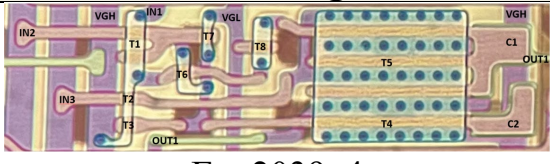
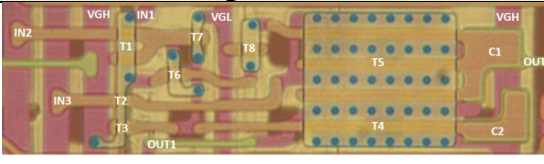
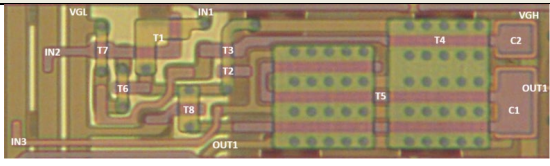
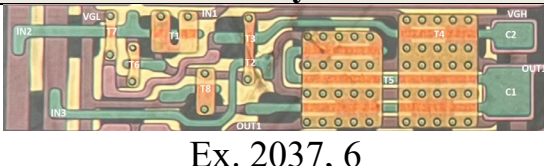
LCD Parts LLC (Ex. 2027); Parts4LCD (Ex. 2040); Mengtor Inc. (Ex. 2026); and Gadgetfix Corp (Ex. 2030). *See* Ex. 2042 (Declaration of Aris Silzars, Ph.D.).

143. As shown in the exemplary side-by-side comparison of teardown images of the scan driver stage circuits from the Galaxy S22 ULTRA AMOLED display (containing a Samsung Display AMOLED display) and the replacement display products, the replacement displays’ scan driver stage circuits are strikingly similar to that of Samsung Display, even down to the physical layouts. These scan driver stage circuit teardown photographs are so similar, including for example in the physical layout topology and geometry of the metal wirings, that the only reasonable inference one could draw is that someone with access to Samsung Display’s AMOLED display products or other confidential technical information determined to replicate Samsung Display’s scan driver stage circuits in the replacement display products.





Mengtor  Ex. 2026, 5	Phone LCD Parts  Ex. 2027, 5
Mobile Defenders  Ex. 2028 at 6	Injured Gadgets  Ex. 2029, 7
Gadgetfix  Ex. 2030, 5	Group Vertical  Ex. 2031, 5
eTech Parts Plus  Ex. 2032, 4	Parts4Cells  Ex. 2033, 4
SEGMobile  Ex. 2034, 4	Captain Mobile Parts  Ex. 2035, 4

Repairs Universe  Ex. 2036, 5	Fixez  Ex. 2038, 6
Wholesale Gadget Parts  Ex. 2039, 4	DFW Cellphone and Parts  Ex. 2041, 6
Parts4LCD  Ex. 2040, 5	SourcelyPlus  Ex. 2037, 6

144. Based on the teardown photos, I prepared an exemplary claim chart based on the Mengtor product to demonstrate how the replica AMOLED display products distributed by the replacement display vendors practice the challenged claims. Ex. 2046 (claim chart mapping challenged claims onto Mengtor AMOLED Display). The Mengtor product's scan driver stage circuit is representative of the scan driver stage circuits used in the other replacement display products. Below is an annotated version of a teardown photograph of the scan driver stage circuits (showing two stages) in the Mengtor product. The scan driver stage circuits used in the Mengtor product is strikingly similar to the one used in the SDC AMOLED display used in the Galaxy S22 ULTRA Product.

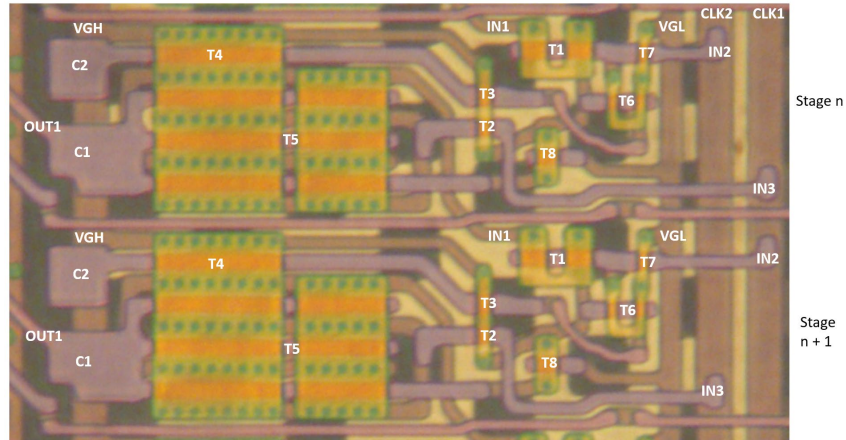
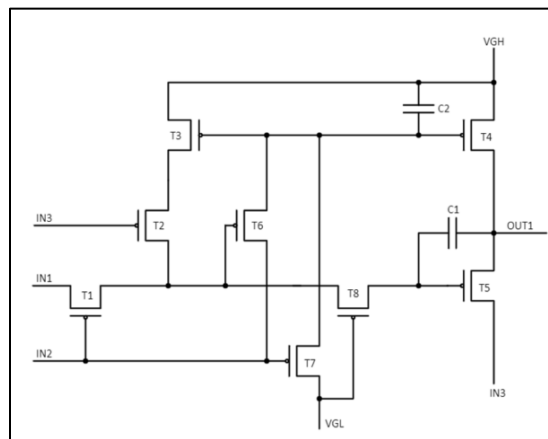


Exhibit 2026 at 6. Based on the striking similarities between the AMOLED display scan driver stage circuits used in the Galaxy S22 ULTRA Product (using a SDC AMOLED display) and the replica Mengtor display, the below circuit diagram was prepared for the Mengtor product.



3. Nexus

145. In my opinion, the evidence of objective indicia that I have reviewed is sufficiently connected to the claimed inventions of the '593 Patent.



146. The challenged claims of the '593 Patent recite scan driver stage circuits whose specific structures allow for a reduction in the space required for those circuits.

147. For example, the '593 Patent's reduces the "dead space" around a display through a scan driver stage circuit structure that decreases the number of required signal lines. The '593 Patent's circuits do not require an initialization signal for each stage by having the output of one stage lead to the input of the next. Ex. 1001 at 4:61–8:17, Fig. 3. For instance, the challenged claims recite "a first input terminal" (e.g., claims 1, 15) that "receives an output signal of a previous stage circuit" (claim 2) or "receives a scan signal of a previous stage circuit" (claim 17). Moreover, the '593 Patent's stage circuits only use two clock signals. Ex. 1001 at 4:61–8:17, Fig. 3. The challenged claims recite, for example, a "second input terminal" (e.g., claims 1, 15) which "receives a first clock signal" (claim 2). *See also*, e.g., claim 18 ("second input terminals of odd stage circuits receive a first clock signal . . . wherein second input terminals of even stage circuits receive the second clock signal"). The claims also recite, for example, a "third input terminal" (e.g., claims 1, 15) which "receives a second clock signal" (claim 2). *See also* claim 18 ("third input terminals of odd stage circuits receive a second clock signal . . . third input terminals of even stage circuits receive the first clock signal"). By reducing the number of input signals as compared to conventional designs, these circuits improve

[REDACTED]

timing, reduce complexity, including the overall footprint of the circuit, and improve stability. Ex. 1001 at 9:12-26 ('593 Patent's stage circuits as "improv[ing] stability and reduc[ing] complexity").

148. I prepared a claim chart mapping the challenged claims of the '593 Patent to an exemplary Samsung Display AMOLED display used in the Samsung Galaxy S22 ULTRA Product. *See* Ex. 2057 (Galaxy S22 ULTRA AMOLED Display Claim Chart). This claim chart is based on teardown photographs obtained from a Galaxy S22 ULTRA sample. *See* Ex. 2043 (Declaration of Adam Fontecchio); Ex. 2024 (Teardown photos of Samsung Galaxy S22 ULTRA Product). [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

149. As demonstrated in the claim chart, Samsung Display's AMOLED display in the Galaxy S22 ULTRA Product practices the claims of the '593 Patent and has the advantage of reducing the circuit's overall footprint by decreasing the number of required signal lines. [REDACTED]

[REDACTED]

[REDACTED]

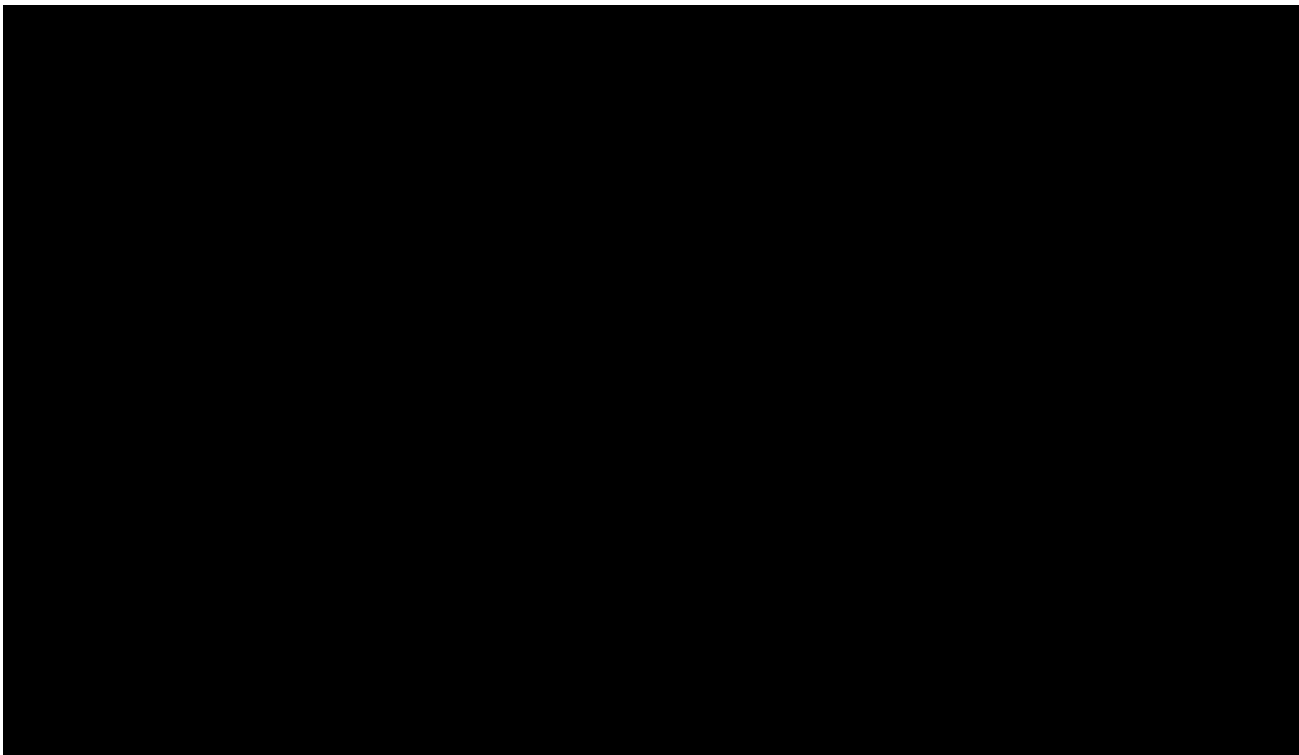
[REDACTED]

[REDACTED]

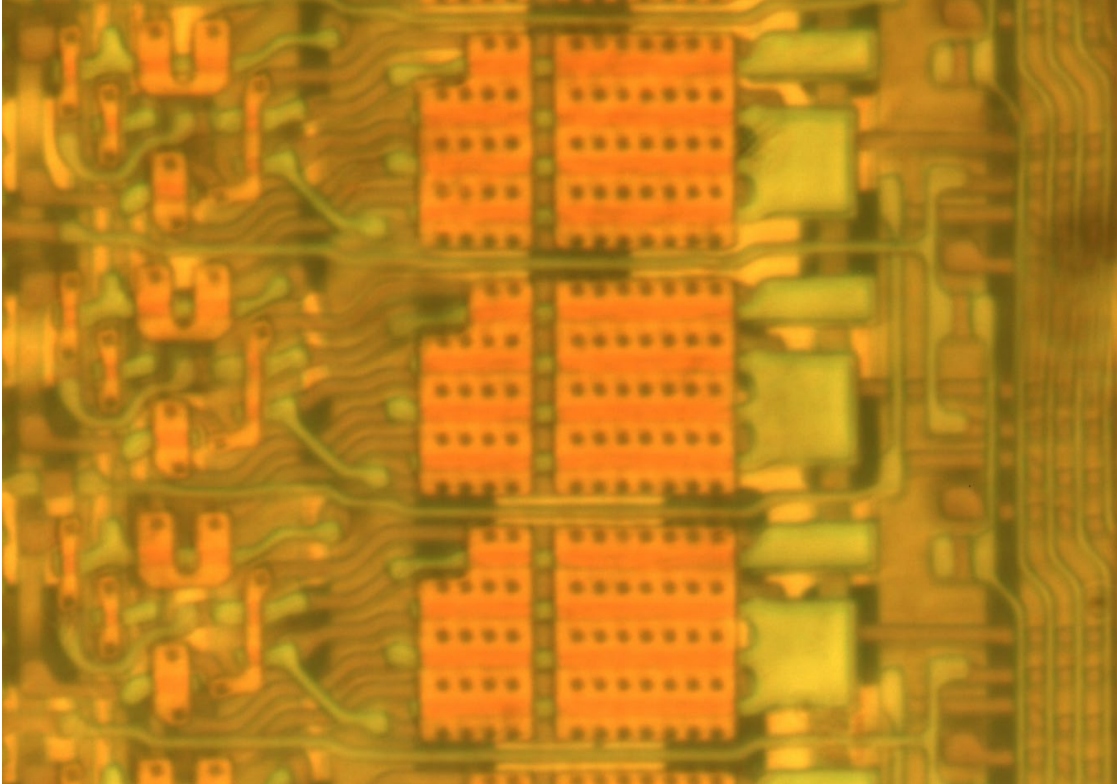
[REDACTED]

150. A teardown image of the scan driver stage circuit obtained from the Galaxy S22 ULTRA Sample is reproduced below, [REDACTED]

[REDACTED]



Teardown Image: SDC AMOLED Display in Galaxy S22 Ultra



Ex. 2024 at 8

151. As can be seen in the teardown photograph and circuit diagram from [REDACTED], the scan driver stage circuit in the SDC AMOLED display incorporated into the Galaxy S22 ULTRA Product includes “a first input terminal” (e.g., FLM) that “receives an output signal of a previous stage circuit” or “receives a scan signal of a previous stage circuit.” The stage circuits only use two clock signals (CLK1 and CLK2). *See also* Ex. 1001 at 4:61–8:17, Fig. 3. The display also includes a “second input terminal” which “receives a first clock signal” (CLK1) and a “third input terminal” which “receives a second clock signal” (CLK1). By reducing the number of input signals as compared to conventional

[REDACTED]

designs, these circuits improve timing, reduce complexity, including the overall footprint of the circuit, and improve stability.

XIV. AVAILABILITY FOR CROSS-EXAMINATION

152. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during a time as mutually agreed between the parties.

XV. RIGHT TO SUPPLEMENT

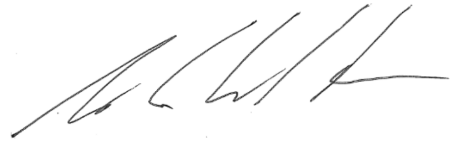
153. I reserve the right to supplement my opinions in the future to respond to any arguments that the Petitioners raise. This declaration represents only those opinions that I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated herein based on new information that becomes available to me and on my continuing analysis of the materials already provided.

* * *

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on: 12/12/2024

By:

A handwritten signature in black ink, appearing to read 'Andrew Wolfe', written over a horizontal line.

Date

Andrew Wolfe, Ph.D.