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4 N O T I C E

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18 assist attorneys in their case preparation and is
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21 other purpose and may not be filed with any court.

22

1 P R O C E E D I N G S

2 VIDEOGRAPHER: Here begins Media Number 1
3 in the videotaped deposition of Daniel Foty Ph.D.
4 in the matter of Mianyang BOE Optoelectronics
5 Tech Company et al V Samsung Display Company PTAB
6 in the United States patent and trademark office
7 before the patent trial and appeal board, case
8 numbers are IPR2023-00941, 0987, 0988, 1075 and
9 00620.

10 Today's date is December 5th, 2024. The
11 time on the video monitor is 9:04 a.m. The remote
12 videographer is Jesse Castro representing Planet
13 Depos. All parties of this video deposition are
14 attending remotely. Would.

15 Counsel please voice-identify themselves
16 and state whom they represent.

17 MR. ANDROS: Derek Andros, Covington and
18 Burling representing patent owner. With me is my
19 colleague Jared Frisch.

20 MR. HERMAN: This is Patrick Herman from
21 Orrick Herrington and Sutcliff here on behalf of
22 petitioners. And just to be clear, this



1 deposition is relating to a single IPR proceeding
2 that is IPR2024-00620.

3 VIDEOGRAPHER: The court reporter today is
4 Susan Klinger also representing Planet Depos, the
5 witness will now be sworn.

6 DANIEL FOTY, Ph.D.,
7 having been first duly sworn testified as follows:

8 EXAMINATION

9 BY MR. ANDROS:

10 Q Good morning, Dr. Foty?

11 A Good morning, counselor.

12 Q Would you please state your full name for
13 the record?

14 A Daniel Patrick Foty.

15 Q You have been deposed a number of times
16 before including in a number of proceeding between
17 BOE and SDC; is that right?

18 A Both of those are correct, I've been
19 deposed many times throughout the years and I've
20 been deposed several times in other aspects of
21 this general matter.

22 Q I will just, I will had it some highlights



1 of the basics today I will be asking you questions
2 during the deposition, if you don't understand one
3 of my questions, just please ask me to clarify and
4 I will do so. Is that okay?

5 A Understood.

6 Q If you do answer a question, I will
7 understand that you have understood my question is
8 that fair?

9 A Understood.

10 Q And we're holding the deposition remotely
11 today but you understand that this will be treated
12 as if it was in in-person proceeding, right?

13 A Yes, I understand that.

14 Q And where are you physically located this
15 morning?

16 A I am physically located at my residence in
17 Fletcher Vermont.

18 Q Do you have anyone else with you today?

19 A Just the cats.

20 Q Do you have any communication tools or
21 utilities open on your computer other than the
22 Zoom that we're using for the deposition today?



1 A No, I do not and if you want to give me a
2 moment I forgot I can go disconnect the VoIP box I
3 won't get a telephone interruption I forgot to do
4 that I will be right back.

5 Q Okay.

6 A Apologies I usually do that before a
7 deposition but i realized when you asked I could
8 be interrupted by a ringing phone, there is
9 nothing that can interrupt mean my mobile phone is
10 off the landline is disconnected and so forth.

11 Q Appreciate it. Do you have any folders
12 saved on your computer with documents for this
13 deposition?

14 A Not for this deposition, no. What I do
15 have is I have a clean copy of my declaration no
16 writing in it it is just for today to make this
17 easier. I have a binder to my right here which
18 has all again clean copies of all of the exhibits
19 that were cited and I have a blank pad of sticky
20 notes which are if we need to use them for
21 bookmarks if we're flipping around in my
22 declaration sometimes it can save trouble if I



1 slip a blank sticky note on the edge so I can find
2 a page we might come back to.

3 Q You are a couple of steps ahead of me.

4 So?

5 A I've done this plenty of times.

6 Q You are a pro.

7 Other than the clean documents hard copy
8 documents that up noted do you have anything else
9 with you today for the deposition?

10 A Just coffee water and do you have drops to
11 keep this there hopefully bogging down.

12 Q Great. So as I go through exhibits today,
13 we will try to bring them up on the screen we will
14 also drop them in the chat. But can you fee free
15 to use those clean hard copies that you mentioned
16 just whatever is easiest for you to navigate the
17 documents today is that okay?

18 A Yes, that is fine the only request I might
19 make again help the smooth if you since I know you
20 will be introducing exhibits and numbering them
21 consecutively for the deposition, if you could
22 also just tell me what the exhibit number if you



1 happen to know it in a declaration it might make
2 it a little quicker to find.

3 Q Sure, I think we will use the IPR exhibit
4 numbers, so those should be consistent, but if
5 there is any, any question, I will be happy to
6 clarify what those what those exhibit numbers are?

7 A I appreciate that, I have the, the binder
8 has inserts that allow me to, that have the
9 exhibit numbers so it should be easy to find.

10 Q Great. So during the deposition I would
11 ask that you not engage in communications with
12 anyone else other than this Zoom platform that
13 we're communicating across is that okay?

14 A That is okay, it would only be if there is
15 some sort of technical difficulty I did once have
16 a power outage in the middle of a deposition.

17 Q All right. If someone attempts to
18 communicate with you during the deposition, will
19 you please let me know for the record?

20 A I will do so, yes, it should be fine the
21 only other way I could be interrupted if someone
22 physically comes to the door which I don't expect,



1 I am actually I am expecting a package to be
2 delivered today but it will be probably be much
3 later on the odd chains it shows up early I will
4 just have to stop and go get it.

5 Q Understand auto. All right. Is there any
6 reason that you can't give full and accurate
7 testimony today?

8 A As long as this big guy isn't bothering
9 you.

10 Q Cats aside?

11 A He's very friendly. He likes you
12 counselor you may want to say hi a few times but
13 other than the cats trying to interrupt me here,
14 there shouldn't be any problems.

15 Q All right. And what did you do to prepare
16 for your deposition today?

17 A I reviewed the materials, the declaration
18 and exhibits and I had a few discussions and a
19 meeting yesterday with counsel.

20 Q So you say you had a few discussions who
21 were those discussions with?

22 A They were just a few email exchanges with



1 Mr. Herman and we met for about an hour and a half
2 yesterday.

3 Q Okay. Did you other than the about an
4 hour and a half meeting with Mr. Herman yesterday,
5 did you have any other meetings to prepare for
6 your deposition?

7 A No, I did not.

8 Q And did you speak to anyone other than
9 counsel in preparing for your deposition today?

10 A No, I did not.

11 Q And you mentioned that you reviewed your
12 declaration as well as the sited exhibits; is that
13 correct?

14 A That's correct.

15 Q So let's turn now to your declaration
16 which understand be Exhibit 1003, the declaration
17 of doctor Daniel Foty if we could get that up on
18 the screen and also dropped in the chat that would
19 be great?

20 A I have my paper copy open 1 thing I will
21 try to do if I turn to look at it, the microphone
22 may be this microphone will be better has trouble



1 picking me up I will try to turn back before I
2 verbalize, but if I don't do that, and is a
3 problem, you know, just somebody let me know if
4 that causes an audio problem.

5 REMOTE TECHNICIAN: Stand by, this is
6 marked Exhibit 10 '03.

7 MR. ANDROS: Yes.

8 REMOTE TECHNICIAN: Now dropping into the
9 chat. Now pulling it up on the screen.

10 (Exhibit 10 '03 discussed.)

11 Q Dr. Foty do you recognize in as a copy of
12 your declaration?

13 A This appears to be the cover page of my
14 declaration, yes, and I see it has appeared in the
15 chat as well but I won't download that copy I will
16 be referring to my paper copy which should be the
17 same.

18 Q Understood. So if we can turn to the last
19 page of the declaration which should be page 306
20 scroll down a little bit there is that your
21 signature on page 306, Dr. Foty?

22 A Yes, it is.



1 Q So your declaration was signed on March
2 6th, 2024; is that right.

3 A That is correct.

4 Q And is that when you finished working on
5 your declaration?

6 A Yes, that was the due date for the
7 declaration back in March or last I apologize
8 there was, it was, the day we file there is not a
9 deadline just the filing date we used.

10 Q And when did you start working on your
11 declaration?

12 A Probably started doing some background on
13 it I believe in December.

14 Q Okay. And how much time did you spend
15 working on your declaration?

16 A I didn't go check my invoices for the
17 hours those of course are discoverable if need be
18 but it was probably something like 100 hours,
19 something in that neighborhood.

20 Q So between December 2023 and March 2024
21 you said about 100 hours is that?

22 A That is a rough guess, it would be



1 something, I would have to go check my invoices it
2 might be a 120, it might be '80, it was not a
3 trivial amount, though.

4 Q And did you write your declaration?

5 A Yes, I did.

6 Q Did anyone else help write your
7 declaration?

8 A Well, as usual, you know, drafts went back
9 and forth with counsel for analysis and
10 discussion.

11 Q Let's -- let's turn to paragraph 133 of
12 your declaration this should be on page 68?

13 A I have that open in my paper copy.

14 Q Had is where your analysis of the Kimora
15 reference begins; is that right?

16 A Yes, that is correct, the unpatentability
17 was all sequestered in section 12 and 12A is the
18 ground 1 Kimora discussion.

19 Q So actually let's quickly pull up on the
20 screen and drop in the chat Exhibit 1004 which
21 should be Kimora Dr. Foty if you are looking for a
22 paper copy?



1 A I'm just verifying we have the exhibit
2 numbers right but.

3 Q That is appreciated?

4 A I don't want anyone to have to stay later
5 than they need to, so me included, so Kimora is
6 Exhibit 1004.

7 Q So Dr. Foty what is up on the screen
8 Exhibit 1004 is that the Kimora you referred to in
9 your declaration?

10 A That appears to be the case, and there is
11 only one Kimora reference in this matter.

12 Q And so if I refer to Exhibit 1004 today as
13 Kimora you will understand what I am referring to?

14 A That should be fine, again unlike some
15 other matters there is only one Kimora reference,
16 so we shouldn't have any confusion I hope.

17 Q Okay. So if we can turn back to Exhibit
18 1003 now. And let's, let's go to paragraph 160.

19 A I have that open in front of me now.

20 Q Are you with me, great.

21 So here you describe that transistor
22 making up the circuit of figure 27C operate to



1 supply logic low logic high signals to the output
2 line do you see that?

3 A Yes, that is a generic description of what
4 the circuit functionality is.

5 Q Could you explain for me what you mean by
6 logic low signal?

7 A I have chosen that gen Lee to mean if
8 there a binary logic being used you have a high
9 voltage and a low voltage to discriminate between
10 the 2 binary states so that is basically standard
11 terminology for using the different voltages to
12 reference by the 2 different binary states.

13 Q Okay. So as to those 2 binary states a
14 low level would be a logic low and a high level
15 would be a logic high do I generally have that
16 right?

17 A That is generally right of course
18 circuitry could output other voltages sometimes
19 beyond those but that gives you the idea of how
20 these circuits function. They're digital logic
21 circuits essentially.

22 Q And so then if we scroll down a little bit



1 in paragraph 160 you have got a timing diagram

2 Figure 21B get that up on the screen?

3 A I do have that on my paper copy if there a
4 technical issue.

5 Q Okay. All right. And so in this diagram
6 we have got signals different signals listed on
7 the left; is that right?

8 A I would not call them all signals it
9 depends how you define signal because the inputs
10 at the top are obviously signals, the voltages
11 below that are labeled V refer to voltage levels
12 inside the circuitry, voltages and nodes.

13 Q Okay. So we've got input signals, IN1,
14 IN2, IN4, and then we have got the voltages of
15 nodes within the circuitry V11, V12, and V13; is
16 that right?

17 A Yes, that is my understanding of how
18 Kimora works and the circuitry on the next page
19 shows nodes 11, 12 and 13 as label would a Kimora.

20 Q And so if we look for example, at V12 we
21 see here sort of a square waveform where there is
22 a low and then it goes up to high back down to low



1 and sort of rev Pets. Do you, do you see that?

2 A Yes, that is what the behavior in this
3 timing diagram of the voltage at node 12.

4 Q Okay. And so if we look for example in
5 that first time period which is labeled time
6 period B, we see V12 low, so that would be a logic
7 low is that correct it?

8 A It is an internal voltage. The logic
9 levels only matter at the output. So I don't know
10 if I would characterize that necessarily as being,
11 it doesn't have to be the exact logic low value,
12 but it is certainly the node can take on a high
13 value and a low value, which reflects some sort of
14 a logic value.

15 Q Okay. So for the, for the voluntary
16 voltage of the node here we would say it a low
17 level but it may not be as you put it the exact
18 logic low for the, for the output of the circuit
19 is that is that accurate?

20 A That may be the case, because as I said
21 the logic level exact logic levels really only
22 matter for the output.



1 Q So then if we look at G out if we look at
2 the time period labeled D, there would be a high a
3 logic high output in period D do I have that
4 correct?

5 A That appears to be the case, yes.

6 Q Okay. So if we look then at paragraph
7 160, you're discussing figure 27C in that
8 paragraph, right?

9 A That is correct, that is the circuit they
10 was analyzing here.

11 Q Right. And that is the circuit that you
12 primarily rely on for your analysis of the
13 independent claims is that correct?

14 A That is the, that is I believe that will
15 it is correct, yes, I would have to review to be
16 sure, but that was certainly the primary
17 embodiment they focused on in my declaration.

18 Q And you agree that Kimora doesn't provide
19 a timing chart that is specific to the circuitry
20 of figure 27C, right?

21 A He doesn't provide 1 specifically, but 27C
22 is a derivative of circuitry he has associated

1 with the Figure 21B timing diagram, so it seemed
2 appropriate to use it.

3 Q Okay. So in your opinion, the circuitry
4 of 27C would be supplied with the same timing that
5 is shown in Figure 21B; is that right?

6 MR. HERMAN: Objection, form.

7 A It could be used that way to do the
8 functionalities in the same way since it is
9 basically the same circuit with just a
10 modifications made to it.

11 Q And in fact you say in paragraph 160, it
12 is readily comprehensible and would so be
13 understood by a POSITA that this circuitry of
14 Figure 27C would be supplied with input signals in
15 the same manner and with the same timing with
16 reference to Figure 21B; is that right?

17 A I have to go read that it was on the
18 previous payment, so I was looking and didn't see
19 what you just said please give me a moment to read
20 that.

21 Q Certainly.

22 A Yes, that is what I did say there in the



1 previous page of paragraph 160.

2 Q So let's go down a couple of paragraphs to
3 paragraph 166. Am you let me know when you are
4 there?

5 A I'm sorry, I am there and I was just
6 looking at that preemptively sorry.

7 Q Certainly. So here is where you begin
8 providing your analysis of claim limitation 1B,
9 right?

10 A Yes, that is the analysis of that claim
11 element.

12 Q And recognizing that we're shorthand being
13 the language here a little bit, can we refer to
14 that limitation 1B as the first driver limitation?

15 A I think that will work, that should be
16 fine.

17 Q Thank you. So if we go now to paragraph
18 171 in paragraph 171 you identify the elements
19 that comprise the first driver, right?

20 A That is correct, they're highlighted in
21 the blue boxing here.

22 Q And within that blue boxing, you have



1 identified a number of transistors?

2 A Yes, I believe 4 transistors are included
3 in that so labeled first driver.

4 Q And so those are 205, transistor 205,
5 transistor 2 '06, transistor 207, and transistor
6 204 did I get all of them?

7 A I believe you did, I believe those are the
8 four they mentioned a moment ago.

9 Q And then in the, in the top left of the
10 annotated figure have you identified the third
11 input terminal in purple and you have identified
12 wiring 112; is that correct?

13 A I've identified the third input terminal
14 which goes to what Kimora has labeled as wiring
15 112.

16 Q And if we look at wiring 112, it is
17 connected to the gate of transistor 204, right?

18 A That appears to be the case, yes.

19 Q And of the 4 transistors that we were
20 discussing that you have identified on the first
21 driver, transistor 204 is the only one of those
22 four that has its gate connected to wiring 112,



1 right?

2 A That appears to be the case, yes.

3 Q I want to keep discussing this transistor
4 204 a little bit if we can move now to paragraph
5 175. There you say the structure also includes
6 yet another transistor transistor 204, do you see
7 that?

8 A Yes, I do.

9 Q Okay. And then in paragraph 175 you have
10 got an annotated version of figure 27C and then
11 just below that the first new full sentence starts
12 this transistor 204 allows the potential of the
13 node 13 to be lowered to prevent dielectric
14 breakdown or deterioration of transistors
15 connected to the node do you see that?

16 A Yes, I see that and I'm quoting Kimora to
17 that effect hence the quotation marks.

18 Q And your citation there is id, right?

19 A The citation after the figure refers to
20 the figure and there is some reference above the
21 figure to particular paragraphs in Kimora.

22 Q Right, so you were, you were referencing



1 back to paragraphs 285 and 286 of Kimora; is that
2 right?

3 A That appears to be the case, yes.

4 Q Okay. Let's, let's look at those quickly.
5 So if we can pulp up Exhibit 1004 which is Kimora
6 go to paragraph 285?

7 A And I extracted the page from the binder
8 with those paragraphs I think hang on a moment.

9 Q You are living dangerously I wouldn't be
10 able to keep individual looseleaf safe and
11 organized?

12 A We will take the chance this binder is too
13 big if I drop it on the desk it may break the
14 camera and we would be done. So let's see sorry I
15 had the wrong page now I have the pages for that
16 have 285 and 286 on the paper copy if that makes
17 my life easier.

18 Q Okay. Now, the language that you were
19 referencing about lowering the potential of the
20 node to prevent break down or deterioration, that
21 comes out of paragraph 286, right?

22 A That appears to be the case, yes.



1 Q Okay. And if we read that in its entirety
2 it says thus I'm reading about halfway through
3 paragraph 286, thus an in a period D, the
4 potential of the node 13 can be lowered therefore,
5 dielectric breakdown or deterioration of
6 transistors connected to the node 13 the e.g. the
7 transistors 102 the transistor 24203, the
8 transistor 205 or the transistor 206 can be
9 prevented. Did I, did I get that right?

10 A I believe you did, if there is any
11 problems with that obviously you are regarding
12 could be compared against the document but I read
13 along with you I believe you were correct.

14 Q Right. So Kimora is discussing the
15 specific period D when the potential of the node
16 13 can be lowered; right?

17 A That is what he specifically says, yes.

18 Q And that is what you cite for the
19 proposition that that transistor 204 can operate
20 to lower the potential of node 13, right?

21 A Yes, that is correct.

22 Q So let's turn back now to the timing



1 diagram we were looking at in Figure 21B of
2 Kimora.

3 It will be at the top of the document with
4 the figures?

5 A Unfortunately some of these figure numbers
6 as we just found out don't appear in the search.

7 Q Yeah, they don't OCR correctly?

8 A Sometimes they do, sometimes they don't.

9 Q Okay. So looking at Figure 21B, one of
10 the voltages that is listed here one of the
11 voltage of the nodes that we were just discussing
12 a moment ago is V13 do you see that?

13 A I see that, yes.

14 Q And so that would be the voltage or the
15 potential of node 13, right?

16 MR. HERMAN: Objection, form.

17 A That is my understanding, yes.

18 Q And so if we look down at the bottom of
19 Figure 21B, there is only one time period labeled
20 as time period D, right?

21 A That is correct.

22 Q And in time period D here, V13 is not



1 shown to be at a low potential, right?

2 MR. HERMAN: Objection, form.

3 A Node V13 is shown in the as this output
4 this node here refers to figure the Figure 21A
5 circuit up above, and in this case, because it
6 doesn't have that transistor, the output
7 bootstraps back to that node and raises the
8 voltage which is why Kimora made the modifications
9 to figure 27 to prevent that from happening.

10 Q Okay. Well, we will get there, but my
11 question is just in 21B, you will agree with me
12 that during time period D the voltage of node 13
13 is shown to be high, right?

14 A It is shown to be in this case high and
15 higher.

16 Q In fact, in period D it is shown to be the
17 highest at any point in operation in the circuit,
18 right?

19 A In the operation of the Figure 21
20 transistor, yes.

21 Q And 21B is the timing diagram that, that
22 you rely on in your declaration, correct?



1 A As I said in my declaration, I rely on it
2 for the inputs because 27C is a modification of
3 the 21A circuit and so I relied on the inputs.

4 Q And this, this figure does not reflect the
5 lowered potential that you cited in, in your
6 analysis of limitation 1A, right?

7 A Yes, my analysis of limitation is it 1A or
8 1B I thought we were talking about 1B actually.

9 Q I believe we were talking about 1B the
10 first driver?

11 A The first driver is 1B, okay sorry could
12 you repeat the question then I got lost there on
13 that confusion.

14 Q Sure. So if your analysis of limitation
15 1B, you reference a lowered potential of node 13,
16 right?

17 A Yes, with respect to the circuitry of
18 figure 27C.

19 Q And this Figure 21B does not show a
20 lowered potential of node 13 during time period D,
21 correct?

22 MR. HERMAN: Objection, form.

1 A I will agree that to the extent that it
2 shows that for the behavior the voltages below are
3 the behavior of the circuit above and that
4 behavior would not be there in figure 27C
5 circuitry it just not show an explicit diagram
6 showing the internal voltages like this for 27C.

7 Q So you would have to change this timing
8 diagram in order to show what the timings of the
9 figure 27C circuit would look like, right?

10 MR. HERMAN: Objection to form.

11 A Not the inputs as I said in my
12 declaration, I used this because it is essentially
13 the same circuit to be run in the same way I use
14 the inputs. The voltages are results and so we
15 actually modifies 27C to prevent what we're
16 looking at from happening, he doesn't show a
17 diagram but he verbally states so.

18 Q If we look at paragraph 160 of your
19 declaration again?

20 A Sorry I'm looking at that now I see it is
21 scrolling up too but I'm look at that.

22 Q You don't explain any of what you just

1 explained to me when you with are describing your
2 reliance on Figure 21B, right?

3 MR. HERMAN: Objection to form.

4 A Well, I say at the right at the bottom of
5 the page there I say that it is readily
6 comprehensible that the circuitry would be
7 supplied with input signals in the same manner and
8 with the same time that go is what I was referring
9 to.

10 Q So you're only taking effectively the top
11 half of Figure 21B and applying that to the figure
12 27C circuit; is that right?

13 A Yes, because those are inputs. The other
14 ones are internal results shall we say the
15 voltages, the internal nodes respond to the inputs
16 for the particular circuit and Kimora modifies
17 this circuit to address the problem we were just
18 discussing but the circuit would use the same
19 inputs and be run in the same way.

20 Q And how do you know that?

21 A Well, because Kimora discusses as we just
22 were looking at modifying the 21A circuit to

1 address the problem we just discussed by making
2 the modification that leads to 27C so otherwise I
3 would assume the circuit would be operated in the
4 same way.

5 Q So you assumed that the circuit would be
6 operated in the same way after this modification?

7 MR. HERMAN: Objection, form.

8 A Well, again, Kimora says he's modifying
9 the circuit to address the problem we just
10 discussed of possible dielectric breakdown and
11 deterioration of the transistor and other than
12 that, he is trying to use the same inputs to
13 produce the same outputs so it seems like it a
14 reasonable assumption to make.

15 Q Kimora never provides a full-timing
16 diagram for the figure 27C circuit that would
17 reflect this lower potential, correct?

18 A He doesn't provide an explicit diagram
19 showing the internal node voltages he just dresses
20 that verbally for that one particular node.

21 Q By verbally you mean within the paragraph
22 286 we were looking at?



1 A Sorry that is essentially that is what I
2 meant that he describes the quota we had earlier
3 about addressing the over voltage that appears in
4 that node in the 21A embodiment and he therefore
5 is making that modification to prevent the
6 bootstrapping of node 13 and prevent that voltage
7 from going as high as that which is what will
8 cause well-known in the art that excessive voltage
9 could cause dielectric breakdown it could cause
10 transistor deterioration.

11 Q Where does Kimora say that it doesn't
12 change the inputs there the Figure 21A circuit to
13 the 27C circuit?

14 MR. HERMAN: Objection, form.

15 A Go ahead Patrick sorry I stepped you on.

16 MR. HERMAN: Objection, form.

17 A Sorry about that.

18 I don't believe he may say that explicitly
19 but it is basically the same circuit and me makes
20 a modification to the circuit is intended to
21 function in the same way other than that problem
22 internally that he addresses so he figures that he

1 addresses that problem and would use the circuit
2 in the same way that seems like a reasonable
3 assumption?

4 Q So you said it is intended to operate in
5 the same way other than the way that it modified
6 did I hear that correctly?

7 A The modification addresses that over
8 voltage otherwise you are trying to do the same
9 inputs to produce the same outputs from the same
10 sort of circuit.

11 Q But again, that is an assumption, right,
12 Kimora you just told me Kimora doesn't tell you
13 that it is using the same inputs?

14 MR. HERMAN: Objection, form.

15 A I would have to review Kimora to see
16 exactly what he says there, but he certainly
17 doesn't provide a full diagram like 21B but again,
18 since it is he is taking 21B and addressing this
19 over voltage problem at 1 node, otherwise had t
20 seems reasonable to assume since he does not
21 provide a timing diagram in fact that tends to
22 indicate that the circuit is being used would be

↑

1 used in the same way in his teachings with the
2 same inputs.

3 Q Could you, could you point me to a passage
4 or passages in Kimora that support that assumption
5 that you are making?

6 A Well, probably the best support for off
7 the cuff here is the beginning of 285 where he
8 just refers to all these structures including 21A,
9 and et cetera et cetera and then he says that in
10 the next paragraph 286, he says 11C, is addressing
11 a problem. This, this bootstrapping the output
12 bootstraps the floating node to a higher voltage.

13 Q Did you say 11C I'm trying to follow
14 along?

15 A I don't know if I said 11C, I, if I did I
16 don't know where that came from let me try again.

17 He addresses at the beginning of paragraph
18 285 a variety of embodiments we he had a list
19 there that includes 21A, and he does go into 286
20 he refers to the change he makes to 27C with that
21 to the, he makes a slight change to prevent the
22 output from bootstrapping the floating node 13 by



1 actually connecting the node to something that
2 prevents the bootstrapping. So he lists a large
3 number there including 21A and so this would
4 indicate that it is a general timing diagram that
5 applies for the inputs to more than just the 21A
6 embodiment and since he's talking about the same
7 type of circuits throughout these stage circuits
8 that seems like a reasonable assumption to make.

9 Q And you say that he's talking about the
10 same types of stage circuits but there is a number
11 of different figures listed here in the top of 2
12 paragraph 285 that you just referenced, right?

13 A Yes, those are all, there is a number of
14 embodiments but the embodiments here as far as I
15 can tell are all involving stage circuits at least
16 the ones I look at which are intended to
17 basically. Same sort of thing.

18 Q But Kimora discusses various conditional
19 modifications to different embodiments, right,
20 each just from what we're look at here in 285 the
21 first terminal of the transistor 204 can issue
22 connected to the a wiring which is different from



1 the wiring 115 so these embedments are varied and
2 describe different modifications, so how do you
3 know that what he's talking about in 285 refers
4 specifically to the 27C circuit you rely on?

5 MR. HERMAN: Objection, form.

6 A Well, first of all, he loses all of those
7 things and then he proceed unless paragraph 286 to
8 discuss 27C explicitly. And so these are all
9 appear to be birds of the same feather.

10 Q So you assume that because they're all
11 stage circuits, that they must refer to the same
12 input timings any way?

13 MR. HERMAN: Objection, form.

14 A Well, there is a general response to that,
15 that since it is a stage circuit you are going to
16 be wanting to run them in the same way and again,
17 27C is a modification of 21A and so otherwise he's
18 modifying it to just address 1 issue in 21A and so
19 otherwise there is no, no reason to assume that he
20 would be using it differently as a stage circuit.

21 Q But the addition of transistor 204 isn't,
22 isn't the only modification as between 21A and



1 27C, right?

2 A I would agree to it is not the only
3 modification but the architecture is clearly the
4 same.

5 Q When you say the architecture is clearly
6 the same, can you explain what you mean?

7 A They're both stage circuits which are
8 designed to have multiple inputs controlling
9 drivers that are to produce the output as a first
10 scan signal which is basically what all of
11 Kimora's embodiments are about.

12 Q So again, because it say stage circuit,
13 these are all interchangeable embodiments?

14 MR. HERMAN: Objection, form.

15 A Well, there is some differences the basic
16 input output functionality should be the same
17 across all of them.

18 Q By that you mean the output will either
19 output a logic high or a low logic?

20 A That is the function that a stage circuit
21 provides.

22 Q But if we look as between Figure 21A the



1 circuit in 21A and the figure or the circuit in
2 27C, there are various different inputs that in
3 the figure 27C circuit that are not shown in 21A,
4 right?

5 A There are some other additions from 21A to
6 27C. As far as I can tell, everything that is in
7 21A is in 27C and there are various additions
8 including the discussion we just had of the
9 architecture that prevents the bootstrapping to a
10 very high voltage of node 13.

11 Q And that also includes an additional input
12 signal 213, right?

13 A That appears to be the case, yes.

14 Q And a number of additional transistors,
15 right?

16 A Yes, there are some additions, but as far
17 as I can tell there are no subtractions.

18 Q So again, I can't remember I apologize if
19 I, if you already answered this, but did you point
20 me to a place where Kimora says that figure 27C is
21 a modification of Figure 21A?

22 A I thought I did, I don't know if I can



1 find it again, I quoted something.

2 Q I think you were in paragraph 285 but I'm
3 not sure that says that 27C is a modification of
4 21A?

5 A Please give me a moment my binder got a
6 little screwed up.

7 Q Please take your time?

8 A I have my paper copy of 285 now. Well,
9 again what I cited before I believe when you did
10 ask me this question, and I don't have the
11 transcript so I can't go back and reread it so
12 hopefully when I say again won't conflict with
13 that in 285 he describes a whole bunch of
14 embodiments heap has a long list and describes
15 some things about them then he specifically says
16 for 27C that he makes the modification to deal
17 well that bootstrapping of the voltage on node 13
18 which would which could be the problem he lists
19 and so that is the main modification he adds to
20 27C that the prior discussions of various
21 circuits.

22 Q But in paragraph 286 where he discuss



1 modification in figure 27C, it doesn't reference
2 21A at all, right?

3 A Not explicitly, no.

4 MR. HERMAN: Objection, form, on sorry
5 Patrick my answer after the objection is still not
6 explicitly, no.

7 Q It seems to reference actually figure 27A,
8 right with respect to the change, right?

9 A That is the lineage he gives but this
10 clearly also points back to 21A in terms of the
11 architecture and again since he doesn't have
12 everything I said earlier about using that timing
13 diagram is still valid because there is a
14 progression through all of these embodiments the
15 same sort of circuitry that would be run in the
16 same way be that 21A, 27A or 27C.

17 Q Okay, but my question was that when in 286
18 Kimora is discussing the modification that is
19 being, you know, discussed for, for the figure 27C
20 circuit, that modification is not provided with
21 reference to figure the circuit in Figure 21A,
22 right?



1 MR. HERMAN: Objection, form.

2 A He, again, he does not explicitly say
3 that, but his flow goes through from 1 from all
4 those circuits in his, in his list above.

5 Q And in fact the only circuit that Kimora
6 references with respect to that modification is a
7 change with respect to figure 27A, right?

8 MR. HERMAN: Objection, form.

9 A That is what he explicitly says in 286 and
10 again 285 at the beginning shows his general group
11 of embodiments which includes 21A, and 27A of
12 course.

13 Q Okay. But there is no explicit discussion
14 anywhere in Kimora that 27C is a modification of
15 21A, right?

16 MR. HERMAN: Objection, form.

17 A The modification he makes in 27C could be
18 made to either 21A or 27A, it is the same sort of
19 modification and again that is why the timing
20 diagram that is associated with 21A is more
21 general than just for the 21A in terms of the
22 inputs.



1 Q Okay, but you told me a moment ago that he
2 doesn't expressly say anywhere that the 27C
3 modification is a is a modification to the 21A
4 circuit, right?

5 MR. HERMAN: Objection, form.

6 A He doesn't say so explicitly, but again,
7 as I'm read this can such as a POSA would be able
8 to look at 21A and 27A and see that the same
9 situation is being addressed in both of them in
10 terms of why the changes for 27C are being made to
11 deal with the problem that Kimora discusses with
12 regard to why he's made the 27C modification.

13 Q But again, that is not Kimora never says
14 that?

15 MR. HERMAN: Objection, form.

16 A He does not explicitly say it but it seems
17 fairly obvious that since it is the same situation
18 he's addressing in 27A as he did in 21A, that the
19 timing, it is an issue of what he doesn't provide
20 an input diagram for 27C and the modification he
21 makes to 27A is could also be made to 21A which is
22 the same sort of circuit and so all of these

↑

1 embodiments are 1 can easily assume that they're
2 being runoff the same, would be are run often the
3 same input timing diagram that is all I'm trying
4 to say.

5 Q I think we've been going for about an hour
6 it little early I could actually use a break could
7 we take a quick break?

8 A Sure.

9 Q 10 minutes what do folks need?

10 A 10 is fine for me if we want to discuss
11 that on the record or off the record.

12 VIDEOGRAPHER: We are going off the record
13 the time is 9:55 a.m.

14 (Recess, 9:55 to 10:06 a.m.)

15 VIDEOGRAPHER: We are going back on the
16 record the time is 10:06 a.m.

17 Q Let's go now to paragraph 362 of your
18 declaration?

19 A I have found that in my paper copy.

20 Q Great. You are ahead of me?

21 A At least these numbers are searchable that
22 should make it easier.

↑

1 Q So looking here at paragraph 362 this is
2 where you start providing your opinions with
3 respect to the Shin and Sasaki references, right?

4 A Yes, that is where ground 2 discussion
5 begins.

6 Q So if we can quickly bring up I think it
7 is Exhibit 1005 or 1005 I apologize?

8 (Exhibit 1005 discussed.)

9 Q If we could also get it in chat that would
10 be great for those following along.

11 Is this Exhibit 1005 is this the Shin
12 reference that you referred to in your
13 declaration?

14 A That is the Shin reference and it appears
15 to match the paper copy I have in the binder on
16 the chair to my right.

17 Q Great. And so you will understand if I
18 refer to Exhibit 1005 as Shin you will understand
19 what I'm talking about?

20 A Yes, I believe I will.

21 Q Now, let's pull up drop in the chat
22 Exhibit 1014 which should be Sasaki mark marks



1 1014 discussed.)

2 Q Dr. Sasaki is this the Sasaki reference
3 you referred to in your declaration?

4 A It appears to be so once again this
5 verifies with the paper copy that I have on the
6 winding on the chair on my right.

7 Q So I can also refer to Exhibit 1014 today
8 as Sasaki?

9 A That should be fine and hopefully we won't
10 neither of us will get the 2 confused.

11 Q All right. So if we now turn back to your
12 declaration and go to paragraph 371 are you with
13 me?

14 A I have in the binder to my left which is
15 my declaration I have paragraph 371 in front of me
16 and it is also on the screen here.

17 Q Okay. And there you say that Sasaki's
18 disclosed circuitry includes transistors with
19 gates connected to a control electrode. Do you
20 see that?

21 A Yes, I see that.

22 Q And then you continue in the conventional



1 way this allow the circuit to apply either a
2 logical high or logical low signal to an output
3 terminal. So that is generally consistent with
4 what we were just talking about before with
5 respect to Kimora, right, providing a logic low or
6 a logic high signal to the output?

7 A Yes, that is again the function of the
8 shift register that gives the Es in a in a scan
9 driver.

10 Q So if we look at Figure 4 of Sasaki, which
11 if it easier have you it reproduced at the top of
12 page 155 of your declaration or you can go to the
13 source?

14 A You said Figure 4 I believe.

15 Q Yes.

16 A I have it in here I also just wanted to
17 pull it up in Sasaki as well in case I need it.

18 Q Sure?

19 A I have the Figure 4 in my binder of course
20 is not a notated in my declaration there is the
21 annotation added to it in red.

22 Q Right. Okay. So looking at Figure 4 it



1 is transistors T2 and T1 that are the transistors
2 you were referring to with gates connected to a
3 control electrode, right?

4 A Well, reading paragraph 371 I believe the
5 first part is basically is more general you have
6 transistors with gates provided control electrode
7 that is basically how a field effect transistor
8 works. And the second part refers to the circuit
9 functionality at the end being able to output a
10 logic high or a logic low.

11 Q Okay, well, let's take it 1 step at a time
12 then. If we look at transistor T2, if transistor
13 T2 is on, that will allow VDD to go to the output
14 terminal which is labeled out has an element 44
15 label as well; is that right?

16 A Well, I will agree with that within the
17 condition that the circuitry has a necessary
18 condition that when you do that transistor T1 is
19 supposed to be off so you don't have a short from
20 VDD to someplace. So within that context, if T1
21 is off and T2 is on, then VDD will be supplied to
22 the output I will agree with that, within the



1 context I just provided.

2 Q Okay. So if T1 is off, T2 is on, then VDD
3 will go out to the output terminal, right?

4 A That is the function of the logic of that
5 circuit, yes.

6 Q Okay. And VDD work high, a high signal a
7 logic high in this case; is that right?

8 A As described here that would be the
9 general expectation, yes.

10 Q Okay. And then similarly, let's assume
11 that T2 is off and T1 is on, that would allow the
12 signal of C1 to go out to the output terminal,
13 right?

14 A Yes, if T2 is off and T1 is on, then the
15 signal applied to C1 would be supplied to the
16 output.

17 Q Okay. If we look at Figure 5 of Sasaki,
18 which again you have got reproduced down on page
19 156 of your report if that is easier, we've got
20 this is another timing diagram, right?

21 A Yes, this appears to be the timing diagram
22 that is a key supplies with respect to at least



1 Figure 4.

2 Q Okay and like the timing diagram we were
3 looking at in Kimora on the left we have got some,
4 some signals or node voltages shown on the left
5 and certain time periods shown on the bottom is
6 that right?

7 A Yes, it it is similar to Kimora in that it
8 has at the top he has some input signals in sort
9 of the middle there he has some voltage there at
10 the nodes as the circuit functions at the bottom
11 he has the output signal.

12 Q If we look at C1 we see that C1 has
13 periods where it is low and periods where it is
14 high, right?

15 A Yes, that is correct.

16 Q And so depending on the timing and again
17 under the presumption you made or that you stated
18 that the T2 is off, the signal of C1 which could
19 be high or could be low, will pass-through
20 transistor T1 to the output terminal, right?

21 A If T1 is on, then yes, the signal C1 the
22 clock signal will be passed through transistor T1



1 to the output, that's correct.

2 Q And if we look at for example, going back
3 to figure Figure 5 the period between time T3 and
4 time T4, the signal of C1 would be a low signal,
5 right?

6 A Yes, that is a low signal.

7 Q Okay. So now, let's now probably makes
8 sense to look back at the annotated figure at the
9 top of Figure 4 at the top of page 155 of your
10 report since that is where you have the
11 annotations. You have included in red boxing what
12 Sasaki refers to as its anti reversal circuit,
13 right?

14 A Yes, I believe the red boxing in the quote
15 below does the red boxing reflects what the quote
16 below from Sasaki refers to that to transistor
17 circuitry as being his anti reversal circuit.

18 Q And that is, that is those transistors T7
19 and T8, right?

20 A Yes, and again that is what Sasaki names
21 them always the anti reversal circuit.

22 Q Okay. And so Sasaki teaches that it is



1 anti reversal circuit is operated to keep
2 transistor T2 off at that period of time between
3 T3 and T4 that we were just looking at, right?

4 MR. HERMAN: Objection, form.

5 A I believe what you have just asked is
6 consistent with the description I provide in my
7 declaration so I would say yes.

8 Q Okay. In fact that is, that is what you
9 say in paragraph 378, right?

10 A Yes, that is what I was consulting during
11 the pause is I believe that that is what 378
12 essentially answers your question.

13 Q Okay. And so as you say here, Sasaki says
14 that without its anti reversal circuitry, it is
15 possible for reversal to occur and that would
16 improperly supply the high signal from V_{dd} to
17 the output, right?

18 A Yes, if 2 problems occur 1 I mentioned
19 there is that if both T1 and T2 are on at the same
20 time you have you would obviously have a signal
21 conflict. The other problem of course is know 1
22 which ask fairly observe they just mentioned it is



1 hopefully observe to a decent undergraduate
2 engineer is that if T2 and T1 are both on you
3 could have a extremely high $\wedge$ which could be
4 damaging literally damaging to the circuitry.

5 Q With respect to the anti reversal circuit
6 Sasaki explains that you, would have you put in a
7 signal conflict a distorted output waveform,
8 right?

9 A Well, when you have when you are trying to
10 have a logic circuit which is drawing its logic
11 level from 1 path which is typical if 2 paths are
12 both trying to feed different logic signals to the
13 same node you are going to certainly get a
14 distorted waveform and that would be the lucky
15 outcome.

16 Q So Sasaki provides its anti reversal
17 circuit to the node connected to the gate of T2,
18 right?

19 A Yes, T7 and 108 connected connect to node
20 2 which connects to the gate of transistor T2.

21 Q As we discussed a moment ago, transistor
22 T2 is the transistor through which the high signal



1 VDD can be provided to the output, right?

2 A Yes, the way the basic functionality works
3 is turn T2, T1 off, turn T2 on and you provide VDD
4 directly to the output.

5 Q Sasaki does not provide its anti reversal
6 circuit to the node connected to the gate of T1,
7 right?

8 A It does not provide that to T1 as a as an
9 output from the anti reversal circuit, that is
10 correct.

11 Q So let's, let's look now at paragraph 382
12 of your declaration does just for context here you
13 have started discussing the Shin reference, right?

14 A Yes, this discusses the Shin reference
15 alone.

16 Q Okay. And you are describing the circuit
17 diagram of Figure 11 of Shin as well as the timing
18 diagram of Figure 12, right?

19 A I just wanted to make sure I had them in
20 the big binder of exhibits to my right, but Figure
21 11 shows circuitry and Figure 12 shows a timing
22 diagram, that's correct.



1 Q Okay. And if we look at the top of page
2 159 of your report, there you have annotated
3 versions of figures 11 and 12, do you see those?

4 A That is correct.

5 Q Okay.

6 A Sorry the question was did I see it and
7 the answer is yes, I do see it, I'm sorry.

8 Q And here you are looking at a particular
9 timing of the signal shown in Figure 12 and
10 showing the operation of the circuit at that time
11 point with a annotated version of a circuit
12 diagram, right?

13 A I believe that's the case, yes.

14 Q Okay. And so at this period of time here,
15 we see that when transistor M5 is on, VDD goes out
16 to the output terminal, right?

17 A Yes, because these are PMOS when you have
18 a low signal applied to the gate of M5 that turn
19 business the transistor on.

20 Q Okay. So in Shin's circuit, it is
21 transistor M5 that allows the high signal VDD to
22 go out to the output, right?



1 A That is correct, yes.

2 Q Okay. And then if we look I don't think
3 you have this annotated, but if we were to assume
4 now that M2 were on, that would allow clock 2 to
5 go out to the output terminal, right?

6 A In and of itself if transistor M2 is
7 turned on then the clock 2 signal will also be
8 provided to the output terminal.

9 Q So that?

10 A I should say, let me rephrase that as I
11 was trying to be careful and I botched it.

12 Alone M2 turning M2 on will provide the
13 clock 2 signal to the output terminal that is what
14 I was trying to say.

15 Q Okay. So it is, it is transistor M2 in
16 Shin's circuitry that let's clock 2 pass to the
17 output terminal; right?

18 A Yes, that is the control element for that
19 functionality.

20 Q Okay. So now if we continue down to
21 paragraph 390 of your report, or your declaration,
22 I apologize, you have here a composite circuit



1 diagram that has the circuitry of Shin's Figure 11
2 in black and then the circuitry from Sasaki that
3 you propose combining with Shin's circuit in red
4 do I have that right?

5 A I believe that you do, yes.

6 Q Okay. And in your declaration be you
7 explain that this added circuitry from Sasaki
8 which shown here in red that ensures that the gate
9 of M2 does not go low when it shouldn't, right?

10 MR. HERMAN: Objection, form.

11 A Yes, the objection here is to make sure
12 the transistor 2, transistor M2 stays off.

13 Q Right. Okay. But as we were just
14 discussing, transistor M2 is not the transistor
15 that allows the high signal VDD to pass to the
16 output terminal, right?

17 A Transistor M5 passes the high signal to
18 the output when transistor M5 is turned on, that
19 is correct.

20 Q Okay. But you have applied Sasaki's anti
21 reversal excuse me, anti reversal circuitry to the
22 other transistor 2M2, right?



1 A Yes, the purpose is to keep make sure
2 transistor M2 stays off when transistor M5 is on.

3 Q Let's move now to paragraph 595 of your
4 declaration. So here if we scroll up just a bit,
5 this is where you, your opinions regarding the
6 Tobita reference begin, right?

7 A That is correct, ground Tobita alone
8 discussion, that's correct.

9 Q So let's quickly pull up Exhibit 1006?
10 (Exhibit 1006 discussed.)

11 Q There we are. Is Exhibit 1006 the Tobita
12 that you reference in your declaration?

13 A That appears to be the case and again, I
14 do have my paper clean paper copy of Tobita to my
15 right in the binder on the chair to my right here.

16 Q Okay. Can we refer to Exhibit 10 '06 as
17 Tobita?

18 A Again, because there is only one Tobita
19 reference that shouldn't be a problem.

20 Q Great. So let's go down now to paragraph
21 614. Here you are discussing the claim limitation
22 1B which is the first driver limitation, right?

1 A Yes, and once again if you want to if it
2 makes your life easier to call that the first
3 driver claim element or claim limitation I'm fine
4 with that.

5 Q Appreciate it. So as we previously
6 discussed actually I think you use the same color
7 scheme have you identified in figure 20 of Tobita
8 in blue boxing the elements that make up the first
9 driver, right?

10 A Yes, the same colors have been used
11 throughout hopefully for to ease the task.

12 Q So that included in the blue boxing or a
13 number of transistors I will just let them, Q3,
14 Q4, Q5, Q18, Q19, Q20, Q21. Did I, did I get them
15 all?

16 A I didn't follow that list because it was
17 long, so I will just read what I think what.

18 Q Okay?

19 A What I have here just to make this if they
20 don't match up tell me because I can't see the,
21 you know the transcript. Q as in Quebec 19, 21,
22 20, 18, 3, 4, and 5 are the transistors I have



1 labeled as being part the first driver.

2 Q Thank you.

3 A Did it match your list by the way.

4 Q It did, yes?

5 A Greats I just wanted --

6 Q I started right to left I think you may
7 have started left to right but we hit the same
8 spot?

9 A As long as the list match I just want to
10 make sure we don't later someone is looking at
11 that and saying these guys are talking past each
12 other.

13 Q Always appreciate a clean record.

14 So if we if we look now at paragraph 617
15 of your declaration here you are offering an
16 opinion as to how you believe the requirement that
17 the first driver controls the voltage of the
18 second node in accordance with the signal of the
19 second input terminal is met, right?

20 A Yes, that appears to be what I'm
21 discussing there.

22 Q Okay. And you have identified the second

1 input terminal here as CK2 is that right?

2 A Yes, just to make sure this is unfortunate
3 the way Tobita and other people do it CK2 is the
4 terminal and above it it refers to a signal
5 applied to it, so CK2 is the terminal that is
6 being referenced although he does seem to okay,
7 CK2 is, is the second input terminal, there is
8 more than 1 instance where it goes into the
9 circuit in different places.

10 Q Right. And so just to clarify that, here
11 is we're look at figure 20, CK2 is, is the input
12 terminal and then the /CLK would be the signal
13 provided to that terminal is that what you are?

14 A That is just a clarification, because
15 everyone who has worked on this has stumbled
16 across this at some point and stumbled over it, so
17 CK2 is the terminal physiologies that were and
18 anatomy, sorry, and the clock signal slash, the
19 /CLK is the physiology it is the clock signal that
20 is being applied to that terminal.

21 Q Right. So that is why I say just below
22 the annotated figure here this occurs when the



1 input signal paren they tech ale /CLK at the
2 second input terminal CK2 is pulled to a
3 particular voltage, right?

4 A Yes, that is correct, because I said
5 everyone who has worked on this, this material and
6 some of these references has stumbled across that
7 difference between the terminal and the signal.

8 Q Okay. And so if we look here at, at the
9 annotation we see that the, the signal of the
10 second input terminal so the /CLK goes to the gate
11 of transistor Q19 and then we see the high signal
12 VDD the high voltage VDD going down through
13 transistor Q19, right?

14 A Yes, that are turns transistor Q19 on and
15 so the VDD is essentially supplied transparently
16 through Q19 to the wiring beyond Q19.

17 Q Okay. And that is, that is what you
18 referred to when you say in paragraph 617 this
19 occurs when the input signal /CLK at the second
20 input terminal CK2 it is pulled through a voltage
21 causes transistor Q19 to turn on this will pull
22 the node labeled N6 to the high i.e. VDD voltage



1 level; is that right?

2 A Yes, that is correct, and I believe you
3 are just reading from below the figure there and
4 you read correctly.

5 Q Okay. And so Q19 there is controlling the
6 voltage of node N6, right?

7 A Q19 are the controls supplies that voltage
8 to N6 however you would like to phrase the
9 terminology but yes.

10 Q Okay. And then if we go down to the next
11 paragraph here you are discussing the requirement
12 that the first driver is able to control the
13 voltage of the second node in accordance with the
14 signal of the third input terminal, right?

15 A Yes, that is how 618 does begin as you
16 have it on the screen and I do again, I have that
17 in my paper copy as well.

18 Q And here you have identified CK1 as the
19 third input terminal and here CLK would be the
20 signal of the third input terminal, right?

21 A Well, as I say right below the figure
22 there, that the third input terminal is CK1 which



1 again has more than 1 pin on this figure, but it
2 it all the same input terminal and the signal that
3 is applied to it is in this case is the signal CLK
4 the clock signal CLK.

5 Q Okay.

6 A By the way if we could scroll down if
7 whoever has control of that I think at this point,
8 thank you because we get, thank you that go it is
9 what I was just discussing there below the figure.

10 Q Okay. And of the transistors that you
11 have identified as part of the first driver
12 transistor Q21 is the only one that has its gate
13 connected to the third input terminal, right?

14 A I was just examining it carefully and that
15 does appear to be the case, yes.

16 Q So if we, if we look just a little below
17 the figure that is on the screen in paragraph 618
18 there you say or down a little bit below the
19 figure thank you, yeah.

20 There you say this occurs when the input
21 signal CLK at the third input terminal CK1 is
22 pulled to a voltage that causes transistor Q2 to



1 turn on do you see that?

2 A Yes, and that does appear to be a typo.

3 Q Okay. Well, have you anticipated my next
4 question. Based on the annotation should that Q2
5 be Q21?

6 A As far as I can tell, yes, those 2
7 instance of Q2 should be Q21 that was a typo that
8 I did not notice and as far as I can tell, that
9 are is a typo it should be Q21.

10 Q Okay. So continuing now with what we will
11 try to fix the typo as we go, this causes the low
12 voltage level VSS to be passed through transistor
13 Q21 to the node labeled N6 do you see that?

14 A Yes, I see that and again, with the
15 assumption again that this is a typo as I believe
16 it is, then that that makes sense now.

17 Q Okay and that is consistent with the
18 annotation that you have immediately above that
19 passage, right?

20 A That is correct, yes.

21 Q Okay. You and so again here transistor
22 Q21 is controlling the voltage of the node N6,



1 right?

2 A Yes, when Q21 is turned on and again
3 assuming the timing does not is only has one of
4 the one of these things we just the previous
5 discussion is not operational it is turned off,
6 then Q21 being turned on will pass the voltage VSS
7 to node 6 and node 6 and 6 will take on that
8 voltage.

9 Q Okay. And then continuing then you say
10 that that, that voltage will be passed to the gate
11 of transistor Q18 which causes transistor Q18 to
12 be turned off, right?

13 A Yes, that is correct.

14 Q So when Q18 turns off, then VSS won't go
15 up through transistor Q18, right?

16 A Well, actually if you can see there it is
17 just kind of very top there the lower part of Q18
18 is not connected to VSS it is connected to S1, so
19 when Q18 is on S1 will pass-through Q18 to node 6
20 and when transistor Q18 is off, you will not be
21 able to pass the signal S1 whatever is at S1 up to
22 node 6.



1 Q Do you read this to say that the signal at
2 S1 is not VSS?

3 A I'm looking at the figure right now, and I
4 think it is reasonable to assume that it is the
5 annotation may be a little as I don't see a signal
6 S1 I believe that is the case it is just the way
7 the way Tobita has drawn this is can be inferred
8 that VSS only applied to write to the transistor
9 Q8 but I think it is reasonable to assume it
10 should be in the middle and pointed to both of
11 them.

12 Q Okay. Well, maybe we can do this specific
13 signal agnostic, if, if Q18 is off the signal at
14 S1 will not be provided through transistor Q18,
15 right?

16 A That is correct. When transistor Q18 is
17 off it will block the node from whatever is at S1.

18 Q But no longer providing a signal through
19 transistor Q18 will not of itself change the
20 voltage of the node on the other side of Q18,
21 right?

22 MR. HERMAN: Objection, form.



1 A Sorry that was extremely convoluted so I
2 kind of lost your train of thought there counsel
3 or.

4 Q Sure, let's break it down?

5 A Sure.

6 Q If we look at the figure here you would
7 agree with me that there is a node N1, right?

8 A The label sell off the page right now but
9 from my paper copy.

10 Q Can we scroll up on have the figure?

11 A Sorry.

12 Q Right there perfect?

13 A That perfect, thank you.

14 Q Okay, so I will repeat the question you
15 will agree with me there a node N1?

16 A Yes, node N1 and we can see what it is
17 now.

18 Q And we were talking about 1 side of Q18
19 where we see the terminal S1, right?

20 A Yes, there a terminal S1 connected to the
21 bottom of transistor Q18.

22 Q Right. And then the top of transistor Q18



1 is connected to node N1, right?

2 A That is correct.

3 Q Okay. So if transistor Q18 turns off,
4 then the signal of S1 will not be provided through
5 Q18, right?

6 A When Q18 is on it will be when Q18 is off
7 it won't be, that is what a transistor in a
8 digital form does.

9 Q Absolutely. So when Q18 turns off, and
10 the signal of S1 is no longer provided through Q18
11 no longer providing that signal will not itself
12 change the voltage on node N1, right?

13 MR. HERMAN: Objection, form.

14 A Sorry I was studying something, could you
15 repeat the question, please, sorry.

16 Q Will sure, if the signal of S1 is no
17 longer provided through Q18 to node N1, that alone
18 will not change the voltage on node N1, right?

19 A When Q18 is off Node 1's voltage will not
20 be affected at all by the signal at the bottom of
21 transistor Q18 again that is a digital transistor
22 form does, it will block that in the off



1 condition.

2 Q Let's go down quickly to let's see there
3 we go, sorry, my feed was not working so I think I
4 understand your question, but let me understand
5 the voltage on node N1 won't change as a result of
6 turning off transistor Q18, right?

7 MR. HERMAN: Objection, form.

8 A Well, it will not change in response to
9 the signal from S1 it may be changed for other
10 reasons of course, but the signal S1 will not have
11 any effect on the voltage on node 1 when
12 transistor Q18 is off.

13 Q And so let's assume that just prior to
14 turning transistor Q18 off there is no other
15 signal voltage applied to N1 and then let's say
16 the only thing that changes in the operation of
17 the circuit is the Q18 is the Q18 turns off; okay,
18 are you following me?

19 A I'm following you are adding other circuit
20 operations in here of course.

21 Q Sure, but if we assume that nothing else
22 is impacting node N1, so node N1 is at a



1 particular potential, right?

2 A Okay.

3 Q And we turnoff Q18?

4 A Okay.

5 Q N1 may now be floating, right if no signal
6 is being provided to the node, right?

7 A Well, if the node is not connected to a
8 rail to a fixed potential then it would be
9 floating that is what floating means.

10 Q Okay. And so but that won't change the
11 voltage on N1?

12 MR. HERMAN: Objection, form.

13 A Well, I will break my answer down into 2
14 things. The first thing again is if you have an
15 ideal circuit and you have node one is floating,
16 it will retain its voltage. That may not happen
17 for other reasons you could have leakage you could
18 have some sort of you know signal integrity issue,
19 but in terms of Q18, if you turn Q18 off, then the
20 S whatever is at S1 at the bottom of Q18 is
21 disconnected from node 1 and will have no affect
22 there.



1 Q And so the operation there of Q18 and the
2 first driver will have no affect on the voltage of
3 node N1, right?

4 MR. HERMAN: Objection, form.

5 A Well, again, if you turn it off and within
6 the context of not having leakage if it is an
7 ideal situation, then S1 will be isolated from N1
8 and will have no effect upon the voltage of node
9 1.

10 Q Let's move now to paragraph 622 of your
11 declaration. And I want to start about halfway
12 down the paragraph it says additionally while I
13 recognize that certain of transistors Q3 to Q5 and
14 Q18 to Q21 do not directly provide output to node
15 N1, let's, let's pause there. What distinction do
16 you make between directly providing output and
17 indirectly providing output?

18 A What I've tried to explain there is it is
19 also it is consistent with the last part of Claim
20 1 of the '593 patent, which refers to directly
21 controlled that the claim says so I hung back to
22 it the claim says in accordance with, and so what



1 I'm just noting here is that these transistors do
2 not directly connect to node N1 but they can be
3 controlled in a way which turns on other
4 transistors which provide a more than 1 transistor
5 path to provide a signal to the node N1.

6 Q Okay. Help me understand exactly what you
7 mean by a more than 1 transistor path to provide a
8 signal to N1?

9 A Well, I think I can illustrate that with
10 the figure I have in paragraph 617 which we
11 discussed a few minutes ago whereas I said the
12 signal on CK2 turns on transistor Q19 that, that
13 turns Q19 on and Q19 therefore provides the VDD
14 high signal down to transistor Q18 and by turning
15 transistor Q18 on, now, whatever signal it is on
16 S1 goes up is able to go up through to node 1 and
17 so that is what I meant by your controlling that
18 by more than 1 transistor.

19 Q Okay. So if we if we down at paragraph
20 618 it a similar situation but here no signal is
21 provided to node N1, right?

22 MR. HERMAN: Objection, form.



1 A Well, again it is the same sort of thing
2 that the signal is applied there to the CLK signal
3 is provided to the terminal in the orange
4 annotation going to Q21. Q21 turns on and -- and
5 that provides a low signal to N6 and that signal
6 N6 is then able to turnoff Q18. And turning off
7 Q18 controls the voltage on node N1 by preventing
8 S1 from getting to it that is what I meant there
9 by controlled.

10 Q But you just told me that that doesn't
11 actually change the voltage of N1, right?

12 MR. HERMAN: Objection, form.

13 A It doesn't change it, but it controls it
14 in the sense that it prevents something from
15 getting in. Prevention is like turning off a
16 water faucet is a form of control.

17 Q So you said a more than 1 transistor sorry
18 I want to get it right more than 1 transistor path
19 to provide a signal to the node N1. Is there any
20 limit on the number of transistors that can be on
21 the path?

22 MR. HERMAN: Objection, form.



1 A The claim merely says in accordance with,
2 so if you have cause and effect, I don't see any
3 reason that accordance limits the number of
4 transistors that could be there here we have 2,
5 but that is more than one.

6 Q So if we look at for example, there is a
7 node between Q1 and Q2 do you see that it is not
8 labeled, but?

9 A Well, essentially that is the output node.

10 Q Right. So would you say that Q18 controls
11 that the voltage of that node in accordance with
12 certain signals?

13 MR. HERMAN: Objection, form.

14 A If you turn Q18 on or off, that, if you
15 turn if you Q18 is on the node N1 with voltage
16 will change and as a further effect of that it is
17 controlling the gate voltage on Q1 owe changing
18 the signal to the bottom of Q18 could change the
19 gate voltage on Q1 and cause Q1 to turn on or off.

20 Q In your opinion, that would be controlling
21 the voltage of that node in accordance with
22 certain input signals?

1 MR. HERMAN: Objection, form.

2 A It seems to meet the criteria of in
3 accordance with.

4 Q If we turn back now to paragraph 622 of
5 your declaration if we continue where we were
6 reading I will read it again, so we have context
7 additionally while I recognize that certain of
8 transistors Q3 to Q5 and Q18 to Q21 do not
9 directly provide output to node N1 as mentioned
10 earlier, it is my understanding that patent owner
11 has taken the position in the associated ITC
12 action that the claim first driver can indirectly
13 control node voltages do you see that?

14 A Yes, it is my understanding from having
15 been there that that is the position that the
16 patentholder was taking in the ITC action with
17 respect to its infringement contentions.

18 Q And why did you reference that, that
19 position here in this paragraph?

20 A Well, I referenced it simply because it
21 was the ITC action was ongoing at the time and
22 that was obviously going to be disputed at the



1 hearing.

2 Q Do you agree with patent owners position
3 in the, in the ITC action?

4 MR. HERMAN: Objection, form.

5 A I don't think I'm saying here whether I
6 agree or not, all I was noting is that if I apply
7 the patent owner's position at the ITC, it
8 actually agrees with my discussion here that in
9 terms of their infringement contentions, they take
10 the, they took the position in the infringement
11 contentions that this would be in accordance with
12 it doesn't have to be directly controlled through
13 a particular transistor they took the opposite
14 position in their invalidity contentions and so,
15 when I'm pointing out here is that what I'm
16 showing here and discussing in this paragraph is
17 consistent with what the patent owner's position
18 is for their infringement contentions.

19 Q But we were just a moment ago when we were
20 talking about the operation of Q18 you told me
21 that a more than 1 transistor path and you said it
22 would meet the criteria of in accordance with,



1 right?

2 A That is my interpretation, yes, that it
3 would be in order to show in accordance with, it
4 does not have to be a transistor that directly has
5 access to the node in question.

6 Q Okay. So in your opinion, the first
7 driver can indirectly control node voltages,
8 right?

9 A Well, in my opinion, I would I wouldn't
10 necessarily say it is indirect or because that, I
11 don't know exactly what you mean by that, but all
12 as I point out here that in accordance with in my
13 view includes you turn a transistor on it passes a
14 voltage through to the gate of another transistor
15 and by turning that transistor on, that actually
16 controls the voltage of the node directly through
17 the second transistor but since the first
18 transistor signal applied to the first transistor
19 starts the process, that meets the in accordance
20 with that the claim element recites.

21 Q Okay, well, help me understand because you
22 just said you wouldn't necessarily say it is in



1 direct, but in paragraph 622 you say I recognize
2 that certain of transistors Q3 to Q5 and Q18 to
3 Q21 do know directly provide output to node N1,
4 right?

5 A Yes, and I realize reading it I did use
6 the word indirectly I thought you had come up with
7 that word I was being careful I see I use it.
8 What I'm just referring to again there is the end
9 of Claim 1 I think it is the last claim element
10 uses the word directly, not in accordance with,
11 and so I took the difference to mean that directly
12 means that it is this transistor has to be
13 controlling the node on its own whereas in
14 accordance with is not restricted to having as we
15 just described the VDD being passed 50 transistor
16 is turned on pulls VDD high and the other side of
17 the transistor which goes to the gate of a second
18 transistor and by controlling the gate of that
19 transistor controls the voltage to the node is
20 that, that is the view I've taken here and I've
21 just pointing out that the patent owner did agree
22 with that in a particular situation.



1 Q Okay. So just to be clear, as you are
2 applying it here you agree with patent owner's
3 position in the associated ITC action that the
4 claimed first driver can indirectly control node
5 voltages?

6 MR. HERMAN: Objection, form.

7 A Well, I would say that I think the patent
8 owner and I are in agreement on that. I believe
9 it was specifically for their infringement
10 contentions, so I believe that we patent owner and
11 I agree on as far as the patent owner's particular
12 use of that in the ITC that they're on the same
13 page as me as this indirect control can meet the
14 in accordance of the claim element.

15 Q And that is, that is the application that
16 you or the analysis that you provided here in your
17 declaration, right?

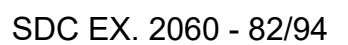
18 MR. HERMAN: Objection, form.

19 A Yes, I did feel restricted to directly
20 controlled in this analysis.

21 Q Why don't we take a short break?

22 A 5 minutes, 10 minutes what do you need









- [REDACTED]
- - [REDACTED]
- [REDACTED]
- [REDACTED]
- - [REDACTED]
- [REDACTED]
- [REDACTED]
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[REDACTED]

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[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

11 VIDEOGRAPHER: We are going off the record

12 the time is 11:30 a.m.

13 (Recess, 11:30 to 11:47 a.m.)

14 VIDEOGRAPHER: We are going back on the

15 record the time is 11:47 a.m.

16 Q So I just want to sort of clarify for the
17 record the exhibit that I previously introduced
18 Exhibit 2024 Dr. Foty seems to have introduced
19 some confusion as to where that comes from that is
20 publicly-available information it is from an
21 injured gadgets product with a serial number
22 IP12-AS-FX5 given the confusion and reference to

1 potential I it, doctor C issues, and Dr. Foty's
2 answers, regarding that exhibit, we think that
3 that testimony should be struck from the record
4 and with that, I have no further questions for the
5 witness?

6 MR. HERMAN: This is com for petitioner,
7 before we conclude today, Dr. Foty, I just have 1
8 question for you.

9 A Sure.

10 Q Counsel for patent owner asked you
11 questions about paragraph 622 of your declaration
12 and you read certain portions of paragraph 622; is
13 that right?

14 A I believe I read some portions of it into
15 the record, yes.

16 Q Okay. And in the final sentence of that
17 paragraph 622, you say, in any event, as I
18 explained above, there are multiple transistors in
19 to be that's first driver that do in fact
20 directly provide output to node N1 including
21 transistors Q3, through Q5 and Q18, correct?

22 A Yes, that is what I wrote, and I'm just



1 trying to verify given there was an earlier typo
2 that that statement is tautologically correct. Q3
3 works, Q4 works, Q5 works, and Q18 works, so those
4 appear to be the, there is 4 transistors all
5 connect directly to node 1 and I don't think there
6 are any others but if there are, I just didn't
7 list it there.

8 Q Now, the universe of transistors that you
9 identified as being part of the first driver I
10 believe you will discussed this with counsel and
11 the universe of transistors include Q3, Q4, Q5,
12 Q18, Q19, Q20 and Q21, correct?

13 A Yes, I believe we listed those as being 7
14 transistors that are to be included in Tobita
15 driver 1, or first driver sorry the patent calls
16 that a first driver so we identified that as being
17 the first driver in to be that.

18 Q It is presence of all of those transistors
19 in your opinion that causes Tobita to teach the
20 required first driver, correct?

21 A I believe that is the case, yes.

22 MR. HERMAN: I don't have any further



1 questions.

2 MR. ANDROS: Just maybe one or 2 more from
3 me.

4 Q So you were just discussing with counsel
5 transistors Q3, Q4, Q5, and Q18 in to be that's
6 figure 20, right, Dr. Foty?

7 A Yes, I believe we just had that
8 discussion.

9 Q Okay. But none of transistors Q3, Q4, Q5
10 or Q18 have their gate connected to what you
11 identified as the third input terminal which is
12 CK1, correct?

13 A Did you list Q18 with that list just so I
14 have the is it 3, 4, 5 and 18 you just listed
15 counselor I just want to be very careful.

16 Q That is correct, 3, 4, 5, and 18 which
17 should be the same that counsel asked you about a
18 moment ago?

19 A And the question was they don't have their
20 gates connected to.

21 Q The third input terminal what you identify
22 as the third input terminal, CK1?



1 A As far as I can will it, none of those
2 have their gates connected to the third input
3 terminal.

4 MR. ANDROS: I have no other questions
5 from me.

6 MR. HERMAN: Same here, and I think with
7 that Dr. Foty I think we may be done for the day
8 thank you for your time.

9 A Thank you very much.

10 MR. ANDROS: Thank you Dr. Foty.

11 VIDEOGRAPHER: Counselor do you want a
12 copy of the video.

13 MR. HERMAN: This is counsel for
14 petitioner I do not need a copy of either the
15 video or the transcript.

16 MR. ANDROS: Whatever our standing order
17 is fine here.

18 VIDEOGRAPHER: Understood, and this marks
19 end of the deposition of doctor Daniel Foty, the
20 time on the monitor is 11:53 a.m.

21

22