

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

MIANYANG BOE OPTOELECTRONICS TECHNOLOGY CO., LTD.; TCL
CHINA STAR OPTOELECTRONICS TECHNOLOGY CO., LTD.; TIANMA
MICROELECTRONICS CO. LTD.; AND VISIONOX TECHNOLOGY, INC.,

Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.,

Patent Owner.

Case No. IPR2024-00620
U.S. Patent No. 9,330,593

PETITIONER'S REPLY

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LISTING OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 9,330,593 (the “’593 patent”)
1002	Prosecution History of U.S. Patent No. 9,330,593
1003	Declaration of Dr. Daniel Foty (“Foty”)
1004	U.S. Patent Publication No. 2011/057190A1 (“Kimura”)
1005	U.S. Patent Publication No. 2007/0063950A1 (“Shin”)
1006	U.S. Patent Publication No. 2008/0101529A1 (“Tobita”)
1007	U.S. Patent Publication No. 2008/0062097A1 (“Jeong”)
1008	Excerpts from <i>Analog Integrated Circuit Design</i> , David A. Johns et al., John Wiley & Sons, Inc. (1997)
1009	Complainant’s Opening Claim Construction Brief, <i>In the Matter of Certain Active Matrix Organic Light-Emitting Diode Display Panels and Modules for Mobile Devices, and Components Thereof</i> , Inv. No. 337-TA-1351
1010	Excerpts from <i>Physics and Technology of Semiconductor Devices</i> , A. Grove, John Wiley & Sons (1967)
1011	Excerpts from <i>CMOS Digital Integrated Circuits: Analysis and Design</i> , (third edition), S. Kang et al., McGraw-Hill (2003)
1012	Docket from <i>Samsung Display Co., Ltd. v. BOE Technology Co., Ltd.</i> , E.D. Tex. 2-23-cv-00309
1013	U.S. Patent Publication No. 2003/0132931A1 (“Kimura”)
1014	U.S. Patent Publication No. 2005/0185752A1 (“Sasaki”)
1015	U.S. Patent Publication No. 2007/0139348A1 (“Lee”)
1016	U.S. Patent No. 4,720,815 (“Ogawa”)

1017	EP 0 138 406 A2 (“Takemae”)
1018	U.S. Patent No. 4,740,922 (“Ogawa II”)
1019	Excerpts from Wolf, “Silicon Processing for the VLSI Era: Volume 2 – Process Integration” (1990)
1020	U.S. Patent Publication No. 2007/0263763 A1 to Moon (“Moon”)
1021	<i>Intentionally Omitted</i>
1022	J. Miller, “Dependence of the input impedance of a three-electrode vacuum tube upon the load in the plate circuit,” Scientific Papers of the Bureau of Standards, 15(351), pp. 367–385 (1920)
1023	US Patent Publication No. 2007/0085808A1 (“Lee”)
1024	US Patent Publication No. 2007/0085808A1 (“Lee”)
1025	Reply Declaration of Dr. Daniel Foty (“Foty Reply”)
1026	Transcript from the February 25, 2025 Deposition of Andrew Wolfe, Ph.D.
1027	U.S. Pub. No. 2020/0410943 A1 (“Kim”)
1028	U.S. Pub. No. 2021/0074220 A1 (“Kim II”)

Petitioner submits this reply in support of its Petition for IPR of the '593 patent. See Petition (Paper 1). Rather than dealing with the prior art as it is, Patent Owner and its expert repeatedly attempt to improperly *re-write* the art.

Patent Owner's discussion of Kimura is the most egregious example of this. According to Patent Owner, the Petition's analysis of Kimura Fig 27C is somehow "flawed." But the Petition correctly reads that figure in the context. Kimura unambiguously teaches that Figure 27C's shift register circuit builds off circuits in earlier figures. This is the case with all Kimura's figures. Each adds transistors or modifies circuit elements to address issues, offer alternatives, or effect improvements. Kimura's detailed step-by-step disclosure enhances its explanatory power to a POSITA, who plainly would have considered Kimura's teachings together. The only proper way to analyze Kimura is to consider not only the circuit of Figure 27C, but also earlier figures showing that circuit's component parts (like Figures 1A, 14A, 16A, 17A, 20A, 21A, 23A, and 25A) and timing diagrams for those components (like that shown in Figure 21B). This is what the Petition did. And this is exactly how Kimura is meant to be read. Indeed, each of these figures are not only related, but Kimura explains that they are all part of the *same* embodiment.

Patent Owner's other arguments are no better. It argues that a POSITA would not apply Sasaki's anti-reversal circuit to Shin's shift register because Shin already

includes a capacitor C1. Patent Owner focuses only on a period of operation where there is redundant protection against reversal. The Petition, however, explained Sasaki’s anti-reversal circuit is needed in a period where there is no redundancy and the capacitor is not supplemented by other circuit elements. Patent Owner addresses none of this. Once again, it seeks to replace Shin and Sasaki’s actual teachings with its own preferred (but erroneous) reading.

Patent Owner’s discussion of Tobita not only ignores the reference itself but is also inconsistent with its other arguments. According to Patent Owner, Tobita’s transistors Q19-Q21 cannot be part of the claimed “first driver” because they only control the voltage of node N1 through transistor Q18. But Patent Owner then takes the opposite view when trying to show that the stage circuit employed by its own Samsung Galaxy S22 product falls within the claim scope. The shift register in that product—like Tobita—includes a first driver (T1-T3) that controls an associated node’s voltage through another transistor (T8).

Finally, Patent Owner’s secondary consideration arguments lack merit. To show the required nexus it points to one of the same products—the Samsung Galaxy S22—that purportedly also has a nexus with a ***completely different*** set of patents relating to pixel layout. This undermines Patent Owner’s argument because it has no evidence that the ’593 patent, as opposed to other technology, is critical to the Galaxy S22’s success. Patent Owner also presents two inconsistent explanations of

why its own product practices the claims and repeatedly points to unclaimed features as purportedly “satisf[ying]” long felt needs and resulting in “succe[ss].”

I. GROUND 1: OBVIOUSNESS OVER KIMURA

Ground 1 explained why Figure 27C of Kimura renders the ’593 patent’s claims obvious. *See* Petition, 14-16.

A. Kimura Renders Claim 1 Obvious

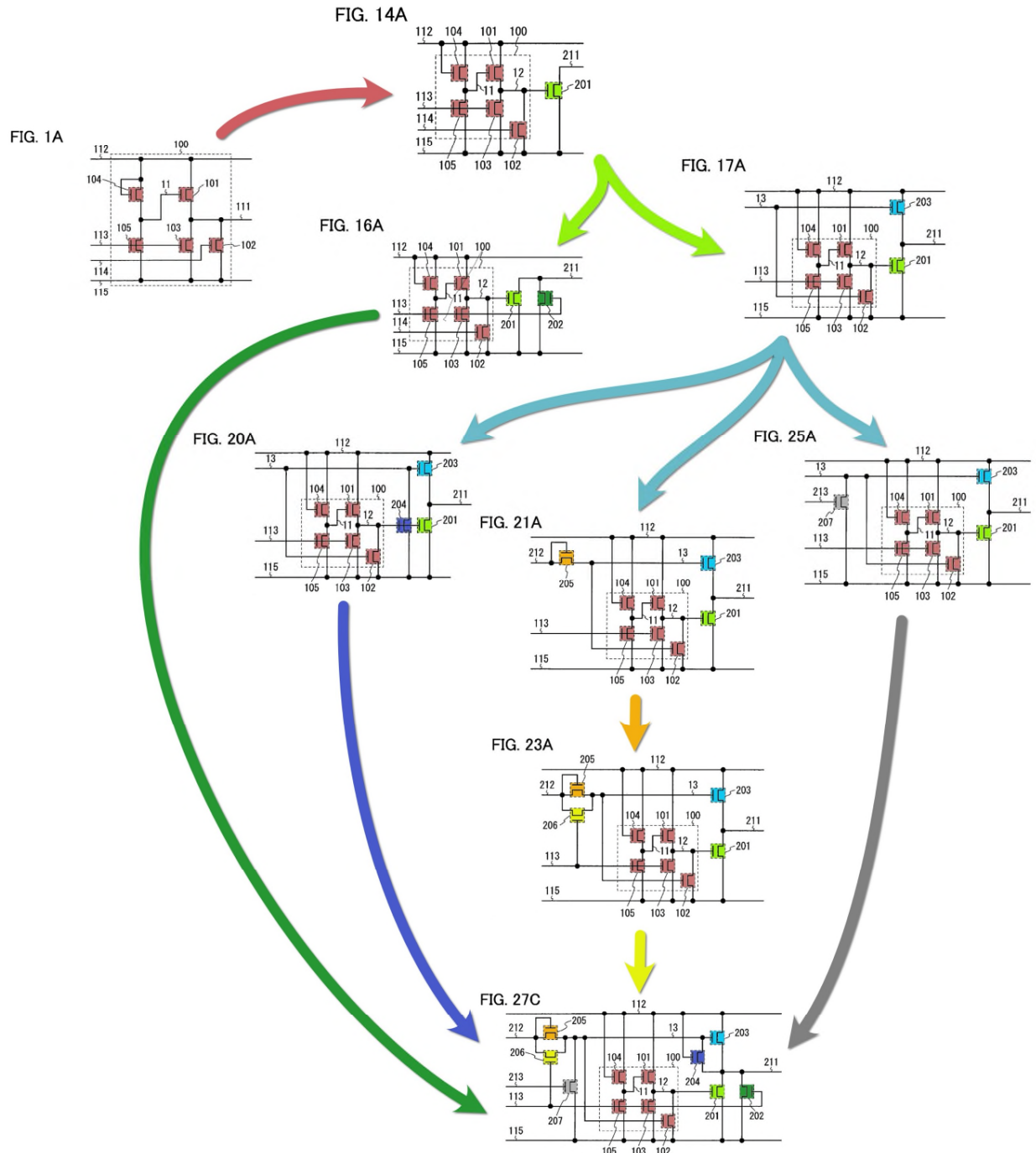
1. *Patent Owner Mischaracterizes Kimura’s Teachings*

Patent Owner argues that the Petition “cites ... description[s] of different circuits from different embodiments.” Response (Paper 23), 7-8. According to Patent Owner, a POSITA would have no idea how Figure 27C functions or what inputs it receives. While the Petition pointed to exemplary “timing diagram” (Figure 21B), Patent Owner argues that this diagram is somehow “inconsistent” with and provides no insight whatsoever into Figure 27C’s operation. *Id.*, 12.

All of this is wrong. Patent Owner fails to even understand—let alone meaningfully address—Kimura’s teachings. Kimura’s embodiments are not distinct and unrelated. Rather, the circuit of Figure 27C “***builds on and shares components with*** the devices of [Kimura’s] other figures.” Petition, 15 (emphasis added). Kimura states this expressly. *See, e.g., id.*, [0093] (later figures include the “same portions or portions having similar functions” as earlier figures); *see also id.*, [0218], [0245], [0249], [0260], [0264], [0270], [0276], [0284] (repeatedly explaining that later circuits add to earlier circuits).

The flow chart below exemplifies the interrelationship between Kimura's figures and circuits. Figure 1A is the starting point and shows five transistors 101-105 (**red**) that produce an output in response to input signals. *Id.*, [0099]. The same five transistors appear in all the circuits that follow, including Figure 27C. *Compare id.*, Figs. 1A, 27C. Kimura then teaches how the addition of transistors improves operation. Figure 14A adds transistor 201 (**light green**). *Id.*, [0218]-[0219]. This "reduc[es]" transistor "on" time to "suppress[]" "deterioration." *Id.*, [0228]. Figure 16A adds transistor 202 (**dark green**). *Id.*, [0245]-[0246]. This reduces noise on wiring 211—the circuit's output—to improve "display quality." *Id.*, [0247]. Figure 17A adds transistor 203 (**light blue**). *Id.*, [0249]. This outputs a high signal at the appropriate time. *See id.*, [0249]. Figure 20A adds transistor 204 (**dark blue**). *Id.*, [0260]-[0261]. This allows the "potential of ... node 13" to be "lowered" again reducing transistor deterioration. *Id.*, [0262]. Figure 21A adds transistor 205 (**orange**). *Id.*, [0264]-[0265]. This implements a "start pulse" signal. *Id.*, [0266]-[0267]. Figure 23A adds transistor 206 (**yellow**). *Id.*, [0270]-[0272]. This provides a more "noise-resistant semiconductor device" by "fix[ing]" the potential of node 13 in period B. *Id.*, [0274]. Finally, Figure 25A adds transistor 207 (**grey**). *Id.*, [0277]-[0280]. This allows for provision of a "reset signal" further lowering node 13's potential in period E. *Id.*, [0280]-[0281]. Figure 27A combines all of transistors 101-105 and 201-207 in a single circuit. *Id.*, [0283]. Figure 27C then simply

relocates transistor 204 to avoid “dielectric breakdown” of “the transistor connected to node 13[.]” *Id.*, [0286].



Id., Figs. 1A-27C; *see also* Foty Reply (Ex. 1025), ¶¶ 28-45; Ex. 1026, 47:6-52:10 (Patent Owner’s expert recognizing relationships between figures).

So, Kimura’s circuits are not “different” unrelated embodiments. Instead, they are ***related, additive, and intended for us together***. While Patent Owner argues that Dr. Foty “admitt[ed]” at his deposition that there is no “supporting disclosure” in Kimura explaining how its figures interrelate, Dr. Foty instead said the opposite: he pointed Patent Owner to Kimura’s teaching that the circuit of Figure 27C builds on earlier circuits. *See* Ex. 2060, 32:3-33:17. Moreover, Kimura explains the purpose of—and benefit provided by—every single one of the transistors employed by Figure 27C’s circuit. The Petition and Dr. Foty properly followed Kimura’s instruction and teachings. To understand the operation of the circuit in Figure 27C, the rest of Kimura must be considered. Patent Owner failed to do so. *See Ericsson Inc. v. Intellectual Ventures I LLC*, 890 F.3d. 1336, 1346 (Fed. Cir. 2018) (arguments “plainly inconsistent with the record” disregarded).

Patent Owner’s discussion of Kimura’s signal timing diagrams is similarly flawed. According to Patent Owner, Figure 21B’s timing diagram is “not compatible” with Figure 27C because Figure 21B depicts the “potential of node 13 (V13)” as being “at its highest level” in “period D” while Figure 27C’s circuit lowers node 13’s potential in this period. *Id.*, 13-14.

Patent Owner focuses on Figure 21B’s internal node voltages. The Petition, however, relies on Figure 21B for its “***input signals***” IN1, IN2, and IN4 used to drive the circuit not the internal node voltages. Petition, 19 (emphasis added). And these

input signals are the **same** in all the figures on which Figure 27C is based. This is the case **despite** the inclusion of additional transistors in each circuit:

FIG. 14A

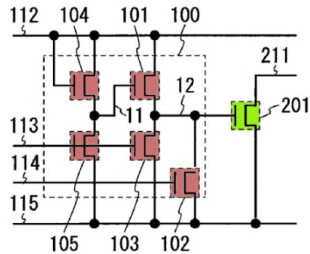


FIG. 15A

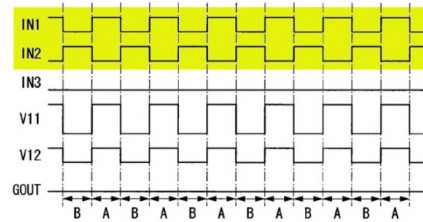


FIG. 17A

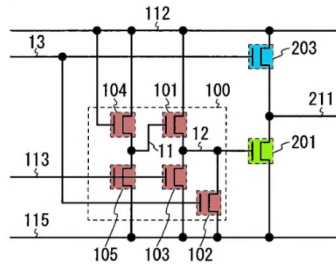


FIG. 17B

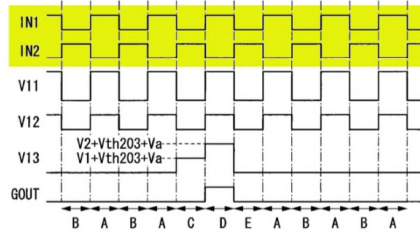


FIG. 21A

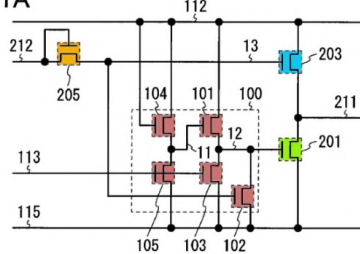


FIG. 21B

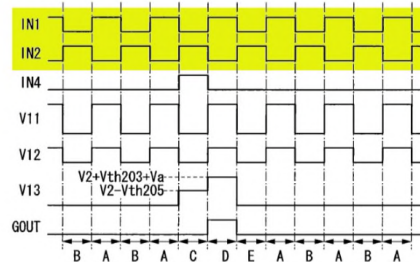


FIG. 25A

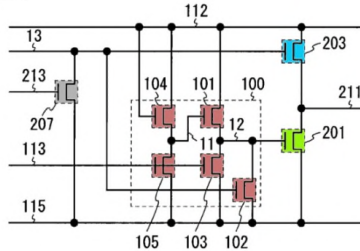
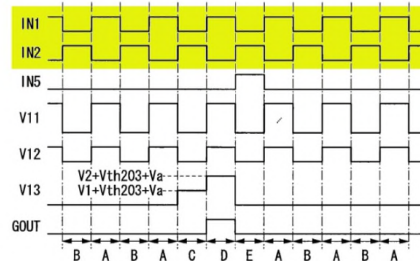


FIG. 25B



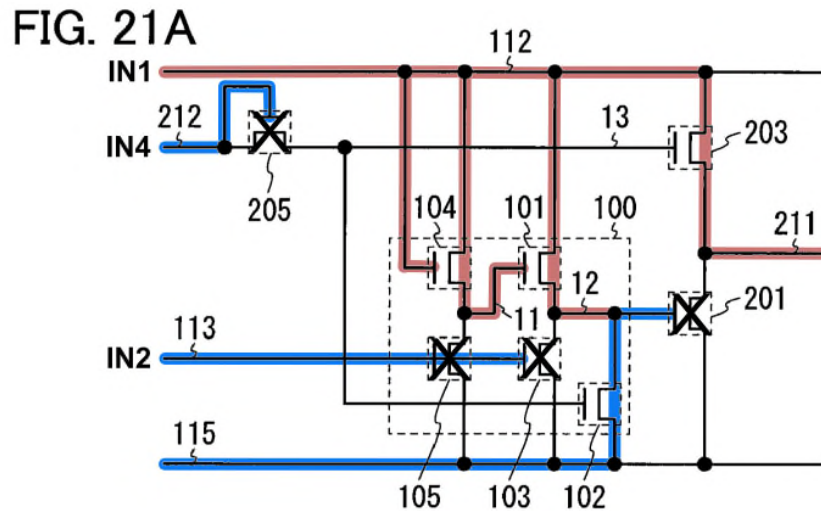
See, e.g., Kimura, Figs. 14A and 15A, 17A and 17B, 21A and 21B, 25A and 25B (all annotated); Foty Reply, ¶¶ 46-60; see also Ex. 1026, 24:25-29:25 (Patent Owner's

expert recognizing similarities between Kimura's timing diagrams); *see also id.*, 30:2-37:14. This is why a POSITA would have understood the Figure 27C circuit uses the same inputs: all of Kimura's other embodiments do the same. Dr. Foty explained this to Patent Owner at his deposition. *See* Ex. 2060, 25:21-27:17. He did not "admit" that Kimura's timing diagrams have no applicability to Figure 27C. *See id.*

Kimura not only includes timing diagrams, but it also discusses how signals are supplied. IN1 and IN2 are both "clock signals" that are "180° out of phase" from each other. Kimura, [0108]-[0109]; *see also id.*, [0229]-[0231]. IN1 is high and IN2 is low in period A. *Id.*, [0226]. The signals reverse in period B, reverse again in the next period, and so on. *See id.*, [0227]. IN4 is "a start pulse." *Id.*, [0266]. This signal goes high in period C causing the circuit to output a high signal in period D. *Id.*, [0269]. Just as shown in the timing diagram, these same inputs are meant for use with **all** of Kimura's circuits and are always supplied on the same input lines. *E.g., id.*, Figs. 1A-27C.

Patent Owner's arguments regarding internal node voltages of Figure 27C circuit—such as V13—being different from that in Figures 21A/21B are irrelevant. The purpose of Figure 27C is to addresses problems arising from the elevated node 13 potential shown in Figure 21B in period D. According to Kimura, in the Figure 21A circuit (the circuit to which Figure 21B directly relates), a high-level "signal

IN4” is supplied to wire 212 in period C. *Id.*, [0269]. This causes “transistor 205” to be “turned on” and the “potential of ... node 13” to rise to “ $V_2 - V_{th205}$.” *Id.* The increase in node 13’s potential turns on transistor 203. *Id.*, Fig. 22A. Then, in period D, IN4 switches back to low turning off transistor 205 and leaving “node 13” in a “floating state.” *Id.*, [0269]. At the same time, IN1 supplied to wire 112 transitions to high and passes through the still open transistor 203 to output line 211:

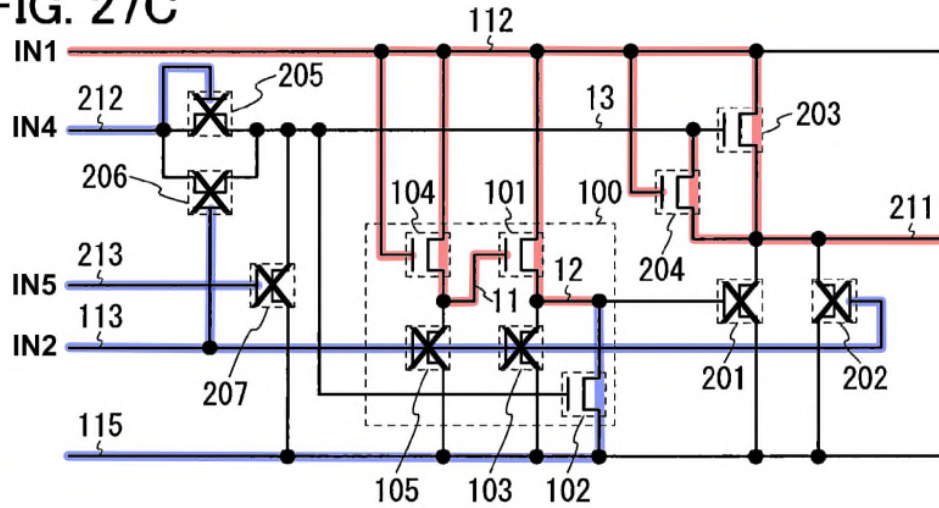


Id., Fig. 21A (annotated); *see also* Foty Reply, ¶¶ 65-66. Kimura explains that this scenario—node 13 is floating while a high voltage is supplied through transistor 203—results in a “bootstrap operation” that causes the potential of node 13 to further increase to $V_2 + V_{th203} + V_a$. Kimura, [0256].

To avoid the transistor “dielectric breakdown or deterioration,” the Figure 27C circuit “lower[s]” the “potential of the node 13” in period D rather than allowing it to increase via bootstrapping. *Id.*, [0286]. To do so, transistor 203’s output is

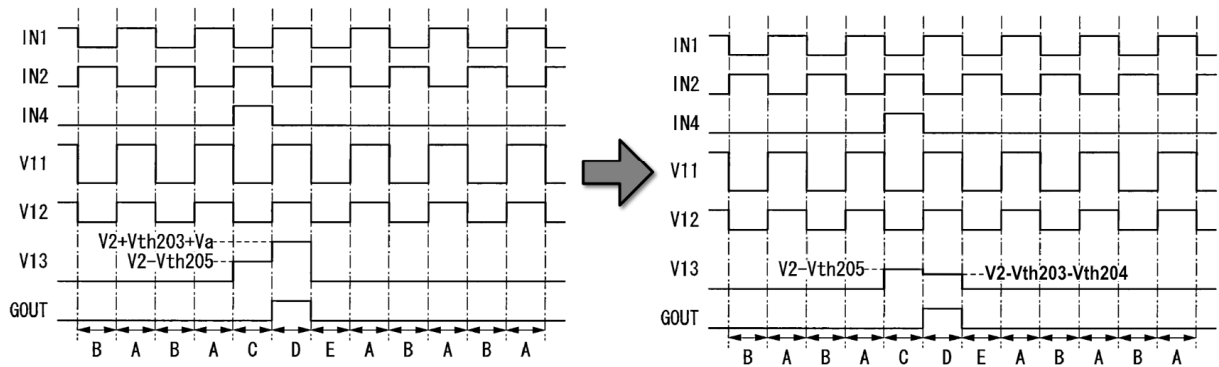
connected to node 13 through transistor 204. *Id.* This allows the high-level signal IN1 supplied to the output through transistor 203 in period D to also be supplied to node 13 via transistor 204. *See id.*, Fig. 27C.

FIG. 27C



Id., Fig. 27C (annotated); *see also* Foty Reply, ¶¶ 67-73; *see also id.*, ¶¶ 11-26; *see also* Ex. 1026, 35:1-38:19. This fixes the node's voltage at a lower potential that still keeps transistor 203 on (for instance, approximately $V_2 - V_{th203} - V_{th204}$) and prevents the bootstrapping-caused potential increase at node 13 in period D:

FIG. 21B



Kimura, Fig. 21B (modified); *see also* Foty Reply, ¶¶ 61-64. So, the Petition’s analysis is not “inconsistent” with Kimura’s figures. Kimura itself already explains the difference between the operation of Figure 27C and what is shown in Figure 21B. Moreover, because Kimura states that the circuit of Figure 27C is meant only to adjust circuit operation in period D (*see* Kimura, [0286]), the plain implication is that the circuit will operate the same in all other periods. Patent Owner fails to properly account for Kimura’s teachings regarding why the circuit of Figures 21A/21B operates the way it does (node 13’s potential is increased via bootstrapping) and how Figure 27C is intended to address this (it is structured to avoid this bootstrapping).

Finally, none of this constitutes an improper “new” argument. Pointing out Patent Owner’s factual errors and mischaracterizations is prototypical reply subject matter. *See Apple, Inc. v. Andrea Elecs. Corp.*, 949 F.3d 697, 706-07 (Fed. Cir. 2020); *see also Axonics, Inc. v. Medtronic, Inc.*, 75 F.4th 1374, 1380 (Fed. Cir. 2024).

2. Kimura Teaches the Claimed “Transistor” That Is “Directly Controlled” by the “Signal of the Third Input Terminal”

Patent Owner next argues that Kimura lacks a “transistor” in its “first driver” that is “directly controlled” by “the signal of the third input terminal.” Response, 14. The Petition pointed to transistor 204 in Figure 27C. *See* Petition, 24. This transistor receives the signal applied wiring 112—the claimed “third input terminal”—at its gate. *See id.* Transistor 204 is part of the claimed “first driver”

because it operates to lower the potential of node 13 during certain periods of the circuit's operation. *Id.*, 20-21.

According to Patent Owner, “Kimura provides no further explanation of this lowering.” Response, 15. Not so. Kimura repeatedly explains that the potential of node 13 can increase due to bootstrapping during period D. See Kimura, [0250]; Figs. 17B, 21B, 25B. Figure 27C avoids the “dielectric breakdown or deterioration” caused by this bootstrap-elevated potential. *Id.*, [0286]. A POSITA would have readily understood from Figure 27C—along with Kimura's input signal timing diagrams—that provision of the signal from wiring 112 in period D effectuates this lowering of node 13's potential. See *supra* Section I.A.1.

Patent Owner also wrongly argues that transistor 204 must itself “turn on or off” transistor 203 (part of Kimura's “outputting unit”) to qualify as part of the “first driver.” *Id.* The claims do not require each first driver transistor to operate this way by itself. Instead, the first driver transistors ***collectively*** “control the voltage of the second node.” See Ex. 1001, Claim 1. This is what transistor 204 does: it contributes—along with transistors 205-207—to the control of node 13's potential.

B. Kimura Renders Claims 6 and 20 Obvious

The Petition also explained how Kimura renders claims 6 and 20 obvious. See Petition, 29. In response, Patent Owner argues that the Petition somehow improperly “suggest[s] that transistor 201 would operate differently between Figure 27C and the

composite Figure 27C and Figure 31B....” Response, 17-18. This misunderstands how the composite circuit operates. Like Figure 31B, the composite circuit has **two** outputs. One of these—line 211—is the same as that shown in Figure 27C. *See* Petition, 29-30. Transistors 201 and 203 continue to control the output signal provided this line as shown in Figure 27C. The composite has a **second** output line 214, which is controlled by transistors 208 and 209. *See id.*; *see also* Kimura, [0304]-[0305]. Transistor 201 does not provide output to line 214. *See id.* Instead, the output of 201 transistor is now supplied to the node 13, which in turn controls transistor 208 and the output on line 214. *See id.* Thus, the Petition’s discussion of claims 6 and 20 simply recognizes the new, dual role played by transistor 201 when Figure 31B is combined with Figure 27C. The transistor (1) continues to control the provision of the line 115 signal to output 211 (making it part of the “outputting unit” for output line 211) and (2) now controls provision of the line 115 signal to the gate of added output transistor 208 (making it part of the “first driver” for output line 214). *See id.* The latter operation satisfies these claims.

Patent Owner next argues that a POSITA would not have been motivated to add transistors 208 and 209 to Figure 27C because doing so supposedly “incur[s] ... significant downsides absent clear benefits.” Response, 20. The only “downside[]” Patent Owner identifies is that additional transistors take up additional space and require further manufacturing costs. *See id.* The ’593 patent does state that “[w]hen

a number of transistors in a stage increases, process yield deteriorates, so that stability of driving is deteriorated.” Ex. 1001, 9:15-22. But the patent proposes different embodiments employing different numbers of transistors. Figure 3 includes seven transistors (M1-M7), two capacitors (C1-C2), and three input terminals (101-103). Figure 7 includes nine transistors (M1-M7, M10-M11), two capacitors (C1-C2), and five input terminals (101-103, CS1, CS2). *Compare id.*, Figs. 3 and 7. The ’593 patent explains that including these additional transistors and inputs is beneficial—despite the extra space and expense—because it allows the circuit to operate bidirectionality. *See id.*, 8:47-52; *see also* Ex. 1026, 20:13-21:19 (Patent Owner’s expert agreeing that the ’593 patent includes embodiments with added circuit elements). Thus, even in the ’593 patent itself, transistor space and expense is not the only factor considered. The functionality achieved by the circuit is equally (if not more) important. If this were not enough, Patent Owner points to a purported commercial embodiment including an extra transistor beyond those in the ’593 patent that—at least in its expert’s view—is completely unnecessary and serves no purpose. *See id.*, 55:7-56:12, 57:20-58:15. If there really were some sort of motivation not to include extra transistors in a stage circuit, then Patent Owner certainly would not have added an extra, unnecessary transistor to its own product.

Kimura also articulates the benefits transistors 208 and 209 provide: they facilitate a further output line that reduces “delay or distortion” when a shift register

output signal from one stage is passed along to the next stage. Kimura, [0304]. Patent Owner does not meaningfully contest that the transistors provide this benefit. Instead, it improperly assumes, contrary to the record, that a POSITA would never under any circumstances consider using more transistors. But the '593 patent claims do not limit the number of transistors and Kimura and the '593 patent itself adds unneeded transistors for functional benefits.

Patent Owner concludes by arguing that line 214 cannot be the claimed “output terminal” because it is not connected “to the pixel circuits via scan lines.” Response, 21. This is not required. Independent claim 1 requires only an “output terminal.” It does not mention pixel circuits or scan lines. While claim 15 does reference a “scan driver for supplying scan signals to the pixels through the scan lines,” it separately claims an “output terminal.” Once again, there is no requirement that the “output terminal” be connected to the “scan lines.” Ex. 1001, Claims 1, 15. The '593 patent does include examples where a circuit's outputs connect to scan lines. But “absent clear and unmistakable language suggesting otherwise”—which is not present here—the claims are not to be limited to preferred embodiments. *Continental Circuits LLC v. Intel Corp.*, 915 F.3d 788, 798 (Fed. Cir. 2019).

C. Kimura Renders Claims 7 and 21 Obvious

These claims require the inclusion of a “first” and “second” capacitor in the claimed stage circuit.

According to Patent Owner, “Kimura never suggests that ... capacitors from different embodiments can or should be added to Figure 27C.” *See* Response, 24. This is wrong. Kimura states that “capacitors can be additionally provided without elimination of transistors.” Kimura, [0198]. It does not limit this to any particular embodiment. Moreover, Kimura makes clear that the component parts making up the circuit of Figure 27C can accommodate capacitors. For instance, per Kimura, a “capacitor 122” can be included in circuit 100. Kimura, [0190]-[0192]. Figure 27C includes a circuit 100. *Compare* Figs. 1A, 27C. Likewise, a capacitor 220 can be connected “between the node 13 and the wiring 211.” *Id.*, [0302]-[0304]. These same elements are also present in Figure 27C. *See id.*, Fig. 27C. Indeed, Kimura specifically identifies Figure 27C as one circuit to which it intends to add a capacitor. *See id.*, [0302].

Patent Owner next faults Petitioner for “seek[ing] to add only capacitor 122 to Figure 27C, and ignor[ing] Kimura’s disclosure that circuit 120” also includes “a resistance component.” Response at 24-25. The Petition did not “ignore” the “resistance component.” Per Kimura, any required “resistance” can simply be “parasitic resistance” or provided by adjusting “the wiring resistance.” *Id.*, [0192]. A separate resistor is not required. *Id.*

Patent Owner also argues that use of capacitors is “inconsistent with Kimura’s focus on preventing or reducing transistor deterioration....” Response at 25. There

is no such inconsistency. According to Kimura, its circuit is designed such that “transistor 201” is not continually on and instead switches between on and off in periods A and B. Kimura, [0228]. The transistor will continue to operate in this manner even when associated with capacitor 122. The capacitor simply adds a minor “delay[]” in the transistor’s operation for purposes “shorten[ing]” the “fall time” of the circuit’s output signal. *Id.*, [0190]. Likewise, inclusion of a capacitor 220 will improve—but not otherwise meaningfully impact—the operation of the circuit of Figure 27C. *See id.*, [0303] (use of a capacitor allows “the fall time or rise time of the signal GOUT” to be “shortened”). Again, the circuit of Figure 27C is already specifically designed to protect the transistors connected to node 13. *See id.*, [0286].

D. Kimura Renders Claims 8 and 22 Obvious

Here, the Petition pointed out that Kimura contemplates both (1) reconfiguring transistor 102 such that one of its terminals is connected to wiring 113 and (2) employing multiple separate power supply voltages. Petition, 35-36.

Patent Owner does not dispute that when the circuit of Figure 27C is modified in this fashion it satisfies claims 8 and 22. Instead, it argues only that these modifications do not apply to Figure 27C. Kimura does provide an example of a modified transistor 102 in Figure 7C. But it also notes that the “**semiconductor device of Figure 1A**”—which includes the same circuit 100 with transistors 101-105 found in Figure 27C—can be modified in the same way. Kimura, [0169] (emphasis

added); [0249] (gate of transistor 102 connected to node 13). Likewise, Kimura explains that “the wiring 115”—which is also found in Figure 27C—can be “divided into a plurality of wirings 115A to 115C” receiving “[d]ifferent voltages or signals.” *Id.*, [0172]-[0173]; *see also id.*, Fig. 30A.

II. GROUND 2-3: OBVIOUSNESS OVER SHIN AND SASAKI

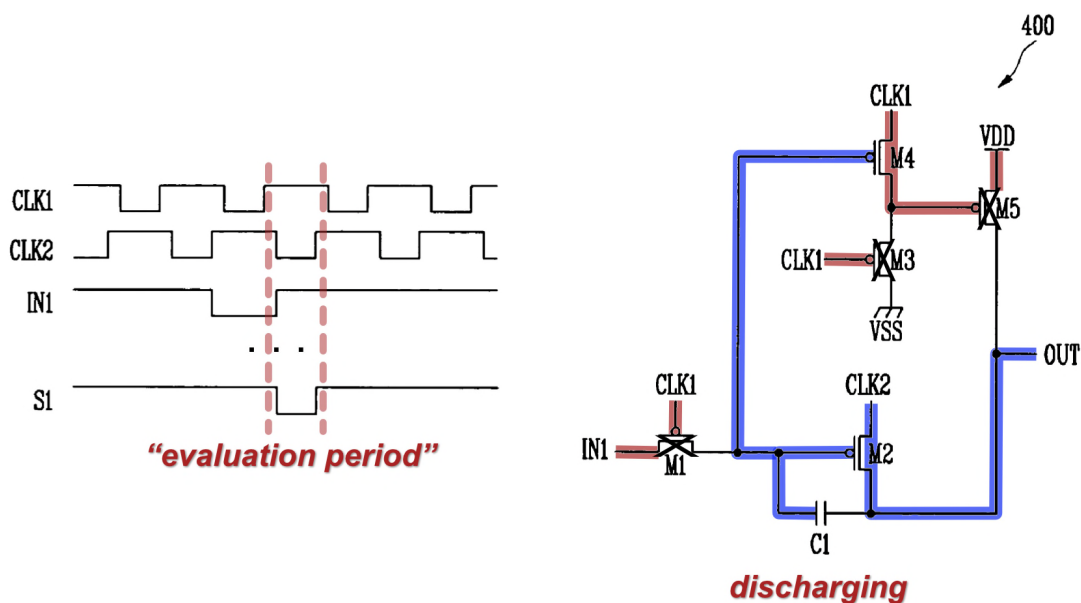
A. Sasaki is Applicable to Shin

Ground 2 explained why Shin—when modified to include Sasaki’s anti-reversal circuit—renders the claims obvious. *See* Petition, 44-54. According to Patent Owner, any benefit provided by Sasaki is “theoretical at best” and supposedly “obviate[d]” by Shin’s inclusion of a capacitor C1. *See* Response, 31-32. Once again, this ignores the prior art’s teachings.

The benefit provided by Sasaki’s anti-reversal circuit is not “theoretical.” The Petition explained—with supporting expert testimony and diagrams—that the gate of transistor M2 is left floating—and is particularly vulnerable—during certain periods of Shin’s operation. Petition, 47-48; *see also* Ex. 1003, ¶¶ 380-383. Patent Owner does not dispute this. Moreover, Sasaki explains why this is a problem: if one of a shift register’s “control electrode[s]” is left “floating” (i.e., “electrical potential is easily variable because” a fixed “voltage ... is not supplied”), then the “voltage level at the control electrode” is liable to be “reversed” resulting in the circuit outputting the wrong signal. Sasaki, [0042]. So, the problem with Shin’s

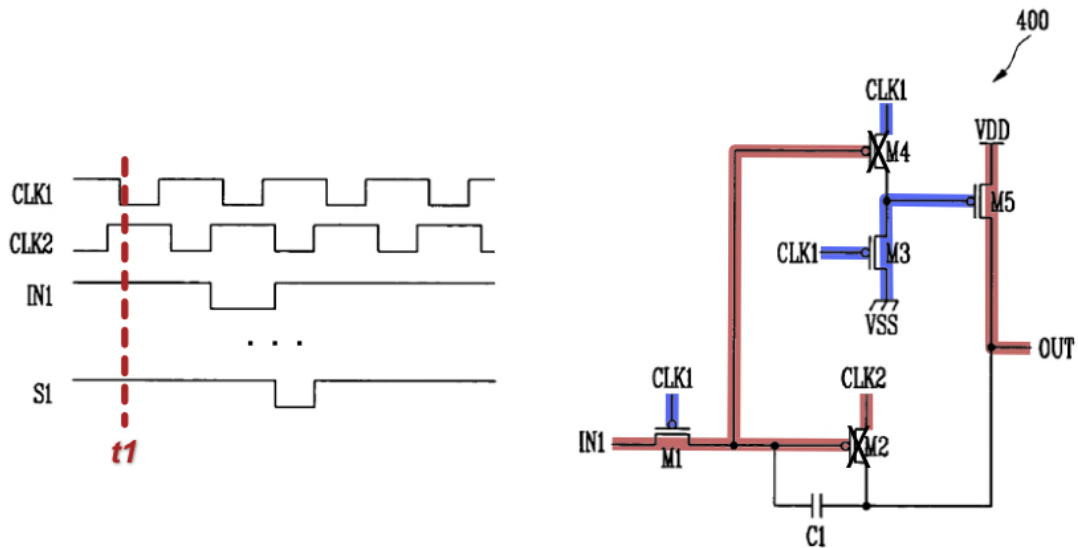
circuit identified by the Petition is not “theoretical.” Instead, it was a known shift register operational issue.

Next, a POSITA would have readily understood that Shin’s capacitor C1 does not “obviate” the reversal problem. Patent Owner misunderstands key differences between the periods of Shin’s operation. According to Shin, capacitor C1 operates to keep transistor M2 “turned-on” during what Shin calls its “evaluation period” so that a low-level CLK2 signal can be output. Shin, [0098]-[0105]. But as shown below, during this period transistor M5 is also closed preventing a high-level VDD signal from reaching the output. This redundancy minimizes the risk of the output of a conflicting signal:

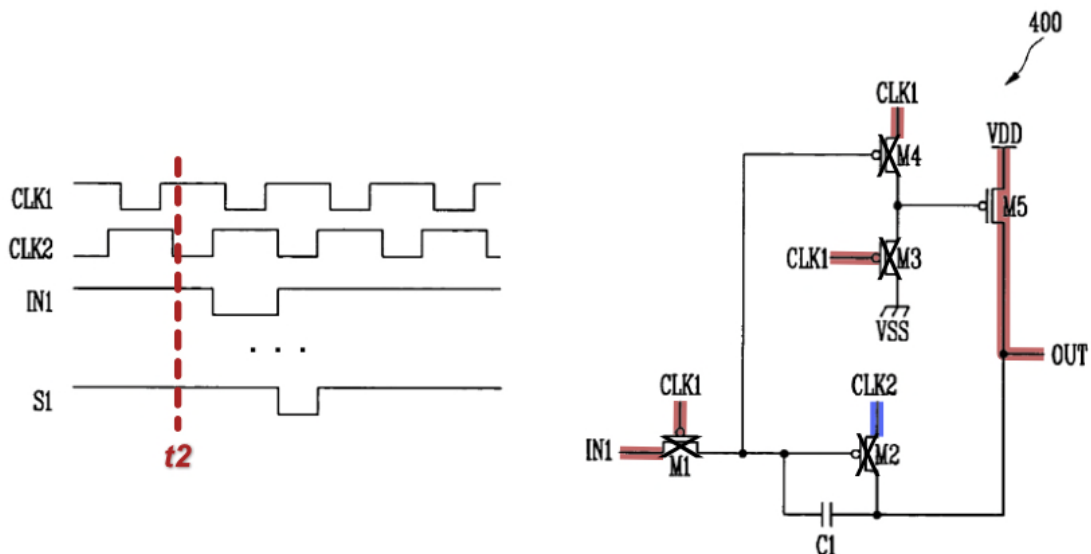


Shin, Figs. 11, 12; [0100]-[0105]; see also Foty Reply, ¶ 82.

Capacitor C1, however, fails to adequately protect against reversal in other periods of operation. For instance, during period of operation $t1$ below, CLK1 is low, CLK2 is high, and IN1 is high. This results in the supply of a high-level signal from VDD to the output terminal:



Ex. 1003, ¶ 382. Then, in the immediately following period $t2$, CLK1 shifts to high and CLK2 shifts to low. The circuit is still meant to output a high-level signal:



Id., ¶ 383. For this to occur, transistor M2 must remain closed. Otherwise, a low CLK2 signal will reach the circuit’s output. But transistor M2’s gate is floating. And capacitor C1 is now the only circuit element preventing reversal and the output of conflicting signals. It is unable to reliably do so because its stored charge—and ability to prevent reversal—can (and will) be overwhelmed by conditions routinely encountered by stage circuits, including interference and crosstalk. *See* Foty Reply, ¶¶ 76-81, 83-87. And once again, unlike in the different periods of operation discussed above (where other transistors provide redundancy), here nothing will prevent output of conflicting signals if the capacitor is overwhelmed. This is why a POSITA would have recognized Sasaki’s anti-reversal circuit to be necessary. *See id.*, ¶¶ 80-82. Patent Owner and its expert ignore this. They focus only on the different periods during Shin’s operation where reversal is less of a concern. *See* Response, 33-34; Ex. 2059, ¶¶ 90-92.

Patent Owner next repeats its argument that “adding elements to a circuit may increase complexity, decrease stability, and lower process yields.” Response, 34. Again, circuit size is only one factor a POSITA would consider. *See supra* p. 14. Proper circuit functionality—which is achieved here by the application is Sasaki’s teachings—is also of importance. *See* Foty Reply, ¶¶ 96-97; *see also id.*, ¶¶ 88-95. Moreover, according to the ’593 patent, known “conventional stage circuits” often included “at least ten transistors.” Ex. 1001, 9:15-16. The combined circuit of Shin

and Sasaki employs less: only seven transistors and one capacitor. Thus, even if increased circuit size were for some reason a determinative factor (it is not), a POSITA would have considered Shin and Sasaki's small-sized circuit to be more than adequate.

Next, Patent Owner is wrong when it argues that the Petition applied Sasaki in a way "inconsistent[]" with its teachings. According to Patent Owner, the only possible way to apply Sasaki's anti-reversal circuit would be to attach it to Shin's output transistor M5. Response, 35-36. There is no such limitation in Sasaki. While Sasaki does provide an example that is structured this way, it more generally teaches that anti-reversal circuits are useful to ensure proper operation of any output transistor. *See, e.g.*, Sasaki, [0042]. Patent Owner ignores this and instead would improperly require that Sasaki be bodily grafted into Shin. *In re Kahn*, 441 F.3d. 977, 990 (Fed. Cir. 2006) (no need to "bodily incorporate" teachings).

B. Jeong's Teachings Are Also Applicable

Ground 3 explained why claims 7 and 21 would have been obvious when Jeong's capacitor teachings are applied to Shin and Sasaki. Petition, 75-78. According to Patent Owner, there is "nothing in Shin or Sasaki" that "suggests any operational issue ... that would motivate adding a capacitor." Response, 39. This is not the case. The Petition explained that Shin's circuit leaves the gate of transistor M5 floating at certain points. *See* Petition at 76-77. Petitioner's expert Dr. Foty

explained why—absent a capacitor—this is a problem. *See, e.g.*, Ex. 1003, ¶¶ 581-583. Moreover, Jeong confirms that addition of a capacitor reduces voltage variation and improves operation stability. *See* Jeong, [0056]. Patent Owner offers nothing beyond a conclusory denial in response.

Next, Patent Owner wrongly argues that “Petitioner’s arguments regarding Shin’s inclusion of capacitor[s]” are “inconsistent with its arguments that capacitor C1 is insufficient for its intended purpose.” Response, 39. There is no inconsistency. Patent Owner does not account for the purpose of capacitor C1 in Shin. Again, this capacitor is “precharged” and then discharged to provide redundancy and keep transistor M2 open. *See supra* Section II. New capacitor C2 serves the very same purpose for a different transistor (M5). *See* Petition, 75-78. Neither capacitor is sufficient to keep its associated transistor closed. This functionality is performed by other circuitry (Sasaki’s anti-reversal circuit in the case of transistor M2, and a high-level CLK1 signal passing through transistor M4 in the case of transistor M5). *See generally* Foty Reply, ¶¶ 85-87.

III. GROUNDS 4-5: OBVIOUSNESS OVER TOBITA

A. Tobita Itself Renders Many Claims Obvious

The Petition also explained why Tobita renders many of the ’593 patent’s claims obvious. *See* Petition, 80-98. None of Patent Owner’s responses have merit.

Patent Owner begins by arguing that transistors Q19-Q21 cannot be considered part of the claimed “first driver” because they purportedly only operate to “determine the voltage of node N6, not node N1 (the identified second node).” Response at 44. But the voltage of node N6 *indirectly* controls node N1’s voltage. See Petition, 84-85 (transistors Q18-Q21 control supply of a “low level” signal to N1). As the Board explained when instituting, “controlling the voltage of the second node does not require the voltage of the second node to be determined by the first driver alone.” See Institution Decision (Paper 12), 12-13. Indeed, Patent Owner itself appears to take this very position when addressing secondary considerations. There it identifies a collection of transistors (T1, T2, and T3) in its own product as the claimed “first driver” even though these transistors only control the potential of the “second node” (the gate of transistor T5) through another transistor (T8). See Response, 64; *see also* Foty Reply, ¶¶ 98-105.

Patent Owner next argues that in Tobita, “the identified ‘first driver’ does not control the voltage of the second node in accordance with the signal of the third input terminal” because transistors Q19-Q21 supposedly only operate to “turn[] off” transistor Q18. Response at 45-47. This is nonsense. When transistor Q18 is off, no low-level VSS signal is supplied to node N1. This allows the other transistors of the “first driver”—Q3, Q4, and Q5—to provide a high-level signal. See Petition, 84; *see also* Tobita, Fig. 9.

Patent Owner’s next argument is no better. According to Patent Owner, Petitioner’s application of the Tobita to the claims must be in error because Dr. Foty “testified ... that ... turning transistor Q21 on would purportedly control not only node N6 and N1 ... but ... also ... the ... output terminal.” Response at 48. Every transistor in Tobita’s circuit—like any stage circuit—plays a role in the generated output. This is all Dr. Foty stated at his deposition. *See* Ex. 2060, 70:6-72:5.

B. Tobita and Jeong Render Claims 7 and 21 Obvious

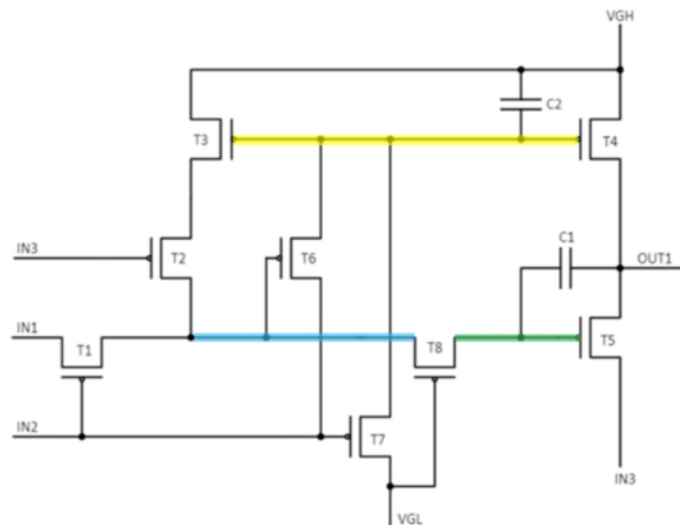
Here—much as it did when assessing the combination of Shin, Sasaki, and Jeong—Patent Owner fails to address the prior art’s teachings. Petitioner’s expert Dr. Foty explained—and Patent Owner does not dispute—that Tobita’s node N2 is electrically isolated during certain operational periods. Ex. 1003, ¶¶ 708-713. This leaves it vulnerable to interference. *See* Jeong, [0057]. Thus, it is Patent Owner’s arguments—not Petitioner’s—that are conclusory and lack evidentiary support.

**IV. PATENT OWNER’S SECONDARY CONSIDERATIONS
ARGUMENTS ARE INAPPOSITE**

Patent Owner concludes by arguing that there is supposedly “real-world objective evidence of non-obviousness.” Response, 50. There is not. Patent Owner points to the Samsung Galaxy S4 and S22 Ultra to show the required nexus. Response, 60. But it also pointed to these same products when making similar arguments for completely different patents. *See, e.g.*, IPR2023-00987, Paper 19 at 58-72 (discussing pixel arrangements patents). Patents that “do not cover the same

invention” do not presumptively have a nexus with the same product. *See Fox Factory, Inc. v. SRAM, LLC*, 944 F.3d 1366, 1377-783 (Fed. Cir. 2019).

Next, Patent Owner contradicts itself when trying to show that its products satisfy the claims. According to Patent Owner, transistors T1, T2, and T3 in the below circuit constitute the claimed “first driver.” Response, 64. But it then ambiguously identifies **both** the blue and green circuit paths as the claimed “second node”:



Id. If the green path is the claimed “second node,” then Patent Owner has contradicted its Tobita arguments (transistors T1-T3 control the green path’s voltage only ***indirectly*** through transistor T8). If the blue path is the claimed “second node,” then Patent Owner creates yet another contraction: the “output terminal” signal is no longer supplied “according to the voltage applied to the second node.” Instead, the second node voltage only indirectly impacts the output (transistor T8 exercises direct

control). See Foty Reply, ¶¶ 98-105. Patent Owner does not identify which theory it is pursuing, let alone explain the discrepancies between these theories and the other arguments it makes.

Finally, Patent Owner argues that the '593 patent solved a “significant and growing need for AMOLED displays suitable for mobile devices” with smaller “bezel[s].” Response, 50. The claims do not require AMOLED displays, mobile devices, or smaller bezels. *E.g.*, Ex. 1026, 9:16-12:25 (Patent Owner’s expert admitting that AMOLEDs and mobile devices not required under “plain meaning construction”). Nor is any of this is mentioned anywhere in the '593 patent. See *WBIP, LLC v. Kohler Co.*, 829 F.3d 1317, 1329 (Fed. Cir. 2016) (secondary considerations cannot be rooted in “extraneous factors”); *see also* Ex. 1026, 12:13-12:25 (no mention of bezel size or active matrix displays in specification). Moreover, any such need was also met by prior art. For instance, Shin teaches a shift register for an OLED display that employs fewer transistors (and thus occupies less space) and fewer input signals than the '593 patent. And contradicting its argument that there was some sort of importance to using fewer transistors in a scan driver, Patent Owner itself filed patents referencing drivers that employed more than 20 transistors years after the '593 patent was filed. See, *e.g.*, Ex. 1027, Fig. 4; Ex. 1028, Fig. 4. Patent Owner’s copying arguments also fall short. All that it has done is point to superficial similarity between its product and that of others. See *Liqwd*,

Inc. v. L'Oreal USA, Inc., 941 F.3d 1133, 1137 (Fed. Cir. 2019) (“[M]ore is needed than merely showing ... similarity....”)

Respectfully submitted,

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Dated: March 6, 2025

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing reply complies with the type volume limitation in 37 C.F.R. § 42.24. According to the utilized word-processing system's word count, the reply—excluding the portions referenced by § 42.24—contains 5,592 words.

Dated: March 6, 2025

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CERTIFICATE OF SERVICE

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