

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

MIANYANG BOE OPTOELECTRONICS TECHNOLOGY CO., LTD.; TCL
CHINA STAR OPTOELECTRONICS TECHNOLOGY CO., LTD.; TIANMA
MICROELECTRONICS CO. LTD.; AND VISIONOX TECHNOLOGY, INC.,

Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.,

Patent Owner.

Case No. IPR2024-00620
U.S. Patent No. 9,330,593

REPLY DECLARATION OF DR. DANIEL FOTY

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I. INTRODUCTION

1. I have been retained by Mianyang BOE Optoelectronics Technology Group Co., Ltd. et al. (“BOE” or “Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”). I am not an employee of BOE or any affiliate or subsidiary of BOE.

2. I have been asked to reply to the Patent Owner Response, as well as certain of the opinions set forth in the declaration of Andrew Wolfe, Ph.D – both of which were submitted by Patent Owner on December 12, 2024 in an *inter partes* review proceeding relating to U.S. Patent No. 9,330,593 (which I refer to herein as “the ’593 patent”). Thus, I submit this declaration to the Board in support of the Reply filed by Petitioner.

3. I am being compensated at my current standard consulting rate, plus reimbursement for any reasonable expenses. My compensation is based solely on the amount of time that I devote to activity related to this case – and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

4. The prior declaration I submitted in connection with this proceeding, which I understand has been designated as Ex. 1003, sets forth (among other topics) my educational background and professional experience (Ex. 1003, ¶¶ 4-5 and

associated Appendix A), my understanding of the law (*id.*, ¶¶ 10-28), an overview of pertinent technical background information (*id.*, ¶¶ 32-80), an overview of the '593 patent and its prosecution history (*id.*, ¶¶ 81-97), the knowledge and characteristics of a person having ordinary skill in the art (*id.*, ¶ 29), and certain claim construction opinions (*id.*, ¶¶ 98-100).

5. In reaching my conclusions and forming my opinions as set forth in this declaration, I have considered and relied upon my education, knowledge of the relevant field, knowledge of scientific and engineering principles, my work with those of ordinary skill at the time of the alleged invention, and my general experience in the field of art.

6. I have also reviewed and considered the materials listed in my prior declaration (*id.*, ¶ 7), the Board's Institution Decision (Paper 12), Patent Owner's Response (Paper 23), the Wolfe declaration (Ex. 2059), and the following materials to the extent relevant to my opinions:

Exhibit	Description
2049	Mengor Product Claim Chart
2060	Transcript of the December 5, 2024 Deposition of Dr. Daniel Foty

7. The version of the Wolfe declaration that I reviewed included redactions. While I understand that a confidential, non-redacted version of this declaration was also filed, the redacted version included all the information I

required to be able to assess and respond to the arguments made by Dr. Wolfe and Patent Owner.

II. SCOPE

8. As noted above, I am submitting this declaration in support of the Reply filed by Petitioner; as the length of the Reply is constrained by the procedures of the PTAB, this declaration will similarly be constrained in scope.

9. Due to those constraints, in this declaration I address only a fraction of the assertions made by Patent Owner in the POR, and only a fraction of the opinions that Dr. Wolfe has set forth in his declaration. The fact that I do not respond to particular assertions made by Patent Owner or particular opinions expressed by Dr. Wolfe should not be considered as in any way to indicate agreement with those assertions and/or opinions.

10. I will address certain of these assertions (POR) and opinions (declaration) during the course of this declaration. However, as both the POR and Dr. Wolfe's declaration grossly mischaracterized (in a variety of ways) my earlier declaration and my deposition testimony, at the end of this declaration I will provide an overview summary of some of the more-notable instances of these mischaracterizations.

III. BOOTSTRAPPING

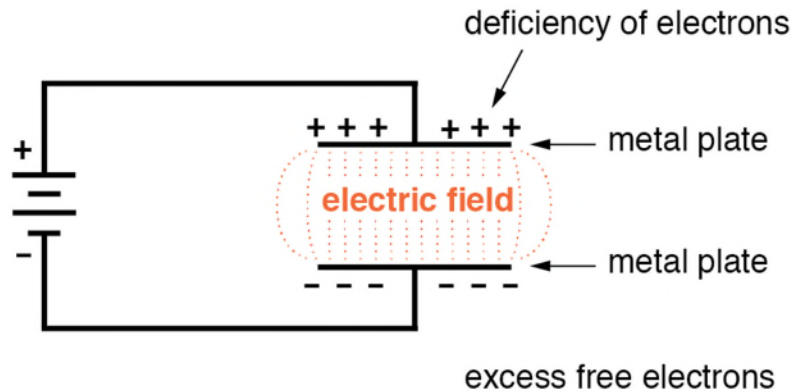
11. What is known as “bootstrapping” is a concept which appears in many of the references that have been cited in this IPR (including, as discussed below in Section IV.A, the Kimura reference); however, none of these references provide a detailed description of what bootstrapping actually is – or of how it behaves; this is because bootstrapping is very well known in the art of electronic circuits – and as it would readily have been known to a POSITA, the authors of the various references saw no need to provide a detailed discussion of the topic.

12. However, to aid in the understanding of the use of bootstrapping in the various references that appear in this matter, a brief overview will be provided here.

13. Bootstrapping is something that is a result of capacitive coupling between various elements in a circuit. As will become clear from the discussion to follow here, bootstrapping can be either a happenstance or something that is designed into the circuit (and its functionality) by intent; however, under either situation, the basic physics remain the same.

14. A capacitor is a rather simple electronic device – consisting (at its simplest) of two metal plates (or a similar structure) that are separated from each other (i.e., not in contact)¹:

¹ <https://www.allaboutcircuits.com/uploads/thumbnails/deficiency-of-electrons-answer.png> .



As this simple figure shows, a capacitor has two terminals – one for each plate of the structure. As the figure further shows, the capacitor blocks the DC transfer of charge from one plate to the other across the gap. Instead, by applying a DC voltage to one plate, charge (either positive or negative – depending on the polarity of the applied voltage) is forced onto one of the plates; as DC voltage is similar to pressure in plumbing, the amount of charge that is forced onto the plate will be a function of the DC voltage – much as water can be forced into an empty pipe until the pressure in that section of pipe is the same as the upstream pressure that is forcing water into that pipe.

15. However, unlike what happens in plumbing, the charge that has been forced onto the first plate will attract charge of the opposite polarity onto the opposing plate – creating what is known as an “image charge” on that opposite plate;

this name is used because the image charge will be of the same magnitude but opposite polarity of the charge that was forced onto the first plate.²

16. As the figure above also shows, with charge layers of opposing polarity on the two plates, there will be an electric field between these charges – across the gap between the plates that defines the basic capacitor structure. The storage of charge and the creation of an electric field in the capacitor are the basic functions inherent in any capacitor.

17. At its most basic, the gap between the two plates of the capacitor is occupied by air – which is literally a natural dielectric material. However, when used in electronic circuitry, the gap between the two plates is usually filled with an insulating material that is often referred to as being a “dielectric material.” A dielectric material is usually included for many reasons – such as providing separation between the plates that is more robust than air, to increase the capacitance of the capacitor (vs. what that value would be with air as the dielectric), and so forth; however, the use of a dielectric material (or the particular type of dielectric material used) does not alter the basic physics of a capacitor.

² For completeness (and as shown in the figure above), as metals have only negative charge (i.e., electrons) in them, when there are two metal plates in a capacitor and negative charge is forced onto the first plate, the (positive) image charge is created by forcing electrons (by repulsion) out of the metal of the opposite plate. Positive charge can be forced onto the first plate by a similar process – and it will attract negative charge into the opposite plate to create the image charge.

18. In more detail, the relationship between the voltage that is applied to one terminal of the capacitor (to force charge onto the associated plate) and the resulting amount of charge that will appear on the plate is well-described by the simple description

$$Q = CV,$$

where V is the voltage across the capacitor (see below), Q is the amount of charge induced, and C is the capacitance of the capacitor.

19. Further, as noted above, the charge and voltage serve to create an electric field between the capacitor plates. As the dielectric is an insulating material which possesses no free charge, the electric field between the plates is a simple function of the voltage across the plates and the distance between those plates:

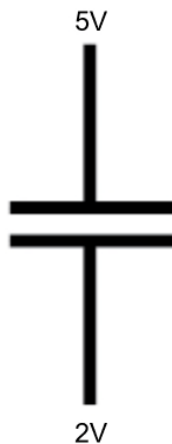
$$E = \frac{V}{d},$$

where d is the separation distance between the plates and E is the magnitude of the electric field that is induced.

20. As noted above, the amount of charge on the plates and the magnitude of the electric field induced between the plates depends on the voltage difference between the plates. When a DC voltage is specified as a single value, this commonly means that the voltage thus described (e.g., “10 volts”) refers to the voltage between that point (i.e., node) and ground (i.e., a reference voltage that is fixed at zero volts). However, when such a voltage description is used for the two terminals of a

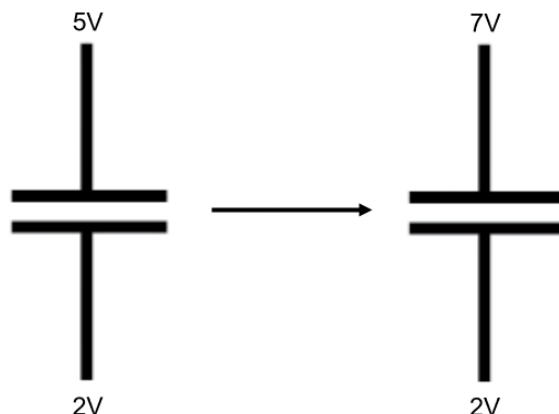
capacitor, it is the difference between them that defines the behavior of the capacitor as described above; if the top and bottom plates have voltages (separately referenced to ground) of (respectively) 5 volts and 2 volts, or 2 volts and -1 volts, or 10 volts and 7 volts, then in all of these cases the voltage difference between the two plates will be 3 volts – and in each instance, the behavior of the capacitor will be the same (reflecting that in each instance, there is a 3-volt difference between the plates).

21. Now, consider a capacitor that has 5 volts (referenced to ground) applied to one terminal (and corresponding plate) and 2 volts (referenced to ground) applied to the other terminal (and corresponding plate).



Both terminals are connected to fixed voltage references – and there will be a 3-volt difference between the capacitor plates; this is enough to describe the static behavior of the capacitor, as per the discussion (and the two equations) presented above.

22. Next, let the voltage on the first plate be changed with time – going from 5 volts to 7 volts.

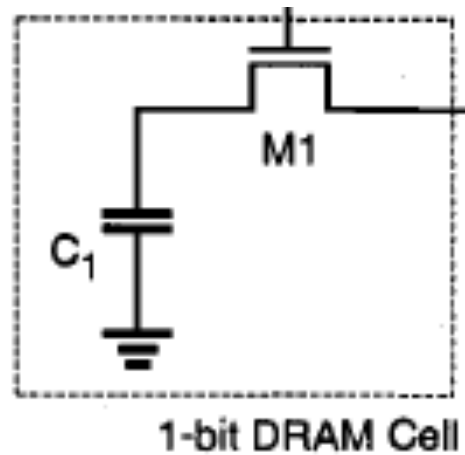


As both capacitor terminals are connected to fixed voltage references throughout, at the end point of the change³ there will be a 5-volt difference between the capacitor plates – and the discussion (and the equations) provided earlier is applicable here under the new state.

23. However, different things happen when one of the terminals of the capacitor is “floating” – wherein “floating” means that (at least) one capacitor terminal is *not* connected to a fixed voltage reference. While one capacitor terminal could literally be not connected to anything, a more-common instance of a “floating

³ For completeness, it should be noted that the change of the charge on the plates (and of the electric field between them) is treated as being an instantaneous function of the voltage difference at any given time as the voltage difference changes; this is known as the “quasi-static approximation” (or assumption), and it is generally a reasonable assumption in electronic circuits. However, even if the particular capacitor characteristics and/or the rate-of-change render the quasi-static approximation inappropriate, the end point of the change will be static – and the capacitor will eventually catch up to that final state.

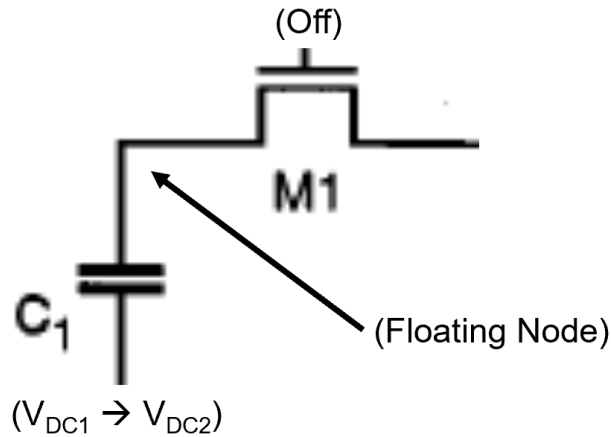
capacitor terminal” occurs when one terminal is connected to a field-effect transistor that is turned off – for example⁴,



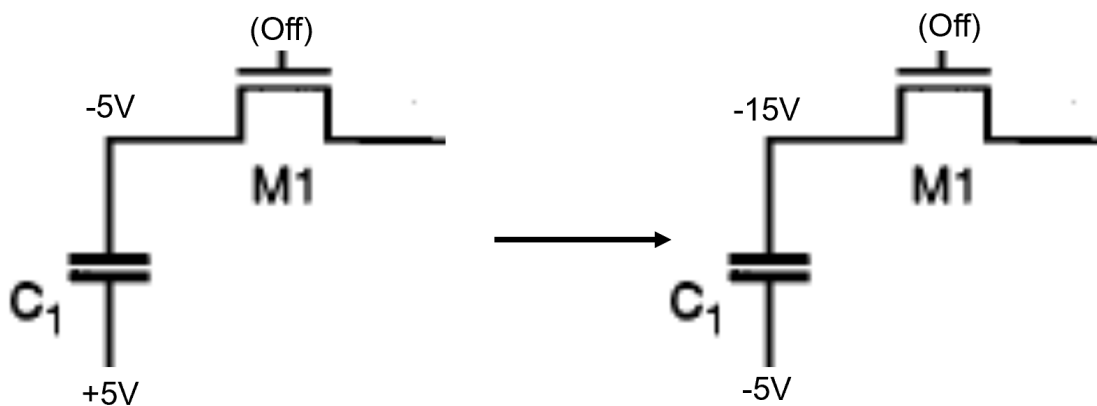
The lower terminal of the capacitor is connected to a fixed voltage (here, ground), while the upper terminal of the capacitor is connected to transistor M1; as per what was just described, when the transistor M1 is turned off, the node between the upper terminal of capacitor C1 and transistor M1 is floating – because, in that state, that node is not connected to any fixed voltage. (As the figure above also indicates, this is the basic structure that is used to store one bit of information (as charge) in one cell of a DRAM memory; similarities between DRAM cells and some of the circuitry that appears in this IPR will be considered at several points later in this declaration.)

24. Now consider what happens when one terminal of the capacitor is floating, while the fixed voltage on the other terminal is changed with time:

⁴ Taken from <https://www.ques10.com/p/39305/explain-dram-operation-1/>.



Because the floating terminal is (by definition) not connected to a fixed voltage, the voltage at that terminal is not forced to retain its initial voltage; rather, as the voltage on the fixed terminal changes, the capacitor will instead react so as to maintain (at a constant value) the magnitude of the electric field between the two plates of the capacitor – which is of course done by maintaining the voltage difference between the two plates of the capacitor. Thus, in this situation, the voltage (with respect to ground) on the floating terminal will change to the same degree as does the voltage on the other terminal of the capacitor (which is connected to a particular voltage value):

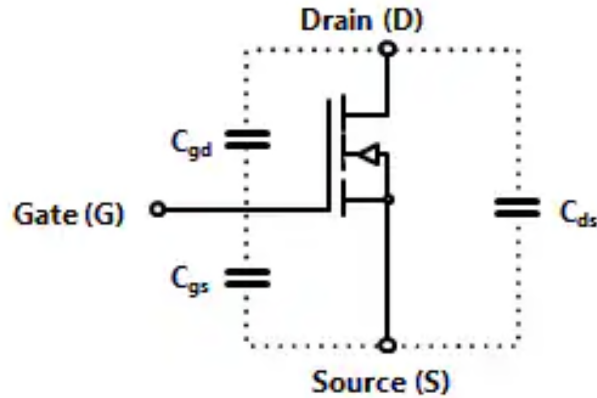


As this figure shows by example, if in the initial condition the voltage on the fixed voltage terminal is +5V and the voltage on the floating terminal is -5V, and then the voltage on the fixed voltage terminal is changed from +5V to -5V, the voltage on the floating terminal will change from -5V to -15V.

25. The terminology used to describe the change in the floating node voltage (as just described, from -5V to -15V) is what is known as “bootstrapping”; as described above, bootstrapping occurs due to the basic physics under which the capacitor maintains the electric field between the plates (and thus the voltage between the plates) at a constant value when the voltage on the non-floating terminal is changed.

26. Finally, it should be noted that while bootstrapping is associated with capacitors, it will also occur when a larger-scale electronic device has inherent capacitors in its basic structure. For example, as is well-known in the art, a field-effect transistor (such as a silicon MOS transistor or a thin-film transistor) has inherent capacitors – such as those between the gate-source and the gate-drain⁵:

⁵ Taken from https://toshiba.semicon-storage.com/content/dam/toshiba-ss-v3/master/en/semiconductor/knowledge/e-learning/discrete/chap3-25-1_en.png .



Because of this, bootstrapping can occur between the nodes of a field-effect transistor; for example, if the node connected to the gate is floating and (e.g.) the node connected to the drain is not floating, when the voltage on the drain node is changed, the voltage on the gate node will be bootstrapped in response (in the way that was already described above for a simple capacitor).

IV. OBVIOUSNESS OVER KIMURA

27. There are three fundamental errors with both Patent Owner's and Dr. Wolfe's analysis of the Kimura reference. First, both Patent Owner and Dr. Wolfe fail to understand that all of Kimura's circuit embodiments are interrelated – and that they build off of each other. Second, both Patent Owner and Dr. Wolfe fail to grasp both the importance and the interrelationships among Kimura's timing diagrams. And third, both Patent Owner and Dr. Wolfe grossly mischaracterize both my earlier declaration and (in particular) my deposition testimony on these issues.

A. Kimura's Circuits Are Interrelated

28. Both Patent Owner and Dr. Wolfe do not understand that the various circuit embodiments disclosed by Kimura are interrelated; for example, according to Dr. Wolfe, “neither Dr. Foty or [sic] the Petition provide a reason why a POSITA would look through the disclosures of Kimura relating to other circuits and embodiments in order to understand the operation of the Figure 27C circuit.” Ex. 2059, ¶ 50.

29. However, this is simply incorrect – as examination of Kimura clearly indicates. As I explained in my prior declaration, a POSITA would understand that the circuit of Figure 27C “***builds on and shares components with*** the devices of [Kimura's] other figures.” Ex. 1003, ¶ 146.

30. Simply put, Kimura states this expressly. *See, e.g.*, Kimura, [0093] (later figures include the “same portions or portions having similar functions” as earlier figures); *see also id.*, [0218], [0245], [0249], [0260], [0264], [0270], [0276], [0284] (repeatedly explaining that later circuits add to earlier circuits).

31. Before I provide a more-detailed explanation of how the various embodiments discussed in Kimura are both interrelated and often proceed from one embodiment to further subsidiary embodiments, I will note here that a flow chart (included following these explanatory paragraphs) below exemplifies the interrelationship among Kimura's figures and circuits.

32. Figure 1A is the starting point and shows five transistors 101-105 (**red**) that produce an output in response to input signals. *Id.*, [0099]. The same five transistors appear in all the circuits that follow - including Figure 27C. *Compare id.*, Figs. 1A, 27C.

33. Kimura then teaches how the addition of transistors improves operation – and each transistor present in Figure 27C is discussed.

34. Figure 14A shows the addition of transistor 201 (**light green**). *Id.*, [0218]-[0219]; this transistor is intended to “reduc[e]” transistor “on” time to “suppress[]” “deterioration.” *Id.*, [0228].

35. Figure 16A shows the addition of transistor 202 (**dark green**). *Id.*, [0245]-[0246]; this transistor is intended to reduce noise on wiring 211—the circuit’s output—to improve “display quality.” *Id.*, [0247].

36. Figure 17A shows the addition of transistor 203 (**light blue**). *Id.*, [0249]; this transistor outputs a high signal at the appropriate time. *See id.*, [0249].

37. Figure 20A shows the addition of transistor 204 (**dark blue**). *Id.*, [0260]-[0261]. This transistor is intended to allow the “potential of ... node 13” to be “lowered” for the purpose of reducing the risk of transistor deterioration. *Id.*, [0262]. Note in particular (as will further be explained below) that the potential (i.e. the voltage) at node 13 will differ across the circuit embodiments – as the voltage at

node 13 is *not* an input signal to circuitry, but rather is a consequence when the same input signals are applied to the different circuitries of the different embodiments.

38. Figure 21A shows the addition of transistor 205 (**orange**). *Id.*, [0264]-[0265]; This transistor is intended to facilitate provision of a “start pulse” signal to the circuit. *Id.*, [0266]-[0267].

39. Figure 23A shows the addition of transistor 206 (**yellow**). *Id.*, [0270]-[0272]; this transistor provides a more “noise-resistant semiconductor device” by “fix[ing]” the potential of node 13 in period B. *Id.*, [0274].

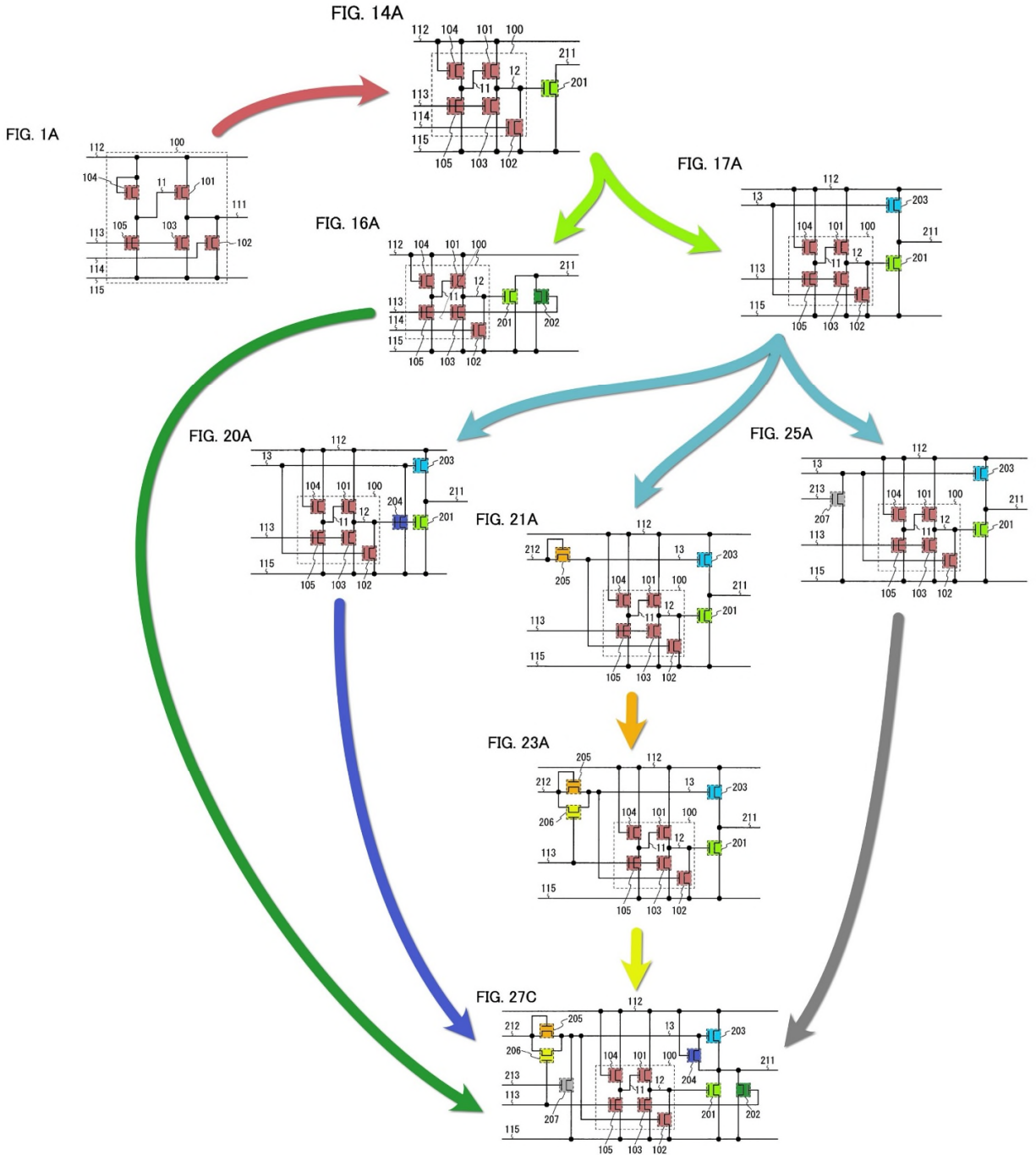
40. Finally, Figure 25A shows the addition of transistor 207 (**grey**). *Id.*, [0277]-[0280]; this transistor allows for provision of a “reset signal” that further lowers node 13’s potential in period E. *Id.*, [0280]-[0281].

41. Figure 27A then combines all of transistors 101-105 and 201-207 in a single circuit embodiment. *Id.*, [0283]. Given that the transistors have the same numbers—and are incorporated into the circuit of Figure 27A in the same way in which they were incorporated into the circuits shown in the figures discussed above—a POSITA would have readily understood that the same transistors will operate in the same way, and perform the same functionalities across the various embodiments (discussed sequentially in Kimura, and explained in the preceding paragraphs).

42. Figure 27C then simply relocates transistor 204 to avoid “dielectric breakdown” of “the transistor connected to node 13[.]” *Id.*, [0286]. Dielectric breakdown⁶ has long been well-known in the field-effect transistor (FET) art, and would thus have been well-known to a POSITA; dielectric breakdown can (and will) occur when an excessively-large voltage is applied to the gate electrode of a field-effect transistor. When such an excessive-voltage is applied to the gate electrode, the dielectric will simply fail as a material – resulting in permanent damage to the dielectric; this generally either ruins the operating characteristics of the transistor, or simply renders the transistor non-functional.

43. As noted above, this verbal description of the sequential evolution of Kimura’s embodiments can also be described via a visual flow chart of the various embodiments – which clearly shows their interrelationship; this is depicted in the figure presented below. As is readily-apparent from this visual depiction, Figure 27C is not a standalone embodiment; rather, the Figure 27C embodiment plainly results from the accumulation and combination of transistors – as discussed in sequence by Kimura:

⁶ To provide context, a simple example of dielectric breakdown in the natural world is lightning – which occurs when excessive voltages associated with convective clouds cause the air (which acts as a dielectric) to break down; when this occurs, current flows between the two (now shorted-together) voltage regions, until the voltage between them equalizes.



Id., Figs. 1A-27C. (Note that the “flow” in this depiction begins with the Figure 1A embodiment in the upper-left of the figure.)

44. Further, as I will explain in the following sub-section, I have already described this structural aspect of Kimura’s teachings (and the various circuit

embodiments of Kimura) in both my earlier declaration *and* in my deposition testimony; however, both Patent Owner and Dr. Wolfe ignored this testimony – and mischaracterized it in order to state that my testimony was the ***exact opposite*** of what it actually was.

45. Thus, it is my conclusion and opinion that both Patent Owner and Dr. Wolfe are factually-incorrect when they argue that Kimura’s circuit embodiments are “different” unrelated embodiments that must be read in isolation. Rather, as per the discussion above (reprising both my earlier declaration and my deposition testimony), Kimura’s circuit embodiments are ***related, additive, and meant to be used together***; this is also something that (as explained above) Kimura itself makes explicitly clear.

B. A POSITA Would Readily Understand What Signals Are Input to the Circuit of Figure 27C

46. Both Patent Owner and Dr. Wolfe also take the position that it was somehow improper to use the timing diagram provided by Kimura in Figure 21B for the circuit embodiment of Figure 27C; for example, as per Dr. Wolfe’s declaration, it is somehow improper and incorrect for “Dr. Foty and the Petition” to “point to the timings provided in Figure 21B” when discussing how the circuit shown in Kimura’s Figure 27C would operate. Ex. 2059, ¶¶ 51-52.

47. However, it is quite clear that both Patent Owner and Dr. Wolfe did not properly assess Kimura’s timing diagrams.

48. To begin, in my prior declaration I pointed to Figure 21B's timing diagram because it provides an example of the "*input signals*" IN1, IN2, and IN4 that are used to drive the circuits. Ex. 1003, ¶ 161.

49. Most importantly, unlike the internal node voltages—which will vary from circuit-embodiment-to-circuit-embodiment—the inputs are the *same* in all the circuit embodiments (in the sequence of figures in Kimura, as explained in the prior sub-section) from which Figure 27C is based. This can be seen below – wherein, as shown, the circuits of Figures 14A, 17A, 21A, and 25A are all supplied with the same input signals IN1 and IN2 (even though each of these circuits involves the sequential-inclusion of additional transistors):

[illegible]

Timing diagram for the 12-bit DAC output of the AD7124. The diagram shows digital signals for IN1, IN2, IN4, V11, V12, V13, and GOUT over 16 clock cycles. IN1, IN2, and IN4 are high for the first 12 cycles and low for the last 4. V11 and V12 are high for the first 12 cycles and low for the last 4. V13 is high for the first 12 cycles and low for the last 4. GOUT is high for the first 12 cycles and low for the last 4. The clock signal is shown at the bottom.

50. Therefore, as can be seen by inspection of the set of figures above, a POSITA would have understood that the Figure 27C circuit uses the same inputs as

do the embodiments of the circuits from which the Figure 27C embodiment descends; quite simply, this is because all of Kimura's other embodiments do this.

51. Further, the rest of Kimura confirms that a POSITA would have understood that the embodiment of Figure 27C receives the same input signals as do the circuits that are referenced elsewhere in Kimura.

52. In this regard, Kimura not only includes timing diagrams showing the input signals; Kimura also explains what these signals are – and how they are supplied.

53. IN1 and IN2 are both “clock signals” that are supplied “180° out of phase” from each other. *Id.*, [0108]-[0109]; *see also id.*, [0229]-[0231]. IN1 is high and IN2 is low in period A. *Id.*, [0226], the signals reverse (i.e., IN1 becomes low and IN2 becomes high) in period B, and reverse again in the next period - and so on and so forth, as the two signals repeat their behavior with the depicted regular periodicity. *See id.*, [0227].

54. Further, as Kimura explains, IN4 “can function as a start pulse.” *Id.*, [0266]. This signal is supplied such that it goes high in period C – which causes the circuit to output a high signal in period D. *Id.*, [0269].

55. These same inputs are meant for use with **all** of Kimura's circuits – and are consequently (and not-surprisingly) always supplied via the same input lines. *See, e.g., id.*, Figs. Figs. 1A-27C.

56. In an effort to show that Figure 21B is inapplicable to the circuit of Figure 27C, Patent Owner and Dr. Wolfe focus on the internal node potentials shown in Figure 21B.

57. Before addressing the technical details of what is actually happening in the circuit of the Figure 27C embodiment of Kimura, it must be noted that both Patent Owner and Dr. Wolfe have ignored what was stated in my earlier declaration – and, further, have mischaracterized my deposition testimony so as to describe that testimony as being the *exact opposite* of what it actually was.

58. For example, at p. 8 of its Response, Patent Owner asserts that “Dr. Foty conceded that Kimura provides no teaching to suggest combining these elements in the way Petitioner suggests, and that his opinions were based on an assumption.” (followed by a quotation in which my answer (to the question asked) was, to say the least, severely truncated). However, this is simply incorrect – as it not only mischaracterizes my actual testimony (which will be properly-quoted below), but completely ignores that testimony *and* then asserts (as per the quote from p. 8 of the POR above) the exact opposite of what that testimony was.

59. As I actually testified, the circuit of Figure 27C “is basically the same circuit” as those referenced previously in Kimura and “is intended to function in the same way other than that problem internally” with node 13 that Figure 27C is specifically intended to address. Ex. 2060, 30:18-31-3. I also pointed out that Figure

27C builds on earlier figures, including Figure 21A, and addresses a “bootstrapping” issue present in those figures’ circuits. *See id.*, 32:3-12. This is what I described in my earlier declaration – and is also what I further-described above. Further, I also explained that Figure 21B and Figure 27C would not require a change in “inputs” – because they both are “essentially the same circuit to be run in the same way I use the inputs.” The other voltages in Figure 21B are “results and so we actually modif[y] 27C to prevent what” Figure 21B shows “happening” to node 13 during period D. While there is no timing diagram showing this, this is what Kimura “verbally states.” Ex. 2060, 27:11-17.

60. Patent Owner’s mischaracterized rendition of my testimony should be rejected – because it is both factually incorrect *and* willfully misleading.

61. Dr. Wolfe (at Paragraph 52 of Ex. 2059) compounds the problem by attempting to state that the timing diagram of Figure 21B is inapplicable to the circuit embodiment of Figure 27C – because (in his view) the voltage of node 13 with time that is shown in the Figure 21B timing diagram would not occur with the circuit embodiment of Figure 27C. However, as per what was discussed in my earlier declaration, my actual deposition testimony (as quoted just above), and in the discussion presented earlier in this declaration, it is the *inputs* that are common across the different circuit embodiments – in contrast to the internal conditions and outputs of the different circuit embodiments. This is a very straightforward aspect

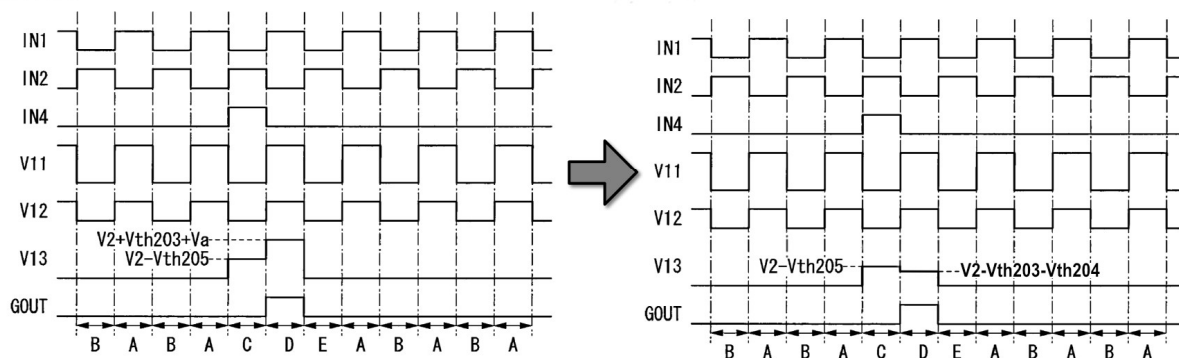
of circuit design – as a circuit is modified so as to (even under the same input signals) provide different operating conditions and/or different outputs than does the original, unmodified circuit.

62. As just described, Dr. Wolfe (again, at Paragraph 52) asserts that the voltage at node 13 that is shown in Figure 21B will not appear at node 13 in the Figure 27C circuit embodiment; however, this is the *entire point* of the modifications that Kimura makes in the sequential evolution of his circuit embodiments – in particular, as described in the preceding sub-section, in the Figure 27C embodiment transistor 204 is relocated for the purpose of preventing “dielectric breakdown” of “the transistor connected to node 13[.]” Kimura, [0286]. The entire point of this modification to the circuit embodiment of Figure 27C is to *alter the waveform of node 13 as it is depicted in Figure 21B*. The “extra” voltage that can be seen in the node 13 waveform in Figure 21B is the excessive voltage that can cause dielectric breakdown – and by making the aforementioned modification to Figure 27C, this excessive voltage is ameliorated (and the risk of dielectric breakdown essentially is eliminated).

63. Although Kimura does not provide a depiction of the resulting waveform for node 13 that would appear in the operation of the circuit embodiment of Figure 27C, a POSITA would have clearly understood what that waveform would

look like – as it would be the same waveform as is depicted in Figure 21B, with the only change being that the excessive voltage is eliminated:

FIG. 21B

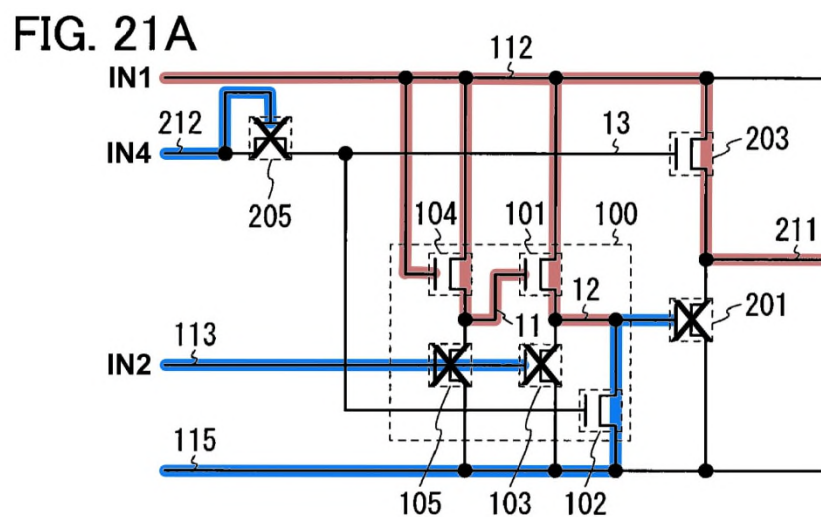


Kimura, Fig. 21B (modified on the right so as to apply to the circuit of Figure 27C). As per the earlier figure that graphically depicts the sequential evolution of Kimura's circuit embodiments, the same inputs are used – with the circuit embodiment of Figure 27C specifically modified to produce the (modified) behavior of the voltage (with time) at node 13.

64. Further, the fact that node values within the Figure 27C circuit, such as V13 (i.e., the voltage at node 13), are different from the Figure 21A (the circuit to which the timing diagram of Figure 21B relates) does not show that there is any sort of difference in the input signals that are used with (and are thus received by) the Figure 27C circuit embodiment; as explained generically above, a circuit can be modified for a particular purpose or purposes – and, in such a situation, it would be expected (as is the intent of doing the modifications in the first place) that the behavior of the circuit would be different under the same input signal conditions. In

particular here, the express purpose of the modification of the Figure 27C circuit is to address the problems that can arise (i.e., dielectric breakdown risk) from the elevated node 13 voltage that is shown in Figure 21B.

65. According to Kimura, in the Figure 21A circuit (which employs the signal timings shown in Figure 21B), a high-level “signal IN4” is supplied to wire 212 in period C. *Id.*, [0269]. This causes “transistor 205” to be “turned on” and the “potential of ... node 13” to rise to “ $V_2 - V_{th205}$.” *Id.* The increase in node 13’s potential (i.e., voltage) turns on transistor 203. *Id.*, Fig. 22A. Then, in period D, IN4 switches back to low – turning off transistor 205, and leaving “node 13” in a “floating state.” *Id.*, [0269]. At the same time, the IN1 signal supplied to wire 112 transitions to high, and passes through the still-turned-on transistor 203 (and thus to the output line 211). This operation is shown in the annotated version of Figure 21A below:



Id., Fig. 21A (annotated). As in my prior declaration, the red annotations are intended to represent a logical high signal, while the blue annotations are meant to represent a logical low signal.

66. Kimura explains that this scenario—*i.e.*, node 13 is floating while a high voltage is supplied through transistor 203—results in a “bootstrap⁷ operation”; this causes the potential of node 13 to further increase – to $V_2 + V_{th203} + V_a$. *Id.*, [0256].

67. To avoid the transistor “dielectric breakdown or deterioration,” the Figure 27C circuit “lower[s]” the “potential of the node 13” in period D – rather than allowing it to be increased via bootstrapping. *Id.*, [0286].

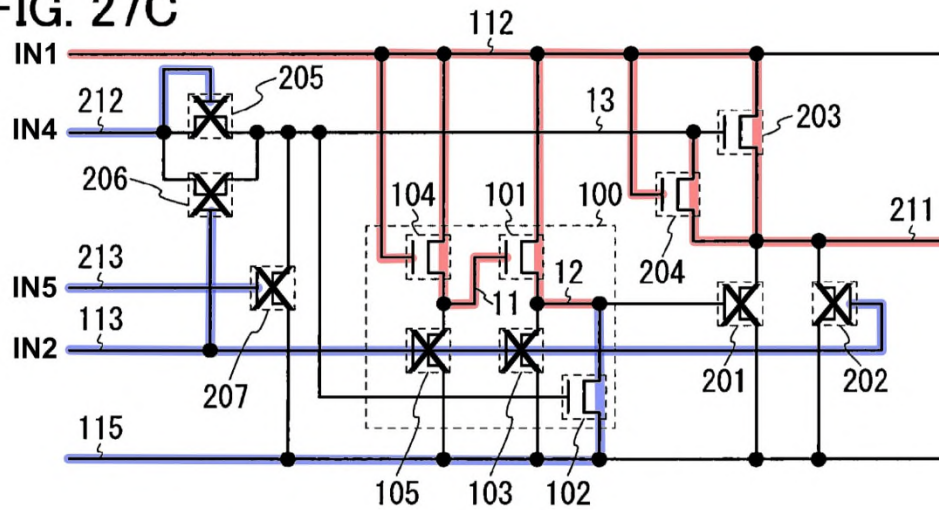
68. This is achieved by modifying earlier circuits (like that in Figure 21A) – by connecting transistor 203’s output to node 13 through transistor 204. *Id.*

69. Because the transistors are connected in this way, the high-level signal IN1 supplied to wiring 112 and through transistor 203 in period D is also supplied to node 13 via transistor 204. *See id.*, Fig. 27C.

70. This operation is shown in the annotated depiction of Figure 27C below. As shown there, rather than leaving node 13 floating, the output signal on wire 211 is also supplied to the node through transistor 204:

⁷ The nature of bootstrapping was explained earlier, in Section III.

FIG. 27C

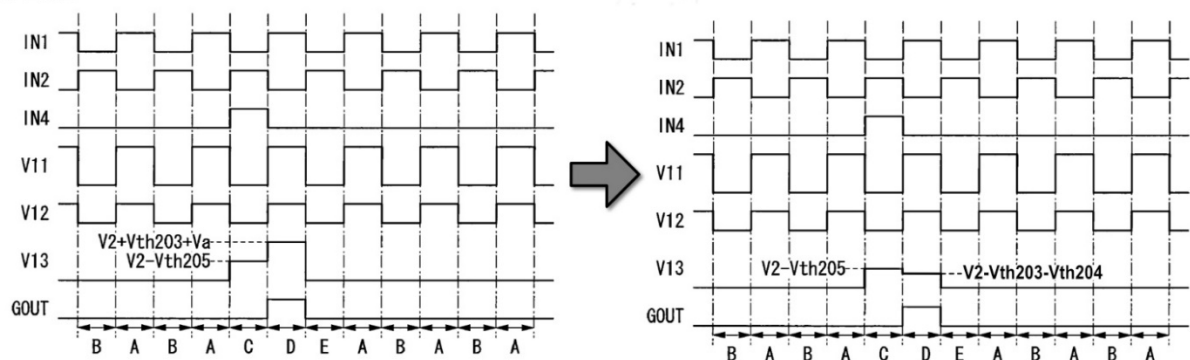


Id., Fig. 27C (annotated).

71. Because the output signal is passed to node 13, this fixes the node's voltage at a lower potential (i.e., voltage) – of approximately $V_2 - V_{th203} - V_{th204}$, showing prevention of the bootstrapping-induced voltage increase at node 13. This is shown in the (earlier-included) depiction below; the timing diagram of Figure 21B is on the left, while the comparable timing diagram that would occur with the circuit embodiment of Figure 27C (and which would be obvious to a POSITA) is on the right. As shown on the left, the potential of node 13 increases via bootstrapping in period D; however, the modifications made to the circuit embodiment of Figure 27C cause the bootstrapping-induced extra voltage on node 13 (during period D) to be eliminated – as was described above. Note that this modified timing diagram (on the right in the figure below) does nothing more than provide a visual depiction of what Kimura itself already expresses in words. The circuit of Figure 27C—like all

of Kimura's circuits—receives the same input signals as did the circuits from which the Figure 27C circuit embodiment descends. Indeed, because Kimura states that the circuit of Figure 27C is meant only to adjust circuit operation in period D (see Kimura, [0286]), the plain implication is that the circuit will operate in the same way(s) in all the other periods. The only difference is that in the Figure 27C embodiment, bootstrapping does not occur in period D – resulting in a lowered node 13 potential:

FIG. 21B



Kimura, Fig. 21B (modified on the right so as to apply to the circuit of Figure 27C).

72. In summary, there is nothing wrong with either my prior discussions of Kimura's timing diagrams or my prior discussions of the operation of Figure 27C – in either my earlier declaration, or in my deposition testimony.

73. Kimura itself already explains the difference between the operation of Figure 27C and what is shown in Figure 21B; Patent Owner and Dr. Wolfe simply fail to properly account for Kimura's teachings regarding the timing diagram of

Figure 21B (where node 13's potential is increased via bootstrapping) and the operation of Figure 27C (which is structured to avoid this extra voltage on node 13 during Period D).

V. OBVIOUSNESS OVER SHIN AND SASAKI

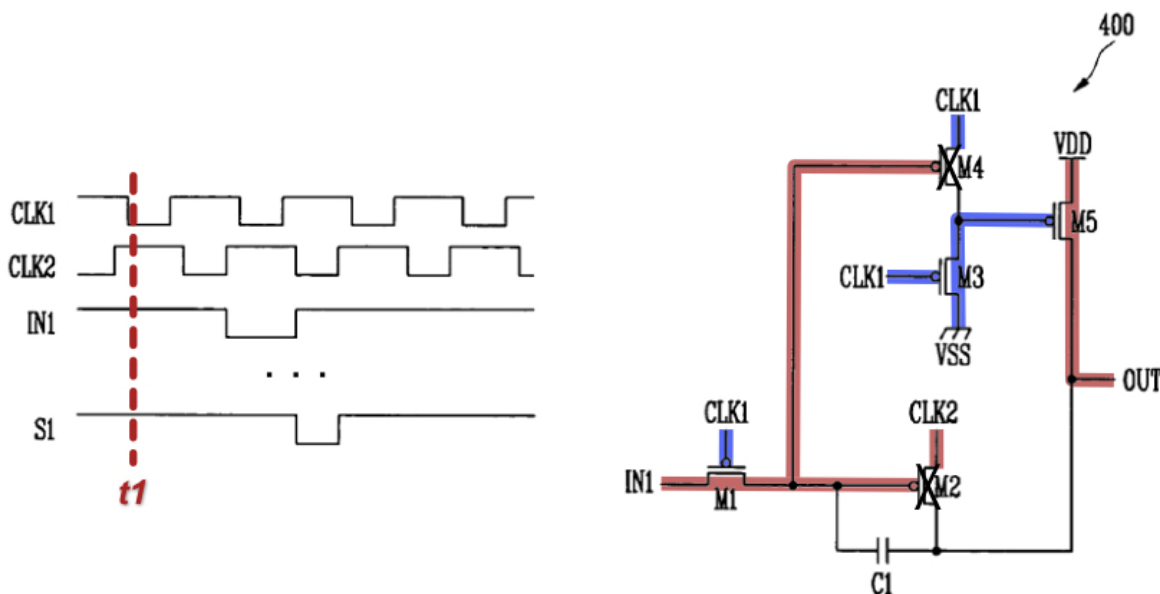
74. In my prior declaration, I explained why a POSITA would have considered it obvious to apply Sasaki's anti-reversal circuit to Shin. *See* Ex. 1003, ¶¶ 363-396.

75. Patent Owner and Dr. Wolfe respond to this by arguing that, in their view, Sasaki's anti-reversal circuit is not needed by Shin. This is because, again in their view, Shin "already contains a capacitor C1" that "addresses the floating state of the node at the gate of transistor M2...." Ex. 2059, ¶¶ 91-92.

76. In my earlier declaration, I explained why a POSITA would have considered this capacitor to be insufficient to the task of preventing the "reversal" (i.e., the unwanted turning-off of a turned-on transistor, or the unwanted turning-on of a turned-off transistor) of transistor M2. *See* Ex. 1003, ¶ 385. As neither Patent Owner nor Dr. Wolfe have presented anything which changes my conclusions and/or opinions on this issue, the paragraphs below reiterate my conclusions and opinions regarding the combination of Shin and Sasaki.

77. It remains my conclusion and opinion that a POSITA would have been motivated to combine Shin and Sasaki – for the reasons explained in my earlier declaration, as per the explanations provided in my earlier declaration.

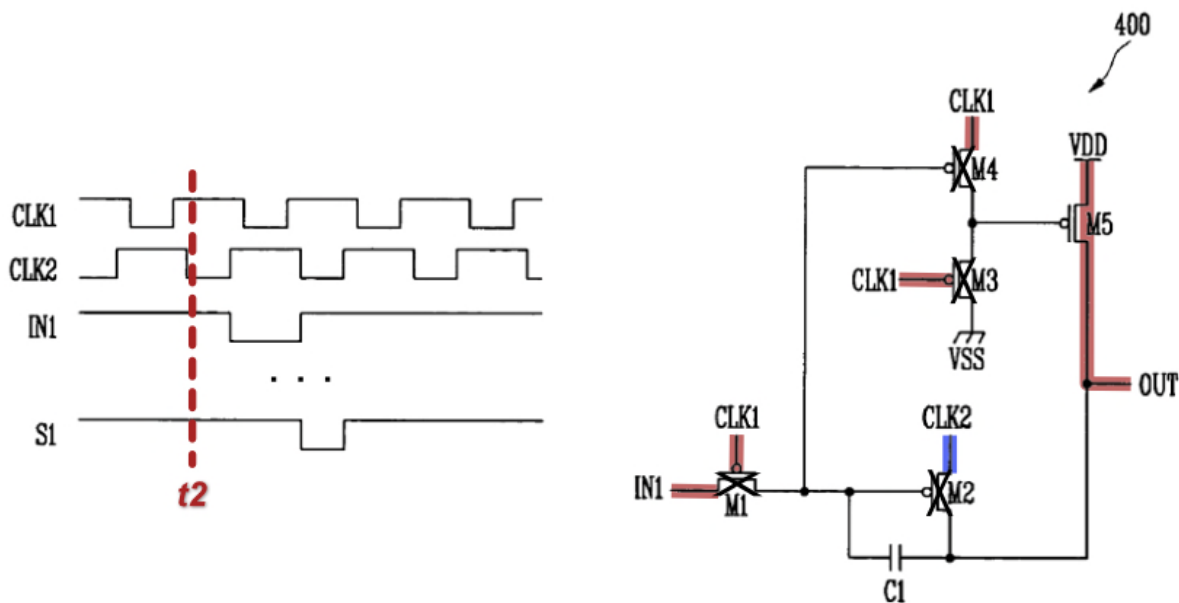
78. In my earlier declaration, I provided a figure which showed a particular point in time in the timing diagram of Figure 11 of Shin, and an annotated depiction of the states (high-logic-level or low-logic-level) of the nodes in the circuit of Figure 12 of Shin; that figure is reprised here:



At the time point $t1$, clock signal CLK1 is low – which turns on transistor M1 and transistor M3; as shown, the high input signal IN1 is passed through transistor M1 to the gate of transistor M2 – which turns off transistor M2, and thus prevents the clock signal CLK2 from being passed to the output node OUT; also, the low (VSS) fixed DC voltage is passed through transistor M3 to the gate of transistor M5 – which

turns on transistor M5, and thus provides the high (VDD) fixed voltage to be passed to the output node OUT. Note in particular that the gate electrodes of all five transistors are connected to external signal inputs; thus, all five nodes at the gate electrodes (respectively) of all five transistors are (by definition) not in a floating state.

79. This changes at time point t_2 :



Here, the clock signal CLK1 has gone high, which turns off transistor M1 and transistor M3. As transistor M1 is turned off, the node that is connected to the gate of transistor M2 is floating – at a high voltage level, which turns off transistor M2, transistor M3, and transistor M4; as transistor M2 is turned off, the clock signal CLK2 (which has gone low) cannot be passed to the output node OUT. In the meantime, the node connected to the gate of transistor M5 is also floating – since it is connected between transistor M3 and transistor M4, which are both turned off;

therefore, this node will remain at a low voltage level – which will keep transistor M5 turned on, which will thus keep the high (VDD) voltage level supplied to the output node OUT. (I further discuss this operation in Ex. 1003, ¶ 383.)

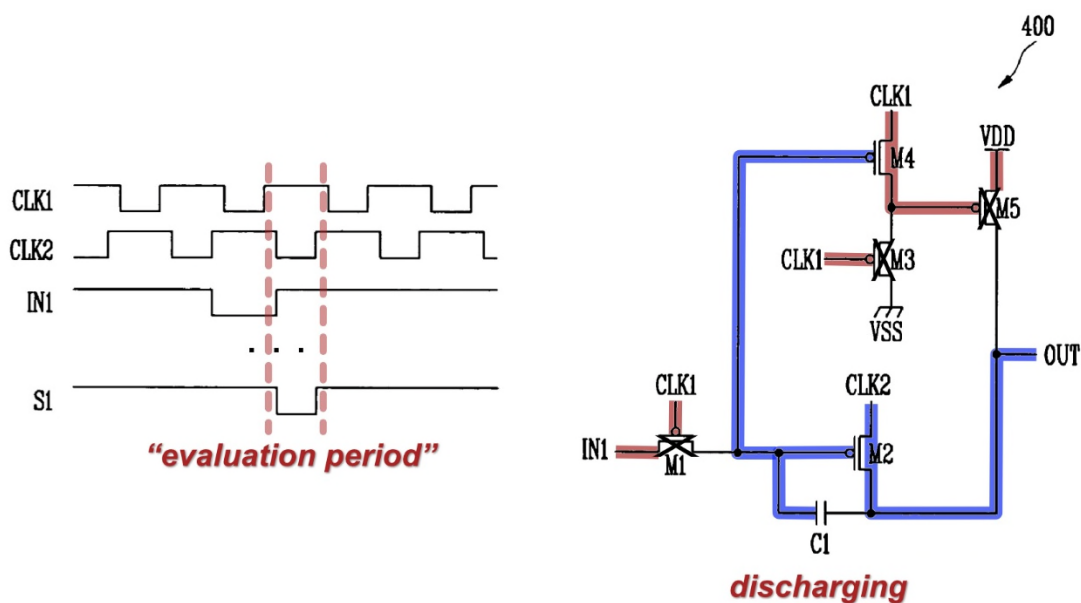
80. However, in order for the VDD signal to be connected unvexed to the output node (OUT) through transistor M5, transistor M2 must remain turned off – as otherwise, the low CLK2 signal will reach the circuit’s output via transistor M2. However, as the high clock signal has turned off transistor M1, the node connected to the gate of transistor M2 (as noted above) is floating. This creates the possibility of a reversal event; noise (due to, for example electromagnetic interference (EMI) – or due to crosstalk from other nearby digital switching events, where switching noise from one circuit (the “aggressor” circuit) propagates (usually capacitively) to an adjacent circuit (the “victim” circuit); this can upset the operational characteristics of the “victim” circuit, such as by causing a logic gate to change its output logic state) can result in spurious signals on this floating node - which can, in turn, cause the transistor M2 to inadvertently turn on, which could instigate the reversal of the signal (from high to low) at the output node – or at least cause a signaling conflict at the output (of uncertain outcome) as two different signals engage in competition for the value (high or low – or something undefined in between) at the output.⁸

⁸ It should also be noted that should transistor M2 turn on at the same time that transistor M5 is (already) turned on, there will be a short circuit between the high

81. This is a particularly-significant problem during this period of Shin’s operation – as no other circuit element is providing any sort of redundant protection for the signal at the output. If the capacitor is unable to maintain the high logic state level on the node that is connected to the gate of transistor M2, conflicting signals will be provided to the output.

82. This can be contrasted with the period of operation shown below. In this period (which Shin refers to as an “evaluation period”), capacitor C1 does operate to keep transistor M2 turned on – so that a low CLK2 signal will be supplied to the output. However, as shown, during this period transistor M5 is turned off – which serves to prevent the high VDD signal from reaching the output at the same time. This redundancy minimizes the risk of the output receiving conflicting signals – even if the capacitor is overwhelmed and is unable to maintain the high logic state level on the node that is connected to the gate of transistor M2:

VDD signal connection at transistor M5 and the low CLK2 signal connection at transistor M2. This would be catastrophic – as such a short circuit would likely cause serious (and permanent) damage to the circuitry. Even if such damage were not to occur, with a large current flowing from high to low through the output node it would be very difficult (if not impossible) for a high VDD voltage to be maintained at the output node.



Shin, Figs. 11, 12; [0100]-[0105]. Again, there is no such redundancy during other periods of operation of Shin’s circuit. Thus, the risk of reversal is greater during those other periods (such as the case explained earlier) – which thus provides motivation for a POSITA to use an anti-reversal circuit (such as the one that is taught by Sasaki, added to Shin’s circuit in the manner that was described in my earlier declaration).

83. As also discussed in my earlier declaration, this is not conjecture on my part; such possible upsets (due to, at least, the two possible causes mentioned above) were well-known in the art as far back as the 1990s (under the general heading of “signal integrity”), and at least one prior art reference cited in that earlier declaration (Moon) specifically refers to this possible problem as being a vulnerability for this type of circuit:

A first capacitor CQ may be connected between the first node Q and an input line of the low-level driving voltage VSS for eliminating noise at the first node Q. Similarly, a second capacitor CBQ may be connected between the fourth node QB and the input line of the low-level driving voltage VSS for eliminating noise at the fourth node QB. (Ex. 1020, ¶ [0053].)

The “noise” mentioned here by Moon can be either of the two types of noise (EMI, or switching noise in the “aggressor/victim” situation) that were mentioned above.

84. As I noted in my earlier declaration, “in Shin’s Figure 11 circuit, there is no way to independently set the node connected to the gate of transistor M2 to a high voltage, so as to ensure that M2 is not turned on unexpectedly.” (Ex. 1003, ¶ 389.) The use of a capacitor (to protect the voltage state of the floating node against being upset sufficiently to reverse the logic signal level and turn transistor M2 on) may be sufficient to stabilize the circuitry against upsets of modest magnitude (and thus sufficient to prevent a node voltage deviation that would reverse the logic signal level of the floating node). However, in the case of a larger upset – one large enough to cause reversal of the logic signal level at the floating node – *the voltage at the capacitor would also be reversed during the upset event*; if this happens, there is no path to recovery – as the voltage at that capacitor terminal will also be changed to the reversed logic state level, and there is nothing that can remedy this occurrence.

85. The key vulnerability to the use of a capacitor is that this approach is *passive* – as once the logic state level has been reversed, there is nothing that can

intervene to remedy the situation. Since the “degree of robustness” provided by the capacitor depends (at least) on the magnitude of the capacitance of the capacitor C1 (which is a function of the physical size of the capacitor and the materials used to construct it), the only way to make the circuitry more robust against upset would be to make the capacitor larger; this raises the threshold for an upset event (as described above) to be induced – but does not provide a remedy for an upset if such an event occurs.

86. In contrast, Sasaki’s anti-reversal circuit is *active* – that is, it will serve to continually keep the node that is connected to the gate of transistor M2 high, so that the off-state of transistor M2 is actively maintained. Thus, the protection from reversal is assured – and is not a function of any of the items listed above with respect to the passive role of capacitor C1.

87. Thus, as these items were all known in the art at the time of the ‘593 patent, a POSITA would have been motivated to remedy the aforementioned deficiency in Shin – by adding Sasaki’s anti-reversal circuit to the Figure 11 stage circuit embodiment of Shin, to provide *active* protection against an upset that would cause a reversal of the logic state level of transistor M2 (and which would turn that transistor on, with the consequences discussed above)⁹.

⁹ As also noted in my earlier Declaration, numerous prior art references employ **both** capacitors and transistors to control a node voltage. (Ex. 1003, ¶ 386.)

88. In addition, I also note that when addressing the combination of Shin and Sasaki (along with other grounds that entail the addition of circuit elements to an existing stage-circuit design), Dr. Wolfe opines that applying Sasaki’s anti-reversal circuit is non-obvious because it “incur[s] ... significant costs in both manufacturing and circuit complexity that stem from adding two additional transistors to a stage circuit.” Ex. 2059, ¶¶ 93-94.

89. However, Dr. Wolfe’s opinion (that the costs of such an addition would be “significant”) is unsupported – as he provides no analysis showing why the costs of such additions would be “significant” (whatever that means). In contrast, it is my conclusion and opinion – for several reasons – that the costs of such a modification would *not* be significant; although TFTs are not as small as are leading-edge silicon-based MOSFETs, TFT manufacturing processes benefit from the sequential (with time) size-reductions and higher-densities that are inherent in what is known as “Moore’s Law” (as lithographic improvements allow for smaller feature sizes from process generation to process generation). Further, as any such modification requires at least some form of cost-benefit analysis to reach conclusions, the benefits can indeed outweigh any costs – which, as discussed above (with respect to the passive capacitor-based approach and the active transistor-based approach), has already been demonstrated to be the case here.

90. As an initial matter, I note that Dr. Wolfe has opined (at Paragraph 45) that a key benefit of the circuitry disclosed in the '593 patent is that the single transistor-level circuit embodiment disclosed in the '593 reduces the number of transistors (and total components) used in such a circuit ("For example, the '593 Patent teaches that prior art stage circuits had 'at least ten transistors,'" (Ex. 2059, ¶ 45)); however, this assertion is problematic for two reasons.

91. First, the '593 patent makes this assertion – but shows no prior art circuits that provide the same functionality but carry it out with a larger number of transistors (as compared to the seven transistors and two capacitors of the circuitry disclosed in the '593 patent); thus, it is unclear what basis there is for this assertion by the '593 patent (or by Dr. Wolfe).

92. Second, other circuitry (which performs the same function as does the circuitry disclosed in the single circuit embodiment of the '593 patent) which has appeared in this matter (and which I included in my original declaration, via several such examples) contains fewer transistors (and total components) than does the disclosed circuitry of the '593 patent; as a direct reference in this declaration, Shin's as-is circuit has only five transistors and one capacitor (i.e., fewer transistors and components than does the single circuit embodiment of the '593 patent), while the combined Shin-Sasaki embodiment has seven transistors and one capacitor (i.e., the

same number of transistors but one less capacitor than does the single circuit embodiment of the '593 patent).

93. Thus, this art indicates that other disclosed (prior art) circuitry contains fewer components than does the circuitry of the '593 patent; further, the combined Shin-Sasaki embodiment (which Dr. Wolfe says would be a bad idea, due to the “significant costs” that the addition of the two transistors to Shin’s original circuit would cause) actually has the same number of transistors (seven) and one less capacitor (one rather than two) than does the circuitry disclosed in the '593 patent.

94. Thus, Dr. Wolfe has argued on the one hand that a stage circuit with seven transistors (and two capacitors) is a significant improvement over the prior art – while on the other hand a stage circuit with seven transistors (and one capacitor) is undesirable because this circuit would have significant cost and manufacturing deficiencies; obviously, these two positions are incompatible.

95. In summary, Figure 3 of the '593 patent shows a circuit that includes seven transistors and two capacitors. Ex. 1001, Fig. 3. The combination of Shin and Sasaki includes seven transistors and one capacitor. Thus, even if increased circuit size were for some reason a determinative factor, a POSITA would have considered the Shin/Sasaki combined embodiment circuit to be more than adequate – as it contains a suitably-small number of components.

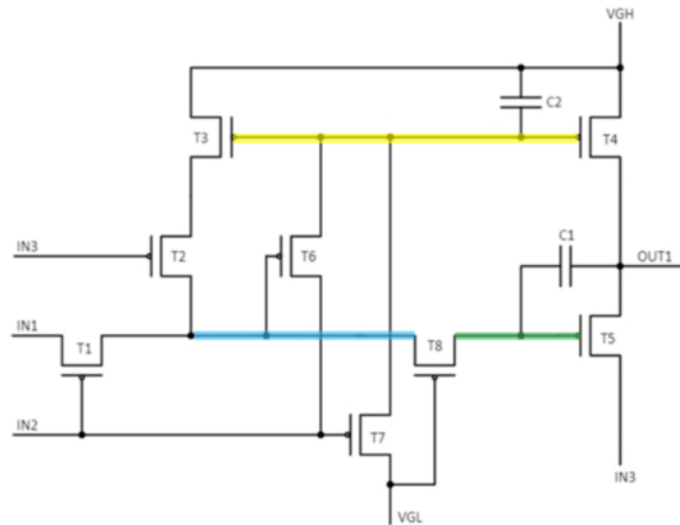
96. Finally, while circuit size and the number of components are notable factors in circuit design, they are not the only key criteria – as circuit engineering requires optimal management of the various trade-offs inherent in any real-world design. At least as important (if not more important) than the two factors mentioned above (that is, circuit size and the number of components) is proper circuit functionality; in fact, proper circuit functionality is arguably the most important factor in circuit design – since, no matter the number of components or the size of the circuit, if the circuit does not function properly then nothing else matters.

97. As described above, the use of a capacitor to prevent reversal of the output signal is a passive method – one that can simply fail to work under particular well-known/real-world circumstances, and without any ability to recover from that failure. In contrast, the added two-transistor anti-reversal circuitry is an active method – one that will remain active for as long as it is needed, and which cannot be overridden by the aforementioned well-known/real-world circumstances that afflict the passive use of a capacitor. The addition of two transistors is a small trade-off price to pay for this robust, active method of preventing the unwanted reversal of the signal at the output.

VI. APPLICATION OF THE CLAIMS TO PATENT OWNER'S ALLEGED PRODUCT

98. I have also been asked to review a discussion of a particular circuit that is included in Patent Owner's Response. According to the Response, this circuit is

representative of “[t]he stage circuits used in the Galaxy S22 Ultra and the Mengtor displays.” Response (Paper 23), p. 61.



99. Patent Owner's and Dr. Wolfe's analysis of this circuit simply makes no sense.

100. According to Patent Owner, transistors T1, T2, and T3 in this circuit constitute the claimed “first driver.” Response, 64.

101. However, Patent Owner does not clearly identify what it believes is the claimed “second node” in this circuit; instead, Patent Owner appears to identify **both** the blue and green circuit annotated paths (which, for convenience here, I will refer to (correctly and properly) as the “blue node” and the “green node”) as the claimed “second node.” *Id.* Dr. Wolfe does the same in a claim chart. *See, e.g.*, Ex. 2046, p. 7.

102. This argument is nonsensical for at least two reasons.

103. First, the “blue node” and the “green node” are on opposite sides of the current path of a transistor; by topological definition, these are separate nodes – as the thin-film transistor used in this circuit has three nodes (the gate, the source, and the drain). Each node must be specified independently in this fashion.

104. Second, as per the discussion just above, the blue node cannot be the claimed “second node” – as it is not connected to the gate of transistor T5. The claims of the ’593 patent require that the “outputting unit” “supply” “a signal of the third input terminal to the output terminal according to a voltage applied to the second node.” Only the green node—which is connected to the gate of transistor T5—is arranged in this way.

105. Thus, in sum, to the extent Patent Owner and Dr. Wolfe are attempting to assert that *both* the blue node and the green node are somehow (collectively) the “second node,” for the reasons described above this is simply not possible and makes no sense – as the source and the drain of any transistor are (by definition) separate nodes.

VII. OTHER ISSUES FROM THE POR AND DR. WOLFE’S DECLARATION

106. As should be apparent from the discussion above, I have addressed only a fraction of the assertions made in the POR and the opinions that Dr. Wolfe has set forth in his declaration. Further, as indicated in Section II, the fact that I did not respond to any particular assertion in the POR or any particular opinion expressed

by Dr. Wolfe should not be considered to indicate agreement with any such assertions (POR) or opinions (Dr. Wolfe's declaration).

107. However, as indicated in Section II, there are a few notable assertions and opinions that should be mentioned – as they are particularly notable.

A. Leakage Current

108. On page 39 of the POR, Patent Owner asserts that I claimed that capacitors are added to reduce the leakage current; however, this is simply wrong – as I claimed no such thing.

109. As is well-known in the field-effect transistor art, if there is a non-zero drain-to-source voltage in a field-effect transistor, then (unless the transistor is operated at a temperature of absolute zero) there will be an off-state leakage current running through that transistor. If one side of the transistor (source or drain) is connected to a floating node, then this leakage current will change the voltage of that floating node until the node voltage there matches the voltage on the other side of the transistor; at that point, this will have caused the voltage between the source and the drain of the transistor to become equal, and the node voltage will have reached its final (changed) state. As an example, if there is high voltage on the floating node on one side of the transistor and the voltage on the other side of the transistor is pulled low, the voltage on the floating node will decrease until it reaches the low voltage level on the other side of the transistor. (The best analogy is that when a

leaky bucket has drained completely of water, then no more water will flow – because there *is* no more water to flow; alternatively, if a leaky box is placed under water, water will flow into the box until the box is filled with water – and, once again, no more water will flow.)

110. The amount of time necessary for this final state to be reached is a function of several characteristics of the transistor through which the stored charged is draining – characteristics such as the size of the transistor, the specific electrical characteristics of the transistor (such as the threshold voltage value), and the operating temperature of the circuitry (which would be at least at room temperature, but likely higher due to heat generated by operation – with a higher temperature causing a higher leakage current). However, as can be seen from this list of characteristics, the leakage current is a function *only* of the transistor in question and the temperature of its operating environment – and has nothing to do with the nature of the floating node that is being drained. (To re-invoke the leaky-bucket analogy, the rate of leakage of water from the bucket is a function of the size of the holes in the bottom of the bucket – not of the amount of water in the bucket at any given time.)

111. A POSITA would have been well-aware of these aspects of the leakage current associated with field-effect transistors and floating nodes – particularly since these are the known operating aspects of DRAM memory cells (and the amount of

time that a DRAM cell is able to retain charge (which represents a stored bit) and the amount of time that will pass before the charge (and thus the stored bit information) is lost).

112. Patent Owner has demonstrated that it does not understand transistor operation and basic semiconductor physics – and as a result has asserted a conclusion from my declaration and my testimony that is simply incorrect.

B. Signal Integrity

113. At Paragraph 79, Dr. Wolfe simply brushes off my discussion (in my earlier declaration) regarding what the Jeong and Moon references have to say about the addition of capacitors to a circuit in particular situations: (arguing that Jeong and Moon do not “‘solve’ generalized concerns such as EMI or crosstalk”) However, this is incorrect – as both Jeong and Moon describe the reasons that a designer would add one of more capacitors to a particular circuit; in fact, contrary to what Dr. Wolfe asserts, Moon *does* discuss “concerns such as EMI or crosstalk” (which, as explained below, Moon refers to as “noise”) – and proposes circuitry modifications that improvement circuit robustness against the effects of “EMI and crosstalk” (i.e., “noise”). As both Jeong and Moon are prior art to the ‘593 patent, both of these references and their content would have been known to a POSITA at the time of the ‘593 patent.

114. Both Jeong and Moon describe the option of including capacitors into circuits for the purpose of improving the robustness of the charge (and thus the voltage state) of particular nodes (particularly floating nodes) against signal-integrity upsets – such as the well-known “aggressor/victim” situation discussed earlier, where switching noise from one circuit (the “aggressor” circuit) propagates (usually capacitively) to an adjacent circuit (the “victim” circuit); this can upset the operational characteristics of the “victim” circuit, such as by causing a logic gate to change its output logic state.. A quotation from Moon that I provided in my original declaration (and also presented earlier in this declaration) is worth repeating here

A first capacitor CQ may be connected between the first node Q and an input line of the low-level driving voltage VSS for eliminating noise at the first node Q. Similarly, a second capacitor CBQ may be connected between the fourth node QB and the input line of the low-level driving voltage VSS for eliminating noise at the fourth node QB. (Ex. 1020, ¶ [0053].)

115. Dr. Wolfe simply rejected the teachings of these references (particularly of Moon) without considering them – even though those teachings are clearly germane to the circuitry that appears in this IPR, and were well-known in the art at the time of the ‘593 patent.

C. Final Comments

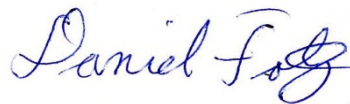
116. As noted in Section II and at the outset of this section, I will not address all of the mischaracterizations and out-of-context usages of my earlier declaration

and my deposition testimony by Patent Owner (in the POR) and by Dr. Wolfe (in his declaration). While I discussed a few notable examples here, as noted earlier my not discussing any particular assertion(s) by either Patent Owner or Dr. Wolfe does mean that I (in any way) agree with those assertions.

VIII. CONCLUSION

117. I am aware that this will be filed as evidence in an IPR proceeding before the PTAB. I am aware that making willfully false statements in my declaration are punishable by fine or imprisonment, or both (under 18 U.S.C. § 1001), and thus such actions may compromise the validity of the IPR Petition. All statements herein made by me of my own knowledge are true, and all statements made on information and belief are believed to be true.

118. I declare under penalty of perjury that the foregoing is true and correct.
Executed this 6th day of March, 2025 in Fletcher, Vermont.



Daniel Foty, Ph.D.