

MIANYANG BOE OPTOELECTRONICS	)	Case No.
TECHNOLOGY CO., LTD.; TCL	)	IPR2024-00620
CHINA STAR OPTOELECTRONICS	)	
TECHNOLOGY CO., LTD.; TIANMA	)	U.S. Patent No.
MICROELECTRONICS CO. LTD.;	)	9,330,593
AND VISIONOX TECHNOLOGY,	)	
INC.,	)	
	)	
Petitioner,	)	
	)	
vs.	)	
	)	
SAMSUNG DISPLAY CO., LTD.,	)	
	)	
Patent Owner.	)	
	)	

Reported in Stenotype by:
Cody R. Knacke, RMR, CSR No. 13691
Job No.: 974310

REMOTE VIDEOTAPED DEPOSITION OF

DR. ANDREW WOLFE, PH.D., taken before Cody R.
Knacke, RMR, CSR No. 13691, a Certified Shorthand
Reporter for the State of California, commencing on
Tuesday, February 25, 2025, at 8:59 a.m.,
Pacific Time.

(All Appearances Via Videoconference.)

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EXAMINATION BY:

BY MR. HERMAN

PAGE

5

E - X - H - I - B - I - T - S

PREVIOUSLY MARKED EXHIBITS

MARKED

DESCRIPTION

PAGE

Exhibit 1001

U.S. Patent No. 9,330,593 - Jang

8

Exhibit 1004

U.S. Patent Application Publication US 2011/0057190 A1 - Kimura, et al.

21

Exhibit 2046

Claim Chart: AMOLED Display in Mengtor Product

55

Exhibit 2059

Declaration of Andrew Wolfe, Ph.D. in Support of the Patent Owner Response

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QUESTIONS INSTRUCTED NOT TO ANSWER

None.

INFORMATION REQUESTED

None.

1 TUESDAY, FEBRUARY 25, 2025

2 8:59 A.M.

3 THE VIDEOGRAPHER: We are now on the record
4 on February 25, 2005, at approximately 8:59 a.m.
5 Pacific Time for the remote video deposition of
6 Dr. Andrew Wolfe, Ph.D., in the matter of Mianyang
7 Boe Optoelectronics Technology Co., et al. versus
8 Samsung Display Co., Ltd.

9 My name is Joshua Clarke, and I'm the
10 videographer on behalf of Lexitas.

11 So starting with the taking attorney, will
12 all counsel please introduce themselves and who they
13 represent.

14 MR. HERMAN: This is Patrick Herman from
15 Orrick Herrington & Sutcliffe here on behalf of
16 petitioners.

17 MR. ANDROS: This is Derek Andros from
18 Covington & Burling on behalf of patent owner.

19 THE VIDEOGRAPHER: All right. Thank you.
20 Now, will the court reporter please swear
21 in the witness.

22 THE STENOGRAPHER: My name is Cody Knacke,
23 CSR 13691.

24 ///

25 ///

1 DR. ANDREW WOLFE, PH.D.,
2 called as a witness, having been first duly sworn,
3 testified as follows:

4 EXAMINATION

5 BY MR. HERMAN:

6 Q. Good morning, Doctor. Before beginning, I
7 would like to briefly go over some basic ground
8 rules to help ensure that things go smoothly here
9 today and just to make sure that we're on the same
10 page.

11 The first is, as you just heard, there's a
12 court reporter here, so it's important that you
13 respond and answer my questions verbally so they can
14 record your testimony.

15 Is that okay?

16 A. Yes.

17 Q. It's also important that we try not to talk
18 over each other so that there's a clear record, and
19 I'll do my best to wait for you to finish answering
20 before asking another question and ask that you wait
21 until I'm done with my question before answering.

22 Is that okay?

23 A. I understand.

24 Q. Next, if anything I ask is unclear, please
25 let me know and I'll try to clarify; otherwise, I'll

1 assume that we're on the same page.

2 Is that okay?

3 A. You assume that I understood the question.

4 Q. Next, I ask that you not look at any
5 documents during the deposition besides the
6 documents that I give you.

7 Is that okay?

8 A. We can start off that way. I may not be
9 able to answer every question without looking at the
10 relevant documents.

11 Q. Sure. So if you need access to a
12 particular document, please let me know and I'll do
13 my best to get that to you.

14 All right?

15 A. Okay.

16 Q. Next, I ask that you not have any side
17 conversations or use technology to chat or
18 communicate with anyone during the deposition.

19 Is that okay?

20 A. Okay.

21 Q. And lastly, is there anything that would
22 prevent or interfere with your ability to testify
23 today?

24 A. Not that I'm aware of, no.

25 Q. So I'm going to start out by putting into

1 the chat a copy of an exhibit that's been previously
2 marked Exhibit 2059.

3 (Exhibit 2059 was previously marked by the
4 Certified Shorthand Reporter, and a copy is
5 attached hereto.)

6 BY MR. HERMAN:

7 Q. Let me know when you've had a chance to
8 download and open that.

9 A. Okay.

10 Q. Do you have that?

11 A. I do.

12 Q. So if you look at the cover of the
13 document, the case caption that the videographer
14 read is there, and it's also entitled "Declaration
15 of Andrew Wolfe, Ph.D. in Support of Patent Owner's
16 Response."

17 Do you see that on the cover?

18 A. Yes.

19 Q. And if you flip through, you'll also see
20 that portions of this particular exhibit,
21 particularly towards the end, are redacted; correct?

22 A. Yes.

23 Q. So today I'm going to be focusing my
24 questions on the non-redacted portions of your
25 declaration in the hopes that this transcript can

1 remain public. And while I don't envision this will
2 come up, if for some reason you believe you're
3 unable to answer a question without revealing
4 something that you believe is somewhere in your
5 declaration but has been redacted, I ask that you
6 tell me that before answering.

7 Is that okay?

8 A. I will try to do that.

9 Q. Now, this declaration relates to
10 U.S. Patent Number 9,330,593; is that right?

11 A. Yes.

12 Q. Is it okay if I refer to that today as the
13 '593 patent?

14 A. I will understand what you mean.

15 Q. So I'm going to put another exhibit into
16 the chat. And this one's been previously designated
17 Exhibit 1001.

18 (Exhibit 1001 was previously marked by the
19 Certified Shorthand Reporter, and a copy is
20 attached hereto.)

21 BY MR. HERMAN:

22 Q. Let me know when you have that.

23 A. I do.

24 Q. That's the '593 patent; correct?

25 A. Yes.

1 Q. That's the patent that you addressed and
2 discussed throughout your declaration?

3 A. Yes.

4 Q. Now, if you could turn to the claims of the
5 '593 patent for me, and those begin on -- or in
6 Column 9 of the patent, which is the second-to-last
7 page of the PDF.

8 A. I see them.

9 Q. And if you can direct your attention to
10 Claim 1.

11 A. Okay.

12 Q. So that claim includes a preamble.
13 You understand what I mean by the preamble
14 of Claim 1?

15 A. I do.

16 Q. So the preamble of Claim 1 states that
17 Claim 1 is directed to a stage circuit having a
18 first input terminal, a second input terminal, a
19 third input terminal, and an output terminal;
20 correct?

21 A. There is a few more words, but you read
22 that correctly.

23 Q. Now, in that preamble and in the rest of
24 Claim 1, there's no reference to what particular
25 type of device that stage -- that stage circuit is

1 used in; correct?

2 MR. ANDROS: Objection. Form.

3 THE WITNESS: There's no particular
4 language that describes a specific kind of device.
5 I think whether or not it describes a specific
6 device would depend on whether or not the legal
7 authorities attribute any particular claim
8 construction.

9 BY MR. HERMAN:

10 Q. But the words in the claim don't make any
11 mention of a particular device. They say the claim
12 is directed to a stage circuit; correct?

13 MR. ANDROS: Objection. Form.

14 THE WITNESS: Again, I'm concerned you're
15 asking for a legal opinion here. My understanding
16 is that these words could refer back to the
17 specification.

18 For purposes of my declaration, I've used
19 the constructions that were suggested by the PTAB.

20 BY MR. HERMAN:

21 Q. So Claim 1 does not mention an OLED
22 display; correct?

23 A. Not in so many words, it does not.

24 Q. And it does not mention an active matrix
25 OLED display; correct?

1 A. Not in so many words, it does not.

2 Q. Instead, the only words that Claim 1 uses
3 in its preamble -- well, I mean, there are other
4 words -- but it references a stage circuit in the
5 preamble; correct?

6 MR. ANDROS: Objection. Form.

7 THE WITNESS: The preamble does claim a
8 stage circuit.

9 BY MR. HERMAN:

10 Q. Now, the claim, Claim 1, does not specify
11 whether that stage circuit is used in a mobile
12 device or a nonmobile device; correct?

13 A. Yeah, I think you're asking me for a legal
14 opinion, but under a plain meaning construction, I
15 don't think that they do.

16 Q. So under that claim meaning construction,
17 the stage circuit could be used in either a mobile
18 device or a non -- nonmobile device; correct?

19 MR. ANDROS: Objection. Form.

20 THE WITNESS: Under a plain meaning
21 construction, the stage circuit of Claim 1 could be
22 used in either a mobile device or a nonmobile
23 device.

24 BY MR. HERMAN:

25 Q. Under a plain meaning construction, that

1 stage circuit could be used in an OLED display or a
2 non-OLED display; correct?

3 MR. ANDROS: Objection. Form.

4 THE WITNESS: Under a plain meaning
5 construction of all the terms, that would be
6 correct.

7 BY MR. HERMAN:

8 Q. Now, if you searched the '593 patent, the
9 word "mobile" does not appear anywhere; correct?

10 MR. ANDROS: Objection. Form.

11 THE WITNESS: I believe that's correct.

12 BY MR. HERMAN:

13 Q. The word "bevel" does not appear anywhere
14 in the '593 patent; correct?

15 A. I believe that's correct as well.

16 Q. And the phrase "active matrix" isn't
17 anywhere to be found in the '593 patent either;
18 correct?

19 MR. ANDROS: Objection. Form.

20 THE WITNESS: I don't see that specific
21 term.

22 BY MR. HERMAN:

23 Q. And the word "active" is not found in the
24 '593 patent; correct?

25 A. I don't see that specific word.

1 Q. Now, I'd like to direct your attention back
2 to Claim 1 again.

3 After the preamble, the claim references,
4 in separate paragraphs, an outputting unit, a first
5 driver, and a second driver; correct?

6 A. Correct.

7 Q. Now, in those three paragraphs referring to
8 the outputting unit, the first driver, and the
9 second driver, there is no language that requires
10 that there be any particular number of transistors
11 in those outputting units, first drivers, and second
12 drivers; correct?

13 MR. ANDROS: Objection. Form.

14 THE WITNESS: I'm struggling with that
15 question. Certainly there are a minimum number of
16 transistors required by the claim.

17 BY MR. HERMAN:

18 Q. So the only place that the word
19 "transistor" appears in the claim appears to be in
20 the final limitation; is that right?

21 A. That's the only place where it literally is
22 present, yes.

23 Q. So the paragraph that references the first
24 driver does not refer to any transistors; correct?

25 A. I'm not quite sure that a person of

1 ordinary skill would know how to build a first
2 driver without any transistors. That really wasn't
3 an issue I had to address in order to reach opinions
4 in my declaration.

5 Q. So in your view, the first driver, the
6 second driver, and the output unit require at least
7 some transistors; correct?

8 MR. ANDROS: Objection. Form.

9 THE WITNESS: Again, I didn't have to reach
10 an opinion on that, but all of the embodiments that
11 I saw and all the prior art that I saw did involve
12 at least some transistors in each of those.

13 BY MR. HERMAN:

14 Q. Is there any limitation in Claim 1
15 regarding the maximum numerical number of
16 transistors that could be in the first driver?

17 MR. ANDROS: Objection. Form.

18 THE WITNESS: I don't know. I mean, that's
19 a complicated analysis as to whether or not there's
20 some number of transistors in which you could no
21 longer meet the other limitations, and I haven't
22 done that analysis.

23 BY MR. HERMAN:

24 Q. But there's no number in Claim 1 when it
25 comes to the first -- the first driver; is that

1 true?

2 MR. ANDROS: Objection. Form.

3 THE WITNESS: There's no literal number of
4 transistors recited in the first driver limitation
5 as a limit, but you do need to meet the requirements
6 of the claim limitation.

7 BY MR. HERMAN:

8 Q. So as long as you meet the requirements of
9 the claim limitation, it does not matter how many
10 transistors you have in your first driver; is that
11 your position?

12 MR. ANDROS: Objection. Form.

13 THE WITNESS: Under the plain meaning
14 construction that I used, you just have to meet the
15 recited limitation. It would not specify a maximum
16 number of transistors that you could use to do that.

17 BY MR. HERMAN:

18 Q. And applying that same claim meaning to the
19 second driver and the outputting unit limitations,
20 are you of the same view, that as long as you
21 perform the function the claim requires, there's no
22 limit on the maximum number of transistors that
23 could be present; correct?

24 MR. ANDROS: Objection to form.

25 THE WITNESS: Under a plain meaning

1 construction, I don't see a maximum number of
2 transistors for the second driver or for the final
3 limitation as long as you meet the limitation in the
4 claim.

5 BY MR. HERMAN:

6 Q. Now, if you could turn back to Figure 3 of
7 the '593 patent, which is on page 4 of the PDF.

8 A. Okay.

9 Q. So Figure 3 has two larger elements, one of
10 which is labeled ST1 and another which is labeled
11 ST2.

12 Do you see that?

13 A. Yes.

14 Q. So ST1 is one stage of stage circuit;
15 correct?

16 A. Yeah. So in particular here, it's a scan
17 driver.

18 Q. And ST2 is a second stage; correct?

19 A. It is -- well, it is an adjacent second
20 stage, not just a second stage.

21 Q. Now, in the circuit ST1, the outputting
22 unit is surrounded by a dashed box that's labeled
23 230; is that right?

24 A. Yes.

25 Q. And there are two transistors in that

1 labeled outputting unit. There are M4 and M5;
2 correct?

3 A. Correct.

4 Q. Now, in that first stage circuit, the first
5 driver is labeled 210, with a dashed box that's
6 labeled 210; correct?

7 A. Yes.

8 Q. And there are three transistors -- M1, M2,
9 and M3 -- in that first driver; correct?

10 A. In this embodiment, yes.

11 Q. And the second driver in this particular
12 stage circuit is in a box, a dashed box that's
13 labeled 220; correct?

14 A. Correct.

15 Q. And there are two transistors, M6 and M7,
16 in this stage circuit second driver; correct?

17 A. Correct.

18 Q. So this embodiment includes a total of
19 seven transistors; is that right?

20 A. Yes, seven transistors and two capacitors.

21 Q. Now, you'll agree with me that the claims
22 in the '593 patent are not limited to circuits
23 employing exactly or no more than seven transistors;
24 correct?

25 MR. ANDROS: Objection. Form.

1 THE WITNESS: Not under the constructions
2 that I've applied.

3 BY MR. HERMAN:

4 Q. Now, what's shown in Figure 3 is meant to
5 be a working stage circuit; is that correct?

6 MR. ANDROS: Objection. Form.

7 THE WITNESS: It's meant to teach a working
8 stage circuit, yes.

9 BY MR. HERMAN:

10 Q. Now, if you could turn to Column 8 starting
11 about line 43.

12 Let me know when you're there.

13 A. Okay.

14 Q. There the '593 patent states that:
15 "Figure 7 illustrates a circuit diagram of a stage
16 circuit according to a third embodiment."

17 Is that right?

18 A. It does.

19 Q. So Figure 3 that we looked at is one
20 embodiment of the stage circuit in the '593 patent;
21 true?

22 A. Yes.

23 Q. Figure 7 is meant to be another embodiment
24 of a stage circuit that's discussed in the
25 '593 patent; correct?

1 MR. ANDROS: Objection. Form.

2 THE WITNESS: Figure 7 illustrates a third
3 embodiment.

4 BY MR. HERMAN:

5 Q. Now, if you could turn to Figure 7 for me,
6 which is on page 8 of the PDF.

7 A. Okay.

8 Q. So the stage circuit -- and there's the two
9 stages listed again, shown in Figure 7; correct?

10 A. Yes.

11 Q. Now, each stage in this stage circuit in
12 Figure 7 is different from the stages in Figure 3;
13 correct?

14 MR. ANDROS: Objection. Form.

15 THE WITNESS: I haven't actually performed
16 that comparison. It wasn't really necessary for the
17 opinions in my declaration.

18 BY MR. HERMAN:

19 Q. So you have not compared Figure 7 to
20 Figure 3 before today?

21 A. No. I don't think that was necessary for
22 any of my opinions.

23 Q. So looking at Figure 7, the stage that's
24 labeled ST1 which is on the top of Figure 7,
25 includes two transistors, M10 and M11; correct?

1 A. Those two transistors are present.

2 Q. And those two transistors were not part of
3 the embodiment shown in Figure 3; correct?

4 A. Correct.

5 Q. And Figure 7 also shows inputs that are not
6 present in Figure 3; correct?

7 MR. ANDROS: Objection. Form.

8 THE WITNESS: Yes.

9 BY MR. HERMAN:

10 Q. And at least two of those are labeled CS1
11 and CS2; is that true?

12 A. Yes.

13 Q. So compared to Figure 3, each stage in
14 Figure 7 includes at least two additional
15 transistors and two additional inputs; true?

16 MR. ANDROS: Objection. Form.

17 THE WITNESS: The totality of the circuit
18 does, yes.

19 BY MR. HERMAN:

20 Q. And the '593 patent identifies Figure 7 as
21 one of its embodiments; is that correct?

22 A. Yes. My understanding is that that's the
23 practice in at least one claim.

24 Q. It identifies this as an embodiment of the
25 '593 patent, even though it employs more transistors

1 than is shown in Figure 3; correct?

2 A. The circuit, as a whole, employs more
3 transistors than the Figure 3 example.

4 Q. Now, if you look at Figure 7, each stage
5 includes what appear to be nine transistors and two
6 capacitors; correct?

7 A. Yes.

8 Q. So a total of 11 circuit elements in each
9 stage?

10 A. Yes.

11 MR. ANDROS: Objection.

12 THE WITNESS: To the extent that you're
13 counting the capacitors and the transistors as
14 circuit elements, that would be true.

15 BY MR. HERMAN:

16 Q. And again, this is a circuit that the
17 '593 patent itself identifies as an embodiment of
18 its invention; correct?

19 A. It does.

20 Q. Now I'm going to put another exhibit in the
21 chat. And this one's been previously marked as
22 Exhibit 1004.

23 (Exhibit 1004 was previously marked by the
24 Certified Shorthand Reporter, and a copy is
25 attached hereto.)

1 BY MR. HERMAN:

2 Q. Let me know when you have that.

3 A. Okay.

4 Q. So Exhibit 1004 is a prior art reference to
5 an individual with the last name Kimura; is that
6 correct?

7 A. Kimura is the first inventor listed.

8 Q. And this is the reference to Kimura that
9 you review and address in your declaration; true?

10 A. It appears to be.

11 Q. Now, if you could turn to Figure 15A for
12 me, which is on page 16 of the PDF.

13 A. Okay.

14 Q. Figure 15A is a timing diagram; correct?

15 MR. ANDROS: Objection. Form.

16 THE WITNESS: I believe so. I don't
17 believe Figure 15A, as best as I can recall, was
18 part of the mapping proposed by the petitioners. So
19 I haven't really studied it, I don't think.

20 BY MR. HERMAN:

21 Q. Now, looking at Figure 15A, there are a
22 number of labels on the left side of the figure.

23 Do you see that?

24 A. Yes.

25 Q. The first two labels are IN1 and IN2.

1 Do you see that?

2 A. Correct.

3 Q. Those are input signals; correct?

4 A. We'd have to go back to the description. I
5 wouldn't want to jump to that conclusion.

6 Q. Sitting here today, you don't know if
7 Kimura uses IN1 and IN2 throughout its disclosure to
8 refer to input signals?

9 MR. ANDROS: Objection to form.

10 THE WITNESS: That wasn't a determination I
11 needed to make. There are more than 50 diagrams in
12 Kimura, and I responded to the mapping put forth in
13 the petition.

14 BY MR. HERMAN:

15 Q. Did you review the totality of Kimura in
16 arriving at your opinions?

17 A. I did review it all, yes.

18 Q. So turn to paragraph 104 of Kimura, which
19 is on page 54 of the PDF.

20 A. Okay.

21 Q. There Kimura states: "The signal IN1 is
22 input to the wiring 112. A signal IN2 is input for
23 the wiring 113. A signal IN3 is input for the
24 wiring 114."

25 Do you see that?

1 A. I do. That is in reference to
2 Embodiment 1, and I'd have to look at exactly which
3 figure it was referring to.

4 Q. Are you aware of any portion of Kimura that
5 refers to signal IN1 as anything other than an input
6 signal?

7 MR. ANDROS: Objection. Form.

8 THE WITNESS: I haven't tried to make that
9 determination.

10 BY MR. HERMAN:

11 Q. So you have not determined in arriving at
12 your opinions whether signal IN1 is consistently
13 referred to throughout Kimura as an input signal?

14 MR. ANDROS: Objection. Form.

15 THE WITNESS: No, because even if it was,
16 that wouldn't really help to inform me as to whether
17 or not any particular circuit would function
18 properly with any particular -- well, let me try to
19 rephrase that.

20 The mere fact, if it's true that it's an
21 input signal, is not particularly informative at
22 making a determination of anticipation or
23 obviousness.

24 BY MR. HERMAN:

25 Q. So turn back to Figure 15A for me.

1 A. Yes.

2 Q. There are two signals in that figure that
3 are labeled as IN1 and IN2; correct?

4 A. There are, but there are different signals
5 labeled that way in 15B and different signals that
6 way labeled in 15C. So the mere fact that they have
7 simple names like that does not convey general
8 information about all the embodiments.

9 Q. Did you review Kimura to determine what it
10 means or what it's intending to convey in
11 Figures 15A, 15B, and 15C?

12 A. At one point, but that's not something I
13 relied on for any of my opinions, because my
14 recollection, unless you can show me differently,
15 was that was not the mapping that Dr. Foty relied
16 on.

17 Q. So in Figure 15A, the signal IN1 is high in
18 what's labeled as period A; correct?

19 A. In Figure 15A, that is true.

20 Q. And in Figure 15A, the signal that's
21 labeled as IN2 is low in that same period A;
22 correct?

23 A. In 15A, that is true.

24 Q. And in 15A, in period B, the two signals
25 reverse, IN1 becomes low and IN2 becomes high;

1 correct?

2 A. In 15A, that is correct.

3 Q. So turn down to Figure 17B, which is on
4 page 18.

5 A. Okay.

6 Q. Figure 17B is another timing diagram;
7 correct?

8 A. It is another timing diagram.

9 Q. And this timing diagram also has signals
10 that are labeled IN1 and IN2; true?

11 A. It does.

12 Q. And the signals IN1 and IN2 behave in the
13 same way in Figure 17B as they did in Figure 15A;
14 true?

15 MR. ANDROS: Objection. Form.

16 THE WITNESS: That is generally true with
17 respect to these two particular drawings. The
18 reason that they're separate drawings is because
19 other signals respond differently and because Kimura
20 teaches them as applying to different circuits.

21 BY MR. HERMAN:

22 Q. But signals IN1 and IN2 are, in fact, the
23 same in Figures 15A and 17B; true?

24 MR. ANDROS: Objection. Form.

25 THE WITNESS: For the portions shown, they

1 are.

2 BY MR. HERMAN:

3 Q. So turn down to Figure 21B, which is on
4 page 22 of the PDF.

5 A. Yes.

6 Q. This is yet another timing diagram;
7 correct?

8 A. It is. It includes a number of other
9 signals that are, in some cases, different from the
10 prior ones.

11 Q. Now, two are of the signals that are
12 depicted are, again, IN1 and IN2; correct?

13 A. Correct.

14 Q. And IN1 and IN2 in Figure 21B are the same
15 as they're depicted in both Figures 15A and 17B;
16 true?

17 MR. ANDROS: Objection. Form.

18 THE WITNESS: For the portions shown they
19 are; although if one reads the text, they apply to
20 different circuits.

21 BY MR. HERMAN:

22 Q. Do you have an understanding of what signal
23 IN2 that's shown in Figure 21B is?

24 A. As shown in Figure 21B, it is illustrated.

25 Q. Do you know if it's an input signal or not?

1 A. Figure 21B is intended -- let me quickly
2 check the text.

3 Figure 21B is intended to reflect
4 connections to circuit 21A, and with respect to
5 Figure 21A, IN4 is an input.

6 Q. Now, if you turn to Figure 25B, which is on
7 page 26 of the PDF.

8 A. Yes.

9 Q. That's another timing diagram; correct?

10 A. It is. I don't recall Dr. Foty relying on
11 25B as a timing diagram, but it is a timing diagram.

12 Q. This one also shows the signals IN1 and IN2
13 again; correct?

14 A. Yes.

15 Q. And those signals are the same, once again,
16 as they were in Figures 15A, 17B, and 21B; true?

17 MR. ANDROS: Objection. Form.

18 THE WITNESS: The portions shown of 25B
19 related to IN1 and IN2 is the same as the portions
20 as shown in 21B and 17B, 15A, but as I noted before,
21 not the same as 15B or 15C.

22 BY MR. HERMAN:

23 Q. Now, do you know what IN5 is referring to?

24 MR. ANDROS: Objection. Form.

25 THE WITNESS: Again, let me just check the

1 text to make sure that I get the language right.

2 It's described in paragraph 281 with
3 respect to the circuit in 25A, and it's described as
4 being able to essentially pull down a particular
5 node with a transistor.

6 BY MR. HERMAN:

7 Q. Do you know if it's an input signal?

8 A. With respect to Figure 25A, it is.

9 Q. Now if you could turn down to Figure 31C,
10 which is on page 32 of the PDF.

11 A. Yes.

12 Q. That's another timing diagram; true?

13 A. It is.

14 Q. And once again, among other things, it
15 shows signals IN1 and IN2?

16 A. Among other things, it does.

17 Q. Once again, they are the same as they were
18 in all of Figures 15A, 17B, 21B, and 25B; true?

19 MR. ANDROS: Objection. Form.

20 THE WITNESS: If you limit yourselves to
21 the illustrated portion of signals IN1 and IN2 and
22 you limit yourselves to that particular set of
23 timing diagrams that you had mentioned and do not
24 compare it to the others, then the illustrations and
25 signals IN1 and IN2 are the same.

1 BY MR. HERMAN:

2 Q. Now, the figures that we've just looked at
3 also include other signals in addition to IN1 and
4 IN2; correct?

5 MR. ANDROS: Objection to form.

6 THE WITNESS: They do.

7 BY MR. HERMAN:

8 Q. For instance, Figure 31C that we're looking
9 at now includes signals labeled VN1, VN -- sorry --
10 VN11, VN12, and V -- V13; is that right?

11 I may have put an N in there when I was not
12 supposed to. Let me start again.

13 So Figure 31C includes what is labeled V11,
14 V12, and V13; correct?

15 A. When taken in the proper context. Each of
16 these timing diagrams is described in Kimura as
17 applying to a specific one or more circuits. And
18 when you take that context into account for 31C,
19 then it applies to Figures 31A and 31B, then it
20 illustrates three additional signals, at least; V11,
21 V12, and V13.

22 Q. So that V11, V12, and V13 in Figure 31C is
23 referring to the internal node or circuit path
24 voltages at the portions of the circuits labeled 11,
25 12, and 13 in Figures 31A and 31B; correct?

1 MR. ANDROS: Objection. Form.

2 THE WITNESS: Let me check the text one
3 more time.

4 I don't think -- I don't see in the text
5 right now a description of whether it applies to 31A
6 or 31B or both, and I haven't done that analysis
7 because it wasn't necessary for my opinions.

8 BY MR. HERMAN:

9 Q. So do you have an understanding of what V11
10 and V12 is meant to refer to in each of the timing
11 diagrams in Kimura?

12 MR. ANDROS: Objection. Form.

13 THE WITNESS: Each of the time -- each of
14 the timing diagrams in Kimura applies to a specific
15 circuit, and to the extent that those circuits have
16 nodes labeled 11 and 12, the corresponding timing
17 diagram is intended to illustrate the voltages at
18 those nodes, 11 and 12.

19 BY MR. HERMAN:

20 Q. So if the corresponding circuit as a
21 node 11, the signal labeled V11 in the corresponding
22 timing diagram is meant to refer to the voltage at
23 node 11 over time; true?

24 A. If by "corresponding" you mean the one that
25 Kimura explains is corresponding, then that would be

1 true.

2 Q. And the same would apply to what's labeled
3 as V12 and V13 in the timing diagrams, if the
4 corresponding circuit in Kimura has a node 12 and a
5 node 13, the corresponding timing diagram is meant
6 to show the voltage at node 12 and node 13 at the
7 times in the timing diagram; correct?

8 MR. ANDROS: Objection. Form.

9 THE WITNESS: I haven't validated that for
10 every timing diagram, whether or not it was referred
11 to in the petition, but, in general, to the extent
12 that Kimura explains that a timing diagram is
13 intended to reflect the operation of a specific
14 circuit diagram, then the nodes V12 and V13 would
15 reflect corresponding circuits -- corresponding
16 nodes.

17 BY MR. HERMAN:

18 Q. So if we look at Figure 17B, for instance,
19 which is on page 18.

20 A. Yes.

21 Q. Figure 17B is a timing diagram that's meant
22 to apply to Figure 17A; correct?

23 A. Let me check.

24 It is.

25 Q. And the circuit that's shown in Figure 17A

1 has nodes that are labeled 11, 12, and 13; true?

2 A. Yes.

3 Q. And the node 13 is leading to the gate of
4 the transistor that's labeled 203; correct?

5 A. It is -- the node 13 is connected to the
6 gate of transistor 203.

7 Q. And the timing diagram that's shown in 17B
8 has -- shows the signals present, that V11, V12, and
9 V13 over time; correct?

10 A. With respect to Figure 17A circuit, when
11 operated as shown in Figure 17B and described in the
12 text with respect to that circuit.

13 The problem is that Dr. Foty relied on it
14 for Figure 27, which doesn't make sense.

15 Q. In Figure 17B, that timing diagram is
16 showing the voltage at node 13 as being $V_2 + V_{th203} + V_a$
17 in period D; correct?

18 A. Yes, although we'd have to look. My
19 recollection -- again, I don't think I analyzed that
20 for this particular diagram because Dr. Foty didn't
21 rely on V13 from this diagram. But let's take a
22 look. I'm not sure that those various terms are
23 actually defined.

24 I don't recall seeing a definition of V_a
25 anywhere in the specification.

1 Q. Now, the potential of node 13 in period D
2 in Figure 17B is the same as the potential at
3 node -- in node -- at node 13 in period D that's
4 shown in Figure 21B; correct?

5 MR. ANDROS: Objection. Form.

6 THE WITNESS: I'm sorry. Can you ask the
7 question one more time?

8 BY MR. HERMAN:

9 Q. So both Figure 17B and Figure 21B label the
10 potential of node 13 in period D as $V_2 + V_{th203} + V_a$;
11 correct?

12 A. They're both labeled that way, but they
13 were -- but they correspond to different circuits.
14 So one would need to go back and confirm what the
15 voltage at V_2 is for each circuit and what the
16 voltage for V_a , which again seems to be undefined,
17 is at each circuit in order to make a determination
18 as to whether or not they were the same, since they
19 are two different circuits.

20 Q. So in arriving at your opinions regarding
21 Kimura, did you consider what Kimura discloses
22 regarding the voltage V_2 and the voltage V_a ?

23 A. I considered what it discloses. As I said,
24 I'm not sure that it actually defines V_a . I don't
25 think I found that definition.

1 Q. Now, if you can turn to paragraph 253 of
2 Kimura for me. And that's on page 65 of the PDF.

3 A. Okay.

4 Q. This is the beginning of the discussion
5 of -- well, actually, the discussion begins in
6 paragraph 252.

7 Paragraph 252 begins the discussion of the
8 timing diagram we've been looking at in Figure 17B;
9 correct?

10 MR. ANDROS: Objection. Form.

11 THE WITNESS: Paragraph 253 describes
12 aspects of circuit 17A when it operates as shown in
13 17B. Again, you know, this is not intended to
14 describe the operation of Figure 27.

15 BY MR. HERMAN:

16 Q. But it is intended to describe the
17 operation of the circuit shown in 17A; correct?

18 A. Under certain operating conditions, that
19 would be the case. Other figures would operate
20 differently with the same conditions.

21 Q. Now, if you look over in the next column,
22 paragraph 256 describes period D.

23 Do you see that?

24 A. Yes. With respect, again, to the circuit
25 in 17A.

1 Q. And about two-thirds of the way down that
2 paragraph 256, there's a sentence that reads: "In
3 this case, node 13 is in a floating state."

4 Do you see that?

5 A. Yes. Again, this is with respect to
6 node 13 in Figure 17A after the actions described in
7 paragraphs 251 through 256 have taken place.

8 Q. The next sentence reads: "Then, the
9 potential of node 13 is raised by capacitive
10 coupling between the gate of the transistor 203 and
11 the second terminal of the transistor 203."

12 Do you see that?

13 A. I see that.

14 Q. And then Kimura goes on to state:
15 "Accordingly, the potential of the node 13 becomes
16 $V_2 + V_{th203} + V_a$."

17 Do you see that?

18 A. I see that language.

19 Q. So that potential, $V_2 + V_{th203} + V_a$, is the
20 potential in period D that's labeled on that signal
21 line V13 in Figure 17B; true?

22 MR. ANDROS: Objection. Form.

23 THE WITNESS: When 17A is operated as
24 described in 17B, that is how it is labeled, yes.

25 And again, as we mentioned before, I have

1 not found a definition for Va.

2 BY MR. HERMAN:

3 Q. The next thing Kimura states is that:

4 "This is so-called bootstrap operation."

5 Do you see that?

6 A. Yes.

7 Q. So Kimura is identifying $V_2 + V_{th203} + V_a$ as a
8 voltage that's appearing on node 13 as a result of
9 what it calls a bootstrap operation; true?

10 MR. ANDROS: Objection. Form.

11 THE WITNESS: He is describing that as a
12 bootstrap operation. I don't see where he says it's
13 the result of a bootstrap operation. And again,
14 it's limited to Figure 17A.

15 BY MR. HERMAN:

16 Q. So looking back at Figure 21B.

17 A. Okay.

18 Q. Figure 21B shows the node 13 again having a
19 potential of $V_2 + V_{th203} + V_a$ in period D; correct?

20 A. It does, but it needs to be understood in
21 context. That's when the series of operations shown
22 in Figure 21B operate on the circuit in 21A, which
23 also includes following the period C which is
24 different than the period C in Figure 17B. So
25 they're talking about different sequences on

1 different circuits that will lead to a voltage
2 calculated by the same formula.

3 I have not validated whether or not the
4 values of V2 and Va correspond because I don't
5 believe that Dr. Foty relied on that.

6 Q. Now, in arriving at your opinions regarding
7 Figure 21B, have you considered whether node 13 is
8 in a floating state in period D?

9 A. Period D. With respect to Figure 21A?

10 Q. Yes. So the timing diagram in Figure 21B
11 applies to the circuit in Figure 21A; correct?

12 A. It does.

13 Q. So in arriving at your opinions regarding
14 Figure 21B's timing diagram, do you consider whether
15 node 13 in Figure 21A is floating in period D?

16 A. I don't recall. We'd have to go back to
17 the declaration. I don't recall Dr. Foty opining on
18 the value of node 13 in Figure 21A, but I may just
19 not be remembering.

20 Q. And you've offered an opinion that you
21 don't believe that there's any connection between
22 Figure 21B and Figure 27C; true?

23 MR. ANDROS: Objection. Form.

24 THE WITNESS: I have offered the opinion
25 that Dr. Foty hasn't established that Figure 21B is

1 in -- taught in Kimura as applying to 27C.

2 And, in fact, if you go through Dr. Foty's
3 opinion as he stated it, it's very clear that that's
4 flawed and incorrect, that it does not.

5 BY MR. HERMAN:

6 Q. So in arriving at your opinion that there
7 is some sort of flaw in attempting to correlate
8 Figure 21B with Figure 27C, did you consider whether
9 in Figure 21A that node 13 is floating in period D?

10 MR. ANDROS: Objection. Form.

11 THE WITNESS: I don't recall whether I
12 considered it or not, but it wouldn't really have
13 been determinative. What 21B does in 21A doesn't
14 mean that it does the same thing in 27C. I analyzed
15 how the timing diagram in 21B would apply to the
16 circuit in Figure 27C because I believe that is what
17 Dr. Foty alleged was the combination that would
18 render claims obvious.

19 And as I said, it would not operate in a
20 way that Dr. Foty concludes; although, in fact, if
21 you actually look at his declaration, he also
22 observed that it would be a flawed circuit. His own
23 diagram showed that it would cause short circuits
24 and it would cause unpredictable operation.

25 ///

1 BY MR. HERMAN:

2 Q. So my question is whether you determined in
3 part of your -- as part of your analysis whether in
4 Figure 21A that node 13 is floating in period D.

5 Did you make that determination?

6 MR. ANDROS: Objection. Form.

7 THE WITNESS: I don't recall. If that was
8 an allegation that Dr. Foty made, I'd be happy to
9 take a look at it and see if I can find the
10 corresponding portion of my declaration.

11 BY MR. HERMAN:

12 Q. Sitting here today, you don't have a
13 particular portion of your declaration in mind; is
14 that true?

15 MR. ANDROS: Objection. Form.

16 THE WITNESS: I don't believe I directly
17 commented on 21A in my declaration.

18 BY MR. HERMAN:

19 Q. Do you know if the node 13 in Figure 27C is
20 floating in period D?

21 A. It's very difficult to completely analyze
22 what would happen in 27C because, as I mentioned,
23 the way that Dr. Foty mapped it, along with
24 Figure 21B, the circuit would likely become damaged
25 almost immediately in use, and it's hard to predict

1 the way a damaged circuit would behave.

2 But if we -- there is a state -- there is a
3 very short period of time under that hypothetical
4 that Dr. Foty's put forth where node 13 would be
5 floating. But it would very quickly be pulled to
6 the value -- well, it would be pulled to the value
7 of node 211 very quickly, or near the value of
8 node 211.

9 So it would not be floating during period D
10 the way that is described for Figure 21A.

11 Q. I think you just said that in period D,
12 node 13 would be very quickly pulled towards the
13 potential line 211; correct?

14 A. Again, if hypothetically it were stimulated
15 from Figure 21B's input signals and if somehow it
16 managed to survive without damage. By the time you
17 get to period D, if you even follow Dr. Foty's
18 analysis, the circuit would likely be damaged.

19 Q. So you keep using the word "damaged," but I
20 just searched your declaration, and that word does
21 not appear anywhere.

22 Can you direct me to the portion of your
23 declaration where you have offered the opinion
24 regarding the damage to the circuit in Figure 27C?

25 MR. ANDROS: Objection. Form.

1 THE WITNESS: I don't think I used the word
2 "damage." I'm sorry, give me one second. I lost
3 what I was looking at.

4 What I -- I do make the statement that
5 there's really no basis in Kimura for using the
6 timing diagram in 21B with respect to the circuit in
7 27C, but then I also note in paragraph 76 that
8 Dr. Foty hasn't taken into account Kimura's
9 teachings about reducing transistor deterioration.

10 So there I used the word "deterioration"
11 rather than "damage," but that's really the -- the
12 problem is that, if operated in the way that
13 Dr. Foty describes, there's going to be
14 deterioration and eventually damage to some of the
15 transistors. And you can see that in his own
16 descriptions, if I recall correctly, page 82 of his
17 declaration.

18 BY MR. HERMAN:

19 Q. But you don't actually say that using
20 Figure 27C by itself is going to result in any sort
21 of deterioration; true?

22 MR. ANDROS: Objection. Form.

23 THE WITNESS: Using it by itself, it's not
24 operating. It's when it receives the signals from
25 21B which, I don't think Kimura ever intended to

1 have happen or ever suggested should happen. You do
2 get a short-circuit in the operation that Dr. Foty's
3 illustrated, and that's very strong evidence that
4 Kimura never intended the timing diagram in 21B to
5 apply to 27C.

6 BY MR. HERMAN:

7 Q. So what you just said, "short circuit,"
8 that also does not appear anywhere in your
9 declaration; true?

10 A. No. Again, I make the more general
11 statements that I don't see any linkage between 21B
12 and 27C in Kimura, and that are -- also that
13 Dr. Foty hasn't paid attention to the issue of
14 reducing transistor deterioration.

15 Q. But what you are saying now, you have not
16 explained anywhere in your declaration how there
17 would be a short circuit in Figure 27C when operated
18 in the way Dr. Foty explains or why that circuit
19 would deteriorate. Those opinions will not be found
20 in your declaration; true?

21 MR. ANDROS: Objection. Form.

22 THE WITNESS: I think I deal with them
23 generally, but I don't use those specific words.

24 BY MR. HERMAN:

25 Q. There's no discussion of how Figure 27C,

1 when operated in the manner that Dr. Foty explains,
2 will short-circuit, period. That opinion cannot be
3 found anywhere in your declaration; true?

4 MR. ANDROS: Objection. Form.

5 THE WITNESS: I don't recall if I cite to
6 that portion of his testimony or not. I don't have
7 Dr. Foty's declaration in front of me. But again, I
8 think I've made the general point that Figure 21B
9 does not apply to 27C. And among the reasons are
10 the fact that the timing just doesn't work.

11 BY MR. HERMAN:

12 Q. So there is no paragraph in here that
13 explains why Figure 27C, in your declaration there
14 is no paragraph that explains why Figure 27C would
15 short-circuit when you apply the input signals from
16 Figure 21B; true?

17 MR. ANDROS: Objection. Form.

18 THE WITNESS: I say it's not compatible. I
19 don't use the word "short circuit."

20 BY MR. HERMAN:

21 Q. So there's no explanation, in words, as to
22 why a short circuit would occur if the input signals
23 in Figure 21B were applied to the circuit at
24 Figure 27C; correct?

25 MR. ANDROS: Objection. Form.

1 THE WITNESS: Well, I mentioned that there
2 would not be a reasonable expectation of success. I
3 mentioned that it's inapplicable, but I don't go
4 into the detail of what the nature of the damage
5 would be. Again, that's in Dr. Foty's declaration.
6 It's illustrated there.

7 BY MR. HERMAN:

8 Q. So you don't identify any specific damage
9 or any specific short circuit that would occur;
10 true?

11 A. I don't illustrate the specifics of that,
12 no. I simply say it's inapplicable and explain that
13 there's no link. From my perspective, a person of
14 ordinary skill wouldn't even try to use Figure 21B
15 with Figure 27C. And I do explain that. And Kimura
16 doesn't really tell you how to hook it up. And
17 again, I explained that there would not be a
18 reasonable expectation of success, and one of the
19 reasons behind that is the short circuit problem.

20 Q. So what I'm struggling is the word "short
21 circuit" is nowhere to be found in your declaration.
22 The first time I'm hearing it is today.

23 Where did you disclose in your declaration
24 that there would be a short circuit problem? Point
25 me to the paragraph, please.

1 A. No, I've already said I did not
2 specifically use the word "short circuit." I said
3 that there was no motivation or no indication in
4 Kimura to use 21B along with 27C, and that a person
5 of ordinary skill would not do it, and a person of
6 ordinary skill would not expect it to work. So I
7 think that's enough.

8 But since you asked me today, one of the
9 reasons behind that is that this short circuit would
10 happen. That's one of the things that makes it
11 difficult for me to answer some of your other answer
12 questions about what individual nodes would do
13 because it can be challenging to model them after a
14 short circuit.

15 Q. So what period of operation are you talking
16 about right now?

17 MR. ANDROS: Objection to form.

18 THE WITNESS: I'd rather not try to
19 remember it off the top of my head. If we can look
20 at Dr. Foty's declaration, it's illustrated.

21 MR. HERMAN: I think we've been going for
22 about more than an hour, so maybe now is a good time
23 for a five-minute break.

24 THE WITNESS: Okay.

25 THE VIDEOGRAPHER: The time is 10:04 a.m.,

1 and we're going off the record.

2 (Recess.)

3 THE VIDEOGRAPHER: The time is 10:11 a.m.,
4 and we're back on the record.

5 BY MR. HERMAN:

6 Q. Okay, Doctor. If you could turn to
7 paragraph 284 of Kimura, which is on page 68.

8 A. Okay.

9 Q. There, Kimura explains that the
10 semiconductor device in Figure 27A corresponds to a
11 semiconductor device in which the transistors 201 to
12 207 are additionally provided in the semiconductor
13 device in Figure 14A.

14 Do you see that?

15 A. That is what it says.

16 Q. Then in paragraph 286, Kimura explains that
17 the circuit shown in Figure 27C is a modified
18 version of the semiconductor device in Figure 27A;
19 correct?

20 MR. ANDROS: Objection. Form.

21 THE WITNESS: It describes a
22 reconfiguration of transistor 204 in a different
23 way, yes.

24 BY MR. HERMAN:

25 Q. And the reconfiguration is made to

1 Figure 27A; correct?

2 A. It's described with respect to it 27A, yes.

3 Q. Now, if you can turn all the way back to
4 paragraph 93 of Kimura. And that's on page 53.

5 A. Okay.

6 Q. This is the beginning of Kimura's detailed
7 description of the invention; true?

8 A. Yes.

9 Q. And it's before what Kimura identifies as
10 Embodiment 1; correct?

11 A. Correct.

12 Q. Now at the end of that paragraph 93, Kimura
13 states: "Note that in the structures described
14 below, the same portions or portions having similar
15 functions are denoted by common reference numerals
16 in different drawings and description thereof is not
17 repeated."

18 Correct?

19 A. It does say that, yes.

20 Q. Now, Figure 14A in Kimura is the start for
21 the first figure of what Kimura identifies as its
22 second embodiment; true?

23 A. I have to look.

24 Second embodiment starts by describing 14A.

25 Q. Now, Figures 27C and 27A are also part of

1 the second embodiment of Kimura; correct?

2 MR. ANDROS: Objection. Form.

3 THE WITNESS: They are described that way,
4 but they are clearly different circuits.

5 BY MR. HERMAN:

6 Q. Now, Figure 14A of Kimura, the circuit
7 that's shown there, it includes transistors 101 to
8 105 and a transistor 201; correct?

9 A. Correct.

10 Q. Now, Figures 27A through 27C all also
11 include transistors labeled with those same
12 reference numerals, 101 through 105 and 201; true?

13 A. Yes, as well as other transistors.

14 Q. Now, if you situate yourself at Figure 14A
15 of Kimura, which is on page 15.

16 A. Okay.

17 Q. Now, if you start scrolling down through
18 the figures eventually you'll reach a Figure 16A.

19 A. Okay.

20 Q. And the transistor that's identified with
21 the reference numeral 202 appears in Figure 16A;
22 correct?

23 A. It does.

24 Q. And that transistor was not in 14A but it
25 is in 16A; correct?

1 A. Yes.

2 Q. Figures 27A through C all also include a
3 transistor that is labeled with the reference
4 numeral 202; correct?

5 A. Yes, although the operation needs to be
6 independently analyzed because of the other
7 transistors.

8 Q. Now if we move down to Figure 17A of
9 Kimura.

10 Figure 17A includes a transistor that's
11 labeled with the numeral 203; correct?

12 A. Yes.

13 Q. And Figures 27A through C also include a
14 transistor that's labeled with the reference numeral
15 203; true?

16 A. Yes, but the input circuit is different.

17 Q. Now if we turn down to Figure 21 -- sorry,
18 20A.

19 Figure 20A adds a transistor that's labeled
20 with the reference numeral 204; correct?

21 MR. ANDROS: Objection. Form.

22 THE WITNESS: 20A does have a transistor
23 labeled 204.

24 BY MR. HERMAN:

25 Q. And Figures 27A through 27C all also

1 include a transistor labeled with the reference
2 numeral 204; true?

3 A. Yes, but connected in some cases in
4 different ways to different nodes and with different
5 inputs.

6 Q. Now, Figure 21A has a transistor that's
7 labeled with the reference numeral 205; correct?

8 A. Yes.

9 Q. And Figures 27A through 27C also include
10 the transistor that's labeled with the same
11 reference numeral 205; true?

12 MR. ANDROS: Objection. Form.

13 THE WITNESS: There is also a transistor
14 205 in 27A through C, but it's paralleled by a
15 transistor 206.

16 BY MR. HERMAN:

17 Q. Now if we turn down to Figure 23A in
18 Kimura.

19 Figure 23A adds that paralleled transistor
20 206 that you've just referred to; true?

21 A. It does, but with different circuits in the
22 output than Figure 27, for example.

23 Q. So Figure 27A through 27C include a
24 transistor that's labeled with the same reference
25 numeral 206 as used in Figure 23A; true?

1 A. There is a transistor 206, but as I noted,
2 its output is connected to a different circuit.

3 Q. Figure 25A of Kimura adds a transistor that
4 is labeled with the reference numeral 207; correct?

5 A. Yes.

6 Q. And Figures 27A through 27C also include a
7 transistor that's labeled with the same reference
8 numeral 207; true?

9 A. They also contain a transistor labeled 207,
10 but it connects to a differently configured node 13.

11 Q. Now, some of the circuits that you assess
12 in your declaration include capacitors; is that
13 right?

14 MR. ANDROS: Objection.

15 THE WITNESS: Across the entire
16 declaration, that is true. Some circuits do.

17 BY MR. HERMAN:

18 Q. How to you charge a capacitor?

19 MR. ANDROS: Objection. Form.

20 THE WITNESS: There are a variety of ways
21 to charge a capacitor, but generally a capacitor
22 will charge when there is a current input to the
23 capacitor, and usually that is caused by a voltage
24 differential between the two terminals of the
25 capacitor.

1 BY MR. HERMAN:

2 Q. Does the potential difference between the
3 two terminals attached to the capacitor's respective
4 plates affect the amount of charge the capacitor
5 accumulates?

6 MR. ANDROS: Objection. Form.

7 THE WITNESS: We don't usually describe it
8 that way. We usually describe it as reflecting the
9 amount of charge that the capacitor has accumulated.

10 BY MR. HERMAN:

11 Q. Do you know approximately how many
12 transistors can fit into a square millimeter of
13 space using today's available process technology?

14 MR. ANDROS: Objection. Form.

15 THE WITNESS: Depends what that process is
16 and what substrate you're building it on.

17 BY MR. HERMAN:

18 Q. Say a standard silicone substrate. What is
19 the maximum number of transistors you could fit into
20 a square millimeter of space on a silicone
21 substrate?

22 MR. ANDROS: Objection. Form.

23 THE WITNESS: I'd have to do the math, but
24 on certain semiconductor processes I would guess
25 that it's more than a million.

1 BY MR. HERMAN:

2 Q. How about in 2012? Do you know how many
3 transistors could fit into a square millimeter of
4 space using existing process technology on a
5 silicone substrate in 2012?

6 MR. ANDROS: Objection. Form.

7 THE WITNESS: Again, it depends on the
8 specific process and the specific silicone
9 substrate. Not all silicone substrates are suitable
10 for all devices. But on a high-performance
11 microprocessor, for example, let's see, in 2012 it
12 still could've been over a million.

13 BY MR. HERMAN:

14 Q. So it's over million transistors per square
15 millimeter in 2012, at least from an order of
16 magnitude perspective; is that true?

17 MR. ANDROS: Objection. Form.

18 THE WITNESS: For certain kinds of
19 semiconductor processes that are suitable for
20 certain kinds of devices. There's a wide range.
21 There would be other kinds of manufacturing
22 processes where it would be tens of transistors per
23 square millimeter.

24 MR. HERMAN: So I'm going to put one more
25 exhibit into the chat here. Just give me a moment.

1 (Exhibit 2046 was previously marked by the
2 Certified Shorthand Reporter, and a copy is
3 attached hereto.)

4 BY MR. HERMAN:

5 Q. Let me know when you have that.

6 A. Okay. I have it.

7 Q. This document has been previously
8 designated Exhibit 2046, and it's entitled "Claim
9 Chart: AMOLED Display in Mengtor Product."

10 Do you see that?

11 A. Yes.

12 Q. Did you prepare this document?

13 A. I did, but based on some other documents
14 that -- well, in this case, yeah, it was based on
15 evidence that other people helped to gather and that
16 I reviewed.

17 Q. So if you could turn to page 4 for me.

18 A. Okay.

19 Q. There's a circuit diagram that's there?

20 A. Yes.

21 Q. So that circuit is different from what's
22 shown in Figure 3 of the '593 patent; true?

23 MR. ANDROS: Objection to form.

24 THE WITNESS: Let me pull it up.

25 It is substantially the same, but there is

1 a difference.

2 BY MR. HERMAN:

3 Q. That difference is that there is an extra
4 transistor, T8, in what's shown on page 4 of
5 Exhibit 2046 that's not present in Figure 3;
6 correct?

7 A. It's not present in Figure 3 of the '593
8 patent, correct.

9 Q. So what's shown on page 4 includes one
10 extra transistor in the stage circuit; true?

11 A. Correct, as compared to Figure 3 in the
12 '593 patent.

13 Q. Now, if you could turn down to page 8 of
14 the same document.

15 On page 8 you're discussing the claim
16 limitation related to the first driver?

17 A. Yes.

18 Q. And you identify transistors T1, T2, and T3
19 as the transistors making up the first driver;
20 correct?

21 A. Yes.

22 Q. If you turn up one page to page 7, you've
23 got a color-annotated version of the circuit that
24 we've been talking about?

25 A. Yes.

1 Q. And in that color-annotated version of the
2 circuit, transistors T1, T2, and T3 output to the
3 line that you've colored in blue, at least in the
4 first instance; correct?

5 MR. ANDROS: Object to form.

6 THE WITNESS: They do supply a signal to
7 the blue line.

8 BY MR. HERMAN:

9 Q. Now, the transistor T5 in that same
10 diagram, that transistor determines whether the
11 signal labeled IN3 makes its way to what's labeled
12 OUT1; correct?

13 MR. ANDROS: Objection. Form.

14 THE WITNESS: Yes, at certain points in
15 operation it does.

16 BY MR. HERMAN:

17 Q. And the line you've annotated in green is
18 connected to that transistor T5's gate; correct?

19 A. Yes.

20 Q. And this diagram shows a transistor T8
21 between what you've colored blue and green; correct?

22 A. Yes.

23 Q. Now, if that transistor T8 is off, the
24 output of transistors T1, T2, and T3 will not be
25 provided to the gate of transistor T5; correct?

1 MR. ANDROS: Objection. Form.

2 THE WITNESS: As a hypothetical, but the
3 way it's wired, that transistor's never turned off
4 when T1, T2, and T3 are trying to provide a signal
5 to T5.

6 BY MR. HERMAN:

7 Q. But if it is off, right, that signal of T1,
8 T2, and T3 will not make its way to T5; true?

9 MR. ANDROS: Object to form.

10 THE WITNESS: If it's operating as
11 designed, that should never happen when T1, T2, and
12 T3 are trying to provide a signal. I suppose that
13 you could damage T8 or something and it could turn
14 off, and in that case the circuit would not be
15 operational.

16 BY MR. HERMAN:

17 Q. So if T1 -- sorry.

18 So if T8 were off for some reason, then the
19 output of T1, T2, and T3 would not make it to the
20 gate of transistor T5; correct?

21 MR. ANDROS: Object to form.

22 THE WITNESS: It would depend why it's off.
23 Again, in normal operation, the way it's designed,
24 when T1, T2, and T3 are trying to provide a signal,
25 T8 is on. If it were off, it would depend on the

1 reason it's off and whether or not it's off because
2 it's short-circuited or whether it's off because
3 it's open.

4 BY MR. HERMAN:

5 Q. And --

6 A. It wouldn't be off under normal conditions.

7 Q. Sorry. Let me know when you're done.

8 A. I'm done.

9 Q. So there would always be some sort of
10 potential on that path that you've labeled as blue;
11 correct?

12 MR. ANDROS: Object to form.

13 THE WITNESS: There is always some
14 potential on any node, yeah.

15 BY MR. HERMAN:

16 Q. And that potential will make its way to the
17 path you've labeled green if T8 is open; correct?

18 MR. ANDROS: Object to form.

19 THE WITNESS: You're saying if T8 is open,
20 will the blue connect to the green?

21 BY MR. HERMAN:

22 Q. Yes.

23 A. Not if it's open, but again, the design is
24 set so that T8 is connected to a signal that is
25 intended to turn it on. So during all the times in

1 which the signals are supposed to flow through T8,
2 it's on. There's not really a control on it. It's
3 just tied to a -- to a constant value that's
4 intended to keep it on.

5 Q. So I think I used the word -- the wrong
6 word there.

7 So when transistor 8 is on, the blue
8 potential would be the same as the green potential;
9 correct?

10 MR. ANDROS: Object to form.

11 THE WITNESS: Substantially the same, yes.

12 BY MR. HERMAN:

13 Q. But when transistor T8 is off, that will
14 not necessarily be the case; correct?

15 MR. ANDROS: Object to form.

16 THE WITNESS: Again, hypothetically that's
17 true, but T8's not intended to be off in normal
18 operation. T8 is intended to be on whenever T1, T2,
19 and T3 are trying to drive a signal through T8.

20 MR. HERMAN: I don't have any further
21 questions.

22 MR. ANDROS: Can we take -- go off the
23 record.

24 THE VIDEOGRAPHER: The time is 10:32 a.m.,
25 and we're going off the record.

1 (Recess.)

2 THE VIDEOGRAPHER: The time is 10:39 a.m.,
3 and we're back on the record.

4 MR. ANDROS: I have no questions.

5 So, Dr. Wolfe, thank you for your time.

6 MR. HERMAN: Thank you, Dr. Wolfe.

7 THE WITNESS: Thanks.

8 THE VIDEOGRAPHER: The time is 10:48 a.m.,
9 and this concludes today's deposition.

10 (Deposition concluded at 10:48 p.m.)

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DECLARATION UNDER PENALTY OF PERJURY

I hereby declare under penalty of perjury
that the foregoing is my deposition under oath; that
I have read same; and that I have made the
corrections, additions, or changes to my answers
that I deem necessary.

In witness thereof, I hereby subscribe my
name this day of , 2025.

DR. ANDREW WOLFE, PH.D.

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