

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MIANYANG BOE OPTOELECTRONICS TECHNOLOGY CO., LTD.;
WUHAN CHINA STAR OPTOELECTRONICS SEMICONDUCTOR DISPLAY
TECHNOLOGY CO., LTD.; TIANMA MICROELECTRONICS CO., LTD.;
AND VISIONOX TECHNOLOGY, INC.,
Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.
Patent Owner.

Case IPR2024-00620
U.S. Patent No. 9,330,593

PATENT OWNER'S SUR-REPLY

TABLE OF CONTENTS

I.	Introduction.....	1
II.	Petitioner Fails to Show a <i>Prima Facie</i> Case of Obviousness.....	2
A.	Kimura Does Not Render Obvious Any Challenged Claim	2
1.	Kimura Does Not Teach or Suggest Claim Elements [1-D]/[15-G]	8
2.	Kimura Does Not Teach or Suggest Claim Elements [1-A]/[15-D] and [6-B]/[20-B]	9
3.	Kimura Does Not Teach or Suggest Claim Elements [7-C]/[21-C] and [7-D]/[21-D]	12
4.	Kimura Does Not Teach or Suggest Claim Elements [8-A]/[22-A] and [8-B]/[22-B]	13
5.	Petitioner’s and Dr. Foty’s Misapplication of Kimura’s Teachings	14
B.	Shin in View of Sasaki Does Not Render Obvious Any Challenged Claim.....	16
C.	Tobita Does Not Render Obvious Any Challenged Claim.....	18
III.	Objective Indicia.....	21
IV.	Conclusion	24

PATENT OWNER'S EXHIBIT LIST

Exhibit	Description
Ex. 2001	Order Amending Schedule, Inv. No. 337-TA-1351
Ex. 2002	Notice of Prior Art, Inv. No. 337-TA-1351
Ex. 2003	Westlaw Company Investigator Report for Mianyang BOE
Ex. 2004	Assignment for U.S. Patent Application No. 15/031,174
Ex. 2005	Assignment for U.S. Patent Application No. 15/031,174
Ex. 2006	Assignment for U.S. Patent Application No. 16/097,538
Ex. 2007	Assignment for U.S. Patent Application No. 15/562,853
Ex. 2008	Assignment for U.S. Patent Application No. 16/968,978
Ex. 2009	Assignment for U.S. Patent Application No. 16/622,918
Ex. 2010	Westlaw Company Investigator Report for TCL Technology Group
Ex. 2011	Westlaw Company Investigator Report for China Star Wuhan
Ex. 2012	May 18, 2017 References Cited by Examiner for U.S. Patent Application No. 15/031,174
Ex. 2013	March 12, 2019 References Cited by Examiner for U.S. Patent Application No. 15/562,853
Ex. 2014	February 2, 2023 References Cited by Examiner for U.S. Patent Application No. 16/968,978
Ex. 2015	May 4, 2022 References Cited by Examiner for U.S. Patent Application No. 16/622,918
Ex. 2016	May 14, 2020 References Cited by Examiner for U.S. Patent Application No. 16/097,538
Ex. 2017	U.S. Patent No. 9,236,377

Exhibit	Description
Ex. 2018	Claim Construction Order, Inv. No. 337-TA-1351
Ex. 2019	Declaration of Dr. Andrew Wolfe, Ph.D. (in support of Patent Owner Preliminary Response)
Ex. 2020	Notice of Allowance for U.S. Patent No. 9,330,593
Ex. 2021	Curriculum Vitae of Andrew Wolfe, Ph.D.
Ex. 2022	Declaration of Derek Andros
Ex. 2023	Declaration of Jared Frisch
Ex. 2024	Teardown Photos of Samsung Galaxy S22Ultra Product
Ex. 2025	Teardown Photos of MobileSentry Product
Ex. 2026	Teardown Photos of Mengtor Product
Ex. 2027	Teardown Photos of Phone LCD Parts Product
Ex. 2028	Teardown Photos of Mobile Defenders Product
Ex. 2029	Teardown Photos of Injured Gadgets Product
Ex. 2030	Teardown Photos of Gadgetfix Product
Ex. 2031	Teardown Photos of Group Vertical Product
Ex. 2032	Teardown Photos of eTech Parts Plus Product
Ex. 2033	Teardown Photos of Parts4Cells Product
Ex. 2034	Teardown Photos of SEGMobile Product
Ex. 2035	Teardown Photos of Captain Mobile Parts Product
Ex. 2036	Teardown Photos of Repairs Universe Product
Ex. 2037	Teardown Photos of Sourcely Plus Product
Ex. 2038	Teardown Photos of Fixez Product

Exhibit	Description
Ex. 2039	Teardown Photos of Wholesale Gadget Parts Product
Ex. 2040	Teardown Photos of Parts4LCD Product
Ex. 2041	Teardown Photos of DFW Cellphone and Parts Product
Ex. 2042	Declaration of Aris Silzars, Ph.D.
Ex. 2043	Declaration of Adam Fontecchio, Ph.D.
Ex. 2044	[PROTECTIVE ORDER MATERIAL – NCT INFORMATION] Declaration of Kwangsae Lee
Ex. 2045	<i>Samsung Display Co., Ltd. v. BOE Tech. Co., Ltd. et al.</i> , Case No. 2-23-cv-00309, Compl. (E.D. Tex. June 26, 2023).
Ex. 2046	Mengtor AMOLED Display Claim Chart
Ex. 2047	[PROTECTIVE ORDER MATERIAL – NCT INFORMATION] Declaration of Hwan-Soo Jang
Ex. 2048	[PROTECTIVE ORDER MATERIAL – NCT INFORMATION] PowerPoint Presentation Drafted by Hwan-Soo Jang
Ex. 2049	Jason Gutierrez, <i>CES is over – where are the bezel-less phones?</i> , Android Authority (2013)
Ex. 2050	Jin Huh, <i>A New Small Sized Integrated Scan & Emission Driver for Compact AMOLED Displays</i> , SID 2012 Digest (2012)
Ex. 2051	United States Patent Application Publication No. 2013/0169609
Ex. 2052	United States Patent No. 9,620,061
Ex. 2053	United States Patent No. 11,227,549
Ex. 2054	Suzanne Kantra, <i>Review of the Samsung Galaxy S4</i> , Techlicious (2013)

Exhibit	Description
Ex. 2055	Tony Fletcher, <i>Samsung Galaxy S4 announced and here's the photos, specs and videos</i> , WireFresh (2013)
Ex. 2056	Chuong Nguyen, <i>Samsung Galaxy S4 Review</i> , GottaBeMobile (2013)
Ex. 2057	[PROTECTIVE ORDER MATERIAL – NCT INFORMATION] Samsung Galaxy S22Ultra AMOLED Display Claim Chart
Ex. 2058	[PROTECTIVE ORDER MATERIAL – NCT INFORMATION] Samsung Display Galaxy S22Ultra Circuit PDR (including certified English translation)
Ex. 2059	[PROTECTIVE ORDER MATERIAL – NCT INFORMATION] Declaration of Dr. Andrew Wolfe, Ph.D. in Support of Patent Owner Response
Ex. 2060	Transcript of December 5, 2024 Deposition of Daniel Foty, Ph.D. (Rough) (redacted)
Ex. 2061	Transcript of June 24, 2024 Deposition of Daniel Foty, Ph.D. (redacted)
Ex. 2062	Transcript of April 4, 2025 Deposition of Daniel Foty, Ph.D.
Ex. 2063 ¹	Transcript of December 5, 2024 Deposition of Daniel Foty, Ph.D. (redacted)

¹ Ex. 2063 is the finalized version of Exhibit 2060, which was filed along with Patent Owner's Response.

I. Introduction

The Petition's obviousness theories suffer from significant defects, as identified by the Board in the Institution Decision and further developed by Patent Owner in the Patent Owner Response supported by the expert declaration of Dr. Wolfe. In its Reply, Petitioner now attempts to change theories from those presented in the Petition. Petitioner's attempts to inject new theories in Reply, which were not presented in its Petition, should be rejected as improper new argument. In any event, even Petitioner's new theories fail to address the fundamental problems in the Petition's theories. If anything, Petitioner's shifting sands approach underscores the nonobviousness of the challenged claims

For example, regarding the Kimura grounds, the Petition wrongly relied on a timing diagram as describing the operation of a circuit when there was a clear discrepancy between that circuit and timing diagram, demonstrating that the timing diagram did not describe that circuit's operation. After the Board noted this discrepancy, DI 25-26, Petitioner now claims that it is not relying on the timing diagram as set forth in Kimura, but purportedly is relying on only a select portion of the timing diagram. To so argue, Petitioner's Reply attempts to manufacture a purported distinction between "input signals" and "internal node voltages." Not only is this unsupported by Kimura's teachings, but Petitioner's expert admitted during deposition that no such distinction exists. In fact, Kimura teaches that the voltage of

node 13 serves as both an “internal node voltage” and an “input signal.” Ex. 2062 (Foty), 32:12-20; Kimura, ¶[0249].

Petitioner’s arguments regarding the Shin/Sasaki and Tobita grounds fare no better. Regarding Shin/Sasaki, Petitioner largely posits the same unsupported, speculative concerns to try to justify adding two additional, entirely extraneous transistors to Shin’s circuitry, when Shin expressly taught that the purported problem of reversal Petitioner identifies was already addressed by its capacitor C1. Regarding Tobita, Patent Owner in its Response identified a fundamental, and fatal, problem with the Petition’s theories. Petitioner now tries to advance a new and different argument, which it fails to adequately explain, let alone show how each element of the claim is allegedly met thereunder. Petitioner’s new argument should be rejected.

II. Petitioner Fails to Show a *Prima Facie* Case of Obviousness

A. Kimura Does Not Render Obvious Any Challenged Claim

As Patent Owner previously explained, while Petitioner purports to base its analysis on the Figure 27C circuit of Kimura, its analysis relies on portions of Kimura directed to different circuits and configurations. *See* POR 7-14. Petitioner does this in an attempt to arrive at the requirements of the challenged claims. *Id.* In the Institution Decision, the Board agreed with Patent Owner that “Petitioner cites Kimura’s description of different circuits, i.e., the circuits in Figures 18A, 19A, and 19B, to show how the circuit of Figure 27C works in operation as part of its analysis,”

and that Petitioner and its expert “do not explain sufficiently why a different arrangement of such components would yield the same results.” DI 25.

Petitioner and its expert still fail to do so. Petitioner now asserts that all of the various figures of Kimura it cites should be considered together. Reply 1. But each of these figures reflects a different circuit, often with different circuit elements, different internal connections, and different input signals. *See* Ex. 2059 (Wolfe), ¶¶46-48. Petitioner creates a complicated flow chart with nine different figures across multiple embodiments to purportedly show how different transistors could be added to various circuits of Kimura, and asserts based on this complex chart of its making that all of these figures are “related, additive, and intended for us together.” Reply, 5-6. This is incorrect. Notably, Petitioner points to nothing in Kimura’s disclosure in support of that assertion. Moreover, Petitioner’s expert admitted that he simply *assumes* each of Kimura’s circuits will operate in the same way on the basis that they are all stage circuits and “intended to basically do the same sort of thing.” Ex. 2063, 37:16-38:3.

Petitioner and its expert also fail to fully consider, let alone adequately explain, how the Figure 27C circuit, with its different arrangement of additional transistors, internal connections, and input signals would operate. Ex. 2059 (Wolfe Dec.), ¶¶46-48. Petitioner now admits that “internal node voltages” will differ based on changes

to a given circuit, yet points to nothing to explain the impact of these changes in the Figure 27C circuit. Reply, 8.

Additionally, Petitioner disregards that each of the additional transistors it identifies in its flow chart is disclosed by Kimura to have various “alternative” functions, and Kimura explains that these transistors do not need to implement each possible function. *See, e.g.*, Ex. 1004, ¶[0222] (listing alternative functions for transistor 201 and stating that “transistor 201 does not need to have all of the above functions.”); *id.*, ¶[0246] (transistor 202); *id.*, ¶[0250] (transistor 203); *id.*, ¶[0262] (transistor 204); *id.*, ¶[0268] (transistor 205); *id.*, ¶[0272] (transistor 206); *id.*, ¶[0280] (transistor 207). Petitioner fails to explain which of these alternative functions it alleges would be implemented for each transistor in the Figure 27C circuit, let alone why or how a POSITA would implement them. Moreover, Kimura never states or discusses how these alternative functions could interoperate with other transistors and their alternative functions.

Petitioner’s expert admitted during deposition that whether a given transistor would implement a particular function would depend on the specific circuit configuration, including the types of input signals provided to the circuit. Ex. 2062 (Foty), 46:11-15 (“what Kimura is saying here is that functionality provided would depend on the exact nature of signals that are being provided.”). Yet he also acknowledged that in analyzing Kimura, he did not consider the factors that would

determine which of the alternative functions a particular transistor would perform. *Id.* (“I didn’t consider this in my analysis, this level of detail.”). Petitioner fails to consider, let alone explain, any of these critical issues of circuit design and operation in its unsupported assertion that the figures of Kimura are somehow all “related, additive, and intended for us together.” Reply 6.

Petitioner’s misapplication of Kimura’s teachings is further underscored by its shifting theories as to the timing diagram of Figure 21B. As Patent Owner previously explained, contrary to the Petition’s theory, Kimura’s description of the Figure 27C circuit is not compatible with the timings shown in Figure 21B. POR 13-15. In the Institution Decision, the Board noted that “Petitioner’s analysis includes inconsistencies that are not sufficiently explained,” and that these inconsistencies “undermine Petitioner’s argument that ‘the device of Figure 27C...would (or at least obviously could) be supplied with input signals in the same manner and with the same timing’ as the Figure 21B timings. DI 25-26.

Petitioner has no substantive response to the showing of these inconsistencies, which undermine the Petition’s theory. Instead, Petitioner now shifts to a contention that it only relies on a *portion* of Figure 21B, and does not rely on the portion of Figure 21B showing “internal node voltages.” Reply 6. As an initial matter, the Petition did not purport to disclaim any portion of Figure 21B. *See, e.g.*, Pet. 19. This a new theory. Moreover, Petitioner’s attempt now to pick and choose portions of

Figure 21B on which to rely (in response to the critical discrepancy noted by Patent Owner and credited by the Board) is unavailing for at least three additional reasons.

First, Petitioner's attempt to distinguish between "input signals" and "internal node voltages" is inconsistent with Kimura's disclosures. For example, Kimura teaches that the voltage of node 13 may be used as an input signal. Kimura, ¶[0249] ("Therefore, a potential of the node 13 (V_{13}) can be used as the signal IN3."). Thus, in the context of Kimura's timing diagrams, Petitioner's manufactured distinction between "input signals" and "internal node voltages" is unfounded. Indeed, while Petitioner's expert asserts in his reply declaration that "the voltage at node 13 is *not* an input signal to circuitry" with respect to the Figure 20A circuit, Ex. 1025, ¶37, he admitted during deposition that this was incorrect:

Q. And so again, we've got node 13 as the signal IN3 connected to the gate of the transistor 102. Is that right?

A. Kimura so identifies it, yes.

Q. So the voltage at that node is an input signal to this Figure 20A. Correct?

A. Kimura describes using it to receive that input signal to that wiring 13, yes.

Ex. 2062, 32:12-20. And as he explained in his declaration, "the potential (i.e., the voltage) at node 13 will *differ* across the circuit embodiments." Ex. 1025, ¶37 (emphasis added).

Second, while Petitioner argues that “input signals” are the “same” between Kimura’s timing diagrams, Petitioner actually points to only a subset of two signals, IN1 and IN2, which it contends are the same in certain timing diagrams. Reply 7. But Petitioner overlooks that there are additional input signals reflected in these timing diagrams that are *not* the same between these figures. *See, e.g.*, Kimura, Fig. 15A (including signal IN3), 21B (including signal IN4), Fig. 25B (including signal IN5). As Petitioner’s expert acknowledged, these additional input signals are not included in the various additional timing diagrams Petitioner now seeks to rely upon. Ex. 2062, 54:3-55:10. Thus, contrary to Petitioner’s assertions, even arbitrarily limiting to just “input signals,” the timing diagrams Petitioner identifies are not the “same.” Petitioner points to nothing in Kimura to support its bare assertion that each of these input signals would somehow be combined in, and apply to, the Figure 27C circuit, let alone explain how the Figure 21B timings would or should apply to that circuit. Reply 8.

Finally, Petitioner argues that the inconsistency between Figure 21B’s timings and Kimura’s disclosures regarding Figure 27C is irrelevant because Figure 27C is “meant only to adjust circuit operation in period D.” Reply 11. This is entirely unfounded. While Petitioner cites to Kimura ¶[0286] as the purported support for this new argument, that paragraph does not support Petitioner’s assertion. That paragraph of Kimura states simply that “in a period D, the potential of the node 13

can be lowered.” Kimura ¶[0286]. Nothing in that paragraph or the remainder of Kimura’s disclosure states that Figure 27C is “meant only to adjust circuit operation in period D.” Petitioner also cites to a lengthy new discussion of “bootstrapping” in Dr. Foty’s reply declaration. Reply 10 (citing Ex. 1025, ¶¶67-73, 11-26). Included in this new discussion is a Petitioner-modified version of Figure 21B with a modified value for node 13 during period D. Reply 10. This modified Figure, including the modified value for node 13, is based entirely on Dr. Foty’s unsubstantiated new speculation, and finds no support in Kimura’s disclosure.

1. Kimura Does Not Teach or Suggest Claim Elements [1-D]/[15-G]

As Patent Owner previously explained, Petitioner is inconsistent with its application of Kimura’s teachings, and specifically fails to take into account the discrepancy between Kimura’s teachings regarding transistor 204 and the timing diagram on which Petitioner relies. POR 14-16.

In particular, Petitioner must rely on transistor 204 as the claimed transistor in the “first driver,” because it is the only transistor in Figure 27C that, according to Petitioner, has its “on/off operation” “directly control[led]” by the “signal of the third input terminal,” as these claim elements require. Pet. 24. However, the claimed first driver must also control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal, as set forth in claim elements [1-B]/[15-E]. POR 15. For these

requirements, Petitioner also relies on transistor 204, and Kimura's discussion of lowering the potential of node 13. POR 14-16. However, Kimura's discussion of *lowering* the potential of node 13 is inconsistent with the Figure 21B timing diagram on which Petitioner relies, and nothing in Kimura suggests that this "lowering" would meet the requirement of the claims that the first driver "control[s] the voltage of the second node in accordance with" the signal of the third input terminal. Ex. 2059, ¶55.

Petitioner continues to fail to account for this inconsistency in its Reply. It cites to disclosures in Kimura relating to an *increased* potential of node 13 shown in certain figures, but the pertinent disclosures relating to the Figure 27C circuit describe *lowering* that potential. Reply 12 (citing Kimura, [0250]; Figs. 17B, 21B, 25B); see also Kimura, [0286]. Petitioner's arguments fail for the same reasons previously discussed, including with respect to the unexplained inconsistencies between Kimura's discussion of Figure 27C and the timings of Figure 21B.

2. Kimura Does Not Teach or Suggest Claim Elements [1-A]/[15-D] and [6-B]/[20-B]

As Patent Owner explained in its response, Petitioner takes inconsistent positions as between its analysis of independent claims 1 and 15, and dependent claims 6 and 20; specifically, analyzing the same Kimura circuit, between these two sets of claims Petitioner identifies different sets of transistors as purportedly being the claimed "outputting unit" and "first driver." See POR 16-23. Petitioner provides

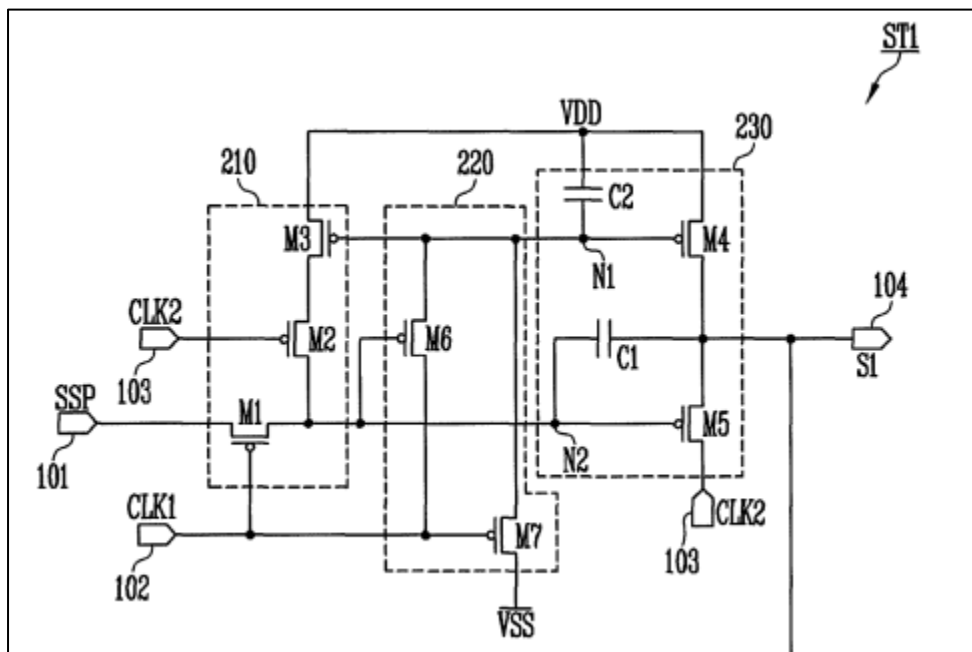
no explanation for its changed analysis. None exists other than Petitioner's hindsight-based attempt to shift its reading of the circuit in order to arrive at claims 6 and 20. Moreover, Petitioner fails to provide any analysis or explanation as to how its different analysis and identification of circuit elements for the dependent claims would apply back to the independent claims. POR 21.

In reply, Petitioner now argues that transistor 201 is part of both the first driver, as well as the outputting unit. *See, e.g.*, Reply 13 (“the Petition’s discussion of claims 6 and 20 simply recognizes the new, dual role played by transistor 201 when Figure 31B is combined with Figure 27C.”). This new argument should be rejected, as the Petition unambiguously identified transistors 208 and 209 as the outputting unit, and transistor 201 as part of the first driver. Pet. 30 (“transistors 208 and 209 now form the device’s outputting unit.”); *id.* at 30 (“The first driver, however, has expanded to include transistor 201.”).

Further, this new argument is inconsistent with Kimura’s teachings. While Petitioner argues that transistor 201 “now controls provision of the line 115 signal to the gate of added output transistor 208 (making it part of the ‘first driver’ *for output line 214*),” Reply at 13, line 214 is *not* an output line, but instead provides the separate signal SOUT as a start pulse to a different stage circuit. As Petitioner acknowledges, “the signal SOUT is not output to the wiring 211 but can be input to a semiconductor device in a different stage as a start pulse.” Kimura ¶[0304].

Petitioner acknowledges that the SOUT signal is a “different” signal than GOUT. Pet. 29. It is instead GOUT that is output to the scan lines that provide scan signals to the rows of pixel circuits. Kimura, ¶[0304]; Pet. 29; POR 19-22. Petitioner implicitly acknowledges this distinction in describing wiring 214 as “a further output line that reduces ‘delay or distortion’ when a shift register output signal from one stage is passed along to the next stage.” Reply 14-15.

As Patent Owner explained, the ’593 Patent makes clear that the “output terminal” provides an output scan signal to the pixel circuits via scan lines. For example, as shown in Figure 3, the output terminal 104 connects to the scan lines Sn, which provide output scan signals to the pixel circuits.



’593 Patent, Fig. 3 (excerpted); *see also, e.g., id.* Fig. 1. This is further illustrated by the language of claim 15, which recites “a scan driver for supplying scan signals to

the pixels through the scan lines, the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals.” Thus, the “output terminal” connects the stage circuits to scan lines that are connected to the pixel circuits. *See also, e.g.,* ’593 Patent, 7:46-48; *id.*, 8:15-17.

3. Kimura Does Not Teach or Suggest Claim Elements [7-C]/[21-C] and [7-D]/[21-D]

The Figure 27C circuit, on which Petitioner relies for independent claims 1 and 15, does not include any capacitors, let alone capacitors in the alleged “outputting unit.” POR 23-24. Petitioner thus must seek to add two capacitors to Figure 27C to arrive at the requirements of claims 7 and 21. There is, however, no reason for adding two capacitors. Petitioner’s bare assertion that “[c]apacitors can be added in various places” belies the hindsight-driven theory the Petition advances for these claims. Pet. 32; Ex. 2059, ¶¶73-75.

In reply, Petitioner argues that “Kimura states that ‘capacitors can be additionally provided without elimination of transistors.” Reply 16 (citing Kimura ¶[0198]). Petitioner asserts that Kimura “does not limit this to any particular embodiment,” but that is incorrect. This disclosure unambiguously relates to figures of Kimura’s Embodiment One, *not* Embodiment Two of which Figure 27C is part. Kimura ¶[0198] (“In the structures illustrated in FIG. 1A, FIGS. 6A to 6F, FIGS. 7A to 7E, FIGS. 8A to 8F, FIGS. 9A and 9B, and FIGS. 11A and 11B, the transistors

can be replaced with capacitors.”); *see also, e.g.*, ¶¶[0046]-[0056] (listing Figs. 1A-6D, 6A-6F, 7A-7E, 8A-8F, 9A-9H, and 11A-11F as part of “Embodiment 1”). Petitioner points to nothing to suggest that this generalized assertion should be applied to Figure 27C.

Additionally, Petitioner’s bare suggestion that various capacitors “can” be added overlooks the significant detriments that would be incurred by adding two capacitors to a stage circuit. Petitioner also overlooks that “obviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.” *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015). As Dr. Wolfe explains, capacitors take up significant circuit area, and this, along with the necessary connections to other circuit elements would need to be taken into account in designing a modified stage circuit. Ex. 2059, ¶78.

4. Kimura Does Not Teach or Suggest Claim Elements [8-A]/[22-A] and [8-B]/[22-B]

Petitioner concedes that “none of Figure 27C’s transistors are connected in the way the claim requires,” and proposes modifications to Figure 27C in order to arrive at the requirements of claims 8 and 22. Patent Owner noted in its Response that, unlike the modifications Petitioner must make for other challenged claims, Petitioner does not even attempt to depict how the modifications it proposes would allegedly be made, or explain how the resulting circuit would operate. Pet. 35-36;

Ex. 2059, ¶¶80-81. Petitioner suggests that Kimura states that these modifications “can be” made. Pet. 35-36. Petitioner cites to no disclosure of Kimura teaching that any of these modifications could be made to Figure 27C. *Id.* Petitioner also provides no rationale for making these modifications, instead suggesting that the needed changes would be a “design alternative.” *Id.*; *see also* Ex. 2059, ¶¶81-86.

In reply, Petitioner largely fails to address these fundamental problems with the Petition’s analysis of claims 8 and 22. Reply 17-18. Instead it simply suggests that these modifications—which it again does not explain, identify, or adequately describe—“can” be made. *Id.* These arguments fail for the same reasons previously identified. POR 27-31.

5. Petitioner’s and Dr. Foty’s Misapplication of Kimura’s Teachings

As described above, as well as in Patent Owner’s response, Petitioner and Dr. Foty make a number of fundamental mistakes regarding Kimura’s teachings. This is not surprising given that Dr. Foty has no experience in display design let alone active matrix design, and does not qualify as a POSITA. Dr. Foty’s lack of relevant knowledge is especially pertinent here, as Petitioner’s misreading of the prior art appears to result from a lack of appreciation of display-related technology.

For example, Kimura’s disclosures relating to the GOUT and SOUT signals are specific to the display context, and make clear that these signals serve different functions within the scan driver and pixel array. *See, e.g.*, Kimura ¶¶[0304]-[0305].

Petitioner's and Dr. Foty's misapplication of these teachings, *see, e.g.*, POR 21-23, underscores how a proper understanding of active matrix and electroluminescent displays is critical to understand the content of the prior art. *See* POR 6-7. Despite Patent Owner pointing out the problems with Dr. Foty's analysis relative to the GOUT and SOUT signals of Kimura, he fails to correct his error or even address the issue in his 51-page reply declaration.

As another example, and as discussed in greater detail above, Dr. Foty misapplies Kimura's teachings relating to its node voltages. Specifically, while he states in his reply declaration that "the voltage at node 13 is *not* an input signal to circuitry" with respect to the Figure 20A circuit, Ex. 1025, ¶37, he admitted in deposition that this was incorrect, and that in fact the voltage at node 13 is an input signal. Ex. 2062 (Foty), 32:12-20.

These failures underscore that Dr. Foty lacks qualification to opine on matters requiring the perspective of a person of ordinary skill, as Patent Owner has argued here, and as was found in the parallel ITC investigation. *See In re Certain Active Matrix Organic Light-Emitting Diode Display Panels And Modules For Mobile Devices, And Components Thereof*, Inv. No. 337-TA-1351, Order No. 60, EDIS Doc. ID 824992 (July 2, 2024) (finding "that Dr. Foty does not meet the level of ordinary skill in the art for the '599 and '593 patents that I adopted," and therefore excluding his expert testimony for the '593 patent); *see Kyocera Senco Indus. Tools Inc. v. Int'l*

Trade Comm’n, 22 F.4th 1369, 1376-77 (Fed. Cir. 2022) (“To offer expert testimony from the perspective of a skilled artisan in a patent case—like for claim construction, validity, or infringement—a witness must at least have ordinary skill in the art.”). Yet even if Dr. Foty were able to meet the level of ordinary skill, his testimony deserves less weight given his lack of understanding of relevant aspects of the technology as reflected in his repeated errors in interpreting the prior art.

B. Shin in View of Sasaki Does Not Render Obvious Any Challenged Claim

Patent Owner identified fundamental problems with Petitioner’s proposed combination of Shin and Sasaki, including that Shin already provides a capacitor that addresses the purported issue of reversal for which Petitioner suggests a POSITA would look to additional circuitry from Sasaki. POR 31-40. In the Institution Decision the Board agreed, noting that Petitioner’s sole rationale for combining Shin and Sasaki rests upon an alleged “lack of robustness” in Shin’s circuit, and that “Petitioner’s allegations are theoretical at best.” DI, 36.

In reply, Petitioner suggests there are unaddressed periods of time in Shin’s operation that show Shin’s capacitor C1 may not be sufficient. Reply 20 (“Capacitor C1, however, fails to adequately protect against reversal in other periods of operation”). But the petition only discussed a single time period. Pet. 51 (“Other than the above application of a high signal to keep transistor M2 closed during period t_2 , the rest of Shin’s operation remains the same.”). The Petition did not address any

additional time periods, and accordingly any arguments regarding such time periods should be rejected. In any event, Petitioner's arguments have no merit. None of Petitioner's arguments change the fundamental problem with Petitioner's combination. Specifically, Shin already includes a capacitor C1 at the node in question, and teaches that it prevents the sort of reversal that Petitioner describes as the sole basis for its proposed modification of Shin. POR 31-40; Ex. 2059, ¶¶90-92. Petitioner repeats the same speculation it offered in the Petition relating to a theoretical possibility of crosstalk and EMI, but these generalized concerns are never raised or discussed in Shin, nor are they sufficient to overcome Shin's specific disclosure that its capacitor maintains the intended value on the node. *Id.* Indeed, as Dr. Wolfe explains, a POSITA would have taken such considerations into account when designing a circuit. *See* Ex. 2019 ¶89; Ex. 2059 ¶92. The Board previously credited this testimony as "consistent with Shin's express disclosure," DI 36, and nothing in Petitioner's reply alters that analysis.

Petitioner additionally speculates that a capacitor could be necessary to prevent, in a particular time period in the circuit's operation, a low voltage being erroneously provided to the output terminal and causing distortion. Reply 19-22. This argument is faulty, and is not supported by the references Petitioner cites. Sasaki only describes an issue with distortion when the *high signal VDD* is erroneously provided to the output terminal. *See, e.g.,* Ex. 2059, ¶¶95-97. Sasaki

never discusses or suggests potential distortion associated with a low clock signal unintentionally being provided when VDD is also provided to the output terminal. *See, e.g., id.* ¶97 (“Notably, Sasaki does not describe potential distortion in the opposite scenario (i.e., when the intended output signal is VDD but CLK2 is low and erroneously provided)). Thus, Sasaki itself only provides its “anti-reversal circuit” at the node that controls whether VDD is provided to the output terminal, not the node that controls whether the clock signal is provided to the output terminal. *Id.* ¶99. For this additional reason, Petitioner’s argument fails.

C. Tobita Does Not Render Obvious Any Challenged Claim

Claim limitations [1-B] and [15-E] require a “first driver” that “control[s] the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal.” The Petition’s theory as to how Tobita allegedly meets this limitation is clear, and fundamentally flawed:

Transistors Q18-Q21—which receive signals from IN (the first input terminal), CK2 (the second input terminal), and CK1 (the third input terminal)—also control the voltage of the node N1 by, e.g., bringing it to a low level.

Pet. 84-85. This is the only theory presented in the Petition as to how the identified first driver of Tobita allegedly controls the voltage of the second node in accordance with the signals of the first, second, and third input terminals. *Id.* 84-86.

In the Institution Decision, the Board found that “Petitioner shows sufficiently for institution that Tobita’s transistors Q19-Q21 (i.e., part of the ‘first driver’) indirectly control the voltage of the node N1 by opening transistor Q18 to allow VSS to be provided to node N1 *for purposes of bringing it to a low level.*” DI 51 (emphasis added).

However, in the Patent Owner Response, Patent Owner demonstrated—supported by the expert declaration of Dr. Wolfe—a number of problems with the Petition’s analysis of Tobita, including a fundamental problem with the “indirect control” theory and the first driver. POR 42-48. Specifically, for the signal of the third input terminal, which is one of the three recited input signals, the Petition’s theory does not “allow VSS to be provided to node N1 for purposes of bringing it to a low level.” POR 41. Instead, the Petition’s theory mistakenly relies upon the *absence* of any input by the first driver.

In particular, when the signal of the third input terminal turns on the identified transistor in the first driver (Q21), it causes transistor Q18 to turn off, and no longer provide any signal to the identified second node. Ex. 1003, ¶618. Petitioner’s expert admitted that this will not change the voltage that is already on the second node. Ex. 2063, 76:19-77:3. As Dr. Wolfe likewise explains, this lack of a signal does not itself change or otherwise control the voltage of the second node. Ex. 2059, ¶115. Indeed, Tobita confirms that the operation of the circuit formed by transistors Q19-Q21 does

not alter the output waveform relative to other embodiments that do not include these transistors. Tobita ¶[0177]. Thus, under Petitioner’s theory, the first driver does *not* control the voltage of the second node in accordance with the signal of the third input terminal at all. Ex. 2059, ¶115.

In reply, Petitioner musters no substantive response and cannot refute Patent Owner’s showing. Instead, Petitioner seeks to dismiss this argument as “nonsense” rather than engaging with it. Reply 24. Tellingly, however, Petitioner additionally presents new argument that when Q18 turns off, the “other transistors” of the alleged “first driver” provide “a *high-level* signal.” Reply 24 (emphasis added). This new argument is inconsistent with the Petition’s theories, and should be rejected for that reason alone. The Petition was clear in advancing the theory that transistors Q18-Q21 receive signals from the alleged first, second, and third output terminals, and control the voltage of node N1 by “bringing it to a *low level*.” Pet. 84-85 (emphasis added). This theory has been shown to be incorrect. Nowhere in the Petition does Petitioner suggest that transistor Q18 operates with Q3-Q5 to provide a “high-level signal.” Reply 24.

Moreover, Petitioner fails to explain the new theory it advances in reply, including how it alleges that this operation purportedly occurs in accordance with the signals of the first, second, and third input terminals. Petitioner’s new argument fails to show the claim limitation is met for this additional reason.

Petitioner also mistakenly suggests that Patent Owner applies a different understanding in its discussion of the operation of the stage circuit in its own product. Reply 24. Not so. As Patent Owner previously explained, there is a material distinction. In the Samsung product, the first driver provides a signal that simply passes through a transistor to control a node. In marked contrast, in Tobita the identified first driver provides a signal (high or low) that controls a different node (N6) to cause a transistor (Q18) to turn on or off, which may then allow a *different* signal (VSS) to be provided to a node (N1). *See* Ex. 2059, ¶¶113-114.

III. Objective Indicia

The evidence of copying—and its nexus—is largely undisputed. Petitioner provides no substantive rebuttal to Patent Owner’s showings that (i) SDC’s stage circuit practices the claims; (ii) the copied products practice the claims in the same manner; and (iii) the copied products are strikingly similar replicas of SDC products.

First, regarding SDC’s stage circuits, Patent Owner and its expert showed the Galaxy S22 Ultra display practiced the claims (POR 54-56, Ex. 2059, ¶148), with a claim chart mapping the display to every claim element. Ex. 2057. Petitioner does not assert that any claim element is not met, beyond asserting, incorrectly, an alleged inconsistency with Patent Owner’s discussion of Tobita, which is separately addressed above. As discussed, there is no inconsistency.

Second, Petitioner does not address (let alone rebut) Patent Owner’s evidence showing that a representative display from Mengtor (Ex. 2046) practices the claims in the same manner as SDC—underscoring the nexus between copying and the claimed features of the invention. *See Liqwd, Inc. v. L’Oreal USA, Inc.*, 941 F.3d 1133, 1138 (Fed. Cir. 2019) (“[T]he proponent of objective evidence offered to show nonobviousness, such as copying, must show that a nexus exists But where there is evidence of actual copying efforts, that evidence is always relevant.”).

Third, Petitioner does not dispute that Patent Owner’s evidence shows these representative displays and others—including products of Petitioner BOE—are strikingly similar to SDC’s, down to the physical layouts. Ex. 2059, ¶¶143-144. Petitioner does not dispute the evidence shows Petitioner BOE’s display, identify any relevant differences from SDC’s stage circuit, or offer any evidence of independent development. As Dr. Wolfe explains, only deliberate copying can explain the striking similarities of the copied products. *Id.*; *cf. Institut Pasteur v. Focarino*, 738 F.3d 1337, 1347-48 (Fed. Cir. 2013).

As for nexus, there is no substantive dispute that SDC’s stage circuit practices the challenged claims, and Petitioner does not raise any substantive dispute that the benefits of reduction of dead space and narrower bezel result from the structures

recited in the claims.² Petitioner makes a legally flawed argument that because certain limitations allegedly could be found in prior art, nexus is not shown. But “proof of nexus is not limited to only when objective evidence is tied to the supposedly ‘new’ feature(s)”; “the patent owner can show that it is the claimed combination as a whole that serves as a nexus for the objective evidence.” *WBIP, LLC v. Kohler Co.*, 829 F.3d 1317, 1330 (Fed. Cir. 2016).

As Patent Owner explained, and Petitioner does not rebut, the ’593 Patent’s claimed inventions provided a unique set of benefits unattainable in the prior art. POR 80. Petitioner purports to find evidence of *certain limitations* in Shin (Reply 27-28), but no prior art disclosure provided the benefits that result from the claimed inventions’ combination of elements. *See* POR 59. The ’593 Patent’s combination of elements is what allowed for AMOLED displays with significantly narrowed bezels. POR 59-64; *cf. Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1332 (Fed. Cir. 2019) (“[O]bjective indicia must be directed to what was not known in the

² Contrary to Petitioner’s argument, specific discussion of “narrowed bezel” benefits in the patent is not required; what is pertinent are “advantages inherent in what is specifically disclosed in a patent”—here, the narrowed bezel benefits flow from the ’593 Patent’s circuit design. *In re Vamco Mach. & Tool, Inc.*, 752 F.2d 1564, 1577 n.5 (Fed. Cir. 1985).

prior art ... [which] may well be the novel combination or arrangement of known individual elements.”) (cleaned up).

Petitioner asks the Board to ignore the ’593 Patent’s contribution to reduction of dead space and a narrowed bezel because Samsung Display has other patents on pixel layout arrangements and pixel circuits that provide other improvements. Reply 27-28. That is illogical and contrary to precedent. That other inventions allowed for *additional* improvements is immaterial. Moreover, nexus can be satisfied even where the success of a patented product “was, in fact, based on two factors,” one “undisputedly covered” by the claims, and the other “undisputedly not covered.” *Ecolochem, Inc. v. S. Cal. Edison Co.*, 227 F.3d 1361, 1378 (Fed. Cir. 2000).

IV. Conclusion

The Board should find the challenged claims patentable.

Date: April 17, 2025

Respectfully submitted,

By /Dave A. Garr/

David A. Garr

Registration No.: 74,932

Scott C. Weidenfeller

Registration No.: 54,531

Counsel for Patent Owner

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), I certify that the present paper contains 5,594 words based on the word count indicated by the word-processing program used to generate the paper and excluding those portions exempted by 37 C.F.R. §§ 42.24(a) and (b).

Date: April 17, 2025

/Dave A. Garr/

David A. Garr

Registration No.: 74,932

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6, I hereby certify that the foregoing Patent Owner's Sur-Reply and accompanying exhibits were served by electronic mail on the following counsel of record for petitioner:

K. Patrick Herman (P52PTABDocket@orrick.com)
Richard F. Martinelli (RFMPTABDocket@orrick.com)
Xiang Wang (XW0PTABDocket@orrick.com)
ORRICK, HERRINGTON & SUTCLIFFE, LLP

Date: April 17, 2025

/Dave A. Garr/
David A. Garr
Registration No.: 74,932