

**UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD**

**MIANYANG BOE OPTOELECTRONICS TECHNOLOGY CO., LTD.; WUHAN CHINA STAR
OPTOELECTRONICS SEMICONDUCTOR DISPLAY TECHNOLOGY CO., LTD.; TIANMA
MICROELECTRONICS CO., LTD.; AND VISIONOX TECHNOLOGY, INC.,
Petitioner,**

v.

**SAMSUNG DISPLAY CO., LTD.,
Patent Owner.**

Case Nos. IPR2024-00620

U.S. Patent No. 9,330,593

**PETITIONER'S HEARING DEMONSTRATIVES
June 13, 2025**

Overview of Argument

Introduction

Kimura renders the independent claims obvious

Kimura also teaches the dependent claim limits

Sasaki improves Shin's stage circuit

Tobita includes the claimed "first driver" "transistor"

Patent Owner's deficient "secondary considerations"

The '593 Patent

1. Field

Embodiments relate to a stage circuit and an organic light emitting display using the same.

Conventional organic light emitting display includes a data driver for supplying data signals to data lines, a scan driver for sequentially supplying scan signals to scan lines, and a pixel unit including a plurality of pixels coupled to the scan lines and the data lines.

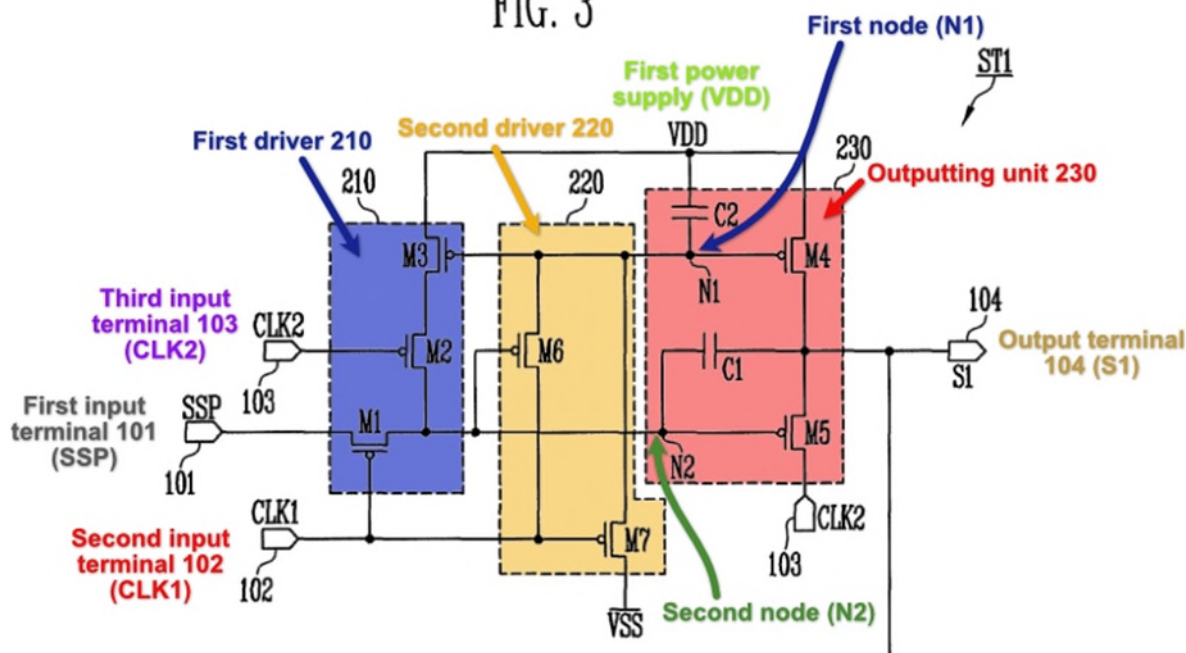
The pixels included in the pixel unit are selected when the scan signals are supplied to the scan lines to receive the data signals from the data lines. The pixels that receive the data signals generate light components with predetermined brightness components corresponding to the data signals to display an image.

The scan driver includes stage circuits coupled to the scan lines. The stages supply the scan signals to the scan lines coupled thereto to correspond to signals supplied thereto.

Ex. 1001 (593 Patent), 1:17-18, 1:34-47;
see also Paper 1 (Petition) at 7

'593 Patent – Claim 1

FIG. 3



1. A stage circuit having a first input terminal, a second input terminal, a third input terminal, and an output terminal, the stage circuit comprising:

an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node;

a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal; and

a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node, wherein

the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver.

Ex. 1001 (593 Patent), Fig. 3, Claim 1;
see also Paper 1 (Petition) at 8

Grounds At Issue

Ground	Prior Art	Claims
1	Kimura	1-8, 14-22, and 25 obvious
2	Shin + Sasaki	1-6, 8, 14-20, 22, and 25 obvious
3	Shin + Sasaki + Jeong	7 and 21 obvious
4	Tobita	1-2 and 15-18 obvious
5	Tobita + Jeong	7 and 21 obvious

Paper 1 (Petition) at 4-5

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FIG. 34

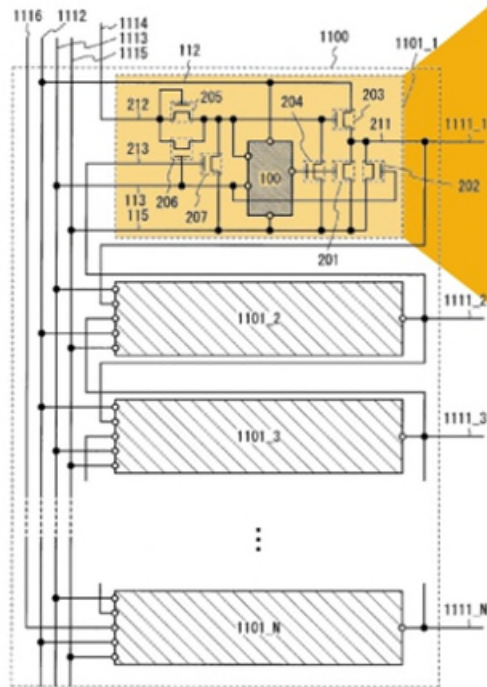
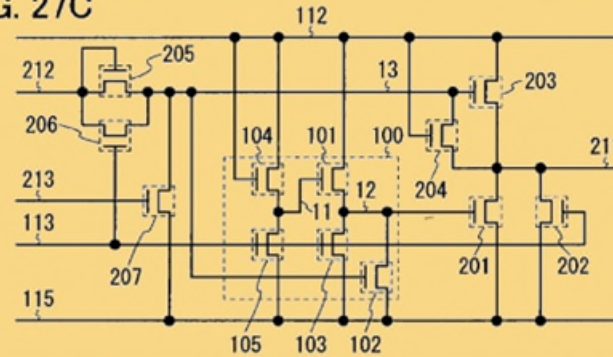


FIG. 27C



[0320] In this embodiment, a display device, a pixel included in the display device and a shift register circuit included in the display device are described. Note that the shift register circuit can include the semiconductor device in Embodiment 1 or 2.

Ex. 1004 (Kimura) at [0320], Figs. 27C, 34;
see also Paper 1 (Petition) at 10-11

Patent Owner Repeatedly Mischaracterizes the Petition and Kimura

- ✗ Petitioner “relies on portions of Kimura directed to different circuits and configurations.”
- ✗ Petitioner “fail[s] to ... adequately explain how the Figure 27 circuit ... would operate.”
- ✗ “Kimura’s description of the Figure 27C circuit is not compatible with the timings shown in in Figure 21B.”
- ✗ “Petitioner now attempts to change theories from those presented in the Petition.”

Paper 30 (PO Sur-Reply) at 1-5

The Petition Noted the Interrelation Between Kimura's Figures

This ground is expressed in terms of obviousness, and not anticipation, because the portion of Kimura discussing Figure 27C does not itself mention all the depicted transistors, inputs, and outputs. Kimura explains, however, that the device of Figure 27C builds on and shares components with the devices of its other figures. Kimura, [0282]-[0286]. Thus, a POSITA would have understood that any shared components in Figure 27C not specifically discussed in the portion of Kimura addressing the figure would obviously be connected—and function—in the same way discussed elsewhere. *See Decl.*, ¶ 146. To be clear, this ground—at least with

Paper 1 (Petition) at 15

The ***Petition*** Explained That Kimura Obviously Uses the Same Input Signals Across Circuits

Figure 21B provides an example “timing chart for illustrating operation of the semiconductor device[.]” *Id.*, [0062], [0066]. While the chart is not specific to the device of Figure 27C, a POSITA would have understood that that device—because it includes the same input and output lines and many of the same transistors as Kimura’s other circuits—would (or at least obviously could) be supplied with input signals in the same manner and with the same timing. *See Decl.*, ¶¶ 160-165.

Paper 1 (Petition) at 19

The Circuits Shown in Kimura's Figures Share Components

[0093] Hereinafter, embodiments will be described with reference to the drawings. Note that the embodiments can be implemented in various different ways and it will be readily appreciated by those skilled in the art that modes and details of the embodiments can be changed in various ways without departing from the spirit and scope of the present invention. Therefore, the present invention should not be construed as being limited to the following description of the embodiments. Note that in structures described below, the same portions or portions having similar functions are denoted by common reference numerals in different drawings, and description thereof is not repeated.

Ex. 1004 (Kimura) at [0093];
see *also* Paper 1 (Petition) at 15; Paper 27 (Reply) at 3

Kimura Repeatedly Explains that its Circuits Build on Each Other

[0218] In this embodiment, a semiconductor device obtained by addition of an element, a circuit, or the like to the semiconductor device in Embodiment 1 is described.

[0219] First, a structure where a transistor 201 (a sixth transistor) is additionally provided in the semiconductor device in Embodiment 1 is described. FIG. 14A illustrates a structure where the transistor 201 is additionally provided in the semiconductor device in FIG. 1A.

[0245] FIG. 16A illustrates a structure where the transistor 202 is additionally provided in the semiconductor device in FIG. 14A. The transistor 202 is an n-channel transistor. How-

[0249] FIG. 17A illustrates a structure where the transistor 203 is additionally provided in the semiconductor device in FIG. 14A. The transistor 203 is an n-channel transistor. How-

[0261] FIG. 20A illustrates a structure where the transistor 204 is additionally provided in the semiconductor device in FIG. 17A. The transistor 204 is an n-channel transistor. How-

[0265] FIG. 21A illustrates a structure where the transistor 205 is additionally provided in the semiconductor device in FIG. 17A. The transistor 205 is an n-channel transistor. How-

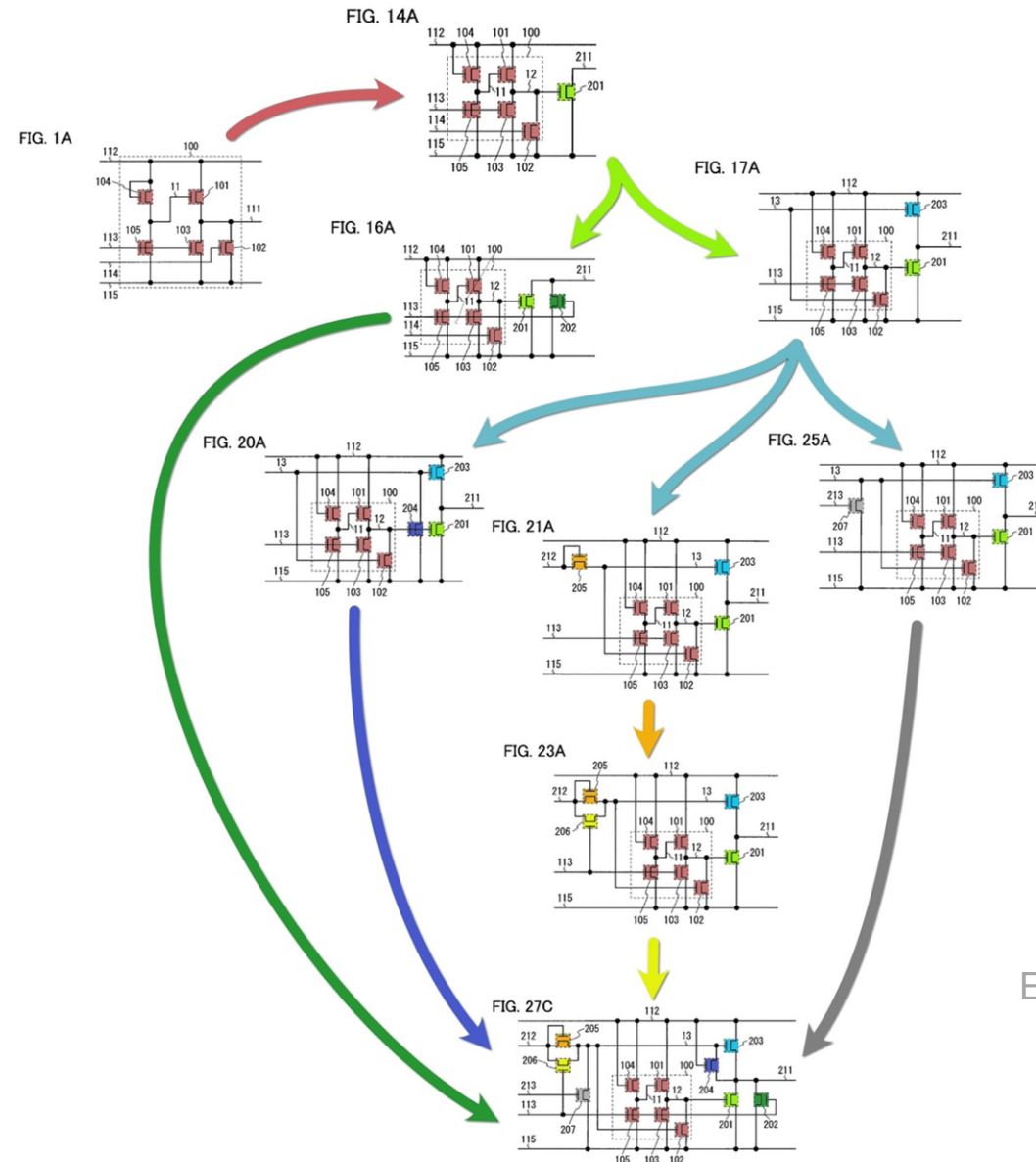
[0271] FIG. 23A illustrates a structure where the transistor 206 is additionally provided in the semiconductor device in FIG. 21A. The transistor 206 is an n-channel transistor. How-

[0277] FIG. 25A illustrates a structure where the transistor 207 is additionally provided in the semiconductor device in FIG. 17A. The transistor 207 is an n-channel transistor. How-

[0284] Note that the semiconductor device in FIG. 27A corresponds to a semiconductor device in which the transistors 201 to 207 are additionally provided in the semiconductor device in FIG. 14A.

Ex. 1004 (Kimura) at [0218]-[0219], [0245], [0249], [0261], [0271], [0277], [0284];
see also Paper 1 (Petition) at 15; Paper 27 (Reply) at 3-5

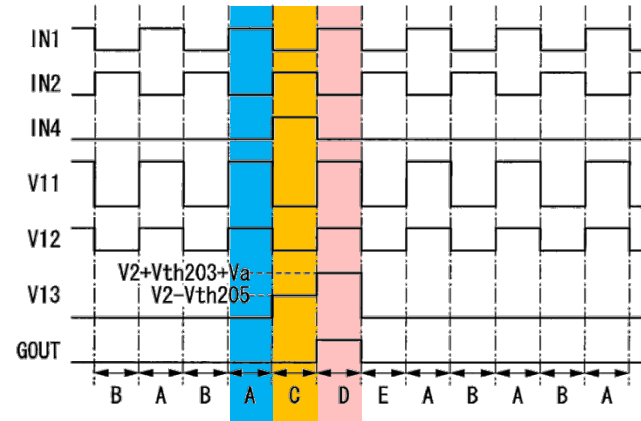
Kimura's Figures Confirm This Circuit-to-Circuit Relationship



Ex. 1004 (Kimura) at Figs. 1A, 14A, 16A, 17A, 20A, 21A, 23A, 25A, 27C; see *also* Paper 27 (Reply) at 5-6

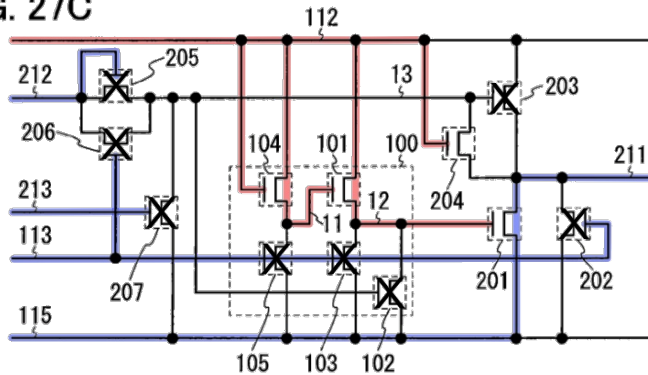
Dr. Foty Explained How Figure 27C Operates in Detail

FIG. 21B



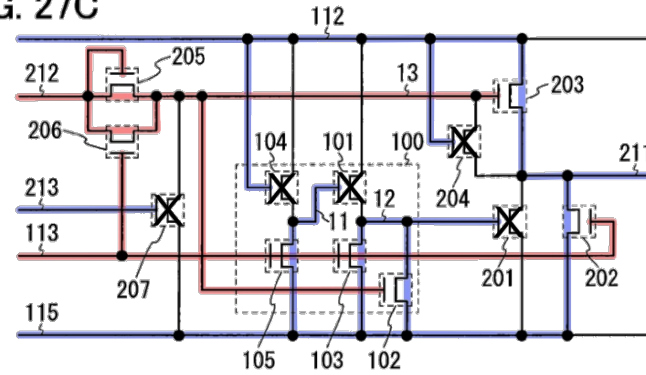
“Period A”

FIG. 27C



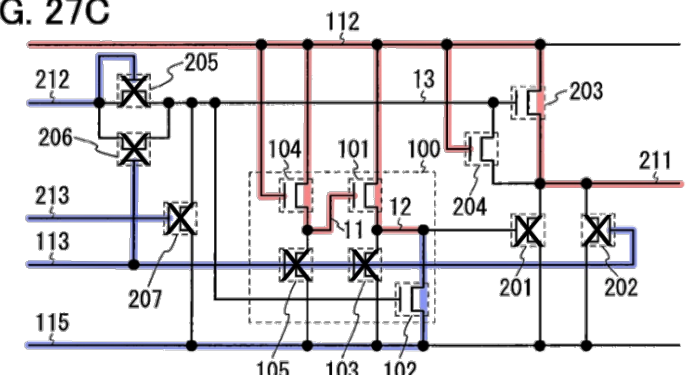
“Period C”

FIG. 27C



“Period D”

FIG. 27C



Ex. 1003 (Foty Dec.), ¶¶ 160-164 (citing Ex. 1004 (Kimura), Figs. 21B, 27C);
see also Paper 1 (Petition) at 19

Kimura Consistently Employs the Same Input Signals

FIG. 14A

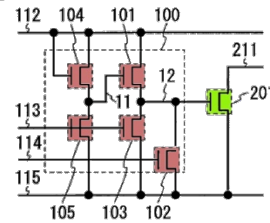


FIG. 15A

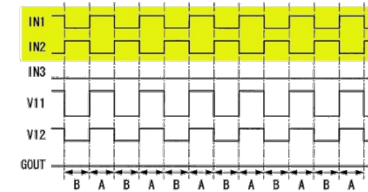


FIG. 17A

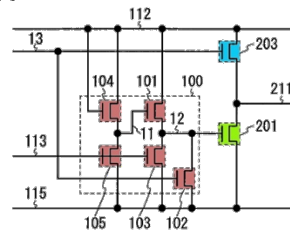


FIG. 17B

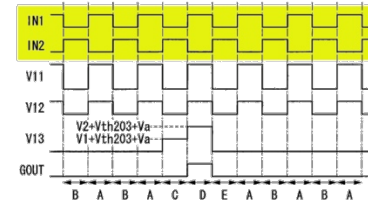


FIG. 21A

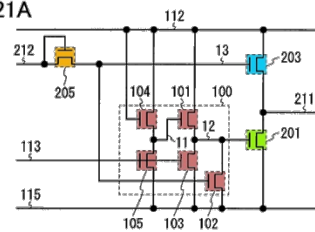


FIG. 21B

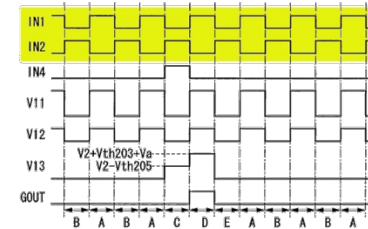


FIG. 25A

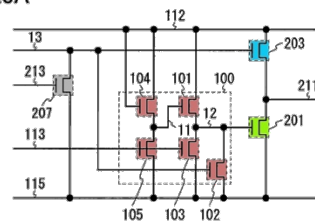
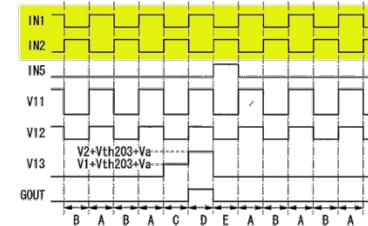


FIG. 25B



Ex. 1004 (Kimura) at Figs. 14A, 15A, 17A, 17B, 21A, 21B, 25A, 25B; see also Paper 27 (Reply) at 6-7

Petitioner's Expert Dr. Foty Clearly Explained that V13 Is the Potential at Node 13 (Which Differs From Circuit-to-Circuit)

37. Figure 20A shows the addition of transistor 204 (**dark blue**). *Id.*, [0260]-[0261]. This transistor is intended to allow the “potential of ... node 13” to be “lowered” for the purpose of reducing the risk of transistor deterioration. *Id.*, [0262]. Note in particular (as will further be explained below) that the potential (i.e. the voltage) at node 13 will differ across the circuit embodiments – as the voltage at node 13 is *not* an input signal to circuitry, but rather is a consequence when the same input signals are applied to the different circuitries of the different embodiments.

Ex. 1025 (Foty Reply), ¶ 37;
see also Paper 27 (Reply) at 5-7

Kimura Explains the Difference in Operation Between Figure 27C and Its Other Circuits

[0256] The operation of the semiconductor device in the period D is described with reference to a schematic view in

...

that the potential of the wiring 211 starts to rise. In this case, the node 13 is in a floating state. Then, the potential of the node 13 is raised by capacitive coupling between the gate of the transistor 203 and the second terminal of the transistor 203. Accordingly, the potential of the node 13 becomes $V_2 + V_{th203} + V_a$. This is so-called bootstrap operation. Thus, the potential of the wiring 211 becomes V_2 , so that the signal GOUT is set at an H level.

[0286] FIG. 27C illustrates a structure where the first terminal of the transistor 204 is connected to the wiring 211 and the gate of the transistor 204 is connected to the wiring 112 in the semiconductor device in FIG. 27A. Thus, in a period D, the potential of the node 13 can be lowered. Therefore, dielectric breakdown or deterioration of the transistor connected to the node 13 (e.g., the transistor 102, the transistor 203, the transistor 205, or the transistor 206) can be prevented.

FIG. 21A

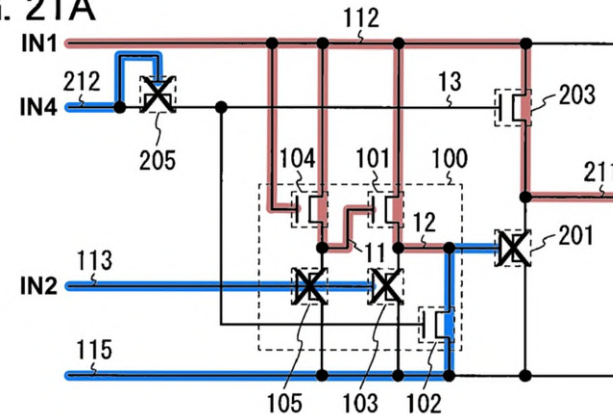


FIG. 21B

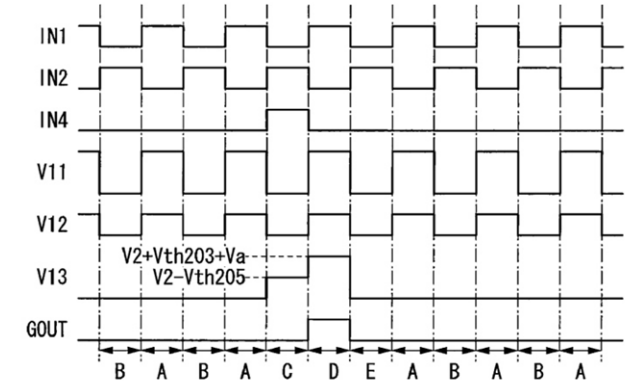
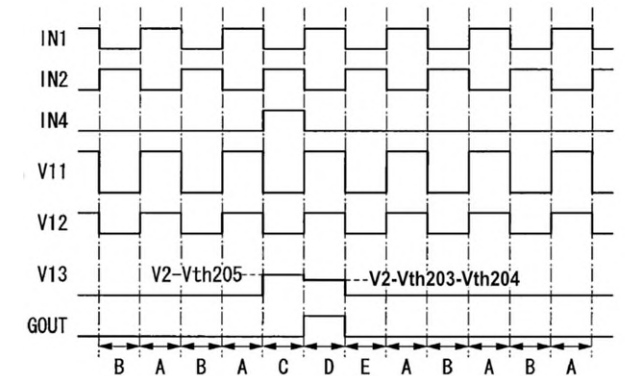
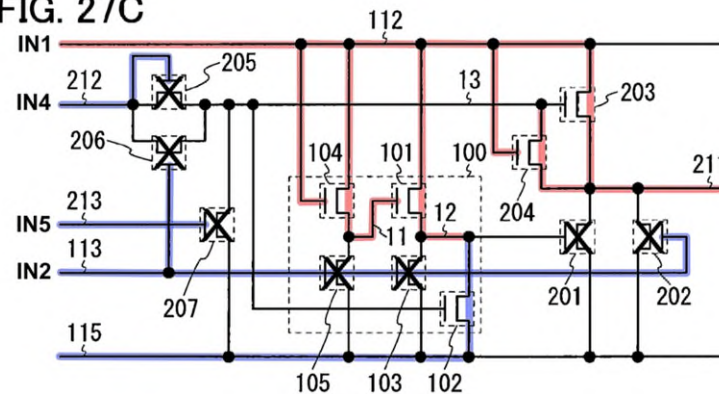


FIG. 27C



Ex. 1004 (Kimura) at [0256], [0286], Figs. 21A-21B, 27C;
see also Ex. 1025 (Foty Reply), ¶¶ 61-64; Paper 27 (Reply) at 8-10

Overview of Argument

Introduction

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Sasaki improves Shin's stage circuit

Tobita includes the claimed "first driver" "transistor"

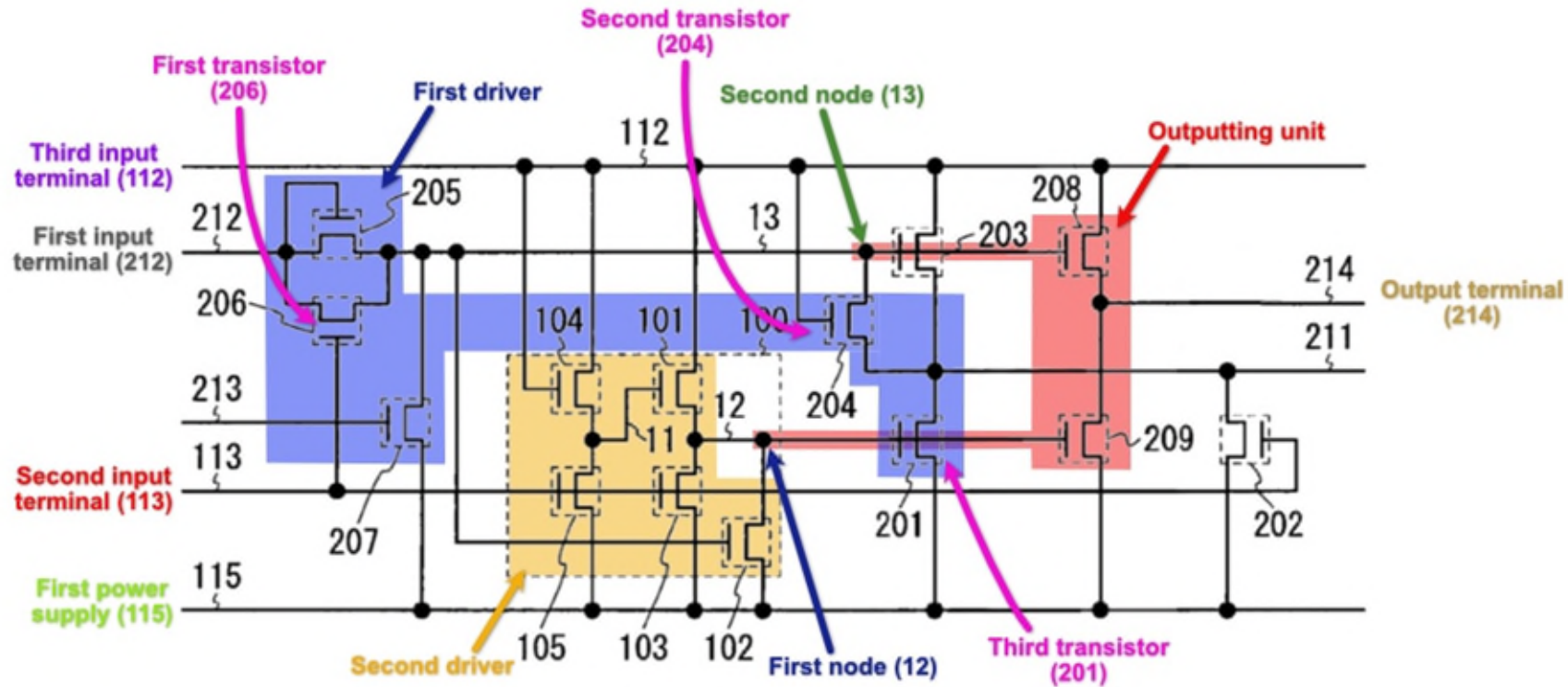
Patent Owner's deficient "secondary considerations"

Only Certain '593 Patent Dependent Claims Are Disputed

- **Claims 6 and 20:** requires “first,” “second,” and “third” transistors” in the “first driver” that are “positioned” and “coupled” in specific ways
- **Claims 7 and 21:** requires “a first capacitor” and “a second capacitor”
- **Claims 8 and 22:** requires different transistor interconnections and a “second power supply” with a “lower voltage”

Paper 23 (PO Response) at 16-30

Claims 6 and 20: The Petition Did Explain How the Combination of Figs. 27C and 31C Practices Claim 1



Paper 1 (Petition) at 30-31

Claims 6 and 20: The Circuit of Figs. 27C and 31C Generates Two Outputs (and Thus Includes Two “Outputting Units”)

[0304] In the structures illustrated in FIGS. 10A to 10C, FIG. 14A, FIG. 16A, FIG. 17A, FIG. 20A, FIG. 21A, FIG. 23A, FIG. 25A, FIGS. 27A to 27C, FIGS. 28A to 28C, FIGS. 29A to 29C, FIGS. 30A to 30C, and FIGS. 47A and 47B, a signal which is different from the signal GOUT can be generated. For example, in the semiconductor device of this embodiment, when a signal SOUT is generated in addition to the signal GOUT and a plurality of semiconductor devices are connected, the signal SOUT is not output to the wiring 211 but can be input to a semiconductor device in a different stage as a start pulse. Thus, the degree of delay or distortion of the signal SOUT is lower than that of the signal GOUT. Therefore, the semiconductor device can be driven with a signal which does not easily cause delay or distortion, delay of an output signal of the semiconductor device can be reduced. In order to realize this, in the structures illustrated in FIG. 14A, FIG. 16A, FIG. 17A, FIG. 20A, FIG. 21A, FIG. 23A, FIG. 25A, FIGS. 27A to 27C, FIGS. 28A to 28C, FIGS. 29A to 29C, FIGS. 30A to 30C, and FIGS. 47A and 47B, a transistor 208 can be additionally provided.

*Ex. 1004 (Kimura) at [0304];
see also Paper 27 (Reply) at 13*

Claims 6 and 20: The Claims Do Not Require Provision of the Claimed “Output Signal” to a Display Scan Line

1. A stage circuit having a first input terminal, a second input terminal, a third input terminal, and an output terminal, the stage circuit comprising:

an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node;

a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal; and

a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node, wherein the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver.

6. The stage circuit as claimed in claim 2, wherein the first driver includes:

a first transistor between the first input terminal and the second node, the first transistor having a gate electrode coupled to the second input terminal; and

a second transistor and a third transistor serially positioned between the second node and the first power supply, wherein a gate electrode of the second transistor is coupled to the third input terminal, and

wherein a gate electrode of the third transistor is coupled to the first node.

*Ex. 1001 (593 Patent) at Claims 1, 6
see also Paper 27 (Reply) at 15*

Claims 6 and 20: The Mere Fact that Additional Transistors Are Included Does Not Show Non-Obviousness

'593 Patent:

FIG. 7 illustrates a circuit diagram of stage circuits according to a third embodiment. In FIG. 7, the same elements as those of FIG. 3 are denoted by the same reference numerals and detailed description thereof will not be repeated.

Referring to FIG. 7, the stage circuit according to the third embodiment further includes a bidirectional driver 240. The bidirectional driver 240 performs control so that the scan signal may be supplied in a first direction (from the first scan line S1 to the nth scan line Sn) or in a second direction (from the nth scan line Sn to the first scan line S1). For this purpose, the bidirectional driver 240 includes a 10th transistor M10 and an 11th transistor M11.

*Ex. 1001 (593 Patent) at 8:47-54
see also Paper 27 (Reply) at 14*

Purported Commercial Embodiment:

Reply 24. Not so. As Patent Owner previously explained, there is a material distinction. In the Samsung product, the first driver provides a signal that simply passes through a transistor to control a node. In marked contrast, in Tobita the

Paper 27 (PO Sur-Reply) at 21

Claims 7 and 21: Kimura Itself Explains How and Why Capacitors Are Included in its Circuit

[0190] FIG. 9A illustrates a structure where the circuit 120 is additionally provided in the semiconductor device in FIG. 1A. The circuit 120 is connected between the wiring 113 and a portion where the gate of the transistor 103 and the gate of the transistor 105 are connected to each other. The circuit 120 has a function of delaying the signal IN2 which is to be input to the wiring 113. Thus, for example, timing of when the potential of the gate of the transistor 105 rises is delayed as compared to timing of when the signal IN2 is set at an H level. In other words, timing of when the transistor 105 is turned on or timing of when the potential of the node 11 is lowered is delayed as compared to the timing of when the

[0191] Note that any circuit can be used as the circuit 120 as long as it includes at least a capacitance component and a resistance component. For example, as the circuit 120, a resistor, a capacitor, a transistor, a diode, an element in which these elements are combined with each other, or a variety of different elements can be used. FIGS. 9C and 9D each illustrate a structure where the circuit 120 includes a resistor 121 and a capacitor 122. As another example, as the circuit 120, a

FIG. 9C

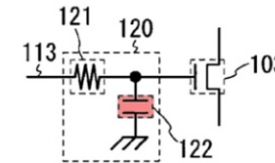
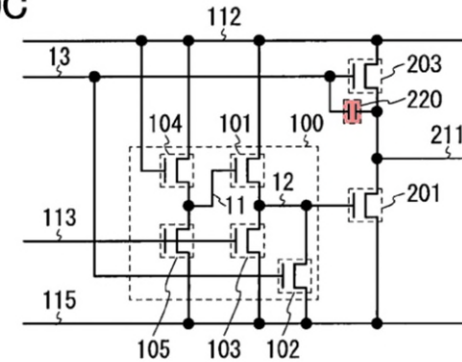


FIG. 30C



[0303] FIG. 30C illustrates a structure where the capacitor 220 which is connected between the node 13 and the wiring 211 is additionally provided in the semiconductor device in FIG. 17A. With this structure, the potential of the node 13 is likely to rise in bootstrap operation. Thus, V_{gs} of the transistor 203 can be increased. Accordingly, the channel width of the transistor 203 can be made small. Alternatively, the fall time or rise time of the signal GOUT can be shortened. A MOS capacitor can be used as the capacitor, for example.

Ex. 1004 (Kimura) at [0190]-[0191], [0303], Figs. 9C and 30C
see also Paper 1 (Petition) at 32-34

Claims 8 and 22: Kimura Also Explains How and Why Different Transistor Interconnections and Power Supply Signals Are Employed

[0169] FIG. 7C illustrates a structure where the first terminal of the transistor 102 is connected to the wiring 113 in the semiconductor device in FIG. 1A. An H-level signal can be supplied to the first terminal of the transistor 102. Thus, a reverse bias can be applied to the transistor 102, so that deterioration of the transistor 102 can be suppressed.

[0172] FIG. 7E illustrates a structure where the wiring 112 is divided into a plurality of wirings 112A and 112B, the wiring 113 is divided into a plurality of wirings 113A and 113B, and the wiring 115 is divided into a plurality of wirings 115A to 115C in the semiconductor device in FIG. 1A. The

...
signals can be supplied to the wirings 113A and 113B. Different voltages or signals can be supplied to the wirings 115A to 115C.

*Ex. 1004 (Kimura) at [0169], [0172]-[0173];
see also Paper 1 (Petition) at 35-36*

Overview of Argument

Introduction

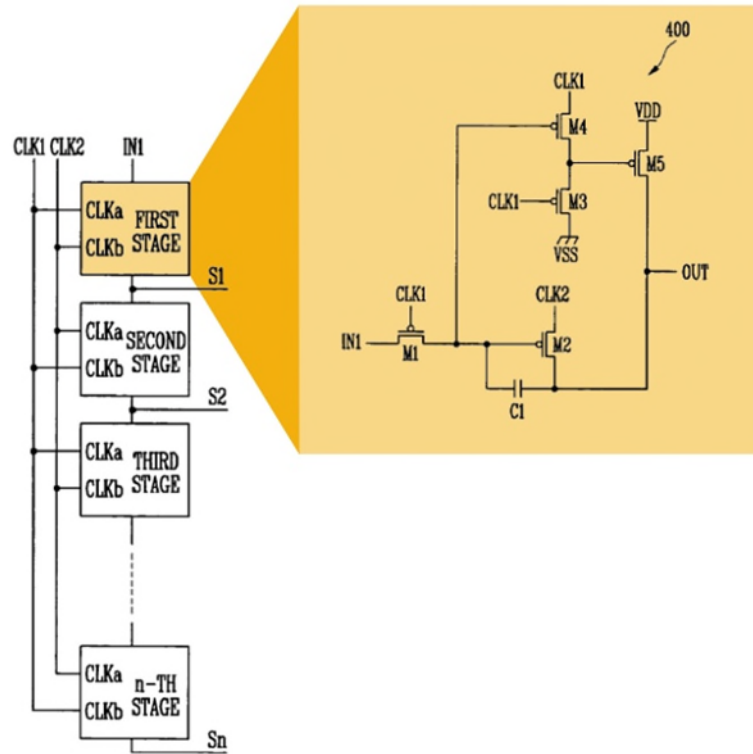
Kimura renders the independent claims obvious

Kimura also teaches the dependent claim limits

Sasaki improves Shin's stage circuit

Tobita includes the claimed “first driver” “transistor”

Patent Owner's deficient “secondary considerations”



[0003] The field of the present invention relates to an organic light emitting display, and more particular to a scan driving circuit used for a current programming type organic light emitting display.

Ex. 1005 (Shin) at [0003], Figs. 10-11;
see also Paper 1 (Petition) at 11-12

[0003] This invention relates to a shift register in an electronic circuit being operated by a pulse-cut clock signal, and to a drive circuit, an electrode substrate and a display device that include the shift register.

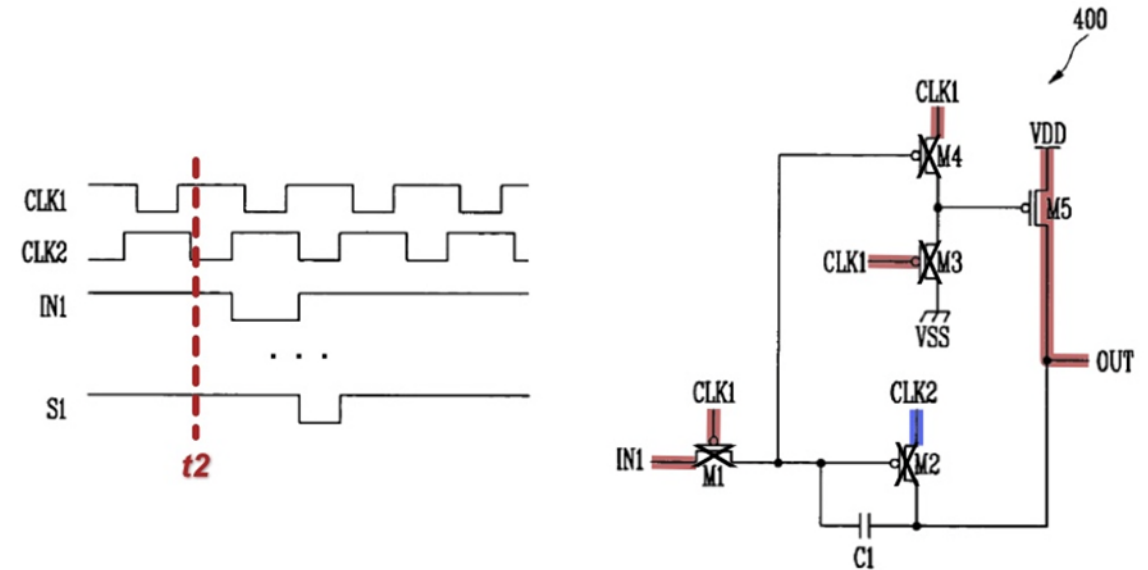
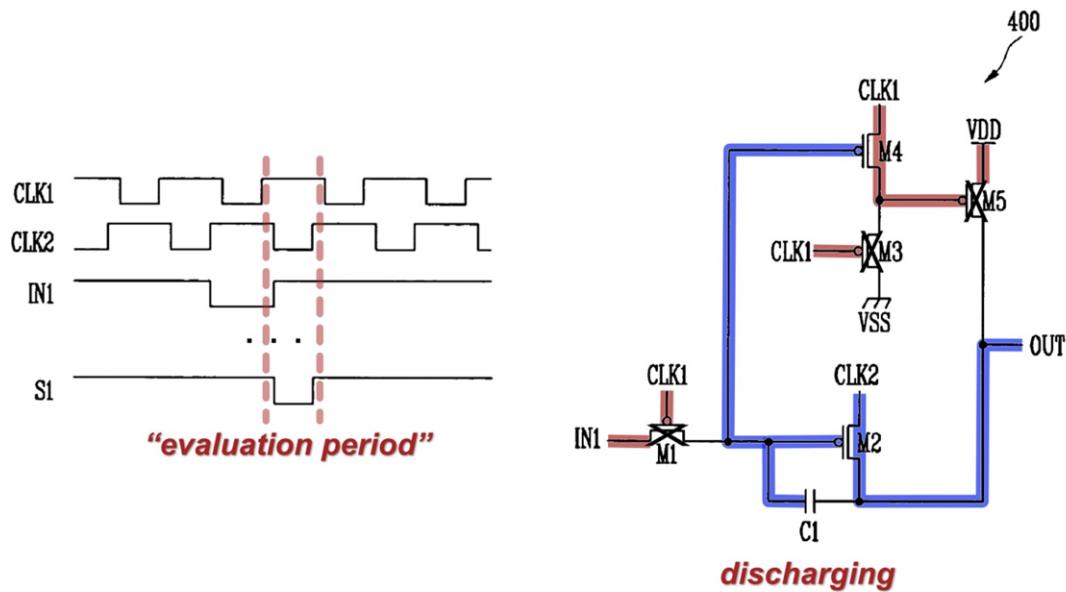
[0042] An anti-reversal circuit includes a seventh transistor T7 and an eighth transistor T8. The seventh transistor T7

...

as node n3. The anti-reversal circuit prevents a voltage level at the control electrode of the second transistor T2 from being reversed, which is attributable to a floating state of the control electrode of the second transistor T2, where if a voltage level of the first clock signal C1 is reversed in the state where the first transistor T1 is turned on and the second transistor T2 is turned off. Here, the floating state refers to a state where electric potential is easily variable because the high voltage VDD is not supplied.

Ex. 1014 (Sasaki) at [0003], [0042];
see also Paper 1 (Petition) at 12

Shin's Circuit Encounters Different Problems in Different Time Periods



Ex. 1006 (Shin), Figs. 11, 12;
see also Paper 1 (Petition) at 47-48; Paper 27 (Reply) at 19-20

A POSITA Would Have Been Motivated to Apply Sasaki to Shin

- Eliminates the effects of noise and interference
- The art is replete with examples of circuits employing both a capacitor and anti-reversal circuit to keep a transistor off
- An anti-reversal circuit provides active protection ensuring transistor M2 remains closed

Paper 1 (Petition) at 51-52;
Paper 27 (Reply) at 20-21

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Kimura also teaches the dependent claim limits

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Tobita includes the claimed “first driver” “transistor”

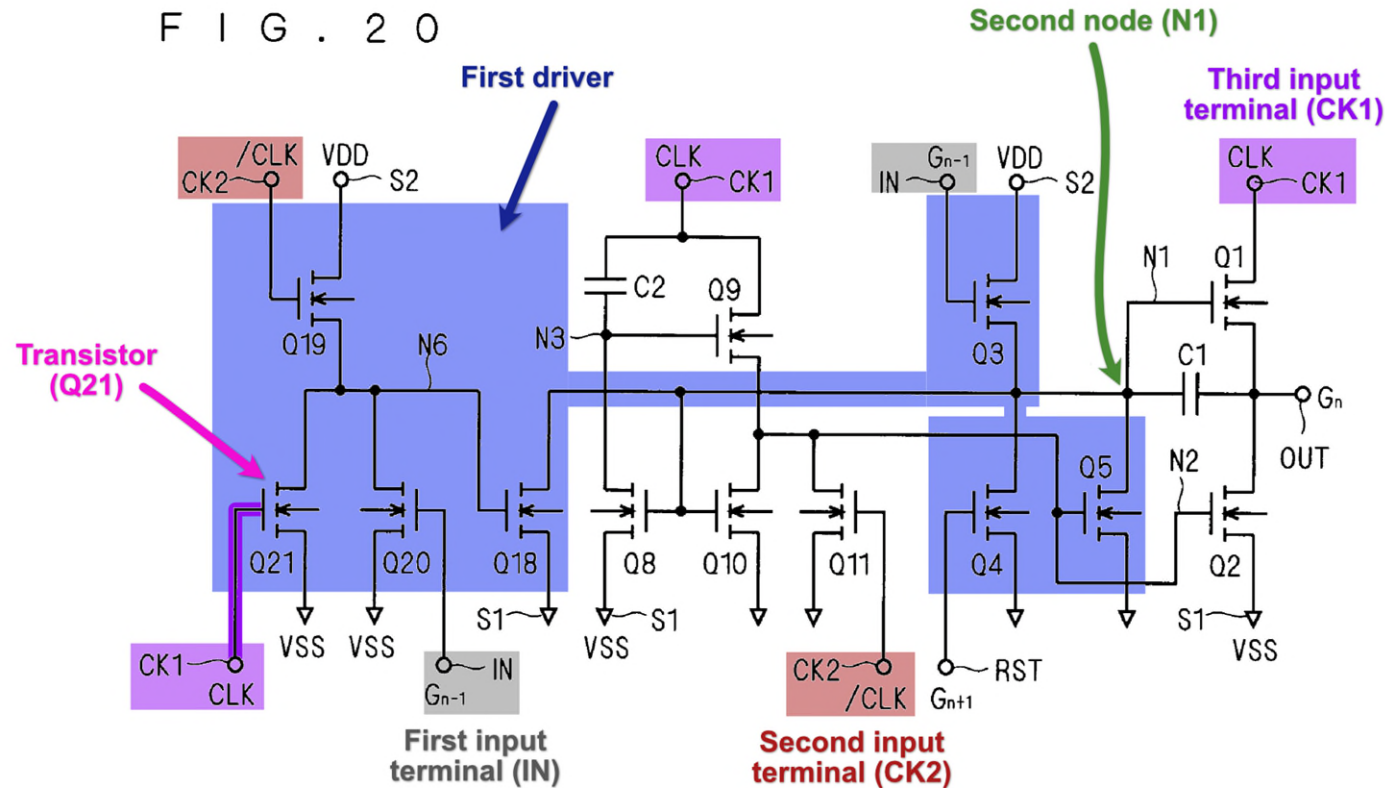
Patent Owner's deficient “secondary considerations”



[0002] The present invention relates to a shift register, and more particularly, to a shift register for use as a scanning-line driving circuit for an image display apparatus or the like, which is formed by field effect transistors of the same conductivity type only.

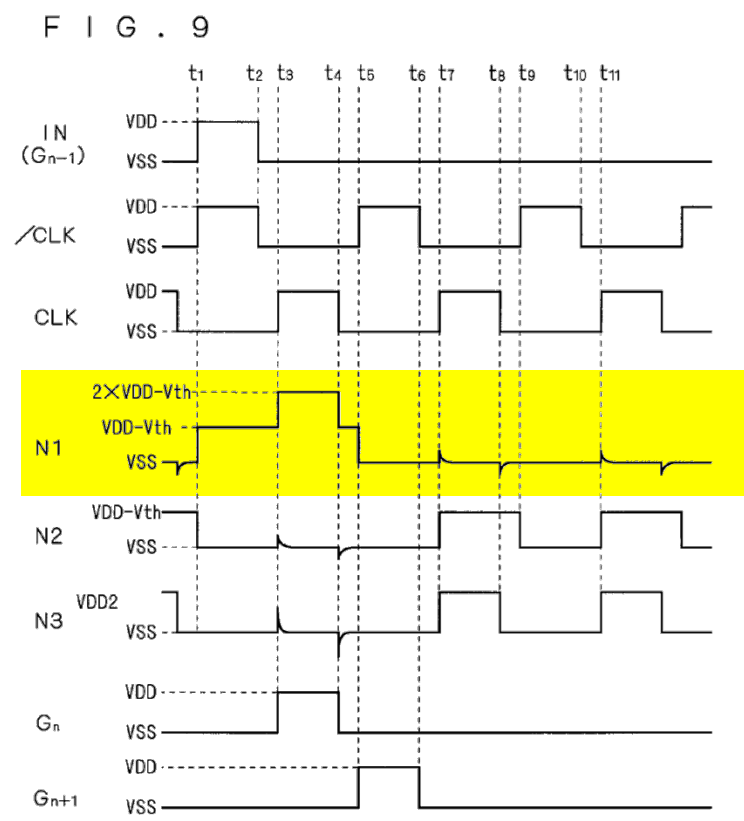
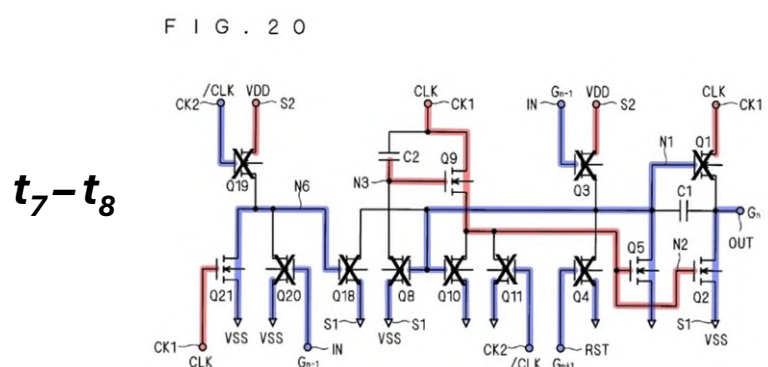
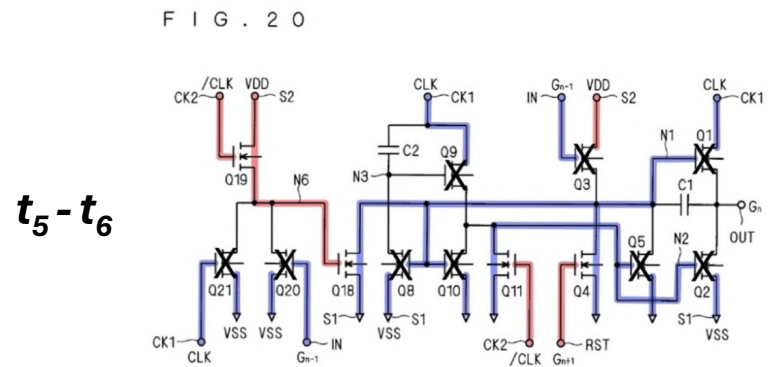
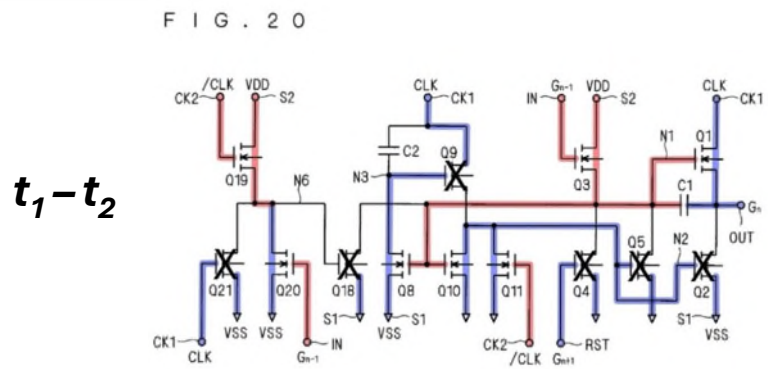
Ex. 1006 (Tobita) at [0002], Figs. 7-8;
see *also* Paper 1 (Petition) at 13

Tobita Includes a “Transistor” in Its “First Driver” Whose “On/Off Operation” is “Directly Control[led]” by a “Signal of the Third Input Terminal”



Ex. 1006 (Tobita) at Fig. 20;
see also Paper 1 (Petition) at 84, 87

Tobita's Transistors Q3-Q5 and Q18-Q21 Collectively “Control” “the Voltage of the Second Node” in Response to the Claimed “Signals”



Ex. 1006 (Tobita), Figs. 9, 20;
Ex. 1003 (Foty Dec.), ¶¶ 610-621;
see also Paper 1 (Petition) at 84-85

Overview of Argument

Introduction

Kimura renders the independent claims obvious

Kimura also teaches the dependent claim limits

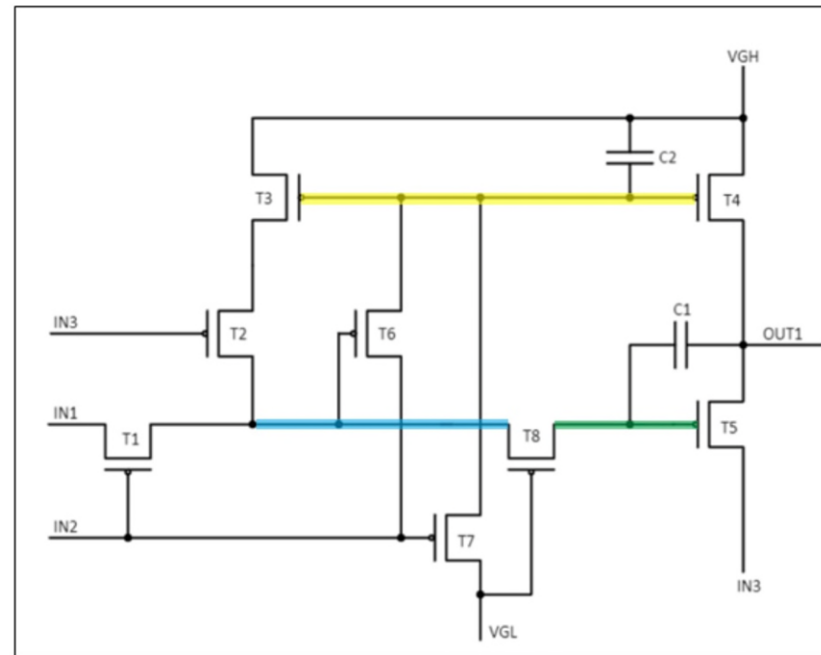
Sasaki improves Shin's stage circuit

Tobita includes the claimed "first driver" "transistor"

Patent Owner's deficient "secondary considerations"

Patent Owner's Claim Charts Are Ambiguous

For example, in the annotated Mengtor Equivalent Circuit below, the first node is a point or area of interconnection between the gates of transistors **T3** and **T4** in the region highlighted in yellow. The second node is a point or area of interconnection between the output of the first driver and the source of transistor **T8** in the region highlighted in blue (or can also be between the drain of transistor **T8** and the gate of transistor **T5** in the region highlighted in green).



Paper 23 (PO Response) at 63;
Ex. 2046 (Claim Chart) at 6

There Are Multiple Additional Issues With Patent Owner's Arguments

- ✗ None of the claims impose limits on the number of transistors used
- ✗ The prior art teaches stage circuits using fewer transistors than the '593 patent
- ✗ The claims and specification do not mention AMOLED displays, mobile devices, or bezel sizes
- ✗ Patent Owner previously argued that the success of the same purported commercial embodiment at issue here is attributable to its pixel geometry

Paper 29 (Reply) at 25-27