

Mianyang BOE Optoelectronics Technology Co., Ltd. (“BOE”); Wuhan China Star Optoelectronics Semiconductor Display Technology Co., Ltd.; Tianma Microelectronics Co. Ltd.; and Visionox Technology, Inc.
v.
Samsung Display Co., Ltd.

Case No. IPR2024-00620
U.S. Patent No. 9,330,593

Patent Owner’s Demonstratives

June 13, 2025 Oral Hearing

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SDC EX. 2064

The challenged '593 Patent

(12) **United States Patent**
Jang

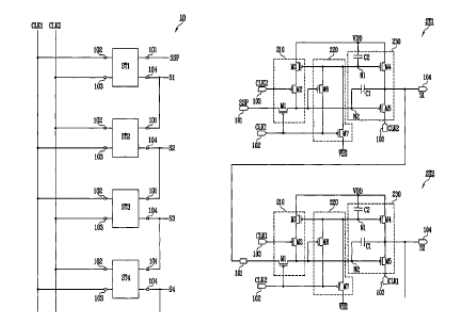
(10) **Patent No.:** **US 9,330,593 B2**
(45) **Date of Patent:** **May 3, 2016**

(54) **STAGE CIRCUIT AND ORGANIC LIGHT
EMITTING DISPLAY USING THE SAME**

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(73) Assignee: **SAMSUNG DISPLAY CO., LTD.,
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(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 184 days.
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G09G 3/32 (2006.01)
H05L 7/00 (2006.01)
G09G 3/32 (2016.01)
(52) **U.S. Cl.**
CPC .. **G09G 3/32** (2013.01); **G09G 3/32** (2013.01);
H05L 7/00 (2013.01)
(58) **Field of Classification Search**
CPC **G09G 3/3677**; **G09G 2310/0286**
USPC **345/98-100**
See application file for complete search history.

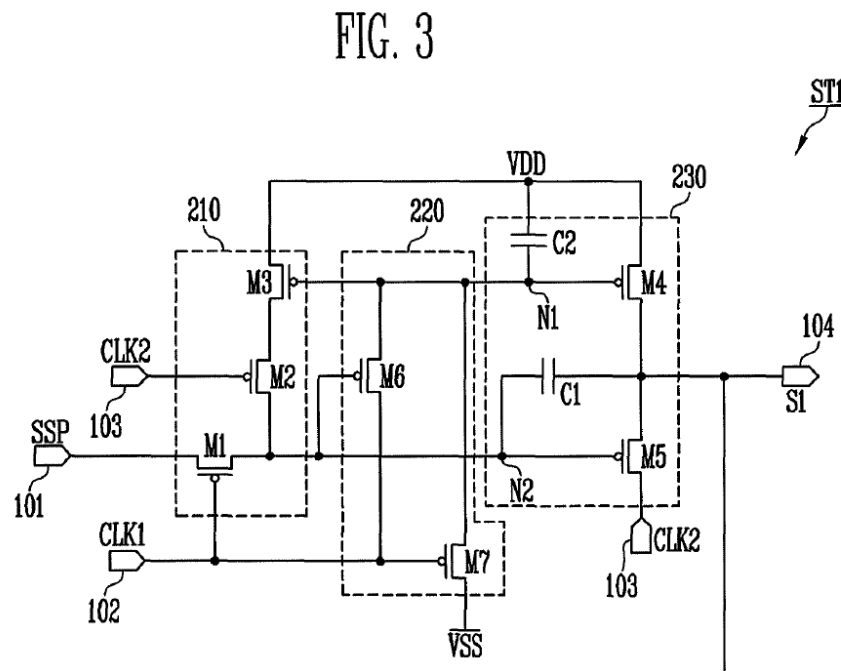
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(57) **ABSTRACT**
A stage circuit includes an outputting unit having a first node and a second node, the output unit configured to supply a voltage of a first power supply or a voltage of a third input terminal to an output terminal in accordance with voltages applied to the first node and the second node, a first driver configured to control the voltage of the second node in accordance with signals of a first input terminal, a second input terminal, and the third input terminal, and a second driver configured to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node.
28 Claims, 7 Drawing Sheets



The image contains two circuit diagrams. The left diagram shows a stage circuit with multiple input terminals (100, 110, 120, 130, 140) and output terminals (150, 160, 170, 180, 190). It includes transistors (200, 210, 220, 230, 240, 250, 260, 270, 280, 290, 300, 310, 320, 330, 340, 350, 360, 370, 380, 390, 400, 410, 420, 430, 440, 450, 460, 470, 480, 490, 500, 510, 520, 530, 540, 550, 560, 570, 580, 590, 600, 610, 620, 630, 640, 650, 660, 670, 680, 690, 700, 710, 720, 730, 740, 750, 760, 770, 780, 790, 800, 810, 820, 830, 840, 850, 860, 870, 880, 890, 900, 910, 920, 930, 940, 950, 960, 970, 980, 990, 1000, 1010, 1020, 1030, 1040, 1050, 1060, 1070, 1080, 1090, 1100, 1110, 1120, 1130, 1140, 1150, 1160, 1170, 1180, 1190, 1200, 1210, 1220, 1230, 1240, 1250, 1260, 1270, 1280, 1290, 1300, 1310, 1320, 1330, 1340, 1350, 1360, 1370, 1380, 1390, 1400, 1410, 1420, 1430, 1440, 1450, 1460, 1470, 1480, 1490, 1500, 1510, 1520, 1530, 1540, 1550, 1560, 1570, 1580, 1590, 1600, 1610, 1620, 1630, 1640, 1650, 1660, 1670, 1680, 1690, 1700, 1710, 1720, 1730, 1740, 1750, 1760, 1770, 1780, 1790, 1800, 1810, 1820, 1830, 1840, 1850, 1860, 1870, 1880, 1890, 1900, 1910, 1920, 1930, 1940, 1950, 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The '593 Patent's stage circuit

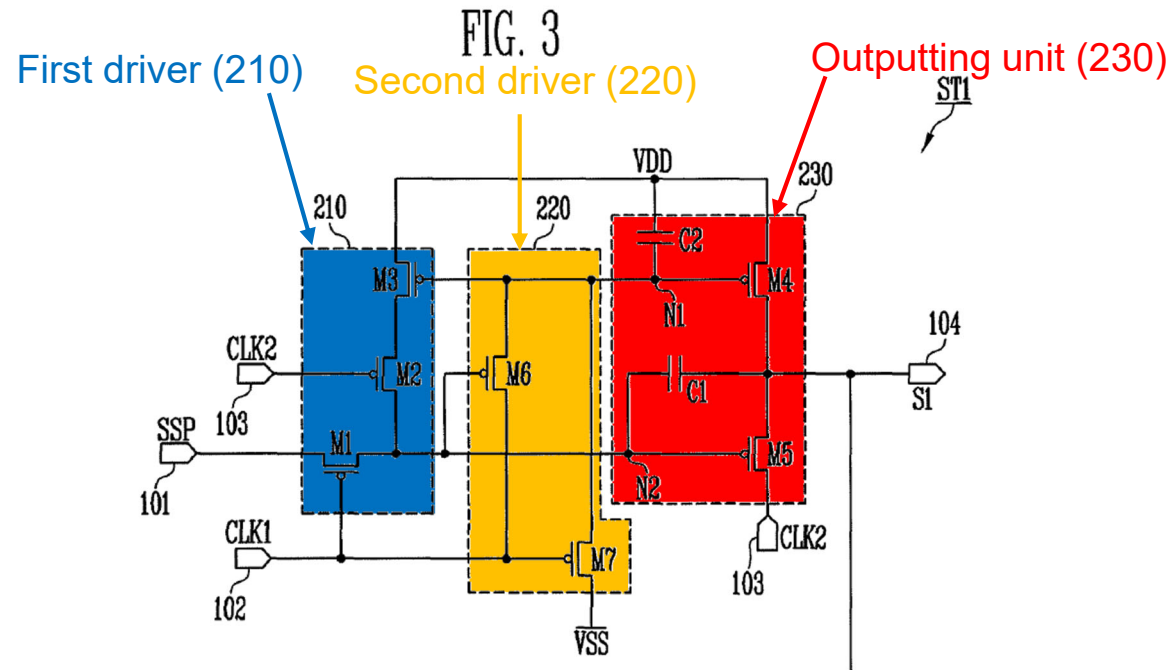


'593 Patent Fig. 3

By way of summation and review, embodiments provide stages having a reduced number of transistors and that output scan signals only using first and second clock signals. In contrast, conventional stage circuits includes a plurality of transistors, e.g., at least ten transistors, to supply the scan signals and/or require use of initializing signal in addition to the first and second clock signals. When a number of transistors in a stage increases, process yield deteriorates, so that stability of driving is deteriorated. When more initializing signals are required, there is less time for supplying scan signals, thereby reducing stability. When a number of transistors is increased and/or more initializing signals are required, complexity increases. Therefore, stages according to embodiments, and an organic light emitting display using the same, improve stability and reduce complexity.

'593 Patent at 9:12-26

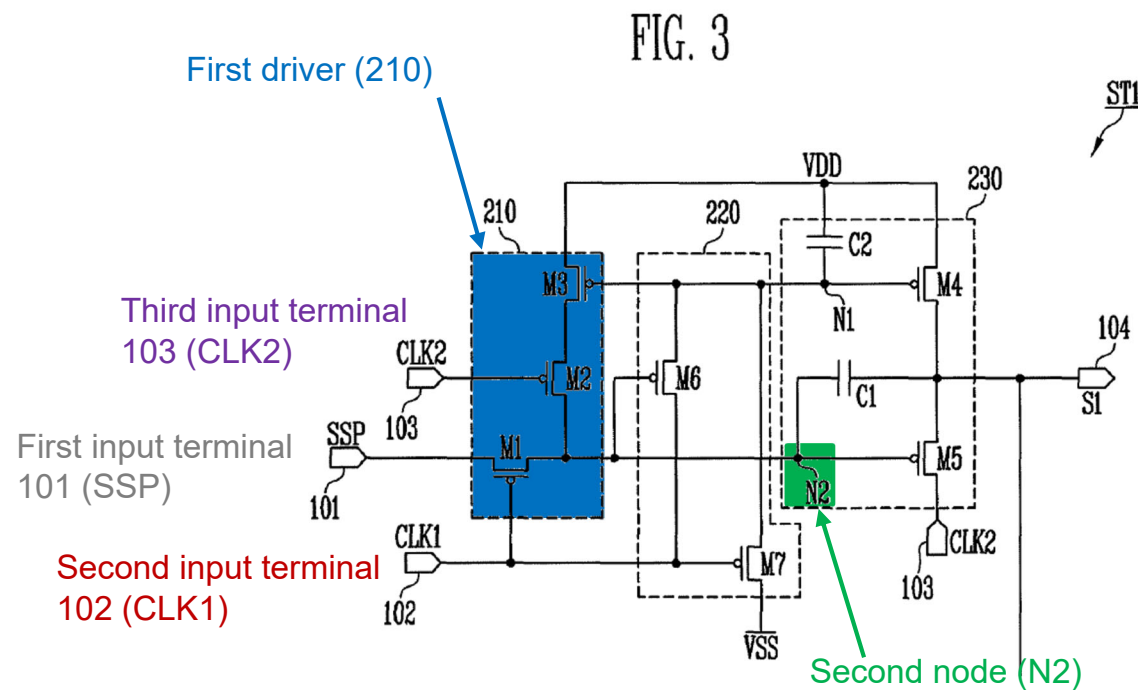
The '593 Patent's stage circuit



'593 Patent Fig. 3

- The claimed invention comprises a first driver, a second driver, and an outputting unit

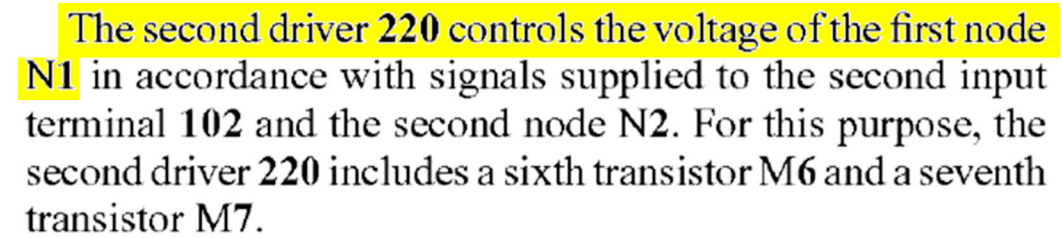
The '593 Patent's first driver



'593 Patent Fig. 3

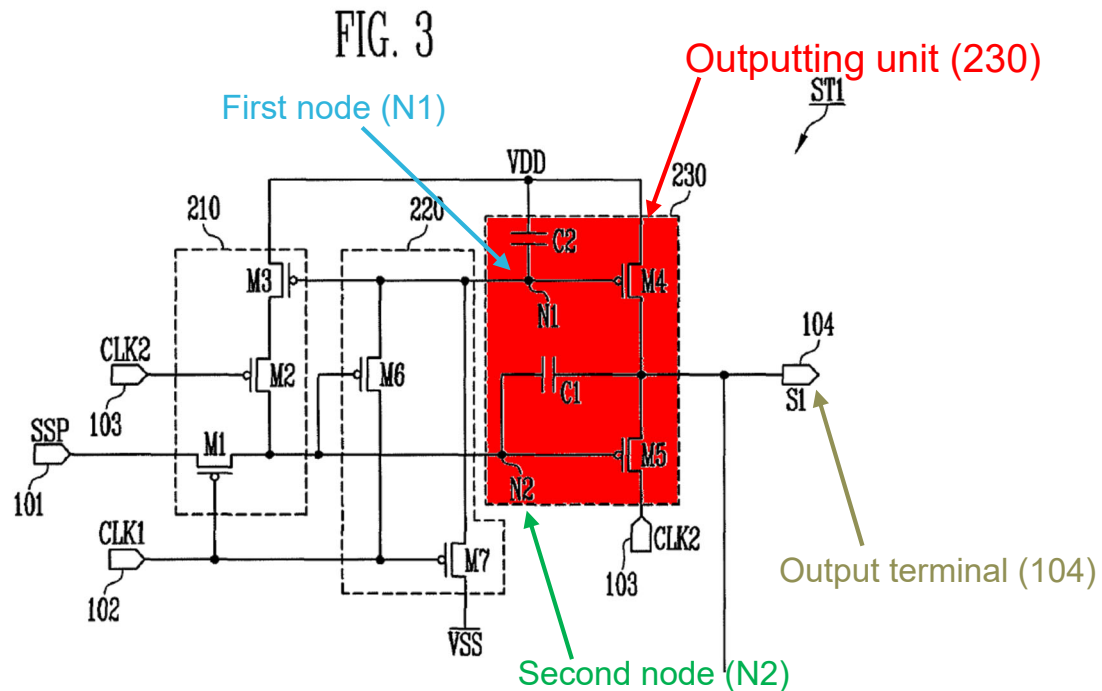
The first driver 210 controls the voltage of the second node N2 in accordance with signals supplied to the first input terminal 101 to the third input terminal 103. For this purpose, the first driver 210 includes a first transistor M1, a second transistor M2, and a third transistor M3.

'593 Patent at 5:63–67



'593 Patent at 6:22–26

The '593 Patent's outputting unit



'593 Patent Fig. 3

The outputting unit 230 controls a voltage supplied to the output terminal 104 in accordance with voltages applied to a first node N1 and a second node N2. For this purpose, the outputting unit 230 includes a fourth transistor M4, a fifth transistor M5, a first capacitor C1, and a second capacitor C2.

'593 Patent at 5:37–41

Overview of challenge

- The petition proposed five grounds of unpatentability:
 1. Obviousness of claims 1–8, 14–22, and 25 over [Kimura](#)
 2. Obviousness of claims 1–6, 8, 14–20, 22 and 25 over [Shin](#) and [Sasaki](#)
 3. Obviousness of claims 7 and 21 over [Shin](#), [Sasaki](#), and [Jeong](#)
 4. Obviousness of claims 1–2 and 15–18 over [Tobita](#)
 5. Obviousness of claims 7 and 21 over [Tobita](#) and [Jeong](#)

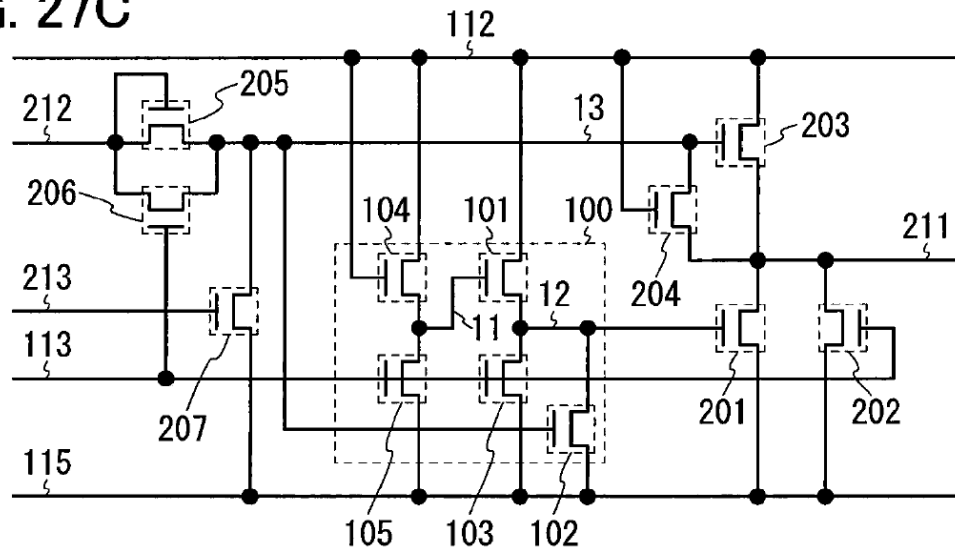
Kimura

Claims 1–8, 14–22, and 25

The Petition's theory

- The Petition relied on Kimura Fig. 27C for its obviousness arguments, acknowledging that Kimura “does not itself mention” each claimed element for Fig. 27C

FIG. 27C



Kimura Fig. 27C

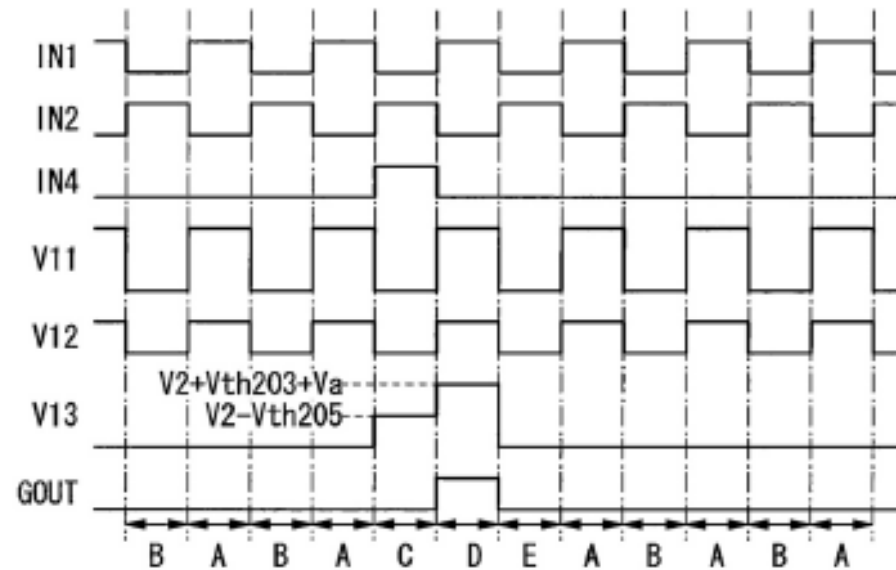
This ground is expressed in terms of obviousness, and not anticipation, because the portion of Kimura discussing Figure 27C does not itself mention all the depicted transistors, inputs, and outputs. Kimura explains, however, that the device

Petition at 15

The Petition's theory

- The Petition sought to apply the timing diagram of Figure 21B to the circuit of Figure 27C

FIG. 21B



Kimura Fig. 21B

Figure 21B provides an example “timing chart for illustrating operation of the semiconductor device[.]” *Id.*, [0062], [0066]. While the chart is not specific to the device of Figure 27C, a POSITA would have understood that that device—because it includes the same input and output lines and many of the same transistors as Kimura’s other circuits—would (or at least obviously could) be supplied with input signals in the same manner and with the same timing. *See Decl.*, ¶¶ 160-165.

Petition at 19

Inconsistencies in the Petition's theory

We agree with Patent Owner that Petitioner's analysis includes inconsistencies that are not sufficiently explained. Patent Owner is correct (Prelim. Resp. 22) that Petitioner cites Kimura's description of different circuits, i.e., the circuits in Figures 18A, 19A, and 19B, to show how the circuit of Figure 27C works in operation as part of its analysis of limitation [1-A]. Pet. 18 (citing Ex. 1004 ¶¶ 253, 255, 256). Although Petitioner and Dr. Foty contend that "shared components . . . would obviously be connected—and function—in the same way discussed elsewhere" (*id.* at 15; Ex. 1003 ¶ 146), they do not explain sufficiently why a different arrangement of such components would yield the same results.

DI at 25

- Petitioner does not explain why a different arrangement of components would yield the same results

Inconsistencies in the Petition's theory

Specifically, Petitioner relies on the timing diagram in Figure 21B of Kimura to illustrate the operation of the circuit in Figure 27C. Pet. 19 (reproducing Ex. 1004, Fig. 21B). Petitioner acknowledges that the timing diagram “is not specific to the device of Figure 27C.” *Id.* Still, Petitioner contends the Figure 27C circuit “would (or at least obviously could) be supplied with input signals in the same manner and with the same timing” because it includes “the same input and output lines and many of the same transistors as Kimura’s other circuits.” *Id.* (citing Ex. 1003 ¶¶ 160–165).

- Kimura’s description of Fig. 27C circuit operation is inconsistent with the Figure 21B timing diagram

DI at 26
level.” Pet. 18 (quoting Ex. 1004 ¶ 256). Yet Kimura describes the Figure 27C circuit’s operation at period D differently: “[I]n a period D, the potential of the node 13 can be *lowered*. Therefore, dielectric breakdown or deterioration of the transistor connected to the node 13 (e.g., the transistor 102, the transistor 203, the transistor 205, or the transistor 206) can be prevented.” Ex. 1004 ¶ 286 (emphasis added). And Petitioner cites this very teaching in its analysis of limitation [1-B]. *See* Pet. 20–21. This inconsistency undermines Petitioner’s argument that “the device of Figure 27C . . . would (or at least obviously could) be supplied with input signals in the same manner and with the same timing.” *Id.* at 19.

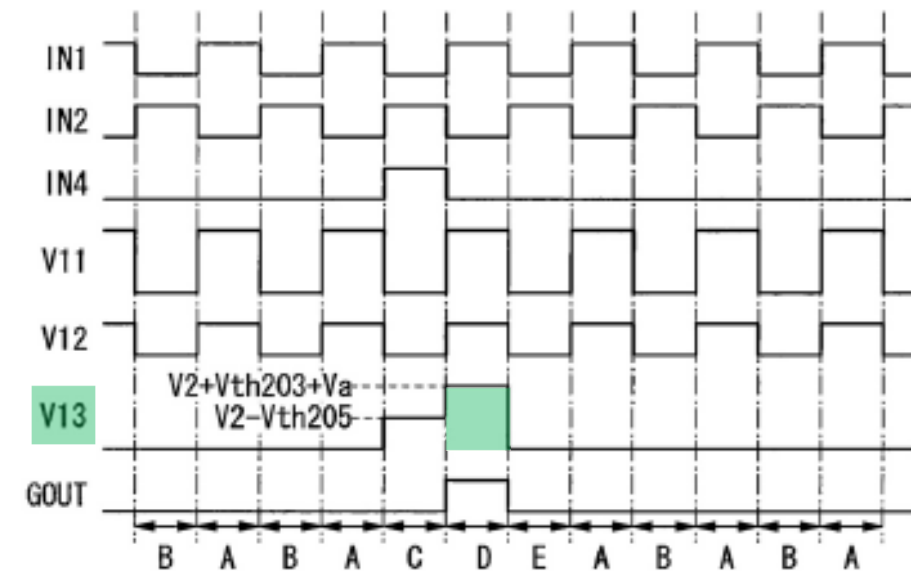
DI at 26

The timing diagram is incompatible with the Figure 27C circuit

[0286] FIG. 27C illustrates a structure where the first terminal of the transistor 204 is connected to the wiring 211 and the gate of the transistor 204 is connected to the wiring 112 in the semiconductor device in FIG. 27A. Thus, in a period D, the potential of the node 13 can be lowered. Therefore, dielectric breakdown or deterioration of the transistor connected to the node 13 (e.g., the transistor 102, the transistor 203, the transistor 205, or the transistor 206) can be prevented.

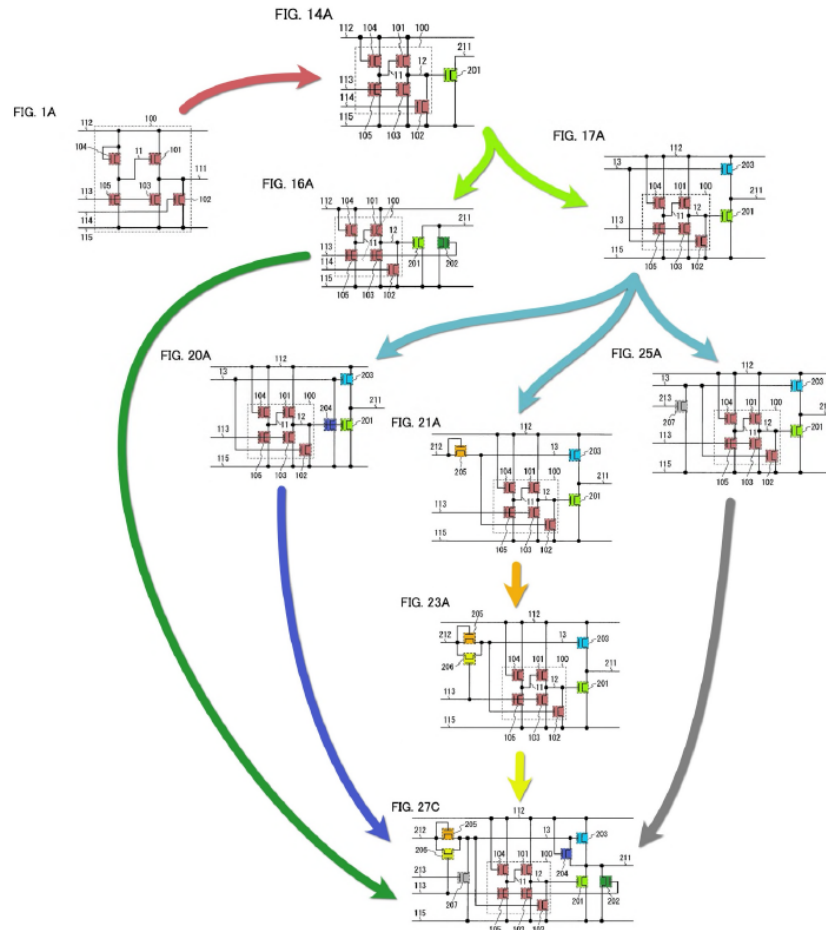
Kimura ¶ [0286]

FIG. 21B



Kimura Fig. 21B (annotated)

Petitioner's Reply theory



Petitioner Reply at 5

Q And you say that he's talking about the same types of stage circuits, but there is a number of different figures listed here in the top of 2 -- paragraph 285 that you just referenced, right?

A Yes. Those are all -- there is a number of embodiments, but the embodiments here as far as I can tell are all involving staged circuits, at least the ones I looked at which are intended to basically do the same sort of thing.

Ex. 2063 (Foty Tr.) 37:16–38:3

Petitioner now argues it relied on only the “input signals” of Figure 21B

Patent Owner focuses on Figure 21B’s internal node voltages. The Petition, however, relies on Figure 21B for its “*input signals*” IN1, IN2, and IN4 used to drive the circuit not the internal node voltages. Petition, 19 (emphasis added). And these

Pet. Reply at 6

37. Figure 20A shows the addition of transistor 204 (**dark blue**). *Id.*, [0260]-[0261]. This transistor is intended to allow the “potential of ... node 13” to be “lowered” for the purpose of reducing the risk of transistor deterioration. *Id.*, [0262]. Note in particular (as will further be explained below) that the potential (i.e. the voltage) at node 13 will differ across the circuit embodiments – as the voltage at node 13 is *not* an input signal to circuitry, but rather is a consequence when the same input signals are applied to the different circuitries of the different embodiments.

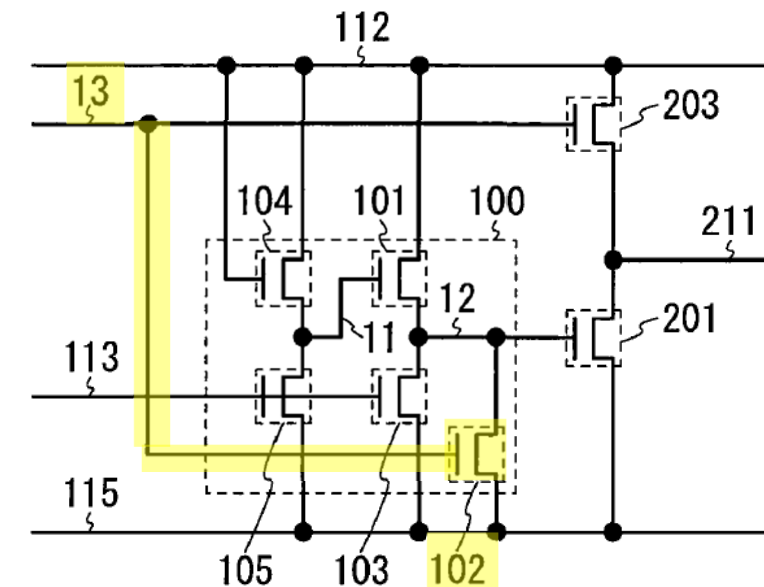
Ex. 1025 (Foty Reply Dec.) ¶ 37

Yet Kimura teaches “internal node voltages” used as “input signals”

[0249] FIG. 17A illustrates a structure where the transistor 203 is additionally provided in the semiconductor device in FIG. 14A. The transistor 203 is an n-channel transistor. However, this embodiment is not limited to this, and the transistor 203 can be a p-channel transistor. A first terminal of the transistor 203 is connected to the wiring 112. A second terminal of the transistor 203 is connected to the wiring 211. Further, a gate of the transistor 203 is denoted by a node 13. Note that the gate of the transistor 102 can be connected to the node 13. Therefore, a potential of the node 13 (V_{13}) can be used as the signal IN3.

Kimura ¶ [0249]

FIG. 17A



Dr. Foty admitted that in Kimura “internal node voltages” are used as “input signals”

12 Q And so again we've got Node 13 as the
13 signal IN3 connected to the gate of the Transistor
14 102.

15 Is that right?

16 A Kimura so identifies it, yes.

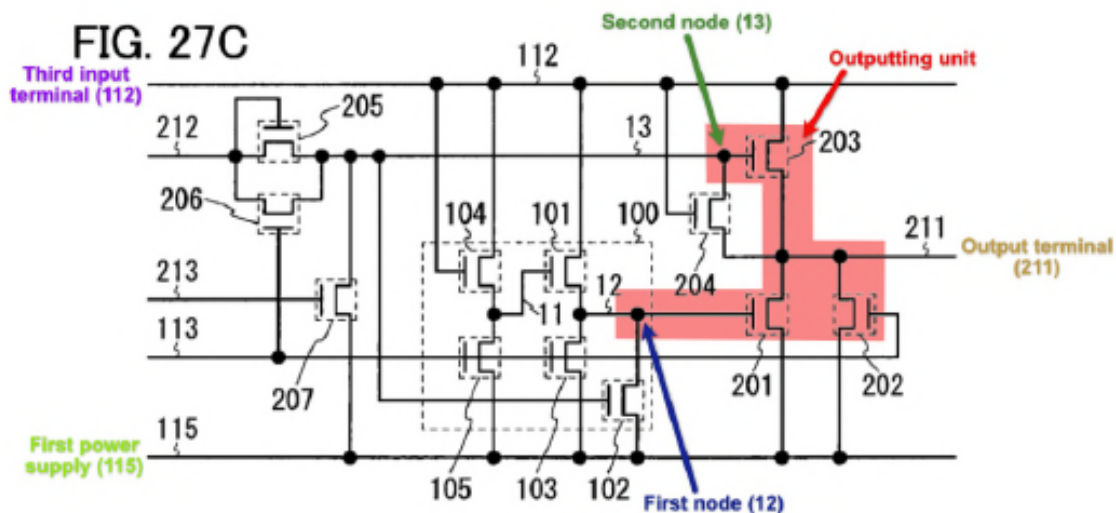
17 Q So the voltage at that node is an input
18 signal to this Figure 20A. Correct?

19 A Kimura describes using it to receive that
20 input signal to that Wiring 13, yes.

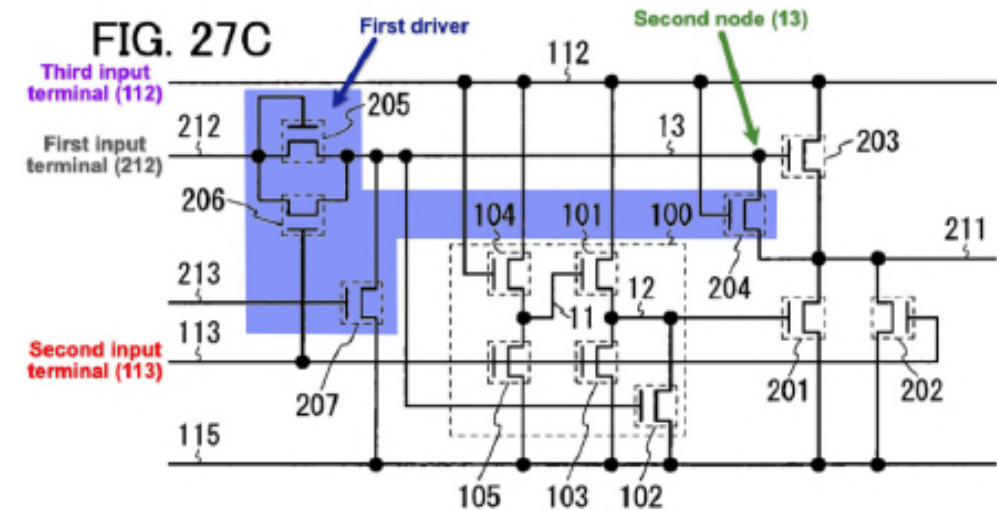
Ex. 2062 (Foty Tr.) 32:12–20

Petitioner's contradictory theories for “outputting unit” and “first driver” in independent and dependent claims

Petitioner's identification of “**outputting unit**” for claim 1

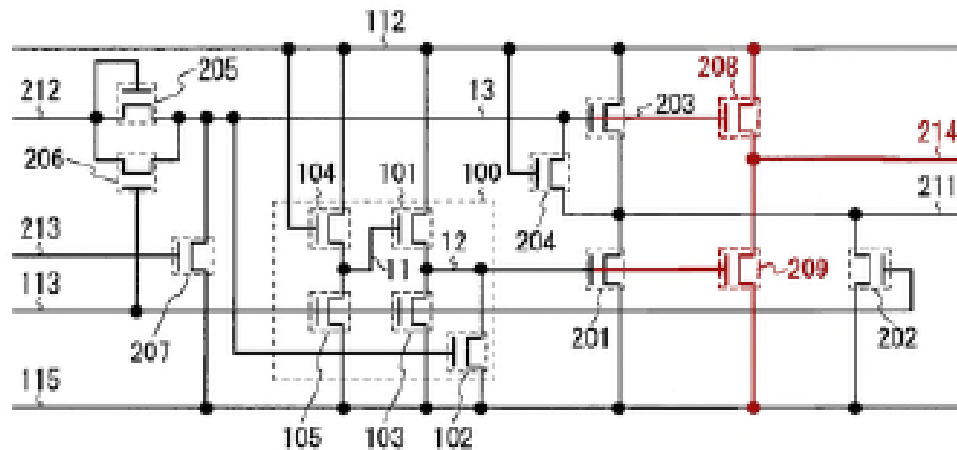


Petitioner's identification of “**first driver**” for claim 1

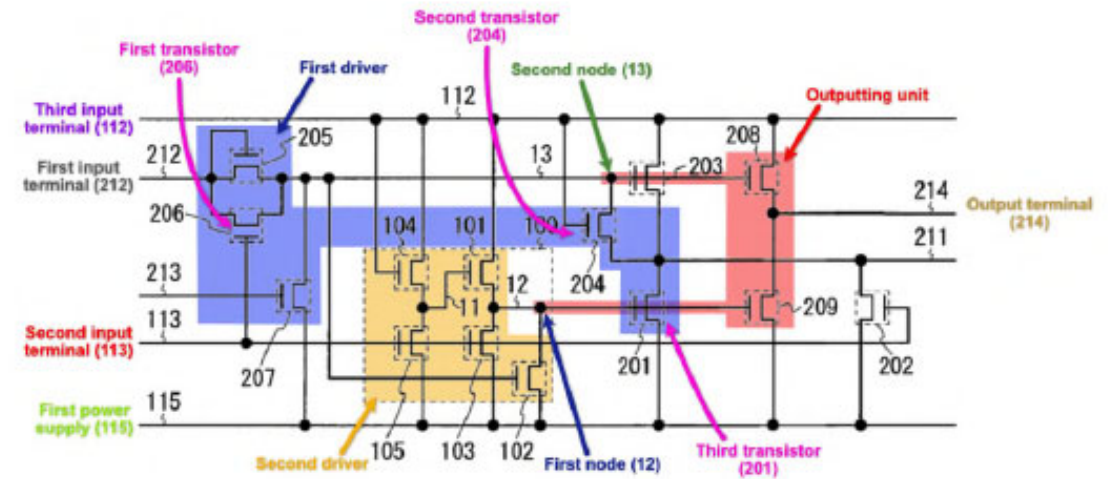


Petitioner's contradictory theories for “outputting unit” and “first driver” in independent and dependent claims

Petitioner's composite circuit for claim 6 (added elements in red)

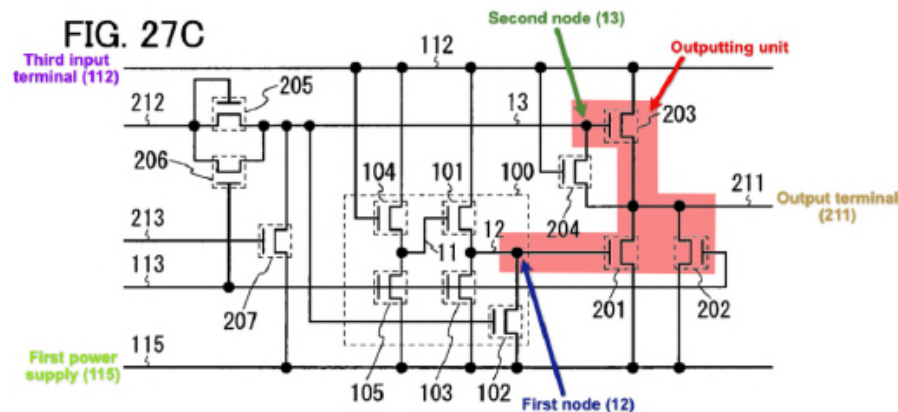


Petitioner's identification of different “outputting unit” and “first driver” for claim 6

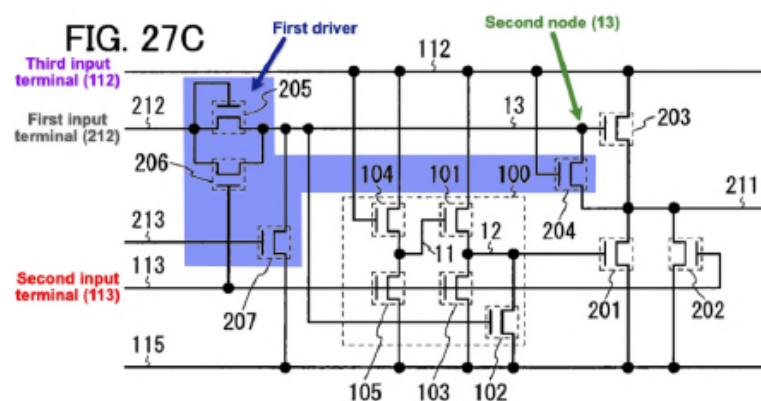


Petitioner's contradictory theories for “outputting unit” and “first driver” in independent and dependent claims

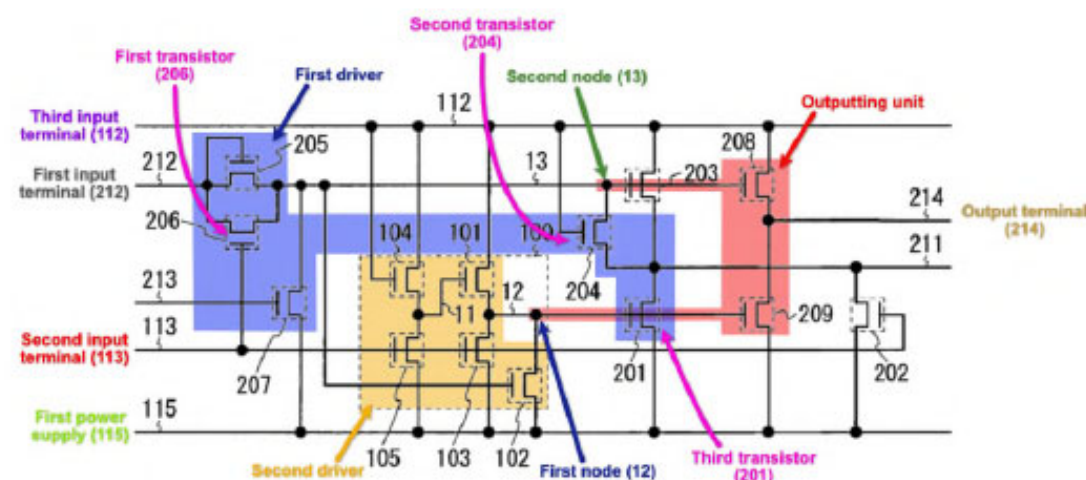
Petitioner's identification of “**outputting unit**” for claim 1



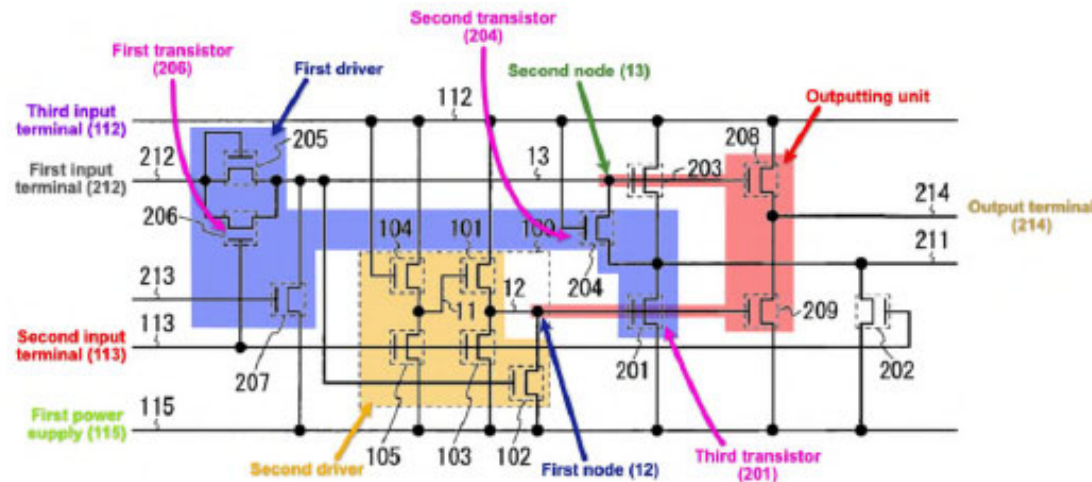
Petitioner's identification of “**first driver**” for claim 1



Petitioner's identification of different “**outputting unit**” and “**first driver**” for claim 6



Petitioner's “outputting unit” for claim 6 is not connected to an actual output terminal



Petition at 31

- SOUT is not output to the display

[0304] In the structures illustrated in FIGS. 10A to 10C, FIG. 14A, FIG. 16A, FIG. 17A, FIG. 20A, FIG. 21A, FIG. 23A, FIG. 25A, FIGS. 27A to 27C, FIGS. 28A to 28C, FIGS. 29A to 29C, FIGS. 30A to 30C, and FIGS. 47A and 47B, a signal which is different from the signal GOUT can be generated. For example, in the semiconductor device of this embodiment, when a signal SOUT is generated in addition to the signal GOUT and a plurality of semiconductor devices are connected, the signal SOUT is not output to the wiring 211 but can be input to a semiconductor device in a different stage as a start pulse. Thus, the degree of delay or distortion of the

According to Kimura, its devices—including that in Figure 27C—can be provided with additional transistors 208 and 209. Kimura, [0304]. These transistors facilitate generation of a “different” output “signal SOUT” for “input to a semiconductor device in a different stage as a start pulse.” *Id.* Using this signal

Kimura ¶ [0304]

Petition at 29

Claims 7 and 21 require capacitors not included in Figure 27C

Ex. 1004, Fig. 27C (annotations added). As can be seen by inspection, this embodiment of Kimura has all of the claim elements of Claim 7 – except for the first capacitor and the second capacitor.

Ex. 1003 (Foty) at ¶ 248

Kimura never describes adding capacitors to Figure 27C

Dr. Foty's theory

259. For example, a “capacitor 122” can be connected between wiring 115 and the wiring leading to the gate of a transistor (like transistor 103 in Figure 1A) that generates the circuit’s output signal. *Id.*, ¶¶ [0190]-[0191]. An example of this inclusion is provided by Kimura in Figure 9C:

Ex. 1003 (Foty) ¶ 259

260. Additionally, Kimura describes how a “capacitor 220” can be “connected between the node 13” and output “wiring 211.” *Id.*, ¶ [0302]. An example of this inclusion is provided by Kimura in Figure 30C:

Ex. 1003 (Foty) ¶ 260

Dr. Wolfe's response

74. Dr. Foty looks to Figure 9C and Figure 30C, and asserts that Kimura “advises that ‘[c]apacitors can be additionally provided’ along with the transistors in its shift register.” Ex. 1003 at ¶ 258. Dr. Foty cites to Kimura ¶ [0198], but this paragraph says nothing about adding capacitors to Figure 27C. Kimura ¶ [0198] (“In the structures illustrated in FIG. 1A, FIGS. 6A to 6F, FIGS. 7A to 7E, FIGS. 9A and 9B, and FIGS. 11A and 11B, the transistors can be replaced with capacitors. For example, the capacitors can be additionally provided without elimination of the transistors.”). This does not suggest that these capacitors from different embodiments can or should be added to Figure 27C. Nor is there any explanation of how the timing or operation of the proposed design would not substantially change due to the addition of these capacitors and the delays they induce.

Ex. 2059 (Wolfe Dec.) ¶ 74

Claims 7 and 21 – Petitioner’s rationale for adding capacitors has no support beyond conclusory testimony

252. This can be problematic, since perturbations in the amount of charge (for example, due to electromagnetic interference (EMI) or interline crosstalk during digital switching events) may cause sizeable changes in the voltage on the node; these types of signal integrity issues are undesirable. Therefore, a POSITA would be motivated to seek methods of making the circuitry of Kimura more robust against a problem of this sort by including further capacitors.

Ex. 1003 (Foty) at ¶ 252

Cf. DI at 58 (recognizing, for Tobita ground, that “Petitioner’s rationale for adding a capacitor to Tobita’s circuit is based on hypothetical concerns.”)

A POSITA would not have added capacitors to Figure 27C

78. The Petition asserts that “Kimura itself contemplates that the capacitors can be employed” and that the “device’s output signal is improved when the capacitors are used.” Pet. at 34. Setting aside that, as discussed above, Kimura does not teach or suggest adding capacitors to Figure 27C, and that the Petition adds them in a manner inconsistent with Kimura’s teachings, Petitioner and Dr. Foty again overlook the significant detriments that would be incurred by adding two capacitors to a stage circuit. Capacitors take up significant circuit area, and this, along with the necessary connections to other circuit elements would have to be taken into account in designing a modified stage circuit. Generalized assertions that these capacitors could be added to Figure 27C would not provide a POSITA sufficient motivation to incur these detriments.

Ex. 2059 (Wolfe Dec.) ¶ 78

Claims 8 and 22 require arrangement of transistors and “second power supply” not found in the Figure 27C circuit

Kimura, Fig. 27C; *see also supra* limit [1-C]; Decl., ¶¶ 267-270. While none of Figure 27C’s transistors are connected in the way the claim requires, Kimura provides a number of design alternatives for use with its devices. For instance, “the

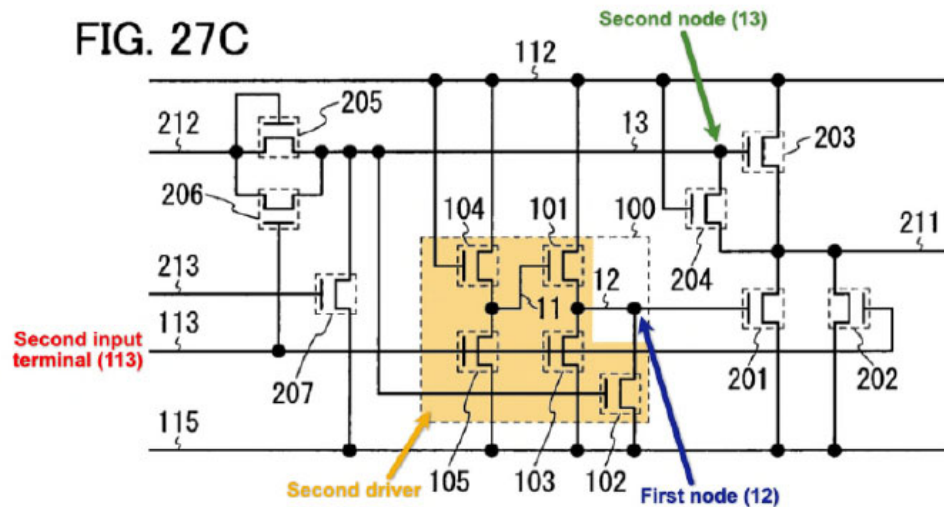
Pet. at 35

Next, Kimura explains that its devices can employ “a power supply voltage, reference voltage, ground voltage, ground, or negative power supply voltage.”

Kimura, [0105]. Moreover, Kimura also teaches that the same device can be provided with multiple different power supply voltages. *See id.*, [0173], [0299]. For

Pet. at 36

Claims 8 and 22 require arrangement of transistors and “second power supply” not found in the Figure 27C circuit



Pet. at 35

- No sixth transistor between the first node and the second input terminal with gate coupled to second node
- No second power supply, let alone “second power supply having a lower voltage than the first power supply”
- No seventh transistor between the first node and second power supply with gate coupled to second input terminal

Petitioner provides no rationale for modifications

Dr. Foty's theory

271. However, while none of Figure 27C's transistors are connected in the way the claim requires, Kimura provides a number of design alternatives (in the text of the specification) for use with its stage circuits.

Ex. 1003 (Foty Dec.) ¶ 271

274. Also, Kimura explains that its stage circuits can employ "a power supply voltage, reference voltage, ground voltage, ground, or negative power supply voltage." *Id.*, ¶ [0105]. Moreover, Kimura also teaches that the same stage circuit

Ex. 1003 (Foty Dec.) ¶ 274

Dr. Wolfe's response

84. Dr. Foty's theory also requires, in addition to changing the connections of the transistors in Figure 27C as he concedes, adding an additional power supply line to Figure 27C. Dr. Foty provides no explanation whatsoever for this proposed modification. Ex. 1003 at ¶¶ 274-278. Dr. Foty simply suggests that "Kimura also teaches that the same stage circuit can be provided with multiple different power supply voltages." Ex. 1003 at ¶ 274. For claims 1 and 15 Dr. Foty and Petitioner identify wiring 115 as the "first power supply." Ex. 1003 at ¶ 152; Pet. at 18. For claims 8 and 22, Dr. Foty points to a different embodiment (Figure 30A) and suggests that wiring 115b in that embodiment would satisfy the "second power supply" limitation of those claims. Ex. 1003 at ¶¶ 274-275. Dr. Foty does not explain what would be the "first power supply" in the proposed modification, explain what voltages would be provided by the purported "first" and "second" power supplies, or explain how the resulting modified circuit would function.

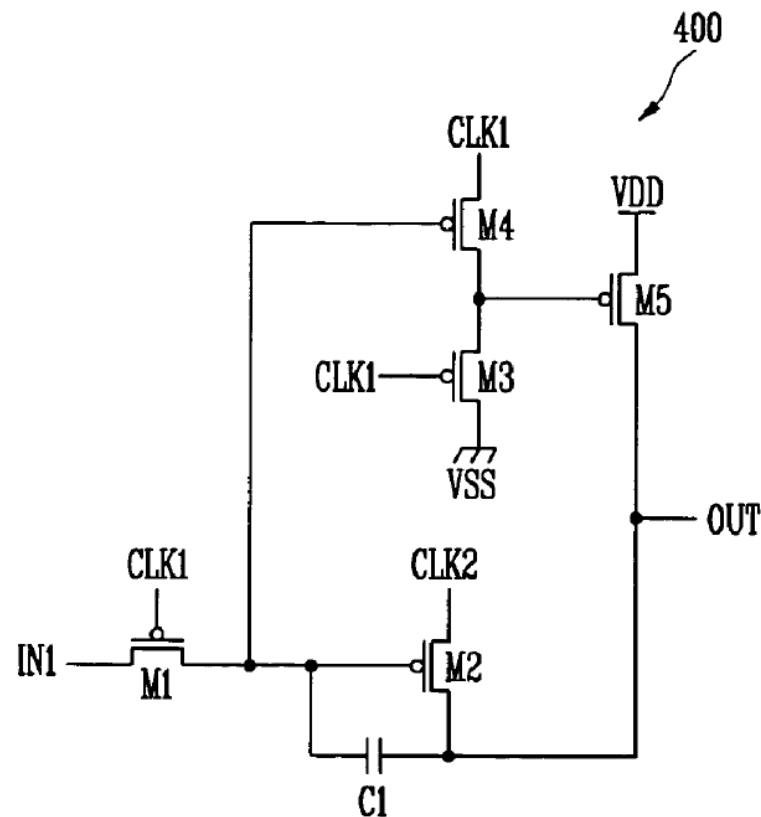
Ex. 2059 (Wolfe Dec.) ¶ 78

Shin and Sasaki

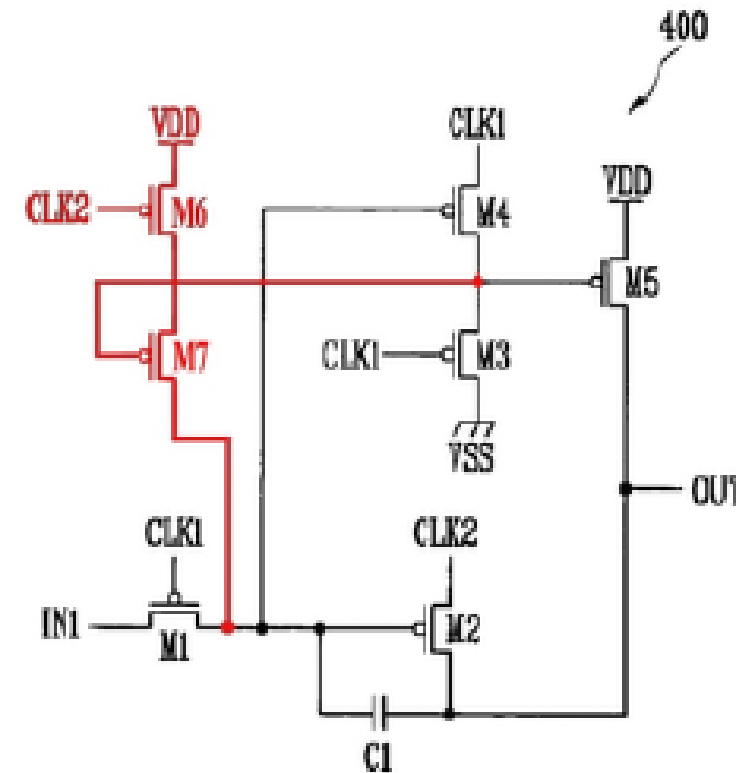
Claims 1–6, 8, 14–20, 22 and 25

Petition seeks to change Shin's circuit based on Sasaki to address "problem" of reversal

FIG. 11



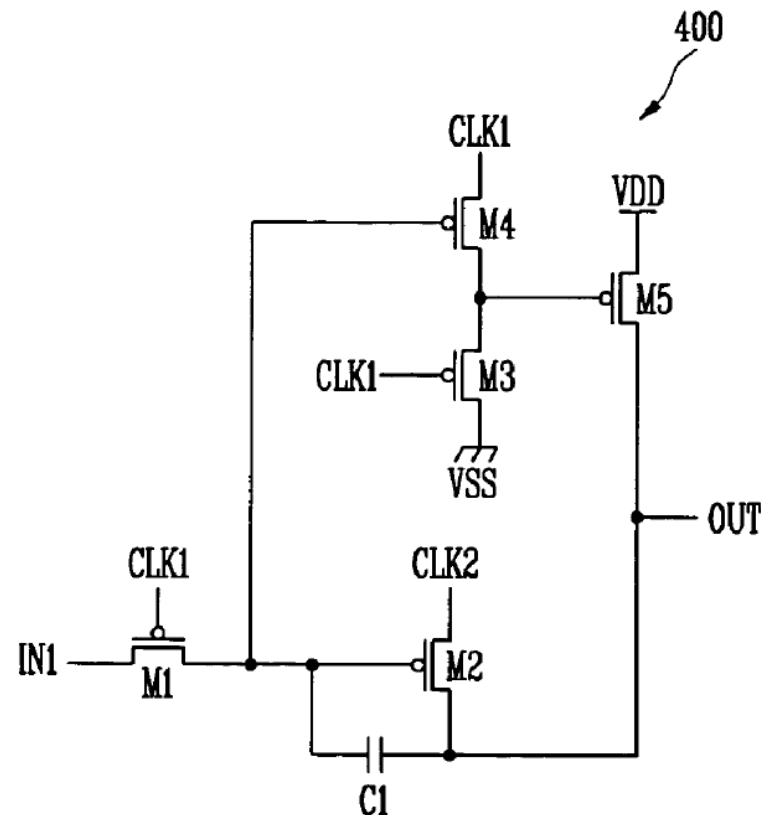
Shin Fig. 11



Petitioner's Modification of Shin (added elements from Sasaki in red)
Pet. at 50

Yet Shin's circuit already addresses potential reversal

FIG. 11



Shin Fig. 11

[0107] On the contrary, when the evaluation transistor M3 is turned-on, since the stage receives a low-level signal, namely, a gate terminal of the second transistor M2 is in a floating state, a voltage of the capacitor C1 remains unchanged, and thus the second transistor M2 continues to be turned-on that causes a second clock signal of high level to be output as an output signal.

Shin ¶ [0107]

Petitioner's alleged rationale is theoretical at best

Nevertheless, we agree with Patent Owner (Prelim. Resp. 41–42) that Petitioner does not sufficiently show that further reversal protection in Shin's circuit would have been necessary or even desirable. Although Petitioner alleges a “lack of robustness” in Shin's circuit (Pet. 49 (citing Ex. 1003 ¶¶ 387–389)), Petitioner's allegations are theoretical at best. *See*

Decision on Institution at 36

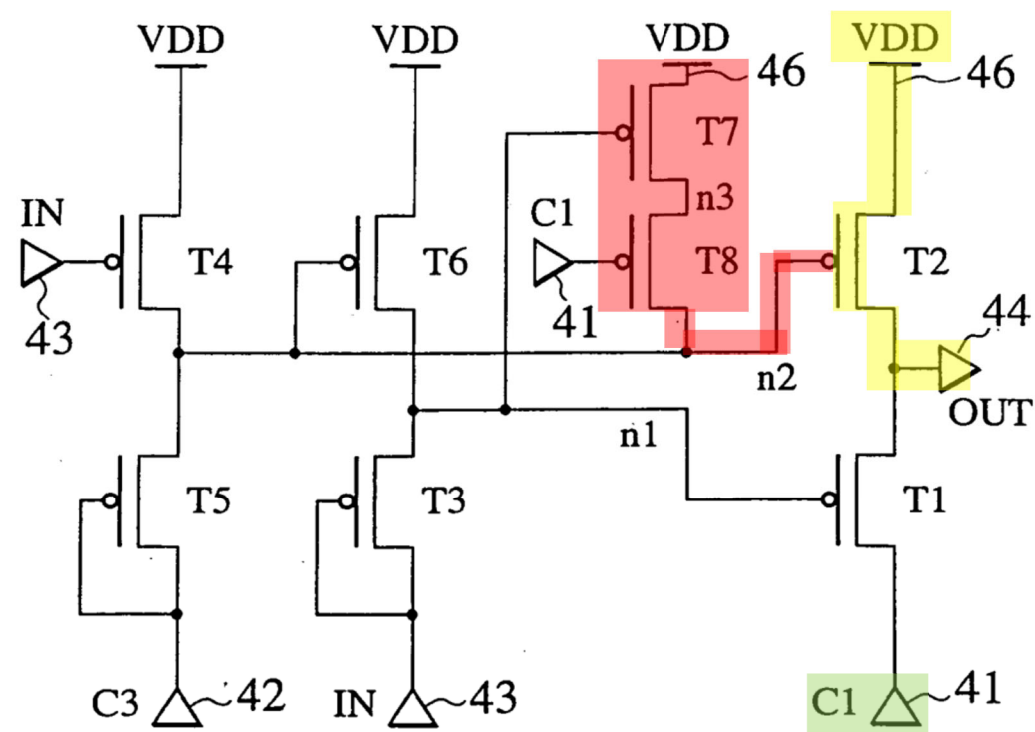
Petitioner misapplies Sasaki's teachings

97. In fact, Sasaki repeatedly describes potential distortion when the intended output signal is low and VDD is erroneously provided to the output terminal. *See, e.g.*, Ex. 1014 ¶ [0051] (“As a result, the output signal OUT at the low level without distortion will be supplied to the output terminal 44.”); *see also* Ex. 1014 at ¶¶ [0055], [0059], [0061], [0064], [0066]. Notably, Sasaki does not describe potential distortion in the opposite scenario (i.e., when the intended output signal is VDD but CLK2 is low and erroneously provided).

Ex. 2059 (Wolfe Dec.) ¶ 97

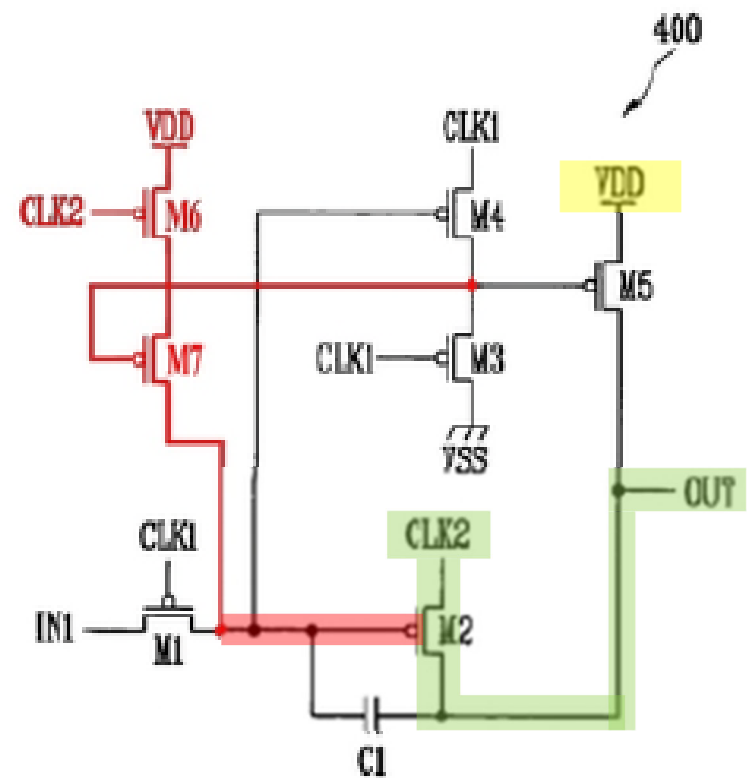
Petitioner misapplies Sasaki's teachings

Sasaki's anti-reversal circuit is connected to **VDD** transistor



Sasaki Fig. 4

Petitioner's modification attaches anti-reversal circuit to **CLK2** transistor



Pet. at 50 (annotated)

A POSITA would not have made Petitioner's modification

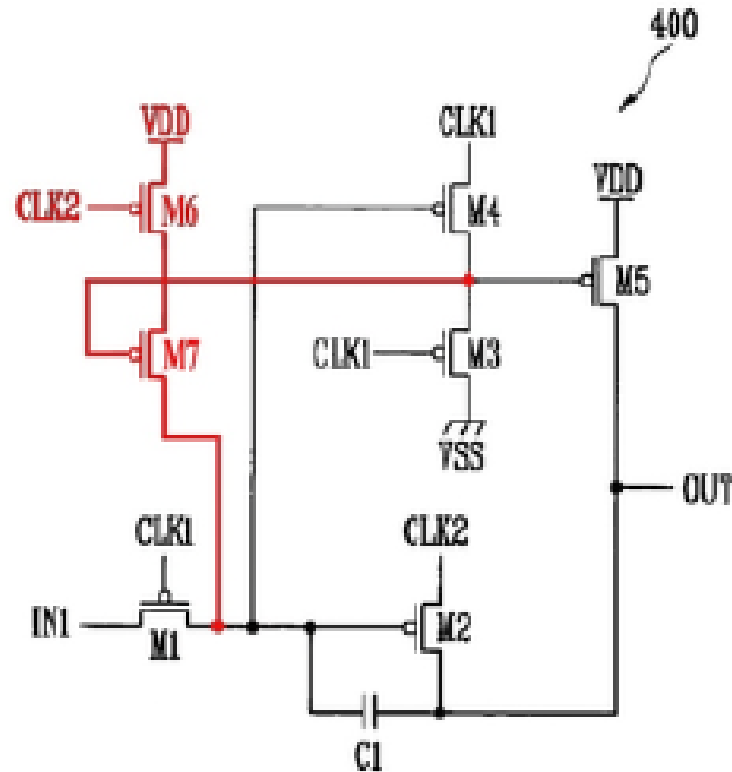
guarantee reversal protection.” Ex. 1003 at ¶ 385. But this is contradicted again by Shin’s provision of capacitor C1 and its teaching that C1 is sufficient to maintain the intended level at the gate of transistor M2. *See, e.g.*, Shin ¶ [0107]. Given that transistor M1 is enabled by a clock, the maximum time for which C1 must maintain its signal is known at design time and can easily be guaranteed. Dr. Foty points to nothing beyond generalized references to electromagnetic interference or crosstalk in support for his theory that Shin’s circuit may still be susceptible to reversal. But these are considerations that a POSITA would take into account in designing a circuit, and Shin teaches a circuit including a capacitor C1 that it teaches addresses such concerns. And Dr. Foty points to nothing in Shin that suggests that its capacitor C1 would be insufficient for this purpose. Moreover, he does not show that the additional transistors would be a meaningful improvement as the operation of M7 is still tied to the timing of CLK1.

Ex. 2059 (Wolfe Dec.) ¶ 92

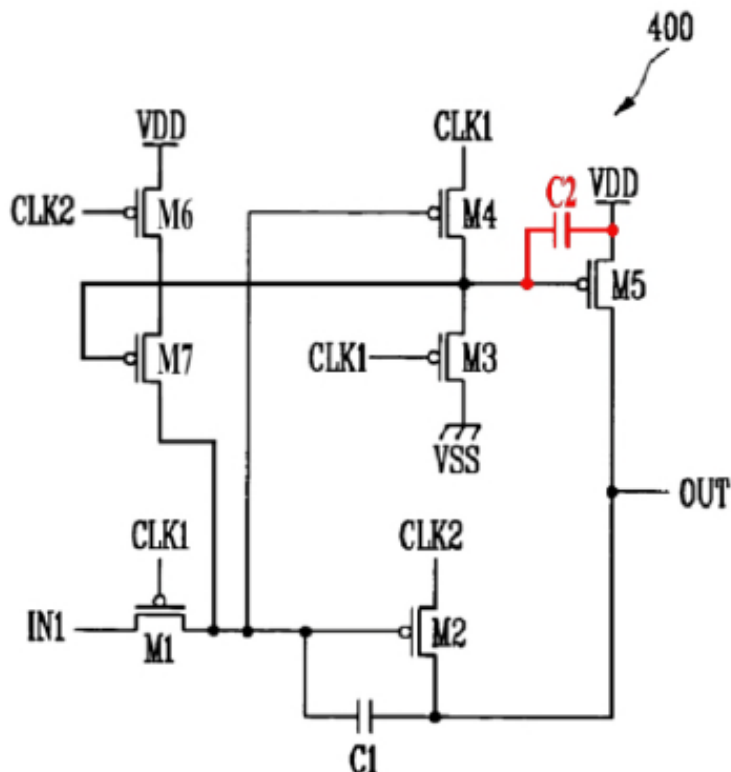
Shin, Sasaki, and Jeong

Claims 7 and 21

Claims 7 and 21 require further modifying the modified Shin circuit



Petitioner's modification of Shin (added elements from Sasaki in red)
Pet. at 50



Petitioner's further modification of Shin
(additional added element from Jeong in red)
Pet. at 78

Claims 7 and 21 – Petitioner’s rationale for adding capacitor has no support beyond conclusory testimony

579. This can be problematic, since perturbations in the amount of charge (for example, due to electromagnetic interference (EMI) or interline crosstalk during digital switching events) may cause sizeable changes in the voltage on the node; these types of signal integrity issues are undesirable. Therefore, a POSITA would

Ex. 1003 (Foty Dec.) ¶ 579

Cf. DI at 58 (recognizing, for Tobita ground, that “Petitioner’s rationale for adding a capacitor to Tobita’s circuit is based on hypothetical concerns.”)

A POSITA would not have added a capacitor to Shin

105. In sum, the generalized concerns Dr. Foty notes would not be sufficient to cause a POSITA to look to add an additional capacitor, let alone connect it in the specific way Dr. Foty does in order to arrive at the requirements of the claims. Dr. Foty's citations to Jeong, which teaches a different circuit with different circuit elements and connections, would similarly not motivate a POSITA to add additional circuit elements to the composite Shin and Sasaki circuit Dr. Foty creates.

Ex. 2059 (Wolfe Dec.) ¶ 105

Tobita

Claims 1–2 and 15–18

The Petition's theory: Q18–Q21 bringing N1 to a *low* level

- Petitioner asserted that transistors Q18–Q21 “control the voltage of the second node” in accordance with the signals of the first, second, and third input terminals *by bringing it to a low level*

See, e.g., Tobita, [0120]-[0121], [0125]. Transistors Q18-Q21—which receive signals from IN (the first input terminal), CK2 (the second input terminal), and CK1 (the third input terminal)—also control the voltage of the node N1 by, e.g., bringing it to a low level. Id., [0172], [0174]-[0177]. Transistors Q4 and Q5 likewise provide

Petition at 84–85 (annotated)

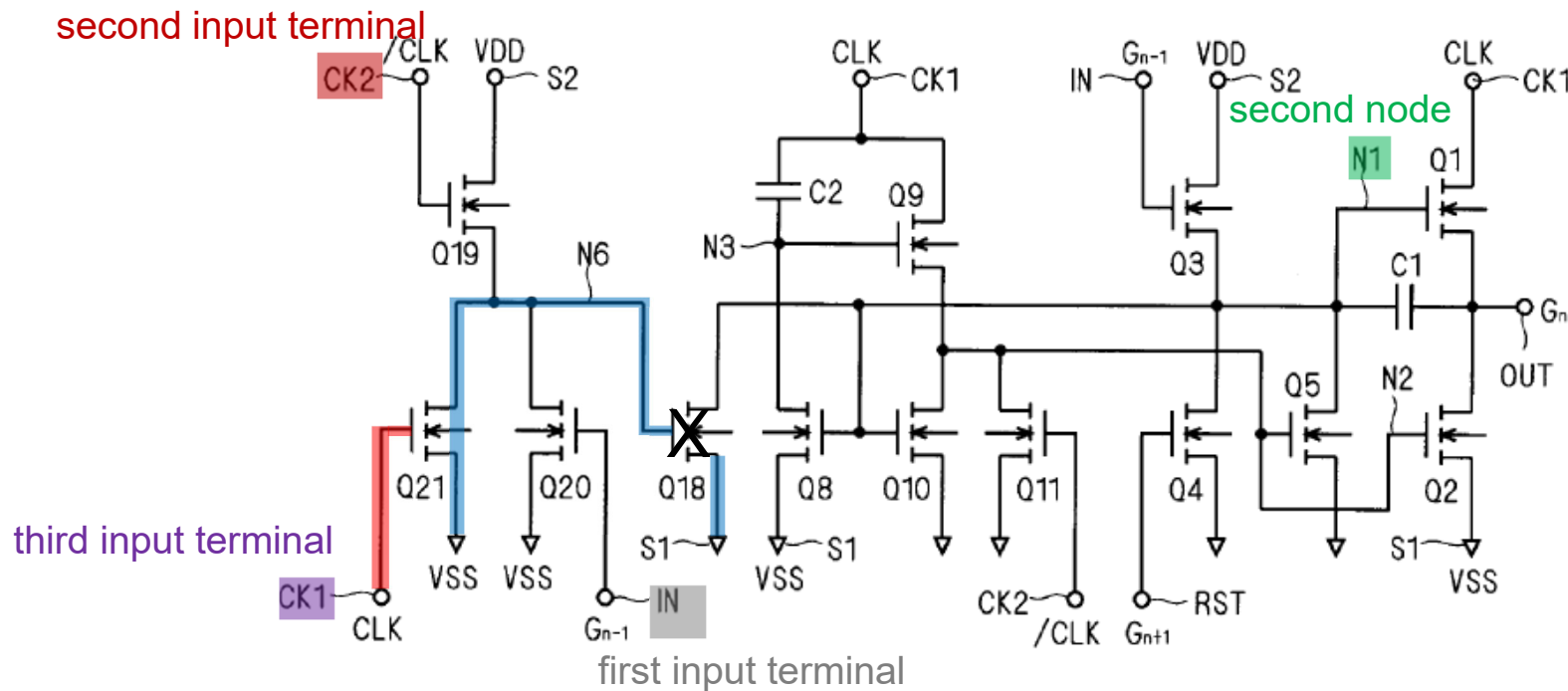
The Petition's theory: Q18–Q21 bringing N1 to a low level

undermine Petitioner's showing. Based on the present record, Petitioner shows sufficiently for institution that Tobita's transistors Q19–Q21 (i.e., part of the “first driver”) indirectly control the voltage of the node N1 by opening transistor Q18 to allow VSS to be provided to node N1 for purposes of bringing it to a low level. See, e.g., Ex. 1003 ¶¶ 617, 620; Ex. 1006 ¶¶ 172, 174–177. Petitioner also shows that transistors Q18–Q21 receive signals

DI at 51 (annotated)

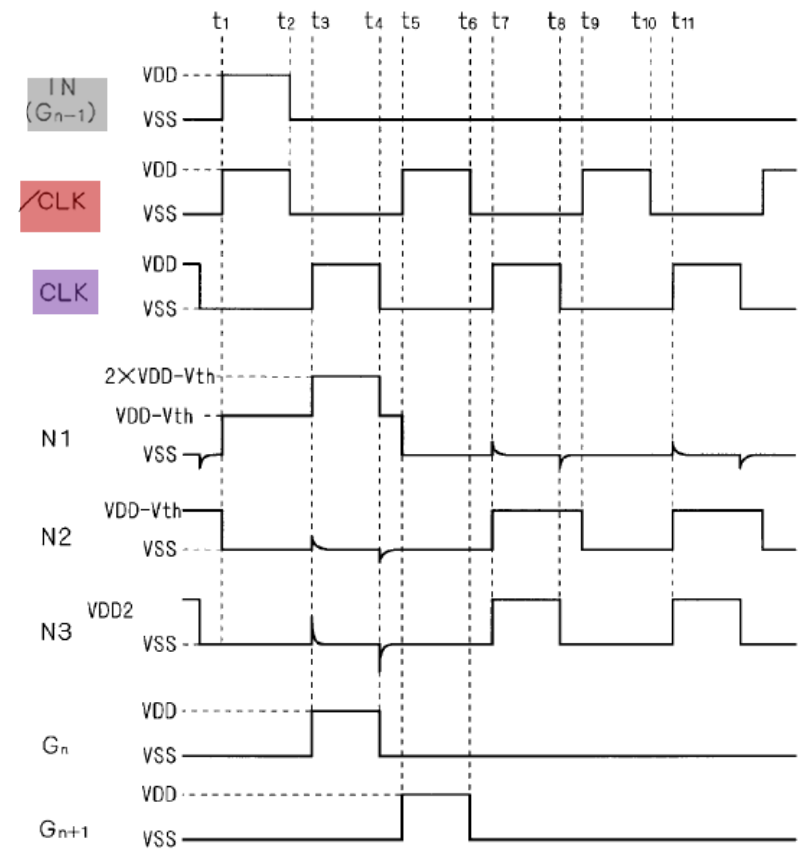
No control of second node in accordance with third input terminal under Petition's theory

FIG. 20



Tobita Fig. 20 (annotated)

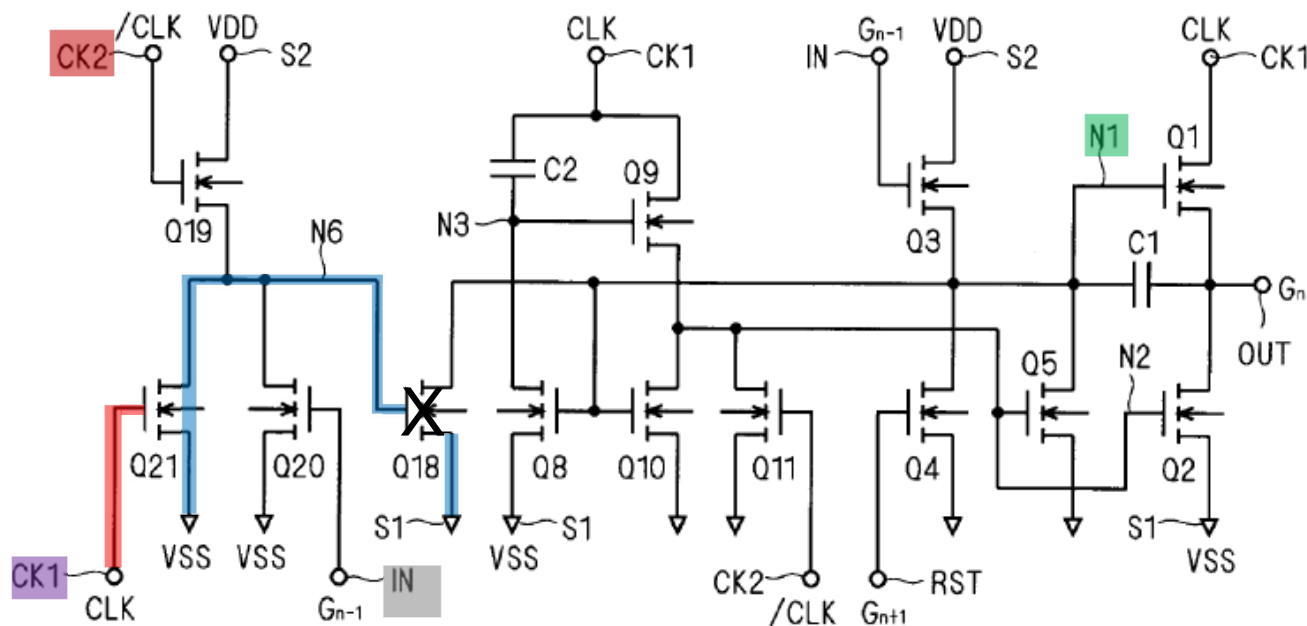
FIG. 9



Tobita Fig. 9 (annotated)

Dr. Foty admitted no control based on signal of third input terminal

F I G . 2 0



Tobita Fig. 20 (annotated)

Q And so the operation there of Q18 and the first driver will have no effect on the voltage of node N1, right?

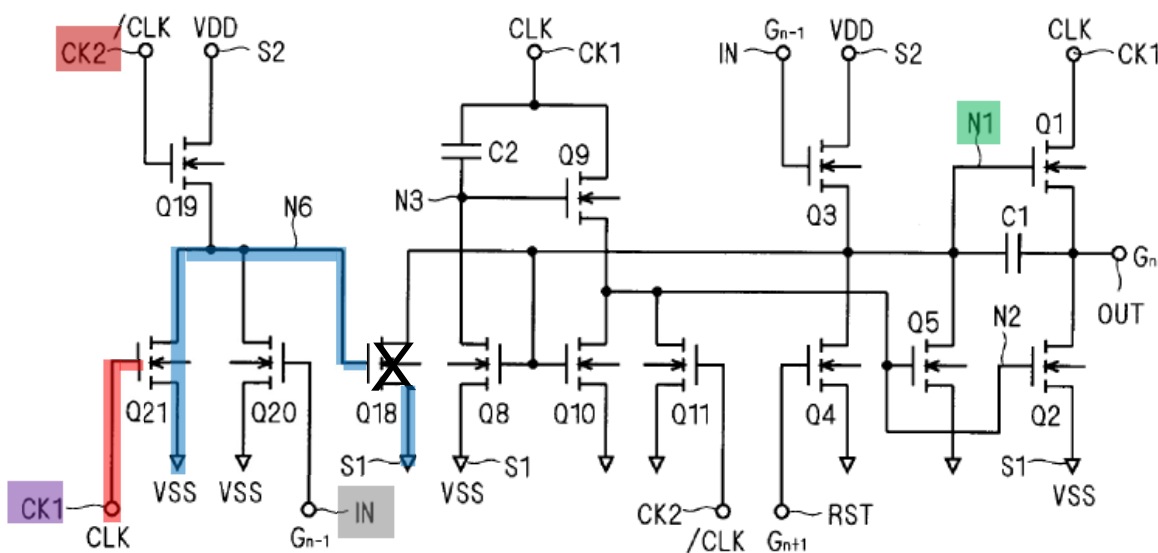
MR. HERMAN: Objection, form.

A Well, again, if you turn it off and within the context of not having leakage, if it is an ideal situation, then S1 will be isolated from N1 and will have no effect upon the voltage of node 1.

Foty Tr. 74:8–16

Petitioner's Reply theory: "other transistors" bringing N1 to a high level

F I G . 2 0

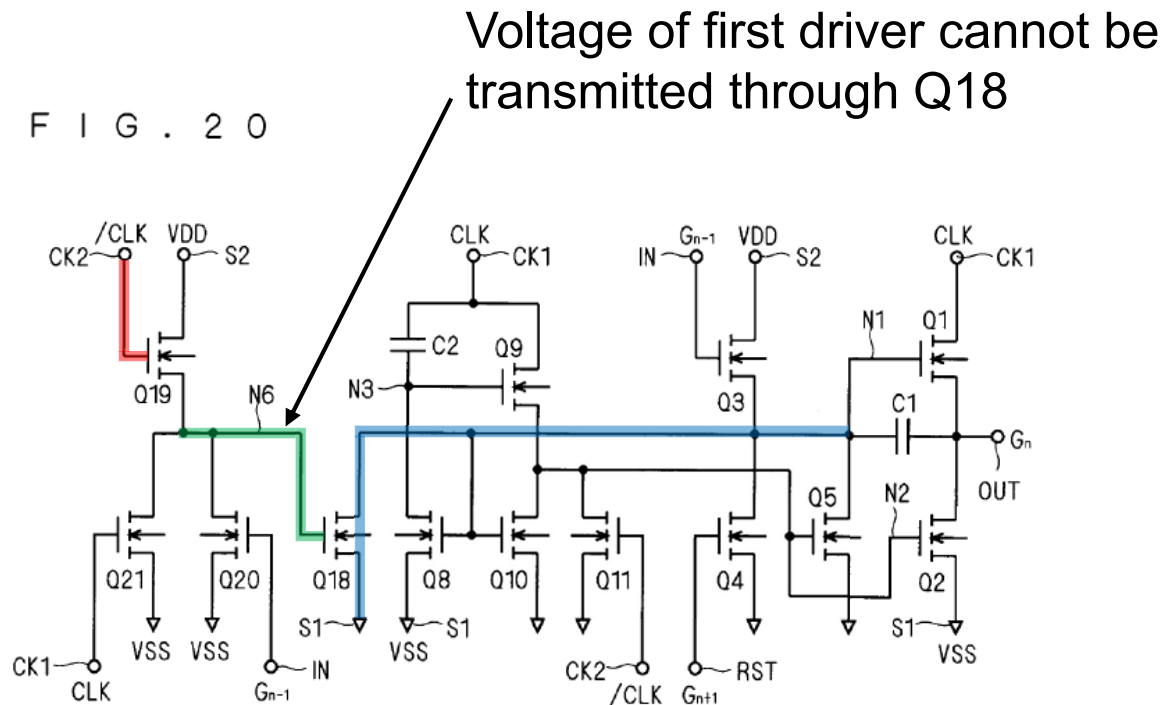


transistor Q18. Response at 45-47. This is nonsense. When transistor Q18 is off, no low-level VSS signal is supplied to node N1. This allows the other transistors of the "first driver"—Q3, Q4, and Q5—to provide a high-level signal. See Petition, 84; see also Tobita, Fig. 9.

Tobita Fig. 20 (annotated)

Reply at 24

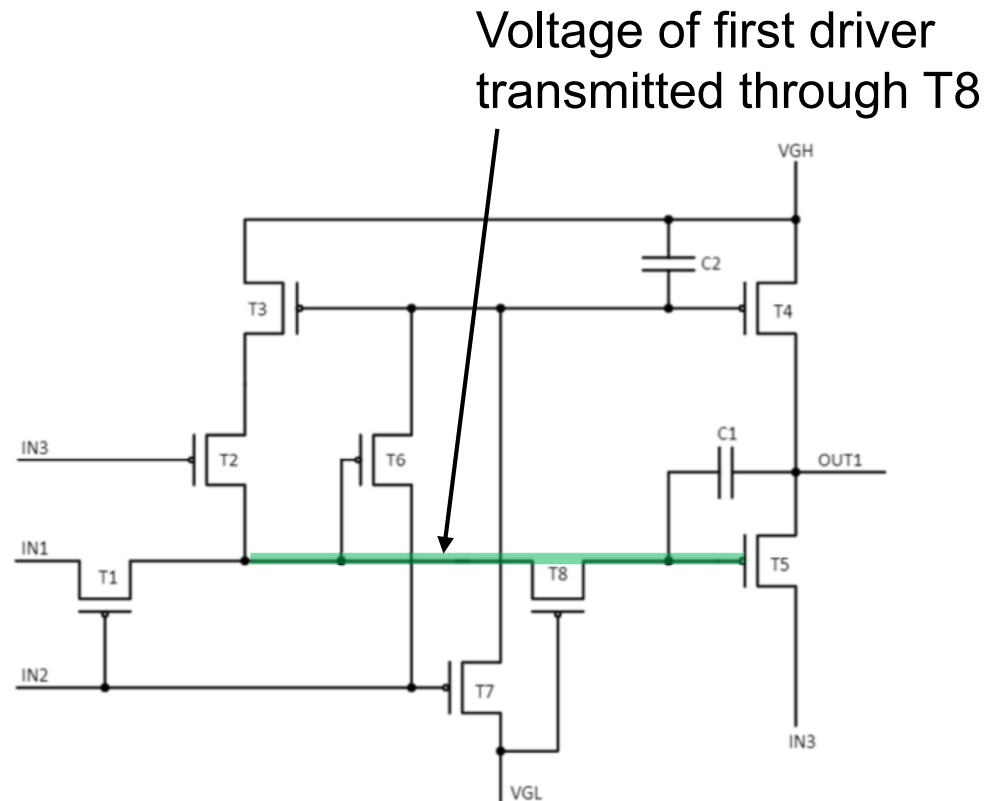
In Tobita, identified first driver does not “control the voltage of the second node”



Tobita Fig. 20 (annotated)

- Voltage of first driver is provided to N6 and cannot be transmitted to alleged second node (N1) and gate of transistor Q1

In commercial device, first driver does “control the voltage of the second node”



- Voltage of first driver is transmitted to second node (along green line) and gate of transistor T5

Circuit Diagram, Ex. 2059 (Wolfe) at 144 (annotated)

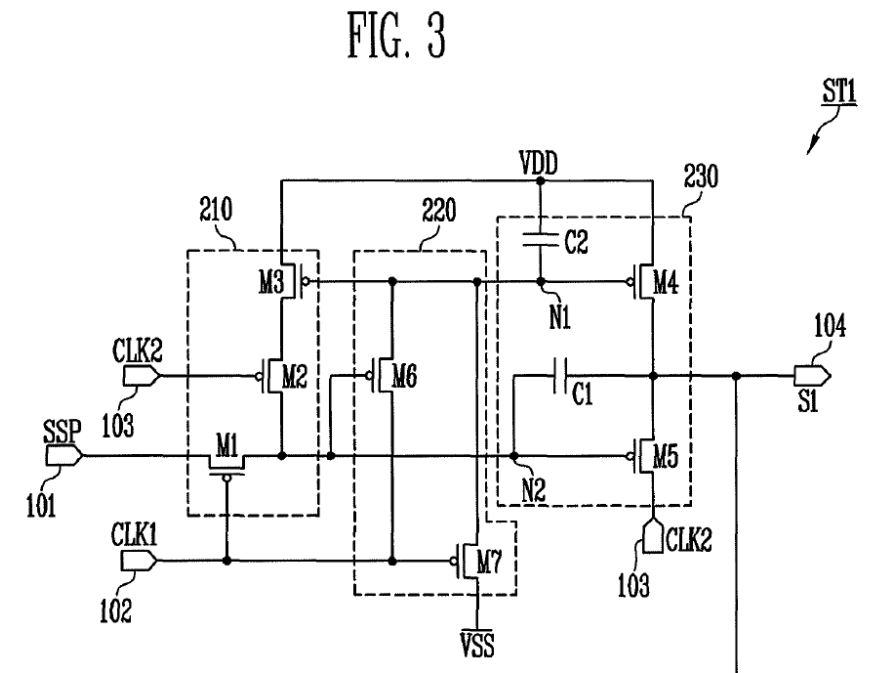
Prior claim construction dispute centered on whether first driver alone must control voltage of second node

Mianyang BOE's expert suggests that a driver cannot “control” the voltage of a node if something other than the driver's output is able to override that output.” Ex. B, Foty Decl., ¶ 108.

Ex. 1009 at 22

require highly persuasive evidentiary support.” *Vitronics*, 90 F.3d at 1583. In the exemplary embodiment of Figure 3, the first driver controls the voltage of the second node in conjunction with other circuit elements, including “first capacitor C1.” The patent explains that “[t]he first

Ex. 1009 at 23

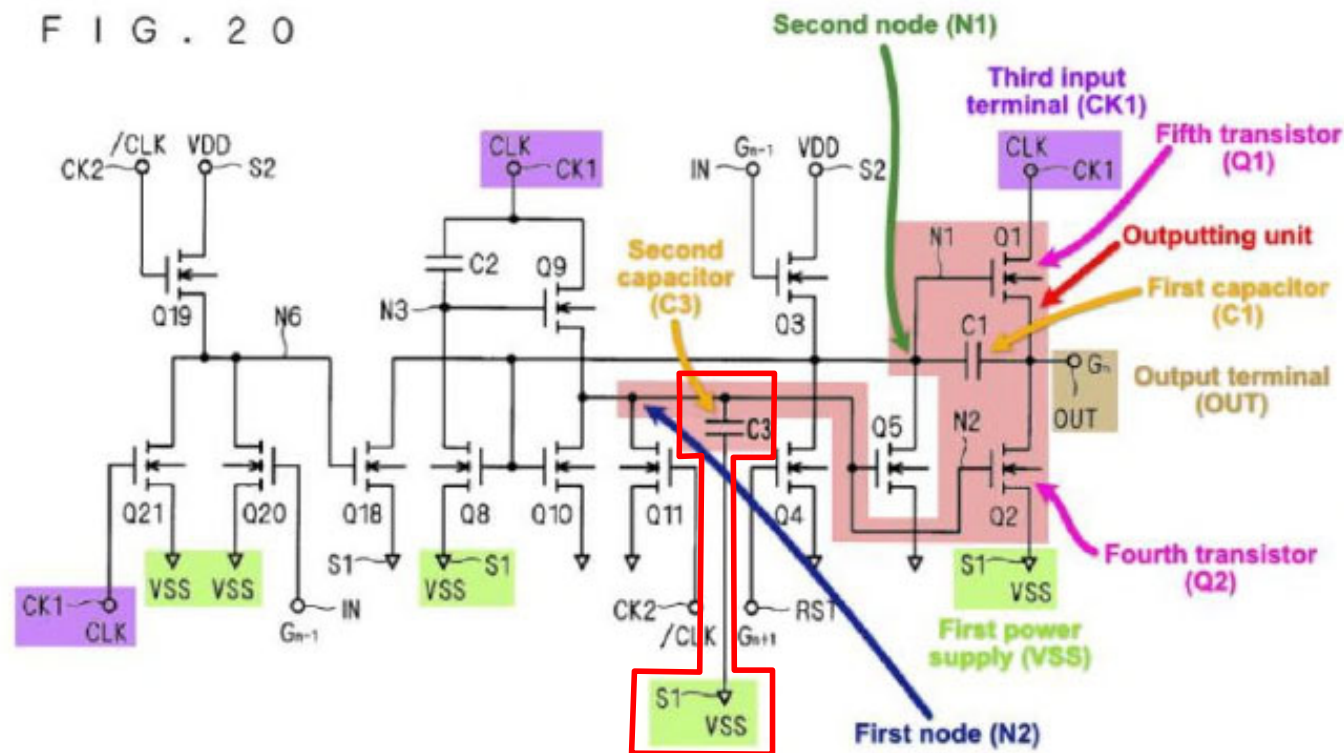


'593 Patent, Fig. 3

Tobita and Jeong

Claims 7 and 21

Claims 7 and 21 require an additional capacitor not found in Tobita



Petitioner's modification of Tobita (added elements in red box)
Pet. at 97

Claims 7 and 21 – Petitioner’s rationale for adding capacitor has no support beyond conclusory testimony

711. This can be problematic, since perturbations in the amount of charge (for example, due to electromagnetic interference (EMI) or interline crosstalk during digital switching events) may cause sizeable changes in the voltage on the node; these types of signal integrity issues are undesirable. Therefore, a POSITA would be motivated to seek methods of making the circuitry of Tobita more robust against a problem of this sort.

Ex. 1003 (Foty Dec.) ¶ 711

Petitioner’s rationale for adding a capacitor to Tobita’s circuit is based on hypothetical concerns. See Pet. 96–97 (stating the Tobita’s node N2 “*may not* adequately maintain a fixed voltage level” and “*could* experience . . . voltage variation” (emphasis added)). At this juncture, the record does not indicate that Tobita’s circuit suffers from these concerns. Further, the fact that an ordinarily skilled artisan *could* have added a capacitor to increase robustness does not mean that the artisan *would* have been motivated to make this modification, particularly given Tobita’s express concerns about increasing circuit area. See *Belden*, 805 F.3d at 1073; Ex.

DI at 58

A POSITA would not have made Petitioner's modification

123. In fact, Tobita explains that capacitors add significant circuit area, and Tobita is directed to reducing circuit area where possible. Tobita ¶ [0015]. Neither the generalized and unsupported concerns Dr. Foty identifies, nor Jeong's teachings relating to a capacitor in a different circuit would provide sufficient motivation for a POSITA to add an additional capacitor to Tobita's circuit. Moreover, Tobita includes a capacitor, C1, in the identified "outputting unit," yet does not include the additional capacitor Petitioner proposes to add. Tobita, Fig. 20. This further confirms that the generic considerations Petitioner advances (of which Tobita's author would have been similarly aware) would not motivate a POSITA to add a capacitor to Tobita as Petitioner suggests, let alone connect it in the specific way Petitioner does, which is necessary to arrive at the claims.

Ex. 2059 (Wolfe Dec.) ¶ 123

Objective Evidence of Non-Obviousness

Long-felt need: reduced drive circuit area and narrower bezel

A New Small Sized Integrated Scan & Emission Driver for Compact AMOLED Displays

Jin Huh and Gyu-Hyeong Cho
Dept. of EE, KAIST, Korea

for some products [1]-[2]. Most of the smartphones employ very high density displays over 300 *ppi* (pixel per inch). Therefore, it becomes more challenge to integrate peripheral drivers within a limited small area on a panel. Though they have been implemented by using low temperature poly-silicon TFT (LTPS TFT) process [3] or advanced solid phase crystallization TFT (A-SPC TFT) process [4], it is still difficult to implement the drivers in a limited area because process design rules of these processes are still in a range of several μm . In addition, a bezel of a panel is also getting narrowed for design of compact displays. Furthermore, AMOLED displays require more peripheral drivers such as a scan driver and an emission driver. Therefore, small sized drivers are required to reduce the area and to implement compact and high density displays.

Ex. 2050 at 1

'593 Patent stage circuit has been used ubiquitously

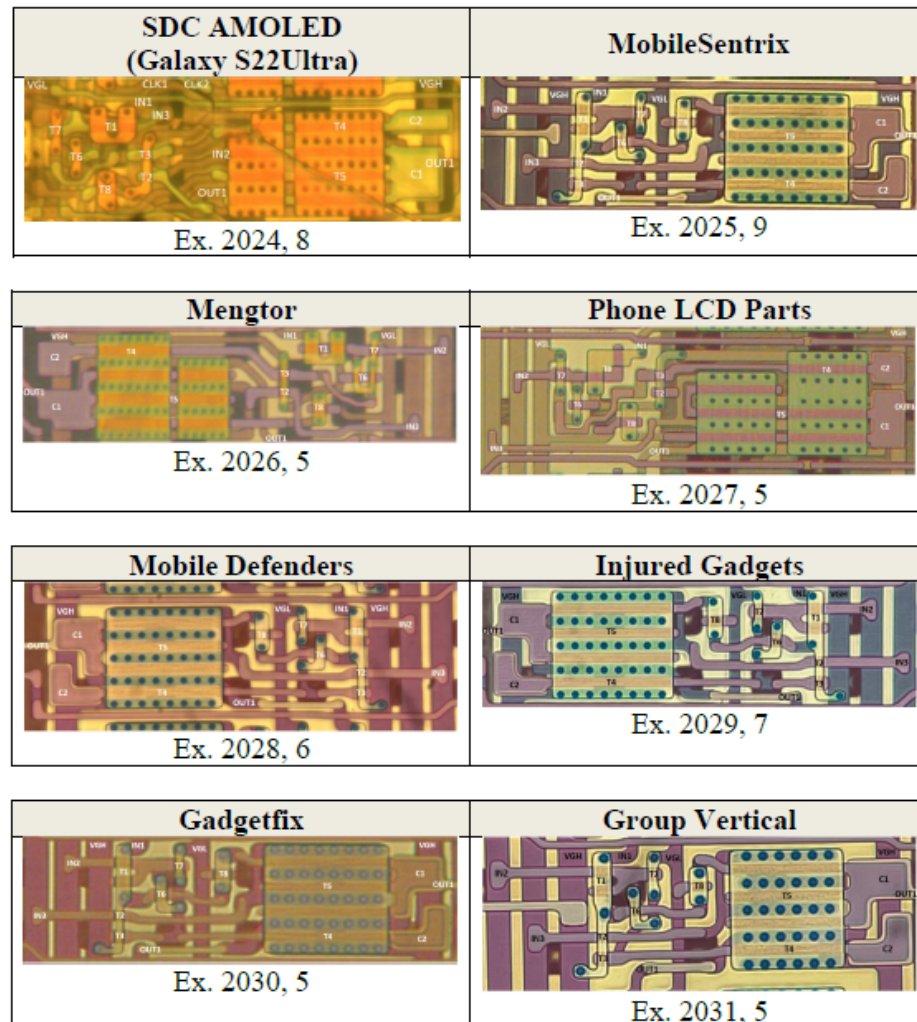
Galaxy S22 Ultra Circuit Analyzed by Dr. Wolfe

EXHIBIT 2057

CLAIM CHART: AMOLED DISPLAY IN SAMSUNG GALAXY S22 ULTRA

- Petitioner does not dispute:
 - that any claim element is not met by Samsung Display's AMOLED displays, beyond asserting an alleged inconsistency in discussion of Tobita
 - the benefits of narrow bezel
- No evidence that any of the alternative stage circuits proposed by others have been successfully implemented in commercialized AMOLED displays for mobile devices

Widespread copying of SDC's patented circuit is clear



- Petitioner does not rebut Dr. Wolfe's analysis showing that representative display from Mengtor practices the claims in the same manner as SDC

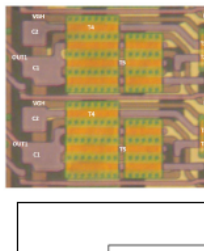
Ex. 2059, ¶¶ 139–144; see also PO Response at 62–79

- Nor does Petitioner rebut Dr. Wolfe's testimony that the copied products are so similar in physical layout that they can only be explained by deliberate copying

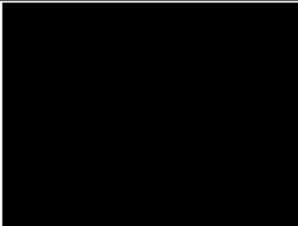
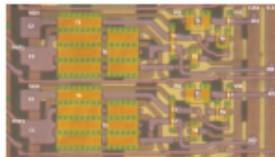
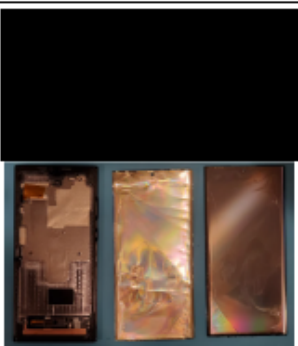
Ex. 2059, ¶¶ 139–144; see *Institut Pasteur v. Focarino*, 738 F.3d1337, 1347–48 (Fed. Cir. 2013)

Patent Owner has documented a nexus to the claimed invention

Excerpts of claim charts showing nexus for SDC's patented circuit and for copied circuit to the claimed invention

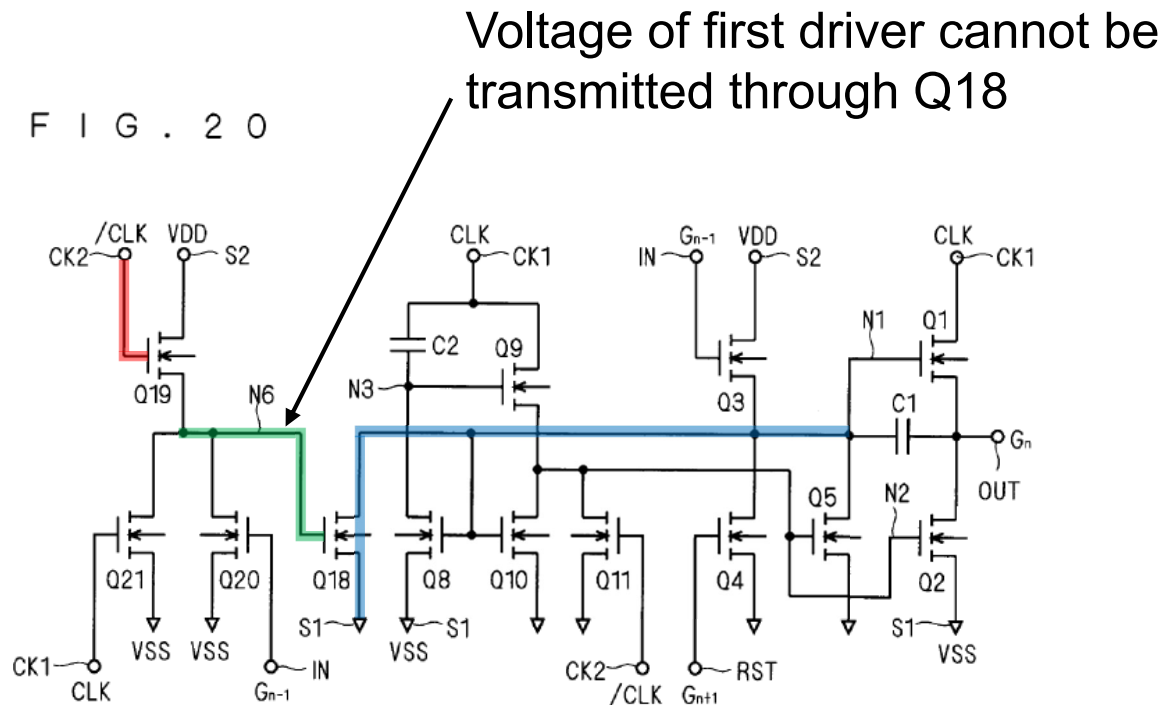
Claim	Galaxy S22ULTRA / Mengtor
1[pre]	The Galaxy S22Ultra and Mengtor products contain a stage circuit having a first input terminal (), a second input terminal (), a third input terminal () and an output terminal () as Dr. Wolfe explains. Ex. 2057, 2; Ex. 2046, 2-4.  
Ex. 2058, 55.	Ex. 2026, 5; Equivalent scan driver stage circuit for Mengtor AMOLED Display (“Mengtor Equivalent Circuit”)

POR at 62

Claim	Galaxy S22ULTRA / Mengtor	
	Ex. 2058, 39 (showing [REDACTED] having lower voltage than [REDACTED] 55.	
14	The Galaxy S22Ultra and Mengtor products contain the stage circuit as claimed in claim 1, wherein the transistor (T3) controls the voltage of the second node (see 1[a], above) according to the on/off operation thereof. Ex. 2057, 32; Ex. 2046, 33.  Ex. 2058, 55.  Ex. 2026, 5	
<u>15[pre]</u>	The Galaxy S22Ultra and Mengtor products contain an OLED display. Ex. 2057, 33-34; Ex. 2046, 34.  	

POR at 75

Petitioner's only argument against nexus is based on its flawed theory of "control"



Tobita Fig. 20 (annotated)

- Voltage of first driver is provided to N6 and cannot be transmitted to alleged second node (N1) and gate of transistor Q1