

Ex. 1030

BOE v. Samsung, IPR2024-00620

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MIANYANG BOE OPTOELECTRONICS TECHNOLOGY CO., LTD.,
WUHAN CHINA STAR OPTOELECTRONICS SEMICONDUCTOR
DISPLAY TECHNOLOGY CO., LTD.,
TIANMAMICROELECTRONICS CO. LTD.,
and VISIONOX TECHNOLOGY, INC.,
Petitioner,

v.

SAMSUNG DISPLAY COMPANY, LTD.,
Patent Owner.

IPR2024-00620
Patent 9,330,593 B2

Before THOMAS L. GIANNETTI, TERRENCE W. MCMILLIN, and
JOHN A. HUDALLA, *Administrative Patent Judges*.

HUDALLA, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Some Challenged Claims Unpatentable
35 U.S.C. § 318(a)

Mianyang BOE Optoelectronics Technology Co., Ltd., Wuhan China Star Optoelectronics Semiconductor Display Technology Co., Ltd., Tianma Microelectronics Co. Ltd., and Visionox Technology, Inc. (collectively, “Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting an *inter partes* review of claims 1–8, 14–22, and 25 (“the challenged claims”) of U.S. Patent No. 9,330,593 B2 (Ex. 1001, “the ’593 patent”). Samsung Display Co., Ltd. (“Patent Owner”) filed a Preliminary Response. Paper 9 (“Prelim. Resp.”). Petitioner also filed a Preliminary Reply (Paper 10) and Patent Owner filed a Preliminary Sur-reply (Paper 11) directed to Patent Owner’s arguments regarding discretionary denial from the Preliminary Response. Taking into account the arguments presented by Patent Owner in the preliminary record, we determined that the information presented in the Petition established that there was a reasonable likelihood that Petitioner would prevail with respect to at least one of the challenged claims. Pursuant to 35 U.S.C. § 314, we instituted this proceeding on September 12, 2024, as to all challenged claims and all grounds of unpatentability presented in the Petition. Paper 12 (“Dec. on Inst.”).

During the course of trial, Patent Owner filed a Patent Owner Response (Paper 22, “PO Resp.”), and Petitioner filed a Reply to the Patent Owner Response (Paper 27, “Pet. Reply”). Patent Owner also filed a Sur-reply (Paper 30, “PO Sur-reply”). An oral hearing with was held on June 13, 2025, and a transcript of the hearing is included in the record. Paper 37 (“Tr.”).

Petitioner filed declarations of Daniel Foty, Ph.D., with its Petition (Ex. 1003) and Reply (Ex. 1025). Patent Owner filed declarations of Aris K. Silzars, Ph.D. (Ex. 2042), Adam Fontecchio, Ph.D. (Ex. 2043),

Kwangsae Lee (Ex. 2044), and Andrew Wolfe, Ph.D. (Ex. 2059) with its Response. The parties also filed transcripts of the depositions of Dr. Foty (Exs. 2060,¹ 2062, 2063) and Dr. Wolfe (Ex. 1026).

We have jurisdiction under 35 U.S.C. § 6. This decision is a Final Written Decision under 35 U.S.C. § 318(a) as to the patentability of claims 1–8, 14–22, and 25 of the ’593 patent. For the reasons discussed below, Petitioner has demonstrated by a preponderance of the evidence that claims 1, 2, and 15–18 of the ’593 patent are unpatentable. Petitioner has not demonstrated by a preponderance of the evidence that claims 3–8, 14, 19–22, and 25 of the ’593 patent are unpatentable.

I. BACKGROUND

A. *Real Parties-in-Interest*

Petitioner identifies Mianyang BOE Optoelectronics Technology Co., Ltd., Wuhan China Star Optoelectronics Semiconductor Display Technology Co., Ltd., Tianma Microelectronics Co. Ltd., Visionox Technology, Inc., and their subsidiaries as the real parties-in-interest. Pet. 2. Patent Owner identifies Samsung Display Co., Ltd. as the real party-in-interest. Paper 7, 2 (Patent Owner’s Mandatory Notices).

¹ Exhibit 2060 is the uncertified rough transcript of Dr. Foty’s deposition on December 5, 2024. The finalized transcript of the same deposition is located at Exhibit 2063. We refer to the finalized transcript herein and have translated all citations from the rough transcript to the finalized transcript.

B. Related Matters

As required by 37 C.F.R. § 42.8(b)(2), the parties identify the following related matters:

In the Matter of Certain Active Matrix Organic Light-Emitting Diode Display Panels and Modules for Mobile Devices, and Components Thereof, International Trade Commission Investigation No. 337-TA-1351 (filed Dec. 28, 2022) (“the ITC Investigation”);

Samsung Display Co., Ltd. v. BOE Technology Co., Ltd., No. 2-23-cv-00309 (E.D. Tex. filed June 26, 2023); and

IPR2023-01221 (terminated Nov. 27, 2023).

Pet. 2; Paper 7, 2. Patent Owner also notes that Petitioner has challenged other patents at issue in the ITC Investigation in IPR2023-00941, IPR2023-00987, IPR2023-00988, and IPR2023-01075. Prelim. Resp. 15 & n.4.

C. The '593 Patent

The '593 patent is directed to “a stage circuit and an organic light emitting display using the same.” Ex. 1001, 1:17–18. The '593 patent states that “conventional stage circuits include[] a plurality of transistors, e.g., at least ten transistors, to supply the scan signals and/or require use of [an] initializing signal in addition to . . . first and second clock signals.” *Id.* at 9:14–18. In contrast, the '593 patent discloses embodiments with “stages having a reduced number of transistors and that output scan signals only using first and second clock signals.” *Id.* at 9:12–14. The '593 patent states that these embodiments advantageously improve stability and reduce complexity. *Id.* at 9:24–26.

Figure 3 of the '593 patent is reproduced below.

FIG. 3

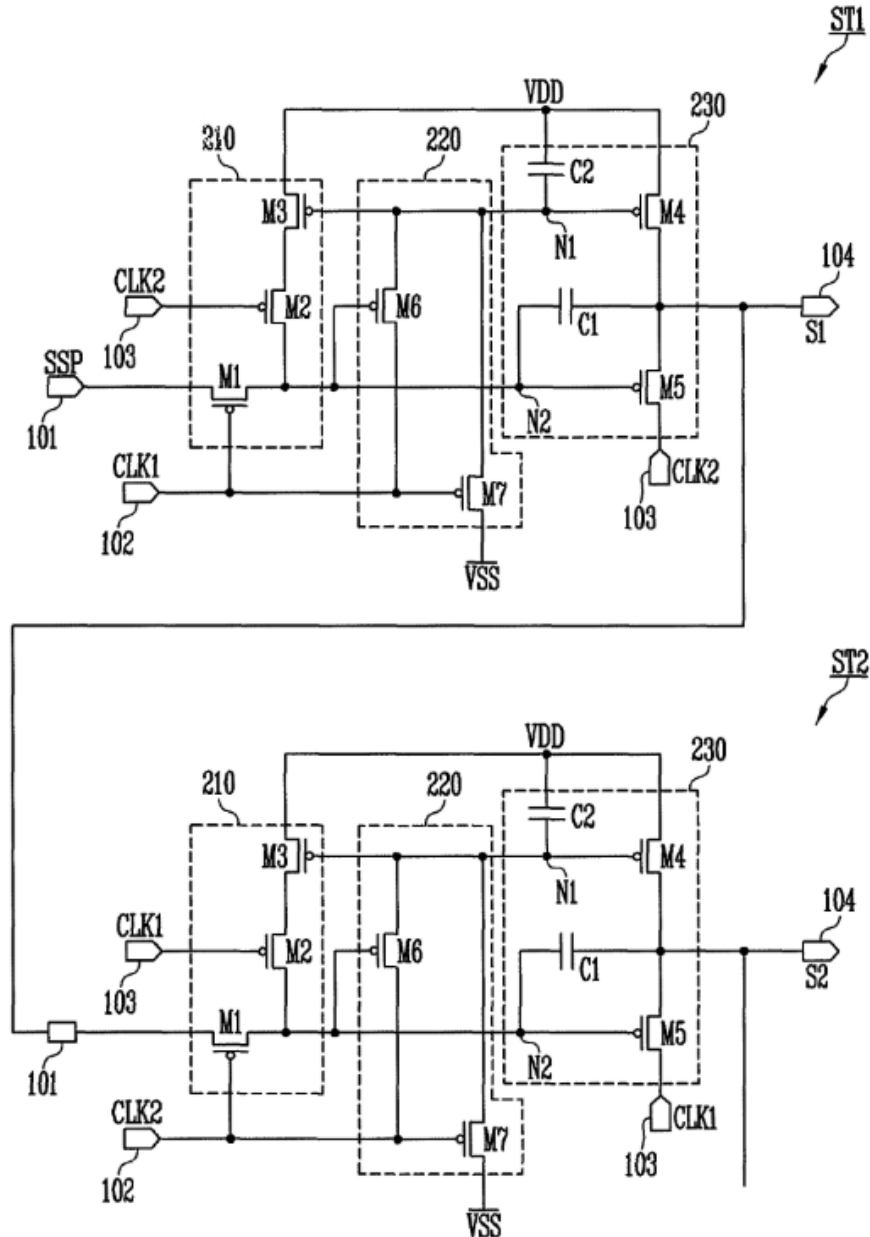


Figure 3 is a circuit diagram illustrating first stage ST1 and second stage ST2. Ex. 1001, 5:29–31. First stage ST1 includes first driver 210, second driver 220, and outputting unit 230. *Id.* at 5:34–36. First driver 210 includes first transistor M1, second transistor M2, and third transistor M3.

Id. at 5:65–67. Second driver 220 includes sixth transistor M6 and seventh transistor M7. *Id.* at 6:24–26. Outputting unit 230 includes fourth transistor M4, fifth transistor M5, first capacitor C1, and second capacitor C2. *Id.* at 6:24–26.

First driver 210 controls the voltage of second node N2 in accordance with signals supplied to first input terminal 101 and third input terminal 103. Ex. 1001, 5:63–65. Second driver 220 controls the voltage of first node N1 in accordance with signals supplied to second input terminal 102 and second node N2. *Id.* at 6:22–24. Outputting unit 230 controls a voltage supplied to output terminal 104 in accordance with voltages applied to first node N1 and second node N2. *Id.* at 5:37–39.

First input terminal 101 of first stage ST1 receives start signal SSP, and first input terminal 101 of second stage ST2 receives the output signal (i.e., the scan signal) of first stage ST1. Ex. 1001, 5:1–7. “The second input terminal 102 of an *i*th (*i* is odd or even) stage ST_{*i*} receives the first clock signal CLK1 and the third input terminal 103 of the *i*th stage ST_{*i*} receives the second clock signal CLK2.” *Id.* at 5:8–11. “The second input terminal 102 of an (*i*+1)th stage ST_{*i*} receives the second clock signal CLK2 and the third input terminal 103 of the (*i*+1)th stage ST_{*i*} receives the first clock signal CLK1.” *Id.* at 5:11–15. First clock signal CLK1 and second clock signal CLK2 have the same period and have phases that do not overlap. *Id.* at 5:16–18.

The application that led to the ’593 patent was filed on February 20, 2013, and claims priority to a Korean patent application that was filed on September 20, 2012. Ex. 1001, codes (22), (30); *see also* Pet. 4 (noting same). Petitioner assumes a priority date of September 20, 2012, for

purposes of this proceeding (Pet. 4), so we apply that date for determining whether the asserted references qualify as prior art.

D. Illustrative Claim

Of the challenged claims, claims 1 and 15 are independent. Claims 2–8 and 14 depend directly or indirectly from claim 1, and claims 16–22 and 25 depend directly or indirectly from claim 15. Claim 1 is illustrative of the challenged claims and recites:

1. [1-PRE] A stage circuit having a first input terminal, a second input terminal, a third input terminal, and an output terminal, the stage circuit comprising:

[1-A] an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node;

[1-B] a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal; and

[1-C] a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node,

[1-D] wherein the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver.

Ex. 1001, 9:43–60 (Petitioner’s identifiers added in brackets); *see also* Pet. ix–xiv (claim listing with Petitioner’s identifiers).

E. Prior Art

Petitioner relies on the following prior art:

U.S. Patent Application Publication No. 2011/0057190 A1, filed Sept. 3, 2010, published Mar. 10, 2011 (Ex. 1004, “Kimura”);

U.S. Patent Application Publication No. 2007/0063950 A1, filed Aug. 18, 2006, published Mar. 22, 2007 (Ex. 1005, “Shin”);

U.S. Patent Application Publication No. 2008/0101529 A1, filed July 31, 2007, published May 1, 2008 (Ex. 1006, “Tobita”);

U.S. Patent Application Publication No. 2008/0062097 A1, filed July 12, 2007, published Mar. 13, 2008 (Ex. 1007, “Jeong”); and

U.S. Patent Application Publication No. 2005/0185752 A1, filed Dec. 6, 2004, published Aug. 25, 2005 (Ex. 1014, “Sasaki”).

F. The Instituted Grounds

We instituted *inter partes* review of claims 1–8, 14–22, and 25 of the ’593 patent on the following grounds (Dec. on Inst. 63), which are all the grounds presented in the Petition (Pet. 4–5):

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–8, 14–22, 25	103(a) ²	Kimura
1–6, 8, 14–20, 22, 25	103(a)	Shin, Sasaki

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. §§ 102 and 103. Because the application for the ’593 patent was filed before March 16, 2013 (the effective date of the relevant amendments), we apply the pre-AIA versions of §§ 102 and 103.

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
7, 21	103(a)	Shin, Sasaki, Jeong
1, 2, 15–18	103(a)	Tobita
7, 21	103(a)	Tobita, Jeong

II. ANALYSIS

A. *Legal Standards*

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007).

The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

We also recognize that prior art references must be “considered together with the knowledge of one of ordinary skill in the pertinent art.” *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (citing *In re Samour*, 571 F.2d 559, 562 (CCPA 1978)).

B. *Level of Ordinary Skill in the Art*

Citing testimony from Dr. Foty, Petitioner contends a person of ordinary skill in the art “would have had a Bachelor’s degree in electrical

engineering or a similar discipline, along with 2-3 years of circuit design experience.” Pet. 5 (citing Ex. 1003 ¶¶ 27–29).

Patent Owner cites testimony from Dr. Wolfe and contends that a person of ordinary skill in the art “would have had a relevant degree in Electrical Engineering, Computer Engineering, Materials Science, Physics, or the like, and 2-3 years of experience in active-matrix display design and electroluminescence.” PO Resp. 3–4 (citing Ex. 2059 ¶ 39). Patent Owner additionally notes that the Administrative Law Judge (ALJ) in the ITC Investigation adopted a similar definition, though he did not quantify the amount of experience required. *Id.* at 4 (citing Ex. 2018, 12).

Patent Owner criticizes Petitioner’s proposed definition because it “entails only general ‘circuit design’ experience with no experience in active-matrix display design and electroluminescence, the subject matter of the ’593 Patent.” PO Resp. 4–5; *see also* Ex. 2059 ¶¶ 41–42 (Dr. Wolfe’s testimony regarding the same). In particular, Patent Owner argues that “[i]mportant aspects and considerations of the pixel circuit design are unique to the context of active-matrix display design and to electroluminescent displays.” PO Resp. 5 (citing Ex. 2059 ¶ 41). Patent Owner notes that the “Field” of the ’593 patent states expressly that its embodiments relate to “a stage circuit and an organic light emitting display using the same.” *Id.* at 6 (quoting Ex. 1001, 1:17–18); *see also id.* at 5–6 (citing other portions of the ’593 patent that are indicative of organic light emitting diode (OLED) displays). Patent Owner also notes that independent claim 15 recites “an organic light emitting display,” as well as other signal lines connected to the pixel circuit.” *Id.* at 5 (quoting Ex. 1001, 11:9) (citing Ex. 2059 ¶ 41).

The main disagreement between the parties is about the type of experience that an ordinarily skilled artisan would have possessed. The record evidence regarding this issue is thin, and it amounts to competing testimony from the parties' declarants. *Compare* Ex. 1003 ¶ 29, *with* Ex. 2059 ¶¶ 41–42. Although Patent Owner argues that experience in active-matrix displays and electroluminescence would have been necessary, the '593 patent includes no disclosures on active-matrix displays. The closest disclosures in the '593 patent relate to organic light-emitting displays (*see, e.g.*, Ex. 1001, 1:16–18), which both declarants acknowledge. Having considered the full trial record, we determine that no specific experience in active-matrix display design and electroluminescence would have been required. In reaching this conclusion, we note that a vast majority of the disclosures in the '593 patent pertain to circuits and circuit elements, whereas OLED displays are the merely the application for using the described circuits. *See, e.g.*, Ex. 1001, 9:43–66 (claim 1 reciting only a “stage circuit”). Under these circumstances, we do not agree with Patent Owner that specialized experience in active-matrix displays would have been required for an ordinarily skilled artisan to understand the relatively basic circuit technology at issue. *See Daiichi Sankyo Co. v. Apotex, Inc.*, 501 F.3d 1254, 1256 (Fed. Cir. 2007) (noting that “sophistication of the technology” is a factor for determining the level of ordinary skill in the art). We also find that a basic understanding of OLED technology is all that would have been necessary to implement the disclosed stage circuits.

For these reasons, we adopt Petitioner's definition of a person of ordinary skill in the art.

C. Claim Interpretation

In an *inter partes* review, we construe each claim using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.

37 C.F.R. § 42.100(b). Accordingly, our claim construction standard is the same as that of a district court. *See id.* Under the standard applied by district courts, claim terms are generally given their plain and ordinary meaning, as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). “There are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution.” *Thorner v. Sony Comput. Entm’t Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012).

Petitioner contends that no claim construction is necessary in this case. Pet. 10. Petitioner further notes that, in the ITC Investigation, Patent Owner argued that all terms should be given their plain and ordinary meaning. *Id.*

Patent Owner notes that the ALJ issued a claim construction order in the ITC Investigation construing certain claim terms of the ’593 patent. PO Resp. 7 (citing Ex. 2018, 15–37 (ITC order)). Notwithstanding, Patent

Owner states that it “does not believe that any specialized constructions are necessary.” *Id.*

1. *“a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal”*

In our Decision on Institution, we found it necessary to construe a limitation in claims 1 and 15 that recites “a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal.” *See* Dec. on Inst. 11–13; Ex. 1001, 9:52–54, 11:28–30. In the ITC Investigation, the ITC ALJ found that “[c]ontrol[ling] the voltage of the second node’ does not require that the voltage of the second node be determined by the first driver alone.” Ex. 2018, 31–32 (alterations in original). We adopted the ALJ’s reasoning in our Decision on Institution and applied the same construction as the ALJ, i.e., that controlling the voltage of the second node does not require the voltage of the second node to be determined by the first driver alone. *See* Dec. on Inst. 12–13. We also noted the contrast between this limitation and another limitation that expressly recites direct control and further noted the Specification’s express mention that it uses the word “directly” where the same is intended. *Id.* (citing Ex. 1001, 4:19–26; 9:58). After institution, Patent Owner stated that it agrees with this construction, though it disputes that Petitioner’s obviousness theory comports with this construction.³ *See* PO Resp. 40–42. Petitioner did not further address our construction.

³ We discuss Patent Owner’s arguments against Petitioner’s analysis for these limitations below.

Accordingly, we maintain the same construction and reasoning from our Decision on Institution. To the extent necessary, we also state expressly that the first driver need not directly control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal. *See* Ex. 1001, 4:19–26; 9:58. As noted in our Decision on Institution (Dec. on Inst. 13), this comports with the reasoning in Patent Owner’s ITC claim construction brief. *See* Ex. 1009, 22–23 (Patent Owner arguing that no direct control limitation should be imputed).

2. *Whether the Preamble of Claim 15 is Limiting*

The preamble of claim 15 recites “[a]n organic light emitting display.” Ex. 1001, 11:9. Petitioner argues that the preamble is “a non-limiting label of intended use.” Pet. 88–89 (citing *Arctic Cat Inc. v. GEP Power Prod., Inc.*, 919 F.3d 1320, 1329–30 (Fed. Cir. 2019)). Patent Owner does not address whether the preamble of claim 15 is limiting.

We are persuaded by Petitioner’s argument that the preamble is not limiting. In particular, “a preamble generally is not limiting when the claim body describes a structurally complete invention such that deletion of the preamble phrase does not affect the structure or steps of the claimed invention.” *Catalina Mktg. Int’l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 809 (Fed. Cir. 2002). Similarly, the preamble is not limiting where it “only . . . state[s] a purpose or intended use for the invention.” *Rowe v. Dror*, 112 F.3d 473, 478 (Fed. Cir. 1997). We note that the body of claim 15 does not further reference the preamble’s “organic light emitting display,” and the body of the claim defines a complete invention comprising

display components regardless of the preamble’s indication of the intended use for that invention. For these reasons, we treat the preamble as non-limiting.

3. *Other Limitations*

We determine that no other aspects of the challenged claims require explicit construction. *See, e.g., Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. *Obviousness Ground Based on Kimura*

Petitioner contends that the subject matter of claims 1–8, 14–22, and 25 would have been obvious over Kimura. Pet. 14–44; Pet. Reply 3–18. Patent Owner disputes Petitioner’s contentions. PO Resp. 7–31; PO Sur-reply 2–16.

1. *Kimura*

Kimura is a U.S. Patent Application Publication directed to “a semiconductor device and a driving method thereof.” Ex. 1004 ¶ 2. Figure 1A of Kimura is reproduced below.

FIG. 1A

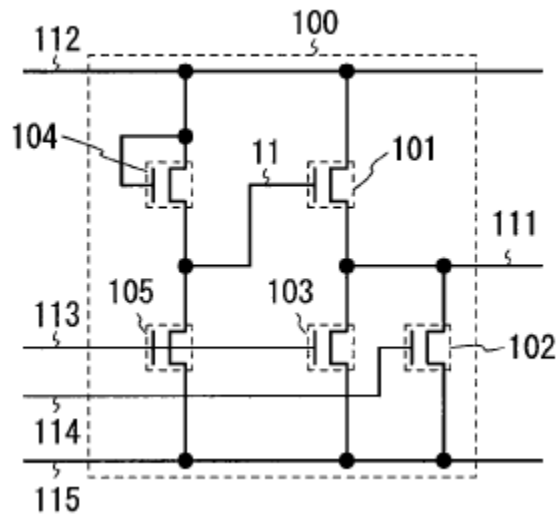


Figure 1A is a circuit diagram of a semiconductor device according to Kimura's "Embodiment 1." *Id.* ¶ 46. Circuit 100 includes transistors 101–105. *Id.* ¶¶ 95, 100. The first terminal of transistor 101 is connected to wiring 112, and the second terminal of transistor 101 is connected to wiring 111. *Id.* ¶ 97. The first terminal of transistor 102 is connected to wiring 115, the second terminal of transistor 102 is connected to wiring 111, and the gate of transistor 102 is connected to wiring 114. *Id.* ¶ 99. The first terminal of transistor 103 is connected to wiring 115, the second terminal of transistor 103 is connected to wiring 111, and the gate of transistor 103 is connected to wiring 113. *Id.* The first terminal of transistor 104 is connected to wiring 112, the second terminal of transistor 104 is connected to the gate of transistor 101, and the gate of transistor 104 is connected to wiring 112. *Id.* ¶ 97. The first terminal of transistor 105 is connected to wiring 115, the second terminal of transistor 105 is connected to the gate of transistor 101, and the gate of transistor 105 is connected to wiring 113. *Id.* ¶ 99. Node 11 designates the location where the gate of transistor 101 is

connected to the second terminal of transistor 104 and the second terminal of transistor 105. *Id.* ¶ 101.

Figure 27C of Kimura is reproduced below.

FIG. 27C

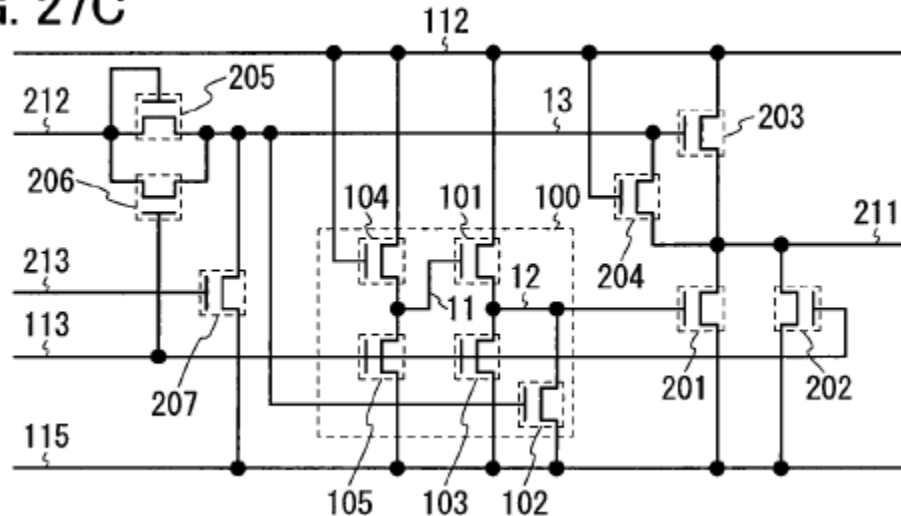


Figure 27C is a circuit diagram of a semiconductor device according to Kimura's "Embodiment 2," which adds transistors 201–207 to the circuit of "Embodiment 1." Ex. 1004 ¶¶ 72, 218–222, 245–246, 248–250, 261–262, 265–268, 270–272, 276–280. The first terminal of transistor 201 is connected to wiring 115, the second terminal of transistor 201 is connected to wiring 211, and the gate of the transistor 201, which is designated node 12, is connected to wiring 111. *Id.* ¶¶ 220–221. The first terminal of transistor 202 is connected to wiring 115, the second terminal of transistor 202 is connected to wiring 211, and the gate of transistor 202 is connected to wiring 113. *Id.* ¶ 245. The first terminal of transistor 203 is connected to wiring 112, the second terminal of transistor 203 is connected to wiring 211, and the gate of transistor 203, which is designated node 13, is connected to the gate of transistor 102. *Id.* ¶ 249. The first terminal of transistor 204 is connected to wiring 115, the second terminal of

transistor 204 is connected to node 13, and the gate of transistor 204 is connected to node 12. *Id.* ¶ 261. The first terminal of transistor 205 is connected to wiring 212, the second terminal of transistor 205 is connected to node 13, and the gate of transistor 205 is connected to wiring 212. *Id.* ¶ 265. The first terminal of transistor 206 is connected to wiring 212, the second terminal of transistor 206 is connected to node 13, and the gate of transistor 206 is connected to wiring 113. *Id.* ¶ 271. The first terminal of transistor 207 is connected to wiring 115, the second terminal of transistor 207 is connected to node 13, and the gate of the transistor 207 is connected to wiring 213. *Id.* ¶ 277.

Figure 34 of Kimura is reproduced below.

FIG. 34

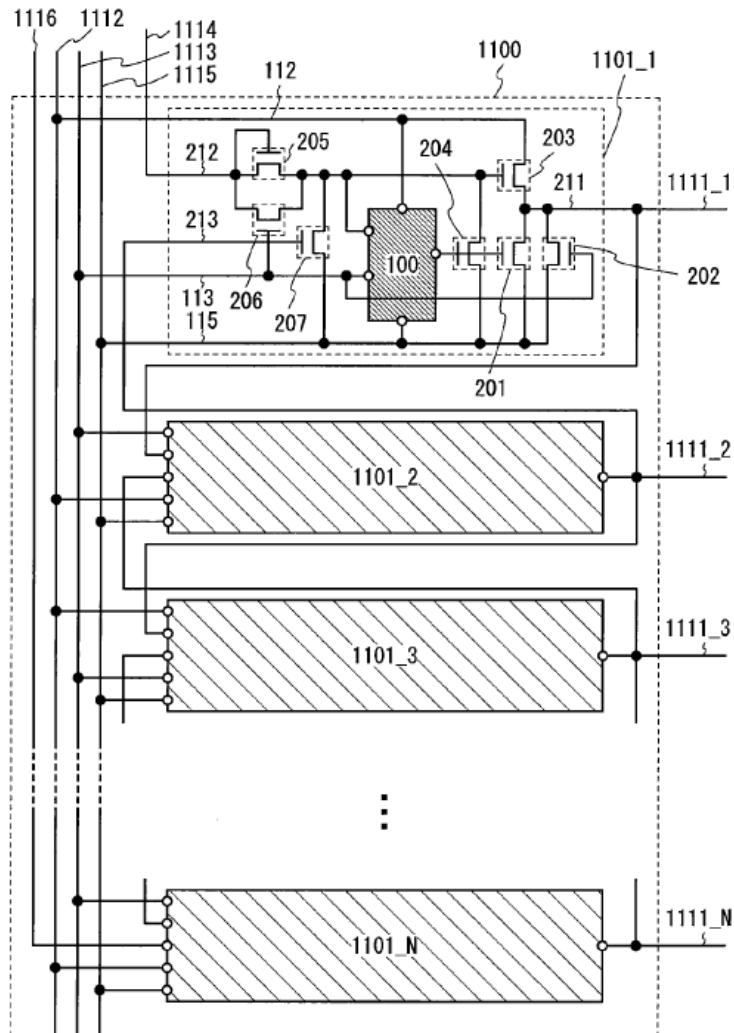


Figure 34 illustrates a shift register circuit according to Kimura's "Embodiment 3," which relates to "a display device, a pixel included in the display device and a shift register circuit included in the display device" that utilizes the disclosed semiconductor device. Ex. 1004 ¶¶ 79, 320. Specifically, shift register circuit 1100 includes a plurality of flip-flop circuits 1101_1 to 1101_N (where N is a natural number). *Id.* ¶¶ 333–334. The semiconductor devices described in Kimura's Embodiment 1 or

Embodiment 2 can be used for each of the flip-flop circuits 1101_1 to 1101_N. *Id.* ¶ 334.

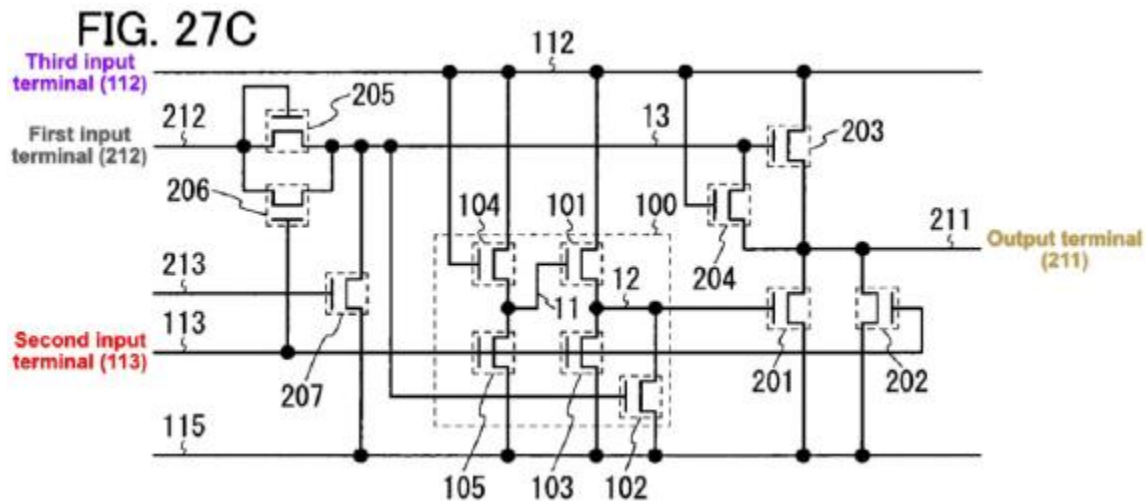
2. *Claim 1*

a. Petitioner's Contentions from the Petition

Petitioner's analysis for this ground is based on the circuit depicted in Figure 27C of Kimura. Petitioner acknowledges that “the portion of Kimura discussing Figure 27C does not itself mention all the depicted transistors, inputs, and outputs.” Pet. 15. Nevertheless, Petitioner asserts that “the device of Figure 27C builds on and shares components with the devices of its other figures,” and Petitioner contends that an ordinarily skilled artisan “would have understood that any shared components in Figure 27C not specifically discussed in the portion of Kimura addressing the figure would obviously be connected—and function—in the same way discussed elsewhere.” *Id.* (citing Ex. 1003 ¶ 146; Ex. 1004 ¶¶ 282–286).

The preamble of claim 1 ([1-PRE]) recites “[a] stage circuit having a first input terminal, a second input terminal, a third input terminal, and an output terminal.” Ex. 1001, 9:43–45. Petitioner cites Kimura's teaching of a “display device” with a “shift register circuit.” Pet. 14 (citing Ex. 1004 ¶ 320). Petitioner notes that Kimura's Figure 34 shows a shift register formed from shift register stages, and Petitioner contends that Kimura's Figure 27C shows one exemplary shift register stage. *Id.* at 14–17 (citing Ex. 1003 ¶¶ 133–147; Ex. 1004 ¶¶ 72, 320, 324, 333, 339, Figs. 27C, 34).

Petitioner provides an annotated version of Kimura's Figure 27C, which is reproduced below, to illustrate its analysis for the preamble of claim 1.



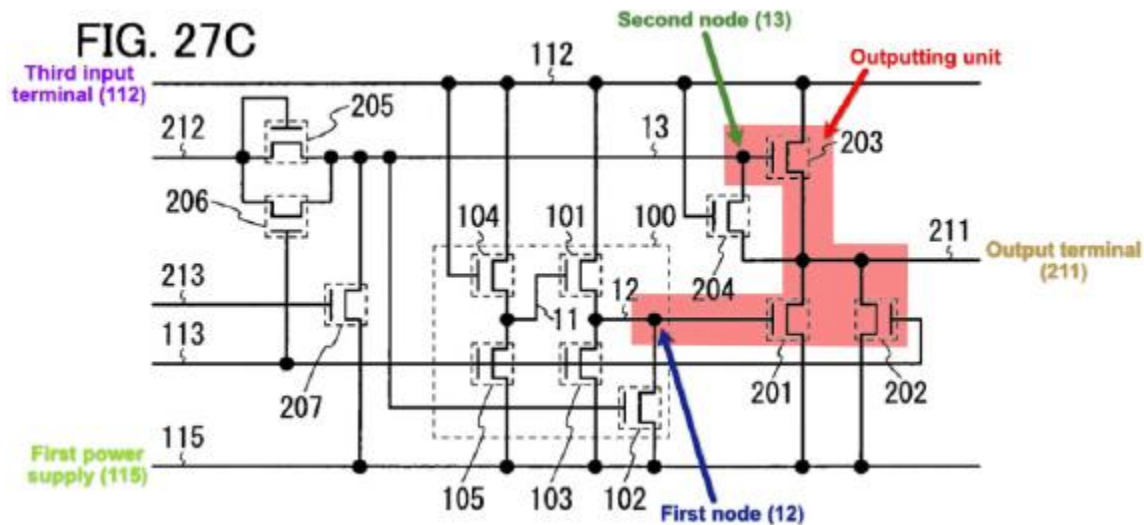
Pet. 16. Figure 27C of Kimura is a circuit diagram of a semiconductor device in Kimura’s “Embodiment 2,” which is described at paragraphs 218–319 of Kimura. Ex. 1004 ¶ 72. Petitioner has indicated its mapping of the “first input terminal” in gray, the “second input terminal” in red, the “third input terminal” in purple, and the “output terminal” in gold. Pet. 16. Specifically, Petitioner maps the “first input terminal” to Kimura’s wiring 212, the “second input terminal” to Kimura’s wiring 113, the “third input terminal” to Kimura’s wiring 112, and the “output terminal” to Kimura’s wiring 211. *Id.* at 17 (citing Ex. 1003 ¶¶ 136–144; Ex. 1004 ¶¶ 103–104, 109, 226, 230–232, 266). Petitioner notes that Kimura’s signal IN4 is inputted to wiring 212 (i.e., the “first input terminal”); Kimura’s signal IN2 is inputted to wiring 113 (i.e., the “second input terminal”); Kimura’s signal IN1 is inputted to wiring 112 (i.e., the “third input terminal”); and Kimura’s signal GOUT is outputted at wiring 211 (i.e., the “output terminal”). *Id.*

Limitation [1-A] recites

an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the

output terminal according to a voltage applied to the first node and a signal of the third input terminal to the output terminal according to a voltage applied to the second node.

Ex. 1001, 9:46–51. Petitioner provides another annotated version of Kimura’s Figure 27C, reproduced below, to illustrate its analysis for this limitation.



Pet. 17. Figure 27C of Kimura is a circuit diagram of a semiconductor device in Kimura’s “Embodiment 2,” which is described at paragraphs 218–319 of Kimura. Ex. 1004 ¶ 72. Petitioner has indicated its mapping of the “third input terminal” in purple, the “first power supply” in light green, the “first node” in dark blue, the “second node” in dark green, the “outputting unit” in red, and the “output terminal” in gold. Pet. 17. Specifically, Petitioner maps the “first power supply” to voltage V_1 that is supplied to Kimura’s wiring 115. *Id.* at 18 (citing Ex. 1004 ¶ 105). Petitioner maps the recited “first node” to Kimura’s node 12 and contends that “the gate of transistor 201 is connected to and controlled by node 12 . . . exiting from circuit 100.” *Id.* (citing Ex. 1004 ¶¶ 222, 226, Fig. 27C). Petitioner maps the recited “second node” to Kimura’s node 13 and contends that

transistor 203 is “controlled by the potential of the node 13.” *Id.* (quoting Ex. 1004 ¶ 250). As shown with red highlighting in Petitioner’s annotated version of Kimura’s Figure 27C, Petitioner maps the recited “outputting unit” to, *inter alia*, transistors 201–203. *Id.* at 17. Petitioner contends that “[t]ransistors 201-203 are responsible for generating stage output” and that transistor 203 “control[s] conduction between the wiring 112 and the wiring 211.” *Id.* at 17–18 (citing Ex. 1004 ¶ 250) (second alteration in original).

Petitioner provides the following explanation of how the alleged “outputting unit” of Kimura’s Figure 27C creates the output at wiring 211:

In operation, during a “period A” input signals are supplied to the shift register to cause “the potential of the node 12” to be “set at a H level.” This causes “transistor 201” to be “turned on” supplying “the potential of the wiring 115 (e.g., the voltage V_1) to the wiring 211.” During “period C” and “period D,” however, different input signals cause “the potential of the node 12” to be “set at an L level” so that “transistor 201 is turned off.” At the same time, “the potential of the node 13 becomes an H level” allowing “transistor 203” to be turned on and “signal IN1” to be supplied to wiring 211.

Pet. 18 (cleaned up) (quoting Ex. 1004 ¶¶ 253, 255–256). Petitioner also cites the timing diagram in Kimura’s Figure 21B, which is reproduced below.

FIG. 21B

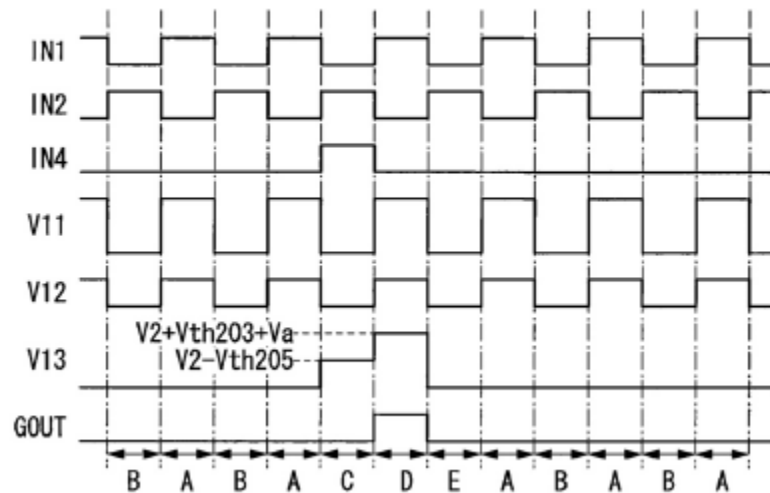
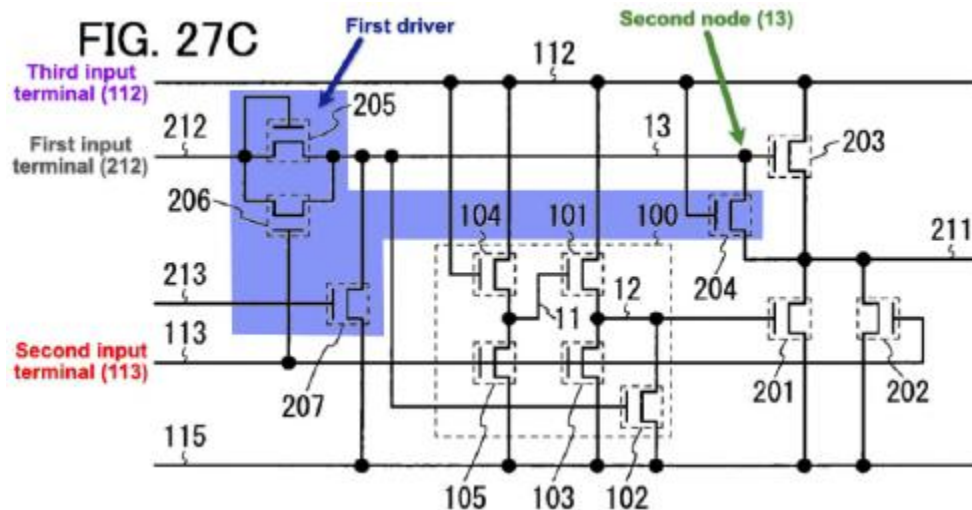


Figure 21B depicts a timing chart illustrating the operation of the semiconductor device in Kimura’s “Embodiment 2,” which is described at paragraphs 218–319 of Kimura. Ex. 1004 ¶ 66. Although Petitioner acknowledges that this timing chart “is not specific to the device of Figure 27C,” Petitioner nonetheless contends that an ordinarily skilled artisan “would have understood that that device—because it includes the same input and output lines and many of the same transistors as Kimura’s other circuits—would (or at least obviously could) be supplied with input signals in the same manner and with the same timing.” Pet. 19 (citing Ex. 1003 ¶¶ 160–165); *see also id.* at 15 (citing Ex. 1003 ¶ 146) (acknowledging that Kimura’s discussion of Figure 27C “does not itself mention all the depicted transistors, inputs, and outputs” but contending that an ordinarily skilled artisan “would have understood that any shared components in Figure 27C . . . would obviously be connected—and function—in the same way discussed elsewhere”).

Limitation [1-B] recites “a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second

input terminal, and the third input terminal.” Ex. 1001, 9:52–54. Petitioner provides another annotated version of Kimura’s Figure 27C, reproduced below, to illustrate its analysis for this limitation.

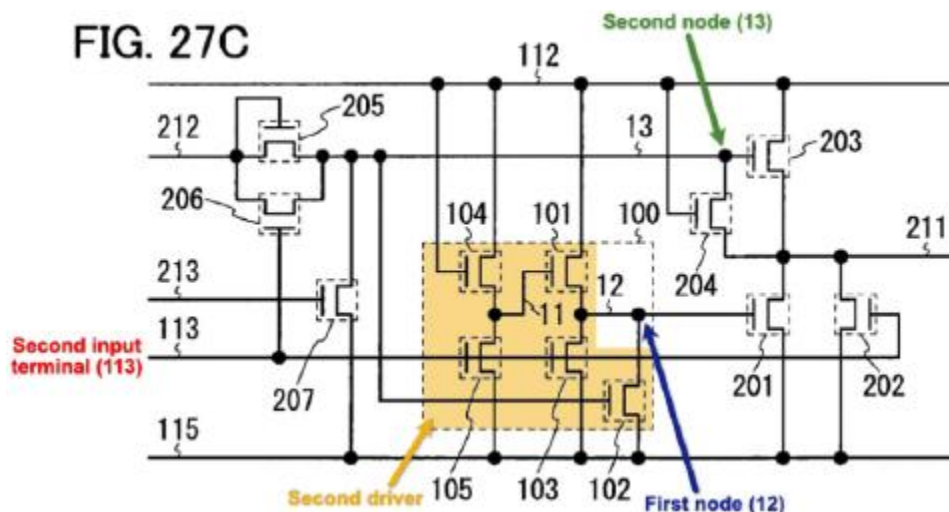


Pet. 20. Figure 27C of Kimura is a circuit diagram of a semiconductor device in Kimura’s “Embodiment 2,” which is described at paragraphs 218–319 of Kimura. Ex. 1004 ¶ 72. Petitioner has indicated its mapping of the “first input terminal” in gray, the “second input terminal” in red, the “third input terminal” in purple, and the “first driver” in blue, and the “second node” in dark green. Pet. 20. In particular, Petitioner maps the recited “first driver” to transistors 204–207, and Petitioner contends these transistors collectively control the potential of node 13 (i.e., the recited “second node”). *Id.* at 20–21 (citing Ex. 1003 ¶¶ 172–179; Ex. 1004, Figs. 17B, 21B).

Petitioner contends that transistor 205 “control[s] conduction between the wiring 212 and the node 13,” including the provision of a high-level signal from wiring 212 to node 13. Pet. 20 (citing Ex. 1004 ¶ 268) (alteration in original). Petitioner also contends that transistor 206 has its gate connected to wiring 113, so transistor 206 facilitates “conduction

between the wiring 212 and the node 13” and allows for the supply of a low-level signal from wiring 113 to node 13. *Id.* (citing Ex. 1004 ¶¶ 270–272). Petitioner further contends that transistor 204 has a gate connected to wiring 112 and its first terminal connected to wiring 211, which “allows ‘the potential of the node 13’ to be ‘lowered’ for purposes of preventing ‘dielectric breakdown or deterioration of’ any transistors connected to the node.” *Id.* at 20–21 (quoting Ex. 1004 ¶ 286). Petitioner additionally contends that transistor 207 receives input from wiring 213 and operates to connect wiring 115 to node 13. *Id.* at 21 (citing Ex. 1004 ¶¶ 276–280).

Limitation [1-C] recites “a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node.” Ex. 1001, 9:55–57. Petitioner provides another annotated version of Kimura’s Figure 27C, reproduced below, to illustrate its analysis for this limitation.



Pet. 23. Figure 27C of Kimura is a circuit diagram of a semiconductor device in Kimura’s “Embodiment 2,” which is described at paragraphs 218–319 of Kimura. Ex. 1004 ¶ 72. Petitioner has indicated its mapping of the

“second input terminal” in red, the “first node” in dark blue, and the “second node” in dark green. Pet. 23. Petitioner maps the recited “second driver” to circuit 100 (which includes transistors 101–105 and is indicated in yellow), and Petitioner contends that circuit 100 controls the potential of node 12 (i.e., the recited “first node”) and connected transistor 201. *Id.* (citing Ex. 1004 ¶¶ 114, 115, 222, 226). According to Petitioner, circuit 100 controls the potential based on (1) signal IN2, which flows through wiring 113 (the recited “second input terminal”) to the gates of transistors 103 and 105; and (2) signal IN3 at node 13 (the recited “second node”), which is connected to the gate of transistor 102. *Id.* (citing Ex. 1003 ¶¶ 182–187; Ex. 1004 ¶¶ 119, 121, 249).

Limitation [1-D] recites “the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver.” Ex. 1001, 9:58–60. Petitioner contends that in Kimura’s Figure 27C embodiment, wiring 112 (i.e., the “third input terminal”) is connected to the gate of transistor 204, which is part of the “first driver” in Petitioner’s analysis.

b. The Parties’ Arguments After Institution

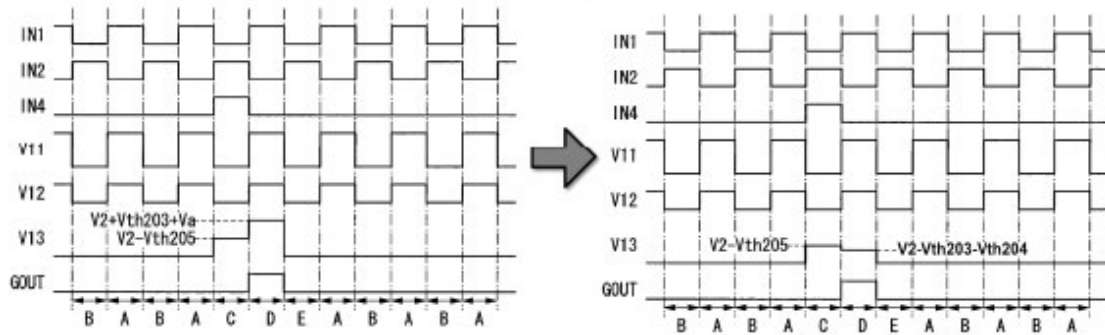
Patent Owner argues that “Kimura’s description of Figure 27C . . . is *not* compatible with the timings shown in Figure 21B.” PO Resp. 13 (citing Ex. 2059 ¶ 52). According to Patent Owner, Figure 21B shows the potential at its highest level for node 13 (i.e., “V13”) in period D, whereas Kimura’s paragraph 286, which explicitly describes the circuit of Figure 27C, states that “in a period D, the potential of the node 13 can be *lowered*.” *Id.* at 13–14 (emphasis by Patent Owner) (quoting Ex. 1004 ¶ 286). Patent Owner

argues that “Petitioner and its expert do not address this discrepancy, or attempt to explain why [an ordinarily skilled artisan] would nevertheless understand Figure 21B’s timings to be compatible with the Figure 27C circuit.” *Id.* at 14.

In its Reply, Petitioner argues that the Petition “relies on Figure 21B for its ‘**input signals**’ IN1, IN2, and IN4 used to drive the circuit not the internal node voltages.” Pet. Reply 6 (citing Pet. 19). Petitioner explains that “these input signals are the **same** in all the figures on which Figure 27C is based.” *Id.* at 6–8 (citing Ex. 1004, Figs. 14A, 15A, 17A, 17B, 21A, 21B, 25A, 25B; Ex. 1025 ¶¶ 46–60; Ex. 1026, 24:25–29:25, 30:2–37:14). Petitioner also distinguishes these input signals from the “internal node voltages of [the] Figure 27C circuit” on which Patent Owner bases its period D arguments. *Id.* at 8.

Petitioner additionally explains that Kimura’s Figure 21B timing diagram shows a high potential for node 13 in period D due to a “bootstrap operation” that occurs in Kimura’s Figure 21A circuit. Pet. Reply 8–9 (citing Ex. 1004 ¶¶ 256, 269, Fig. 21A; Ex. 1025 ¶¶ 65–66). Petitioner contrasts this situation with what occurs in Kimura’s Figure 27C circuit, which allegedly lowers the potential of node 13 in period D to avoid transistor dielectric breakdown or deterioration rather than letting it increase via bootstrapping. *Id.* at 9–11 (citing Ex. 1004 ¶ 286, Fig. 27C; Ex. 1025 ¶¶ 11–26, 61–64, 67–73; Ex. 1026, 35:1–38:19). To show this lowering effect in the Figure 27C circuit, Petitioner provides the following illustration of the change to Kimura’s Figure 21B timing diagram.

FIG. 21B



In this illustration from Petitioner’s Reply, Petitioner presents two versions of Kimura Figure 21B timing diagram. *Id.* at 10–11 (citing Ex. 1004, Fig. 21B; Ex. 1025 ¶¶ 61–64). The potential of node 13 in period D has been modified from $V_2 + V_{th203} + V_a$ in the left version of the timing diagram to “approximately $V_2 - V_{th203} - V_{th204}$ ” in the right version of the timing diagram. *Id.*

In its Sur-reply, Patent Owner argues that Petitioner has “change[d] theories from those presented in the Petition,” so we should reject those new theories as improper new argument. PO Sur-reply 1. Specifically, Patent Owner argues that Petitioner has manufactured a distinction between “input signals” and “internal node voltages” that is unfounded. *Id.* at 6 (citing Ex. 1004 ¶ 249). Patent Owner also notes that many of Kimura’s circuits that are cited by Petitioner have additional input signals that are not the same as those used with other circuits. *Id.* at 6–7 (citing Ex. 1004, Figs. 15A, 21B, 25B; Ex. 1025 ¶ 37; Ex. 2062, 32:12–20, 54:3–55:10). Patent Owner additionally criticizes Petitioner’s assertion that the Figure 27C circuit is “meant only to adjust circuit operation in period D” as being unfounded. *Id.* at 7–8 (citing Pet. Reply 11). Patent Owner also criticizes Petitioner’s modified version of Kimura’s Figure 21B timing diagram as being “based

entirely on Dr. Foty’s unsubstantiated new speculation” and as “find[ing] no support in Kimura’s disclosure.” *Id.* at 8 (citing Pet. Reply 10).

c. Analysis

We agree with Patent Owner that Petitioner’s contentions for this ground are fatally flawed because they are internally inconsistent. First, Petitioner’s argument about lowering the potential of node 13 in Kimura’s Figure 27C circuit during period D to combat bootstrapping (Pet. 20–21; Pet. Reply 8–11) directly conflicts with another explanation of circuit operation at page 18 of the Petition. In that explanation, Petitioner cites Kimura for teaching that “‘the potential of the node 13 becomes an H level’ allowing ‘transistor 203’ to be turned on and ‘signal IN1’ to be supplied to wiring 211.” Pet. 18 (quoting Ex. 1004 ¶ 256). Obviously, an “H level” or high-level potential cannot be squared with the alleged lowering of the potential during the same period to combat bootstrapping. And Patent Owner provides an accurate diagnosis for this inconsistency: Petitioner cites Kimura’s discussions of different circuit embodiments throughout its analysis for claim 1, but fails to reconcile the differences in a coherent way. *See* PO Resp. 12–14.

Second, this same problem exists with Petitioner’s citation of Kimura’s Figure 21B timing diagram. *See* Pet. 19. Although Petitioner acknowledged in the Petition that this timing diagram is not specific to the circuit in Kimura’s Figure 27C, Petitioner did not specify how the diagram would change. *See id.* That explanation was presented for the first time in Petitioner’s Reply. *See* Pet. Reply 9–11. The result was a changed Figure 21B timing diagram with a lengthy new explanation about

combatting dielectric breakdown caused by bootstrapping. *See id.* Petitioner also attempts to disavow its reliance in the Petition on the Figure 21B timing diagram for all but certain input signals based on a newly raised distinction vis-à-vis “internal node voltages.” *See id.* at 6–9. We find Petitioner’s belated explanation regarding bootstrapping and *ex post* rationalizations regarding the timing diagram to represent “a new direction with a new approach as compared to the positions taken in a prior filing.” Patent Trial and Appeal Board Consolidated Trial Practice Guide at 74 (Nov. 2019) (“Consolidated Trial Practice Guide”), *available at* <https://www.uspto.gov/sites/default/files/documents/tpgnov.pdf>. As such, we agree with Patent Owner (PO Resp. 1) that Petitioner’s new analysis amounts to improper reply argument. *See* 37 C.F.R. § 42.23(b) (“A reply may only respond to arguments raised in the corresponding . . . patent owner response, or decision on institution.”).

Furthermore, even if Kimura supports Petitioner’s analysis of Kimura’s efforts to address bootstrapping by lowering the potential of node 13 (Ex. 1004 ¶ 286), this still cannot square with Petitioner’s separate explanation of the circuit’s operation where Petitioner said that the potential of node 13 in period D is high. *See* Pet. 18. We would have to ignore this contrary passage from the Petition, where Petitioner cites teachings of Kimura that do not apply to the Figure 27C circuit, to rule in favor of Petitioner. We decline to do so.

Although Petitioner is correct that Kimura’s circuit embodiments have common elements and input signals that tend to build upon one another (Pet. 15–16; Pet. Reply 3–6), this circumstance does not excuse Petitioner from acknowledging and rectifying the differences among the embodiments

when setting forth its unpatentability contentions. Given the discrepancies in Petitioner’s analysis, we determine that Petitioner has not shown by a preponderance of the evidence that the subject matter of claim 1 would have been obvious over Kimura.

3. *Claims 2–8 and 14*

Claims 2–8 and 14 depend directly or indirectly from claim 1. *See* Ex. 1001, 9:61–10:45, 11:6–8. Petitioner’s analysis for claims 2–8 and 14 relies on the same deficient analysis that is discussed above with respect to claim 1. *See* Pet. 24–37. Further, Petitioner’s analysis for these claims does not cure the deficiencies discussed above with respect to claim 1. Thus, we determine that Petitioner has not shown by a preponderance of the evidence that the subject matter of claims 2–8 and 14 would have been obvious over Kimura.

4. *Claim 15*

Claim 15 is an independent claim directed to “[a]n organic light emitting display” that shares some similarities with claim 1. *See* Ex. 1001, 11:9–36. Petitioner relies on the same deficient analysis that is discussed above with respect to claim 1. *See* Pet. 37–41. Thus, we determine that Petitioner has not shown by a preponderance of the evidence that the subject matter of claim 15 would have been obvious over Kimura.

5. *Claims 16–22 and 25*

Claims 16–22 and 25 depend directly or indirectly from claim 15. *See* Ex. 1001, 11:37–12:27, 12:39–42. Petitioner’s analysis for claims 16–22

and 25 relies on the same deficient analysis that is discussed above with respect to claim 1. *See* Pet. 41–44. Further, Petitioner’s analysis for these claims does not cure the deficiencies discussed above with respect to claim 1. Thus, we determine that Petitioner has not shown by a preponderance of the evidence that the subject matter of claims 16–22 and 25 would have been obvious over Kimura.

E. Obviousness Grounds Based on Shin and Sasaki

Petitioner contends that the subject matter of claims 1–6, 8, 14–20, 22, and 25 would have been obvious over the combination of Shin and Sasaki. Pet. 44–73; Pet. Reply 18–22. Patent Owner disputes Petitioner’s contentions. PO Resp. 31–38; PO Sur-reply 16–18.

1. Shin

Shin is a U.S. Patent Application Publication directed to a scan driving circuit for an OLED display. Ex. 1005, code (57). Figure 4 of Shin is reproduced below.

FIG. 4

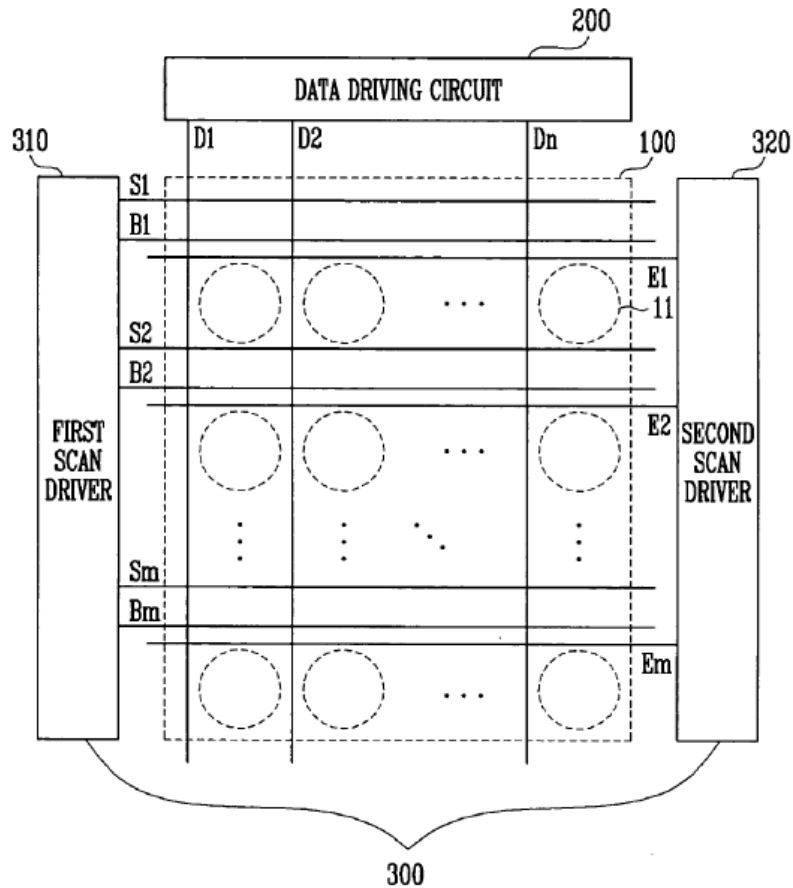


Figure 4 of Shin depicts an organic light emitting display including organic light emitting display panel 100, data driving circuit 200, and scan driving circuit 300. *Id.* ¶¶ 41–42. Scan driving circuit 300 includes first scan driver 310, which provides a selection signal and/or a boost signal, and second scan driver 320, which provides an emission signal. *Id.* ¶ 42.

Figure 10 of Shin is reproduced below.

FIG. 10

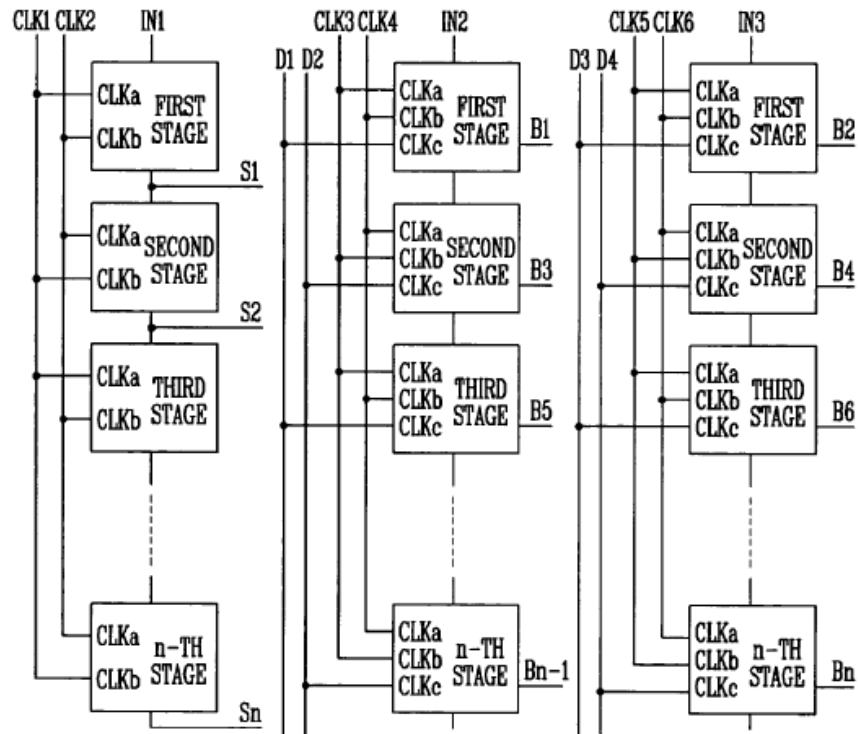
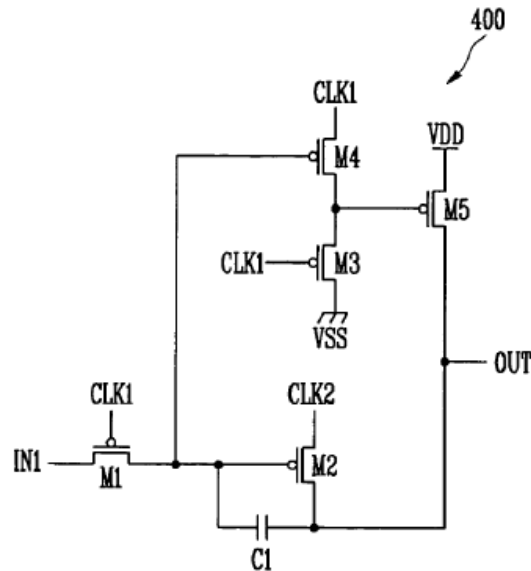


Figure 10 of Shin depicts a first scan driving circuit, which is divided into a scan drive unit and a boost drive unit for outputting a selection signal and a boost signal, respectively. Ex. 1005 ¶¶ 115, 117.

An excerpt of Figure 11 of Shin is reproduced below.

FIG. 11



This excerpt of Shin's Figure 11 depicts a circuit diagram of odd-numbered stage 400 in a first scan driver of the scan driving circuit. Ex. 1005

¶¶ 88, 120. Odd-numbered stage 400 includes transistors M1, M2, M3, M4, and M5. *Id.* ¶ 88. Transistor M1 receives first input signal IN1, and the gate terminal of transistor M1 is coupled with a first clock terminal that receives first clock signal CLK1. *Id.* ¶¶ 88, 90. Transistor M2 is coupled with a second clock terminal (which receives second clock signal CLK2) and an output line OUT, and the gate terminal is coupled with an output terminal of transistor M1. *Id.* Transistor M3 is coupled between second power supply VSS and first node N1,⁴ and the gate terminal of transistor M3 is coupled

⁴ Although the written description of Shin refers to first node N1, the drawing figures do not show such a node. We interpret Shin's first node N1 as the location between transistors M3 and M4 that is coupled to the gate terminal of transistor M5.

with the first clock terminal (which receives first clock signal CLK1). *Id.* Transistor M4 is coupled between the first clock terminal and first node N1, and the gate terminal of transistor M4 is coupled with an output terminal of transistor M1. *Id.* Transistor M5 is coupled between first power supply VDD and output line OUT, and the gate terminal of transistor M5 is coupled with first node N1. *Id.* Capacitor C1 is coupled between the output terminal of transistor M1 and output line OUT. *Id.* ¶ 89.

2. Sasaki

Sasaki is a U.S. Patent Application Publication directed to “a shift register in an electronic circuit being operated by a pulse-cut clock signal, and to a drive circuit, an electrode substrate and a display device that include[s] the shift register.” Ex. 1014 ¶ 3. Figure 4 of Sasaki is reproduced below.

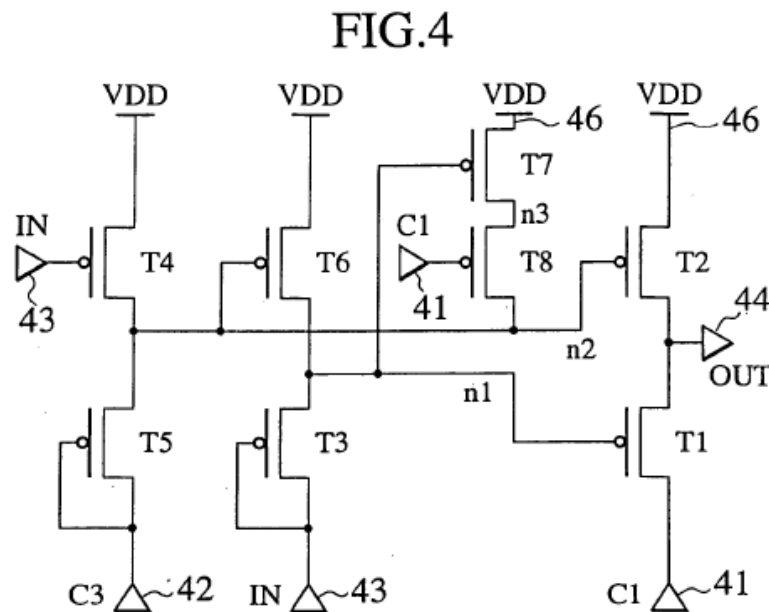


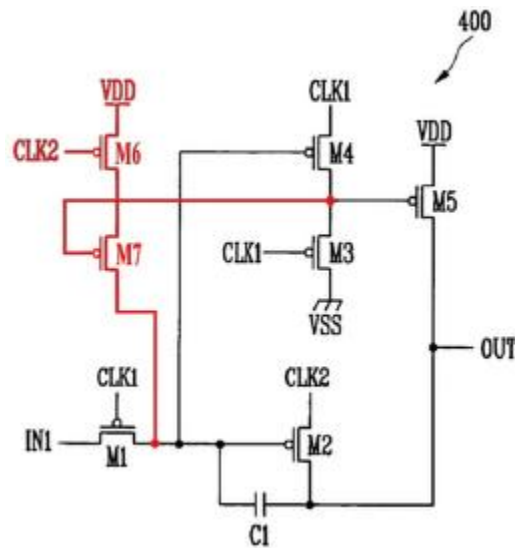
Figure 4 of Sasaki depicts a shift register. *Id.* ¶ 15. The shift register includes an anti-reversal circuit comprising seventh transistor T7 and eighth

transistor T8. *Id.* ¶ 42. “The anti-reversal circuit prevents a voltage level at the control electrode of the second transistor T2 from being reversed, which is attributable to a floating state of the control electrode of the second transistor T2.” *Id.*

3. *Claim 1*

Petitioner’s analysis for claim 1 is based on the “scan driving circuit” in Figure 11 of Shin. Pet. 44–45 (citing Ex. 1005 ¶¶ 3, 16, Fig. 11). Petitioner contends that an ordinarily skilled artisan would have known that transistors in Shin’s circuit are susceptible to the problem of reversal, as recognized by Sasaki, which means that a transistor is “open when it is supposed to be closed” due to the control electrode entering a floating state. *Id.* at 46 (citing Ex. 1003 ¶¶ 364–369; Ex. 1014 ¶ 42). According to Petitioner, reversal “can result in unwanted mixing of high and low signals at the output terminal.” *Id.* at 46–47 (citing Ex. 1014 ¶ 42).

Thus, Petitioner proposes a modification of Shin’s Figure 11 circuit to include an anti-reversal circuit like that disclosed in Sasaki’s Figure 4. Pet. 51 (citing Ex. 1003 ¶¶ 363, 389–391). Petitioner provides an illustration of this modified circuit on page 50 of the Petition, as reproduced below.



Id. at 50. In this illustration, Petitioner has modified the circuit of Shin’s Figure 11 (shown in black) with the anti-reversal elements disclosed in Sasaki (shown in red). *Id.* (citing Ex. 1003 ¶ 390). Among the added elements are transistors M6 and M7, which allegedly “operate to supply a high VDD signal to transistor M2’s gate to prevent the transistor from opening and inadvertently supplying a low CLK2 signal to OUT at a time when the circuit’s output is intended to be high.” *Id.* at 50–51 (citing Ex. 1003 ¶ 390).

Petitioner acknowledges that Shin’s circuit already has “capacitor C1 electrically connected to transistor M2’s gate” as an anti-reversal measure, but Petitioner contends that an ordinarily skilled artisan “would have recognized that this capacitor is not sufficient by itself to address Shin’s anti-reversal problem.” Pet. 49; Ex. 1003 ¶ 385. Petitioner cites the timing diagram in Shin’s Figure 9 and contends that “in period t_2 , the capacitor [C1] has not accumulated significant charge that would allow it to guarantee reversal protection” and that “the lowering of the potential at transistor M2’s gate due to the transition of CLK2 to low further minimizes the capacitor’s

effect.” Pet. 49 (citing Ex. 1003 ¶¶ 383–386, 389). According to Petitioner, an ordinarily skilled artisan “would have recognized that Sasaki’s anti-reversal circuit accounts for the lack of robustness of the capacitor and ensures that transistor M2 is reliably kept closed.” *Id.* (citing Ex. 1003 ¶¶ 387–389).

Patent Owner disputes Petitioner’s rationale for combining Sasaki with Shin because “Shin already contains circuitry, namely capacitor C1, which Shin explains will mitigate concerns of reversal at the node to which Petitioner proposes to add these additional circuit elements.” PO Resp. 33 (citing Ex. 2059 ¶ 89). Patent Owner cites Shin’s teaching that, to counter the “floating state” at the gate of transistor M2, “a voltage of the capacitor C1 remains unchanged, and thus the second transistor M2 continues to be turned-on.” *Id.* (quoting Ex. 1005 ¶ 107). Patent Owner argues that “there is nothing in Shin that states or would suggest to [ordinarily skilled artisans] that capacitor C1 is ‘not robust enough’ to carry out the specific function for which Shin teaches it is provided.” *Id.* at 34 (citing Ex. 2059 ¶ 92). Patent Owner likewise argues that nothing in Shin suggests that adding two extra transistors (M6 and M7) to existing capacitor C1 would have been “necessary, or even helpful” to maintain the gate voltage at capacitor M2. *Id.* at 33–34 (citing Ex. 2059 ¶ 92).

In its Reply, Petitioner argues that the proposed benefits of its proposed modification are not merely theoretical given Petitioner’s undisputed showing that transistor M2 is vulnerable during certain periods of operation. Pet. Reply 18–19 (citing Pet. 47–48; Ex. 1003 ¶¶ 380–383; Ex. 1014 ¶ 42). Petitioner notes a potential reversal problem in periods outside of what Shin calls its “evaluation period.” *Id.* at 19–21 (citing, *inter*

alia, Ex. 1025 ¶¶ 76–87). Petitioner also asserts that considerations about “[p]roper circuit functionality” would trump concerns about increased complexity, decreased stability, and lower process yields brought about by Petitioner’s proposed modification. *Id.* at 21–22.

In its Sur-reply, Patent Owner calls Petitioner’s explanation about periods other than Shin’s evaluation period a “new and different argument.” PO Sur-reply 2. Patent Owner notes that the Petition only discusses one period in which Shin’s capacitor C1 might be insufficient, and, as such, Patent Owner asks us to reject Petitioner’s arguments about additional time periods. *Id.* at 16–17 (citing Pet. 51). Patent Owner also argues that capacitor C1 already protects the node in question in the additional time periods and prevents the reversal problem on which Petitioner bases its proposed modification. *Id.* at 17 (citing PO Resp. 31–40; Ex. 2059 ¶¶ 90–92). Patent Owner additionally cites Dr. Wolfe’s testimony that an ordinarily skilled artisan already would have taken into account the potential problems Petitioner cites—crosstalk and electromagnetic interference—when designing a circuit. *Id.* (citing Ex. 2019 ¶ 89; Ex. 2059 ¶ 92).

We are persuaded by Patent Owner’s arguments. Petitioner’s obviousness rationale is based on “the potential of reversal” in Shin’s transistor M2 when its gate electrode is in a floating state. Pet. 49 (citing Ex. 1003 ¶ 384). Yet, as highlighted by Patent Owner (PO Resp. 32–34; PO Sur-reply 17) and as acknowledged by Petitioner (Pet. 49–50), Shin already contemplates this problem and provides capacitor C1 to combat it. Specifically, Shin states that when “a gate terminal of the second transistor M2 is in a floating state, a voltage of the capacitor C1 remains unchanged, and thus the second transistor M2 continues to be turned-on.” Ex. 1005

¶ 107. As such, Petitioner’s rationale hinges on its allegation that reversal issues persist in Shin’s circuit despite the described function of capacitor C1. See Pet. 49–50; Ex. 1003 ¶¶ 384–385, 390.

Nevertheless, we agree with Patent Owner (PO Resp. 32–35) that Petitioner does not show persuasively that further reversal protection in Shin’s circuit would have been necessary or even desirable. Although Petitioner alleges a “lack of robustness” in Shin’s circuit (Pet. 49 (citing Ex. 1003 ¶¶ 387–389)), Petitioner’s allegations are merely hypothetical. See *id.* (citing Ex. 1003 ¶ 385) (basing the alleged deficiency on “the *potential* of reversal” and an inability to “*guarantee* reversal protection” (emphasis added)). Indeed, Dr. Foty testifies that electromagnetic interference or crosstalk at a floating node could “create[] the *possibility* of a reversal event.” Ex. 1003 ¶ 384 (emphasis added). But Dr. Wolfe testifies that an ordinarily skilled artisan already would have taken these considerations into account when designing a circuit, as evidenced by Shin’s provision of capacitor C1 for anti-reversal protection. See Ex. 2059 ¶ 92. Specifically, Dr. Wolfe testifies that “the maximum time for which C1 must maintain its signal is known at design time and can easily be guaranteed” given that “transistor M1 is enabled by a clock.” *Id.* We find Dr. Wolfe’s testimony persuasive and consistent with Shin’s express disclosure. See Ex. 1005 ¶ 107.

We additionally find Petitioner’s reply arguments about additional time periods where reversal might occur (Pet. Reply 19–21) to be improper reply argument representing a new direction in the argument. See 37 C.F.R. § 42.23(b); Consolidated Trial Practice Guide at 74. Petitioner could have, but did not, discuss these allegations of Shin’s circuit malfunctioning outside

of the “evaluation period” in the Petition. And, in any event, we are more persuaded by Patent Owner’s arguments (as supported by Dr. Wolfe’s testimony) that Shin’s circuit is already designed to protect against reversal throughout the course of its operation. *See, e.g.*, Ex. 2059 ¶¶ 90–92.

One other weakness in Petitioner’s obviousness rationale pertains to disadvantages with its proposed combination. Patent Owner notes the ’593 patent’s recognition that adding transistors to a circuit increases complexity, decreases stability, and lowers process yield. PO Resp. 34 (citing Ex. 1001, 9:12–26). Patent Owner also cites known concerns in the prior art about increasing circuit area. *Id.* (citing Ex. 1006 ¶¶ 15, 107). Although Petitioner does not address these known concerns in the Petition, Petitioner suggests in reply that they are less important than “[p]roper circuit functionality.” Pet. Reply 21 (citing Ex. 1025 ¶¶ 88–97). As stated above, however, Petitioner has not shown persuasively that Shin’s circuit suffers from the operational faults that Petitioner suggests. Thus, we find that Patent Owner’s cited disadvantages also tend to undermine Petitioner’s rationale for making the combination.

For these reasons, Petitioner has not shown persuasively that an ordinarily skilled artisan would have modified Shin’s circuit to additionally include the anti-reversal elements taught by Sasaki. Thus, we determine that Petitioner has not shown by a preponderance of the evidence that the subject matter of claim 1 would have been obvious over the combination of Shin and Sasaki.

4. *Claims 2–6, 8, and 14*

Claims 2–6, 8, and 14 depend directly or indirectly from claim 1. *See* Ex. 1001, 9:61–10:22, 10:36–45, 11:6–8. Petitioner’s analysis for claims 2–6, 8, and 14 relies on the same faulty rationale for combining Sasaki with Shin that is discussed above with respect to claim 1. *See* Pet. 44–53, 59–66. Thus, we determine that Petitioner has not shown by a preponderance of the evidence that the subject matter of claims 2–6, 8, and 14 would have been obvious over the combination of Shin and Sasaki.

5. *Claim 15*

Claim 15 is an independent claim directed to “[a]n organic light emitting display” that shares some similarities with claim 1. *See* Ex. 1001, 11:9–36. Petitioner relies on the same faulty rationale for combining Sasaki with Shin that is discussed above with respect to claim 1. *See* Pet. 44–53, 67–71. Thus, we determine that Petitioner has not shown by a preponderance of the evidence that the subject matter of claim 15 would have been obvious over the combination of Shin and Sasaki.

6. *Claims 16–20, 22, and 25*

Claims 16–20, 22, and 25 depend directly or indirectly from claim 15. *See* Ex. 1001, 11:37–12:4, 12:18–27, 12:39–42. Petitioner relies on the same faulty rationale for combining Sasaki with Shin that is discussed above with respect to claim 1. *See* Pet. 44–53, 71–73. Thus, we determine that Petitioner has not shown by a preponderance of the evidence that the subject matter of claims 16–20, 22, and 25 would have been obvious over the combination of Shin and Sasaki.

F. Obviousness Grounds Based on Shin, Sasaki, and Jeong

Petitioner contends that the subject matter of claims 7 and 21 would have been obvious over the combination of Shin, Sasaki, and Jeong. Pet. 74–80; Pet. Reply 22–23. Patent Owner disputes Petitioner’s contentions. PO Resp. 38–40.

1. Jeong

Jeong is a U.S. Patent Application Publication directed to “a shift register for a driving circuit for driving a pixel of the organic light emitting display.” Ex. 1007 ¶ 2. Figure 4 of Jeong is reproduced below.

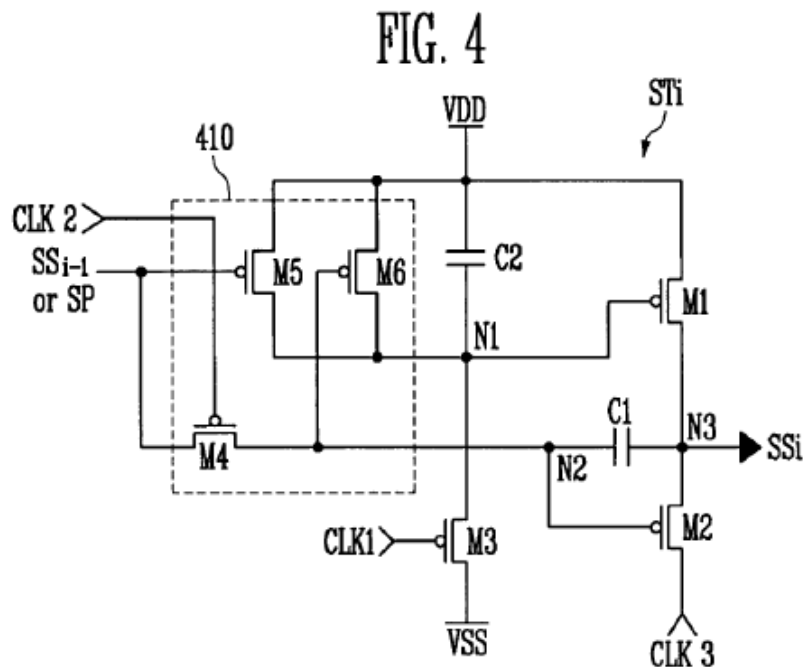


Figure 4 of Jeong is a diagram of a stage circuit. *Id.* ¶¶ 24, 44. The stage circuit includes voltage level controller 410, first to third transistors M1 to M3, and first and second capacitors C1 and C2. *Id.* ¶ 45. Second capacitor C2 is coupled between first power supply VDD and first node N1

and “may function to reduce a variation of a voltage, which may be applied to the first power supply VDD or the first node N1.” *Id.* ¶ 57.

2. *Claims 7 and 21*

Claim 7 depends from claim 2 and claim 21 depends from claim 18. *See* Ex. 1001, 9:61–67, 12:5–17. Petitioner’s rationale for combining Shin, Sasaki, and Jeong incorporates the same faulty rationale for combining Sasaki with Shin that is discussed above with respect to claim 1. *See* Pet. 74–80. Thus, we determine that Petitioner has not shown by a preponderance of the evidence that the subject matter of claims 7 and 21 would have been obvious over the combination of Shin, Sasaki, and Jeong.

G. *Obviousness Grounds Based on Tobita*

Petitioner contends that the subject matter of claims 1, 2, and 15–18 would have been obvious over Tobita. Pet. 80–95; Pet. Reply 23–25. Patent Owner disputes Petitioner’s contentions. PO Resp. 40–48; PO Sur-reply 18–21.

1. *Tobita*

Tobita is a U.S. Patent Application Publication directed to “a shift register for use as a scanning-line driving circuit for an image display apparatus.” Ex. 1006 ¶ 2. Figure 20 of Tobita is reproduced below.

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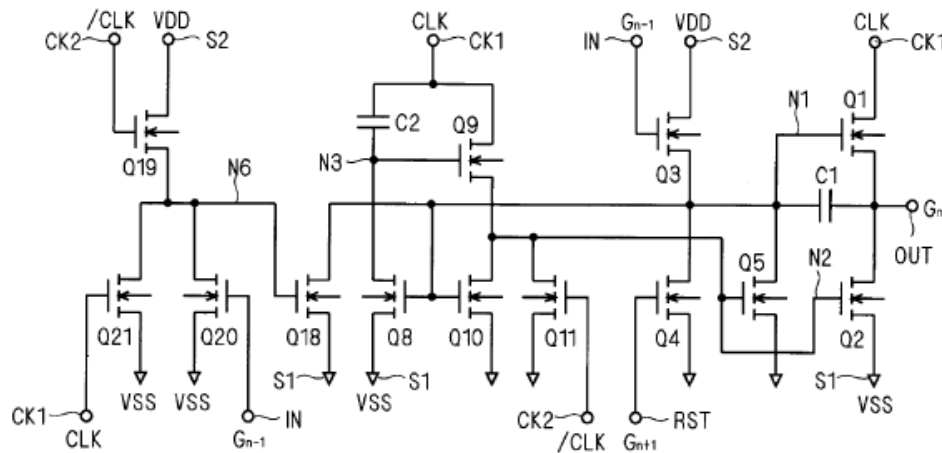


Figure 20 of Tobita is a circuit diagram of unit shift register SR according to what Tobita calls its “eighth preferred embodiment.” *Id.* ¶¶ 39, 172. Unit shift register SR includes transistor Q1 connected between output terminal OUT and first clock terminal CK1 and transistor Q2 connected between output terminal OUT and first power terminal S1. *Id.* ¶ 109. Transistor Q1 is intended to supply clock signal input from first clock terminal CK1 to output terminal OUT, and transistor Q2 is intended to supply low supply voltage VSS to output terminal OUT to discharge output terminal OUT. *Id.* Node N1 is connected to the gate of transistor Q1, and node N2 is connected to the gate of transistor Q2. *Id.* Capacitive element C1 is provided between the gate and source of transistor Q1 to increase the step-up effect at node N1 following the rise in level at output terminal OUT. *Id.* ¶ 110. Transistor Q3, which is connected between node N1 and input terminal IN, has its gate connected to the input terminal IN. *Id.* ¶ 111. Transistor Q4, which has its gate connected to reset terminal RST, and transistor Q5, which has its gate connected to the gate of the transistor Q2 (node N2), are connected in parallel to each other between node N1 and first power terminal S1. *Id.*

Unit shift register SR includes a pull-down driving circuit with (1) an inverter circuit in which node N1 serves as the input node and (2) a buffer circuit receiving the output of the inverter circuit and outputting a signal improved in driving capability to node N2. Ex. 1006 ¶ 113. The inverter circuit is formed of capacitive element C2 and transistor Q8 connected in series between first clock terminal CK1 and first power terminal S1. *Id.* Transistor Q8 has its gate connected to node N1 as the input node of the inverter circuit. *Id.* Capacitive element C2 serves as a capacitive load, and transistor Q8 serves as a driver element. *Id.* The output node of the inverter circuit is node N3 between capacitive element C2 and transistor Q8. *Id.* A clock signal (CLK) input to first clock terminal CK1 is power for this inverter circuit. *Id.* Capacitive element C2 serves as a coupling capacitance for coupling the clock signal to node N3. *Id.*

The buffer circuit is formed of transistors Q9 and Q10 connected in series between first clock terminal CK1 and first power terminal S1. Ex. 1006 ¶ 114. Transistor Q9 is connected between first clock terminal CK1 and node N2, and has its gate connected to node N3. *Id.* Transistor Q10 is connected between node N2 and first power terminal S1, and has its gate connected to node N1. *Id.* Because node N1 is the input node and node N3 is the output node of the inverter circuit, transistors Q9 and Q10 serve as a totem-pole buffer circuit for performing a push-pull operation. *Id.* Power for this buffer circuit is also the clock signal input (CLK) to first clock terminal CK1. *Id.*

The pull-down driving circuit further includes transistor Q11 connected between node N2 and first power terminal S1 with its gate connected to second clock terminal CK2. Ex. 1006 ¶ 115. Transistor Q11 is

controlled by a clock signal input (“/CLK”) to second clock terminal CK2 and supplies node N2 with the low supply voltage VSS to discharge node N2. *Id.* Second clock terminal CK2 receives a clock signal of opposite phase (i.e., “/CLK”) to that input to first clock terminal CK1 (i.e., “CLK”). *Id.*

Tobita describes a problem with optical leakage current that occurs when power supply VDD is connected to the drain of transistor Q3. Ex. 1006 ¶ 170. In this scenario, optical leakage current flows from second power terminal S2 to node N1 through transistor Q3 under the influence of external light incident into the display device or backlit light of a display panel, such that “node N1 rises in level when it is in the high impedance state.” *Id.* In turn, clock signal CLK at first clock terminal CK1 rises, and “node N1 further rises in level by means of the coupling through the gate-to-drain overlap capacitance of the transistor Q1.” *Id.* ¶ 171. Transistor Q1 thereby turns on, and “a malfunction that the output signal G_n reaches the H level occurs.” *Id.*

To combat the optical leakage problem, Tobita’s “eighth preferred embodiment” includes a circuit formed of transistors Q18 to Q21 that “brings the node N1 into the L level with low impedance during a period in which the first clock terminal CK1 is at the H level in the non-selected period of the gate line GL_n .” Ex. 1006 ¶ 172. Transistor Q18 is connected between node N1 and first power terminal S1, and its gate is designated node N6. *Id.* ¶ 173. Transistor Q19 is connected between node N6 and second power terminal S2, and its gate is connected to second clock terminal CK2. *Id.* Transistor Q20 is connected between node N6 and first power terminal S1, and its gate is connected to input terminal IN. *Id.*

Transistor Q21 also is connected between node N6 and first power terminal S1, and its gate is connected to first power terminal S1. *Id.*

Petitioner contends that Tobita qualifies as prior art under 35 U.S.C. § 102(b) based on its publication date.⁵ Pet. 4. Patent Owner does not contest the prior art status of Tobita. We determine that Tobita qualifies as prior art under 35 U.S.C. § 102(b) because Tobita’s publication date of May 1, 2008, is more than one year before the earliest effective filing date of the challenged claims, which is September 20, 2012. Ex. 1001, code (30); Ex. 1006, code (45).

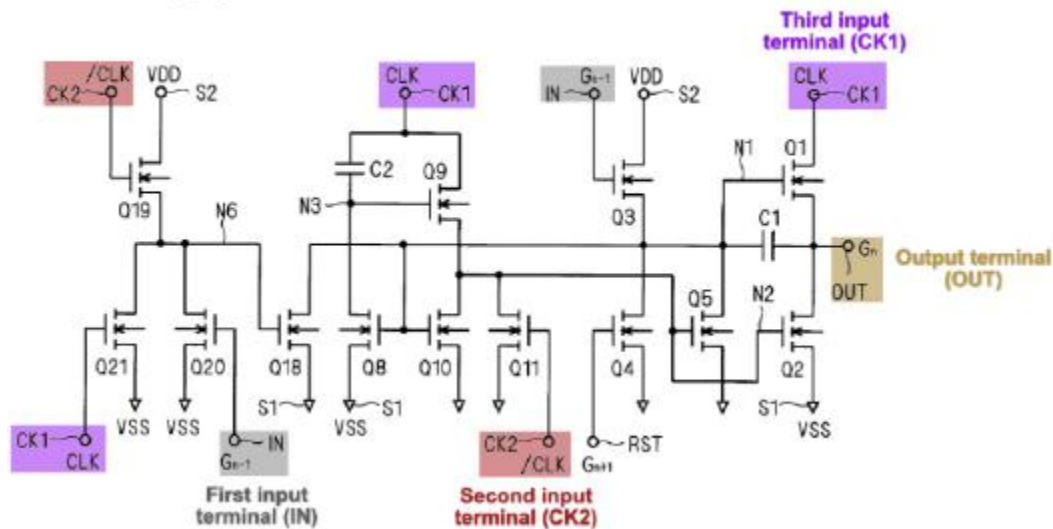
2. *Claim 1*

a. Preamble ([1–PRE])

The preamble of claim 1 recites “[a] stage circuit having a first input terminal, a second input terminal, a third input terminal, and an output terminal.” Ex. 1001, 9:43–45. Petitioner cites the shift register in Tobita’s Figure 20 for teaching the recited “stage circuit.” Pet. 80–82 (citing Ex. 1006 ¶¶ 2, 109, 111, 115, 172, 173, 178, Fig. 20). Petitioner contends that an ordinarily skilled artisan “would have found it obvious to employ Tobita’s circuit with an OLED.” *Id.* at 89 (citing Ex. 1003 ¶¶ 646–648). Petitioner provides an annotated version of Tobita’s Figure 20, which is reproduced below, to illustrate its analysis for the preamble of claim 1.

⁵ Petitioner mistakenly lists Tobita’s publication date as “7/28/2011.” Pet. 4. The actual publication date is May 1, 2008. Ex. 1006, code (43). We consider this to be harmless error.

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Id. at 82. Figure 20 is a circuit diagram illustrating the configuration of a unit shift register according to what Tobita calls its “eighth preferred embodiment.” Ex. 1006 ¶ 172. Petitioner has indicated its mapping of the “first input terminal” in gray, the “second input terminal” in red, the “third input terminal” in purple, and the “output terminal” in gold. Pet. 82. Specifically, Petitioner maps the “first input terminal” to Tobita’s input terminal IN, the “second input terminal” to Tobita’s second clock input terminal CK2, the “third input terminal” to Tobita’s first clock input terminal CK1, and the “output terminal” to Tobita’s output terminal OUT. *Id.* at 81–82 (citing Ex. 1003 ¶¶ 598–601; Ex. 1006 ¶¶ 109, 111, 115, 173, 178, Fig. 20).

Patent Owner argues that “Tobita’s eight embodiment . . . is directed to solving a problem with optical leakage current that may predominantly arise due to the display’s backlight,” but OLED displays do not have

backlights.⁶ PO Resp. 43 (citing Ex. 1006 ¶ 170; Ex. 2059 ¶ 109).

According to Patent Owner, an ordinarily skilled artisan “would not have looked to a reference [like Tobita] directed to liquid crystal displays, let alone an embodiment that adds significant additional circuitry to account for a problem with incident light such as that from backlight leakage for an OLED stage circuit.” *Id.* (citing Ex. 2059 ¶ 109).

We do not agree with Patent Owner’s argument to the extent it suggests that Tobita’s Figure 20 embodiment is limited for use with displays having backlights.⁷ As noted by Petitioner elsewhere in the Petition, Tobita is directed to a “display apparatus,” of which “a liquid crystal display” is only an example. Pet. 89 (citing Ex. 1006 ¶ 4). Furthermore, Tobita associates the Figure 20 embodiment with the problem of an “optical leakage current [that] flows from the second power terminal S2 to the node N1 through the transistor Q3 under the influence of external light incident into the display device or backlit light of a display panel.” Ex. 1006 ¶ 170. Thus, Tobita states that the Figure 20 embodiment is useful for combatting

⁶ Elsewhere in the Patent Owner Response, Patent Owner states that “[t]he ’593 Patent is directed to active-matrix organic light-emitting diode (AMOLED) displays and solving problems specific to those displays.” PO Resp. 5 (citing Ex. 2059 ¶ 41). As discussed below, however, claim 1 does not include any limitations directed to a particular type of display.

⁷ Neither party addresses whether the preamble is limiting and/or whether the recited “stage circuit” of the preamble is limited for use in OLED displays. As discussed below, Petitioner shows persuasively that Tobita teaches the subject matter of the preamble regardless of whether the preamble is so limited, so we need not determine whether the preamble is limiting. *See Realtime Data*, 912 F.3d at 1375.

optical leakage current due to “external light incident into the display device” regardless of other potential benefits for backlit displays. *Id.*

And, even if claim 1 were limited to stage circuits for OLED displays as Patent Owner seems to imply (*see* PO Resp. 43), Petitioner puts forth a persuasive rationale that an ordinarily skilled artisan would have found it obvious to employ Tobita’s circuit with an OLED given that (1) OLEDs were known “to share features with LCD displays including pixel matrices, data drivers, and scan drivers” and (2) LCD and OLED displays were known to “employ structurally and functionally similar stage circuits.” Pet. 89 (citing Ex. 1003 ¶¶ 646–651; Ex. 1015, claims 1, 14). In addition, Dr. Wolfe testifies only that OLED displays are “far less susceptible” to the problem of optical leakage current that is discussed in Tobita, not that the problem is inapplicable to OLED displays. Ex. 2059 ¶ 109.

Otherwise, Patent Owner does not dispute Petitioner’s mapping of the recited “first input terminal,” “second input terminal,” “third input terminal,” and “output terminal.” We are persuaded by Petitioner’s mapping of these limitations to Tobita’s Figure 20 embodiment as discussed above. For these reasons, and even if the “stage circuit” of the preamble must relate to OLED displays, Petitioner establishes that Tobita teaches the subject matter of the preamble.

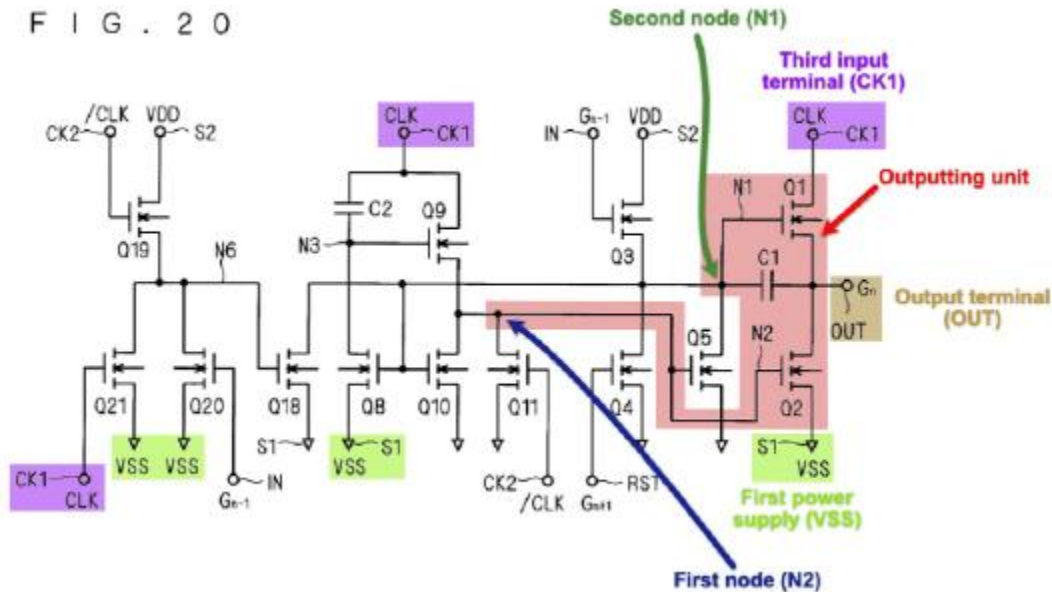
b. Limitation [1-A]

Claim 1 further recites

an outputting unit having a first node and a second node, the outputting unit to supply a voltage of a first power supply to the output terminal according to a voltage applied to the first node

and a signal of the third input terminal to the output terminal according to a voltage applied to the second node.

Ex. 1001, 9:46–51. Petitioner provides another annotated version of Tobita’s Figure 20, reproduced below, to illustrate its analysis for this limitation.



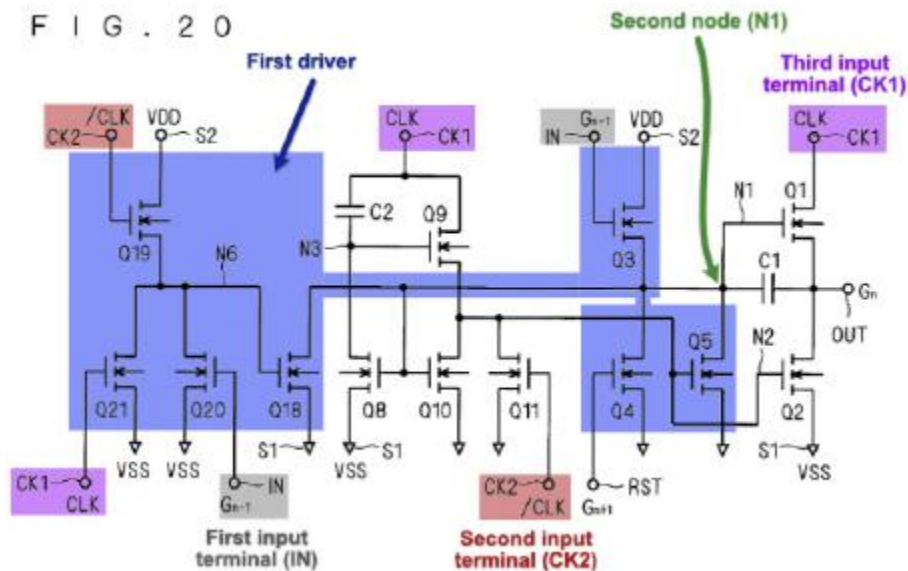
Pet. 82. Figure 20 is a circuit diagram illustrating the configuration of a unit shift register according to what Tobita calls its “eighth preferred embodiment.” Ex. 1006 ¶ 172. Petitioner has indicated its mapping of the “third input terminal” in purple, the “first power supply” in light green, the “first node” in dark blue, the “second node” in dark green, the “outputting unit” in red, and the “output terminal” in gold. Pet. 82. Specifically, Petitioner maps the recited “outputting unit” to, *inter alia*, Tobita’s transistors Q1 and Q2, as is shown in red highlighting. *Id.* at 82–83 (citing Ex. 1003 ¶ 603; Ex. 1006 ¶ 109, Fig. 20). Petitioner contends that transistors Q1 and Q2 supply either (1) a clock signal from clock terminal CK1 (i.e., the “third input terminal”), or (2) low supply voltage VSS (i.e., the “first power supply”), to output terminal OUT (i.e., the “output

terminal”). *Id.* (citing Ex. 1006 ¶ 109); *see also id.* at 83–84 (describing the output with reference to the timing diagram of Tobita’s Figure 7). Petitioner further contends that “[t]he gate electrodes of Q1 and Q2 are respectively connected to—and thus controlled by—Tobita’s node N1 (the claimed second node) and the node N2 (the claimed first node).” *Id.* at 83 (citing Ex. 1003 ¶¶ 603–604).

Patent Owner does not dispute Petitioner’s analysis of limitation [1-A] apart from its arguments discussed above. Based on the full trial record and Petitioner’s analysis discussed above, we find that Tobita teaches limitation [1-A].

c. Limitation [1-B]

Claim 1 further recites “a first driver to control the voltage of the second node in accordance with signals of the first input terminal, the second input terminal, and the third input terminal.” Ex. 1001, 9:52–54. Petitioner provides another annotated version of Tobita’s Figure 20, reproduced below, to illustrate its analysis for this limitation.



Pet. 84. Figure 20 is a circuit diagram illustrating the configuration of a unit shift register according to what Tobita calls its “eighth preferred embodiment.” Ex. 1006 ¶ 172. Petitioner has indicated its mapping of the “first input terminal” in gray, the “second input terminal” in red, the “third input terminal” in purple, the “first driver” in blue, and the “second node” in dark green. Pet. 84.

Petitioner contends that “[s]ignal G_{n-1} received at IN (Tobita’s first input terminal) controls the on/off operation of transistor Q3, which in turn contributes to control of the voltage of node N1 (the claimed second node).” Pet. 84 (citing Ex. 1006 ¶¶ 120–121, 125). Petitioner further contends that “[t]ransistors Q18–Q21—which receive signals from IN (the first input terminal), CK2 (the second input terminal), and CK1 (the third input terminal)—also control the voltage of the node N1 by, *e.g.*, bringing it to a low level.” *Id.* at 84–85 (citing Ex. 1006 ¶¶ 172, 174–177). Petitioner additionally contends that “[t]ransistors Q4 and Q5 likewise provide output to and operate to control the potential of node N1.” *Id.* at 85 (citing

Ex. 1006 ¶¶ 175–176). Petitioner concludes that “transistors Q3-Q5 and Q18-Q21 are the claimed first driver: they receive input from IN, CK2, and CK1 (the claimed first input terminal, second input terminal, and third input terminal) and collectively operate to control the voltage of node N1 (the claimed second node).” *Id.* (citing Ex. 1003 ¶¶ 614–621).

Although Patent Owner agrees with our construction that the voltage of the second node need not be determined by the first driver alone (PO Resp. 40; *see also supra* § II.C), Patent Owner nonetheless disputes that Petitioner has established that Tobita teaches the recited “control.” In essence, Patent Owner argues that the alleged control actions of Petitioner’s cited elements from Tobita are so far removed from the alleged “second node” as to render meaningless the “in accordance with” language of limitation [1-B]. PO Resp. 48. In support of this argument, Patent Owner explains that

[Tobita’s transistors] Q19, Q20, and Q21 (which Petitioner has identified as part of the “first driver”) do not control the voltage of the identified second node (N1) as this claim element requires; they instead control the voltage of a different node, N6, and the voltage on node N6 is not passed to the node N1.

Id. at 45 (Ex. 2059 ¶¶ 113–114); *see also id.* at 44–45 (further explanation of same).

Patent Owner also argues that Petitioner’s obviousness theory relies on the *absence* of an input at the third input terminal, which Petitioner identifies as Tobita’s CK1. PO Resp. 42, 45–58; PO Sur-reply 19. Patent Owner notes Dr. Foty’s explanation that a high-level signal applied to CK1 “causes transistor Q21 to turn ON, which allows VSS to be passed to the gate of transistor Q18, which turns transistor Q18 **OFF**.” PO Resp. 46

(citing Ex. 1003 ¶ 618). According to Patent Owner, “turning transistor Q18 **OFF** does not bring node N1 ‘to a low level’ as Petitioner asserts.” *Id.* (citing Ex. 2059 ¶¶ 115–119). Patent Owner also notes Tobita’s statement that “the circuit formed of the transistors Q18 to Q21 does not affect the operation of the unit shift register SR_n , of outputting the output signal G_n .” PO Resp. 42, 44–45; PO Sur-reply 19–20 (both citing Ex. 1006 ¶ 177). According to Patent Owner, this shows that “the operation of the circuit formed by transistors Q19–Q21 does not alter the output waveform relative to other embodiments that do not include these transistors.” PO Resp. 42; *see also* PO Sur-reply 19–20 (same argument).

In its Reply, Petitioner argues that Patent Owner’s argument is “nonsense” because “[w]hen transistor Q18 is off, no low-level VSS signal is supplied to node N1,” which in turn “allows the other transistors of the ‘first driver’—Q3, Q4, and Q5—to provide a high-level signal.” Pet. Reply 24 (citing Pet. 84; Ex. 1006, Fig. 6). In its Sur-reply, Patent Owner calls Petitioner’s explanation a new argument that is inconsistent with the Petition’s theories. PO Sur-reply 20.

We are persuaded by Petitioner’s contentions. Petitioner establishes that the on/off operation of transistor Q3 “contributes to control of the voltage of node N1 (the claimed second node)” based on signal G_{n-1} received at IN (the recited “first input terminal”). Pet. 84; Ex. 1003 ¶ 616; Ex. 1004 ¶¶ 120–121, 125. Petitioner also shows that Tobita’s transistors Q18–Q21 control the voltage of node N1 by “bringing it to a low level,” with transistors Q18–Q21 receiving signals from IN (the “first input terminal”), CK2 (the “second input terminal”), and CK1 (the “third input terminal”).

Pet. 84–85; Ex. 1003 ¶¶ 617, 620; Ex. 1004 ¶¶ 172, 174–177. Dr. Foty explains that, in this scenario,

the input signal (/CLK) at the second input terminal (CK2) is pulled to a voltage that causes transistor Q19 to turn on; this will pull the node labeled “N6” to the high (i.e., VDD) voltage level. This will cause transistor Q18 to turn on; when this is done, the second node (N1) is pulled to the low voltage level VSS.

Ex. 1003 ¶ 617; *see also id.* ¶ 620. Petitioner additionally shows that, at certain times, transistors Q4 and Q5 “provide output to and operate to control the potential of node N1” by providing VSS signals. Pet. 85; Ex. 1003 ¶ 621; Ex. 1004 ¶¶ 175–176.

Patent Owner’s arguments focus on a particular scenario for transistors Q18 and Q21 during the periods of clock signals CLK and /CLK that are the opposite of those cited by Petitioner.⁸ *See* PO Resp. 45–47; PO Sur-reply 19–20. In Patent Owner’s posited scenario, a high-level signal is applied at the third input terminal CK1, which turns on transistor Q21. *See* Ex. 1003 ¶ 618. In turn, a low-level voltage is provided to transistor Q18, thus turning it off and preventing low voltage level VSS from being applied to node N1 (i.e., the “second node”). *See id.* ¶¶ 617–618. This also is the situation mentioned in paragraph 177 of Tobita, which states that the output signal is unchanged. *See* Ex. 1006 ¶ 177. Yet even if this scenario with transistor Q18 turned off somehow does not evidence the recited “control,” we find that Petitioner’s primary contentions based on Tobita—with transistor Q18 turned *on* (*see* Pet. 84–85; Ex. 1003 ¶ 620)—teach the recited

⁸ Clock signals CLK and /CLK have opposite phases to each other and active periods that do not coincide. *See* Ex. 1006 ¶ 95.

“control” of limitation [1-B] by transistor Q18 in some usage conditions. This is sufficient to show obviousness. *See Unwired Planet, LLC v. Google Inc.*, 841 F.3d 995, 1002 (Fed. Cir. 2016) (“[C]ombinations of prior art that sometimes meet the claim elements are sufficient to show obviousness.”); *Hewlett-Packard Co. v. Mustek Sys., Inc.*, 340 F.3d 1314, 1326 (Fed. Cir. 2003) (“[A] prior art product that sometimes, but not always, embodies a claimed method nonetheless teaches that aspect of the invention.”). We also disagree with Patent Owner (PO Resp. 42) that a signal is absent at the third input signal in this scenario; rather, it merely reflects the opposite period of the clock signal CLK.

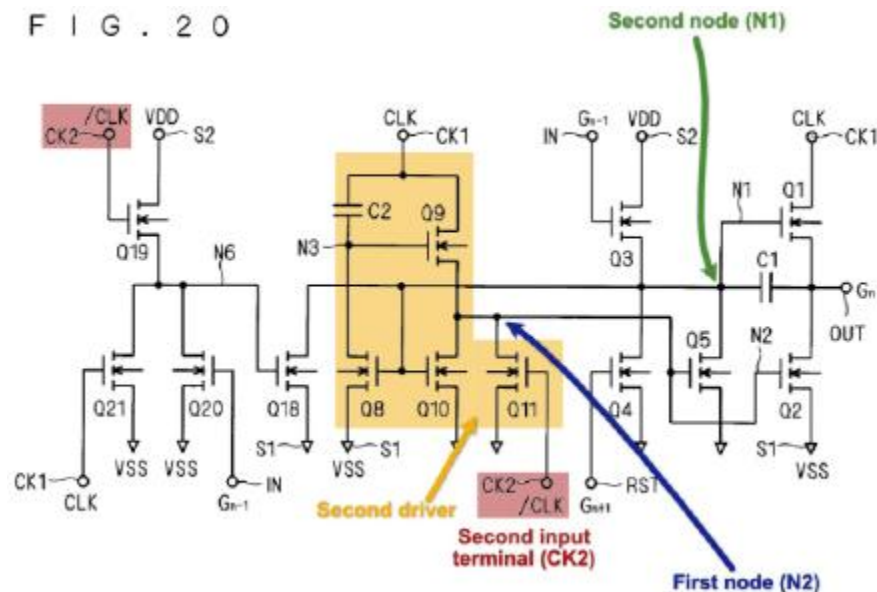
We also have considered Patent Owner’s arguments about whether Petitioner’s cited transistors from Tobita for the “first driver” sufficiently control node N1 “in accordance with” signals of the first input terminal, the second input terminal, and the third input terminal. *See* PO Resp. 48. Patent Owner’s arguments amount to criticism about how some of these transistors do not directly control node N1. But, as stated above, our construction of this limitation is premised on there being no requirement for direct control. *See supra* § II.C. In addition, Patent Owner can scarcely maintain that such indirect control is outside of the scope of limitation [1-B] given Patent Owner’s assertions before the ITC that, in the absence of a recitation about “direct” control, no such limitation should be imputed. *See* Ex. 1009, 22–23. Although Patent Owner may be correct that transistors Q19–Q21 directly control node N6 (PO Resp. 44–45), this does not detract from Petitioner’s showing that these transistors also indirectly control node N1 via their on/off control of transistor Q18. *See, e.g.*, Ex. 1003 ¶¶ 615–620. Petitioner also

has established that other parts of the “first driver,” namely transistors Q3–Q5 and Q18, directly control node N1. See Pet. 85; Ex. 1003 ¶ 622.

Based on the full trial record, we find that Petitioner has shown that Tobita teaches limitation [1-B].

d. Limitation [1-C]

Claim 1 further recites “a second driver to control the voltage of the first node in accordance with the signal of the second input terminal and the voltage of the second node.” Ex. 1001, 9:55–57. Petitioner provides another annotated version of Tobita’s Figure 20, reproduced below, to illustrate its analysis for this limitation.



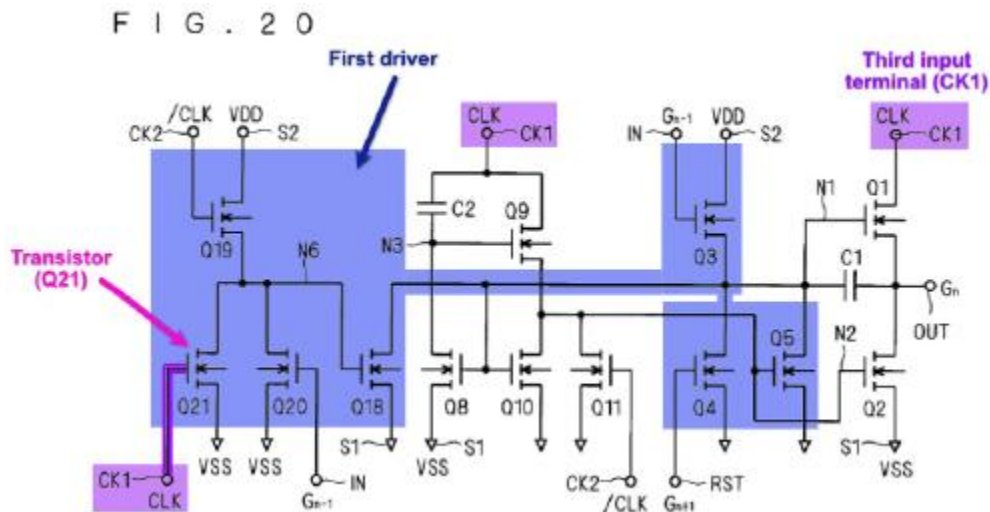
Pet. 86. Figure 20 is a circuit diagram illustrating the configuration of a unit shift register according to what Tobita calls its “eighth preferred embodiment.” Ex. 1006 ¶ 172. Petitioner has indicated its mapping of the “second driver” in yellow, the “second input terminal” in red, the “first node” in dark blue, and the “second node” in dark green. Pet. 86.

In particular, Petitioner contends that transistors Q8–Q11 constitute the recited “second driver.” Pet. 86. Petitioner explains that “[n]ode N2 (the claimed first node) is coupled to gate electrode and controls operation of transistor Q2” and that “[t]he potential of node N2 is itself controlled by the output of transistors Q8–Q11.” *Id.* (citing Ex. 1003 ¶¶ 624–625; Ex. 1006 ¶¶ 115, 120–121, 123–124, 129–132, 134, 136). Petitioner further contends that transistors “Q8 and Q10 have their gates connected to and are controlled by node N1 (the claimed second node)” and that “[t]ransistor Q11 is controlled by the /CLK signal supplied to CK2 (the second input terminal).” *Id.* (citing Ex. 1003 ¶¶ 626–630; Ex. 1006 ¶¶ 115, 120–121, 123–124, 129–132, 134, 136).

Patent Owner does not dispute Petitioner’s analysis of limitation [1-C] apart from its arguments discussed above. Based on the full trial record and Petitioner’s analysis discussed above, we find that Tobita teaches limitation [1-C].

e. Limitation [1-D]

Claim 1 further recites “the signal of the third input terminal directly controls an on/off operation of a transistor, the transistor included in the first driver.” Ex. 1001, 9:58–60. Petitioner provides another annotated version of Tobita’s Figure 20, reproduced below, to illustrate its analysis for this limitation.



Pet. 87. Figure 20 is a circuit diagram illustrating the configuration of a unit shift register according to what Tobita calls its “eighth preferred embodiment.” Ex. 1006 ¶ 172. Petitioner has indicated its mapping of the “third input terminal” in purple and the “first driver” in blue. Pet. 87. Petitioner also has indicated transistor Q21 in red. *Id.* Petitioner contends that “the gate of transistor Q21 (part of Tobita’s first driver) is coupled to [and] has its on/off functionality controlled by the CLK signal supplied to CK1 (the third input terminal).” *Id.* at 86–87 (citing Ex. 1003 ¶¶ 631–632; Ex. 1006 ¶¶ 86, 177, Fig. 20).

Patent Owner does not dispute Petitioner’s analysis of limitation [1-D] apart from its arguments discussed above. Based on the full trial record and Petitioner’s analysis discussed above, we find that Tobita teaches limitation [1-D].

f. Secondary Considerations of Nonobviousness

“[E]vidence rising out of the so-called ‘secondary considerations’ must always when present be considered en route to a determination of

obviousness.” *Transocean Offshore Deepwater Drilling, Inc. v. Maersk Drilling USA, Inc.*, 699 F.3d 1340, 1349 (Fed. Cir. 2012) (quoting *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 1538 (Fed. Cir. 1983)). “For objective evidence of secondary considerations to be accorded substantial weight, its proponent must establish a nexus between the evidence and the merits of the *claimed invention*.” *In re Huai-Hung Kao*, 639 F.3d 1057, 1068 (Fed. Cir. 2011) (quoting *Wyers v. Master Lock Co.*, 616 F.3d 1231, 1246 (Fed. Cir. 2010)). Patent Owner argues that “Petitioner’s obviousness theories are . . . undercut by real-world, objective evidence of non-obviousness,” including long-felt need, failure of others, and copying. PO Resp. 50–80; PO Sur-reply 21–24. Petitioner disputes that Patent Owner’s evidence substantiates nonobviousness. Pet. Reply 25–28.

(1) *Long-Felt Need*

Patent Owner argues that the inventions of the ’593 patent solved a long-felt need for “AMOLED displays suitable for mobile devices, and in turn a need for scan driver stage circuit designs that would allow for a reduction in the non-active bezel spaces (also known as ‘dead space’) around displays.” PO Resp. 50–51 (citing Ex. 2059 ¶¶ 126–137). Patent Owner associates the alleged need for narrower bezels with the need for smaller scan driver circuits given the disposition of scan driver circuits along the size bezels of a display. *Id.* at 51 (citing Ex. 2049, 2; Ex. 2050, 1). Although the ’593 patent does not mention the benefits of narrower bezels, Patent Owner argues that specific discussion of bezels is not required given that the benefits “flow from the ’593 Patent’s circuit design.” PO Sur-reply

23 n.2 (citing *In re Vamco Mach. & Tool, Inc.*, 752 F.2d 1564, 1577 n.5 (Fed. Cir. 1985)).

Patent Owner also argues that Hwan-Soo Jang, the named inventor of the '593 patent, “[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED].” PO Resp. 54

(citing Ex. 2047; Ex. 2048, 14; Ex. 2059 ¶¶ 131–132). Patent Owner notes that it “[REDACTED]

[REDACTED]” smartphone. *Id.* (citing, *inter alia*, Ex. 2044 ¶ 7; Ex. 2059 ¶ 138). As such, Patent Owner argues that

[REDACTED]

[REDACTED] by utilizing Mr. Jang’s invention. *Id.* (quoting Ex. 2048, 11); *see also* PO Sur-reply 23 (“The ’593 Patent’s combination of elements is what allowed for AMOLED displays with significantly narrowed bezels.”).

Petitioner argues that the claims of the ’593 patent “do not require AMOLED displays, mobile devices, or smaller bezels.” Pet. Reply 27.

Patent Owner has adduced some evidence of a desire for smartphone displays with narrower or no bezels. *See* Ex. 2049, 2; Ex. 2050, 1; Ex. 2059 ¶¶ 126–127. One cited article expressly pertains to AMOLED displays. *See* Ex. 2050, 1. Patent Owner also cites a contemporaneous patent application that notes how conventional scan driver circuits were associated with the problem of “dead space” around a display. *See* Ex. 2051 ¶¶ 13–14; Ex. 2059 ¶ 130. Petitioner argues only that AMOLED displays, mobile devices, and smaller bezels are not mentioned or claimed in the ’593 patent. Pet.

Reply 27. But this observation does not counteract Patent Owner’s evidence showing a long-felt need for narrower bezels. We find that Patent Owner’s evidence substantiates a long-felt need for AMOLED displays for mobile devices with narrower bezels.

The issue of whether the ’593 patent satisfied the long-felt need for AMOLED smartphone displays with narrower bezels is more tenuous. In order for us to accord weight to this secondary consideration of nonobviousness, Patent Owner must establish that “the *claimed invention* satisfied a long felt need.” *Sjolund v. Musland*, 847 F.2d 1573, 1582 (Fed. Cir. 1988). Patent Owner adduces evidence that implementing its claimed stage circuit led to a REDACTED reduction in dead space (Ex. 2048, 14; Ex. 2059 ¶ 131), and one of Patent Owner’s cited articles associates narrower bezels for AMOLED smartphone displays with smaller scan drivers. *See* Ex. 2050, 1. As noted by Petitioner, however, the claims of the ’593 patent do not mention AMOLED displays, mobile devices, or smaller bezels. Pet. Reply 27. We are mindful that objective evidence of nonobviousness fails where it is not “commensurate in scope with the claims which the evidence is offered to support.” *Therasense, Inc. v. Becton, Dickinson & Co.*, 593 F.3d 1325, 1336 (Fed. Cir. 2010) (quoting *In re Grasselli*, 713 F.2d 731, 743 (Fed. Cir. 1983)). We find this case similar to *MeadWestVaco Corp. v. Rexam Beauty & Closures, Inc.*, 731 F.3d 1258, 1264–65 (Fed. Cir. 2013). In that case, the Federal Circuit determined that the trial court erred in crediting objective evidence of nonobviousness for “fragrance-specific uses” when the claims were directed to a dispenser assembly that was “not fragrance-specific.” *Id.* Here, the proffered objective evidence pertains to bezels for mobile devices with AMOLED displays (as defined by Patent Owner; *see* PO Resp. 50–51),

but claim 1 is not specific to AMOLED displays, mobile devices, or bezels. Given that Patent Owner's proffered evidence is not commensurate in scope with claim 1, we find that Patent Owner's evidence does not establish that the invention of claim 1 satisfied the need annunciated by Patent Owner.

Thus, we accord Patent Owner's evidence of a long-felt need little weight.

(2) *Failure of Others*

Patent Owner argues that others in the industry failed to satisfy the demand for AMOLED displays with narrower bezels. PO Resp. 51–53. Patent Owner notes that the '593 patent “discusses the problem of ‘conventional stage circuits’ which used ‘a plurality of transistors, e.g., at least ten transistors’ that led to process yield deterioration, stability reduction, and greater circuit complexity.” *Id.* at 51 (quoting Ex. 1001, 9:12–26). According to Patent Owner, the stage circuits in Kimura and Tobita are representative of “[t]he wide-ranging efforts by others to develop alternative stage circuits, without success, [which] supports non-obviousness.” *Id.* at 52 (citing Ex. 2059 ¶ 133). Patent Owner also argues that continuing research after the '593 patent by Petitioner BOE and Hefei BOE “failed to result in successful scan driver stage circuit structures” because they used three or more clock signals and numerous transistors. *Id.* at 52–53 (citing Ex. 2052, Fig. 3; Ex. 2053, Fig. 4; Ex. 2059 ¶¶ 134–136).

Petitioner relies on the same argument discussed above, i.e., that the claims do not require AMOLED displays, mobile devices, or smaller bezels. Pet. Reply 27. Petitioner also argues that Patent Owner overstates the importance of using fewer transistors in a scan driver circuit given that

Patent Owner filed patent applications referencing drivers with more than 20 transistors years after the '593 patent was filed. *Id.* (citing Ex. 1027, Fig. 4; Ex. 1028, Fig. 4). Petitioner also argues that the Shin reference, which is in the prior art, met the need for narrower bezels with its disclosed “shift register for an OLED display that employs fewer transistors (and thus occupies less space) and fewer input signals than the '593 patent.” *Id.*

In its Sur-reply, Patent Owner argues that “Petitioner purports to find evidence of *certain limitations* in Shin, but no prior art disclosure provided the benefits that result from the claimed inventions’ combination of elements.” PO Sur-reply 23 (citing Pet. Reply 27–28).

For similar reasons to those discussed above regarding long-felt need, we find that Patent Owner’s evidence of unsuccessful attempts by others is not commensurate with the scope of claim 1. In particular, Patent Owner’s “evidence does not suggest that these prior attempts failed because the devices lacked the claimed features.” *Ormco Corp. v. Align Tech., Inc.*, 463 F.3d 1299, 1313 (Fed. Cir. 2006). This is especially true given that claim 1 does not recite a limit on the number of transistors or clock signals in the claimed stage circuit, so we do not credit Patent Owner’s evidence of stage circuits with more transistors or clock signals as evidence of failure. Nor do the challenged claims recite limitations directed to AMOLED displays, mobile devices, or smaller bezels. As such, any alleged failure to create a mobile device with an AMOLED display having a smaller bezel is not creditable evidence. *See Sjölund*, 847 F.2d at 1582 (limiting objective evidence to situations where “the *claimed invention* . . . solved problems where others had failed”). Thus, we accord Patent Owner’s evidence of

unsuccessful attempts by others little weight.

(3) *Copying*

“Copying requires duplication of features of the patentee’s work based on access to that work, lest all infringement be mistakenly treated as copying.” *Institut Pasteur & Universite Pierre et Marie Curie v. Focarino*, 738 F.3d 1337, 1347–48 (Fed. Cir. 2013) (citing *Iron Grip Barbell Co. v. USA Sports, Inc.*, 392 F.3d 1317, 1325 (Fed. Cir. 2004)); *see also Wyers*, 616 F.3d at 1246 (stating that copying requires “access to the patented product combined with substantial similarity to the patented product”).

Patent Owner argues that vendors of replacement AMOLED displays copied the design of Patent Owner’s scan driver stage circuits that embody the patented inventions.⁹ PO Resp. 54–58. In support of this argument, Patent Owner puts forth a claim chart evidencing a direct nexus between the claims of the ’593 patent and the display for the Samsung Galaxy S22 Ultra smartphone. *Id.* at 58–79. The same claim chart includes Patent Owner’s analysis of the how the Mengtor replacement AMOLED display practices the challenged claims. *Id.* Patent Owner calls the Mengtor display’s stage circuit “representative of the circuits used in all of the replacement display

⁹ Patent Owner’s copying allegations encompass replacement AMOLED displays from Petitioner Mianyang BOE Optoelectronics Technology Co., Ltd. (“Mianyang BOE”), as well as MobileSentry, Mobile Defenders, LLC, Injured Gadgets, LLC, Group Vertical, LLC, Fixez.com, Repairs Universe, LLC, SEGMobile.com, Sourcelly Plus LLC, eTech Parts, LLC, Parts4Cells, Inc., Wholesale Gadget Parts, Inc., Captain Mobile Parts, Inc., DFW Cellphone and Parts, Phone LCD Parts LLC, Parts4LCD, Mengtor Inc., and Gadgetfix Corp. *See* PO Resp. 55–58; Ex. 2059 ¶¶ 139–145.

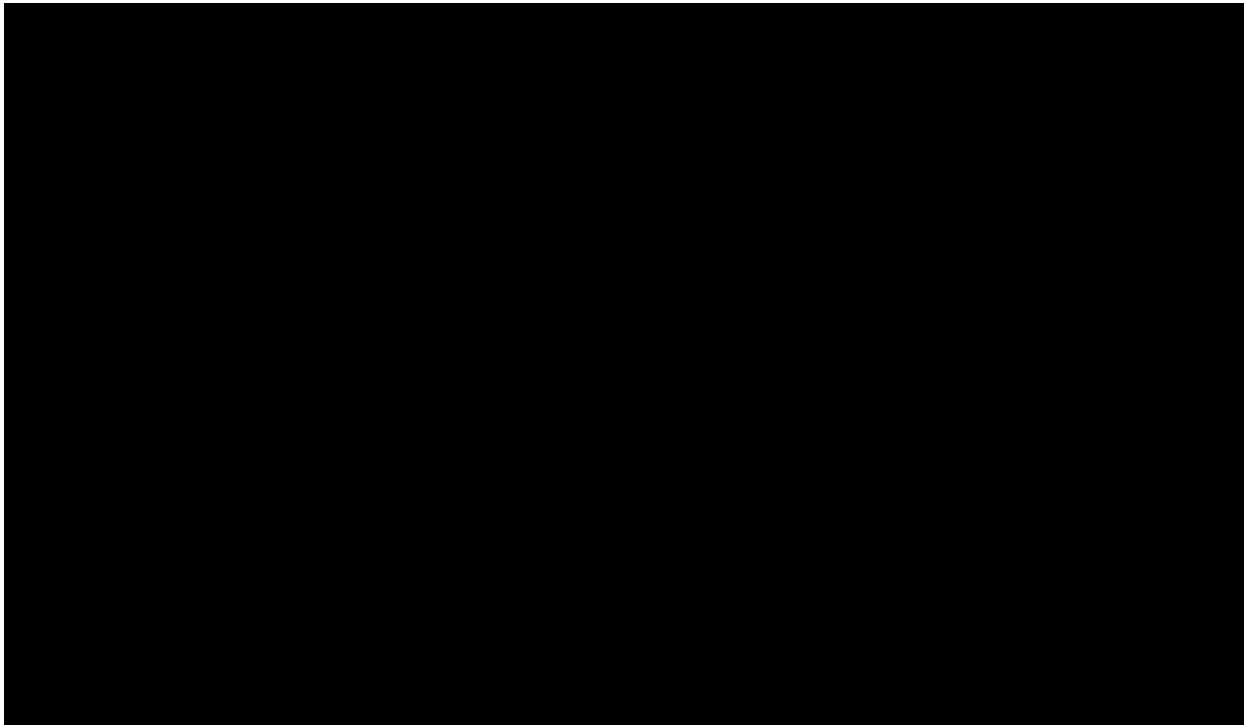
products” that Patent Owner accuses of copying. *Id.* at 55–58 & n.4. Patent Owner also argues that the replacement displays “are so similar to those of [Patent Owner], down to their physical layouts and shapes of circuit elements, that they show copying.” *Id.* at 56 (citing Ex. 2059 ¶¶ 142–144). Patent Owner additionally reproduces side-by-side teardown images of the stage circuits from the Galaxy S22 ULTRA smartphone display and from the replacement displays to show their similarity. *See id.* at 55–57.

Petitioner disputes Patent Owner’s evidence of copying to the extent it merely “point[s] to superficial similarity between its product and that of others.” Pet. Reply 27–28 (citing *Liqwd, Inc. v. L’Oreal USA, Inc.*, 941 F.3d 1133, 1137 (Fed. Cir. 2019)).

We start by assessing the issue of nexus. Patent Owner puts forth evidence of a direct nexus between the challenged claims of the ’593 patent and the display for the Samsung Galaxy S22 Ultra smartphone, which is produced by Patent Owner. PO Resp. 60–80. Patent Owner cites testimony from Dr. Wolfe “explain[ing] that the AMOLED display used in the Galaxy S22 ULTRA product practices all challenged claims.” *Id.* at 60 (citing Ex. 2044 ¶¶ 3–9; Exs. 2057–2058; Ex. 2059 ¶¶ 148–151). In particular, Dr. Wolfe created a claim chart (Ex. 2057) mapping the challenged claims to the AMOLED display in the Galaxy S22 ULTRA smartphone based on teardown photographs (Ex. 2024) obtained from a Galaxy S22 ULTRA sample by Adam Fontecchio, Ph.D. (see Ex. 2043 ¶¶ 2–3) and [REDACTED] [REDACTED] (Ex. 2058). Ex. 2059 ¶ 148. Patent Owner also has reproduced portions of Dr. Wolfe’s claim chart in its Response. PO Resp. 62–79.

Petitioner argues that “Patent Owner contradicts itself when trying to show that its products satisfy the claims.” Pet. Reply 26. Specifically, Petitioner alleges an inconsistency between Patent Owner’s mapping to the Galaxy S22 ULTRA smartphone and Patent Owner’s arguments against the Tobita obviousness ground. *Id.* Petitioner mistakenly keys its argument to an equivalent circuit diagram that Patent Owner associates with the Mengtor replacement display rather than the Galaxy S22 ULTRA smartphone. *Compare id.*, with Ex. 2046, 6 (Mengtor claim chart). Notwithstanding, we understand and consider Petitioner’s argument based on similar shading in the correct circuit diagram. *See* Ex. 2057, 3 (Galaxy S22 ULTRA smartphone claim chart).

An annotated circuit diagram for the Galaxy S22 ULTRA smartphone display from Dr. Wolfe’s claim chart is reproduced below.



The annotated circuit diagram above depicts Patent Owner’s AMOLED display in the Samsung Galaxy S22 Ultra smartphone. *See* Ex. 2057, 2–3. According to Dr. Wolfe,



Id. at 3.

Petitioner argues that Patent Owner has mapped the recited “first driver” to transistors T1, T2, and T3, “[b]ut it then ambiguously identifies **both** the blue and green circuit paths as the claimed ‘second node.’” Pet.

Reply 26. According to Petitioner, this creates an inconsistency:

If the green path is the claimed “second node,” then Patent Owner has contradicted its Tobita arguments (transistors T1-T3 control the green path’s voltage only indirectly through transistor T8). If the blue path is the claimed “second node,” then Patent Owner creates yet another contra[di]ction: the “output terminal” signal is no longer supplied “according to the voltage applied to the second node.” Instead, the second node voltage only indirectly impacts the output (transistor T8 exercises direct control). Patent Owner does not identify which theory it is pursuing, let alone explain the discrepancies between these theories and the other arguments it makes.

Id. at 26–27 (citing Ex. 1025 ¶¶ 98–105).

In its Sur-reply, Patent Owner asserts there is a “material distinction” in its arguments. PO Sur-reply 21. Specifically, Patent Owner argues that, in the Samsung Galaxy S22 Ultra smartphone display, “the first driver provides a signal that simply passes through a transistor to control a node.”

Id. Patent Owner contrasts this arrangement with Tobita’s stage circuit,

where “the identified first driver provides a signal (high or low) that controls a different node (N6) to cause a transistor (Q18) to turn on or off, which may then allow a *different* signal (VSS) to be provided to a node (N1).” *Id.* (citing Ex. 2059 ¶¶ 113–114).

We find that the alleged inconsistency does not undermine Patent Owner’s nexus analysis. As discussed above, claim 1 does not require direct control (*see supra* §§ II.C.1), so this argument does not affect the instant nexus analysis. Given this understanding, we credit Patent Owner’s analysis based on the green region being the “second node,” an alternative presented by Patent Owner (*see* PO Resp. 63; Ex. 2057, 3) and a mapping with which Dr. Foty agrees (*see* Ex. 1025 ¶ 104).

Otherwise, Petitioner does not dispute Patent Owner’s and Dr. Wolfe’s analysis of a direct nexus to the Galaxy S22 ULTRA smartphone display. Accordingly, we credit Patent Owner’s evidence of nexus to the Galaxy S22 ULTRA smartphone display. *See, e.g.*, Ex. 2057; Ex. 2059 ¶¶ 148–151. Patent Owner also has put forth undisputed testimony, which we credit, that [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED].” Ex. 2044 ¶ 7.

Next, we turn to Patent Owner’s evidence of copying. Patent Owner’s best evidence of copying pertains to the Mengtor replacement display, so we start by analyzing that product. Dr. Wolfe created a claim chart (Ex. 2046) showing how the Mengtor display practices the challenged claims based on teardown images (Ex. 2026) created by Dr. Silzars (Ex. 2042 ¶ 3). Ex. 2059

¶ 144. Patent Owner also has reproduced portions of Dr. Wolfe’s claim chart in its Response. PO Resp. 62–79. Dr. Silzars testifies that he purchased the Mengtor replacement display, which was sold as “OLED Screen Digitizer Assembly With Frame for iPhone 12 / 12 Pro (High Quality) – Black,” from Mengtor’s online store. Ex. 2026, 2; Ex. 2042 ¶ 3. Patent Owner also cites a comparison of side-by-side teardown photos between, *inter alia*, the Galaxy S22 Ultra display and the Mengtor display in support of its contention that the Mengtor display is “so similar to those of [Patent Owner], down to [its] physical layouts and shapes of circuit elements, that [it] show[s] copying.” PO Resp. 56–58 (citing Ex. 2059 ¶¶ 142–144). Dr. Wolfe likewise testifies that

[t]hese scan driver stage circuit teardown photographs are so similar, including for example in the physical layout topology and geometry of the metal wirings, that the only reasonable inference one could draw is that someone with access to [Patent Owner’s] AMOLED display products or other confidential technical information determined to replicate [Patent Owner’s] scan driver stage circuits in the replacement display products. Ex. 2059 ¶ 143; *see also id.* ¶ 144 (Dr. Wolfe testifying that “[t]he scan driver stage circuit[] used in the Mengtor product is strikingly similar to the one used in [Patent Owner’s] AMOLED display used in the Galaxy S22 ULTRA Product”).

Petitioner does not dispute that the Mengtor product practices the challenged claims. Petitioner argues only that Patent Owner has shown superficial similarity between Patent Owner’s product and the Mengtor product. Pet. Reply 27–28.

Dr. Wolfe’s claim chart analysis persuasively shows that the Mengtor replacement display practices the challenged claims. *See* Ex. 2046. We

further find substantial similarity between the stage circuit in the Mengtor product and the stage circuit in the Galaxy S22 ULTRA smartphone display. We base this on both Patent Owner’s side-by-side claim chart in Patent Owner’s Response (PO Resp. 61–79) and Dr. Wolfe’s testimony (Ex. 2059 ¶ 143). Although the Mengtor product is sold as a replacement for an iPhone display (Ex. 2042 ¶ 3), Mr. Lee testifies that [REDACTED] [REDACTED] [REDACTED].” Ex. 2044 ¶ 7. Mr. Lee’s testimony is undisputed, so we find that the [REDACTED] [REDACTED]. We also infer that Mengtor had access to Patent Owner’s patented products given that Mengtor marketed its display as a replacement part for the iPhone. *See* Ex. 2026, 2; Ex. 2042 ¶ 3. For these reasons, we accord substantial weight to Patent Owner’s evidence of copying as to the Mengtor product.

We now consider Patent Owner’s evidence of copying as to replacement displays other than Mengtor. Patent Owner relies only on side-by-side comparisons of a single teardown photograph for each display next to a teardown photograph of the Samsung Galaxy S22 ULTRA smartphone display. PO Resp. 55–58; Ex. 2059 ¶¶ 140–143. Again, Patent Owner argues that these other replacement displays are so similar that they show copying. *See* PO Resp. 56; Ex. 2059 ¶ 143. Yet we agree with Petitioner (Pet. Reply 27–28) that Patent Owner’s cited evidence—a single photograph for each display—is too superficial to draw reliable conclusions. The record is devoid of analysis or explanation from Patent Owner and Dr. Wolfe as to the significance of these photographs. Moreover, given that these

replacement circuits arise from numerous different entities, we also do not credit Dr. Wolfe’s conclusory and unsupported statement that “[t]he Mengtor product’s scan driver stage circuit *is representative* of the scan driver stage circuits used in the other replacement display products.”

Ex. 2059 ¶ 144 (emphasis added). Finally, Patent Owner makes no appreciable attempt to show that the other replacement displays practice the challenged claims. For these reasons, we accord little weight to Patent Owner’s evidence of copying for replacement displays other than Mengtor.

(4) *Conclusion Regarding Secondary Considerations of Nonobviousness*

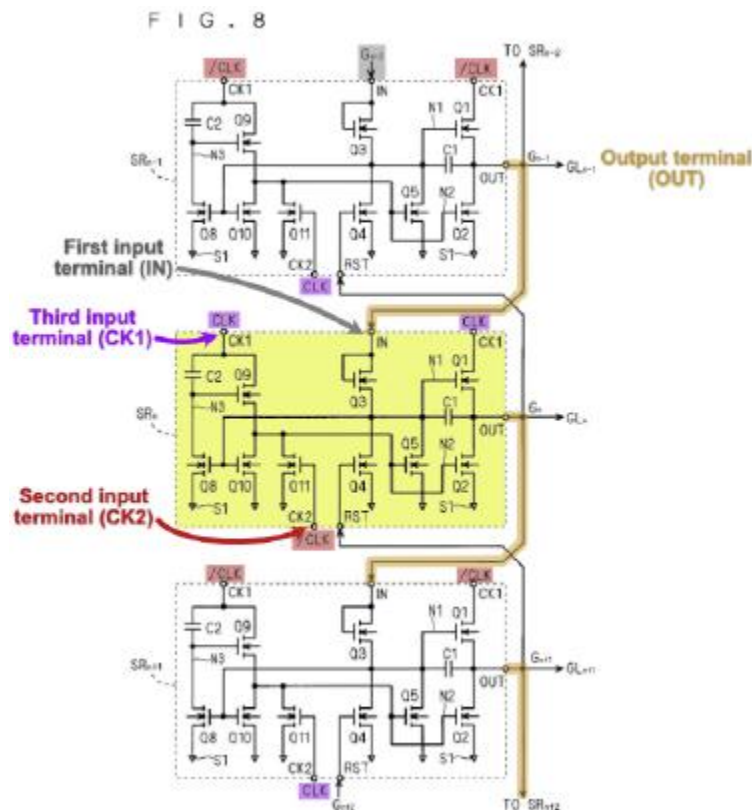
We have accorded substantial weight to Patent Owner’s evidence of copying as to the Mengtor replacement display. We have accorded little weight to Patent Owner’s evidence of long-felt need, failure of others, and copying as to all other replacement displays.

g. *Conclusion Regarding Claim 1*

Petitioner has shown persuasively that Tobita teaches all limitations of claim 1 in light of the knowledge of one of ordinary skill in the art. Although we accord substantial weight to Patent Owner’s evidence of copying as to the Mengtor replacement display, we find that this evidence, and Patent Owner’s other evidence of secondary considerations, does not outweigh Petitioner’s persuasive obviousness showing under the other *Graham* factors. Thus, we determine that Petitioner has shown by a preponderance of the evidence that the subject matter of claim 1 would have been obvious over Tobita.

3. *Claim 2*

Claim 2 depends from claim 1 and further recites that “the first input terminal receives an output signal of a previous stage circuit or a start signal,” “the second input terminal receives a first clock signal,” and “the third input terminal receives a second clock signal.” Ex. 1001, 9:61–67. Petitioner cites Tobita’s teaching of a shift register having multiple stages. Pet. 87–88 (citing Ex. 1006 ¶ 117, Fig. 8). Petitioner provides an annotated version of Tobita’s Figure 8, reproduced below, to illustrate its analysis for claim 2.



Id. at 88. Figure 8 is a circuit diagram showing the connection between the unit shift registers. Ex. 1006 ¶ 27. Petitioner indicates its mapping of the “first input terminal” in gray, the “second input terminal” in red, the “third input terminal” in purple, and the “output terminal” in gold. Pet. 88.

Petitioner contends that Tobita's "terminal IN (the first input terminal) of stage SR_n receives output signal G_{n-1} of the previous stage circuit SR_{n-1} (that stage's output signal)." *Id.* (citing Ex. 1006 ¶ 117, Fig. 8). Petitioner also contends that Tobita's "[t]erminal CK2 (the second input terminal) of SR_n receives /CLK (the claimed first clock signal), and terminal CK1 (the third input terminal) of SR_n receives CLK (the claimed second clock signal)." *Id.*

Patent Owner relies on the same arguments discussed above for claim 1. We are persuaded by Petitioner's analysis as indicated in the annotated version of Tobita's Figure 8 above. In particular, Petitioner has established that Tobita's terminal IN (i.e., the "first input terminal") at stage circuit SR_n receives output signal G_{n-1} from the previous stage circuit SR_{n-1} . *See, e.g.*, Ex. 1006 ¶ 117, Fig. 8. Our analysis regarding secondary considerations of nonobviousness discussed above for claim 1 applies equally to this claim (*see supra* § II.G.2.f.), and we find that Patent Owner's evidence of secondary considerations does not outweigh Petitioner's persuasive obviousness showing for claim 2 under the other *Graham* factors. Thus, we determine that Petitioner has shown by a preponderance of the evidence that the subject matter of claim 2 would have been obvious over Tobita.

4. Claim 15

a. Preamble ([15-PRE])

As discussed above, we determine the preamble of claim 15 to be non-limiting. *See supra* § II.C.2. Thus, we need not address the preamble in order to assess Petitioner's obviousness contentions.

b. Limitation [15-A]

Claim 15 further recites “pixels positioned in regions partitioned by scan lines and data lines.” Ex. 1001, 11:10–11. Petitioner cites Tobita’s teaching of “pixels . . . arrayed in a matrix” with gate/scanning lines connected to rows of pixels and data lines connected to columns of pixels. Pet. 89 (citing Ex. 1006 ¶¶ 4, 59). Petitioner also cites Figure 1 of Tobita for teaching that “[t]he scan lines and data lines are located between and separate the pixels.” *Id.* at 89–90 (citing Ex. 1006 ¶¶ 59–60, Fig. 1).

Patent Owner does not dispute Petitioner’s analysis of limitation [15-A]. Based on the full trial record, we find that Tobita teaches limitation [15-A]. *See, e.g.*, Ex. 1006 ¶¶ 4, 59–60, Fig. 1.

c. Limitation [15-B]

Claim 15 further recites “a data driver for supplying data signals to the pixels through the data lines.” Ex. 1001, 11:12–13. Petitioner cites Tobita’s source driver 40, which “output[s] display voltages set stepwise by a display signal SIG . . . to the data lines DL.” Pet. 90 (quoting Ex. 1006 ¶ 62) (citing Ex. 1006 ¶ 71). Petitioner contends that “[t]he displayed image is based on this signal.” *Id.* at 90–91 (citing Ex. 1006 ¶¶ 62, 71, Fig. 1).

Patent Owner does not dispute Petitioner’s analysis of limitation [15-B]. Based on the full trial record, we find that Tobita teaches limitation [15-B]. *See, e.g.*, Ex. 1006 ¶¶ 62, 71, Fig. 1.

d. Limitation [15-C]

Claim 15 further recites

a scan driver for supplying scan signals to the pixels through the scan lines, the scan driver including stage circuits coupled to the scan lines, each of the stage circuits generating a corresponding scan signal of the scan signals and having a first input terminal, a second input terminal, a third input terminal, and an output terminal.

Ex. 1001, 11:14–20. Petitioner cites Tobita’s gate-line/scanning-line driving circuit 30, which “sequentially drives the gate lines . . . in synchronization with the scanning cycle.” Pet. 91–92 (quoting Ex. 1006 ¶ 71) (citing Ex. 1006 ¶¶ 58, 61, Fig. 1). Petitioner contends that the scanning-line driving circuit includes stages of “cascade-connected unit shift registers,” with each unit shift register receiving “input from IN (the first input terminal), CK2 (the second input terminal), and CK1 (the third input terminal), and output[ting] a corresponding scan signal G_n to OUT (the output terminal).” *Id.* at 92 (citing Ex. 1006 ¶ 167); *see also supra* § II.G.2.a (similar analysis for limitation [1-A]).

Patent Owner does not dispute Petitioner’s analysis of limitation [15-C]. Based on the full trial record, we find that Tobita teaches limitation [15-C]. *See, e.g.*, Ex. 1006 ¶¶ 58, 61, 71, 167, Fig. 1; *supra* § II.G.2.a.

e. Remaining Limitations

The remaining limitations of claim 15 are identical to the limitations of claim 1. *Compare* Ex. 1001, 11:21–36, *with id.* at 10:43–67. Petitioner relies on the same analysis discussed above for claim 1. Patent Owner relies on the same arguments discussed above for claim 1. We are persuaded by

Petitioner’s analysis for the same reasons discussed above. *See supra* § II.G.2.b–e.

f. Secondary Considerations of Nonobviousness

Although the preamble of claim 15 recites an “organic light emitting display,” we have determined that the preamble is non-limiting. *See supra* § II.C.2. Thus, the preamble of claim 15 does not materially change our analysis of secondary considerations discussed above in claim 1. And, even if the preamble of claim 15 were limiting, we note that Patent Owner’s assertions of long-felt need and failure of others are tied to AMOLED displays (*see* PO Resp. 50–52), whereas the preamble of claim 15 is not directed to active-matrix displays. Having considered these issues, we find that our analysis regarding secondary considerations of nonobviousness discussed above for claim 1 applies equally to this claim. *See supra* § II.G.2.f.

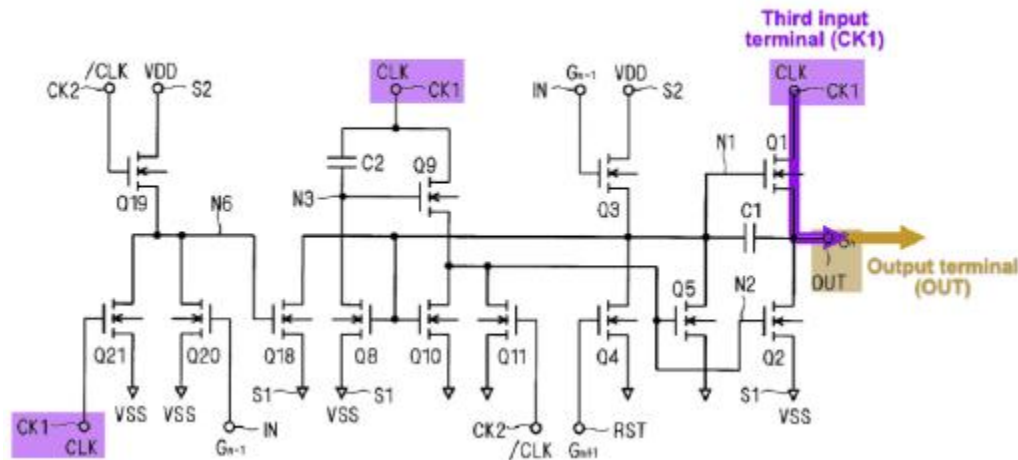
g. Conclusion Regarding Claim 15

Petitioner has shown persuasively that Tobita teaches all limitations of claim 15 in light of the knowledge of one of ordinary skill in the art. Although we accord substantial weight to Patent Owner’s evidence of copying as to the Mengtor replacement display, we find that this evidence and Patent Owner’s other evidence of secondary considerations do not outweigh Petitioner’s persuasive obviousness showing under the other *Graham* factors. Thus, we determine that Petitioner has shown by a preponderance of the evidence that the subject matter of claim 15 would have been obvious over Tobita.

5. *Claim 16*

Claim 16 depends from claim 15 and recites that “a clock signal supplied to the third input terminal is used as the scan signal.” Ex. 1001, 11:37–39. Petitioner contends that “Tobita’s circuit supplies the CLK signal from terminal CK1 (the third input terminal) to OUT for use as gate line / scan signal G_n .” Pet. 93 (citing Ex. 1003 ¶¶ 682–689; Ex. 1006 ¶¶ 109, 117, 122, 125–126, Fig. 20). Petitioner provides an annotated version of Tobita’s Figure 20, reproduced below, to illustrate its analysis for this limitation.

F I G . 2 0



Id. Figure 20 is a circuit diagram illustrating the configuration of a unit shift register according to what Tobita calls its “eighth preferred embodiment.” Ex. 1006 ¶ 172. Petitioner has indicated its mapping of the “third input terminal” in purple and the “output terminal” in gold. Pet. 93.

Patent Owner relies on the same arguments discussed above for claim 1. We are persuaded that when transistor Q1 is turned on, the third input terminal (CK1) is connected to the output terminal (OUT) such that the clock signal of the third input terminal (CLK) is outputted as the scan signal. *See, e.g.*, Ex. 1003 ¶¶ 682–689; Ex. 1006 ¶¶ 109, 117, 122, 125–126,

Fig. 20. Our analysis regarding secondary considerations of nonobviousness discussed above for claim 1 applies equally to this claim (*see supra* § II.G.2.f.), and we find that Patent Owner’s evidence of secondary considerations does not outweigh Petitioner’s persuasive obviousness showing for claim 2 under the other *Graham* factors. Thus, we determine that Petitioner has shown by a preponderance of the evidence that the subject matter of claim 16 would have been obvious over Tobita.

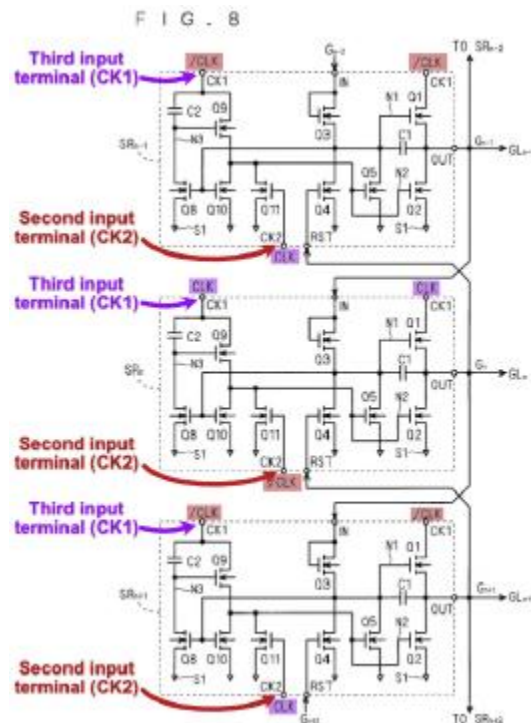
6. *Claim 17*

Claim 17 depends from claim 16 and recites a limitation similar to a limitation in claim 2. *Compare* Ex. 1001, 11:40–42, *with id.* at 9:62–63. Petitioner relies on the same analysis from claim 2. Pet. 94. Patent Owner relies on the same arguments discussed above for claim 1. We are persuaded by Petitioner’s analysis for the same reasons discussed above in our analysis of claim 2. *See supra* § II.G.3. Our analysis regarding secondary considerations of nonobviousness discussed above for claim 1 applies equally to this claim (*see supra* § II.G.2.f.), and we find that Patent Owner’s evidence of secondary considerations does not outweigh Petitioner’s persuasive obviousness showing for claim 17 under the other *Graham* factors. Thus, we determine that Petitioner has shown by a preponderance of the evidence that the subject matter of claim 17 would have been obvious over Tobita.

7. *Claim 18*

Claim 18 depends from claim 17 and recites that “second input terminals of odd stage circuits receive a first clock signal and third input

terminals of odd stage circuits receive a second clock signal,” and that “second input terminals of even stage circuits receive the second clock signal and third input terminals of even stage circuits receive the first clock signal.” Ex. 1001, 11:43–50. Petitioner contends that “in Tobita’s odd stage circuits (*e.g.*, SR_n), the second input terminals (CK2) receive a first clock signal (/CLK) and the third input terminals (CK1) receive a second clock signal (CLK),” whereas “[t]he even stage circuits (*e.g.*, SR_{n-1} , SR_{n+1}) are reversed.” Pet. 94–95 (citing Ex. 1003 ¶¶ 694–700; Ex. 1006, Fig. 8). Petitioner provides an annotated version of Tobita’s Figure 8, reproduced below, to illustrate its analysis for this limitation.



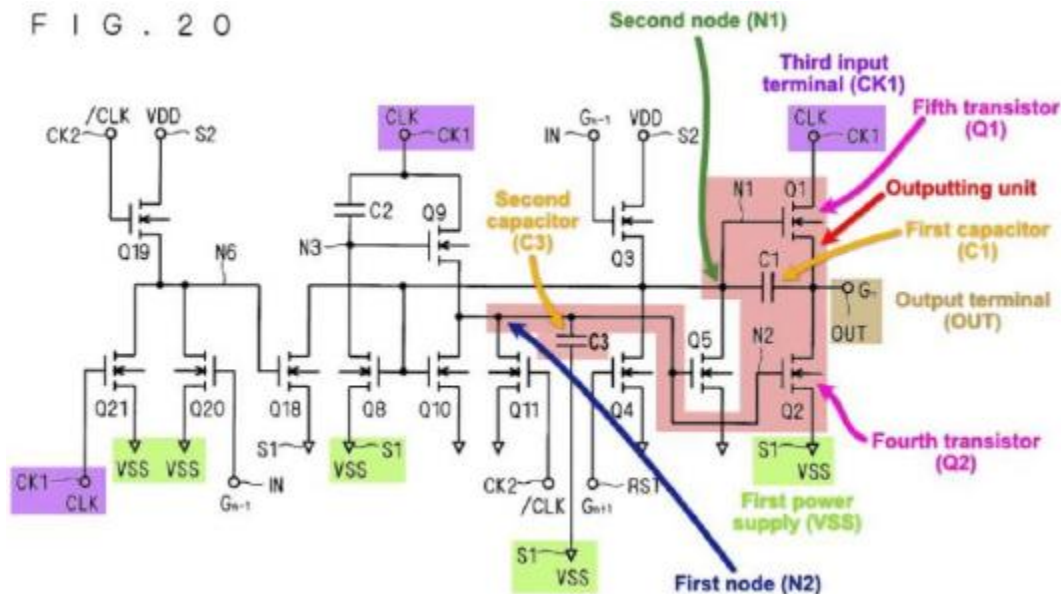
Patent Owner relies on the same arguments discussed above for claim 1. We are persuaded by Petitioner’s analysis as indicated in Petitioner’s annotated version of Tobita’s Figure 8 above. *See, e.g.*, Ex. 1003 ¶¶ 694–700; Ex. 1006, Fig. 8. Our analysis regarding secondary considerations of nonobviousness discussed above for claim 1 applies equally to this claim (*see supra* § II.G.2.f.), and we find that Patent Owner’s evidence of secondary considerations does not outweigh Petitioner’s persuasive obviousness showing for claim 18 under the other *Graham* factors. Thus, we determine that Petitioner has shown by a preponderance of the evidence that the subject matter of claim 18 would have been obvious over Tobita.

H. Obviousness Grounds Based on Tobita and Jeong

Petitioner contends that the subject matter of claims 7 and 21 would have been obvious over the combination of Tobita and Jeong. Pet. 95–98; Pet. Reply 25. Patent Owner disputes Petitioner’s contentions. PO Resp. 49–50.

Petitioner notes that claims 7 and 21 both include “additional limitations requiring that the ‘outputting unit’ include a ‘fourth transistor,’ ‘fifth transistor,’ ‘first capacitor,’ and ‘second capacitor’ connected in particular ways.” Pet. 95. Petitioner contends that “Tobita’s outputting unit contains all the required components except the second capacitor.” *Id.* at 95–96. As such, Petitioner relies on Jeong for teaching the “second capacitor.” *Id.* at 97 (citing Ex. 1007 ¶ 57). Petitioner provides an annotated and modified version of Tobita’s Figure 20, reproduced below, to illustrate its analysis.

F I G . 2 0



Id. Figure 20 is a circuit diagram illustrating the configuration of a unit shift register according to what Tobita calls its “eighth preferred embodiment.”

Ex. 1006 ¶ 172. Petitioner has indicated its mapping of the “fourth transistor” (Q2) in pink, the “fifth transistor” (Q1) in pink, the “first capacitor” (C1) in yellow. Pet. 96–97. Based on Jeong’s teachings, Petitioner has added a “second capacitor” (C3) in yellow to Tobita’s Figure 20 circuit. *Id.*

Petitioner contends that an ordinarily skilled artisan would have recognized that Tobita’s “node N2 only has a small amount of capacitance and may not adequately maintain a fixed voltage level in the presence of perturbations in electrical charge level or when the node is electrically isolated (when Q9–Q11 are all off).” Pet. 96 (citing Ex. 1003 ¶¶ 708–713); *see also id.* at 97 (“Tobita’s circuit could experience unintended—and highly undesirable—voltage variation”). Thus, Petitioner contends that an ordinarily skilled artisan would have been motivated “[t]o avoid this and

increase the robustness of the circuit's operation" by "add[ing] a capacitor to this node as taught by Jeong." *Id.* at 96–97 (citing Ex. 1003 ¶¶ 714–721).

Patent Owner disputes Petitioner's rationale for adding a capacitor to Tobita's node N2 based on Jeong's teachings. *See* PO Resp. 49–50. Patent Owner argues that Petitioner does not identify any operational issues with the embodiment of Tobita on which it relies, instead making unsupported assertions that Tobita's circuit 'could experience' unintended 'voltage variation.'" *Id.* at 49 (quoting Pet. 97). Citing testimony from Dr. Wolfe, Patent Owner argues that an ordinarily skilled artisan "would not simply assume that there could possibly be such issues, and any generic concerns would not motivate [ordinarily skilled artisans] to add a capacitor to Tobita's circuit." *Id.* (citing Ex. 2059 ¶ 122). Patent Owner likewise notes Dr. Foty's similar testimony from a prior proceeding, which Patent Owner calls inconsistent with Dr. Foty's testimony here. *Id.* at 50 (citing Ex. 2061, 58:4–11). Patent Owner also argues that Tobita's circuit already includes capacitor C1, thus showing that "Tobita was familiar with the generalized concerns Petitioner points to," yet Tobita neither included a second capacitor nor connected it in the specific way Petitioner proposes. *Id.* (citing Ex. 1006, Fig. 20; Ex. 2059 ¶¶ 122–123). Patent Owner additionally argues that adding a capacitor is antithetical to Tobita's teachings on reducing circuit area. *Id.* at 49 (citing Ex. 1006 ¶¶ 15–17).

In its Reply, Petitioner argues that "Dr. Foty explained—and Patent Owner does not dispute—that Tobita's node N2 is electrically isolated during certain operational periods," which "leaves it vulnerable to interference." Pet. Reply 25 (citing Ex. 1003 ¶¶ 708–713; Ex. 1007 ¶ 57).

The question of whether Petitioner has established an adequate rationale for combining Jeong’s capacitor with Tobita’s circuit is a close one, particularly given that adding a capacitor to reduce a node’s voltage variation appears to be well known. *See, e.g.*, Ex. 1007 ¶ 57. On one hand, Petitioner presents unrebutted testimony from Dr. Foty establishing that Tobita’s “node N2 only has a small amount of capacitance and may not adequately maintain a fixed voltage level in the presence of perturbations in electrical charge level or when the node is electrically isolated.” *See* Pet. 96; Ex. 1003 ¶¶ 708–713. On the other hand, Patent Owner presents testimony from Dr. Wolfe noting that “Dr. Foty does not identify any operational issues with the embodiment of Tobita” and opining that an ordinarily skilled artisan would not have been motivated to add circuit elements based on “generalized concerns” given that the circuit was “specifically designed for its intended purpose.” Ex. 2059 ¶ 122. Dr. Foty also previously testified that an ordinarily skilled artisan reading a reference like Tobita “would assume that you have a functioning process, which produces good transistors, not transistors that have a failure mechanism type of leakage.” Ex. 2061, 58:4–11. Patent Owner also points out that Tobita “intentionally added a capacitor (C1) where it was needed, and did not add a capacitor where it was not.” PO Resp. 50.

On balance, we find Patent Owner’s arguments more persuasive. In particular, we note an apparent contradiction between Dr. Foty’s testimony here and his prior testimony in a different proceeding. *Compare* Ex. 1003 ¶¶ 708–713 (discussing potential problems with Tobita’s circuit), *with* Ex. 2061, 58:4–11 (testifying that an ordinarily skilled artisan would assume that a circuit was designed for its intended purpose). In light of this

contradiction, we give Dr. Wolfe’s testimony more weight and find that the premise of Petitioner’s proposed modification—generalized concerns about interference and robustness—would not have motivated an ordinarily skilled artisan to make the combination in the absence of an identified problem with Tobita’s circuit. *See* Ex. 2059 ¶ 122. Petitioner has not established that any such problem existed. Further, we find that an ordinarily skilled artisan would not have added a circuit element (and thus increased circuit area) without clear objectives or benefits. *See id.* ¶¶ 122–123; *see also* Ex. 1006 ¶ 15 (noting that capacitive elements detrimentally increase circuit area). The fact that an ordinarily skilled artisan *could* have made this modification is insufficient to show obviousness; rather, Petitioner was required to show that the artisan “*would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention.” *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015). It failed to do so persuasively.

For these reasons, we are not persuaded by Petitioner’s rationale for combining Jeong with Tobita. Accordingly, we determine that Petitioner has not shown by a preponderance of the evidence that the subject matter of claims 7 and 21 would have been obvious over the combination of Tobita and Jeong.

III. CONCLUSION¹⁰

Petitioner has shown, by a preponderance of the evidence, that the subject matter of claims 1, 2, and 15–18 of the '593 patent would have been obvious over Tobita. Petitioner has not shown, by a preponderance of the evidence, that (1) the subject matter of claims 1–8, 14–22, and 25 of the '593 patent would have been obvious over Kimura; (2) the subject matter of claims 1–6, 8, 14–20, 22, and 25 of the '593 patent would have been obvious over the combination of Shin and Sasaki; (3) the subject matter of claims 7 and 21 of the '593 patent would have been obvious over the combination of Shin, Sasaki, and Jeong; and (4) the subject matter of claims 7 and 21 of the '593 patent would have been obvious over the combination of Tobita and Jeong.

¹⁰ Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this Decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not shown Unpatentable
1–8, 14–22, 25	103(a)	Kimura		1–8, 14–22, 25
1–6, 8, 14–20, 22, 25	103(a)	Shin, Sasaki		1–6, 8, 14–20, 22, 25
7, 21	103(a)	Shin, Sasaki, Jeong		7, 21
1, 2, 15–18	103(a)	Tobita	1, 2, 15–18	
7, 21	103(a)	Tobita, Jeong		7, 21
Overall Outcome			1, 2, 15–18	3–8, 14, 19–22, 25

IV. ORDER

Accordingly, it is

ORDERED that claims 1, 2, and 15–18 of the '593 patent are unpatentable;

FURTHER ORDERED that claims 3–8, 14, 19–22, and 25 of the '593 patent are not unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to this proceeding seeking judicial review of our decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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Patent 9,330,593 B2

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