UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/204,011	10/18/2016	9471074	68354.225441	9205

86528 7590 09/28/2016

Slayden Grubert Beard PLLC
401 Congress Avenue
Suite 1900
Austin, TX 78701

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 104 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Microchip Technology Incorporated, Chandler, AZ
Huamin Zhou, Chandler, AZ;
Woowai Martin, Phoenix, AZ;
Cristian Albina, Chandler, AZ;
Fritz Schlunder, Gilbert, AZ;
Minh Le, Gilbert, AZ;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

86528 7590 06/22/2016
Slayden Grubert Beard PLLC
401 Congress Avenue
Suite 1900
Austin, TX 78701

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Todd Rosson	(Depositor's name)
/Todd Rosson/	(Signature)
September 21, 2016	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/204,011	03/11/2014	Huamin Zhou	68354.225441	9205

TITLE OF INVENTION: USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	09/22/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
ZHANG, JUE	2838	323-280000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Slayden Grubert Beard PLLC
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: MICROCHIP TECHNOLOGY INCORPORATED

(B) RESIDENCE: (CITY and STATE OR COUNTRY): CHANDLER, ARIZONA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☑ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☑ Payment by credit card. Form PTO-2038 is attached.
- ☑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 50-6736 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ☐ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ☐ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Andreas H. Grubert/ Date September 21, 2016

Typed or printed name Andreas H. Grubert Registration No. 59,143

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Electronic Patent Application Fee Transmittal

Application Number:	14204011
Filing Date:	11-Mar-2014
Title of Invention:	USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor
First Named Inventor/Applicant Name:	Huamin Zhou
Filer:	Eric M. Grabski/Todd Rosson
Attorney Docket Number:	68354.225441

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**960**

Electronic Acknowledgement Receipt	
EFS ID:	26987581
Application Number:	14204011
International Application Number:	
Confirmation Number:	9205
Title of Invention:	USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor
First Named Inventor/Applicant Name:	Huamin Zhou
Customer Number:	86528
Filer:	Eric M. Grabski/Todd Rosson
Filer Authorized By:	Eric M. Grabski
Attorney Docket Number:	68354.225441
Receipt Date:	21-SEP-2016
Filing Date:	11-MAR-2014
Time Stamp:	11:00:21
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$960
RAM confirmation Number	8535
Deposit Account	506736
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 CFR 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 CFR 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 CFR 1.19 (Document supply fees)

Charge any Additional Fees required under 37 CFR 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	Issue_Fee_225441.pdf	108123 425e7873eed560284f86fdbb11d73b24a49a421a	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	31239 15fefe608aff455b2d1a1befceb6eb48ef0b1ba5	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	139362		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/204,011	03/11/2014	Huamin Zhou	68354.225441	9205

86528 7590 08/11/2016

Slayden Grubert Beard PLLC
401 Congress Avenue
Suite 1900
Austin, TX 78701

EXAMINER	
ZHANG, JUE	

ART UNIT	PAPER NUMBER
2838	

NOTIFICATION DATE	DELIVERY MODE
08/11/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

trosson@sgbfirm.com
patent@sgbfirm.com
dallen@sgbfirm.com

Supplemental Notice of Allowability	Application No. 14/204,011	Applicant(s) ZHOU ET AL.	
	Examiner JUE ZHANG	Art Unit 2838	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *IDS filed on 08/04/2016*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-4, 7-20*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/JUE ZHANG/
Primary Examiner, Art Unit 2838

PTO-1449 **Information Disclosure Citation in an Application**	Application No. 14/204,011	Applicant(s) Huamin Zhou et al.	
	Docket Number 68354.225441	Group Art Unit 2838	Filing Date March 11, 2014

U.S. PATENT DOCUMENTS

		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	A.						
	B.						
	C.						
	D.						
	E.						
	F.						
	G.						
	H.						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	I.	101853040 A	10-06-10	CN (w/ abstract & translation)	G05F	1/56	X	
	J.	101419477 A	04-29-09	CN (w/ abstract & translation)	G05F	1/56	X	
	K.	102915061 A	02-06-13	CN (w/ abstract & translation)	G05F	1/56	X	
	L.							
	M.							
	N.							
	O.							
	P.							
	Q.							

NON-PATENT DOCUMENTS

		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
	R.	~~Chinese Office Action, Application No. 201480011600.6, 9 pages~~	~~07-28-16~~
	S.	No corresponding English translation of the item R submitted with this IDS.	
	T.		

EXAMINER	/Jue Zhang/	DATE CONSIDERED	08/07/2016

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.Z./

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Huamin Zhou et al.
Serial No.:	14/204,011
Date Filed:	March 11, 2014
Group Art Unit:	2838
Confirmation No.:	9205
Examiner:	Zhang, Jue
Title:	**USB REGULATOR WITH CURRENT BUFFER TO REDUCE COMPENSATION CAPACITOR SIZE AND PROVIDE FOR WIDE RANGE OF ESR VALUES OF EXTERNAL CAPACITOR**

MAIL STOP - AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INFORMATION DISCLOSURE STATEMENT

Applicants cite the information on the attached Form PTO-1449, pursuant to 37 C.F.R. §§1.56, 1.97, and 1.98. Applicants have enclosed a copy of each foreign patent document and non-patent literature, if applicable.

Applicants state that pursuant to 37 C.F.R. §1.97(e), that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this information disclosure statement.

The citation of this information does not constitute an admission of priority or that any cited item is available as a reference, or a waiver of any right Applicants may have under applicable statutes, Rules of Practice in patent cases, or otherwise.

This Information Disclosure Statement is being filed after receipt of a Notice of Allowance. A fee in the amount of $180.00, as required by 37 C.F.R. § 1.17(p), is being deposited at the time of filing via Deposit Account No. 50-6736 of Slayden Grubert Beard P.L.L.C. The Commissioner is authorized to charge any additional fees, or to credit any overpayment, to Deposit Account No. 50-6736.

If there are any matters concerning this Application that may be cleared up in a telephone conversation, please contact Applicants' attorney at 512.402.3553.

Respectfully submitted,
SLAYDEN GRUBERT BEARD PLLC
Attorney for Applicants

Andreas H. Grubert
Registration No. 59,143

Date: August 4, 2016

SEND CORRESPONDENCE TO:
SLAYDEN GRUBERT BEARD PLLC
CUSTOMER ACCOUNT NO. **86528**
512-402-3553
512-402-6865 (fax)

PTO-1449	Application No.	Applicant(s)		
Information Disclosure Citation in an Application	14/204,011	Huamin Zhou et al.		
	Docket Number	Group Art Unit	Filing Date	
	68354.225441	2838	March 11, 2014	

U.S. PATENT DOCUMENTS

		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	A.						
	B.						
	C.						
	D.						
	E.						
	F.						
	G.						
	H.						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	I.	101853040 A	10-06-10	CN (w/ abstract & translation)	G05F	1/56	X	
	J.	101419477 A	04-29-09	CN (w/ abstract & translation)	G05F	1/56	X	
	K.	102915061 A	02-06-13	CN (w/ abstract & translation)	G05F	1/56	X	
	L.							
	M.							
	N.							
	O.							
	P.							
	Q.							

NON-PATENT DOCUMENTS

		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
	R.	Chinese Office Action, Application No. 201480011600.6, 9 pages	07-28-16
	S.		
	T.		

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

Espacenet

Bibliographic data: CN101419477 (A) — 2009-04-29

Controllable low voltage differential linear voltage stabilizing circuit for providing multi-output voltages

Inventor(s): HAIGANG ZHU [KR] + (ZHU HAIGANG)

Applicant(s): SAMSUNG ELECTRONICS CO LTD [KR] + (SAMSUNG ELECTRONICS CO., LTD, ; SAMSUNG SEMICONDUCTOR (CHINA) R&D CO., LTD)

Classification: **- international:** ***G05F1/56***
- cooperative:

Application number: CN20071166861 20071022

Priority number (s): CN20071166861 20071022

Also published as: CN101419477 (B)

Abstract of CN101419477 (A)

The invention provides a low-dropout linear voltage regulator circuit which comprises a bandgap reference voltage circuit for generating reference voltage, an error amplifier, a driving cushion circuit, a power PMOS pipe and a feedback control circuit, wherein a negative end of the error amplifier receives reference voltage output by the bandgap reference voltage circuit; a positive end of the driving cushion circuit is connected with an output end of the error amplifier, and a negative end is connected with the output end; a source electrode of the power PMOS pipe receives power voltage of the low-dropout linear voltage regulator circuit, a drain electrode outputs the voltage, and a mesh electrode is connected to the output end of the driving cushion circuit,; the feedback control circuitis connected between the positive end of the error amplifier and the drain electrode of the power PMOS pipe for the feedback of the output voltage. The low-dropout linear voltage regulator circuit realizes multiple voltage output by controlling feedback coefficients of a feedback resistive network by two signals. Moreover, a broadband operation transconductance amplification circuit with low power consumption and a unit gain structure is used for realizing the driving cushion circuit and the stable work of the high-load current circuit and rapid response performance can be ensured.

Aptiv Services US, LLC Exhibit 1003 Page 13

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

DESCRIPTION CN101419477

It provides a low dropout linear regulator circuit, comprising: a bandgap reference voltage circuit for generating a reference voltage; an error amplifier which receives negative bandgap voltage reference circuit output voltage to the end; driving buffer circuit, the forward end connected to the output of the error amplifier, the negative terminal and the output terminals shorted; power PMOS transistor having a source receiving low-dropout linear regulator circuit power supply voltage, the output voltage of the drain and the gate connected to the driving buffer circuit output end; feedback control circuit connected between the forward end and the power drain of PMOS transistor error amplifier for feedback output voltage. The low dropout linear regulator circuit is controlled by two signal feedback coefficient feedback resistor network, enabling multi-voltage output. In addition, by adopting the structure of unity gain wideband low power operational transconductance amplifier to achieve the driving buffer circuit to ensure the stable operation of high load currents and rapid response.

Provide more controllable output voltage low dropout linear regulator circuit

TECHNICAL FIELD

The present invention relates to a low dropout linear regulator circuit, and more particularly, relates to a method of providing multiple-output Controllable voltage low dropout linear regulator circuit.

Background technique

Low dropout linear regulator circuit power supply is an important branch of the integrated circuit, and based on a pulse width Modulation (PWM), pulse frequency modulation (PFM) Principle of DC-DC (direct current - direct current) converters Compared to its low cost, low noise and small quiescent current and inductance without merit. Portable Electronic products, often using low dropout linear regulator circuit as a power supply system.

Figure 1 shows a conventional low-dropout linear regulator circuit schematic. As shown, a conventional low Dropout linear regulator circuit includes a reference voltage circuit, an error amplifier OTA1, power PMOS transistor, Feedback resistor network. Reference voltage circuit commonly used bandgap reference voltage circuit, an error amplifier OTA1 Usually two differential operational amplifier, the power PMOS transistor channel width is large, large-small channel length PMOS transistor size, but also the use of special manufacturing process of the power PMOS transistor, such as PDMOS tubes.

PMOS source power source input voltage (ie, low-dropout linear regulator circuit power supply voltage Vin), the drain output voltage, output voltage through the feedback resistor divider network input of the error amplifier OTA1 the positive side, the reference voltage input of the error amplifier OTA1 negative terminal of the error amplifier OTA1 Compare and amplifies the voltage across the positive and negative input, and the output voltage to the control gate of power PMOS transistor, Whereby the output voltage. Thus, the error amplifier OTA1, PMOS power transistor and the feedback resistor network Constitutes a stable feedback loop.

Based on the feedback loop has a sufficient degree of gain and phase threshold, the output voltage and the reference value is only Feedback coefficient voltage and the feedback resistor network related, independent of the input voltage. Meanwhile, since the reference level Pressure has a very low temperature drift, so if the feedback resistor network are well matched, the output voltage also Low temperature drift. It is possible to achieve a high precision, low noise and output ripple voltage.

However, the conventional low dropout linear regulator circuit has the following two problems.

First, the traditional low dropout linear regulator circuit is generally only a fixed and externally adjustable output voltage input Two types of voltage. Fixed output voltage of the circuit can provide an output voltage; externally adjustable output Voltage circuit must be connected externally different resistor values to get different output voltages, such parties Since the law requires an external resistor, not only increases the cost of the application, and an external resistor accuracy and temperature coefficient And number seriously affect the accuracy of the output voltage.

Secondly, when higher output drive current, power PMOS transistor dimensions will also increase, Thus the PMOS gate parasitic capacitance power corresponding increase, which makes the loop first parasitic pole (ie, closest to the dominant pole parasitic pole) frequency reduced accordingly. On the other hand, a large driving So that the first main flow loop pole moves to higher frequencies. Thus, the first primary and the first parasitic pole Pole close, resulting in a substantial decline in the loop of the phase threshold, so that the entire circuit is not stable. Eye Before the general solution is to use a high ESR (equivalent series resistance) of the load capacitance to generate a left Half-plane zero to eliminate the first parasitic pole. However, the high ESR of the load capacitance increases the cost of the application, And will reduce the transient performance of the circuit. Another solution is the error amplifier and power Increase between the PMOS transistor a source follower buffer stage driving structure to isolate the error amplifier circuit high input impedance and power PMOS transistor gate large parasitic capacitance. However, the drive source follower buffer stage structure It will produce the input and output voltage level shift, causing the PMOS power can not be turned on or off.

SUMMARY

One aspect of the present invention, an exemplary embodiment is that at least solve the above problems and / or disadvantages and at least It provides the following advantages. Accordingly, one aspect of the present invention, an exemplary embodiment can be provided to provide a More controllable output voltage low dropout linear regulator circuit.

According to an aspect of the present invention, there is provided a low dropout linear regulator circuit, comprising: a bandgap The reference voltage circuit for generating a reference voltage; an error amplifier which receives negative bandgap reference voltage circuit to the end Output reference voltage; driving buffer circuit, the forward end of the error amplifier is connected to the output, Electric power PMOS transistor having a source receiving low dropout linear regulator circuit; short to the negative terminal and the output terminal Source voltage, output voltage of the drain and the gate connected to the driving buffer circuit output terminal; a feedback control Circuit connected between the forward end and the power drain of PMOS transistor error amplifier for feedback input Voltage.

The low dropout linear regulator circuit by using a feedback control circuit to achieve a multi-voltage output, this In addition, by using the unity gain structure across broadband low power operational amplifier to achieve the guide drive slow Chong circuit to ensure the stable operation of high load currents and rapid response.

BRIEF DESCRIPTION

With reference to the following description of embodiments, these and / or other aspects of the present invention and Advantages will become apparent and more readily appreciated in which:

Figure 1 shows a conventional low-dropout linear regulator circuit schematic diagram;

Figure 2 shows an embodiment according to the principles of the present invention, low-dropout linear regulator circuit embodiment of FIG;

Figure 3 shows a unity gain knot according to low dropout linear regulator circuit of the embodiment of the present invention employed Configuration of a wideband low power operational transconductance amplifying circuit diagram of a circuit implementation of the driving buffer circuit; and

Figure 4 is a diagram showing low dropout linear regulator circuit of the embodiment of the present invention, a feedback control circuit Circuit diagram.

detailed description

Embodiments of the invention will now be described in detail, which are illustrated in the accompanying drawings, wherein the phase The same reference numerals refer to like parts. Below by referring to the accompanying drawings, embodiments will be described to explain the present invention.

Figure 2 shows an embodiment according to the principles of the present invention, low-dropout linear regulator circuit embodiment of FIG. Referring to Figure 2, The low dropout linear regulator circuit includes a bandgap reference voltage circuit 201, an error amplifier OTA 1 202, Driving buffer circuit OTA 2 203, PMOS transistor 204 and the power feedback control circuit 205. Power PMOS Tube 204 source input voltage (ie, low-dropout linear regulator circuit power supply voltage Vin), a drain output Voltage. The feedback control circuit 205 is connected to the positive terminal of the error amplifier and output OTA1 202 in Between the pressure side, the bandgap reference voltage circuit 201 outputs a reference voltage of the error amplifier OTA1 202 The negative terminal is connected, the error amplifier output OTA1 202 and the driving buffer circuit OTA 2 203 The positive terminal is connected, the error buffer circuit OTA negative terminal to its output terminal shorting 2203, the drive slow Chong circuit OTA output terminal 2203 is connected to the gate of the power PMOS tube.

[1]

At the output low dropout linear regulator circuit is connected to an external load RL. Meanwhile, low-dropout line The connection between the output terminal of the voltage regulator circuit and the ground capacitor CL, and thus at the output frequency of about 1Main regulator circuit / 2πRLCL pole so low dropout linear regulator circuit has sufficient phase threshold Degrees, keep the whole circuit stability. In this embodiment, CL = 1μF. However, the present invention is not limited to This may also be used other large capacitance capacitors.

[2]

Figure 3 shows a unity gain knot according to low dropout linear regulator circuit of the embodiment of the present invention employed Configuration of a wideband low power operational transconductance amplifier to achieve a driving buffer circuit driving buffer circuit OTA 2 203The circuit diagram in which the bias (Bias) end by a bandgap reference voltage circuit 201 provided. Referring to FIG. 3 , Driving buffer circuit OTA 2 203 units gain structure using wideband low power operational transconductance amplifier circuit The way to achieve. Driving buffer circuit OTA 2 203 to isolate the error amplifier output impedance and high Great power PMOS transistor gate parasitic capacitance. From ac circuit analysis point of view, the driving buffer circuit OTA 2Parasitic poles 203 is split into a lower frequency of the two poles of a higher frequency, thereby increasing the The error amplifier OTA1 202, the driving buffer circuit OTA 2 203, PMOS transistor 204 and the power feedback Negative feedback loop phase threshold of the unit and the control circuit 205 feedback resistor network consisting of band gain Wide, to ensure stability and fast response regulator circuit. And drive single-tube structure of the source follower buffer Chong circuit, this kind of unity gain structure using wideband low power operational transconductance amplifier driving Buffer circuit, no input and output level shift, which can guarantee the normal power PMOS transistor On and off. Parasitic pole position and structure

Aptiv Services US, LLC Exhibit 1003 Page 16

of the original structure in accordance with an embodiment of the present invention is defined by the following Expressed as follows:

The original structure: a lower frequency parasitic poles, fp = 1 / 2πREAoutCpmos.

Embodiments of the invention: two higher frequency parasitic node, fp1 = 1 / 2πREAoutCOTA2in and fp2 = 1 / 2πROTA2outCpmos.

Wherein, REAout to the original structure of the output impedance of the error amplifier, Cpmos of the power PMOS Parasitic gate capacitance, ROTA2out to drive the output impedance of the buffer circuit 2203 of OTA, COTA2in drive OTA 2 203 buffer circuit input capacitance.

OTA 2 203 driving buffer circuit output resistance ROTA2out = 1 / gm · N, therefore, fp2 = gm · N / 2πCpmos, where, gm is the driving buffer stage circuit inlet tube (ie, power PMOS Tube) transconductance, (W / L) MP4 MP4 tube in FIG. 3 the channel width and the channel Ratio of the length, channel width and channel length (W / L) MP2 MP2 in FIG tube 3 ratio. While driving Buffer circuit input capacitance of OTA 2 203 COTA2in the drive circuit input buffer stage tube (ie, power PMOS transistors) of the channel width and channel length is proportional to the product of W · L. Thus, by adjusting to The parameters to set fp1 and fp2 location.

[205]

Figure 4 is a diagram showing low dropout linear regulator circuit of the embodiment of the present invention, a feedback control circuit 205Circuit diagram. By appiying feedback control circuit, the output voltage can be achieved in a controlled low pressure Dropout linear regulator circuit. Feedback control circuit is not increased static power consumption, and its occupation of the wafer surface Product compared with the original circuit area is small.

[2]

Referring to FIG. 4, the feedback control circuit 205 by a decoding circuit 2-4, the switch circuit and the feedback resistor network Network of three parts. Feedback resistor network comprising four resistors R1, R2, R3 and R4, are connected in series Low dropout linear regulator circuit between the output and ground. R1 input and low-dropout linear regulator circuit The output terminal connected to the output of R1 and R2 is connected to the input terminal. The output of R2 and R3 is Input terminal connected to the output terminal R3 is connected to the input terminal of R4, R4 is an output terminal connected to ground. Switching circuit includes four switches S1, S2, S3 and S4, which are connected to the positive OTA1 202 Between the input terminal and the input terminal of the four resistors. 2-4 Decoding circuit the two input signals are A and B, its value is 0 or Vin. 2-4 Decoding circuit to decode the two input signals O1, O2, O3 and O4 Four signals. The four signals are controlled by the four switches S1, S2, S3 and S4 of the switch To determine the overall state of the loop feedback factor, thereby obtaining different output voltage values. Specific output Pressure derivation formula as follows:

When S1 is turned on, Vreg = Vbgr;

When S2 is turned on,

When S3 is turned on,

When S4 is turned on,

Wherein, Vreg is the output voltage, Vbgr reference voltage.

[14]

When the reference voltage is 1.2V, in order to obtain the output voltage 1.2V, 1.5V, 1.8V and 2.5V Respectively corresponding feedback coefficient resistor network design R1: R2: R3: R4 ratio of 15:10: 14: 36. According to the above formula, low dropout linear regulator circuit specific output voltage control as shown in Table 1 Shown.

Table 1

<Img class = "EMIRef" id = "101481524-idf0005" />

All circuits of the present invention are in the standard CMOS process, not using special technology MOS tube.

In summary, low dropout linear regulator circuit according to the present invention by using a feedback control circuit real Now the multi-voltage output. In addition, through the gate of the power output of the error amplifier PMOS transistor Adopted by the unit gain structure between broadband low power operational transconductance amplifier driving buffer circuit implemented Way to ensure the stability of high load currents and rapid response.

Although the present invention with reference to certain exemplary embodiments of the present invention is shown and described, but the present The skilled artisan will appreciate that, without departing from the claims and their equivalents of the present invention. The case of God and scope of the various changes in form and detail.

[19] 中华人民共和国国家知识产权局

[51] Int. Cl.
G05F 1/56 (2006.01)

[12] 发明专利申请公布说明书

[21] 申请号 200710166861.7

[43] 公开日 2009 年 4 月 29 日

[11] 公开号 CN 101419477A

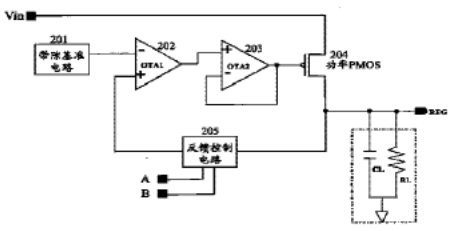
[22] 申请日 2007.10.22
[21] 申请号 200710166861.7
[71] 申请人 三星电子株式会社
地址 韩国京畿道水原市灵通区梅滩洞 416
共同申请人 三星半导体(中国)研究开发有限公司
[72] 发明人 朱海刚
[74] 专利代理机构 北京铭硕知识产权代理有限公司
代理人 郭鸿禧 韩素云
权利要求书 1 页 说明书 6 页 附图 2 页

[54] 发明名称

提供多输出电压的可控低压差线性稳压电路

[57] 摘要

提供了一种低压差线性稳压电路，包括：带隙基准电压电路，产生基准电压；误差放大器，其负向端接收带隙基准电压电路输出的基准电压；驱动缓冲电路，其正向端与误差放大器的输出端相连接，负向端与输出端短接；功率 PMOS 管，其源极接收低压差线性稳压电路的电源电压，漏极输出电压，并且栅极连接到驱动缓冲电路的输出端；反馈控制电路，连接在误差放大器的正向端和功率 PMOS 管的漏极之间，用于反馈输出电压。所述低压差线性稳压电路通过两个信号来控制反馈电阻网络的反馈系数，从而实现多电压输出。此外，通过采用单位增益结构的宽带低功耗运算跨导放大电路来实现驱动缓冲电路，保证了高负载电流电路的稳定工作和快速响应性能。



1、一种低压差线性稳压电路，包括：

带隙基准电压电路，产生基准电压；

误差放大器，其负向端接收带隙基准电压电路输出的基准电压；

驱动缓冲电路，其正向端与误差放大器的输出端相连接，负向端与输出端短接；

功率 PMOS 管，其源极接收低压差线性稳压电路的电源电压，漏极输出电压，并且栅极连接到驱动缓冲电路的输出端；

反馈控制电路，连接在误差放大器的正向端和功率 PMOS 管的漏极之间，用于反馈输出电压。

2、如权利要求 1 所述的低压差线性稳压电路，其中，反馈控制电路包括：

2-4 译码电路，其两个输入信号分别为 0 或低压差线性稳压电路的电源电压，并输出将两个输入信号译码而得到的四个输出信号；

反馈电阻网络，由四个串联连接的电阻器构成，连接在输出电压和地之间，其中，所述四个电阻器中的第一电阻器的输入端连接到输出电压，而第四电阻器的输出端连接到地；

开关电路，包括四个开关，所述四个开关分别连接在误差放大器的正向端和所述四个电阻的输入端之间，并且所述四个开关分别由 2-4 译码器的所述四个输出信号控制其导通与否。

3、如权利要求 1 所述的低压差线性稳压电路，其中，驱动缓冲电路是采用单位增益结构的宽带低功耗运算跨导放大电路。

4、如权利要求 1 所述的低压差线性稳压电路，还包括：

电容器，连接在功率 PMOS 管的漏极和地之间，用于产生低压差线性稳压电路的主极点，使得低压差线性稳压电路具有足够的相位阈度。

5、如权利要求 2 所述的低压差线性稳压电路，其中，通过根据 2-4 译码电路的输出信号导通开关电路中不同的开关，低压差线性稳压电路被控制以提供多个不同的输出电压。

Aptiv Services US, LLC Exhibit 1003 Page 20

提供多输出电压的可控低压差线性稳压电路

技术领域

本发明涉及一种低压差线性稳压电路，更具体地讲，涉及一种提供多输出电压的可控低压差线性稳压电路。

背景技术

低压差线性稳压电路是电源集成电路中的一个重要分支，和基于脉冲宽度调制（PWM）、脉冲频率调制（PFM）原理的 DC-DC（直流-直流）转换器相比，它具有低成本、低噪声和静态电流小以及无需电感的优点。在便携式电子产品中，经常会使用低压差线性稳压电路作为系统的电源。

图 1 示出传统的低压差线性稳压电路的原理图。如图 1 所示，传统的低压差线性稳压电路包括基准电压电路、误差放大器 OTA1、功率 PMOS 管、反馈电阻网络。基准电压电路一般采用带隙基准电压电路，误差放大器 OTA1 一般为两级差分运算放大器，功率 PMOS 管为大沟道宽度、小沟道长度的大尺寸 PMOS 管，也有利用特殊工艺制造的功率 PMOS 管，如 PDMOS 管等。

功率 PMOS 管的源极输入电压（即，低压差线性稳压电路的电源电压 Vin），漏极输出电压，输出电压经过反馈电阻网络分压后输入误差放大器 OTA1 的正向端，基准电压输入误差放大器 OTA1 的负向端，误差放大器 OTA1 比较并放大正负两端的输入电压，并输出电压以控制功率 PMOS 管的栅极，从而得到输出电压。这样，误差放大器 OTA1、PMOS 功率管和反馈电阻网络构成一个稳定的反馈环路。

在反馈环路具有足够的增益和相位阈度的基础上，输出电压值只与基准电压和反馈电阻网络的反馈系数有关，与输入电压无关。同时，因为基准电压具有极低的温漂，所以如果反馈电阻网络匹配良好，那么输出电压也具有较低的温漂。从而能够实现一种高精度、低噪声和纹波的输出电压。

然而，传统的低压差线性稳压电路具有以下两个问题。

首先，传统的低压差线性稳压电路一般只有固定输出电压和外部可调输出电压两种类型。固定输出电压电路只能提供一种输出电压值；外部可调输

Aptiv Services US, LLC Exhibit 1003 Page 21

出电压电路需要在外部连接不同阻值的电阻来获得不同的输出电压，这种方法由于需要外部电阻，不仅增加了应用成本，而且外部电阻的精度和温度系数等严重影响了输出电压的精度。

其次，当输出驱动电流要求较高时，功率 PMOS 管的尺寸也相应增大，从而功率 PMOS 管的栅极寄生电容相应增大，这使得环路的第一寄生极点（即，最靠近主极点的寄生极点）的频率相应降低。另一方面，大的驱动电流使得环路的第一主极点向更高的频率移动。这样，第一主极点和第一寄生极点靠近，导致环路的相位阈度大幅下降，从而整个电路不能稳定工作。目前的解决方式一般是使用高 ESR（等效串联电阻）的负载电容来产生一个左半平面零点来消除第一寄生极点。但是，高 ESR 的负载电容增加了应用成本，并且会降低电路的瞬态性能。另外一种解决方式是在误差放大器和功率 PMOS 管之间增加一级源随器结构的驱动缓冲级来隔离误差放大电路的高输出阻抗和功率 PMOS 管的栅极大寄生电容。但是，源随器结构的驱动缓冲级会使输入和输出电压产生电平位移，导致功率 PMOS 管无法导通或截止。

发明内容

本发明示例性实施例的一方面在于至少解决上述问题和/或缺点，并至少提供以下优点。因此，本发明示例性实施例的一方面在于提供一种能够提供多输出电压的可控低压差线性稳压电路。

根据本发明的一方面，提供了一种低压差线性稳压电路，包括：带隙基准电压电路，产生基准电压；误差放大器，其负向端接收带隙基准电压电路输出的基准电压；驱动缓冲电路，其正向端与误差放大器的输出端相连接，负向端与输出端短接；功率 PMOS 管，其源极接收低压差线性稳压电路的电源电压，漏极输出电压，并且栅极连接到驱动缓冲电路的输出端；反馈控制电路，连接在误差放大器的正向端和功率 PMOS 管的漏极之间，用于反馈输出电压。

所述低压差线性稳压电路通过使用反馈控制电路实现了多电压输出。此外，通过采用由单位增益结构的宽带低功耗运算跨导放大电路实现的驱动缓冲电路，保证了高负载电流电路的稳定工作和快速响应性能。

附图说明

Aptiv Services US, LLC Exhibit 1003 Page 22

通过下面结合附图对实施例进行的描述，本发明的这些和/或其他方面和优点将会变得清楚和更易于理解，其中：

图 1 示出传统的低压差线性稳压电路的原理图；

图 2 示出根据本发明实施例的低压差线性稳压电路的原理图；

图 3 是示出根据本发明实施例的低压差线性稳压电路中采用单位增益结构的宽带低功耗运算跨导放大电路实现的驱动缓冲电路的电路图；和

图 4 是示出根据本发明实施例的低压差线性稳压电路中的反馈控制电路的电路图。

具体实施方式

现在对本发明实施例进行详细的描述，其示例表示在附图中，其中，相同的标号始终表示相同部件。下面通过参照附图对实施例进行描述以解释本发明。

图 2 示出根据本发明实施例的低压差线性稳压电路的原理图。参照图 2，所述低压差线性稳压电路包括带隙基准电压电路 201、误差放大器 OTA1 202、驱动缓冲电路 OTA 2 203、功率 PMOS 管 204 和反馈控制电路 205。功率 PMOS 管 204 的源极输入电压（即，低压差线性稳压电路的电源电压 Vin），漏极输出电压。反馈控制电路 205 连接在误差放大器 OTA1 202 的正向端和输出电压端之间，带隙基准电压电路 201 的输出基准电压与误差放大器 OTA1 202 的负向端连接，误差放大器 OTA1 202 的输出端和驱动缓冲电路 OTA 2 203 的正向端连接，误差缓冲电路 OTA 2 203 的负向端与其输出端短接，驱动缓冲电路 OTA 2 203 的输出端连接到功率 PMOS 管的栅极。

在低压差线性稳压电路的输出端连接有外部负载 R_L。同时，在低压差线性稳压电路的输出端与地之间连接有电容器 C_L，从而在输出端产生频率约为 $1/2\pi R_L C_L$ 的稳压电路的主极点，使得低压差线性稳压电路具有足够的相位阈度，保持整个电路稳定工作。在本实施例中，C_L=1μF。然而，本发明不限于此，也可采用其他容值较大的电容器。

图 3 是示出根据本发明实施例的低压差线性稳压电路中采用单位增益结构的宽带低功耗运算跨导放大电路实现的驱动缓冲电路驱动缓冲电路 OTA 2 203 的电路图，其中，偏置（Bias）端由带隙基准电压电路 201 提供。参照图 3，驱动缓冲电路 OTA 2 203 采用单位增益结构的宽带低功耗运算跨导放大电

Aptiv Services US, LLC Exhibit 1003 Page 23

路来实现。驱动缓冲电路 OTA 2 203 用来隔离误差放大电路的高输出阻抗和功率 PMOS 管的栅极大寄生电容。从电路的 ac 分析上看，驱动缓冲电路 OTA 2 203 把一个较低频率的寄生极点分裂成两个较高频率的极点，从而增大了由误差放大器 OTA1 202、驱动缓冲电路 OTA 2 203、功率 PMOS 管 204 和反馈控制电路 205 中的反馈电阻网络构成的负反馈环路的相位阈度和单位增益带宽，保证稳压电路的稳定性和快速响应能力。与单管源跟随器结构的驱动缓冲电路相比，这种采用单位增益结构的宽带低功耗运算跨导放大电路的驱动缓冲电路，不会产生输入输出电平位移，从而能够保证功率 PMOS 管的正常开启和关断。原有结构和根据本发明实施例的结构的寄生极点位置由如下公式表述：

原有结构：一个较低频率的寄生极点，$f_p = 1/2\pi R_{EAout} C_{pmos}$。

本发明实施例：两个频率较高的寄生节点，$f_{p1} = 1/2\pi R_{EAout} C_{OTA2in}$ 和 $f_{p2} = 1/2\pi R_{OTA2out} C_{pmos}$。

其中，R_{EAout} 为原有结构中误差放大器的输出阻抗，C_{pmos} 为功率 PMOS 的栅极寄生电容，$R_{OTA2out}$ 为驱动缓冲电路 OTA 2 203 的输出阻抗，C_{OTA2in} 为驱动缓冲电路 OTA 2 203 的输入电容。

驱动缓冲电路 OTA 2 203 的输出电阻为 $R_{OTA2out} = 1/g_m \bullet N$，因此，$f_{p2} = g_m \bullet N/2\pi C_{pmos}$，其中，$g_m$ 为驱动缓冲级电路输入管（即，功率 PMOS 管）的跨导，$N = \frac{(W/L)_{MP4}}{(W/L)_{MP2}}$，$(W/L)_{MP4}$ 为图 3 中 MP4 管的沟道宽度和沟道长度之比，$(W/L)_{MP2}$ 为图 3 中 MP2 管的沟道宽度和沟道长度之比。而驱动缓冲电路 OTA 2 203 的输入电容 C_{OTA2in} 与驱动缓冲级电路输入管（即，功率 PMOS 管）的沟道宽度和沟道长度的乘积 $W \bullet L$ 成正比。因此，可通过调整以上参数来设置 f_{p1} 和 f_{p2} 的位置。

图 4 是示出根据本发明实施例的低压差线性稳压电路中的反馈控制电路 205 的电路图。通过应用反馈控制电路，可以实现一种可控输出电压的低压差线性稳压电路。增加的反馈控制电路没有静态功耗，而且其占用的硅片面积跟原电路面积相比也很小。

参照图 4，反馈控制电路 205 由 2-4 译码电路、开关电路和反馈电阻网络三部分构成。反馈电阻网络包括四个电阻 R1、R2、R3 和 R4，串联连接在低压差线性稳压电路的输出端和地之间。R1 的输入端与低压差线性稳压电路的输出端相连接，R1 的输出端与 R2 的输入端相连接。R2 的输出端与 R3 的

Aptiv Services US, LLC Exhibit 1003 Page 24

输入端相连接，R3 的输出端与 R4 的输入端相连接，R4 的输出端连接到地。开关电路包括四个开关 S1、S2、S3 和 S4，它们分别连接在 OTA1 202 的正向输入端和四个电阻的输入端之间。2-4 译码电路的两个输入信号分别为 A 和 B，其值为 0 或 Vin。2-4 译码电路将两个输入信号译码为 O1、O2、O3 和 O4 这四个信号。所述四个信号通过分别控制四个开关 S1、S2、S3 和 S4 的开关状态来决定整个环路的反馈系数，从而得到不同的输出电压值。具体输出电压的推导公式如下：

当 S1 导通时，$Vreg = Vbgr$；

当 S2 导通时，$Vreg = Vbgr \bullet \frac{R_1 + R_2 + R_3 + R_4}{R_2 + R_3 + R_4}$；

当 S3 导通时，$Vreg = Vbgr \bullet \frac{R_1 + R_2 + R_3 + R_4}{R_3 + R_4}$；

当 S4 导通时，$Vreg = Vbgr \bullet \frac{R_1 + R_2 + R_3 + R_4}{R_4}$。

其中，*Vreg* 为输出电压，*Vbgr* 为基准电压。

当基准电压为 1.2V 时，为了得到与输出电压 1.2V、1.5V、1.8V 和 2.5V 分别相应的反馈系数，电阻网络的设计中 R1：R2：R3：R4 的比值为 15：10：14：36。根据以上公式，低压差线性稳压电路的具体输出电压控制如表 1 所示。

表 1

A	B	O1	O2	O3	O4	REG
0	0	Vin	0	0	0	1.2V
0	Vin	0	Vin	0	0	1.5V
Vin	0	0	0	Vin	0	1.8V
Vin	Vin	0	0	0	Vin	2.5V

本发明的所有电路均在标准 CMOS 工艺下实现，并未采用特殊工艺制作的 MOS 管。

综上所述，根据本发明的低压差线性稳压电路通过使用反馈控制电路实现了多电压输出。此外，通过在误差放大器的输出端功率 PMOS 管的栅极之间采用由单位增益结构的宽带低功耗运算跨导放大电路实现的驱动缓冲电路，保证了高负载电流电路的稳定工作和快速响应性能。

Aptiv Services US, LLC Exhibit 1003 Page 25

虽然已经参照本发明的特定示例性实施例显示和描述了本发明，但是本领域技术人员应该理解，在不脱离由权利要求及其等同物限定的本发明的精神和范围的情况下，可在形式和细节上进行各种改变。

Aptiv Services US, LLC Exhibit 1003 Page 26

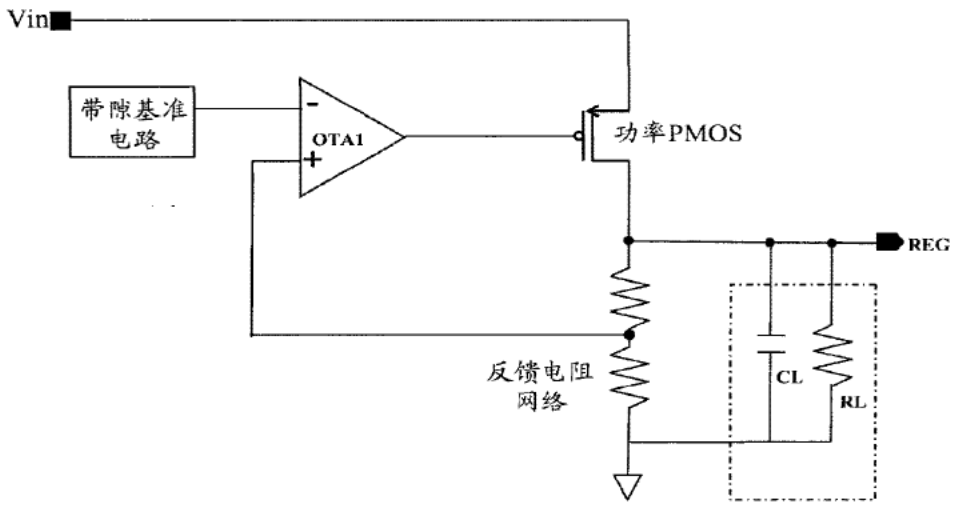


图1

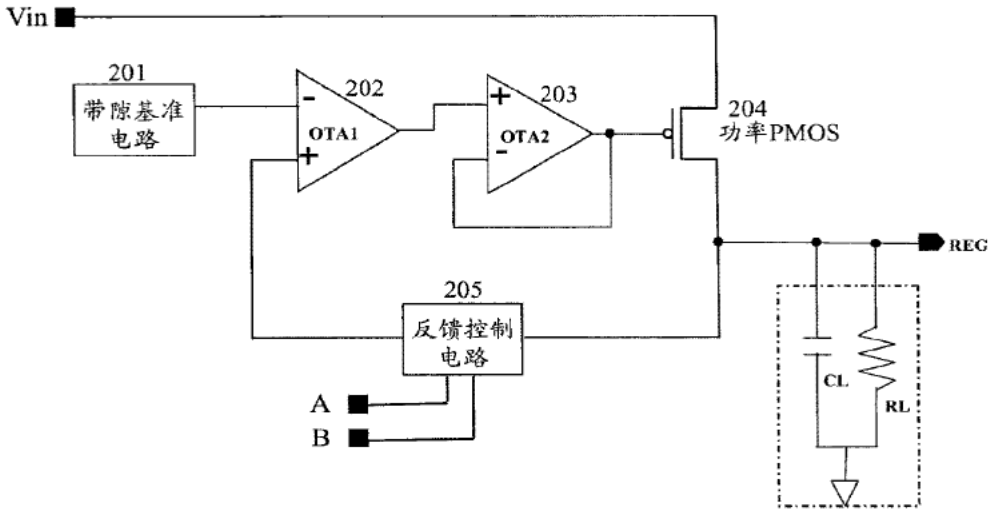


图2

Aptiv Services US, LLC Exhibit 1003 Page 27

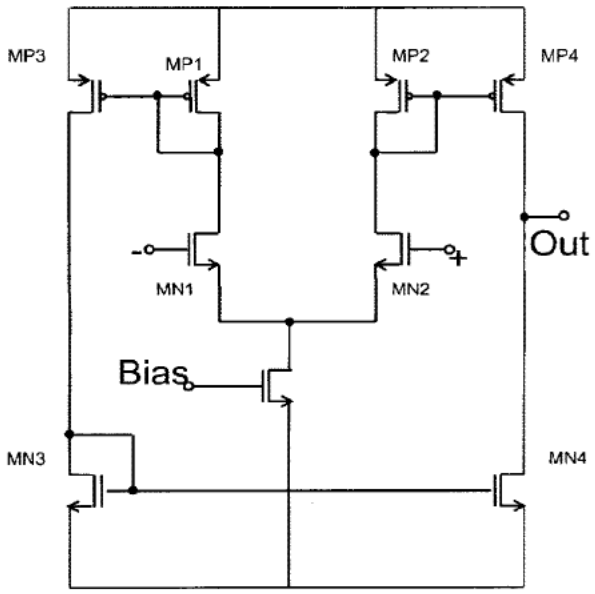


图3

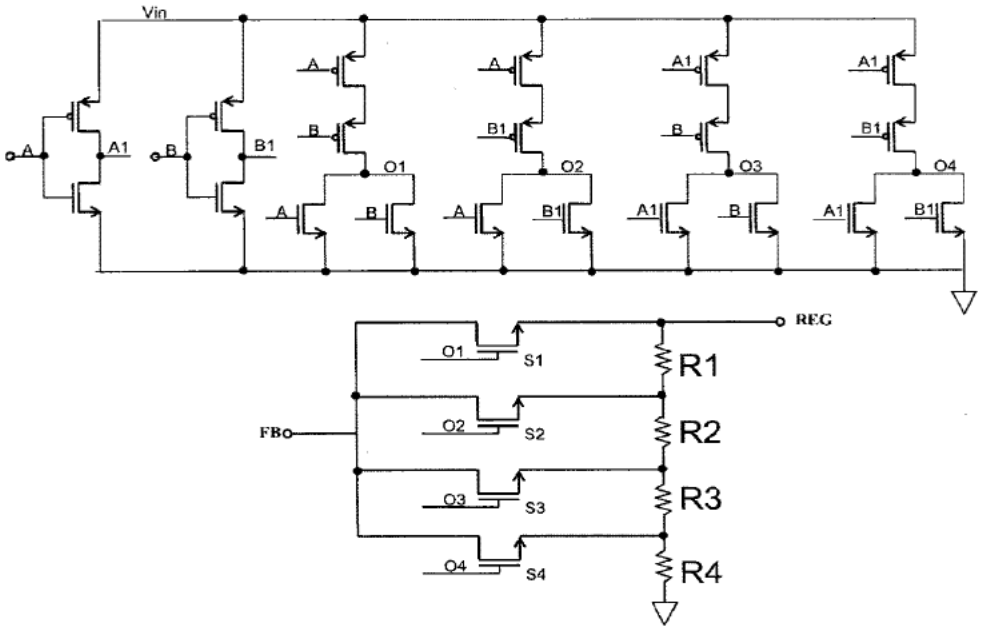


图4

Aptiv Services US, LLC Exhibit 1003 Page 28

Espacenet

Bibliographic data: CN101853040 (A) — 2010-10-06

High mains rejection ratio low dropout voltage linear voltage regulator with feedforward transconductance

Inventor(s): SHENGZHUAN HUANG; ZHE ZHAO; FENG ZHOU ± (HUANG SHENGZHUAN, ; ZHAO ZHE, ; ZHOU FENG)

Applicant(s): UNIV FUDAN ± (FUDAN UNIVERSITY)

Classification: **- international:** ***G05F1/56***
- cooperative:

Application number: CN20101217348 20100705

Priority number (s): CN20101217348 20100705

Abstract of CN101853040 (A)

The invention belongs to the technical field of integrated circuits and specifically relates to a high mains rejection ratio low dropout voltage linear voltage regulator with a feedforward transconductance, which consists of an error amplifier, a buffer, a PMOS pass transistor, a feedforward transconductance, two feedback resistors and a filter capacitor, wherein the error amplifier is a current mirror amplifier consisting of a tail current source, a PMOS input differential pair and three groups of current mirrors. The mains voltage fluctuation influences the output mainly via two paths of the PMOS pass transistor and the parasitic resistor of and PMOS pass transistor. The feedforward transconductance transforms the perturbation of the mains voltage into the perturbation of the current, and then the perturbation of the current is transformed into the in-phase voltage perturbation of the grid of the pass transistor via the parasitic resistor of the error amplifier. The influence of the mains voltage perturbation on the output can be eliminated by the control of the gain of the feedforward transconductance so as to realize high mains rejection ratio. The invention can optimize the mains rejection ratio within a wider range of load current and does not reduce the efficiency of the low dropout voltage linear voltage regulator.

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

DESCRIPTION CN101853040

The present invention belongs to the field of integrated circuit technology, in particular to a band feedforward transconductance high PSRR low-dropout linear regulator. It consists of an error amplifier, a buffer, PMOS transfer tubes, feedforward transconductance, two feedback resistors and filter capacitors. The error amplifier by the tail current source, PMOS input differential pair and the current mirror three groups constitute a current mirror amplifier. Effect of supply voltage fluctuations on the output of the main transmission through the parasitic resistance PMOS and PMOS transfer tubes of these two pathways. Feedforward transconductance of the power supply voltage disturbances into electricity disturbance, and then after the error amplifier parasitic resistance transfer tube into the gate of an in-phase voltage disturbances. Through feedforward control transconductance gain, eliminate disturbances on the power supply voltage output, high power supply rejection ratio. The present invention can be optimized without degrading the power supply rejection low dropout linear regulator efficiency than in a wider range of load currents.

One kind with feedforward transconductance High PSRR Low Dropout Linear Regulator

TECHNICAL FIELD

The present invention belongs to the field of integrated circuit technology, in particular to a with feedforward transconductance high PSRR low-dropout linear regulator (LDO).

Background technique

[0002]

LDO power management is the core module, analog circuits and RF circuits and other noise-sensitive circuitry to improve supplies power mainly. Thus, the power supply rejection ratio is one of the key performance parameters.

Currently, most commercial high PSRR LDO chip LDO cascade, such programs had led to low efficiency of LDO. Although in recent years, many papers appeared high PSRR LDO solutions, but they are mostly in increasing the output of the output voltage noise, increasing circuit complexity and expense of lower load currents.

Therefore, to design a not to increase the output voltage noise at the cost of a simple circuit structure, can provide more load current high power supply rejection ratio has great application significance.

SUMMARY

To solve the above problems, the present invention provides a high power supply based on the feedforward transconductance rejection ratio LDO. Before the invention of the proposed method of maintaining LDO transconductance fed a high efficiency, low noise performance, simple circuit structure and make LDO get high power supply rejection ratio over the entire load range of power.

The present invention is proposed based on the feedforward transconductance high PSRR LDO, by the error amplifier 1, buffer 2, PMOS transfer tubes 3, feedforward transconductance feedback resistor in series 4,2 5,6-chip compensation via the capacitor 7 connected to form a circuit; wherein the non-inverting input of the error amplifier 1 connected to a voltage feedback

terminal 11, an output terminal connected to a reference source Vref is inverted, the end of the error amplifier 8 and a feedforward transconductance output terminal 4 of the buffer 2 connected to the input; feedforward transconductance 4 input termination power output of the buffer 2 of 9 transfer tubes connected PMOS gate terminal 3, the PMOS source termination power transfer tubes 3, the drain terminal connected to the output of the LDO 10 ; a feedback resistor in series with one end of the LDO output 10, the other end; a compensation capacitor 7 termination LDO output 10, the other end.

The present invention feedforward transconductance 4 will fluctuate on supply voltage into a current fluctuations, and then by the error output parasitic resistance converted into phase with the voltage fluctuation PMOS transfer tubes 3 gate offset supply voltage fluctuation transfer tube source of output voltage impact. In different load current conditions, the desired different transconductance gain. In the present invention, the feedforward transconductance gain of 4 with load current can be varied to achieve the purpose of optimizing power supply rejection ratio in the whole load range.

The present invention, the LDO error amplifier 1 through the feedback resistor 5 and 6 as the feedback voltage with a reference voltage Vref of comparison, and to ensure the feedback voltage node 11 the node 12 is equal to the reference voltage Vref. 1 by the error amplifier MOS transistors 13 to 21 is connected via the circuit constitution. PMOS transistors 15 and 16 constitute a differential pair, NMOS and PMOS transistors 19, 20, 13,17,14,18 tube consisting of three current mirror, PMOS tube 21 mirror-chip current differential pair tail current offer. Inverting terminal of the error amplifier 1 is attached to the feedback voltage node 11, attached to the opposite end of the reference voltage Vref node 12. Source and substrate source NMOS transistors 13,14,17,18 and the substrate is grounded, then the power of the PMOS transistors 19, 20, the substrate and the source of PMOS transistor 15 and 16 are connected to eliminate the effect of partial lining , NMOS drain terminal of the drain pipe 13, PMOS transistors 15 and 16 are respectively connected with the diode-connected. All pipe work in the saturation region.

The present invention, the use of low output impedance buffer 2 of the PMOS transistor gate parasitic transfer tubes 9 3 pole push beyond the LDO loop bandwidth, to ensure system stability. It consists of NMOS transistors 24 ~ 26, PMOS circuit 30 via the pipe 27 to the connection components. Wherein the PMOS transistor 23 is a source follower gate is connected to the output of the error amplifier 1 terminal 8, the source connected to the gate of the PMOS transfer tubes 3 9, PMOS and NMOS transistors 24, 25, 28, 29 pipe for the PMOS transistor 23 provides partial on current, the PMOS and NMOS transistors 24, 25 and tube 27 form a negative feedback to reduce the output impedance of the buffer, the PMOS pipe 30 is connected to a diode 9 is connected to the input of the buffer so that the buffer output impedance of the load current increases and decreases, Paul not only improve the high current efficiency also allows the LDO LDO stability over the entire load range.

The present invention, feedforward transconductance 4 by the NMOS transistors 31 ~ 37, PMOS tube 38 to 43 and resistors 44 and 45 via the electrical connection components. PMOS transistor 40, NMOS tube 35 is the core of their transconductance values increase with increased power. Feedforward transconductance gain is equivalent PMOS transistor 40 and NMOS transistor 35 differential transconductance of the error amplifier output resistance of the product. NMOS transistors 41, 42, 33, 34 and PMOS transistor 40 provides bias for the PMOS transistors, NMOS transistors 31, 32 and PMOS transistors 43 tube current mirror PMOS transfer tubes 3, the PMOS transconductance tube 40 with the load current changes, thereby adjusting the feedforward transconductance gain of the LDO to maintain a high power supply rejection ratio characteristics over the entire load range. NMOS transistors 38, 39, 36, 37 and PMOS current mirror consisting of two mirrored the equivalent transconductance error amplifier output terminal 1 of 8. So that the feed for the first transconductance error amplifier output impedance does not affect the properties, PMOS channel length of pipe 38, 39 is greater than 20μm.

The present invention, the error amplifier from the tail current source, PMOS input differential pair and the current mirror three groups constitute a current mirror amplifier. Effect of supply voltage fluctuations on the output of the main transmission through the parasitic resistance PMOS and PMOS transfer tubes of these two pathways. Feedforward transconductance of the power supply voltage disturbances into electricity disturbance, and then after the error amplifier parasitic resistance transfer tube into the gate of an in-phase voltage disturbances. Through feedforward control transconductance gain completely eliminate disturbances on the output voltage of the power supply, enabling high power supply rejection ratio. Compared to conventional high power supply rejection ratio, low dropout linear regulator circuit, the present invention can achieve higher power supply rejection ratio, power supply rejection ratio optimization does not reduce the low-dropout linear regulator in a wider range of load current efficiency .

BRIEF DESCRIPTION

Figure 1. A with feedforward transconductance high PSRR low-dropout linear regulator (LDO) structure of FIG.

Figure 2 of the present invention applied error amplifier circuits.

Buffer circuit of Figure 3 of the present invention applied to achieve.

Feedforward transconductance circuit in Figure 4 of the present invention designed to achieve.

Explanation of Reference: 1 is a schematic diagram of the error amplifier 2 is a schematic of the buffer, 4 is a diagram of the feedforward transconductance resistor 5,6,44,45, 12,19,20,21,23,28,29, 30,38,39,40,41,42,43 for the PMOS transistor, 13,14,17,18,24,25,26,31,32,33,34,35,36,37 the NMOS transistor 7 compensation capacitor 8 1 output of the error amplifier, the output of buffer 2 to 9, 10 to LDO output terminal voltage feedback terminal 11, 12 of the node of the error amplifier 1 connected to the reference voltage Vref, 22, 45 for the chip the bias voltage input terminal.

detailed description

Below in conjunction with the accompanying drawings of the present invention is further described.

Figure 1 shows the whole with feedforward transconductance high PSRR LDO's structure. , The error amplifier with 1 in FIG. 1 with a feedback voltage input terminal connected to terminal 11, the output of the inverting terminal 1 of 8 with feedforward transconductance output terminal 4 connected to the input buffer 2 is connected reference source Vref, error amplifier, feedforward transconductance 4 input termination power output of the buffer 2 of 9 transfer tubes connected PMOS gate terminal 3, the PMOS transfer tubes termination power source 3, a drain terminal connected to the output of the LDO 10, one end of the feedback resistor in series LDO output 10, the other end. Compensation capacitor 7 a termination LDO output 10, the other end.

Figure 2 shows the error amplifier circuit 1 in Figure 1 implemented. FIG PMOS transistors 15 and 16 constitute a differential pair, NMOS and PMOS transistors 19, 20, 13,17,14,18 tube consisting of three current mirror, PMOS tube 21 external current mirror provides differential pair tail current. Inverting terminal of the error amplifier 1 is attached to the feedback voltage node 11, attached to the opposite end of the reference voltage Vref node 12. Source and substrate source NMOS transistors 13,14,17,18 and the substrate is grounded, then the power of the PMOS transistors 19, 20, the substrate and the source of PMOS transistor 15 and 16 are connected to eliminate the effect of partial lining NMOS transistors 13, 14, the drain drain terminal, PMOS tube 15, 16 are connected to the diode is connected. All pipe work in the saturation region.

Figure 1 shows the buffer circuit of FIG. 2 implementation 3. FIG. 23 is a PMOS transistor source follower gate is connected to the output of the error amplifier 1 terminal 8, a source terminal is connected PMOS transistor gate 93 of the transfer tube, PMOS transistors 28, 29 and NMOS transistors 24 and 25 provide for the PMOS transistor 23 bias current, PMOS and NMOS transistors 24, 25 and tube 27 form a negative feedback to reduce the output impedance of the buffer, PMOS tube 30 is connected to a diode 9 is connected to the input of the buffer. Source and PMOS (27 to 30) connected to the power source and the substrate, PMOS tube (23) of the source and substrate connected PMOS transistor (29) of the drain terminal, NMOS tube (24,25,26) of substrate is grounded.

Figure 4 shows the Figure 1 cross feedforward circuit 4 is implemented. PMOS figure Cascode connection tubes 41, 42 and diode-connected NMOS transistors 33, 34, 40 for the PMOS transistor to provide bias voltage. NMOS transistors 31, 32 and PMOS transistors 43 tube current mirror PMOS transfer tubes 3. NMOS transistors 38, 39, 36, 37 and PMOS current mirror consisting of two mirrored the equivalent transconductance error amplifier output terminal 1 of 8. Wherein, NMOS tube 31,32,33,35,36,37 of the source and the substrate are grounded, PMOS tube 38,39,40,42,43 the source and the substrate are connected to the supply, NMOS source tube 34 terminating the NMOS gate terminal 33, NMOS tube substrate is grounded 34, PMOS tube terminating source PMOS 41 of the drain pipe 42, PMOS substrate connected to the supply pipe. The NMOS and PMOS channel length 36, 37 38, 39 are larger than 20μm, all tubes are working in strong inversion region.

The present invention is achieved with feedforward transconductance high PSRR low-dropout linear regulator with fully compatible with standard CMOS process, the full load range power supply rejection ratio, load current, etc., applicable to a variety of power supply noise sensitive high-precision analog, RF circuits.

The above are only preferred embodiments of the present invention, it should be noted that, without departing from the principles of the present invention, the premise of a number of improvements and modifications made shall also be considered the scope of the present invention.

(19)中华人民共和国国家知识产权局

(12)发明专利申请

(10)申请公布号 CN 101853040 A
(43)申请公布日 2010.10.06

(21)申请号 201010217348.8

(22)申请日 2010.07.05

(71)申请人 复旦大学
地址 200433 上海市杨浦区邯郸路 220 号

(72)发明人 黄圣专 周锋 赵喆

(74)专利代理机构 上海正旦专利代理有限公司 31200
代理人 陆飞 盛志范

(51)Int.Cl.
G05F 1/56(2006.01)

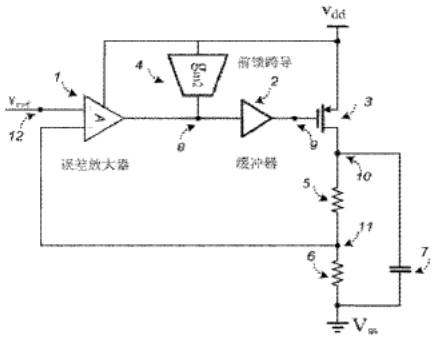
权利要求书 2 页 说明书 3 页 附图 4 页

(54)发明名称

一种带前馈跨导的高电源抑制比低压差线性稳压器

(57)摘要

本发明属集成电路技术领域，具体为一种带前馈跨导的高电源抑制比低压差线性稳压器。它由误差放大器、缓冲器、PMOS 传输管、前馈跨导、两个反馈电阻和滤波电容组成。误差放大器由尾电流源、PMOS 输入差分对以及三组电流镜构成电流镜放大器。电源电压波动对输出的影响主要通过 PMOS 传输管和 PMOS 传输管的寄生电阻这两条通路。前馈跨导将电源电压的扰动转化为电流的扰动，再经过误差放大器的寄生电阻转化为传输管栅极的一个同相电压扰动。通过控制前馈跨导的增益，可消除电源电压扰动对输出的影响，实现高电源抑制比。本发明能在更宽的负载电流范围内优化电源抑制比且不降低低压差线性稳压器的效率。



CN 101853040 A

1. 一种带前馈跨导的高电源抑制比低压差线性稳压器，其特征在于由误差放大器(1)，缓冲器(2)，PMOS 传输管(3)，前馈跨导(4)，2 个串联的反馈电阻(5、6)，片外补偿电容(7)经电路连接构成；其中，误差放大器(1)的同相输入端连接电压反馈端(11)，反相端(12)连基准源 V_{ref}，误差放大器(1)的输出端(8)与前馈跨导(4)的输出端、缓冲器(2)的输入端相连；前馈跨导(4)的输入端接电源，缓冲器(2)的输出端(9)连 PMOS 传输管(3)的栅端，PMOS 传输管(3)的源端接电源，漏端连 LDO 的输出端(10)；反馈电阻串联一端接 LDO 输出(10)，另一端接地；补偿电容(7)一端接 LDO 输出端(10)，另一端接地。

2. 根据权利要求 1 所述的带前馈跨导的高电源抑制比低压差线性稳压器，其特征在于所述的误差放大器电路(1)由 9 个 MOS 管 (13 ～ 21) 经电路连接构成；其中，2 个 PMOS 管 (15、16) 组成差分对，4 个 NMOS 管 (13、17、14、18) 和 2 个 PMOS 管 (19、20) 组成三组电流镜，PMOS 管 (21) 镜像片外电流为差分对提供尾电流；4 个 NMOS 管(13、14、17、18)的源端和衬底接地，3 个 PMOS 管(19、20、21)的源端和衬底接电源，2 个 PMOS 管(15、16)的衬底和源端相连以消除衬偏效应，2 个 PMOS 管(15、16)的漏端分别与二极管连接的 2 个 NMOS 管(13、14)漏端相连。

3. 根据权利要求 1 所述的带前馈跨导的高电源抑制比低压差线性稳压器，其特征在于所述的缓冲器(2)由 3 个 NMOS 管(24 ～ 26)，4 个 PMOS 管(27 ～ 30)经由电路连接组成；其中，PMOS 管(23)是源跟随器，栅极连接误差放大器(1)的输出端(8)，源端连接 PMOS 管传输管(3)的栅极(9)，2 个 PMOS 管(28、29)和 2 个 NMOS 管(24、25)为 PMOS 管(23)提供偏置电流，PMOS 管(27)和 3 个 NMOS 管(24、25、26)构成负反馈降低缓冲器的输出阻抗，PMOS 管(30)二极管连接与缓冲器输入端(9)相连；4 个 PMOS 管(27 ～ 30)的源端和衬底接电源，PMOS 管(23)的源端和衬底接 PMOS 管(29)的漏端，3 个 NMOS 管(24、25、26)的源端和衬底接地。

4. 根据权利要求 1 所述的带前馈跨导的高电源抑制比低压差线性稳压器，其特征在于所述的前馈跨导(4)由 7 个 NMOS 管(31 ～ 37)，6 个 PMOS 管(38 ～ 43)和 2 个电阻(44、45)经电路连接组成；其中，Cascode 连接的 2 个 PMOS 管(41、42)和二极管连接的 2 个 NMOS 管(33、34)，为 PMOS 管(40)提供偏置电压；2 个 NMOS 管(31、32)和 PMOS 管(43)镜像传输管 PMOS 管(3)的电流；2 个 NMOS 管(36、37)和 2 个 PMOS 管(38、39)组成两组电流镜，将等效跨导镜像到误差放大器(1)的输出端(8)；6 个 NMOS 管(31、32、33、35、36、37)的源端和衬底都接地，5 个 PMOS 管(38、39、40、42、43)的源端和衬底都接电源，NMOS 管(34)的源端接 NMOS 管(33)的栅端，NMOS 管(34)的衬底接地，PMOS 管(41)的源端接 PMOS 管(42)的漏端，PMOS 管(41)的衬底接电源。

5. 根据权利要求 4 所述的带前馈跨导的高电源抑制比低压差线性稳压器，其特征于所述的前馈跨导(4)中，PMOS 管(40)和 NMOS 管(35)的跨导值都随电源电压增加而增加，前馈跨导的等效增益是 PMOS 管(40)和 NMOS (35)的跨导之差与误差放大器的输出电阻的乘积；通过 PMOS 管(43)和 2 个 NMOS 管(31、32)，前馈跨导的增益随负载电流变化而变化，使 LDO 在全负载范围内保持高电源抑制比的特性。

6. 根据权利要求 4 所述的带前馈跨导的高电源抑制比低压差线性稳压器，其特征在于，2 个 PMOS 管(38、39)的沟道长度不小于 20μm；2 个 NMOS 管(36、37)的沟道长度不小于 10μm。

Aptiv Services US, LLC Exhibit 1003 Page 34

7. 根据权利要求 4 所述的带前馈跨导的高电源抑制比低压差线性稳压器，其特征在于 PMOS 管（40）和 NMOS 管（35）的沟道长度不小于 20 μm。

Aptiv Services US, LLC Exhibit 1003 Page 35

一种带前馈跨导的高电源抑制比低压差线性稳压器

技术领域

[0001] 本发明属于集成电路技术领域，具体涉及一种带前馈跨导的高电源抑制比低压差线性稳压器（LDO）。

背景技术

[0002] [0002]LDO 是电源管理中的核心模块，主要为模拟电路和射频电路提高等噪声敏感电路提供电源。因此，电源抑制比是其关键性能参数之一。

[0003] 目前，多数商用高电源抑制比 LDO 芯片采用 LDO 级联，此种方案直接导致 LDO 效率低下。虽然近年来，论文中出现许多高电源抑制比 LDO 解决方案，但是它们大都以增加输出输出电压噪声、增加电路复杂度和较低负载电流为代价。

[0004] 所以，设计一种不以增加输出电压噪声为代价，电路结构简单，能提供较大的负载电流的高电源抑制比具有较大的应用意义。

发明内容

[0005] 为了解决上述问题，本发明提出了一种基于前馈跨导的高电源抑制比 LDO。本发明所提出前馈跨导方法保持 LDO 的高效率、低噪声等性能，电路结构简单且能使 LDO 在整个负载电力范围内得到较高的电源抑制比。

[0006] 本发明提出的基于前馈跨导的高电源抑制比的 LDO，由误差放大器 1，缓冲器 2，PMOS 传输管 3，前馈跨导 4，2 个串联的反馈电阻 5、6，片外补偿电容 7 经电路连接构成；其中，误差放大器 1 的同相输入端连接电压反馈端 11，反相端连基准源 V_{ref}，误差放大器 1 的输出端 8 与前馈跨导 4 的输出端、缓冲器 2 的输入端相连；前馈跨导 4 的输入端接电源，缓冲器 2 的输出端 9 连 PMOS 传输管 3 的栅端，PMOS 传输管 3 的源端接电源，漏端连 LDO 的输出端 10；反馈电阻串联一端接 LDO 输出 10，另一端接地；补偿电容 7 一端接 LDO 输出端 10，另一端接地。

[0007] 本发明中前馈跨导 4 将电源上电压的波动转换成电流的波动，再通过误差输出寄生电阻转化为 PMOS 传输管 3 栅极的同相电压波动，抵消电源电压在传输管源端的波动对输出电压的影响。在不同的负载电流情况，所需跨导增益不同。在本发明中，前馈跨导 4 的增益能随负载电流变化，以达到在全负载范围内优化电源抑制比的目的。

[0008] 本发明中，误差放大器 1 将 LDO 通过反馈电阻 5、6 所反馈的电压与基准电压 Vref 比较，保证反馈电压节点 11 与基准电压 V_{ref} 节点 12 相等。误差放大器 1 由 MOS 管 13 ～ 21 经电路连接构成。PMOS 管 15、16 组成差分对，NMOS 管 13、17、14、18 和 PMOS 管 19、20 组成三组电流镜，PMOS 管 21 镜像片外电流为差分对提供尾电流。误差放大器 1 的同相端连着反馈电压节点 11，反向端连着基准电压 V_{ref} 节点 12。NMOS 管 13、14、17、18 的源端和衬底接地，PMOS 管 19、20、21 的源端和衬底接电源，PMOS 管 15、16 的衬底和源端相连以消除衬偏效应，PMOS 管 15、16 的漏端分别与二极管连接的 NMOS 管 13、14 漏端相连。所有管子工作于

Aptiv Services US, LLC Exhibit 1003 Page 36

饱和区。

[0009] 本发明中，利用缓冲器 2 的低输出阻抗将 PMOS 管传输管 3 栅极 9 的寄生极点推到 LDO 环路带宽以外，保证系统稳定。它由 NMOS 管 24 ～ 26，PMOS 管 27 ～ 30 经由电路连接组成。其中 PMOS 管 23 是源跟随器，栅极连接误差放大器 1 的输出端 8，源端连接 PMOS 管传输管 3 的栅极 9，PMOS 管 28、29 和 NMOS 管 24、25 为 PMOS 管 23 提供偏置电流，PMOS 管 27 和 NMOS 管 24、25、26 构成负反馈降低缓冲器的输出阻抗，PMOS 管 30 二极管连接与缓冲器输入端 9 相连使缓冲器输出阻抗随负载电流增大而减小，既保提高了 LDO 的高电流效率又使 LDO 在整个负载范围内稳定。

[0010] 本发明中，前馈跨导 4 由 NMOS 管 31 ～ 37、PMOS 管 38 ～ 43 和电阻 44、45 经电路连接组成。PMOS 管 40、NMOS 管 35 是核心，它们的跨导值都随电源增加而增加。前馈跨导的等效增益是 PMOS 管 40 和 NMOS 管 35 的跨导之差与误差放大器 1 输出电阻的乘积。NMOS 管 33、34 和 PMOS 管 41、42 为 PMOS 管 40 提供偏置，NMOS 管 31、32 和 PMOS 管 43 镜像传输管 PMOS 管 3 的电流，使 PMOS 管 40 的跨导随负载电流变化，从而调整前馈跨导的增益，使 LDO 在全负载范围内保持高电源抑制比的特性。NMOS 管 36、37 和 PMOS 管 38、39 组成两组电流镜将等效跨导镜像到误差放大器 1 的输出端 8。为使前馈跨导的输出阻抗不影响误差放大器的特性，PMOS 管 38、39 的沟道长度要大于 20μm。

[0011] 本发明中，误差放大器由尾电流源、PMOS 输入差分对以及三组电流镜构成电流镜放大器。电源电压波动对输出的影响主要通过 PMOS 传输管和 PMOS 传输管的寄生电阻这两条通路。前馈跨导将电源电压的扰动转化为电流的扰动，再经过误差放大器的寄生电阻转化为传输管栅极的一个同相电压扰动。通过控制前馈跨导的增益，达到完全消除电源电压扰动对输出的影响，从而实现高电源抑制比。相比以往的高电源抑制比低压差线性稳压器电路，本发明能达到更高的电源抑制比，在更宽的负载电流范围内优化电源抑制比且不降低低压差线性稳压器的效率。

附图说明

[0012] 图 1 一种带前馈跨导的高电源抑制比低压差线性稳压器（LDO）的结构图。

[0013] 图 2 本发明中应用的误差放大器的电路实现。

[0014] 图 3 本发明中应用的缓冲器的电路实现。

[0015] 图 4 本发明中设计的前馈跨导的电路实现。

[0016] 标号说明：1 为误差放大器的示意图，2 为缓冲器的示意图，4 为前馈跨导的示意图，5、6、44、45 为电阻，12、19、20、21、23、28、29、30、38、39、40、41、42、43 为 PMOS 管，13、14、17、18、24、25、26、31、32、33、34、35、36、37 为 NMOS 管，7 为补偿电容，8 为误差放大器 1 输出端，9 为缓冲器 2 输出端，10 为 LDO 输出端，11 为电压反馈端，12 为误差放大器 1 与基准电压 V_{ref} 连接的节点，22、45 为片外偏置电压输入端。

具体实施方式

[0017] 下面结合附图进一步描述本发明。

[0018] 图 1 所示为整个带前馈跨导高电源抑制比 LDO 的结构图。图 1 中，误差放大器 1 的同相输入端连接电压反馈端 11，反相端连基准源 V_{ref}，误差放大器 1 的输出端 8 与前馈跨

Aptiv Services US, LLC Exhibit 1003 Page 37

导 4 的输出端、缓冲器 2 的输入端相连，前馈跨导 4 的输入端接电源，缓冲器 2 的输出端 9 连 PMOS 传输管 3 的栅端，PMOS 传输管 3 的源端接电源，漏端连 LDO 的输出 10，反馈电阻串联一端接 LDO 输出 10，另一端接地。补偿电容 7 一端接 LDO 输出端 10，另一端接地。

[0019] 图 2 所示为图 1 中误差放大器 1 的电路实现。图中 PMOS 管 15、16 组成差分对，NMOS 管 13、17、14、18 和 PMOS 管 19、20 组成三组电流镜，PMOS 管 21 镜像外部电流为差分对提供尾电流。误差放大器 1 的同相端连着反馈电压节点 11，反向端连着基准电压 Vref 节点 12。NMOS 管 13、14、17、18 的源端和衬底接地，PMOS 管 19、20、21 的源端和衬底接电源，PMOS 管 15、16 的衬底和源端相连以消除衬偏效应，PMOS 管 15、16 的漏端分别与二极管连接的 NMOS 管 13、14 漏端相连，。所有管子工作于饱和区。

[0020] 图 3 所示为图 1 中缓冲器 2 的电路实现。图中 PMOS 管 23 是源跟随器，栅极连接误差放大器 1 的输出端 8，源端连接 PMOS 管传输管 3 的栅极 9，PMOS 管 28、29 和 NMOS 管 24、25 为 PMOS 管 23 提供偏置电流，PMOS 管 27 和 NMOS 管 24、25、26 构成负反馈降低缓冲器的输出阻抗，PMOS 管 30 二极管连接与缓冲器输入端 9 相连。PMOS 管（27 ～ 30）的源端和衬底接电源，PMOS 管（23）的源端和衬底接 PMOS 管（29）的漏端，NMOS 管（24、25、26）的源端和衬底接地。

[0021] 图 4 所示为图 1 中前馈跨 4 的电路实现方式。图中 Cascode 连接的 PMOS 管 41、42 和二极管连接的 NMOS 管 33、34，为 PMOS 管 40 提供偏置电压。NMOS 管 31、32 和 PMOS 管 43 镜像传输管 PMOS 管 3 的电流。NMOS 管 36、37 和 PMOS 管 38、39 组成两组电流镜将等效跨导镜像到误差放大器 1 的输出端 8。其中，NMOS 管 31、32、33、35、36、37 的源端和衬底都接地，PMOS 管 38、39、40、42、43 的源端和衬底都接电源，NMOS 管 34 的源端接 NMOS 管 33 的栅端，NMOS 管 34 的衬底接地，PMOS 管 41 的源端接 PMOS 管 42 的漏端，PMOS 管的衬底接电源。NMOS 管 36、37 和 PMOS 管 38、39 的沟道长度都大于 20 μ m，所有管子都工作于强反型区。

[0022] 本发明所实现的带前馈跨导的高电源抑制比低压差线性稳压器具有完全与标准 CMOS 工艺兼容、全负载范围内电源抑制比高，负载电流大等优点，适用于个各种对电源噪声敏感的高精度模拟、射频电路。

[0023] 以上所述仅是本发明的优选实施方式，应当指出，在不脱离本发明原理的前提下，所作出的若干改进和润饰也应视为本发明的保护范围。

Aptiv Services US, LLC Exhibit 1003 Page 38

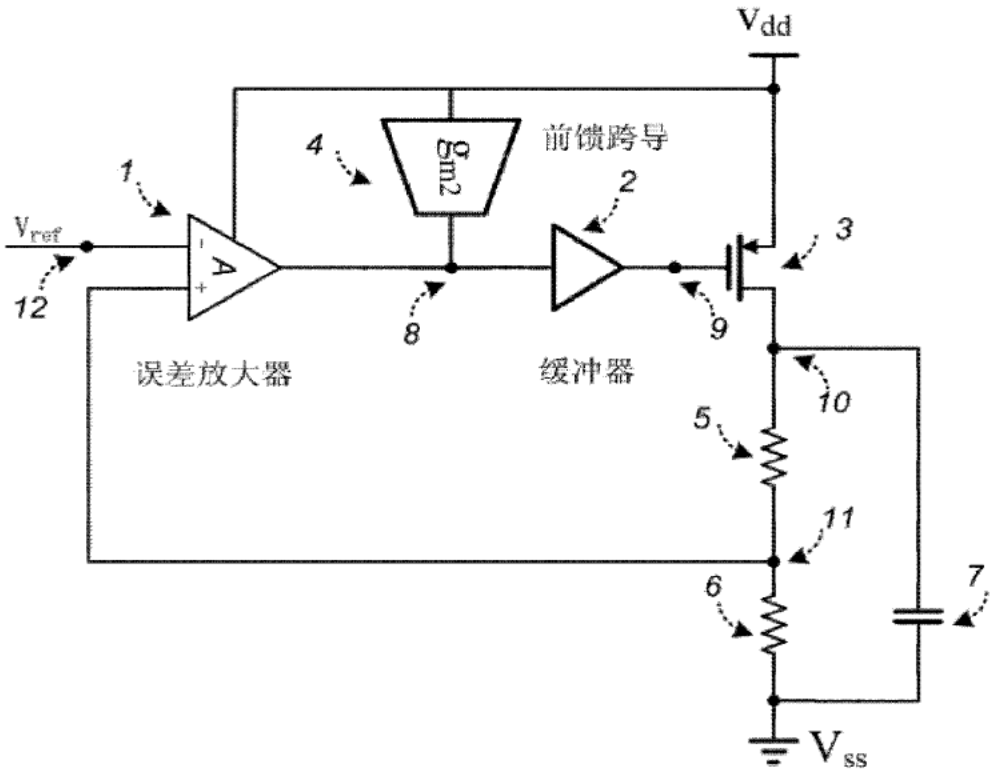


图 1

Aptiv Services US, LLC Exhibit 1003 Page 39

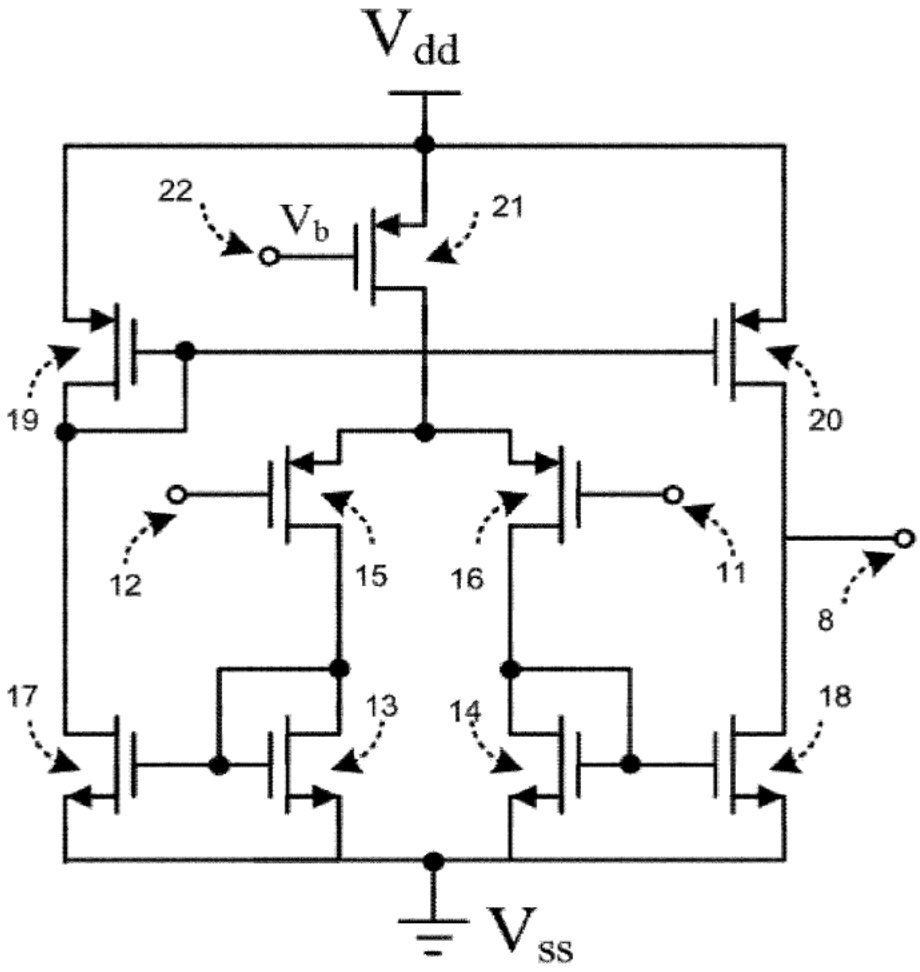


图 2

Aptiv Services US, LLC Exhibit 1003 Page 40

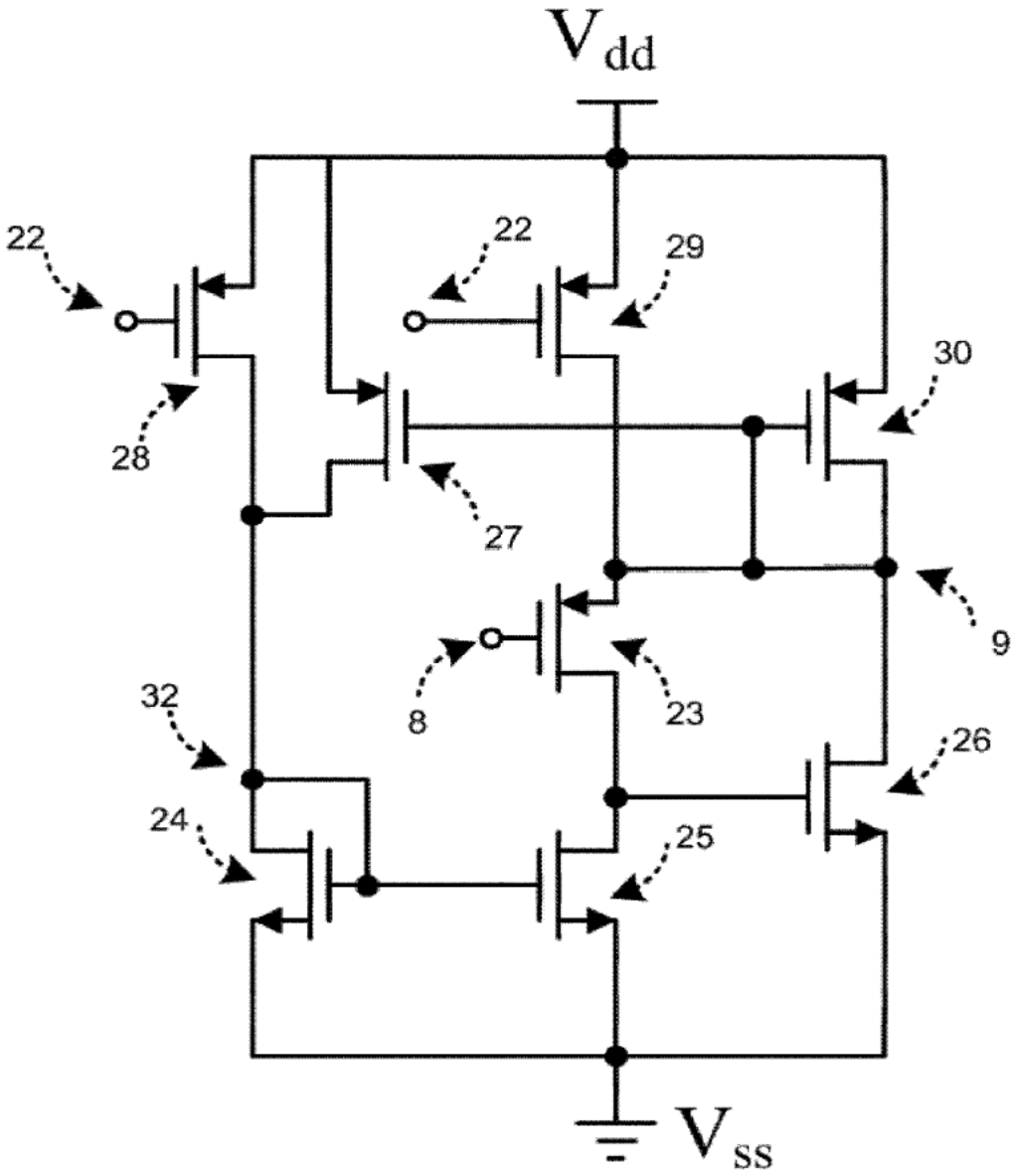


图 3

Aptiv Services US, LLC Exhibit 1003 Page 41

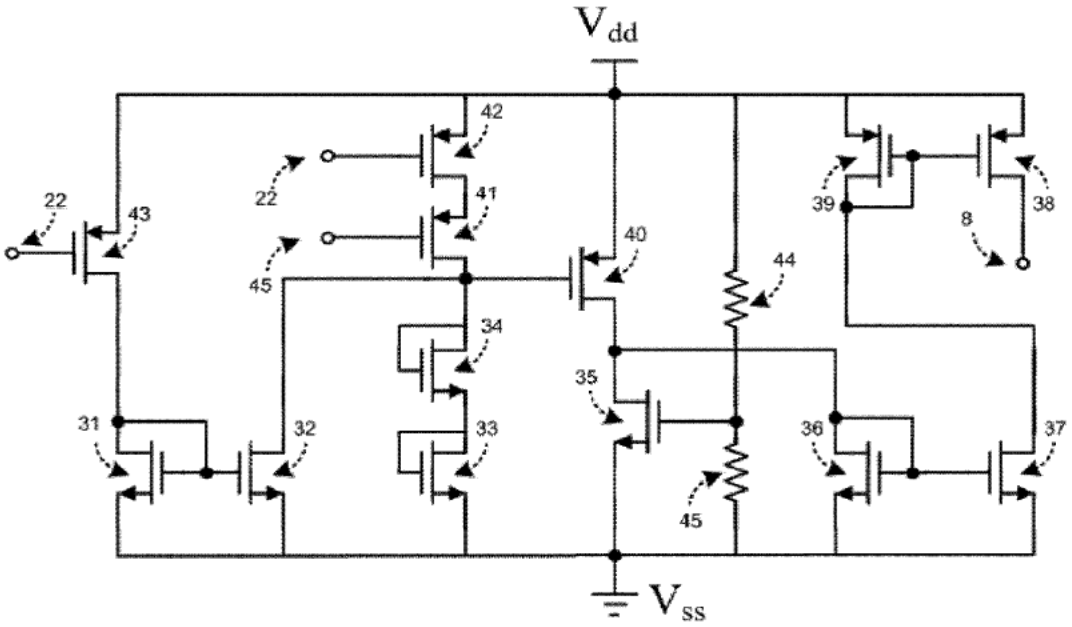


图 4

Aptiv Services US, LLC Exhibit 1003 Page 42

Espacenet

Bibliographic data: CN102915061 (A) — 2013-02-06

Low-voltage stabilizer for ultra-low static current

Inventor(s): HU SHUYUN ± (HU SHUYUN)

Applicant(s): SHENZHEN HUICHUN TECHNOLOGY CO LTD ± (SHENZHEN HUICHUN TECHNOLOGY CO.,LTD)

Classification: **- international:** ***G05F1/56***
- cooperative:

Application number: CN20111224037 20110805

Priority number (s): CN20111224037 20110805

Also published as: CN102915061 (B)

Abstract of CN102915061 (A)

The invention relates to a low-voltage stabilizer for ultra-lower static current, which comprises an error amplification circuit, an output circuit, a voltage feedback circuit, a compensation circuit and a current feedback device, wherein an input end VI of the current feedback device is connected with the input end of the output circuit, the current feedback device is used for transforming voltage VI input by the output circuit into current I01 fed back to a ground end of the error amplification circuit; when the stabilizer suffers a heavy load, the feedback current I01 is increased, and the current of the ground end of the error amplification circuit is also increased, and the response speed of the error amplification current is increased;; and when the stabilizer suffers a light load, the feedback current I01 of the current feedback device is reduced, the bias current of the ground end of the error amplification circuit is also reduced, and the consumption of the low-voltage stabilizer is in a static current state. The low-voltage stabilizer has the advantages that after adopting a dynamic current feedback device, the static current of the low-voltage stabilizer can be lower than 1 microampere, and the low-voltage stabilizer has incomparable technical advantages than other traditional low-voltage stabilizers.

Aptiv Services US, LLC Exhibit 1003 Page 43

Patent Translate
Powered by EPO and Google

Notice

This translation is machine-generated. It cannot be guaranteed that it is intelligible, accurate, complete, reliable or fit for specific purposes. Critical decisions, such as commercially relevant or financial decisions, should not be based on machine-translation output.

DESCRIPTION CN102915061

One kind of extremely low quiescent current LDO, including error amplifier, the output circuit, a voltage feedback circuit and compensation circuit; feedback means further comprises a current input terminal V access to the means of the output current feedback input circuit end, that is, the current feedback circuit means output voltage V input into a current I is fed back to the error amplifier circuit ground terminal, when the regulator in heavy load, the feedback current I is increased, the error amplifying circuit ground current also increased, which improves the response speed of the error amplifying circuit; regulator when the load is light, the feedback current Io1 current feedback means becomes smaller, the error amplifying circuit a ground terminal of the bias current is reduced, so that the regulator's low quiescent low current consumption in the state. The beneficial effects of the present invention are: the use of dynamic current feedback device of the present invention, after the proposed LDO quiescent current at light loads and during sleep can be less than 1μA, having other existing LDO unmatched technological superiority.

Very low quiescent current LDO

The present invention relates to a low-dropout regulator, and more particularly to a collector circuit chip LDO, particularly, to a very low quiescent current LDO.

With the development of semiconductor integrated circuits, integrated circuit chips used in more advanced technology, the chip circuitry required supply voltage and chip input power voltage is typically inconsistent, in most cases the internal circuitry of the chip required supply voltage is low the chip supply voltage input, which requires the chip integrates a low dropout regulator, the chip input supply voltage into an internal power supply voltage required for other circuits. Such low dropout regulators in other circuits to provide power for self-consumption also need less current, particularly in the sleep circuit chip, low-dropout voltage regulator current consumption as low as possible.

Art LDO for stability at work, usually quiescent current design is relatively large, usually more than 10μA, so much so that the class quiescent current LDOs not energy during sleep. In order to save energy, some LDO uses a control terminal to control the LDO work on and off: the chip will work through the open control terminal low dropout regulator; the chip will sleep Low Dropout Regulators closed. Such control end by internal digital circuits controlled by a digital circuit and power supply LDO output supplying. When the digital closed circuit LDO, the LDO can not give the digital circuitry, digital circuitry, no power can not wake up LDO, low dropout regulator so in a state of sleep and wake exists between a self-locking mechanism, how to break this self-locking mechanism is a very complicated matter, need a lot of control circuit designed for this purpose, when the control circuit design, it might cause unsuccessful; and low-dropout regulator closed memory status in digital circuits are lost after the wake of these states and the need to re-set.

The technical problem to be solved by the invention of the present invention is to avoid the shortcomings of the prior art and to provide a very low quiescent current low dropout regulator, to solve the prior art LDO sleep or light-load power consumption big problem.

The present invention solves the technical problem is solved by the following technical solution to achieve, to design a very low quiescent current LDO, including error amplifier, the output circuit, a voltage feedback circuit and compensation circuit; the error amplifier circuit the difference between the reference voltage V ref and the voltage feedback circuit feedback voltage V fb sent from an amplifier to the input terminal of said output circuit; said feedback circuit is a voltage output circuit output voltage V out fed back to the error amplifier circuit ; the compensation circuit is connected across the output terminal of the error amplifier

circuit and the output circuit of the output terminal; in particular, also includes a current feedback means, the input terminal VI of the current feedback means connected to the output circuit input terminal, i.e. the output of the current feedback circuit means input voltage VI into a current I O1 is fed back to the ground terminal of the error amplifier circuit, when the regulator is under heavy load, the feedback current I O1 is increased, then the error amplifier circuit ground currents also increased to improve the response speed of the error amplifier circuit; when the regulator is light loads, the current feedback device feedback current I O1 becomes smaller, the error amplifying circuit ground terminal of the bias current is reduced such that the LDO quiescent low current consumption in the state.

The LDO also includes a buffer circuit, the buffer circuit is connected in series between the error amplifier circuit and the output circuit; the buffer circuit of the error amplifier output voltage to pan and / or follow the treatment to the output input of the circuit; the output of said current feedback means of feedback current I O2 delivery to the ground terminal of the buffer circuit.

Said current feedback means comprises a voltage / current converter and a current mirror; the voltage / current converter connected to the input of VI in the output circuit of the input, the output is about input voltage VI to current converter circuit, sending to the input of the voltage / current converter connected to the current mirror I in, the current through the current mirror copy I O1, I O2.

The voltage / current converter which includes a resistor R4 and a P-type MOS field effect transistor Q 2, the resistor R 4 is connected across the LDO power V IN and the source of the field effect transistor Q 2 between the poles ; the gate and drain of the field effect transistor Q 2 are connected the four voltage / current switch input terminal VI and the output terminal IO.

Said current mirror comprises an N-type MOS field-effect transistors Q3, Q4 and Q5; of the field effect transistors Q3, Q4 and Q5 is parallel ground source, the transistor Q3 is connected to the drain and the gate of the said voltage / current converter connected to an output terminal IO; of the field effect transistors Q4, Q5 image composition means, connected in parallel between the gate electrode, and then connecting the gate of the field-effect transistor Q3; said mirror means to the input current I respectively, in proportion to copy and redistribute to the current mirror output port I O1, or / and I O2, the current I in the proportion of redistribution, Q5 and Q3 size ratio is determined by the field-effect transistor Q4.

The op-amp error amplifier ground terminal 1 via a bias current source I 1 is grounded, so that the bias current source I 1 flows grounded; the current output feedback means feedback current to said current I O1 source I 1 inflow end.

The op amp buffer circuit ground terminal 2 via a bias current source I 2 is grounded, so that the bias current source I 2 flowing grounded; the output current feedback means feedback current I O2 to the current source I 2 of the inflow end.

Compared with the prior art, the beneficial effects of the present invention is: A method to achieve dynamic current feedback device, real-time monitoring of the device LDO output current, the output current is adjusted according to the size of LDO bias current to achieve both under heavy load drive capability is very strong, but also at light load or very low quiescent current sleep, very energy efficient; and LDO without sleep / wake control terminal, there is no existing self-locking technology issues LDO sleep / wake; because the LDO has been working, the output current persists, and therefore the state of memory in a digital circuit is not lost. Compared with other existing LDO, dynamic current feedback device of the present invention, after the proposed LDO quiescent current at light loads and during sleep can be less than 1μA, having other existing LDO is unmatched technological superiority.

Figure 1 of the present invention is a low-voltage low dropout regulator quiescent current of the logical structure of the preferred embodiment of the schematic;

Figure 2 is a current feedback means 60 of the preferred embodiment an electrical schematic diagram of embodiment;

Figure 3 is a current feedback means 60 of the second electrical schematic diagram of the preferred embodiment implementation;

Figure 4 is a preferred embodiment of the current feedback structure schematic logic device 60;

Figure 5 is a schematic diagram of a circuit 61 in the case of the preferred embodiment of the voltage converter;

FIG 6 is a circuit schematic of the preferred embodiment of the current mirror 62.

DETAILED DESCRIPTION Hereinafter, with reference to preferred embodiments illustrated in the drawings of the present invention is illustrated further.

See Figure 1-2, the preferred embodiment of the present invention, one A low quiescent current LDO, including error amplifier 10, the output circuit 30, a voltage feedback circuit 40 and compensation circuit 50; the error a difference amplifying circuit 10 and the reference voltage V REF voltage feedback circuit 40 is sent to the feedback voltage V FB output of the amplifying circuit 30 is supplied to the input terminal; said voltage feedback circuit 40 to the output circuit 30 is the output voltage V out feedback to the error amplifying circuit 10; and the compensation circuit 50 is connected across the output terminal of the error amplifying circuit 10 and the output terminal of the output circuit 30; a current feedback means further comprises a buffer circuit 60 and 20, the buffer circuit 20 connected in series between the error amplifying circuit 10 and an output circuit 30; after the buffer circuit 20 to the error amplifier output voltage translation circuit 10 and / or follow the process to the input of the output circuit 30; the said current feedback input device 60 inputs the output Vl of the access circuit 30, the output of the current feedback means 60 of conveying feedback current I O1 and I O2 are respectively supplied to the error amplifying circuit 10 and buffer circuit ground 20 end; when the regulator is in a heavy load, the feedback current I O1 and I O2 is increased, the error amplifying circuit 10 and buffer circuit 20 is a ground terminal of each current also increases, thereby increasing the error 10 and the response speed of the buffer circuit 20 of the amplifier circuit; when the regulator is light loads, the current feedback device 60 feedback current I O1 and I O2 becomes smaller, the error amplifier ground circuit 10 and buffer circuit 20 end of the bias current is reduced, so that the regulator's low quiescent low current consumption in the state.

In conjunction with Figure 2, Figures 4 to 6, the preferred embodiment, the function of each circuit component are as follows:

The op-amp error amplifier ground terminal 10 1 via a bias current source I 1 to ground, that the bias current source I 1 flows grounded, the injection end through a line connected to the op-amp network n3 1 to end; the bias current source I 1 1 to provide the most basic op amp bias current to ensure that the operational amplifier 1 in LDO is able to operate at light load or sleep. The means 60 feedback current I O1 of feedback current delivered to the inflow end of the current source I 1.

The buffer amplifier circuit 20 of the ground terminal 2 via a bias current source I 2 ground that the bias current source I 2 flows grounded, which is connected to the inflow end to end operational amplifier 2 through wire mesh n2 , 2 provides the most basic to the op amp bias current to ensure that the operational amplifier 2 in LDO is able to operate at light load or sleep. The current feedback means 60 outputs the feedback current I O2 to the injection end of the current source I 2.

An operational amplifier as the error amplifier, its negative input connected to a reference power source V ref, the output voltage of the positive input of the feedback circuit 50 through the terminal resistor R wire net n5 1, R 2. 1 op amp feedback voltage V fb and V ref with the difference to be drawn error correction voltage amplification, and then transmitted to the error correction voltage op amp buffer circuit 20 2. 2 is a buffer amplifier, op amp which an error correction voltage output from the voltage follower, the voltage may be necessary to follow the translational movement of the voltage follower, and then through the wire mesh n1 to the output circuit 30, the Q output of the power transistor 1 gate. The op amp output drive capability 2 is stronger

than the op amp output drive dynamic capability 1, an order of magnitude or more, the output power transistor Q gate capacitance of a relatively large, the op amp input 2 parasitic capacitance is relatively small, so transport put 2 isolation amplifier case directly drive large capacitive loads of 1, greatly improving the ability to respond to the high frequency amplifier 1, and the operational amplifier 2 because of their relatively strong drive capability, even if the gate drive output of the power transistor Q 1 the case of the capacitor is still better than its frequency response amplifier 1 several times faster.

Output power transistors Q 1 using PMOS (P-type metal - oxide semiconductor) having a gate connected to the output of the operational amplifier 2, a source connected to power supply V In, a drain connected LDO output V out. Voltage feedback circuit 50 by the dividing resistors R 1, R 2 composition, the V out voltage proportional feedback to the positive input of the operational amplifier 1. Figure 2 shows, the output voltage of the op amp 1 changes LDO output voltage V out of the relationship is the same, the op amp output voltage of the op amp output 2 voltage to 1 is the same relationship, the output power transistors Q drain voltage and the gate voltage variation 1 is an inverse relationship, so the LDO voltage feedback loop is negative feedback, LDO real-time correction of the output voltage V out , so that the output voltage V out and the reference voltage V ref maintaining a constant voltage proportional relationship.

The output power transistors Q 1 size design is relatively large, and thus a strong drive capability, so that regardless of the load is heavy load (load resistor RL small value) or light load (resistance load resistor RL large), the output voltage V out all remains substantially constant, the error will not be much.

Current feedback means 60 via line network n1 sampling gate voltage output power transistors Q 1 and the voltage into a current, an output current I O2 which is connected to the amplifier ground terminal 2 through the wire mesh n2, another unit output current I O1 connected by wire to the op amp network n3 ground terminal 1. When the LDO load becomes heavy, the output voltage V out will be slightly lowered by the voltage negative feedback loop so that the gate voltage of the power transistor Q 1 becomes low, while the output current of the power transistor Q 1 increases, boycott output voltage V out goes low because the gate voltage of the power transistor Q 1 becomes low, the output current of the current feedback device is increased to improve the op amp bias current operational amplifier 1 and 2, thereby improving the operational amplifier 1 and the response speed of the operational amplifier 2, the response speed of the system also will be increased. Conversely, when the LDO load becomes lighter, the gate voltage of the power transistor Q 1 becomes high, the output current of the current feedback device becomes smaller, the op amp bias current operational amplifier 1 and 2 is reduced, the entire system quiescent current consumption is reduced in order to achieve a low dropout voltage regulator in heavy load fast response at light load quiescent current is low, and without increasing the LDO control port. Join current feedback device such LDO both energy-saving and efficient, is a simple and efficient means.

Figure 3 resistor R 3 and capacitor C 2 constitute a stability compensation circuit 40, one end of the capacitor C voltage output V out 2, the other end of resistor R 3, the other end of the resistor R 3 is connected through a wire mesh n4 op 1 output. Resistor R 3 and capacitor C 2 is in effect when the system is heavily loaded compensate the op amp output pole 1 so that the output of op amp output pole 1 pole for the first secondary pole while the pole falls by the capacitor C 1 and a resistor nearby R es composed of zero poles and zeros close to each other to form a dipole, interaction offset frequency domain. Capacitor C 1 is the output voltage V out of the stable capacitance, while the main system falls pole output stage, resistor R es is the equivalent capacitance C 1 of the series resistor and capacitor C 1 R es together constitute the output voltage stabilizing circuit . R L is the load resistance.

See Figure 4, the present invention 3 in view of a current feedback device 60 to achieve a functional block diagram. Current feedback means 60 consists of two parts means: part of the apparatus of the voltage / current converter 61, the port from which the current feedback VI means converts the voltage to the output current I o, and another portion of the current mirror device 62; the input 61 of the current mirror copying and redistribution of the current I in and are output to the port current feedback device 60 I O1 and I O2.

Refer to FIG. 5, the invention of FIGURE 3 is a voltage / current converter 60 one specific embodiment of the circuit, which consist of two components: the resistor R 4 and the PMOS transistor Q 2. One end of resistor R 4 power supply V In, the other end of the PMOS transistor Q 2 source electrode, the gate and drain of PMOS transistor Q 2 are connected to the voltage / current converter V I port and I O. Resistor R 4 function acts as a current limiting device, the drain current in the PMOS transistor Q 2 is relatively small, the resistance R 4 almost does not work, can be ignored as a wire, then drain current of the PMOS transistor Q 2 by transconductance gm 2 decision, the drain current Id 2 ≈gm 2 * Vgs 2, Vgs 2 for the PMOS transistor Q 2 gate-source voltage difference; drain current in the PMOS transistor Q 2 is relatively large, the resistance R 4 play a negative feedback, limiting the drain current of the PMOS transistor Q 2 growth, in which case the drain current of the PMOS transistor Q 2 is decided by the transconductance of Gm 2, 2 of Gm formula:

[image]

GMB is 2 and the drain of PMOS transistor Q 2 is the transconductance of the substrate

The PMOS transistor Q 2, the drain current Id 2 ≈Gm 2 * Vgs 2, due to the addition of 4 R, making the PMOS transistor Q 2 at high currents drain current role gm 2 Dui weakened, limiting the drain current unlimited increases, ultimately limits the voltage / current converter maximum output current. Output current I O = -Id 2, so the gate voltage of the PMOS transistor Q 2 becomes low, the output current I O becomes larger; otherwise contrary.

Refer to FIG. 6, the present invention is a specific circuit diagram of an embodiment 4 in the current mirror 62 comprising components: NMOS tube Q 3, Q 4, Q 5. NMOS transistor Q 3 port to accept the current mirror input current I in and through the mirror means comprises NMOS transistors Q 4, Q 5, respectively, consisting of a current copy and redistribute by a certain percentage to the current mirror output port I O1 and I O2 current redistribution ratio is determined by the ratio of the size of the NMOS transistor Q 4 and Q 5 and Q 3 in. Of which only two cases mark the output current, in accordance with the present invention, one or two or more output currents are possible; the figure using only a single MOS current mirror to produce, according to the present invention, designed to be easily cascaded MOS the way to make the current mirror. These are within the scope of protection of this patent.

1 and 3, the preferred embodiment of the present invention, two with an instance of the exception that the low quiescent current LDO input VI no access buffer 20, current feedback device 60 the input of the circuit 30 is output, i.e., the current feedback circuit 60 sets the output 30 of the input voltage VI is converted into a current I O1 is fed back to the ground terminal of the error amplifying circuit 10, the regulator when the heavy loads the feedback current I O1 increases, the error amplifier circuit 10 ground current also increases, which improves the response speed of the error amplifier circuit 10; when the regulator is light load, the current feedback device 60 feedback current I O1 becomes smaller, the ground terminal of the error amplifier bias current circuit 10 is also reduced, so that the regulator's low quiescent low current consumption in the state.

In this example embodiment of the current feedback circuit 60 of the apparatus may be employed in the instance of a program, current mirror 62 is used to make a single MOS current mirror to which the present technical field of ordinary skill in one embodiment in conjunction very obvious, not repeat them here.

(19)中华人民共和国国家知识产权局

(12)发明专利申请

(10)申请公布号 CN 102915061 A
(43)申请公布日 2013.02.06

(21)申请号 201110224037.9

(22)申请日 2011.08.05

(71)申请人 深圳市汇春科技有限公司
地址 518057 广东省深圳市南山区科技园北区松坪山5号嘉达研发大楼B座六楼

(72)发明人 胡术云

(74)专利代理机构 深圳市睿智专利事务所 44209
代理人 林青 陈鸿荫

(51)Int.Cl.
G05F 1/56(2006.01)

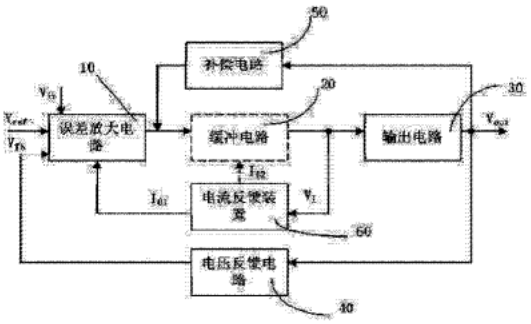
权利要求书 1 页 说明书 5 页 附图 3 页

(54)发明名称

极低静态电流的低压降稳压器

(57)摘要

一种极低静态电流的低压降稳压器，包括误差放大电路、输出电路、电压反馈电路和补偿电路；还包括电流反馈装置，该电流反馈装置的输入端 V_I 接入所述输出电路的输入端，即该电流反馈装置将输出电路输入的电压 V_I 转换成电流 I_{01} 反馈到所述误差放大电路的接地端，当所述稳压器在重负载时，该反馈电流 I_{01} 增大，则所述误差放大电路接地端的电流也随之增大，提高了该误差放大电路的响应速度；当所述稳压器为轻负载时，该电流反馈装置的反馈电流 Io1 变小，所述误差放大电路的接地端之偏置电流也减小，使得所述低稳压器的消耗处于静态低电流状态。本发明的有益效果是：采用本发明提出的动态电流反馈的装置后的低压降稳压器在轻负载和睡眠时的静态电流能低于 1μA，具有现有其它低压降稳压器无可比拟的技术优势。



CN 102915061 A

1. 一种极低静态电流的低压降稳压器，包括误差放大电路（10）、输出电路（30）、电压反馈电路（40）和补偿电路（50）；所述误差放大电路（10）将参考电压 V_{ref} 与电压反馈电路（40）送来的反馈电压 V_{fb} 之差值放大送至所述输出电路（30）的输入端；所述电压反馈电路（40）是将输出电路（30）的输出电压 V_{out} 反馈至误差放大电路（10）中；所述补偿电路（50）跨接在所述误差放大电路（10）的输出端和所述输出电路（30）的输出端之间；其特征在于：还包括电流反馈装置（60），该电流反馈装置（60）的输入端 V_I 连接所述输出电路（30）的输入端，即该电流反馈装置（60）将输出电路（30）输入的电压 V_I 转换成电流 I_{O1} 反馈到所述误差放大电路（10）的接地端，当所述稳压器在重负载时，该反馈电流 I_{O1} 增大，则所述误差放大电路（10）接地端的电流也随之增大，提高了该误差放大电路（10）的响应速度；当所述稳压器为轻负载时，该电流反馈装置（60）的反馈电流 I_{O1} 变小，所述误差放大电路（10）的接地端之偏置电流也减小，使得所述低压降稳压器的消耗处于静态低电流状态。

2. 按照权利要求 1 所述的极低静态电流的低压降稳压器，其特征在于：

还包括缓冲电路（20），该缓冲电路（20）串联在所述误差放大电路（10）和输出电路（30）之间；该缓冲电路（20）将所述误差放大电路（10）输出的电压进行平移或 / 和跟随处理后送至输出电路（30）的输入端；所述电流反馈装置（60）的输出端输送反馈电流 I_{O2} 至该缓冲电路（20）的接地端。

3. 按照权利要求 1 或 2 所述的极低静态电流的低压降稳压器，其特征在于：

所述电流反馈装置（60）包括电压 / 电流转换器（61）和电流镜（62）；所述电压 / 电流转换器（61）的输入端 V_I 连接在所述输出电路（30）的输入端，即将所述输出电路（30）的输入端电压 V_I 转换为电流，再送至与该电压 / 电流转换器（61）相连接的电流镜（62）的输入端 I_{in}，经电流镜（62）复制出电流（I_{O1}、I_{O2}）。

4. 按照权利要求 3 所述的极低静态电流的低压降稳压器，其特征在于：

所述电压 / 电流转器（61）包括电阻 R4 和 P 型 MOS 场效应晶体管 Q_2，所述电阻 R_4 跨接在所述低压降稳压器的电源 V_{IN} 与场效应晶体管 Q_2 的源极之间；所述场效应晶体管 Q_2 的栅极和漏极分别连接所述电压 / 电流转换器（61）的输入端 V_I 和输出端 I_O。

5. 按照权利要求 3 所述的极低静态电流的低压降稳压器，其特征在于：

所述电流镜（62）包括 N 型 MOS 场效应晶体管 Q_3、Q_4 和 Q_5；所述各场效应晶体管 Q_3、Q_4 和 Q_5 的源极并联接地，所述场效应晶体管 Q_3 的栅极与漏极连接且与所述电压 / 电流转换器（61）输出端 I_O 连接；所述场效应晶体管 Q_4、Q_5 组成的镜像装置，两者栅极并联，并再连接所述场效应晶体管 Q_3 的栅级；所述镜像装置将输入电流 I_{in} 分别按比例复制并再分配给电流镜的输出端口 I_{O1} 或 / 和 I_{O2}，电流 I_{in} 再分配比例由所述场效应晶体管 Q_4、Q_5 与 Q_3 的尺寸比例决定。

6. 按照权利要求 1 或 2 所述的极低静态电流的低压降稳压器，其特征在于：

所述误差放大电路（10）运放 1 的接地端经由一偏置电流源 I_1 接地，即所述偏置电流源 I_1 流出端接地；所述电流反馈装置（60）输出的反馈电流 I_{O1} 送到所述电流源 I_1 的注入端。

7. 按照权利要求 2 所述的极低静态电流的低压降稳压器，其特征在于：

所述缓冲电路（20）的运放 2 的接地端经由一偏置电流源 I_2 接地，即所述偏置电流源 I_2 流出端接地；所述电流反馈装置（60）输出的反馈电流 I_{O2} 送到所述电流源 I_2 的注入端。

Aptiv Services US, LLC　Exhibit 1003　Page 50

极低静态电流的低压降稳压器

[0001] 技术领域 本发明涉及低压降稳压器，特别是涉及集电电路芯片中的低压降稳压器，尤其是涉及一种极低静态电流的低压降稳压器。

[0002] 背景技术 随着半导体集成电路的发展，集成电路芯片所用工艺越来越先进，该芯片内部电路所需电源电压与芯片的输入电源电压通常不一致，大部分情况下该芯片内部电路所需电源电压低于芯片的输入电源电压，这就需要在芯片内部集成一低压降稳压器，将芯片的输入电源电压转换成内部其他电路需要的电源电压。此类低压降稳压器在给其他电路提供电源的同时需要自身消耗比较少的电流，特别是在芯片电路的睡眠期，低压降稳压器消耗的电流越低越好。

[0003] 现有技术低压降稳压器在工作时出于稳定性考虑，通常将其静态电流设计比较大，通常在 10μA 以上，这么大的静态电流使得该类低压降稳压器在睡眠时不节能。为了达到节能的目的，有的低压降稳压器采用一控制端来控制该低压降稳压器的工作与关闭：芯片工作时通过低压降稳压器的控制端将之开启；芯片睡眠时将低压降稳压器关闭。此类控制端由内部数字电路控制，数字电路所用电源又由低压降稳压器的输出供给。当该数字电路关闭低压降稳压器后，低压降稳压器就不能给该数字电路供电，数字电路没有电源则不能唤醒低压降稳压器，这样低压降稳压器在睡眠和唤醒状态之间存在一自锁机制，如何打破这一自锁机制是一件很复杂的事情，需要为此设计很多控制电路，当控制电路设计不好就会造成解锁失败；而且低压降稳压器关闭后，记忆在数字电路中的状态均会丢失，唤醒后这些状态又需要重新设定。

[0004] 发明内容 本发明要解决的技术问题在于避免上述现有技术的不足之处而提供一种极低静态电流的低压降稳压器，解决现有技术低压降稳压器睡眠或轻负载时功耗大的问题。

[0005] 本发明解决所述技术问题是通过采用以下技术方案来实现，设计一种极低静态电流的低压降稳压器，包括误差放大电路、输出电路、电压反馈电路和补偿电路；所述误差放大电路将参考电压 V_{ref} 与电压反馈电路送来的反馈电压 V_{fb} 之差值放大送至所述输出电路的输入端；所述电压反馈电路是将输出电路的输出电压 V_{out} 反馈至误差放大电路中；所述补偿电路跨接在所述误差放大电路的输出端和所述输出电路的输出端之间；特别是，还包括电流反馈装置，该电流反馈装置的输入端 V_I 连接所述输出电路的输入端，即该电流反馈装置将输出电路输入的电压 V_I 转换成电流 I_{O1} 反馈到所述误差放大电路的接地端，当所述稳压器在重负载时，该反馈电流 I_{O1} 增大，则所述误差放大电路接地端的电流也随之增大，提高了该误差放大电路的响应速度；当所述稳压器为轻负载时，该电流反馈装置的反馈电流 I_{O1} 变小，所述误差放大电路的接地端之偏置电流也减小，使得所述低压降稳压器的消耗处于静态低电流状态。

[0006] 所述低压降稳压器还包括缓冲电路，该缓冲电路串联在所述误差放大电路和输出电路之间；该缓冲电路将所述误差放大电路输出的电压进行平移或 / 和跟随处理后送至输出电路的输入端；所述电流反馈装置的输出端输送反馈电流 I_{O2} 至该缓冲电路的接地端。

[0007] 所述电流反馈装置包括电压 / 电流转换器和电流镜；所述电压 / 电流转换器的输

Aptiv Services US, LLC Exhibit 1003 Page 51

入端 V_I 连接在所述输出电路的输入端，即将该输出电路的输入端电压 V_I 转换为电流，再送至与该电压 / 电流转换器相连接的电流镜的输入端 I_{in}，经电流镜复制出电流 I_{O1}、I_{O2}。

[0008] 所述电压 / 电流转器包括电阻 R4 和 P 型 MOS 场效应晶体管 Q_2，所述电阻 R_4 跨接在所述低压降稳压器的电源 V_{IN} 与场效应晶体管 Q_2 的源极之间；所述场效应晶体管 Q_2 的栅极和漏极分别四连接所述电压 / 电流转器的输入端 V_I 和输出端 I_O。

[0009] 所述电流镜包括 N 型 MOS 场效应晶体管 Q3、Q4 和 Q5；所述各场效应晶体管 Q3、Q4 和 Q5 的源极并联接地，所述场效应晶体管 Q3 的栅极与漏极连接且与所述电压 / 电流转换器输出端 I_O 连接；所述场效应晶体管 Q4、Q5 组成镜像装置，两者栅极并联，并再连接所述场效应晶体管 Q3 的栅级；所述镜像装置将输入电流 I_{in} 分别按比例复制并再分配给电流镜的输出端口 I_{O1}、或 / 和 I_{O2}，电流 I_{in} 再分配比例由所述场效应晶体管 Q4、Q5 与 Q3 的尺寸比例决定。

[0010] 所述误差放大电路运放 1 的接地端经由一偏置电流源 I_1 接地，令所述偏置电流源 I_1 流出端接地；所述电流反馈装置输出的反馈电流 I_{O1} 送至所述电流源 I_1 的流入端。

[0011] 所述缓冲电路的运放 2 的接地端经由一偏置电流源 I_2 接地，令所述偏置电流源 I_2 流出端接地；所述电流反馈装置输出的反馈电流 I_{O2} 送到所述电流源 I_2 的流入端。

[0012] 同现有技术相比较，本发明的有益效果在于：提出了一种动态电流反馈装置的实现方法，该装置实时监测低压降稳压器的输出电流，根据输出电流的大小调节低压降稳压器的偏置电流，达到既在重负载情况下驱动能力很强，又在轻负载或睡眠时静态电流极低，非常节能；而且低压降稳压器无需睡眠 / 唤醒的控制端，不存在现有技术低压降稳压器的睡眠 / 唤醒的自锁问题；由于低压降稳压器一直工作，其输出电流一直存在，因而记忆在数字电路中的状态也不会丢失。与现有其它低压降稳压器相比，采用本发明提出的动态电流反馈装置后的低压降稳压器在轻负载和睡眠时的静态电流能低于 1μA，具有现有其它低压降稳压器无可比拟的技术优势。

[0013] 附图说明 图 1 是本发明极低静态电流的低压降稳压器之优选实施例的逻辑结构示意图；

图 2 是所述电流反馈装置 60 优选实施例一电原理图；

图 3 是所述电流反馈装置 60 优选实施例二电原理图；

图 4 是所述优选实施例中电流反馈装置 60 的逻辑结构示意图；

图 5 是所述优选实施例中电压转换器 61 的电路示意图；

图 6 是所述优选实施例中电流镜 62 的电路示意图。

[0014] 具体实施方式 下面，结合附图所示之优选实施例进一步阐述本发明。

[0015] 参阅图 1 至 2，本发明的优选实施例一是，一种极低静态电流的低压降稳压器，包括误差放大电路 10、输出电路 30、电压反馈电路 40 和补偿电路 50；所述误差放大电路 10 将参考电压 V_{ref} 与电压反馈电路 40 送来的反馈电压 V_{fb} 之差值放大送至所述输出电路 30 的输入端；所述电压反馈电路 40 是将输出电路 30 的输出电压 V_{out} 反馈至误差放大电路 10 中；所述补偿电路 50 跨接在所述误差放大电路 10 的输出端和所述输出电路 30 的输出端之间；还包括电流反馈装置 60 和缓冲电路 20，该缓冲电路 20 串联在所述误差放大电路 10 和输出电路 30 之间；该缓冲电路 20 将所述误差放大电路 10 输出的电压进行平移或 / 和跟随处理后送至输出电路 30 的输入端；所述电流反馈装置 60 的输入端 V_I 接入所述输出电路

Aptiv Services US, LLC Exhibit 1003 Page 52

30 的输入端，电流反馈装置 60 的输出端输送反馈电流 I_{O1} 和 I_{O2} 分别送至所述误差放大电路 10 和缓冲电路 20 的接地端；当所述稳压器在重负载时，该反馈电流 I_{O1} 和 I_{O2} 增大，则所述误差放大电路 10 和缓冲电路 20 各自接地端的电流也随之增大，从而提高了该误差放大电路 10 和缓冲电路 20 的响应速度；当所述稳压器为轻负载时，该电流反馈装置 60 的反馈电流 I_{O1} 和 I_{O2} 变小，所述误差放大电路 10 和缓冲电路 20 的接地端之偏置电流也减小，使得所述低稳压器的消耗处于静态低电流状态。

[0016] 结合图 2、图 4 至图 6 所示，优选实施例中各电路构件的功能分述如下：

所述误差放大电路 10 的运放 1 的接地端经由一偏置电流源 I_1 接地，即所述偏置电流源 I_1 的流出端接地，其注入端通过线网 n3 连接至运放 1 的地端；该偏置电流源 I_1 给运放 1 提供最基本的偏置电流，确保运放 1 在低压降稳压器处于轻负载或睡眠时仍能工作。所述反馈电流装置 60 输送的反馈电流 I_{O1} 送至所述电流源 I_1 的流入端。

[0017] 所述缓冲电路 20 的运放 2 的接地端经由一偏置电流源 I_2 接地，即所述偏置电流源 I_2 流出端接地，其流入端通过线网 n2 连接至运放 2 的地端，给运放 2 提供最基本的偏置电流，确保运放 2 在低压降稳压器处于轻负载或睡眠时仍能工作。所述反馈电流装置 60 输出的反馈电流 I_{O2} 送至所述电流源 I_2 的注入端。

[0018] 运放 1 为误差放大器，其负输入端接参考电源 V_{ref}，正输入端通过线网 n5 接电阻 R_1、R_2 组成的电压反馈电路 50 的输出。运放 1 将反馈电压 V_{fb} 与 V_{ref} 的差值进行同向放大得出误差校正电压，然后将误差校正电压传递给缓冲电路 20 的运放 2。运放 2 为缓冲器，其将运放 1 输出的误差校正电压进行电压跟随，必要时也可先进行电压平移再作电压跟随，然后通过线网 n1 输出至输出电路 30 中输出功率晶体管 Q_1 的栅极。运放 2 的输出驱动能力比较强，比运放 1 的输出驱动动能力大一个数量级或以上，输出功率晶体管 Q_1 的栅极电容比较大，运放 2 的输入端寄生电容比较小，这样运放 2 隔离了运放 1 直接驱动大容性负载的情况，大大提高了运放 1 的高频响应能力，而运放 2 因本身驱动能力比较强，在即使驱动输出功率晶体管 Q_1 的栅极电容的情况下其频率响应仍比运放 1 快若干倍。

[0019] 输出功率晶体管 Q_1 采用 PMOS（P 型金属 - 氧化物半导体），其栅极接运放 2 的输出，源极接电源 V_{In}，漏极接低压降稳压器的输出 V_{out}。电压反馈电路 50 由分压电阻 R_1、R_2 组成，将 V_{out} 的电压按比例反馈至运放 1 的正输入端。由图 2 可知，运放 1 的输出电压变化与低压降稳压器的输出 V_{out} 的电压变化是同向关系，运放 2 的输出电压变化与运放 1 的输出电压变化是同向关系，而输出功率晶体管 Q_1 的漏极电压变化与栅极电压变化是反向关系，故该低压降稳压器的电压反馈环路为负反馈，低压降稳压器能实时校正其输出电压 V_{cut}，使得输出电压 V_{out} 保持与参考电压 V_{ref} 恒定的电压比例关系。

[0020] 将输出功率晶体管 Q_1 的尺寸设计的比较大，因而驱动能力很强，使得无论负载为重负载（负载电阻 R_L 阻值小）还是轻负载（负载电阻 R_L 阻值大），输出电压 V_{out} 均保持基本恒定，误差不会太大。

[0021] 电流反馈装置 60 通过线网 n1 采样输出功率晶体管 Q_1 的栅极电压，并将电压转换为电流，其一股输出电流 I_{O2} 通过线网 n2 连接至运放 2 的地端，另一股输出电流 I_{O1} 通过线网 n3 连接至运放 1 的地端。当该低压降稳压器的负载变重时，输出电压 V_{out} 会略变低，通过电压负反馈环路使得功率晶体管 Q_1 的栅电压变低，同时功率晶体管 Q_1 的输出电流增大，抵制输出电压 V_{out} 变低，同时因功率晶体管 Q_1 的栅极电压变低，电流反馈装置的输出电流变

Aptiv Services US, LLC Exhibit 1003 Page 53

大，提高了运放1和运放2的偏置电流，从而提高了运放1和运放2的响应速度，整个系统的响应速度也随之增加了。反之，当该低压降稳压器的负载变轻时，功率晶体管 Q_1 的栅电压变高，电流反馈装置的输出电流变小，将运放1和运放2的偏置电流减小，整个系统的消耗的静态电流变小，从而实现了低压降稳压器在重负载时响应速度快，在轻负载时静态电流低，且无需增加低压降稳压器的控制端口。电流反馈装置的加入，使得低压降稳压器既节能又高效，是一种简单高效装置。

[0022] 图3中电阻 R_3 和电容 C_2 构成一种稳定性补偿电路40，电容 C_2 的一端接输出电压 V_{out}，另一端接电阻 R_3，电阻 R_3 的另一端通过线网n4接运放1的输出。电阻 R_3 和电容 C_2 的作用是在系统重负载时补偿运放1的输出极点，使得运放1的输出极点的输出极点为第二次要极点，同时极点落在由电容 C_1 和电阻 R_{e-s} 构成的零点附近，互相靠近的极点和零点形成偶极子，在频域的作用互相抵消。电容 C_1 为输出电压 V_{out} 的稳定电容，同时又使系统的主极点落在输出级，电阻 R_{e-s} 为电容 C_1 的等效串联电阻，电阻 R_{e-s} 和电容 C_1 共同组成输出电压稳定电路。电阻 R_L 为负载。

[0023] 请参阅图4所示，为本发明图3中电流反馈装置60的一种实现功能框图。电流反馈装置60包括两部分装置：一部分装置为电压/电流转换器61，其将从电流反馈装置的端口 V_I 的电压转换为电流 I_o 并输出给另一部分装置电流镜62；电流镜61将输入电流 I_{in} 复制并再分配并分别输出至电流反馈装置60的端口 I_{O1} 和 I_{O2}。

[0024] 请参阅图5所示，是本发明图3中电压/电流转换器60的一种具体电路实施方式，其由两个元件组成：电阻 R_4 和PMOS管 Q_2。电阻 R_4 的一端接电源 V_{In}，另一端接PMOS管 Q_2 的源极，PMOS管 Q_2 的栅极和漏极分别接电压/电流转换器的端口 V_I 和 I_O。电阻 R_4 充当限流装置的功能，在PMOS管 Q_2 的漏极电流比较小时，电阻 R_4 几乎不起作用，可以当作导线将其忽略，此时PMOS管 Q_2 的漏极电流由其跨导 gm_2 决定，漏极电流 $Id_2 \approx gm_2 * Vgs_2$，$Vgs_2$ 为PMOS管 Q_2 的栅源电压差；在PMOS管 Q_2 的漏极电流比较大时，电阻 R_4 起到负反馈的作用，限制PMOS管 Q_2 的漏极电流的增长，此时PMOS管 Q_2 的漏极电流由其跨导 Gm_2 决定，Gm_2 的公式为：

$$Gm_2 \approx \frac{gm_2}{1+(gm_2+gmb_2)*R_4}$$

gmb_2 为PMOS管 Q_2 的漏极与衬底的跨导

该PMOS管 Q_2 的漏极电流 $Id_2 \approx Gm_2 * Vgs_2$，由于 R_4 的加入，使得PMOS管 Q_2 在大电流时 gm_2 对漏极电流的作用被弱化，限制了漏极电流无限增大，最终限制了电压/电流转换器的最大输出电流。输出电流 $I_O = -Id_2$，所以PMOS管 Q_2 的栅极电压变低时，输出电流 I_O 变大；反之则反之。

[0025] 请参阅图6所示，为本发明图4中电流镜62的一种具体电路实施方式，其包括元件：NMOS管 Q_3、Q_4、Q_5。NMOS管 Q_3 接受电流镜的端口 I_{in} 的输入电流，并通过由NMOS管 Q_4、Q_5 组成的镜像装置将电流分别按一定比例复制并再分配给电流镜的输出端口 I_{O1} 和 I_{O2}，电流再分配比例由NMOS管 Q_4 和 Q_5 与 Q_3 的尺寸比例决定。图中只标示出两路输出电流的情况，依据本发明，输出一路或两路以上电流也是可以的；图中只使用了单个MOS来制作电流镜，依据本发明，很容易设计成MOS级联的方式来制作电流镜。这些均属于本专利的保护范畴。

[0026] 参考图1和3，本发明的优选实施例二与实例一所不同之处在于，所述极低静态电

Aptiv Services US, LLC Exhibit 1003 Page 54

流的低压降稳压器中没有缓冲器 20，电流反馈装置 60 的输入端 V_I 接入所述输出电路 30 的输入端，即该电流反馈装置 60 将输出电路 30 输入的电压 V_I 转换成电流 I_{O1} 反馈到所述误差放大电路 10 的接地端，当所述稳压器在重负载时，该反馈电流 I_{O1} 增大，则所述误差放大电路 10 接地端的电流也随之增大，即而提高了该误差放大电路 10 响应速度；当所述稳压器为轻负载时，该电流反馈装置 60 的反馈电流 I_{O1} 变小，所述误差放大电路 10 的接地端之偏置电流也减小，使得所述低稳压器的消耗处于静态低电流状态。

[0027] 本例中电流反馈装置 60 的实施电路均可采用实例一中的方案，只是电流镜 62 只使用了单个 MOS 来制作电流镜即可，这对对于本技术领域的普通技术人员结合实施例一是很显而易见的，此处不赘述。

Aptiv Services US, LLC Exhibit 1003 Page 55

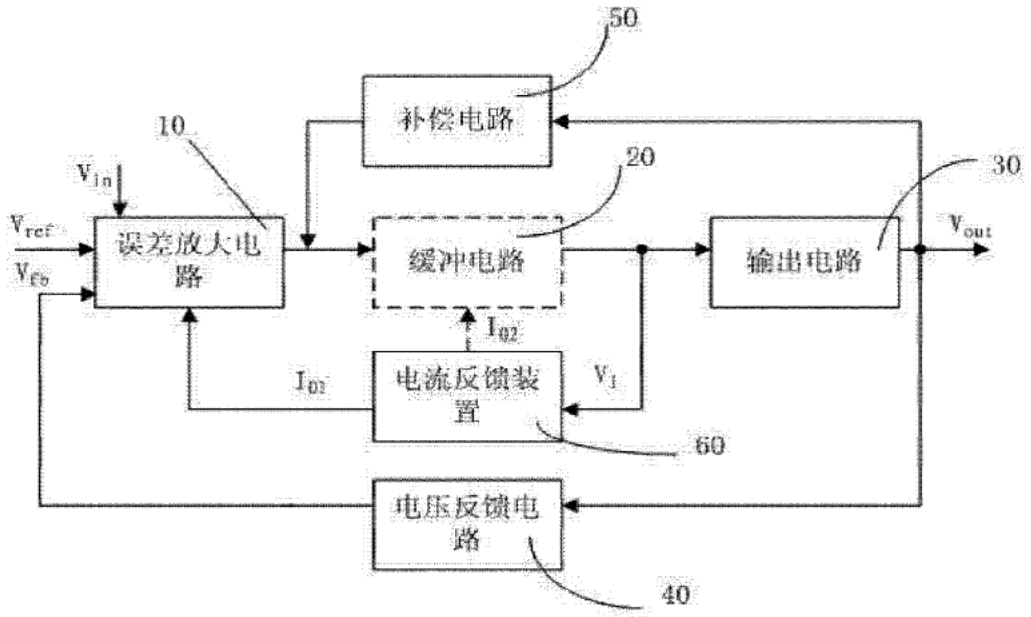


图 1

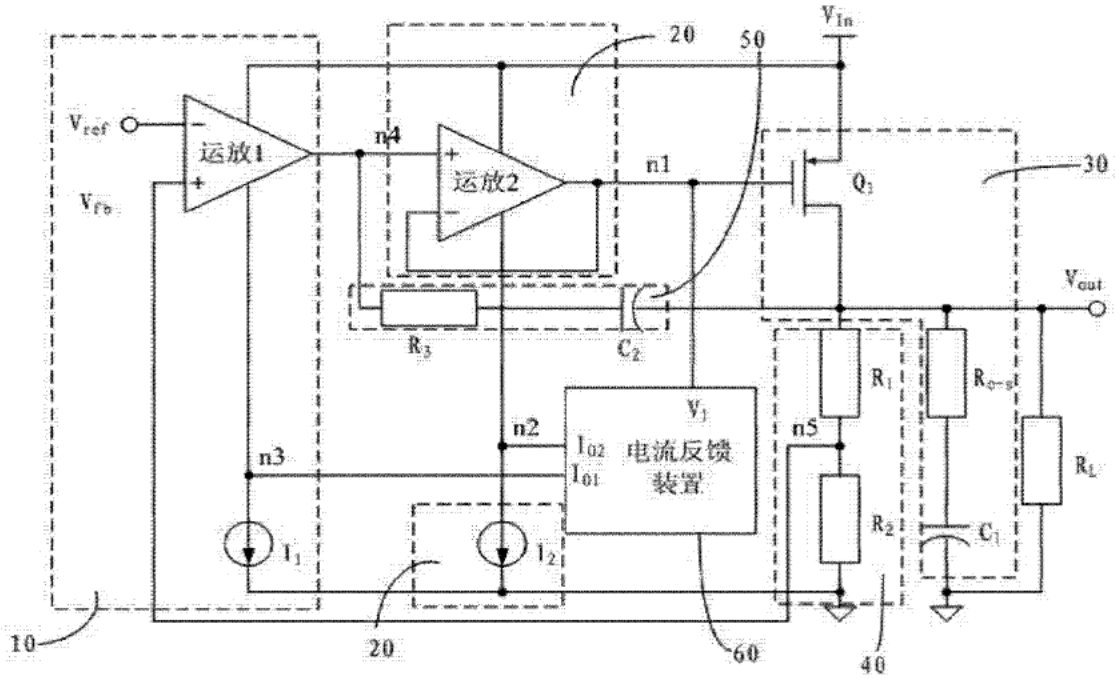


图 2

Aptiv Services US, LLC Exhibit 1003 Page 56

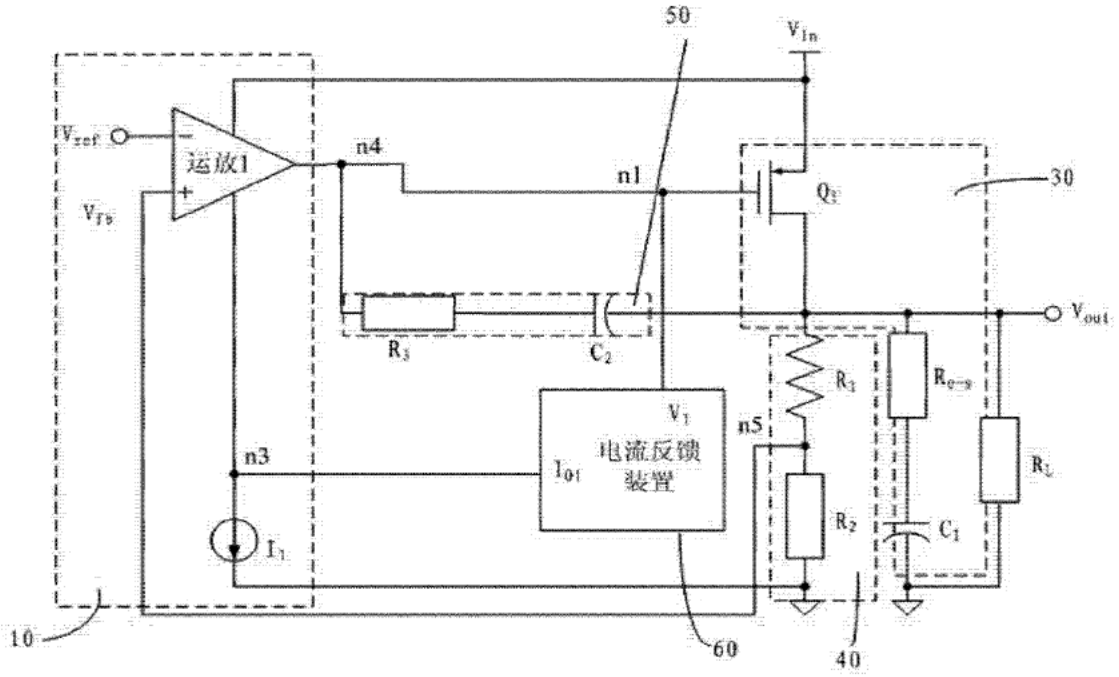


图 3

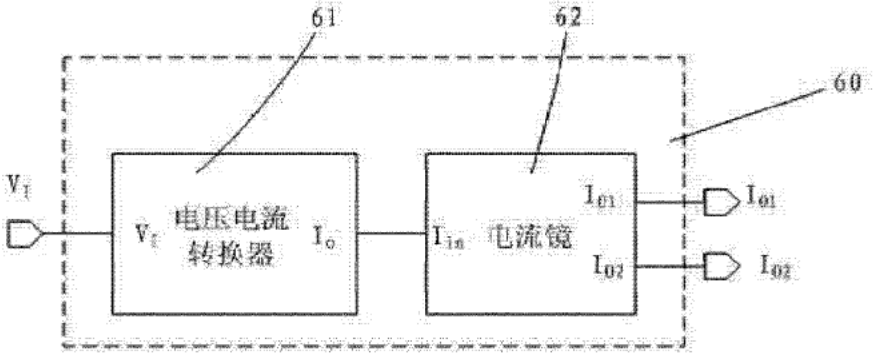


图 4

Aptiv Services US, LLC Exhibit 1003 Page 57

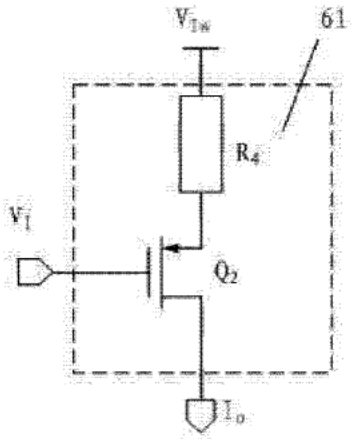


图 5

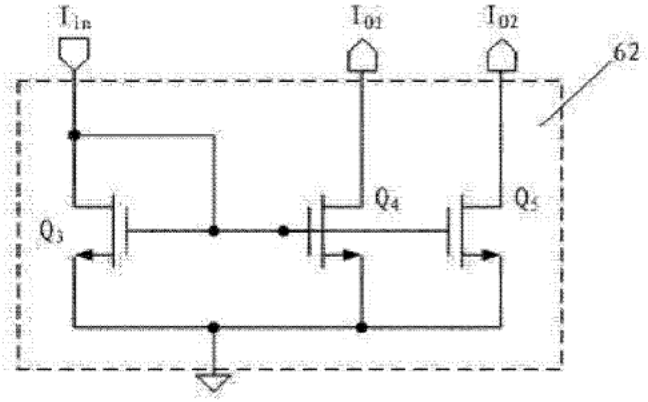


图 6

Aptiv Services US, LLC Exhibit 1003 Page 58

Electronic Patent Application Fee Transmittal

Application Number:	14204011
Filing Date:	11-Mar-2014
Title of Invention:	USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor
First Named Inventor/Applicant Name:	Huamin Zhou
Filer:	Eric M. Grabski/Jennie Averyt
Attorney Docket Number:	68354.225441

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt	
EFS ID:	26545456
Application Number:	14204011
International Application Number:	
Confirmation Number:	9205
Title of Invention:	USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor
First Named Inventor/Applicant Name:	Huamin Zhou
Customer Number:	86528
Filer:	Eric M. Grabski/Jennie Averyt
Filer Authorized By:	Eric M. Grabski
Attorney Docket Number:	68354.225441
Receipt Date:	04-AUG-2016
Filing Date:	11-MAR-2014
Time Stamp:	12:06:25
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$180
RAM confirmation Number	11281
Deposit Account	506736
Authorized User	GRUBERT, ANDREAS H
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 CFR 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 CFR 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 CFR 1.19 (Document supply fees)

Charge any Additional Fees required under 37 CFR 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	IDS_225441.pdf	103693 e1f93a2ee36727d5bb434c1c170c37834508ee6f	no	3
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
2	Foreign Reference	CN101419477A_225441.pdf	687512 2a48bad391e5a6527a09990686729e54e226164a	no	16
Warnings:					
Information:					
3	Foreign Reference	CN101853040A_225441.pdf	701642 a68aef4c8b69eced672a4e6988886c2a916f4403	no	14
Warnings:					
Information:					
4	Foreign Reference	CN102915061A_225441.pdf	1053025 1edc21f6ad2f0278c8680d06826e2f7ca054d0a4	no	16
Warnings:					
Information:					
5	Other Reference-Patent/App/Search documents	CNOA_225441.pdf	6247313 ea630a02621970e21ddfe6e00fc58d155f45ae8e	no	9
Warnings:					
Information:					
6	Fee Worksheet (SB06)	fee-info.pdf	31073 cb4b3f499b755afcae06224bb09f17e5e6a065f5	no	2
Warnings:					

Information:	
Total Files Size (in bytes):	8824258

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14204011	ZHOU ET AL.
	Examiner	**Art Unit**
	JUE ZHANG	2838

CPC						
Symbol					**Type**	**Version**
G05F		1	/	575	F	2013-01-01
H03F		2203	/	45192	A	2013-01-01
H03F		2203	/	45626	A	2013-01-01
H03F		3	/	45192	I	2013-01-01
H03F		2200	/	45	A	2013-01-01
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	18	
/JUE ZHANG/ Primary Examiner.Art Unit 2838	06/29/2016	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14204011	ZHOU ET AL.
	Examiner	**Art Unit**
	JUE ZHANG	2838

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
		G	0	5	F	1 / 575 (2006.01.01)						
CROSS REFERENCE(S)												
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)											

NONE (Assistant Examiner) (Date)	**Total Claims Allowed:** 18	
/JUE ZHANG/ Primary Examiner.Art Unit 2838 06/29/2016 (Primary Examiner) (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 2

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14204011	ZHOU ET AL.
	Examiner	**Art Unit**
	JUE ZHANG	2838

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	15	17												
2	2	16	18												
3	3	17	19												
4	4	18	20												
	5														
	6														
5	7														
6	8														
7	9														
8	10														
9	11														
10	12														
11	13														
12	14														
13	15														
14	16														

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	18	
/JUE ZHANG/ Primary Examiner.Art Unit 2838	06/29/2016	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/204,011	03/11/2014	Huamin Zhou	68354.225441	9205

86528 7590 07/06/2016

Slayden Grubert Beard PLLC
401 Congress Avenue
Suite 1900
Austin, TX 78701

EXAMINER	
ZHANG, JUE	

ART UNIT	PAPER NUMBER
2838	

NOTIFICATION DATE	DELIVERY MODE
07/06/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

trosson@sgbfirm.com
patent@sgbfirm.com
dallen@sgbfirm.com

Supplemental Notice of Allowability	Application No. 14/204,011	Applicant(s) ZHOU ET AL.	
	Examiner JUE ZHANG	Art Unit 2838	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed on 06/06/2016*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-4, 7-20*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☒ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/JUE ZHANG/
Primary Examiner, Art Unit 2838

The present application is being examined under the pre-AIA first to invent provisions.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Andreas H. Grubert on 06/29/2016.

The application has been amended as follows:

a. Claim 6 has been amended from:

"6. (Cancelled)"

To:

"5-6. (Cancelled)"

REASONS FOR ALLOWANCE

2. Claims 1-4, 7-20 are allowed.

3. The following is an examiner's statement of reasons for the indication of allowable subject matters:

For claim 1, see previous office action sent on 03/04/2016 for the examiner's statement of reasons for the indication of allowable subject matters

The aforementioned limitations in combination with all remaining limitations of the respective claims are believed to render the aforementioned indicated claim and any dependent claims thereof patentable over the art of record.

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jue Zhang whose telephone number is (571) 270-1263. The examiner can normally be reached on M-TH 8:00-5:00PM EST, Other F 8:00AM-4:00PM EST

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Monica Lewis can be reached on 571-272-1838. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JUE ZHANG/
Primary Examiner, Art Unit 2838

1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

86528 7590 06/22/2016

Slayden Grubert Beard PLLC
401 Congress Avenue
Suite 1900
Austin, TX 78701

EXAMINER
ZHANG, JUE

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 06/22/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/204,011	03/11/2014	Huamin Zhou	68354.225441	9205

TITLE OF INVENTION: USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	09/22/2016

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

86528 7590 06/22/2016
Slayden Grubert Beard PLLC
401 Congress Avenue
Suite 1900
Austin, TX 78701

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/204,011	03/11/2014	Huamin Zhou	68354.225441	9205

TITLE OF INVENTION: USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	09/22/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
ZHANG, JUE	2838	323-280000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/204,011	03/11/2014	Huamin Zhou	68354.225441	9205

86528 7590 06/22/2016

Slayden Grubert Beard PLLC
401 Congress Avenue
Suite 1900
Austin, TX 78701

EXAMINER	
ZHANG, JUE	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 06/22/2016

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/204,011	Applicant(s) ZHOU ET AL.	
	Examiner JUE ZHANG	Art Unit 2838	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed on 06/06/2016*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-5 and 7-20*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/JUE ZHANG/
Primary Examiner, Art Unit 2838

The present application is being examined under the pre-AIA first to invent provisions.

REASONS FOR ALLOWANCE

1. Claims 1-5, 7-20 are allowed.

2. The following is an examiner's statement of reasons for the indication of allowable subject matters:

For claim 1, see previous office action sent on 03/04/2016 for the examiner's statement of reasons for the indication of allowable subject matters

The aforementioned limitations in combination with all remaining limitations of the respective claims are believed to render the aforementioned indicated claim and any dependent claims thereof patentable over the art of record.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jue Zhang whose telephone number is (571) 270-1263. The examiner can normally be reached on M-TH 8:00-5:00PM EST, Other F 8:00AM-4:00PM EST

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Monica Lewis can be reached on 571-272-1838. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JUE ZHANG/
Primary Examiner, Art Unit 2838

1.

Notice of References Cited	Application/Control No. 14/204,011	Applicant(s)/Patent Under Reexamination ZHOU ET AL.	
	Examiner JUE ZHANG	Art Unit 2838	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2009/0009147 A1	01-2009	JIAN; MING-HONG	G05F1/575	323/280
*	B	US-7,656,224 B2	02-2010	Perez; Raul A.	H03F1/0261	323/282
*	C	US-7,683,720 B1	03-2010	Yehui; Sun	H03F3/45192	30/252
*	D	US-2007/0210770 A1	09-2007	Dean; James Robert	G05F1/46	323/273
*	E	US-2002/0171403 A1	11-2002	Lopata, Douglas D.	H03F3/45183	323/280
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14204011	ZHOU ET AL.
	Examiner	Art Unit
	JUE ZHANG	2838

CPC- SEARCHED		
Symbol	Date	Examiner
G05F1/575	8/23/2015	JZ
H03F3/45192	8/23/2015	JZ
Above search updated	2/27/2016	JZ
Above search updated	6/12/2016	JZ

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
323	280	8/23/2015	JZ
	Above search updated	2/27/2016	JZ
	Above search updated	6/12/2016	JZ

SEARCH NOTES		
Search Notes	Date	Examiner
See east search notes	8/23/2015	JZ
Inventor name search	8/23/2015	JZ
East search updated	2/27/2016	JZ
East search updated	6/12/2016	JZ

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	See east search notes in claim context	6/12/2016	JZ
G05F1	575	6/12/2016	JZ
H03F3	45192	6/12/2016	JZ

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	((Huamin) near2 (Zhou)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/12 21:23
L2	4	((Woowai) near2 (Martin)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/12 21:23
L3	2	((Cristian) near2 (Albina)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/12 21:23
L4	1	((Fritz) near2 (Schlunder)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/12 21:23
L5	396	((Minh) near2 (Le)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2016/06/12 21:23
L6	82	((Huamin) near2 (Zhou)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 21:23
L7	15	((Woowai) near2 (Martin)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 21:23
L8	9	((Cristian) near2 (Albina)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 21:23
L9	4	((Fritz) near2 (Schlunder)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 21:23

EAST Search History (Prior Art)

L10	1001	((Minh) near2 (Le)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 21:23
L11	98	L6 L7 L8 L9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 21:23
L12	1089	L6 L7 L8 L9 L10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/06/12 21:23
L13	4	L12 gm voltage regulator	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/06/12 21:23
L14	1	(("200500168272") or ("200600192538") or ("7312598") or ("200900009147")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/06/12 21:23
L15	4	(("20050168272") or ("20060192538") or ("7312598") or ("20090009147")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/06/12 21:23
L16	0	(("201361780985") or ("201414204011")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/06/12 21:23
L17	1	gm enhanced current buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	NEAR	ON	2016/06/12 21:23
L18	0	gm enhanced buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	NEAR	ON	2016/06/12 21:23

EAST Search History (Prior Art)

L19	5	gm current buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	NEAR	ON	2016/06/12 21:23
L20	21	gm with current buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	NEAR	ON	2016/06/12 21:23
L21	1	(gm or transconductance) enhanced current buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	NEAR	ON	2016/06/12 21:23
L22	7	L12 (gm or transconductance) voltage regulator	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/06/12 21:23
L23	318	(gm or transconductance) with voltage near regulator	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/06/12 21:23
L24	17	(gm or transconductance) enhanc$3 current near buffer voltage near regulator	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	AND	ON	2016/06/12 21:23
L25	3	(gm or transconductance) enhanc$3 current near buffer voltage near regulator with (low near drop near out or LDO)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	AND	ON	2016/06/12 21:23
L26	4	(gm or transconductance) with (enhanc$3 or boost$3) current near buffer voltage near regulator with (low near drop near out or LDO)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	AND	ON	2016/06/12 21:23

EAST Search History (Prior Art)

L27	3	"US 20150220094"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2016/06/12 21:23
L28	6	(gm or transconductance) with (enhanc$3 or boost$3) current near feedback (low near drop near out or LDO)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	AND	ON	2016/06/12 21:23
L29	183	folded-cascode amplifier	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	NEAR	ON	2016/06/12 21:23
L30	9667	folded-cascode near amplifier ldo	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	ON	2016/06/12 21:23
L31	1	folded-cascode near amplifier ldo	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	AND	ON	2016/06/12 21:23
L32	16	folded-cascode near amplifier voltage regulator	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	AND	ON	2016/06/12 21:23
L33	3363	G05F1/575.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	ON	2016/06/12 21:23
L34	1199	323/280.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	ON	2016/06/12 21:23
L35	4118	L33 L34	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	ON	2016/06/12 21:23

EAST Search History (Prior Art)

L36	138	L35 miller near compensat$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	AND	ON	2016/06/12 21:23
L37	65	L36 (gm or transconductance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/06/12 21:23
L38	37	L36 (gm or transconductance) bias	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/06/12 21:23
L39	0	L36 (gm or transconductance) bias near ratio	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/06/12 21:23
L40	2	L35 (gm or transconductance) bias near ratio	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/06/12 21:23
L41	1401	H03F3/45192.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	ON	2016/06/12 21:23
L42	73	L41 miller near compensat$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	AND	ON	2016/06/12 21:23
L43	47	L42 (gm or transconductance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/06/12 21:23

EAST Search History (Prior Art)

L44	1	L41 (gm or transconductance) bias near ratio	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/06/12 21:23
L45	0	L42 voltage near regulator	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/06/12 21:23
L46	4	(("20050168272") or ("20060192538") or ("7312598") or ("20090009147")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/06/12 21:23
L47	1257	(gm or transconductance) with current near (buffer or driv$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/06/12 21:23
L48	157	(gm or transconductance) near current near (buffer or driv$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/06/12 21:23
L49	14	(gm or transconductance) near current near (buffer or driv$3) (ldo or regulator)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/06/12 21:23
L50	167	(gm or transconductance) near (buffer or driv$3) (ldo or regulator)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/06/12 21:23
L51	2	(gm or transconductance) near (boost$3 or enhanc$3 or improv$3) near (buffer or driv$3) (ldo or regulator)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/06/12 21:23

EAST Search History (Prior Art)

L52	20	"US 6703816"	US-PGPUB; USPAT; USOCR; DERWENT	OR	OFF	2016/06/12 21:23
L53	8	(gm or transconductance) near (boost$3 or enhanc$3 or improv$3) with (buffer or driv$3) (ldo or regulator)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/06/12 21:23
L54	4	(("20090039849") or ("20070210770") or ("20050083027") or ("20050073286")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/06/12 21:23
L55	6	(("20090039849") or ("20070210770") or ("20050083027") or ("20050073286") or ("20020171403") or ("7639067")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/06/12 21:23
L56	8	(gm or transconductance) near (boost$3 or enhanc$3 or improv$3) with (buffer$3 or driv$3) (ldo or regulator)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/06/12 21:23
L57	83	(gm or transconductance) near (boost$3 or enhanc$3 or improv$3) (ldo or regulator)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/06/12 21:23
L58	22	(gm or transconductance) near (boost$3 or enhanc$3 or improv$3) with current (ldo or regulator)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/06/12 21:23
L59	17	L58 not L53	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/06/12 21:23
L60	0	biasing near circuit with noise near immunity with capacitor ldo	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2016/06/12 21:23

EAST Search History (Prior Art)

L61	0	biasing near circuit with noise with capacitor ldo	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2016/06/12 21:23
L62	18	bias$3 with noise with capacitor ldo	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2016/06/12 21:23
L63	3363	G05F1/575.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	ON	2016/06/12 21:23
L64	1199	323/280.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	ON	2016/06/12 21:23
L65	1401	H03F3/45192.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	ON	2016/06/12 21:23
L66	5503	L63 L64 L65	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/06/12 21:23
L67	5	L66 bias$3 with noise with capacitor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2016/06/12 21:23
L68	1	("6246221").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/06/12 21:23

EAST Search History (Prior Art)

L69	720	bias$3 with capacitor (ldo or low near drop)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2016/06/12 21:23
L70	55	bias$3 near capacitor (ldo or low near drop)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2016/06/12 21:23

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L71	661	G05F1/575.cpc.	US-PGPUB	OR	ON	2016/06/12 21:47
L72	741	G05F1/575.cpc.	USPAT	OR	ON	2016/06/12 21:52
L73	266	H03F3/45192.cpc.	US-PGPUB	OR	ON	2016/06/12 21:59

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14204011	ZHOU ET AL.
	Examiner	**Art Unit**
	JUE ZHANG	2838

CPC						
Symbol					**Type**	**Version**
G05F		1	/	575	F	2013-01-01
H03F		2203	/	45192	A	2013-01-01
H03F		2203	/	45626	A	2013-01-01
H03F		3	/	45192	I	2013-01-01
H03F		2200	/	45	A	2013-01-01
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			
			/			

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 19	
/JUE ZHANG/ Primary Examiner.Art Unit 2838 (Primary Examiner)	06/12/2016 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 2

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14204011	ZHOU ET AL.
	Examiner	**Art Unit**
	JUE ZHANG	2838

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
		G 0 5 F 1 / 575 (2006.01.01)	

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	19	
/JUE ZHANG/ Primary Examiner.Art Unit 2838	06/12/2016	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14204011	ZHOU ET AL.
	Examiner	**Art Unit**
	JUE ZHANG	2838

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	16	17												
2	2	17	18												
3	3	18	19												
4	4	19	20												
5	5														
	6														
6	7														
7	8														
8	9														
9	10														
10	11														
11	12														
12	13														
13	14														
14	15														
15	16														

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 19	
/JUE ZHANG/ Primary Examiner.Art Unit 2838 (Primary Examiner)	06/12/2016 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Huamin Zhou et al.
Serial No.:	14/204,011
Date Filed:	March 11, 2014
Group Art Unit:	2838
Confirmation No.:	9205
Examiner:	Zhang, Jue
Title:	**USB REGULATOR WITH CURRENT BUFFER TO REDUCE COMPENSATION CAPACITOR SIZE AND PROVIDE FOR WIDE RANGE OF ESR VALUES OF EXTERNAL CAPACITOR**

MAIL STOP – AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Examiner:

RESPONSE TO OFFICE ACTION

In response to the Office Action mailed March 4, 2016 Applicants respectfully submit the following remarks and request favorable action thereon.

Amendments to Claims begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

CLAIM AMENDMENTS

IN THE CLAIMS

This listing of the claims will replace all prior versions, and listing, of claims in the application or previous response to office action:

1. (**Currently Amended**) A voltage regulator, comprising:

an operational amplifier;

a gm enhanced current buffer driver;

a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver;

an enable/disable function to enable/disable the biasing circuit for reducing standby current;

an output power driver, wherein the current buffer driver is coupled between the operational amplifier and the output power driver;

a current feedback circuit coupled between the output power driver and the current buffer driver; and

a feedback loop coupled between the output power driver and the operational amplifier.

2. (Original) The voltage regulator according to claim 1, further comprising a gm-boost circuit coupled to the current buffer driver.

3. (Original) The voltage regulator according to claim 2, wherein the gm-boost circuit increases the current buffer driver input impedance.

4. (Original) The voltage regulator according to claim 2, wherein the gm-boost circuit enables the current buffer driver to have a large gm value.

6. (Cancelled)

7. (Original) The voltage regulator according to claim 1, further comprising a compensation capacitor coupled between the output power driver and a cascode node of the operational amplifier.

8. (Original) The voltage regulator according to claim 1, wherein the voltage regulator is a low drop out (LDO) voltage regulator.

9. (Original) The voltage regulator according to claim 1, wherein the operational amplifier has a first input adapted for coupling to a voltage reference, and a second input coupled to the feedback loop.

10. (Original) The voltage regulator according to claim 1, wherein the operational amplifier is a low gain and high bandwidth amplifier.

11. (Original) The voltage regulator according to claim 10, wherein the low gain and high bandwidth amplifier is a folded-cascode amplifier.

12. The voltage regulator according to claim 11, wherein the operational amplifier comprises diode connected PMOS transistors for lowering an output impedance of the folded-cascode amplifier.

13. (Original) The voltage regulator according to claim 1, wherein the current buffer driver is an operational transconductance amplifier (OTA).

14. (Original) The voltage regulator according to claim 1, wherein the current feedback circuit senses a current change at the output power driver.

15. (Original) The voltage regulator according to claim 1, wherein the current feedback circuit provides transient enhancement for improved load regulation.

16. (Original) The voltage regulator according to claim 1, wherein the current feedback circuit provides a feedback voltage from an output voltage node.

17. (Original) The voltage regulator according to claim 1, wherein the current buffer driver has a low output impedance.

18. (**Currently Amended**) The voltage regulator according to claim ~~5~~1, further comprising capacitors in the biasing circuit for improving noise immunity thereof.

19. (Original) The voltage regulator according to claim 1, wherein the voltage regulator is a USB voltage regulator.

20. (Original) The voltage regulator according to claim 1, wherein the current buffer driver has low input impedance and provides a high frequency pole that does not substantially affect the voltage regulator dominant pole.

REMARKS

This Application has been carefully reviewed in light of the Office Action mailed March 4, 2016. Claims 1-17 and 19-20 were rejected and Claims 6 and 18 were objected to in the Office Action. Applicants amend claims 1 and 18. Claims 5 and 6 have been cancelled. Applicants respectfully request reconsideration and allowance of all pending claims.

Allowable Subject Matter

Applicants appreciate Examiner's consideration and indication that Claims 6 and 18 would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims. Applicants amended independent claim 1 to include the limitations of former claims 5 and 6. Claim 18 has been amended to be dependent on claim 1.

CONCLUSION

Applicants have made an earnest effort to place this case in condition for allowance in light of the remarks set forth above. Applicants respectfully request reconsideration of the pending claims.

Applicants believe there are no fees due at this time. However, the Commissioner is hereby authorized to charge any fees necessary or credit any overpayment to Deposit Account No. 50-6736 of SLAYDEN GRUBERT BEARD PLLC.

If there are any matters concerning this Application that may be cleared up in a telephone conversation, please contact Applicants' attorney at 512-402-3553.

Respectfully submitted,
SLAYDEN GRUBERT BEARD PLLC.
Attorney for Applicants

Andreas H. Grubert
Registration No. 59,143

Date: June 6, 2016

SEND CORRESPONDENCE TO:
SLAYDEN GRUBERT BEARD PLLC
CUSTOMER ACCOUNT NO. **86528**
512-402-3553

Electronic Acknowledgement Receipt	
EFS ID:	25980363
Application Number:	14204011
International Application Number:	
Confirmation Number:	9205
Title of Invention:	USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor
First Named Inventor/Applicant Name:	Huamin Zhou
Customer Number:	86528
Filer:	Eric M. Grabski/Todd Rosson
Filer Authorized By:	Eric M. Grabski
Attorney Docket Number:	68354.225441
Receipt Date:	06-JUN-2016
Filing Date:	11-MAR-2014
Time Stamp:	16:04:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Response_OA_225441.pdf	111225 eb9707e0652e054af2adca8bab00e17bf71d743b	yes	6

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	5
	Applicant Arguments/Remarks Made in an Amendment	6	6
Warnings:			
Information:			
	Total Files Size (in bytes):	111225	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/204,011	Filing Date 03/11/2014	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT		(Column 1)		(Column 2)	(Column 3)		
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

AMENDMENT	06/06/2016	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 18	Minus	** 20	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 1	X $420 =	420
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	**420**

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/Chantae Dessau/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/204,011	03/11/2014	Huamin Zhou	68354.225441	9205

86528 7590 03/04/2016

Slayden Grubert Beard PLLC
401 Congress Avenue
Suite 1900
Austin, TX 78701

EXAMINER	
ZHANG, JUE	

ART UNIT	PAPER NUMBER
2838	

NOTIFICATION DATE	DELIVERY MODE
03/04/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

trosson@sgbfirm.com
patent@sgbfirm.com
wjenks@sgbfirm.com

Office Action Summary	Application No. 14/204,011	Applicant(s) ZHOU ET AL.	
	Examiner JUE ZHANG	Art Unit 2838	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/24/2015*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-17,19 and 20* is/are rejected.

8)☒ Claim(s) *6 and 18* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☒ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *11/24/2015* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the reply filed on 11/24/2015. Claims 1-20 are pending.

Notice of Pre-AIA or AIA Status

2. The present application is being examined under the pre-AIA first to invent provisions.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5, 7-17, 20 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Al-Shyoukh et al. (NPL_IEEE_JSSC_2007, hereinafter Al-Shyoukh).

Claim 1, Al-Shyoukh teaches a voltage regulator (e.g., see Fig. 4-9), comprising: an operational amplifier (e.g., the Error Amplifier comprising M1-M8, see Fig. 8 in view of Fig. 4-5); a gm enhanced current buffer driver (e.g., the circuits comprising M21-M27, see Fig. 8 in view of Fig. 4-5); an output power driver (e.g., Mp), wherein the current buffer driver is coupled between the operational amplifier and the output power driver (e.g., see Fig. 8 in view of Fig. 4-5); a current feedback circuit (e.g., the circuits

comprising Cc, , see Fig. 8 in view of Fig. 4-5) coupled between the output power driver and the current buffer driver (e.g., see Fig. 8 in view of Fig. 4-5); and a feedback loop (e.g., the loop through N5 to M2) coupled between the output power driver and the operational amplifier (e.g., see Fig. 8 in view of Fig. 4-5).

Claim 2, '221 teaches the limitations of claim 1 as discussed above. It further teaches that a gm-boost circuit coupled to the current buffer driver (e.g., see Fig. 2).

Claim 3, '221 teaches the limitations of claim 2 as discussed above. It further teaches that wherein the gm-boost circuit increases the current buffer driver input impedance (e.g., see col. 7 lines 2-12 in view of Fig. 2).

Claim 4, '221 teaches the limitations of claim 2 as discussed above. It further teaches that wherein the gm-boost circuit enables the current buffer driver to have a large gm value (e.g., see col. 7 lines 50-53 in view of Fig. 2).

Claim 5, '221 teaches the limitations of claim 2 as discussed above. It further teaches that a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver (e.g., the ratio of I21 and I22, see Fig. 8 in view of Fig. 3b).

Claim 7, '221 teaches the limitations of claim 1 as discussed above. It further teaches that a compensation capacitor (e.g., Cc) coupled between the output power driver and a cascode node of the operational amplifier (e.g., N4, see Fig. 8 in view of Fig. 4-5).

Claim 8, '221 teaches the limitations of claim 1 as discussed above. It further teaches that wherein the voltage regulator is a low drop out (LDO) voltage regulator

(e.g., see Abstract).

Claim 9, '221 teaches the limitations of claim 1 as discussed above. It further teaches that wherein the operational amplifier has a first input adapted for coupling to a voltage reference (e.g., Vbg), and a second input coupled to the feedback loop (e.g., see Fig. 8).

Claim 10, '221 teaches the limitations of claim 1 as discussed above. It further teaches that wherein the operational amplifier is a low gain and high bandwidth amplifier (e.g., the gain and the bandwidth of the Error Amplifier which is the same OpAmp Applicant disclosed in Fig. 3A of the current application, see Fig. 8).

Claim 11, '221 teaches the limitations of claim 10 as discussed above. It further teaches that wherein the low gain and high bandwidth amplifier is a folded-cascode amplifier (e.g., the Error Amplifier of Fig. 4, 8, see col. 1, page 1735).

Claim 12, '221 teaches the limitations of claim 11 as discussed above. It further teaches that wherein the operational amplifier comprises diode connected PMOS transistors for lowering an output impedance of the folded- cascode amplifier (e.g., the Error Amplifier of Fig. 4, 8, see col. 1, page 1735).

Claim 13, '221 teaches the limitations of claim 1 as discussed above. It further teaches that wherein the current buffer driver is an operational transconductance amplifier (OTA) (e.g., see Fig. 8 in view of Fig. 3b).

Claim 14, '221 teaches the limitations of claim 1 as discussed above. It further teaches that wherein the current feedback circuit senses a current change at the output power driver (e.g., the load current sensed by Cc and M3, see Fig. 8 in view of Fig. 4-5).

Claim 15, '221 teaches the limitations of claim 1 as discussed above. It further teaches that wherein the current feedback circuit provides transient enhancement for improved load regulation (e.g., see Abstract, Fig. 8).

Claim 16, '221 teaches the limitations of claim 1 as discussed above. It further teaches that wherein the current feedback circuit provides a feedback voltage from an output voltage node (e.g. the node Vout, see Fig. 8, 4-5).

Claim 17, '221 teaches the limitations of claim 1 as discussed above. It further teaches that wherein the current buffer driver has a low output impedance (e.g., the impedance at N2, see para2, col. 1 page 1735, para2, col. 2 page 1735, Fig. 8, 4-5).

Claim 20, '221 teaches the limitations of claim 1 as discussed above. It further teaches that wherein the current buffer driver has low input impedance and provides a high frequency pole that does not substantially affect the voltage regulator dominant pole (e.g., the pole at N2 (p2), see Abstract, para 3, col. 1 page 1735, para2, col. 2 page 1735, Fig. 8, 4-5).

Claim Rejections - 35 USC § 103

5. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1,148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Al-Shyoukh et al. (NPL_IEEE_JSSC_2007, hereinafter Al-Shyoukh

Claim 19, Al-Shyoukh discloses the claimed invention except for explicitly disclosing that wherein the voltage regulator is a USB voltage regulator. However, It would have been obvious to one having ordinary skill in the art at the time of invention was made to modify the voltage regulator circuit to use the voltage regulator of Al-Shyoukh as a USB voltage regulator, because it is dynamically adaptable, as demonstrated by Al-Shyoukh, to either the light load or the heavy load (e.g., see [0006]).

Allowable Subject Matter

9. Claims 6, 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matters:

For claim 6, the prior art does not disclose or suggest, in combination with the limitations of the base claim and any intervening claims, primarily, the voltage regulator further having … an enable/disable function to enable/disable the biasing circuit for reducing standby current.

For claim 18, the prior art does not disclose or suggest, in combination with the limitations of the base claim and any intervening claims, primarily, the voltage regulator further having … capacitors in the biasing circuit for improving noise immunity thereof.

Response to Argument

11. Applicant's arguments filed on 11/24/2015 have been fully considered but are moot in view of the new ground of rejections in the current office action above.

Examiner's Note:

12. Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the

references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

13. In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JUE ZHANG whose telephone number is (571)270-1263. The examiner can normally be reached on M-Th 7:30-5:00PM EST, Other F 7:30AM-5:00PM EST

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Monica Lewis can be reached on 571-272-1838. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JUE ZHANG/
Primary Examiner, Art Unit 2838

Notice of References Cited	Application/Control No. 14/204,011	Applicant(s)/Patent Under Reexamination ZHOU ET AL.	
	Examiner JUE ZHANG	Art Unit 2838	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-6,246,221 B1	06-2001	Xi; Xiaoyu	G05F1/575	323/280
*	B	US-2013/0241505 A1	09-2013	CHANG; JUNG-FU	G05F1/575	323/282
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Al-Shyoukh et al., 08/2007, IEEE, JOSSC Vol. 42 No. 8, 1732-1742
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14204011	ZHOU ET AL.
	Examiner	Art Unit
	JUE ZHANG	2838

CPC- SEARCHED		
Symbol	Date	Examiner
G05F1/575	8/23/2015	JZ
H03F3/45192	8/23/2015	JZ
Above search updated	2/27/2016	JZ

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
323	280	8/23/2015	JZ
	Above search updated	2/27/2016	JZ

SEARCH NOTES		
Search Notes	Date	Examiner
See east search notes	8/23/2015	JZ
Inventor name search	8/23/2015	JZ
East search updated	2/27/2016	JZ

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	((Huamin) near2 (Zhou)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/08/09 14:51
S2	4	((Woowai) near2 (Martin)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/08/09 14:52
S3	2	((Cristian) near2 (Albina)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/08/09 14:52
S4	1	((Fritz) near2 (Schlunder)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/08/09 14:52
S5	348	((Minh) near2 (Le)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/08/09 14:52
S6	54	((Huamin) near2 (Zhou)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/09 14:52
S7	14	((Woowai) near2 (Martin)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/09 14:52
S8	5	((Cristian) near2 (Albina)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/09 14:53
S9	3	((Fritz) near2 (Schlunder)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/09 14:53

EAST Search History (Prior Art)

S10	903	((Minh) near2 (Le)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/09 14:53
S11	67	S6 S7 S8 S9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/09 14:53
S12	961	S6 S7 S8 S9 S10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/09 14:53
S13	3	S12 gm voltage regulator	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2015/08/09 14:54
S14	1	(("200500168272") or ("200600192538") or ("7312598") or ("200900009147")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/08/09 14:56
S15	4	(("20050168272") or ("20060192538") or ("7312598") or ("20090009147")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/08/09 14:56
S16	0	(("201361780985") or ("201414204011")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/08/09 14:58
S17	1	gm enhanced current buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	NEAR	ON	2015/08/09 15:00
S18	0	gm enhanced buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	NEAR	ON	2015/08/09 15:00

EAST Search History (Prior Art)

S19	3	gm current buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	NEAR	ON	2015/08/09 15:01
S20	18	gm with current buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	NEAR	ON	2015/08/09 15:01
S21	1	(gm or transconductance) enhanced current buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	NEAR	ON	2015/08/09 15:03
S22	6	S12 (gm or transconductance) voltage regulator	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2015/08/09 15:03
S23	299	(gm or transconductance) with voltage near regulator	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2015/08/09 15:04
S24	13	(gm or transconductance) enhanc$3 current near buffer voltage near regulator	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	AND	ON	2015/08/09 15:05
S25	2	(gm or transconductance) enhanc$3 current near buffer voltage near regulator with (low near drop near out or LDO)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	AND	ON	2015/08/09 15:11
S26	3	(gm or transconductance) with (enhanc$3 or boost$3) current near buffer voltage near regulator with (low near drop near out or LDO)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	AND	ON	2015/08/09 15:12

EAST Search History (Prior Art)

S27	1	"US 20150220094"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2015/08/09 15:14
S28	6	(gm or transconductance) with (enhanc$3 or boost$3) current near feedback (low near drop near out or LDO)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	AND	ON	2015/08/09 15:38
S30	176	folded-cascode amplifier	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	NEAR	ON	2015/08/09 16:49
S31	8508	folded-cascode near amplifier ldo	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	ON	2015/08/09 16:50
S32	1	folded-cascode near amplifier ldo	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	AND	ON	2015/08/09 16:50
S33	16	folded-cascode near amplifier voltage regulator	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	AND	ON	2015/08/09 16:51
S34	2916	G05F1/575.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	ON	2015/08/23 13:30
S35	1124	323/280.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	ON	2015/08/23 13:30
S36	3667	S34 S35	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	ON	2015/08/23 13:30

EAST Search History (Prior Art)

S37	121	S36 miller near compensat$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	AND	ON	2015/08/23 13:31
S38	59	S37 (gm or transconductance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2015/08/23 13:32
S39	33	S37 (gm or transconductance) bias	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2015/08/23 13:33
S40	0	S37 (gm or transconductance) bias near ratio	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2015/08/23 13:33
S41	1	S36 (gm or transconductance) bias near ratio	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2015/08/23 13:33
S42	1322	H03F3/45192.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	ON	2015/08/23 13:42
S43	73	S42 miller near compensat$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	AND	ON	2015/08/23 13:42
S44	47	S43 (gm or transconductance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2015/08/23 13:42

EAST Search History (Prior Art)

S45	1	S42 (gm or transconductance) bias near ratio	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2015/08/23 13:43
S46	0	S43 voltage near regulator	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2015/08/23 13:44
S47	4	(("20050168272") or ("20060192538") or ("7312598") or ("20090009147")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/08/23 13:47
S48	1235	(gm or transconductance) with current near (buffer or driv$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/02/03 14:11
S49	154	(gm or transconductance) near current near (buffer or driv$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/02/03 14:11
S50	13	(gm or transconductance) near current near (buffer or driv$3) (ldo or regulator)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/02/03 14:11
S51	164	(gm or transconductance) near (buffer or driv$3) (ldo or regulator)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/02/03 14:14
S52	2	(gm or transconductance) near (boost$3 or enhanc$3 or improv$3) near (buffer or driv$3) (ldo or regulator)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/02/03 14:16

EAST Search History (Prior Art)

S53	19	"US 6703816"	US-PGPUB; USPAT; USOCR; DERWENT	OR	OFF	2016/02/03 14:21
S54	7	(gm or transconductance) near (boost$3 or enhanc$3 or improv$3) with (buffer or driv$3) (ldo or regulator)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/02/04 10:56
S55	4	(("20090039849") or ("20070210770") or ("20050083027") or ("20050073286")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/02/04 11:03
S56	6	(("20090039849") or ("20070210770") or ("20050083027") or ("20050073286") or ("20020171403") or ("7639067")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/02/04 11:07
S57	7	(gm or transconductance) near (boost$3 or enhanc$3 or improv$3) with (buffer$3 or driv$3) (ldo or regulator)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/02/04 11:19
S58	81	(gm or transconductance) near (boost$3 or enhanc$3 or improv$3) (ldo or regulator)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/02/04 11:20
S59	20	(gm or transconductance) near (boost$3 or enhanc$3 or improv$3) with current (ldo or regulator)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/02/04 11:20
S60	16	S59 not S54	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2016/02/04 11:20
S61	0	biasing near circuit with noise near immunity with capacitor ldo	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2016/02/27 09:33

EAST Search History (Prior Art)

S62	0	biasing near circuit with noise with capacitor ldo	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2016/02/27 09:34
S63	18	bias$3 with noise with capacitor ldo	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2016/02/27 09:34
S64	3266	G05F1/575.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	ON	2016/02/27 09:36
S65	1170	323/280.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	ON	2016/02/27 09:36
S66	1381	H03F3/45192.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	ON	2016/02/27 09:36
S67	5380	S64 S65 S66	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/02/27 09:36
S68	4	S67 bias$3 with noise with capacitor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2016/02/27 09:36
S69	1	("6246221").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/02/27 09:48

EAST Search History (Prior Art)

S70	695	bias$3 with capacitor (ldo or low near drop)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2016/02/27 10:10
S71	53	bias$3 near capacitor (ldo or low near drop)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	OFF	2016/02/27 10:10

EAST Search History (Interference)

		<This search history is empty>				

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Huamin Zhou et al.
Serial No.:	14/204,011
Date Filed:	March 11, 2014
Group Art Unit:	2838
Confirmation No.:	9205
Examiner:	Zhang, Jue
Title:	**USB REGULATOR WITH CURRENT BUFFER TO REDUCE COMPENSATION CAPACITOR SIZE AND PROVIDE FOR WIDE RANGE OF ESR VALUES OF EXTERNAL CAPACITOR**

MAIL STOP – AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Examiner:

RESPONSE TO OFFICE ACTION

In response to the Office Action mailed August 31, 2015, Applicants respectfully submit the following remarks and request favorable action thereon.

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Drawings begin on page 3 of this paper and include both an attached replacement sheet and an annotated sheet showing changes.

Amendments to Claims are reflected in the listing of claims which begins on page 4 of this paper.

Remarks/Arguments begin on page 7 of this paper.

SPECIFICATION AMENDMENT

1. Please replace the abstract with the following amended abstract:

A voltage regulator ~~comprises~~ has a large gm current buffer driver added between a first stage of an operation amplifier and a last stage power transistor. This current buffer allows a significant reduction in the maximum internal and external compensation capacitances needed for regulator stability. The current buffer compensation circuit allows a wide range of external capacitor sizes that increases the flexibility in choosing the external capacitor types (with low to high ESR ratings).

DRAWING AMENDMENTS

IN THE DRAWING:

The drawings were objected to for failing to show every feature of the invention as specified in the claims. Applicants provide formal corrected drawings to be entered if the proposed changes are accepted by the Examiner.

CLAIM AMENDMENTS

IN THE CLAIMS

This listing of the claims will replace all prior versions, and listing, of claims in the application or previous response to office action:

1. (Original) A voltage regulator, comprising:

an operational amplifier;

a gm enhanced current buffer driver;

an output power driver, wherein the current buffer driver is coupled between the operational amplifier and the output power driver;

a current feedback circuit coupled between the output power driver and the current buffer driver; and

a feedback loop coupled between the output power driver and the operational amplifier.

2. (Original) The voltage regulator according to claim 1, further comprising a gm-boost circuit coupled to the current buffer driver.

3. (Original) The voltage regulator according to claim 2, wherein the gm-boost circuit increases the current buffer driver input impedance.

4. (Original) The voltage regulator according to claim 2, wherein the gm-boost circuit enables the current buffer driver to have a large gm value.

5. (Original) The voltage regulator according to claim 1, further comprising a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver.

6. (Original) The voltage regulator according to claim 5, further comprising an enable/disable function to enable/disable the biasing circuit for reducing standby current.

7. (Original) The voltage regulator according to claim 1, further comprising a compensation capacitor coupled between the output power driver and a cascode node of the operational amplifier.

8. (Original) The voltage regulator according to claim 1, wherein the voltage regulator is a low drop out (LDO) voltage regulator.

9. (Original) The voltage regulator according to claim 1, wherein the operational amplifier has a first input adapted for coupling to a voltage reference, and a second input coupled to the feedback loop.

10. (Original) The voltage regulator according to claim 1, wherein the operational amplifier is a low gain and high bandwidth amplifier.

11. (Original) The voltage regulator according to claim 10, wherein the low gain and high bandwidth amplifier is a folded-cascode amplifier.

12. The voltage regulator according to claim 11, wherein the operational amplifier comprises diode connected PMOS transistors for lowering an output impedance of the folded-cascode amplifier.

13. (Original) The voltage regulator according to claim 1, wherein the current buffer driver is an operational transconductance amplifier (OTA).

14. (Original) The voltage regulator according to claim 1, wherein the current feedback circuit senses a current change at the output power driver.

15. (Original) The voltage regulator according to claim 1, wherein the current feedback circuit provides transient enhancement for improved load regulation.

16. (Original) The voltage regulator according to claim 1, wherein the current feedback circuit provides a feedback voltage from an output voltage node.

17. (Original) The voltage regulator according to claim 1, wherein the current buffer driver has a low output impedance.

18. (Original) The voltage regulator according to claim 5, further comprising capacitors in the biasing circuit for improving noise immunity thereof.

19. (Original) The voltage regulator according to claim 1, wherein the voltage regulator is a USB voltage regulator.

20. (Original) The voltage regulator according to claim 1, wherein the current buffer driver has low input impedance and provides a high frequency pole that does not substantially affect the voltage regulator dominant pole.

REMARKS

This Application has been carefully reviewed in light of the Office Action mailed August 31, 2015. Claims 1-4, 7-17, and 19-20 were rejected and Claims 5-6 and 18 were objected to in the Office Action. Applicants respectfully request reconsideration and allowance of all pending claims.

Rejections under 35 U.S.C. § 102

Claims 1-4, 7-10, 13-17, and 20 were rejected under 35 U.S.C. §102(b) as being anticipated by *Xi* (US 6,246,221). Applicants respectfully traverse and submit the cited art does not teach all of the elements of the claimed embodiment of the invention.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Furthermore, "the identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co. Ltd.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). Applicants respectfully submit that the cited art as anticipated by the Examiner cannot anticipate the rejected Claims, because the cited art does not show all the elements of the present Claims.

Rejections under 35 U.S.C. §103

Claims 11-12 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Xi* in view of *Chang* (US 2013/0241505).

Claim 19 was rejected under 35 U.S.C. §103(a) as being unpatentable over *Xi*.

Applicants respectfully traverse and submit the cited art combinations, even if proper, which Applicant does not concede, does not render the claimed embodiment of the invention obvious.

In order to establish a prima facie case of obviousness, the references cited by the Examiner must disclose all claimed limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A.

1974). Even if each limitation is disclosed in a combination of references, however, a claim composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art. *KSR Int'l. Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1741 (2007). Rather, the Examiner must identify an apparent reason to combine the known elements in the fashion claimed. *Id.* "Rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *Id.*, citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006). Finally, the reason must be free of the distortion caused by hindsight bias and may not rely on ex post reasoning. *KSR*, 127 S.Ct. at 1742. In addition, evidence that such a combination was uniquely challenging or difficult tends to show that a claim was not obvious. *Leapfrog Enterprises, Inc. v. Fisher-Price, Inc. and Mattel, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007), citing *KSR*, 127 S.Ct. at 1741.

The Examiner stated that *Xi* allegedly discloses all the limitations of independent claim 1. Applicant respectfully disagrees.

Independent claim 1 includes amongst others:

"a gm enhanced current buffer driver;"

(emphasis added). *Xi* neither discloses nor suggest such a buffer. According to *Xi* a unity gain voltage buffer is implemented as buffer 210. The operational amplifier 212 is connected such that it forms a voltage follower by connecting the output directly with the inverting input and feeding an input signal to the non-inverting input. Thus, the output of operational amplifier 212 will be the same voltage as the input voltage. A current fed into the operational amplifier cannot be buffered by such a circuit. In fact, due to the high impedance at the input of operational amplifier 212, there is basically no input current flowing into the buffer 210.

Hence, *Xi* clearly fails to disclose the use of a current buffer between the operational amplifier 204 and the output power driver 206. Therefore, *Xi* cannot anticipate present claim 1. Applicants respectfully submit that the dependent Claims are allowable at least to the extent of the independent Claim 1 to which they refer, respectively. Thus, Applicants respectfully request reconsideration and allowance of the dependent Claims. Applicants reserve the right to make

further arguments regarding the Examiner's rejections under 35 U.S.C. ß103(a), if necessary, and do not concede that the Examiner's proposed combinations are proper.

Allowable Subject Matter

Applicants appreciate Examiner's consideration and indication that Claims 5-6 and 18 would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims. However, as stated above, Applicant respectfully submits that all pending claims are allowable in view of the cited art.

CONCLUSION

Applicants have made an earnest effort to place this case in condition for allowance in light of the remarks set forth above. Applicants respectfully request reconsideration of the pending claims.

Applicants believe there are no fees due at this time. However, the Commissioner is hereby authorized to charge any fees necessary or credit any overpayment to Deposit Account No. 50-6736 of SLAYDEN GRUBERT BEARD PLLC.

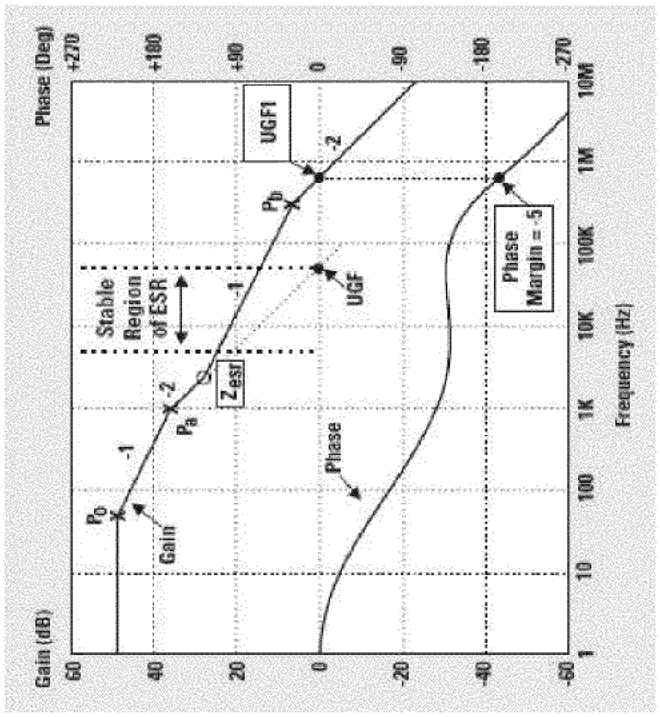
If there are any matters concerning this Application that may be cleared up in a telephone conversation, please contact Applicants' attorney at 512-402-3553.

Respectfully submitted,
SLAYDEN GRUBERT BEARD PLLC.
Attorney for Applicants

Andreas H. Grubert
Registration No. 59,143

Date: November 24, 2015

SEND CORRESPONDENCE TO:
SLAYDEN GRUBERT BEARD PLLC
CUSTOMER ACCOUNT NO. **86528**
512-402-3553

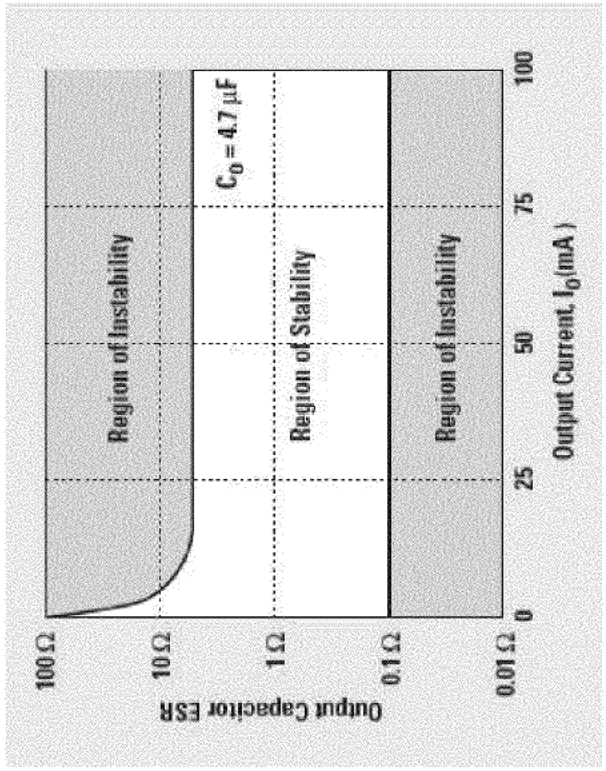


(a) Normal frequency response

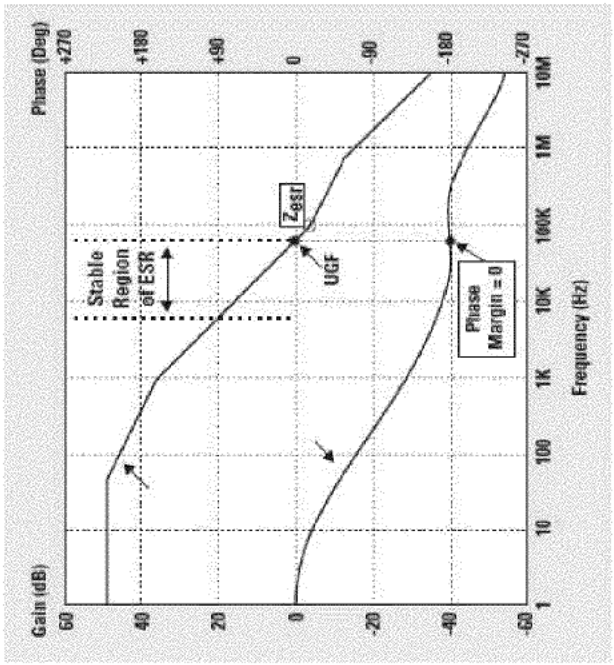
(b) ESR value too high

FIGURE 1

PRIOR ART



(d) "Tunnel of death"



(c) ESR value too low

FIGURE 1A

PRIOR ART

Electronic Acknowledgement Receipt

EFS ID:	24186460
Application Number:	14204011
International Application Number:	
Confirmation Number:	9205
Title of Invention:	USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor
First Named Inventor/Applicant Name:	Huamin Zhou
Customer Number:	86528
Filer:	Eric M. Grabski/Todd Rosson
Filer Authorized By:	Eric M. Grabski
Attorney Docket Number:	68354.225441
Receipt Date:	24-NOV-2015
Filing Date:	11-MAR-2014
Time Stamp:	20:31:58
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Response_OA_225441.pdf	157963 9fa0e44fc0788a9b10ba3f54cbac5277c16f5463	yes	10

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Specification	2	3
	Claims	4	6
	Applicant Arguments/Remarks Made in an Amendment	7	10

Warnings:					
Information:					
2	Drawings-only black and white line drawings	Replacement_Draws_225441.pdf	524285 f066811d70221902d2a7581205ec80c152fb4038	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	682248		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/204,011	Filing Date 03/11/2014	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	11/24/2015	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	**0**

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/ALA HUNTER/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/204,011	03/11/2014	Huamin Zhou	68354.225441

CONFIRMATION NO. 9205

86528
Slayden Grubert Beard PLLC
823 Congress Avenue
Suite 525
Austin, TX 78701

POA ACCEPTANCE LETTER

OC000000078724198

Date Mailed: 11/19/2015

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/07/2015.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/dtdinh/

PTO/SB/80 (11-08)
Approved for use through 11/30/2011. OMB 0651-0035
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:

☒ Practitioners associated with Customer Number: 86528

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:

☒ The address associated with Customer Number 86528

OR

☐ Firm or Individual Name			
Address			
City		State	Zip
Country			
Telephone		Email	

Assignee Name and Address:

MICROCHIP TECHNOLOGY INCORPORATED
2355 WEST CHANDLER BLVD.
CHANDLER, ARIZONA 85224-6199

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	April 11, 2009
Name	David Yeskey	Telephone	480.792.7509
Title	Director of Legal		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Electronic Acknowledgement Receipt

EFS ID:	24017833
Application Number:	14204011
International Application Number:	
Confirmation Number:	9205
Title of Invention:	USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor
First Named Inventor/Applicant Name:	Huamin Zhou
Customer Number:	86528
Filer:	Eric M. Grabski/Todd Rosson
Filer Authorized By:	Eric M. Grabski
Attorney Docket Number:	68354.225441
Receipt Date:	07-NOV-2015
Filing Date:	11-MAR-2014
Time Stamp:	21:21:03
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	POA_Microchip.pdf	270213 dd78f3a050cd05208d2731710994c37d33fb40c6	no	1

Warnings:	
Information:	

Total Files Size (in bytes):	270213

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/204,011	03/11/2014	Huamin Zhou	68354.225441	9205

86528 7590 08/31/2015

Slayden Grubert Beard PLLC
823 Congress Avenue
Suite 525
Austin, TX 78701

EXAMINER	
ZHANG, JUE	

ART UNIT	PAPER NUMBER
2838	

NOTIFICATION DATE	DELIVERY MODE
08/31/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

trosson@sgb-ip.com
patent@sgb-ip.com
wjenks@sgb-ip.com

Office Action Summary	Application No. 14/204,011	Applicant(s) ZHOU ET AL.	
	Examiner JUE ZHANG	Art Unit 2838	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/11/2014*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-4,7-17,19 and 20* is/are rejected.

8)☒ Claim(s) *5,6 and 18* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☒ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *3/11/2014* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *12/17/2014* .

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the application filed on 3/11/2014. Claims 1-20 are pending.

Notice of Pre-AIA or AIA Status

2. The present application is being examined under the pre-AIA first to invent provisions.

Priority

3. Applicant's claim for the benefit of a prior-filed application under 35 U.S.C. 119(e) or under 35 U.S.C. 120, 121, or 365(c) is acknowledged.

Specification

4. The Abstract is objected for containing claim language, such as "comprises". Correction is required. See MPEP § 608.01(b).

Drawing

5. Figures Fig. 1, 1A should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Information Disclosure Statement

6. The information disclosure statements (IDS) submitted on 12/17/2014 has been considered by the examiner.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-4, 7-10, 13-17, 20 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Xi (US Patent No. 6246221, hereinafter '221).

Claim 1, '221 teaches a voltage regulator (e.g., see Fig. 4-9), comprising:

an operational amplifier (e.g., 204);

a gm enhanced current buffer driver (e.g., the circuits comprising 202, 210, see Fig. 2);

an output power driver (e.g., 206), wherein the current buffer driver is coupled between the operational amplifier and the output power driver (e.g., see Fig. 2);

a current feedback circuit (e.g., 214, see col. 7 lines 50-53, claims 12-14 in view of Fig. 2) coupled between the output power driver and the current buffer driver; and a feedback loop coupled between the output power driver and the operational amplifier (e.g., the circuits providing Vfb, see Fig. 2).

Claim 2, '221 teaches the limitations of claim 1 as discussed above. It further teaches that a gm-boost circuit coupled to the current buffer driver (e.g., see Fig. 2).

Claim 3, '221 teaches the limitations of claim 2 as discussed above. It further teaches that wherein the gm-boost circuit increases the current buffer driver input impedance (e.g., see col. 7 lines 2-12 in view of Fig. 2).

Claim 4, '221 teaches the limitations of claim 2 as discussed above. It further teaches that wherein the gm-boost circuit enables the current buffer driver to have a large gm value (e.g., see col. 7 lines 50-53 in view of Fig. 2).

Claim 7, '221 teaches the limitations of claim 1 as discussed above. It further teaches that a compensation capacitor (e.g., Cc) coupled between the output power driver and a cascode node of the operational amplifier (e.g., see Fig. 2).

Claim 8, '221 teaches the limitations of claim 1 as discussed above. It further teaches that wherein the voltage regulator is a low drop out (LDO) voltage regulator (e.g., 200, see Fig. 2).

Claim 9, '221 teaches the limitations of claim 1 as discussed above. It further teaches that wherein the operational amplifier has a first input adapted for coupling to a voltage reference (e.g., Vref), and a second input coupled to the feedback loop (e.g., see Fig. 2).

Claim 10, '221 teaches the limitations of claim 1 as discussed above. It further teaches that wherein the operational amplifier is a low gain and high bandwidth amplifier (e.g., 204, see Fig. 2).

Claim 13, '221 teaches the limitations of claim 1 as discussed above. It further teaches that wherein the current buffer driver is an operational transconductance amplifier (OTA) (e.g., 204, see Fig. 2).

Claim 14, '221 teaches the limitations of claim 1 as discussed above. It further teaches that wherein the current feedback circuit senses a current change at the output power driver (e.g., see col. 7 lines 50-53, claims 12-14 in view of Fig. 2).

Claim 15, '221 teaches the limitations of claim 1 as discussed above. It further teaches that wherein the current feedback circuit provides transient enhancement for improved load regulation (e.g., see Fig. 23-28).

Claim 16, '221 teaches the limitations of claim 1 as discussed above. It further teaches that wherein the current feedback circuit provides a feedback voltage from an output voltage node (e.g., the current sensed through the current mirror pair 214, 206 from the node 224, see Fig. 2).

Claim 17, '221 teaches the limitations of claim 1 as discussed above. It further teaches that wherein the current buffer driver has a low output impedance (e.g., the output impedance of 210, see Fig. 2).

Claim 20, '221 teaches the limitations of claim 1 as discussed above. It further teaches that wherein the current buffer driver has low input impedance and provides a high frequency pole that does not substantially affect the voltage regulator dominant pole (e.g., see Abstract, col. 4 lines 11-17, col. 6 lines 16-27 in view of Fig. 1).

Claim Rejections - 35 USC § 103

9. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1,148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

> 1. Determining the scope and contents of the prior art.
> 2. Ascertaining the differences between the prior art and the claims at issue.
> 3. Resolving the level of ordinary skill in the pertinent art.
> 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

12. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xi (US Patent No. 6246221, hereinafter ‘221), in view of Chang (US PG Pub. No. 20130241505, hereinafter ‘505).

Claim 11, ‘221 teaches the limitations of claim 10 as discussed above. ‘221 does not explicitly disclose that wherein the low gain and high bandwidth amplifier is a folded-cascode amplifier.

‘221 discloses a voltage regulator with miller compensation (e.g., see Abstract; Fig. 1-3). It further discloses that it is preferable to use a folded-cascode amplifier as its first stage amplifier (e.g., see [0014] in view of Fig. 1).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to modify the voltage regulator circuit to include the folded-cascode amplifier as its the first stage amplifier as disclosed in ‘505, because it is preferable, as demonstrated by ‘505, to use a folded-cascode amplifier as the first stage amplifier in voltage regulator circuits.

Claim 12, the combination of “221 and “505 teach the limitations of claim 11 as discussed above. ‘221 further discloses that wherein the operational amplifier comprises diode connected PMOS transistors (e.g., MP8, MP58, MP32) for lowering an output impedance of the folded-cascode amplifier (e.g., see Fig. 4).

13. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Xi (US Patent No. 6246221, hereinafter ‘221).

Claim 19, ‘221 dislcoses the claimed invention except for explicitly disclosing that wherein the voltage regulator is a USB voltage regulator. However, It would have been obvious to one having ordinary skill in the art at the time of invention was made to modify the voltage regulator circuit to use the voltage regulator of ‘221as a USB voltage regulator, because it is dynamically adaptable, as demonstrated by ‘505, to either the light load or the heavy load (e.g., see [0006]).

Allowable Subject Matter

14. Claims 5, 6, 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. The following is a statement of reasons for the indication of allowable subject matters:

For claims 5, 6, 18, the prior art does not disclose or suggest, in combination with the limitations of the base claim and any intervening claims, primarily, … a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver.

Examiner's Note:

16. Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

17. In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jue Zhang whose telephone number is (571) 270-1263. The examiner can normally be reached on M-TH 8:00-5:00PM EST, Other F 8:00AM-4:00PM EST

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Monica Lewis can be reached on 571-272-1838. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JUE ZHANG/
Primary Examiner, Art Unit 2838

Notice of References Cited	Application/Control No. 14/204,011	Applicant(s)/Patent Under Reexamination ZHOU ET AL.	
	Examiner JUE ZHANG	Art Unit 2838	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-6,246,221 B1	06-2001	Xi; Xiaoyu	G05F1/575	323/280
*	B	US-2013/0241505 A1	09-2013	CHANG; JUNG-FU	G05F1/575	323/282
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 9205

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/204,011	03/11/2014 RULE	323	2838	68354.225441

APPLICANTS
Microchip Technology Incorporated, Chandler, AZ

INVENTORS
Huamin Zhou, Chandler, AZ;
Woowai Martin, Phoenix, AZ;
Cristian Albina, Chandler, AZ;
Fritz Schlunder, Gilbert, AZ;
Minh Le, Gilbert, AZ;

**** CONTINUING DATA **************************
This appln claims benefit of 61/780,985 03/14/2013

**** FOREIGN APPLICATIONS **************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
03/27/2014

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /JUE ZHANG/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		AZ	8	20	1

ADDRESS
Slayden Grubert Beard PLLC
823 Congress Avenue
Suite 525
Austin, TX 78701
UNITED STATES

TITLE
USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor

FILING FEE RECEIVED	FEES: Authority has been given in Paper	☐ All Fees
1600	No._____ to charge/credit DEPOSIT ACCOUNT	☐ 1.16 Fees (Filing)
	No._____ for following:	☐ 1.17 Fees (Processing Ext. of time)
		☐ 1.18 Fees (Issue)
		☐ Other _____
		☐ Credit

Receipt date: 12/17/2014

PTO-1449 **Information Disclosure Citation in an Application**	Application No. 14/204,011	Applicant(s) Huamin Zhou et al.	
	Docket Number 68354.225441	Group Art Unit 2838	Filing Date March 11, 2014

U.S. PATENT DOCUMENTS

		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	A.	2005/0168272 A1	08-04-05	Banerjee et al.	327	541	02-02-04
	B.	2006/0192538 A1	08-31-06	Wang et al.	323	282	05-23-05
	C.	7312598 B1	12-25-07	Huang	323	280	08-25-06
	D.	2009/0009147 A1	01-08-09	Jian	323	280	03-04-08
	E.						
	F.						
	G.						
	H.						
	I.						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	J.							
	K.							
	L.							
	M.							
	N.							
	O.							
	P.							
	Q.							
	R.							

NON-PATENT DOCUMENTS

		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
	S.	International Search Report and Written Opinion, Application No. PCT/US2014/023962, 16 pages	11-03-14
	T.		
	U.		

EXAMINER /Jue Zhang/	DATE CONSIDERED 08/23/2015

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

24577061

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.Z./

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	2916	G05F1/575.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	ON	2015/08/23 13:30
L4	1124	323/280.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	ON	2015/08/23 13:30
L5	3667	3 4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	ON	2015/08/23 13:30
L7	121	5 miller near compensat$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	AND	ON	2015/08/23 13:31
L8	59	7 (gm or transconductance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2015/08/23 13:32
L9	33	7 (gm or transconductance) bias	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2015/08/23 13:33
L10	0	7 (gm or transconductance) bias near ratio	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2015/08/23 13:33

EAST Search History (Prior Art)

L11	1	5 (gm or transconductance) bias near ratio	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2015/08/23 13:33
L13	1322	H03F3/45192.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	ON	2015/08/23 13:42
L14	73	13 miller near compensat$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	AND	ON	2015/08/23 13:42
L15	47	14 (gm or transconductance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2015/08/23 13:42
L16	1	13 (gm or transconductance) bias near ratio	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2015/08/23 13:43
L17	0	14 voltage near regulator	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2015/08/23 13:44
S1	1	((Huamin) near2 (Zhou)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/08/09 14:51
S2	4	((Woowai) near2 (Martin)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/08/09 14:52
S3	2	((Cristian) near2 (Albina)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/08/09 14:52
S4	1	((Fritz) near2 (Schlunder)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/08/09 14:52

EAST Search History (Prior Art)

S5	348	((Minh) near2 (Le)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/08/09 14:52
S6	54	((Huamin) near2 (Zhou)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/09 14:52
S7	14	((Woowai) near2 (Martin)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/09 14:52
S8	5	((Cristian) near2 (Albina)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/09 14:53
S9	3	((Fritz) near2 (Schlunder)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/09 14:53
S10	903	((Minh) near2 (Le)).INV.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/09 14:53
S11	67	S6 S7 S8 S9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/09 14:53
S12	961	S6 S7 S8 S9 S10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/09 14:53

EAST Search History (Prior Art)

S13	3	S12 gm voltage regulator	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2015/08/09 14:54
S14	1	(("200500168272") or ("200600192538") or ("7312598") or ("200900009147")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/08/09 14:56
S15	4	(("20050168272") or ("20060192538") or ("7312598") or ("20090009147")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/08/09 14:56
S16	0	(("201361780985") or ("201414204011")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/08/09 14:58
S17	1	gm enhanced current buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	NEAR	ON	2015/08/09 15:00
S18	0	gm enhanced buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	NEAR	ON	2015/08/09 15:00
S19	3	gm current buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	NEAR	ON	2015/08/09 15:01
S20	18	gm with current buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	NEAR	ON	2015/08/09 15:01
S21	1	(gm or transconductance) enhanced current buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	NEAR	ON	2015/08/09 15:03

EAST Search History (Prior Art)

S22	6	S12 (gm or transconductance) voltage regulator	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2015/08/09 15:03
S23	299	(gm or transconductance) with voltage near regulator	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2015/08/09 15:04
S24	13	(gm or transconductance) enhanc$3 current near buffer voltage near regulator	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	AND	ON	2015/08/09 15:05
S25	2	(gm or transconductance) enhanc$3 current near buffer voltage near regulator with (low near drop near out or LDO)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	AND	ON	2015/08/09 15:11
S26	3	(gm or transconductance) with (enhanc$3 or boost$3) current near buffer voltage near regulator with (low near drop near out or LDO)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	AND	ON	2015/08/09 15:12
S27	1	"US 20150220094"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2015/08/09 15:14
S28	6	(gm or transconductance) with (enhanc$3 or boost$3) current near feedback (low near drop near out or LDO)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	AND	ON	2015/08/09 15:38
S30	176	folded-cascode amplifier	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	NEAR	ON	2015/08/09 16:49

EAST Search History (Prior Art)

S31	8508	folded-cascode near amplifier ldo	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	ON	2015/08/09 16:50
S32	1	folded-cascode near amplifier ldo	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	AND	ON	2015/08/09 16:50
S33	16	folded-cascode near amplifier voltage regulator	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	AND	ON	2015/08/09 16:51

EAST Search History (Interference)

		<This search history is empty>				

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14204011	ZHOU ET AL.
	Examiner	Art Unit
	JUE ZHANG	2838

CPC- SEARCHED		
Symbol	Date	Examiner
G05F1/575	8/23/2015	
H03F3/45192	8/23/2015	

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
323	280	8/23/2015	

SEARCH NOTES		
Search Notes	Date	Examiner
See east search notes	8/23/2015	JZ
Inventor name search	8/23/2015	JZ

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Huamin Zhou et al.
Serial No.:	14/204,011
Date Filed:	March 11, 2014
Group Art Unit:	2838
Confirmation No.:	9205
Examiner:	Lewis, Monica
Title:	**USB REGULATOR WITH CURRENT BUFFER TO REDUCE COMPENSATION CAPACITOR SIZE AND PROVIDE FOR WIDE RANGE OF ESR VALUES OF EXTERNAL CAPACITOR**

MAIL STOP - AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

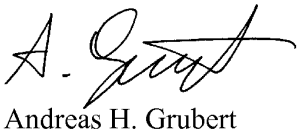
INFORMATION DISCLOSURE STATEMENT

Applicants respectfully request, pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, that the references listed on the attached PTO-1449 form, be considered and cited in the examination of the above-identified application. Pursuant to 37 C.F.R. 1.98(a)(2), legible copies of any foreign patents, unpublished U.S. applications, and/or non-patent published documents cited on the attached PTO Form 1449 are being submitted with this Information Disclosure Statement. Consistent with the provisions of 37 C.F.R. § 1.97(h), this submission does not constitute an admission or representation that the submitted reference(s) is/are material to the patentability of the subject matter disclosed in the application.

Applicants believe there are no fees due at this time, however, the Commissioner is hereby authorized to charge any fees necessary or credit any overpayment to Deposit Account No. 50-4871 of King & Spalding L.L.P.

If there are any matters concerning this Application that may be cleared up in a telephone conversation, please contact Applicants' attorney at 512.457.2030.

Respectfully submitted,
KING & SPALDING LLP
Attorney for Applicants



Andreas H. Grubert
Registration No. 59,143

Date: December 17, 2014

SEND CORRESPONDENCE TO:
KING & SPALDING L.L.P.
CUSTOMER ACCOUNT NO. **86528**
512-457-2025
512-457-2100 (fax)

PTO-1449 **Information Disclosure Citation in an Application**	Application No. 14/204,011	Applicant(s) Huamin Zhou et al.	
	Docket Number 68354.225441	Group Art Unit 2838	Filing Date March 11, 2014

U.S. PATENT DOCUMENTS

		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	A.	2005/0168272 A1	08-04-05	Banerjee et al.	327	541	02-02-04
	B.	2006/0192538 A1	08-31-06	Wang et al.	323	282	05-23-05
	C.	7312598 B1	12-25-07	Huang	323	280	08-25-06
	D.	2009/0009147 A1	01-08-09	Jian	323	280	03-04-08
	E.						
	F.						
	G.						
	H.						
	I.						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	J.							
	K.							
	L.							
	M.							
	N.							
	O.							
	P.							
	Q.							
	R.							

NON-PATENT DOCUMENTS

		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
	S.	International Search Report and Written Opinion, Application No. PCT/US2014/023962, 16 pages	11-03-14
	T.		
	U.		

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

24577061

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:
Slayden, Bruce W. Ii
KING & SPALDING LLP
401 Congress Avenue, Suite 3200
Austin, TX 78701
ETATS-UNIS D'AMERIQUE

RECEIVED
NOV 12 2014
KING & SPALDING

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

Applicant's or agent's file reference 68354.227590	Date of mailing *(day/month/year)* 3 November 2014 (03-11-2014) **FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. PCT/US2014/023962	International filing date *(day/month/year)* 12 March 2014 (12-03-2014)
Applicant MICROCHIP TECHNOLOGY INCORPORATED	

1. [X] The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the International Application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the International Search Report.

   How? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Fascimile No.: (41-22) 338.82.70

   For more detailed instructions, see *PCT Applicant's Guide*, International Phase, paragraphs 9.004 - 9.011.

2. [ ] The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. [ ] **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   [ ] the protest together with the decision thereon has been transmitted to the International Bureau together with any applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

   [ ] no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   The applicant may **submit comments on an informal basis on the written opinion of the International Searching Authority** to the International Bureau. These comments will be made available to the public after international publication. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established.

   Shortly after the expiration of **18 months from the priority date, the international application will be published** by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90*bis*.1 and 90*bis*.3).

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for **entry into the national phase** before those designated Offices. In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months. For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the *PCT Applicant's Guide*, National Chapters.

   Within **19 months from the priority date, the applicant may request that a supplementary international search be carried out** by a different International Searching Authority that offers this service (Rule 45*bis*.1). The procedure for requesting supplementary international search is described in the *PCT Applicant's Guide*, International Phase, paragraphs 8.006-8.032.

Name and mailing address of the International Searching Authority European Patent Office, P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk Tel. (+31-70) 340-2040 Fax: (+31-70) 340-3016	Authorized officer KLáG, Brigitta Tel: +31 (0)70 340-1034

Form PCT/ISA/220 (July 2014)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
68354.227590		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US2014/023962	12 March 2014 (12-03-2014)	14 March 2013 (14-03-2013)
Applicant		
MICROCHIP TECHNOLOGY INCORPORATED		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 5 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language,** the international search was carried out on the basis of:
      ☒ the international application in the language in which it was filed
      ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (See Box No. II)

3. ☒ **Unity of invention is lacking** (see Box No III)

4. With regard to the **title,**
   ☒ the text is approved as submitted by the applicant
   ☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**
   ☒ the text is approved as submitted by the applicant
   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority

6. With regard to the **drawings,**
   a. the figure of the **drawings** to be published with the abstract is Figure No. 2
      ☐ as suggested by the applicant
      ☒ as selected by this Authority, because the applicant failed to suggest a figure
      ☐ as selected by this Authority, because this figure better characterizes the invention
   b. ☐ none of the figures is to be published with the abstract

Form PCT/ISA/210 (first sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/023962

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-6, 8, 9, 13-17, 19, 20

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/023962

A. CLASSIFICATION OF SUBJECT MATTER
INV. G05F1/575
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G05F H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005/168272 A1 (BANERJEE JAIDEEP [IN] ET AL) 4 August 2005 (2005-08-04) abstract; figures 1,2	1-6,8,9, 13-17, 19,20
X	US 2006/192538 A1 (WANG WEI [CN] ET AL) 31 August 2006 (2006-08-31) abstract; figure 4	1-6,8,9, 13-16, 19,20
A	US 2009/009147 A1 (JIAN MING-HONG [TW]) 8 January 2009 (2009-01-08) abstract; figure 8	1-6,8,9, 13-17, 19,20
A	US 7 312 598 B1 (HUANG SHENGMING [GB]) 25 December 2007 (2007-12-25) abstract; figure 2A	1-6

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 July 2014	03/11/2014

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Arias Pérez, Jagoba

1

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2014/023962

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2005168272 A1	04-08-2005	NONE	
US 2006192538 A1	31-08-2006	TW I285804 B	21-08-2007
		US 2006192538 A1	31-08-2006
US 2009009147 A1	08-01-2009	JP 2009015810 A	22-01-2009
		TW 200903988 A	16-01-2009
		US 2009009147 A1	08-01-2009
US 7312598 B1	25-12-2007	NONE	

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-6, 8, 9, 13-17, 19, 20

   Voltage regulator having a biasing circuit with an enable/disable function.

   ---

2. claims: 7, 10-12

   Voltage regulator having a folded cascode amplifier.

   ---

3. claim: 18

   Voltage regulator having a biasing circuit with capacitors.

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

see form PCT/ISA/220

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY
(PCT Rule 43*bis*.1)

Date of mailing
(day/month/year) see form PCT/ISA/210 (second sheet)

Applicant's or agent's file reference
see form PCT/ISA/220

FOR FURTHER ACTION
See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2014/023962	12.03.2014	14.03.2013

International Patent Classification (IPC) or both national classification and IPC
INV. G05F1/575

Applicant
MICROCHIP TECHNOLOGY INCORPORATED

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☒ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☒ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notifed the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA:	Date of completion of this opinion	Authorized Officer
European Patent Office P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk - Pays Bas Tel. +31 70 340 - 2040 Fax: +31 70 340 - 3016	see form PCT/ISA/210	Arias Pérez, Jagoba Telephone No. +31 70 340-4194

Form PCT/ISA/237 (Cover Sheet) (July 2009)

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1 (b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43bis.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing filed or furnished:

   a. (means)

      ☐ on paper

      ☐ in electronic form

   b. (time)

      ☐ in the international application as filed

      ☐ together with the international application in electronic form

      ☐ subsequently to this Authority for the purposes of search

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability

The questions whether the claimed invention appears to be novel, to involve an inventive step (to be non obvious), or to be industrially applicable have not been examined in respect of

☐ the entire international application

☒ claims Nos. 7, 10-12, 18

because:

☐ the said international application, or the said claims Nos. relate to the following subject matter which does not require an international search *(specify)*:

☐ the description, claims or drawings *(indicate particular elements below)* or said claims Nos. are so unclear that no meaningful opinion could be formed *(specify)*:

☐ the claims, or said claims Nos. are so inadequately supported by the description that no meaningful opinion could be formed *(specify)*:

☒ no international search report has been established for the whole application or for said claims Nos. 7, 10-12, 18

☐ a meaningful opinion could not be formed without the sequence listing; the applicant did not, within the prescribed time limit:

- ☐ furnish a sequence listing on paper complying with the standard provided for in Annex C of the Administrative Instructions, and such listing was not available to the International Searching Authority in a form and manner acceptable to it.
- ☐ furnish a sequence listing in electronic form complying with the standard provided for in Annex C of the Administrative Instructions, and such listing was not available to the International Searching Authority in a form and manner acceptable to it.
- ☐ pay the required late furnishing fee for the furnishing of a sequence listing in response to an invitation under Rules 13*ter*.1(a) or (b).

☐ See Supplemental Box for further details

Box No. IV Lack of unity of invention

1. ☒ In response to the invitation (Form PCT/ISA/206) to pay additional fees, the applicant has, within the applicable time limit:

   ☐ paid additional fees

   ☐ paid additional fees under protest and, where applicable, the protest fee

   ☐ paid additional fees under protest but the applicable protest fee was not paid

   ☒ not paid additional fees

2. ☐ This Authority found that the requirement of unity of invention is not complied with and chose not to invite the applicant to pay additional fees.

3. This Authority considers that the requirement of unity of invention in accordance with Rule 13.1, 13.2 and 13.3 is

   ☐ complied with

   ☒ not complied with for the following reasons:

   see separate sheet

4. Consequently, this report has been established in respect of the following parts of the international application:

   ☐ all parts.

   ☒ the parts relating to claims Nos. 1-6, 8, 9, 13-17, 19, 20

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	6, 19
	No:	Claims	1-5, 8, 9, 13-17, 20
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-6, 8, 9, 13-17, 19, 20
Industrial applicability (IA)	Yes:	Claims	1-6, 8, 9, 13-17, 19, 20
	No:	Claims	

2. Citations and explanations

see separate sheet

Re Item IV

Lack of unity of invention

1 The following documents (D) are referred to in this communication:

D1 US 2005/168272 A1 (BANERJEE et al) 4 August 2005

D2 US 2006/192538 A1 (WANG et al) 31 August 2006

2 The application lacks unity within the meaning of Rule 13.1 PCT because for the reasons given below, the following inventions are not linked so as to form a single general inventive concept:

(a) Claims 1 to 6, 8, 9, 13 to 17, 19 and 20: Voltage regulator having a biasing circuit with an enable/disable function.

(b) Claims 7 and 10 to 12: Voltage regulator having a folded cascode amplifier.

(c) Claim 18: Voltage regulator having a biasing circuit with capacitors.

The closest prior art for the sake of assessing non-unity has been identified as D1 (US2005/0168272). This document (see figures 1 and 2 and accompanying text) discloses a voltage regulator (10) comprising an operational amplifier (12); a gm enhanced current buffer driver (14); an output power driver(16), wherein the current buffer driver (14) is coupled between the operational amplifier (12) and the output power driver (16); a current feedback circuit (18) coupled between the output power driver (16) and the current buffer driver (14); and a feedback loop (17) coupled between the output power driver (16) and the operational amplifier (12).

Hence D1 anticipates all the technical features of independent claim 1, whose subject-matter is therefore not new. Since claim 1 does not contribute to the prior art, its features cannot be considered to constitute "special technical features" (STF) of the invention in the sense of Rule 13.2 PCT. The first claim depending on claim 1 whose subject-matter contains a contribution over the prior art disclosed in D1 is claim 6.

2.1 The following technical feature of the first invention can be seen to make a contribution over the teaching of D1 and is therefore considered to be an STF of the invention in the sense of Rule 13.2 PCT (see claim 6):

- The voltage regulator comprises an enable/disable function to enable/ disable the biasing circuit for reducing standby current.

The objective technical problem to be solved by this STF may be seen to reduce the current consumed by the regulator when it is not in use.

2.2 Likewise, the STF of the second invention is:

- The operational amplifier is a folded cascode amplifier.

The objective technical problem to be solved by this STF may be seen to reduce the complexity of the frequency compensation, while providing a good driving capacity for the buffer (see from page 5, line 25 to page 6, line 2).

2.3 Similarly, the STF of the third invention is:

- The biasing circuit comprises capacitors.

The objective technical problem is to improve the noise immunity of the biasing circuit.

2.4 Thus the groups of claims mentioned above do not present a single common special technical feature, nor are these special technical features corresponding ones, since they do not solve a single common objective problem since they do not solve a single common objective problem which is new and inventive. Therefore the technical relationship required by Rule 13.2 PCT is not present between these groups of claims.

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

3 The application does not meet the requirements of Article 6 PCT, because claims 1 to 5, 15, 17 and 20 are not clear.

3.1 In claim 1, the expression "a gm enhanced current buffer driver" does not have a recognised meaning in the field of electronics. The term "gm" seems to refer to the transconductance of the buffer, which seems to be "enhanced"; however an improvement of any circuit needs a reference to establish with respect to which other circuit this particular value has been improved. In its absence, any buffer can be considered to improve another buffer which is not part of the claim.

Moreover this expression merely defines the subject-matter in terms of the result to be achieved, which merely amounts to a statement of the underlying problem, without providing the technical features necessary for achieving this result.

The same objection applies *mutatis mutandis* to claims 2 to 4, 15 and 20.

3.2 In claim 4, the expression "a large gm value" is vague and indefinite, since it is not clear how large a gm value needs to be to be considered "large". This expression should be replaced by a functional feature or a range of values

that, being directly and unambiguously derivable from the application as filed, allows the skilled person to objectively establish whether a certain gm value is large enough to fall within the scope of the claim.

A similar objection applies claims 17 and 20.

3.3 In claim 5, the expression "to set a biasing ratio for gm-boost of the current driver" is not clear because it does not define what kind of ratio is such biasing ratio (is a ration between resistors? transistors? currents?). However it is not clear from the application what magnitudes are linked by this ratio or what is its desired effect and therefore this feature should be excised.

4 The present application does not meet the requirements of Article 33(2) PCT, because, with respect to each of documents D1 and D2 taken in isolation, the subject-matter of independent claim 1 is not new.

4.1 Document D1, for the reasons given in section 2.1 above, discloses in combination all technical features of claim 1, whose subject-matter is therefore not new.

4.2 The subject-matter of claim 1 is also known from D2 (see in particular figure 4). Document D2 discloses a voltage regulator (200), comprising an operational amplifier (210); a gm enhanced current buffer driver (73); an output power driver (230), wherein the current buffer driver (73) is coupled between the operational amplifier (210) and the output power driver (230); a current feedback circuit (220) coupled between the output power driver (230) and the current buffer driver (73); and a feedback loop (240) coupled between the output power driver (230) and the operational amplifier (210).

Hence also D2 discloses in combination all technical features of claim 1, whose subject-matter is therefore not new.

5 Dependent claims 2 to 6, 8, 9, 13 to 17, 19 and 20 do not contain any additional features which, in combination with the features of any claim to which they refer, meet the requirements of Article 33(2) and (3) PCT regarding novelty and inventive step.

5.1 The additional features of claims 2 to 4 are known from D1 (see figure 2), where the gm-boost circuit is considered to be transistor 50. This transistor is connected as a source bias, which increases the transconductance (gm) of the buffer (14) and its input impedance.

5.2 The features added by claim 5 are known from D1, where a biasing circuit is disclosed to bias the gm-boost transistor 50 (see figure 2 and paragraph [0019]).

5.3 The features added by claim 6 constitute a well known standard technique to reduce power consumption in circuits. The skilled person would readily add such a function to the voltage regulator of D1 or D2 whenever she wanted to be able to put the load of the regulator in sleep mode.

5.4 The additional features of claim 8 are known from D1 (see paragraph [0001]), where the regulator disclosed therein is defined as an LDO regulator. Those of claim 9 are also known from D1 (see figure 1), where the operational amplifier (12) has a first input coupled to a reference voltage (VREF) and a second input coupled to the feedback loop (VFB, 17).

5.5 The features added by claims 13 and 17 are also known from D1 (see figure 2), where the current buffer driver (14) is disclosed to be a PMOS transistor in common drain configuration, exactly as the buffer driver of the present application (compare with figure 3B, transistor 384) and therefore it forms an operational transconductance amplifier.

5.6 The additional features of claims 14 to 16 are also known from D1 (see figure 2, feedback circuit 18) and D2 (see figure 4, block 220), where the feedback circuits of both voltage regulators sense the output current and provides

transient enhancement. In particular both current feedback circuits are identical to the current feedback circuit in the present application (see figure 3B, transistors 374, 376, 378, 400 and 402).

5.7 The features added by claim 19 constitute a well known standard technique to provide a USB bus with regulated voltage. Those of claim 20 are also known from D1.

6 For the sake of completeness the following minor deficiencies are mentioned:

6.1 Contrary to the requirements of Rule 5.1(a)(ii) PCT, the documents D1 and D2 are not identified in the description and the relevant background art disclosed therein is not at least briefly discussed.

6.2 Contrary to the requirements of Rule 6.3(b) PCT, the independent claims are not properly drafted in the two-part form, with those features which in combination are part of the closest prior art (cf. document D1) being placed in the preamble.

6.3 No reference signs in parentheses have been inserted in the claims to increase their intelligibility (Rule 6.2(b) PCT). This applies to both the preamble and characterising portion.

6.4 The application contains passages (see page 1, lines 6 to 8 and from page 7, line 27 to the end) which incorporate external documents to the present application by reference and that try to extend the scope of protection of the claims in an unclear and not defined way. These passages should be excised.

7 Because of the reasons stated in sections 2 to 6 above, claims 1 to 6, 8, 9, 13 to 17, 19 and 20 are not allowable. However, in view of the available prior art, it appears that if the construction of the current buffer as shown in figure 3B were introduced in the independent claim, the resulting subject-matter would be new and inventive.

Electronic Acknowledgement Receipt

EFS ID:	20985385
Application Number:	14204011
International Application Number:	
Confirmation Number:	9205
Title of Invention:	USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor
First Named Inventor/Applicant Name:	Huamin Zhou
Customer Number:	86528
Filer:	Eric M. Grabski/Jennie Averyt
Filer Authorized By:	Eric M. Grabski
Attorney Docket Number:	68354.225441
Receipt Date:	17-DEC-2014
Filing Date:	11-MAR-2014
Time Stamp:	10:48:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	IDS_225441.pdf	96763 b4f069aed0b458bf7b43a349b4cd31ca7642da75	no	3

Warnings:	
Information:	

This is not an USPTO supplied IDS fillable form					
2	Other Reference-Patent/App/Search documents	ISR_225441.pdf	650777 6a427c208b3c073426f217676b43f9223ec0f635	no	16
Warnings:					
Information:					
			Total Files Size (in bytes):	747540	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/204,011	03/11/2014	Huamin Zhou	68354.225441

CONFIRMATION NO. 9205

86528
King & Spalding LLP
401 Congress Avenue
Suite 3200
Austin, TX 78701

PUBLICATION NOTICE

Title:USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor

Publication No.US-2014-0266107-A1
Publication Date:09/18/2014

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/204,011	03/11/2014	2838	1600	68354.225441	20	1

CONFIRMATION NO. 9205

86528
King & Spalding LLP
401 Congress Avenue
Suite 3200
Austin, TX 78701

FILING RECEIPT

Date Mailed: 03/31/2014

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Huamin Zhou, Chandler, AZ;
Woowai Martin, Phoenix, AZ;
Cristian Albina, Chandler, AZ;
Fritz Schlunder, Gilbert, AZ;
Minh Le, Gilbert, AZ;

Applicant(s)

Microchip Technology Incorporated, Chandler, AZ

Power of Attorney: None

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/780,985 03/14/2013

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 03/27/2014
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/204,011**
Projected Publication Date: 09/18/2014

Non-Publication Request: No

Early Publication Request: No

Title

USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor

Preliminary Class

323

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 14/204,011

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600

APPLICATION AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

PTO/AIA/14 (08-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	68354.225441
	Application Number	
Title of Invention	USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Huamin		Zhou	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Chandler	State/Province	AZ	Country of Residence	US

Mailing Address of Inventor:

Address 1	733 W. Armstrong Way		
Address 2			
City	Chandler	State/Province	AZ
Postal Code	85286	Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Woowai		Martin	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Phoenix	State/Province	AZ	Country of Residence	US

Mailing Address of Inventor:

Address 1	14217 South 5th Street		
Address 2			
City	Phoenix	State/Province	AZ
Postal Code	85048	Country	US

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Cristian		Albina	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	68354.225441
	Application Number	
Title of Invention	USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor	

City	Chandler	State/Province	AZ	Country of Residence i	US

Mailing Address of Inventor:

Address 1	400 North Coronado St., Apt. #1099		
Address 2			
City	Chandler	State/Province	AZ
Postal Code	85224	Country i	US

Inventor 4 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Fritz		Schlunder	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	Gilbert	State/Province	AZ	Country of Residence i	US

Mailing Address of Inventor:

Address 1	1129 Nancy Lane		
Address 2			
City	Gilbert	State/Province	AZ
Postal Code	85296	Country i	US

Inventor 5 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Minh		Le	

Residence Information (Select One) (•) US Residency ( ) Non US Residency ( ) Active US Military Service

City	Gilbert	State/Province	AZ	Country of Residence i	US

Mailing Address of Inventor:

Address 1	711 West Desert Avenue		
Address 2			
City	Gilbert	State/Province	AZ
Postal Code	85233	Country i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

PTO/AIA/14 (08-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	68354.225441
	Application Number	
Title of Invention	USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor	

Customer Number	86528		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor		
Attorney Docket Number	68354.225441	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	8	Suggested Figure for Publication (if any)	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	86528		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	non provisional of	61780985	2013-03-14

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

PTO/AIA/14 (08-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	68354.225441
	Application Number	
Title of Invention	USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor	

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country i	Filing Date (YYYY-MM-DD)	Priority Claimed
			○ Yes ◉ No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (08-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	68354.225441
	Application Number	
Title of Invention	USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor	

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Remove

○ Assignee	○ Legal Representative under 35 U.S.C. 117
◉ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Assignee is an Organization check here. ☒

Organization Name	Microchip Technology Incorporated		
Mailing Address Information:			
Address 1	2355 West Chandler Blvd.		
Address 2			
City	Chandler	**State/Province**	AZ
Country [i]	US	Postal Code	85244-6199
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications

Signature	/Andreas H. Grubert/			Date (YYYY-MM-DD)	2014-03-11
First Name	Andreas H.	Last Name	Grubert	Registration Number	59143

Additional Signature may be generated within this form by selecting the Add button. Add

PTO/AIA/14 (08-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	68354.225441
	Application Number	
Title of Invention	USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT APPLICATION COVER SHEET

FOR

USB REGULATOR WITH CURRENT BUFFER TO REDUCE COMPENSATION CAPACITOR SIZE AND PROVIDE FOR WIDE RANGE OF ESR VALUES OF EXTERNAL CAPACITOR

Inventors:

Huamin Zhou
733 W. Armstrong Way
Chandler, Arizona 85286
Citizenship: China

Fritz Schlunder
1129 Nancy Lane
Gilbert, Arizona 85296
Citizenship: U.S.A.

Woowai Martin
14217 South 5th Street
Phoenix, Arizona 85048
Citizenship: U.S.A.

Minh Le
711 West Desert Ave.
Gilbert, Arizona 85233
Citizenship: U.S.A.

Cristian Albina
400 North Coronado St., Apt. 1099
Chandler, Arizona 85224
Citizenship: Germany

Assignee: Microchip Technology Incorporated

Attorney: Andreas H. Grubert
King & Spalding LLP
401 Congress Ave.
Suite 3200
Austin, TX 78701
(Customer Number 86528)

Attorney Docket No.: 68354.225441

Client Reference: MTI-3670.US.0

22533539

USB REGULATOR WITH CURRENT BUFFER TO REDUCE COMPENSATION CAPACITOR SIZE AND PROVIDE FOR WIDE RANGE OF ESR VALUES OF EXTERNAL CAPACITOR

RELATED PATENT APPLICATION

[0001] This application claims priority to commonly owned United States Provisional Patent Application Serial Number 61/780,985; filed March 14, 2013; which is hereby incorporated by reference herein for all purposes.

TECHNICAL FIELD

[0002] The present disclosure relates to USB voltage regulators, and, more particularly, to a USB voltage regulator having **a** current buffer to reduce compensation capacitor size and provide for a wide range of external compensation capacitor ESR values.

BACKGROUND

[0003] USB voltage regulators operate with extremely low equivalent series resistance (ESR) values, for example around 10 milliohms. This ESR value is not very accurate because the ceramic capacitor manufacturers rarely specify the value of ESR in their data sheets. Additionally, the exact value depends on the size/voltage rating design of the external capacitor, and can vary based on user connection topology (circuit board layout and components used thereon), *e.g.*, putting multiple small capacitors in parallel, thereby reducing ESR; or using thin/long printed circuit board traces to connect to the capacitor, thereby adding copper trace resistance ESR. Typically the externally compensated low-drop out (LDO) voltage regulator uses large value external capacitors for stability with a limited range of ESR ratings. The ESR values will heavily impact the design of LDO voltage regulators due to its variable zero pole locations depending upon the load conditions. Therefore existing products having a USB interface use standard voltage regulator architectures that require very large external capacitor sizes with variations of ESR values in order to keep the voltage regulator stable.

[0004] Referring to Figures 1 and 1A, depicted are various frequency response graphs showing different ESR situations. Figure 1(a) shows a desired normal frequency response. Figure 1(b) shows a situation where the ESR is too high. Figure 1A(c) shows a situation where the ESR is too low. And Figure 1A(d) shows ESRs resulting in the dreaded "tunnel of death."

SUMMARY

[0005] Therefore a need exists to significantly improve the range of external capacitors with small to large ESR values and reduce the size of the internal compensation capacitance value for stabilizing an associated voltage regulator, especially a low-drop out (LDO) voltage regulator.

[0006] According to an embodiment, a voltage regulator may comprise: an operational amplifier; a gm enhanced current buffer driver; an output power driver, wherein the current buffer driver may be coupled between the operational amplifier and the output power driver; a current feedback circuit coupled between the output power driver and the current buffer driver; and a feedback loop coupled between the output power driver and the operational amplifier.

[0007] According to a further embodiment, a gm-boost circuit may be coupled to the current buffer driver. According to a further embodiment, the gm-boost circuit increases the current buffer driver input impedance. According to a further embodiment, the gm-boost circuit enables the current buffer driver to have a large gm value. According to a further embodiment, a biasing circuit may be coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver. According to a further embodiment, an enable/disable function may be provided to enable/disable the biasing circuit for reducing standby current. According to a further embodiment, a compensation capacitor may be coupled between the output power driver and a cascode node of the operational amplifier. According to a further embodiment, the voltage regulator may be a low drop out (LDO) voltage regulator. According to a further embodiment, the operational amplifier may have a first input adapted for coupling to a voltage reference, and a second input coupled to the feedback loop. According to a further embodiment, the operational amplifier may be a low gain and high bandwidth amplifier. According to a further embodiment, the low gain and high bandwidth amplifier may be a folded-cascode amplifier. According to a further embodiment, the operational amplifier may comprise diode connected PMOS transistors for lowering an output impedance of the folded-cascode amplifier. According to a further embodiment, the current buffer driver may be an operational transconductance amplifier (OTA).

[0008] According to a further embodiment, the current feedback circuit may sense a current change at the output power driver. According to a further embodiment, the current feedback circuit may provide transient enhancement for improved load regulation. According to a

further embodiment, the current feedback circuit may provide a feedback voltage from an output voltage node. According to a further embodiment, the current buffer driver may have a low output impedance. According to a further embodiment, capacitors in the biasing circuit may be provided for improving noise immunity thereof. According to a further embodiment, the voltage regulator may be a USB voltage regulator. According to a further embodiment, the current buffer driver may have low input impedance and may provide a high frequency pole that may not substantially affect the voltage regulator dominant pole.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] A more complete understanding of the present disclosure may be acquired by referring to the following description taken in conjunction with the accompanying drawings wherein:

[0010] Figures 1 and 1A illustrate various frequency response graphs showing different ESR situations;

[0011] Figure 2 illustrates a schematic block diagram of a USB voltage regulator, according to a specific example embodiment of this disclosure;

[0012] Figures 3, 3A and 3B illustrate in combination a schematic diagram of a folded-cascode amplifier having bias, gm-boost, current driver and current feedback circuits, according to a specific embodiment of this disclosure; and

[0013] Figures 4 and 5 illustrate transient and regulation response curves, according to the teachings of this disclosure.

[0014] While the present disclosure is susceptible to various modifications and alternative forms, specific example embodiments thereof have been shown in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific example embodiments is not intended to limit the disclosure to the particular forms disclosed herein, but on the contrary, this disclosure is to cover all modifications and equivalents as defined by the appended claims.

DETAILED DESCRIPTION

[0015] In typical low-drop out regulator (LDO) designs, the output load is not always constant. As the load changes, the pole location at the output varies from relatively high frequency (full load, e.g., >30 mA) to very low frequency (no load or very low load, *e.g.*, < 100μA), resulting in difficulty in separating the output pole and the gate pole due to large power PMOS transistor size. A USB regulator has a very large power PMOS transistor as an output driver due to the large transition range in load currents, typically from very low, less than 250 μA to very large at about 60 mA. Due to this unique application, SoC (system on chip) design (capacitor-less architecture) is very hard to achieve. An external capacitor is needed for USB LDO voltage regulator applications. The external capacitor may have very different ESR (equivalent series resistance) values ranging from a few milliohms to tens of ohms causing the output pole-zero locations to shift drastically. Therefore a need exists to push the gate pole of the last stage PMOS power transistor to a higher frequency when using external capacitors in, for example but not limited to, a USB LDO voltage regulator.

[0016] According to various embodiments, a voltage regulator may comprise a large gm (transconductance) current driver (low impedance current buffer amplifier) added between a first stage operation amplifier (OpAmp) and a last stage power transistor, *e.g.*, p-channel metal oxide semiconductor (PMOS) transistor. This current buffer allows a significant reduction of the maximum internal compensation capacitance to about 3.7 picofarads, and the working range of the external load capacitance from about 0.4 microfarads to about 4.7 microfarads. In addition, the current buffer, according to the teachings of this disclosure, offers the circuit designer a wider range of external capacitor sizes to choose from. The current buffer compensation circuit described and claimed herein allows reduced external capacitor size that increases the overall circuit board layout efficiency and flexibility of capacitor choices. In addition, according to various embodiments, the voltage regulator, *e.g.*, USB voltage regulator, may consume less power by, for example but is not limited to, using low-drop out (LDO) voltage regulator circuit designs, according to the teachings of this disclosure.

[0017] According to various embodiments, various values of ESR may be handled by separating the poles inside of the voltage regulator circuit sufficiently to create an approximate one pole system. Referring to Figure 2, depicted is a schematic block diagram of a voltage regulator, according to a specific example embodiment of this disclosure. The regulator may

comprise a low-gain operational amplifier (OpAmp) 202, a low-impedance current buffer driver 204, and a power output driver 206, *e.g.,* PMOS. The key to being able to use smaller value internal and external capacitances is to have a large gm current driver buffer amplifier 204 between the first stage OpAmp 202 and the last stage power output driver 206. The voltage regulator of Figure 2 may further comprise biasing circuits 208, current feedback 210, a feedback loop 212, a compensation capacitor 214 and a gm-boost circuit 218. This voltage regulator may supply power (voltage and current) to an external load and capacitor 216 and may further be used as a USB voltage regulator.

[0018] The implementation of the OpAmp 202 as a folded-cascode configuration is due to its unique architecture which results in a single pole at the output that minimizes the complexity of its compensation. The current buffer driver 204 acts like a low impedance driver which connects between the OpAmp 202 and the output driver 206. Since the output driver 206 may provide very large amounts of switching current during power supply operation, the gate capacitance is significantly high due to the size of the driver, thereby resulting in the generation of a pole at relatively low frequency. Thus the current buffer driver 204 pushes this pole to a high frequency beyond unity-gain frequency due to its low-impedance characteristics in order to get the pole-splitting effect. To achieve this, it is necessary to provide a fairly large gm value of the current buffer driver 204. The gm-boost circuit 218 may provide a gm-boost technique that will increase the impedance value of the current buffer driver 204 with the help of the current feedback 210 which may sense the current change at the output of the output driver 206. The current feedback 210 also may behave like a transient enhancement circuit which will help with load regulation of the regulator during, for example but is not limited to, USB power supply operation.

[0019] The input stage OpAmp 202 may be a low-gain, high-bandwidth amplifier comprising diode connected PMOS transistors that lower the output impedance of the folded-cascode amplifier. Referring to Figures 3, 3A and 3B, depicted in combination is a schematic diagram of a folded-cascode amplifier having gm-boost, current driver and current feedback circuits, according to a specific embodiment of this disclosure. A folded-cascode amplifier design was selected for the input stage OpAmp 202 for the following reasons: (1) The architecture forms only one pole at the output of the folded stage which reduces the complexity of frequency compensation, (2) it provides a good driving capability for the source follower

stage of the current buffer 204 shown in Figure 3B placed thereafter due to its characteristics of being an OTA (Operational Transconductance Amplifier) that may be adapted to drive a capacitive load such as the gate of transistor 384, and (3) its uniqueness of the folded stage (transistors 360 and 366 shown in Figure 3A) may be used as an indirect compensation node E.

[0020] Shown in Figure 3 is the bias circuit 208 for the USB regulator. Transistors 320, 330, 334 and 336 may be shut off during disabling/power down operation to make sure this circuit will consume substantially no DC current. Capacitors 322 and 342 are coupling capacitors to improve the VDD noise cancelation making sure the gates of transistors 324, 326 and 328 are moving the same way as VDD (node A) to cancel the power noise resulting with Vsg_noise = 0. 342 acts similarly to help transistor 340 have better ground noise immunity resulting in Vgs_noise = 0. Node M is the enable signal coming to the regulator circuit so that the module can be turned off when disabled.

[0021] The output stage (transistors 350, 360 and 366) from the OpAmp 202 (Figure 3A, node C) then connects to the gate of the PMOS second stage transistor 384. The low impedance looking into the amplifier function of the current buffer 204 and source of transistor 384 creates a fairly high frequency pole that would be irrelevant to interact with the system dominant pole, which connects to the power PMOS transistor 380 in the power output driver 206, thereby having more efficient pole-splitting, and allowing easier frequency compensation. The current driver stage transistor 384 (in the current buffer 204) of the regulator circuit shown in Figure 3B creates a low impedance environment using the current buffer (transistors 384 and 394, and resistor 372) to separate the poles seen on the big power output driver 206 comprising transistor 380 and the internal stages of the regulator (OpAmp 202, Figure 3A, node C). By literally pushing the pole at the gate of transistor 380 to a high frequency domain, effectively leaves the only dominant pole at the output (node C) of the OpAmp 202 during full-load conditions. To achieve such operation, a gm-boost stage may be used.

[0022] The gm-boost stage 218 may comprise transistors 368, 370, 374, 376, 378, 382, 396, 394, 400, 402, 384 and resistor 372 shown in Figure 3B of the current buffer 204. The current driver may comprise transistors 370, 384 and 394, and resistor 372 shown in Figure 3B of the current buffer 204, and the current feedback circuits 210 may comprise transistors 374, 376, 378, 400, 402, and 394 shown in Figure 3B of the current buffer 204. The gm of the PMOS

current buffer driver 204 may comprise transistor 384 and may be coupled to two sources of currents, one from the bias network and the other as current feedback 210 comprising transistors 378, 400, 402 and 376 from the power output stage 206 that may comprise transistor 380. The bias network may be fixed by transistor 396. Then these currents are ratio'ed in transistors 368 and 370 to provide a sufficient amount of current for the driver transistor 384 but not enough to increase more current based upon a limited current mirror by transistor 396.

[0023] The feedback network 212 may comprise transistor 380, the resistors 388 and 390 may be coupled to the output transistor 380, and may actively provide current to the current driver transistor 384 when the regulation circuit experiences different output load conditions. This feedback network 212 provides feedback voltage to one differential input (transistor 356, Figure 3A, node D) of the OpAmp 202 to compare with a reference voltage (from a voltage reference not shown) connected to the other differential input (transistor 354, Figure 3A, node H). The only compensation capacitor required between the output stage of the OpAmp 202 node C in Figure 3A and the output stage of the regulator above resistor 388 coupled to output node N in Figure 3B need only be sized to make sure that the poles are even further well separated. This value is limited to a small number which helps in stabilizing the regulator system. With the simple current buffer 204 comprising transistors 368, 370, 374, 376, 378, 382, 396, 394, 400, 402, 384 and resistor 372, the voltage regulator acts like a pseudo "one-pole" system that is independent from the output pole changing so long as it falls within the bandwidth of the system. Thus, the range of ESR is extended along with the output capacitance. Therefore a wider range of external capacitors may be effectively used, according to the teachings of this disclosure.

[0024] Referring to Figures 4 and 5, depicted are transient and regulation response curves, according to the teachings of this disclosure. Shown are line transient response graphs reflecting the AC response of the system wherein the regulator output is stable with supply voltage change in transient. These graphs show the regulator system using a small compensation capacitor is stable.

[0025] While embodiments of this disclosure have been depicted, described, and are defined by reference to example embodiments of the disclosure, such references do not imply a limitation on the disclosure, and no such limitation is to be inferred. The subject matter

disclosed is capable of considerable modification, alteration, and equivalents in form and function, as will occur to those ordinarily skilled in the pertinent art and having the benefit of this disclosure. The depicted and described embodiments of this disclosure are examples only, and are not exhaustive of the scope of the disclosure.

Aptiv Services US, LLC Exhibit 1003 Page 203

CLAIMS

What is claimed is:

1. A voltage regulator, comprising:

an operational amplifier;

a gm enhanced current buffer driver;

an output power driver, wherein the current buffer driver is coupled between the operational amplifier and the output power driver;

a current feedback circuit coupled between the output power driver and the current buffer driver; and

a feedback loop coupled between the output power driver and the operational amplifier.

2. The voltage regulator according to claim 1, further comprising a gm-boost circuit coupled to the current buffer driver.

3. The voltage regulator according to claim 2, wherein the gm-boost circuit increases the current buffer driver input impedance.

4. The voltage regulator according to claim 2, wherein the gm-boost circuit enables the current buffer driver to have a large gm value.

5. The voltage regulator according to claim 1, further comprising a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver.

6. The voltage regulator according to claim 5, further comprising an enable/disable function to enable/disable the biasing circuit for reducing standby current.

7. The voltage regulator according to claim 1, further comprising a compensation capacitor coupled between the output power driver and a cascode node of the operational amplifier.

8. The voltage regulator according to claim 1, wherein the voltage regulator is a low drop out (LDO) voltage regulator.

9. The voltage regulator according to claim 1, wherein the operational amplifier has a first input adapted for coupling to a voltage reference, and a second input coupled to the feedback loop.

10. The voltage regulator according to claim 1, wherein the operational amplifier is a low gain and high bandwidth amplifier.

11. The voltage regulator according to claim 10, wherein the low gain and high bandwidth amplifier is a folded-cascode amplifier.

12. The voltage regulator according to claim 11, wherein the operational amplifier comprises diode connected PMOS transistors for lowering an output impedance of the folded-cascode amplifier.

13. The voltage regulator according to claim 1, wherein the current buffer driver is an operational transconductance amplifier (OTA).

14. The voltage regulator according to claim 1, wherein the current feedback circuit senses a current change at the output power driver.

15. The voltage regulator according to claim 1, wherein the current feedback circuit provides transient enhancement for improved load regulation.

16. The voltage regulator according to claim 1, wherein the current feedback circuit provides a feedback voltage from an output voltage node.

17. The voltage regulator according to claim 1, wherein the current buffer driver has a low output impedance.

18. The voltage regulator according to claim 5, further comprising capacitors in the biasing circuit for improving noise immunity thereof.

19. The voltage regulator according to claim 1, wherein the voltage regulator is a USB voltage regulator.

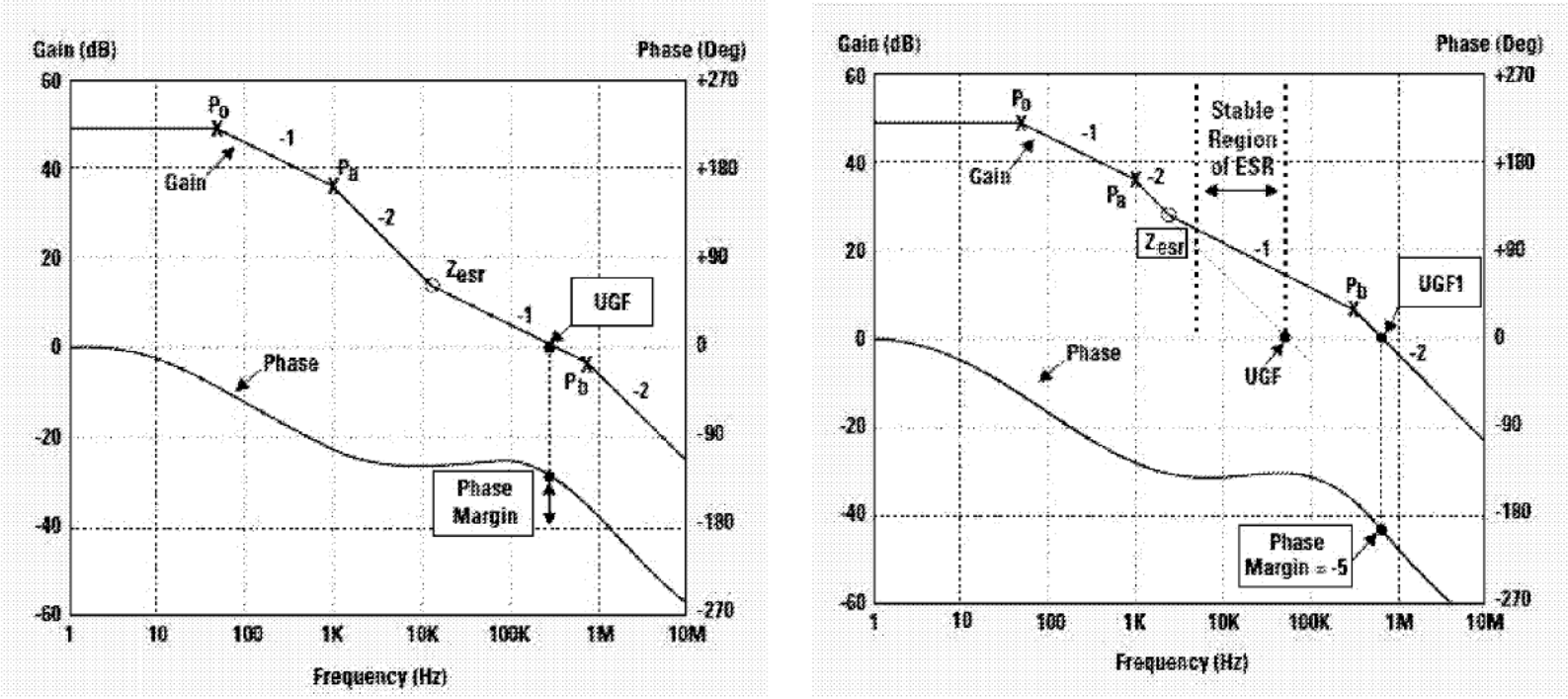
20. The voltage regulator according to claim 1, wherein the current buffer driver has low input impedance and provides a high frequency pole that does not substantially affect the voltage regulator dominant pole.

Aptiv Services US, LLC Exhibit 1003 Page 206

USB REGULATOR WITH CURRENT BUFFER TO REDUCE COMPENSATION CAPACITOR SIZE AND PROVIDE FOR WIDE RANGE OF ESR VALUES OF EXTERNAL CAPACITOR

ABSTRACT OF THE DISCLOSURE

A voltage regulator comprises a large gm current buffer driver added between a first stage of an operation amplifier and a last stage power transistor. This current buffer allows a significant reduction in the maximum internal and external compensation capacitances needed for regulator stability. The current buffer compensation circuit allows a wide range of external capacitor sizes that increases the flexibility in choosing the external capacitor types (with low to high ESR ratings).

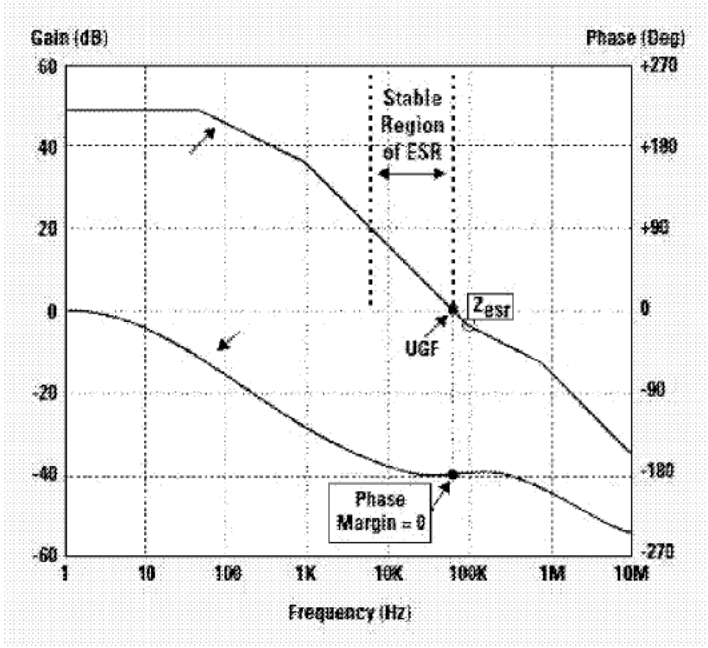


(a) Normal frequency response

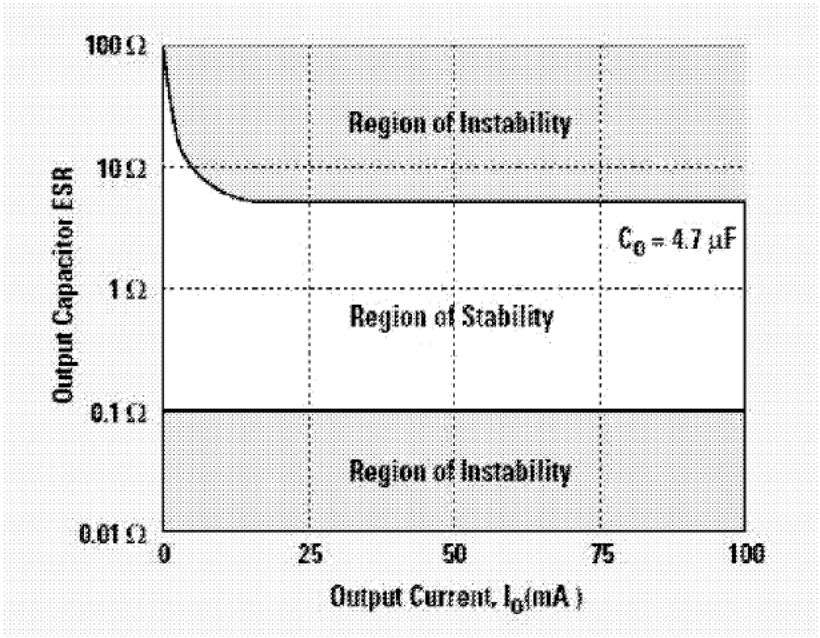
(b) ESR value too high

FIGURE 1

Aptiv Services US, LLC Exhibit 1003 Page 208



(c) ESR value too low



(d) "Tunnel of death"

FIGURE 1A

Aptiv Services US, LLC Exhibit 1003 Page 209

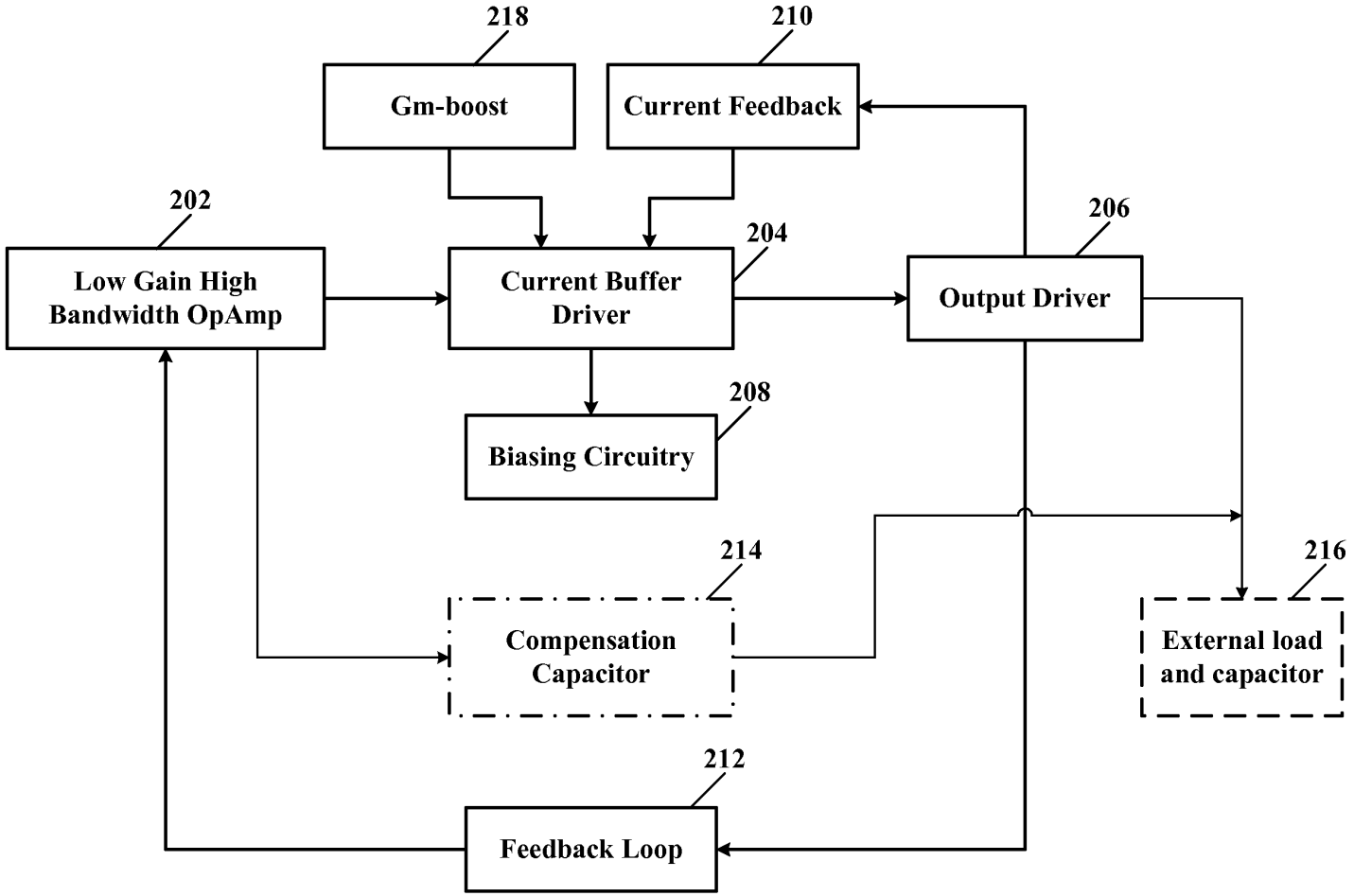

218
210
Gm-boost
Current Feedback
202
204
206
Low Gain High Bandwidth OpAmp
Current Buffer Driver
Output Driver
208
Biasing Circuitry
214
216
Compensation Capacitor
External load and capacitor
212
Feedback Loop

FIGURE 2

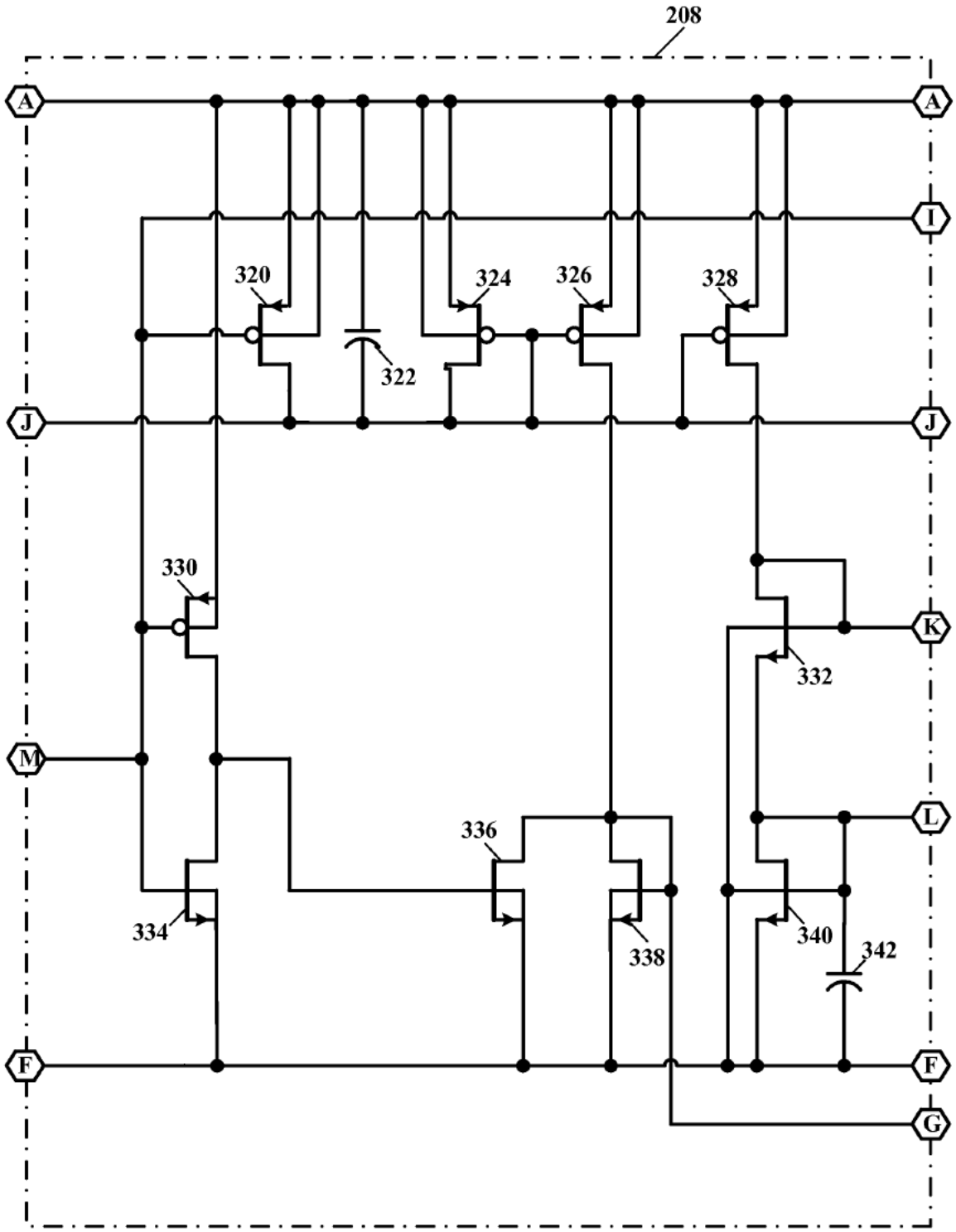

208
A
A
I
320
324
326
328
322
J
J
330
K
332
M
L
336
334
338
340
342
F
F
G

FIGURE 3

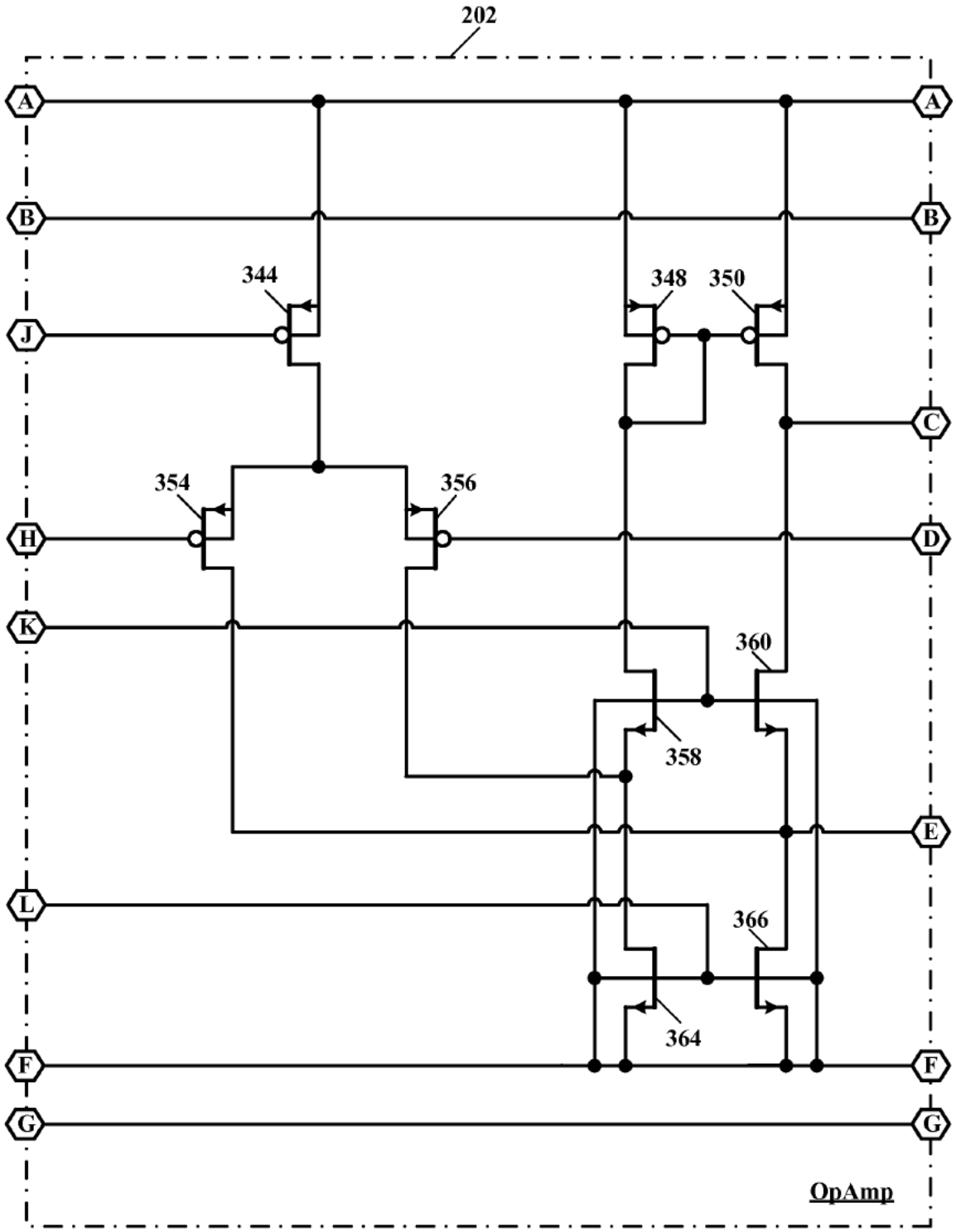


FIGURE 3A

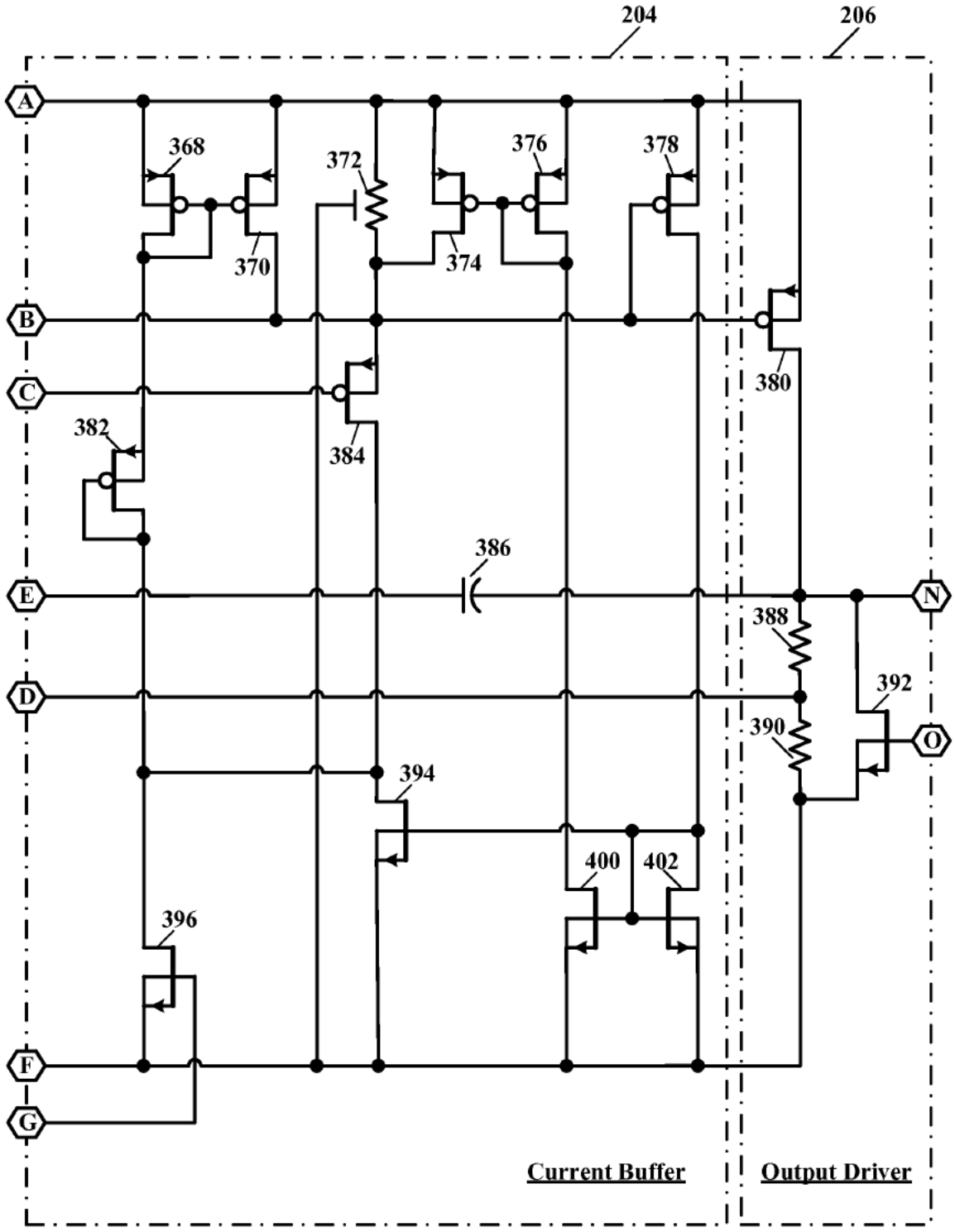

204
206
A
B
C
E
D
F
G
N
O
368
370
372
374
376
378
380
382
384
386
388
390
392
394
396
400
402
Current Buffer
Output Driver

FIGURE 3B

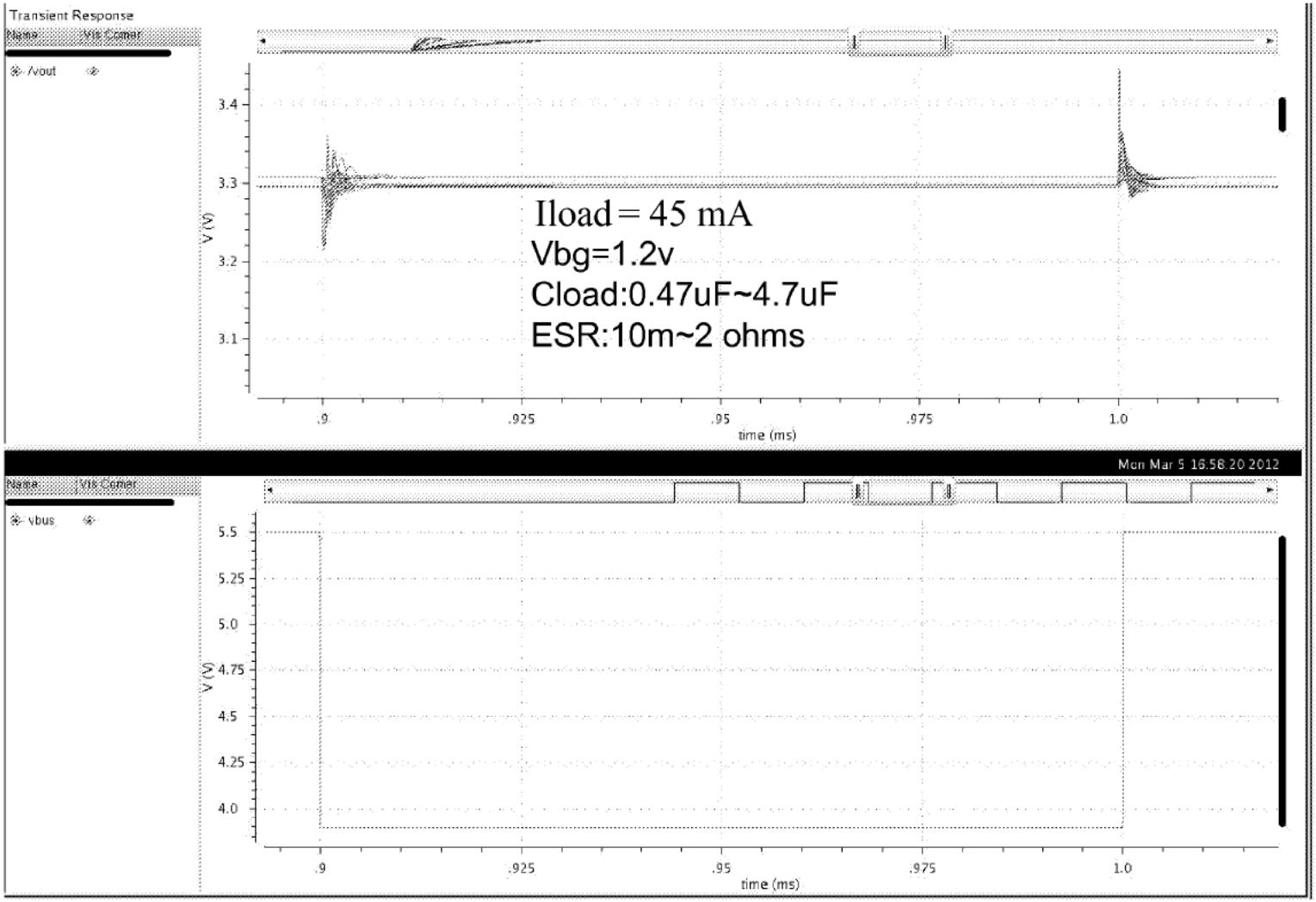

Transient Response
Name
Vtt Corner
/vout
3.4
3.3
3.2
3.1
V (V)
Iload = 45 mA
Vbg=1.2v
Cload:0.47uF~4.7uF
ESR:10m~2 ohms
.9
.925
.95
.975
1.0
time (ms)
Mon Mar 5 16:58:20 2012
Name
Vtt Corner
vbus
5.5
5.25
5.0
4.75
4.5
4.25
4.0
V (V)
.9
.925
.95
.975
1.0
time (ms)

FIGURE 4

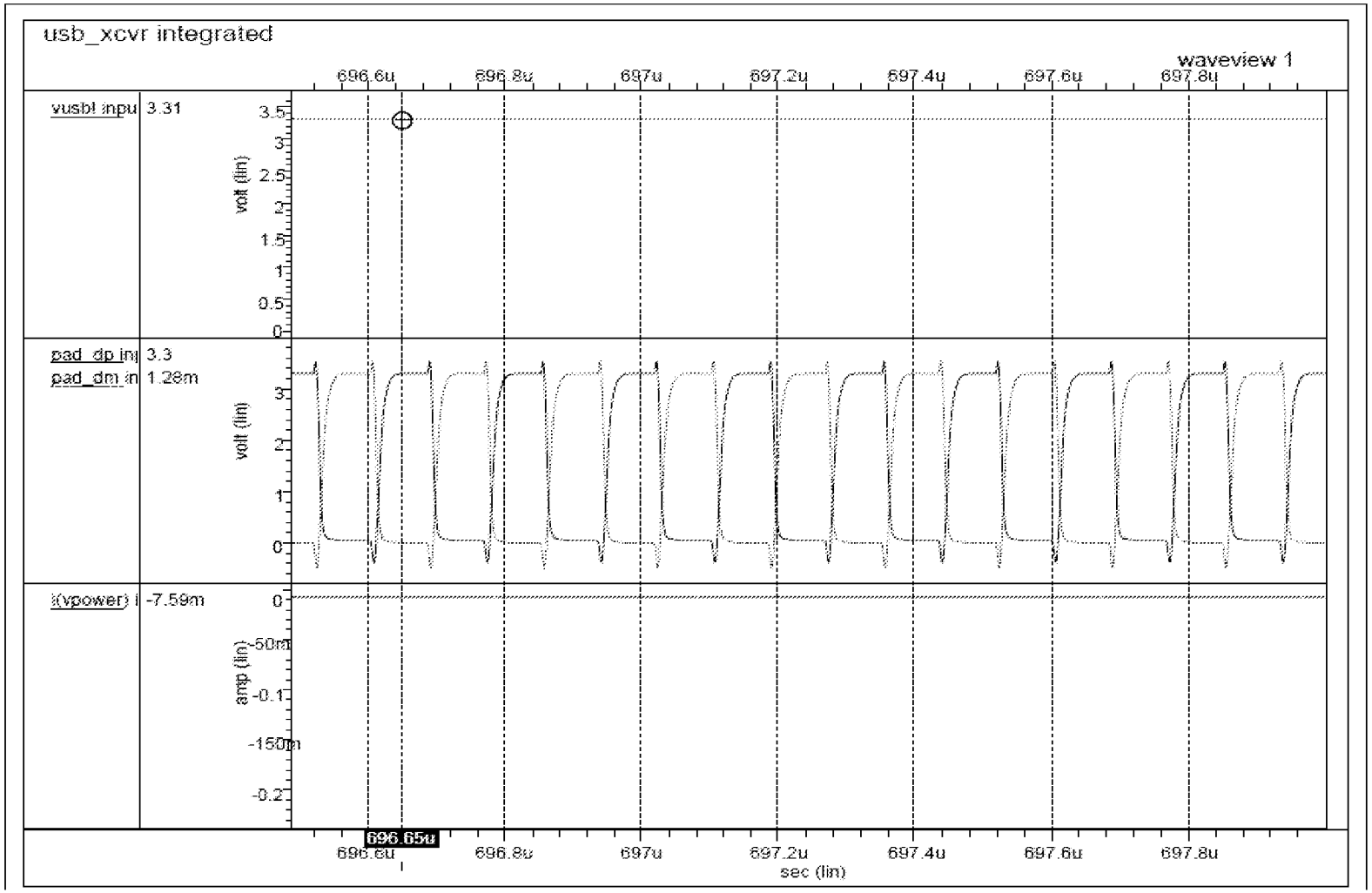

usb_xcvr integrated
waveview 1
696.6u
696.8u
697u
697.2u
697.4u
697.6u
697.8u
vusbl inpu 3.31
volt (lin)
pad_dp in
pad_dm in 1.28m
i(vpower) i -7.59m
amp (lin)
696.65u
sec (lin)

FIGURE 5

PTO/AIA/01 (06-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor

As the below named inventor, I hereby declare that:

This declaration is directed to:

- [x] The attached application, or
- [ ] United States application or PCT international application number _____

  filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Huamin Zhou Date (Optional) :_____

Signature: _____

Note: An application data sheet (PTO/AIA/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/SB/AIA01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/01 (06-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor

As the below named inventor, I hereby declare that:

This declaration is directed to:

- [x] The attached application, or
- [ ] United States application or PCT international application number _____

filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Woowai Martin Date (Optional) :_____

Signature: _____

Note: An application data sheet (PTO/AIA/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/SB/AIA01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/01 (06-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor

As the below named inventor, I hereby declare that:

This declaration is directed to:

- [x] The attached application, or
- [ ] United States application or PCT international application number _____ filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Cristian Albina Date (Optional) :_____

Signature: _____

Note: An application data sheet (PTO/AIA/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/SB/AIA01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/01 (06-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor

As the below named inventor, I hereby declare that:

This declaration is directed to:

- [x] The attached application, or
- [ ] United States application or PCT international application number _____

filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Fritz Schlunder Date (Optional) :_____

Signature: _____

Note: An application data sheet (PTO/AIA/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/SB/AIA01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/01 (06-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor

As the below named inventor, I hereby declare that:

This declaration is directed to:

- [x] The attached application, or
- [ ] United States application or PCT international application number _____

filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Minh Le Date (Optional) :_____

Signature: _____

Note: An application data sheet (PTO/AIA/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/SB/AIA01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Patent Application Fee Transmittal	
Application Number:	
Filing Date:	
Title of Invention:	USB REGULATOR WITH CURRENT BUFFER TO REDUCE COMPENSATION CAPACITOR SIZE AND PROVIDE FOR WIDE RANGE OF ESR VALUES OF EXTERNAL CAPACITOR
First Named Inventor/Applicant Name:	Huamin Zhou
Filer:	Eric M. Grabski/Todd Rosson
Attorney Docket Number:	68354.225441
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1600**

Electronic Acknowledgement Receipt	
EFS ID:	18431661
Application Number:	14204011
International Application Number:	
Confirmation Number:	9205
Title of Invention:	USB REGULATOR WITH CURRENT BUFFER TO REDUCE COMPENSATION CAPACITOR SIZE AND PROVIDE FOR WIDE RANGE OF ESR VALUES OF EXTERNAL CAPACITOR
First Named Inventor/Applicant Name:	Huamin Zhou
Customer Number:	86528
Filer:	Eric M. Grabski/Todd Rosson
Filer Authorized By:	Eric M. Grabski
Attorney Docket Number:	68354.225441
Receipt Date:	11-MAR-2014
Filing Date:	
Time Stamp:	13:48:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1600
RAM confirmation Number	12542
Deposit Account	504871
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees) Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees) Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	ADSA_225441.pdf	635780 2dd2d34135faf80b5a130769c2176d9a5d348141	no	7
Warnings:					
Information:					
2		Patent_Application_225441.pdf	165964 1892d6f8a69554023214 65c135516335212094f7	yes	13

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Specification	1	9
	Claims	10	12
	Abstract	13	13

Warnings:					
Information:					
3	Drawings-only black and white line drawings	Drawings_225441.pdf	618904 7d5f5d514f55d2d76908b5b540bc5229d407ccbb	no	8
Warnings:					
Information:					
4	Oath or Declaration filed	Declaration_225441.PDF	295133 2f362e68b94bf1b44120a772f5d4295ad7373f79	no	5
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	33525 b7864aee7ed8f160ba8b69bff999e817b20521d1	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1749306		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

SCORE Placeholder Sheet for IFW Content

Application Number: 14204011 Document Date: 03/11/2014

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

- Drawings – Other than Black and White Line Drawings

Since this was an electronic submission, there is no physical artifact folder, no artifact folder is recorded in PALM, and no paper documents or physical media exist. The TIFF images in the IFW record were created from the original documents that are stored in SCORE.

To access the documents in the SCORE database, refer to instructions below.

At the time of document entry (noted above):

- Examiners may access SCORE content via the eDAN interface.
- Other USPTO employees can bookmark the current SCORE URL (http://Score.uspto.gov/ScoreAccessWeb/).
- External customers may access SCORE content via the Public and Private PAIR interfaces.

Form Revision Date: September 30, 2013