

Highly Power-Efficient Active-RC Filters With Wide Bandwidth-Range Using Low-Gain Push-Pull Opamps

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Abstract—This paper presents a generic-purpose solution of highly power-efficient active-RC filters, which is suitable for analog baseband with wide bandwidth-range from several mega-Hz to hundreds of mega-Hz in wireless receivers. A 260 μA 7–20 MHz 6th-order active-RC low-bandwidth low-pass filter (LBW-LPF) and a 2.3 mA 240–500 MHz 6th-order active-RC high-bandwidth low-pass filter (HBW-LPF) are implemented in a standard 0.18 μm CMOS process to demonstrate this versatile solution. Highly power-efficient push-pull opamps with 30-to-35 dB gain are adopted for the filters, which allow us to focus on extending the bandwidth and reducing the power consumption. The push-pull opamp with adaptive-biased and pole-cancellation push-pull source follower (APP-SF) as the buffer stage is proposed to greatly reduce the power consumption and effectively extend the bandwidth. An adaptive bias mechanism is also proposed to tolerate the PVT variations for the opamps. In addition, the GBW compensation and the Q-degrading scheme are adopted to relax the opamp GBW requirement, further reducing the power dissipation. The LBW-LPF only consumes 260 μA current from 1.8 V supply, achieves 14.4 dBm in-band IIP3 and 66.2 nV/ $\sqrt{\text{Hz}}$ INR density, and occupies 0.21 mm² silicon area without pads. The HBW-LPF merely dissipates 2.3 mA current from 1.8 V supply, achieves 11.3 dBm in-band IIP3 and 13.1 nV/ $\sqrt{\text{Hz}}$ INR density, and occupies 0.23 mm² silicon area without pads.

Index Terms—Active-RC filter, adaptive bias, analog integrated circuits, buffer, continuous-time filter, high power-efficiency, operational amplifier, opamp, pole-cancellation, push-pull, source follower, ultra-low power, ultra-wideband.

I. INTRODUCTION

THE MODERN wireless communication systems, such as CDMA/LTE cellular, GNSS, WLAN/WPAN, UWB, and so on [1]–[4], are developing rapidly. To be embedded in the mobile phones, wireless terminals, and other portable equipments, the modern wireless receivers and transceivers greatly desire low power consumption, which is crucial for the longer battery life. The integrated analog baseband circuits, including

the continuous-time filters and programmable gain amplifiers (PGA), are the indispensable building blocks in wireless receivers or transceivers. The analog baseband filters typically consumes several mW to tens of mW, which cannot be negligible in the total power consumption of the whole receivers or transceivers.

Several topologies of integrated continuous-time filters have been developed, mainly including the Gm-C [5], active-RC [6], active-Gm-C [7], source-follower-based [8] architecture, and so on. Gm-C topology is traditionally regarded as a low-power solution, and has great potential of working at high frequency [9], [10], since the Gm-C integrator is based on the open-loop and the minimum gain-bandwidth-product (GBW) of the Gm cell is only required to be not less than the filter's cutoff frequency. However, the Gm-C filters suffer from poor linearity due to the open-loop nature. Linearity enhancement techniques [11], [12] can be applied, but higher excess noise would be produced, which implies additional power is necessary to sustain high dynamic range.

Another popular approach for continuous-time filters is active-RC topology. If an ideal opamp with sufficient gain and GBW was available, the opamp-based active-RC filter would perform excellent linearity due to the close-loop mechanism [13]. It also has low excess noise and large swing, resulting in large dynamic range [14] for given power consumption. Compared to the Gm-C topology, the nodes in active-RC filter are the opamp input nodes of virtual ground or opamp output nodes of low-impedance. Thus, the active-RC filters are insensitive to the parasitic capacitance, including the capacitance of opamp input/output nodes and interconnection.

However, active-RC filters' performance is deeply dependent on opamps' performance, mainly including the GBW, gain, and output impedance. The GBW should be at least eight times of $f_{\text{cutoff}} \cdot Q_{\text{filter}}$, where f_{cutoff} is the cutoff frequency of the filter and Q_{filter} is the maximum quality factor. For example, a 6th-order butterworth low-pass filter requires the maximum Q_{filter} of 1.932. If the active-RC topology is selected to implement a 500 MHz 6th-order butterworth low-pass filter, the opamp should have a large GBW of at least 7.7 GHz, which is very difficult to design and desires large power consumption. In addition, the high-gain opamp always needs complicated multi-stage topology, such as the miller-compensation two-stage architecture, nested-compensation three-stage architecture, and so on. They will consume large power consumption especially for the high GBW. The

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low-output-impedance and large-swing requirements at high frequency also demand large power dissipation. Due to such limitations, the opamp-based active-RC topology is generally regarded as a high-power solution compared with the Gm-C topology. To a large extent, it is always recommended to be applied in low or moderate frequency.

Recently, several works have been published to improve the power efficiency of the active-RC filters. A Q-tuning technique in a 19.7 MHz fifth-order active-RC chebyshev low-pass filter with 11.25 mW power consumption was reported in [15]. It was able to relax the Q requirement of the opamp, thereby reducing the power consumption. A 20 MHz fifth-order chebyshev active-RC filter using the Gm-assisted-OTA-RC technique with 4.5 mW power consumption is proposed in [16]. It combined Gm-C and active-RC integrators to enhance the linearity and speed, while adding little excess noise and power dissipation. Reference [17] prompted the active-RC filter to high frequency of 500 MHz with 90 mW power by using the three-stage feedforward-compensated opamp. Reference [18] achieved a wide bandwidth tuning range from 44 MHz to 300 MHz with 54 mW power through the “constant-capacitance scaling” principle for the feedforward-compensated opamp. Reference [19] proposed an inherently linear current division network (CDN) to achieve a good linearity with 71 dB SFDR, which only consumes 2.7 mW for 5.5 MHz bandwidth. Reference [20] presented a active-RC filter with a new method for noise reduction to realize a low noise of $9.5 \text{ nV}/\sqrt{\text{Hz}}$ input-referred noise density, which consumes 5 mW for 2.5 MHz center frequency. Among the recently published active-RC filters, the multi-stage amplification architecture with frequency compensation or cascode topology is chosen to implement the high-gain opamps of over 50 dB gain, which guarantees the good in-band linearity and little gain variation due to PVT (process, voltage, and temperature) variations. But how to extend the bandwidth with high power-efficiency is difficult for the high-gain opamp based active-RC filters. The power efficiency of these works still seems to be non-advantageous, compared to Gm-C, or source-follower-based, and is not able to cover a wide bandwidth-range with high power-efficiency, especially for the high bandwidth of hundreds of mega-Hz.

In this paper, a generic-purpose solution of highly power-efficient active-RC filters for a wide bandwidth-range is demonstrated. The low-gain opamps with 30-to-35 dB gain are used to implement the proposed active-RC filters. It will degrade the feedback depth, resulting in a little gain fluctuation due to the PVT variations and deterioration of in-band linearity in the close loop. But they are acceptable by modern wireless receivers. Consequently, based on the low-gain opamps, the filter can focus on extending the bandwidth and reducing the power consumption. Additionally, we propose highly power-efficient opamps using the adaptive-biased and pole-cancellation push-pull source follower (APP-SF) as the buffer stage, which drastically extend the bandwidth with high power-efficiency. On the basis of the APP-SF, two relative low-bandwidth opamps (LBW-Opamp) and a high-bandwidth opamp (HBW-Opamp) are implemented for the proposed LBW-LPF and HBW-LPF. An adaptive bias circuit is also proposed for the opamps, which successfully help the filters to tolerate the PVT variations.

What's more, three techniques in filter architecture were presented to further reduce the power consumption. Based on the GBW compensation mechanism in the biquad, the relative low-GBW opamp with less power consumption are able to construct the high-bandwidth filter. Q-degrading resistors, which are similar to [15], are adopted to relax the Q requirement of biquad, which is valuable for power reduction. Because of the different Q requirements in each biquad, various opamps with scaling GBW and power are customized for each biquad to further reduce the power consumption.

For demonstrating the generic-purpose solution of highly power-efficient active-RC filters, a $260 \mu\text{A}$ 7–20 MHz 6th-order active-RC low-pass filter [21] and a 2.3 mA 240–500 MHz 6th-order active-RC low-pass filter [22] are implemented, which verified the proposed solution is not only suitable for the low frequency, but also for the high-frequency up to 500 MHz. The LBW-LPF achieves a linearity of 14.4 dBm IIP3, and the HBW-LPF achieves a linearity of 11.3 dBm IIP3, which are acceptable by modern wireless receivers. The figure-of-merit (FOM) of the filters is 4.1 aJ and 1.66 aJ, respectively. They are not only much more power-efficient than the traditional active-RC filters, but also than the Gm-C topology which was always regarded as the low power option. This work indicates that the proposed solution can be widely applicable for a wide bandwidth-range. By using the techniques of positive substrate bias or enhancing the power supply voltage, the proposed opamp is also suitable for the advanced CMOS technique such as 65 nm CMOS. It can be further evolved into the more advanced CMOS technique.

This paper is organized as follows. Section II discusses the consideration for high power-efficiency in the filter architecture; Section III describes the proposed highly power-efficient opamps, and makes detailed analysis of the opamps; Section IV presents the proposed filters implementation, together with the architecture techniques for reducing the power consumption; Section V shows the measurement results and a conclusion is drawn in Section VI.

II. CONSIDERATION IN FILTER ARCHITECTURE

As for the opamp-based close-loop applications, the gain and GBW of opamp are the two of the most important specifications. Conventionally, the gain of the opamp should be large enough to sustain sufficient gain accuracy in the close loop. But it poses a big challenge for high bandwidth and low power. More complicated opamp topology should be chosen to obtain high gain, resulting in more internal nodes and more parasitic capacitance, which implies that the GBW is difficult to extend with high power-efficiency. As a result, the relative low GBW will limit the close-loop bandwidth as shown in Fig. 1(a). Consequently, more power would be consumed to extend the GBW for the targeted close-loop bandwidth.

However, we noticed that the relative low-gain opamp with high GBW is much more suitable for the close-loop applications in modern wireless transceivers, as shown in Fig. 1(b). Simpler topology of opamp can be chosen for the low-gain opamp, which indicates fewer internal nodes, fewer poles, and less parasitic capacitance. Thus, the opamp is easier to extend the GBW

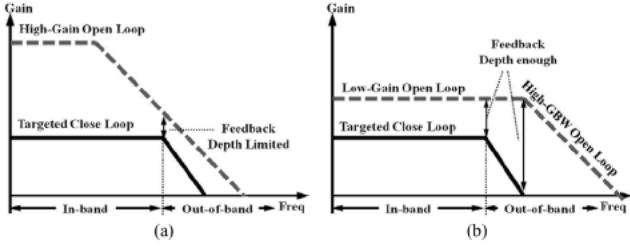


Fig. 1. The relationship between open-loop and the close-loop transfer function: (a) using high-gain open loop; (b) using high-GBW and low-gain open loop.

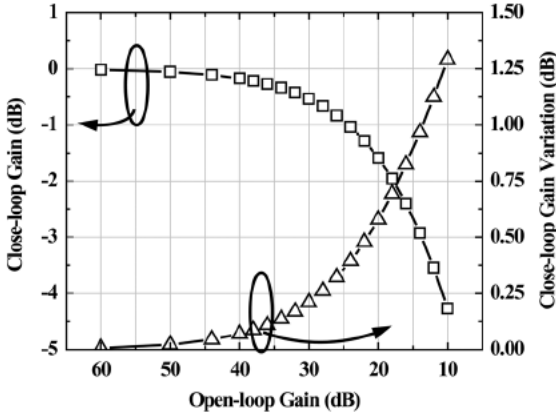


Fig. 2. The simulated gain and gain variation of the opamp-based unit-gain close-loop versus the open-loop gain of the opamp.

and save the power consumption, and can construct the high bandwidth close-loop circuits with higher power-efficiency.

But the low-gain opamp might point two potential problems. First, the relative low feedback depth at low frequency would introduce the dc gain error in the close loop. We used an opamp-based resistive negative-feedback close-loop to construct the unit-gain amplifier. As illustrated in Fig. 2, in pace with the opamp gain becomes smaller; the close-loop gain error gradually increases. A 60 dB-gain opamp introduces nearly no close-loop gain error, while a 30 dB-gain opamp introduces -0.53 dB close-loop gain error. Fortunately, such gain error can be easily overcome by adjusting the ratio of the feedback resistors in the close loop. Secondly, the relative low gain of opamp would result in the close-loop gain fluctuation due to PVT variations. We assume the opamp would have ± 3 dB gain variance due to PVT variations. With the opamp gain becomes smaller, the close-loop gain fluctuation progressively enhances, as illustrated in Fig. 2. For instance, a 60 dB-gain opamp only introduces $+0.005/-0.008$ dB gain variation in close loop, while a 30 dB-gain opamp leads $+0.15/-0.21$ dB close-loop gain variation. As for the analog baseband chain in wireless receivers, such small gain fluctuation can be acceptable and it can be easily resolved by the AGC (auto gain control) loop in the analog baseband chain.

Furthermore, the gain of open loop might affect the in-band linearity in the close loop. The negative-feedback can effectively improve the close-loop linearity. It is the main reason why the active-RC filter has a better linearity than the other open-loop topologies. In the traditional active-RC filter, the high-gain

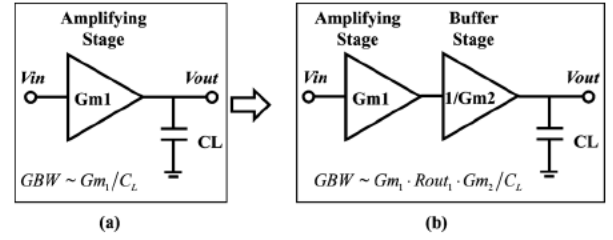


Fig. 3. The simplified diagram of amplification: (a) without buffer stage; (b) with buffer stage.

opamp can achieve good in-band linearity in close loop. While in the proposed active-RC filter based on the low-gain opamp, it will have worse in-band linearity in close loop, but have better out-of-band linearity due to the larger GBW. But it is enough to be acceptable by modern wireless receivers.

In this paper, we construct the active-RC low-pass filters by the low-gain opamp. Thus, we can focus on enhancing the power efficiency and extending the bandwidth.

III. PROPOSED HIGHLY POWER-EFFICIENT OPAMPS

The opamps consist of the buffer stage, amplifying stage, as well as the CMFB circuit. The proposed adaptive-biased pole-cancellation push-pull source-follower (APP-SF) buffer stage effectively expands the bandwidth and drastically cut down the power consumption. The one-stage amplifying stage with simple topology can create enough gain of over 30 dB. An adaptive bias circuit is proposed to generate the adaptive bias voltages to tolerate PVT variations.

A. Adaptive-Biased Pole-Cancellation Push-Pull Source Follower (APP-SF) Buffer Stage

As demonstrated in Fig. 3, if the amplifying stage directly sees the load capacitor, the bandwidth would be limited by the large output resistance of the amplifying stage. If a buffer stage, such as the source follower, is added between the amplifying stage and the load capacitor, the buffer stage can effectively isolate the high-impedance output node of the amplifying stage and the load capacitor, which is beneficial for wide bandwidth and low-power consumption. How to realize a highly power-efficient buffer stage is crucial for the low-power opamp.

As shown in Fig. 4(a), the simple source follower is widely used for the buffer stage, but it suffers from low power-efficiency. Instead, the principle of the push-pull source follower was developed, as depicted in Fig. 4(b). The power dissipation is reduced thanks to the current reuse mechanism. But how to drive the push-pull source follower in linear mode is another critical problem. One conventional method has been developed as shown in Fig. 4(c). However, this topology has two high-impedance nodes "A" and "B," which seriously deteriorate the bandwidth. In this paper, an adaptive-biased pole-cancellation source follower (APP-SF) is proposed to, which is more power-efficient than the traditional buffer stage.

As described in Fig. 5(b), the push-pull source follower constructed by the complementary devices of Mn6/Mp6 is able to achieve about twice bandwidth as the simple source follower at cost of the same current, mainly owing to the current reuse in the

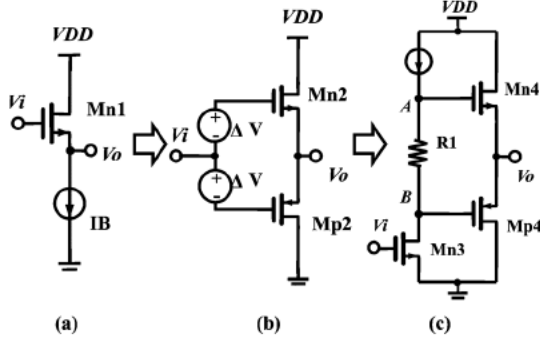


Fig. 4. The conventional topology of: (a) the simply source follower; (b) the principle of the push-pull source follower; (c) the push-pull buffer stage.

push-pull principle. It is a critical issue to drive the push-pull device Mn6/Mp6 simultaneously without dead zone. We utilized an adaptive-biased branch to drive the Mn6/Mp6 in class-A mode for high linearity. The current sources Mn5/Mp5 controlled by adaptive bias voltages “VBN/VBP” provide a small current, which should be as small as possible to reduce the power and parasitic capacitance. When this small current flows through the resistors R1/R2, dc level-shifting voltage is generated to drive the complementary Mn6/Mp6 in class-A mode. The dc level-shifting voltage can be optimized by changing the resistors R1/R2 to adjust the gate-source voltage Vgs of Mn6/Mp6. The current sources Mn5/Mp5 can provide sufficient high resistance which is much larger than the resistors R1/R2, so that there is no loss when signals transfer from input node to nodes “A” and “B.” The resistance of Mn5/Mp5 should also be larger than the output resistance of the forward amplifying stage to avoid the loss. This is another reason to reduce the device size of Mn5/Mp5 to enhance the resistance of Mn5/Mp5. The output swing is mainly restricted by the adaptive bias branch, but the adaptive bias branch has four stack devices. In order to elevate the voltage swing, the Vgs of Mn5/Mp6 and Mn6/Mp6 should be relative small, and the dc level at the input node of the buffer stage should be set at the middle of the allowable voltage swing range.

However, in Fig. 5(b), an additional pole is appealed at node “A/B,” which significantly deteriorates the bandwidth. Fortunately, as shown in Fig. 5(c), we adopted small capacitors C1/C2 in parallel with R1/R2 to introduce an additional zero, which is able to cancel the pole to maintain the wide bandwidth. Fig. 6 illustrates the simplified small-signal equivalent circuit of the proposed APP-SF as shown in Fig. 5(c). As depicted in Fig. 6, if the capacitor C1/C2 is not adopted, the transfer function from “Vin” to “VA” is expressed as

$$\frac{V_A}{V_{in}} = \frac{r_{ds_{Mn5}}}{r_{ds_{Mn5}} + R_1} \cdot \frac{1}{1 - j\omega/p_{add}} \quad (1)$$

$$p_{add} = -C_A/(R_1 \parallel r_{ds_{Mn5}}) \approx -C_A/R_1$$

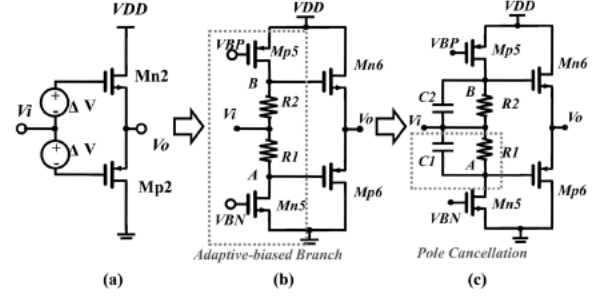


Fig. 5. The evolution of the proposed push-pull buffer: (a) the principle of the push-pull source follower; (b) the proposed push-pull source-follower without pole-cancellation technique; (c) the proposed pole-cancellation push-pull source follower.

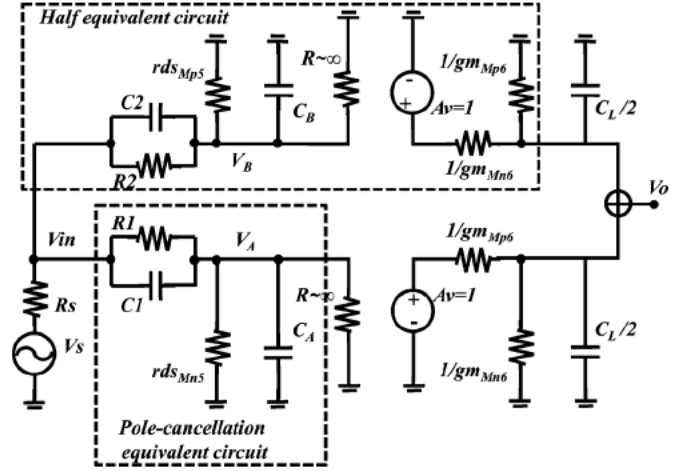


Fig. 6. The small-signal equivalent circuit of the proposed pole-cancellation push-pull source follower.

where $r_{ds_{Mn5}}$ is the resistance of current source Mn5, and C_A is the total capacitance to ground at node “A.” From (1), we find that there exists an additional pole p_{add} , which will significantly limit the bandwidth of the buffer.

But if the pole-cancellation technique of capacitors C1/C2 is adopted, we can get the transfer function from “Vin” to “VA” as shown in (2) at the bottom of the page. If the capacitor C1 satisfies the relationship as

$$R_1 \cdot C_1 = r_{ds_{Mn5}} \cdot C_A \quad (3)$$

The transfer function (3) can be modified as

$$\frac{V_A}{V_{in}} = \frac{r_{ds_{Mn5}}}{r_{ds_{Mn5}} + R_1} \quad (4)$$

Compared with (1), we find that the additional pole is cancelled out by the additional zero generated by the capacitor C1/C2. Consequently, the adaptive bias branch will not affect

$$\frac{V_A}{V_{in}} = \frac{r_{ds_{Mn5}}/(1 + j\omega \cdot r_{ds_{Mn5}} \cdot C_A)}{r_{ds_{Mn5}}/(1 + j\omega \cdot r_{ds_{Mn5}} \cdot C_A) + R_1/(1 + j\omega \cdot R_1 \cdot C_1)} \quad (2)$$

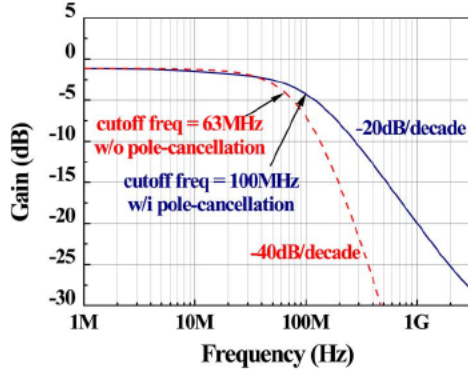


Fig. 7. The comparison of simulated magnitude response between the proposed APP-SF with and without pole-cancellation technique.

the bandwidth of the APP-SF buffer. If we assume the half equivalent circuit has nearly the same transfer function, transfer function of the APP-SF buffer can be expressed as follows:

$$H(s) = \frac{V_O}{V_S} = \frac{A_V}{(1 - j\omega/p_1)(1 - j\omega/p_2)}, \quad A_V \approx 1, \\ p_1 = -C_A / \frac{2R_S \cdot r_{ds_{Mn5}}}{2R_S + r_{ds_{Mn5}} + R_1} \approx -C_A / 2R_S, \\ p_2 = -C_L / 2 \cdot (gm_{Mp6} + gm_{Mn6}) \quad (5)$$

where R_S is the source resistance which is the output resistance of the forward amplifying stage, p_1 is the main pole, which dominates the APP-SF bandwidth, and p_2 is the second pole. Just because the APP-SF can effectively isolate the large load capacitor and the high impedance node at the output of the amplifying stage with highly power-efficiency, the opamp with such APP-SF can achieve low power and wide bandwidth.

Fig. 7 shows the comparison of the simulated magnitude response between the APP-SF with and without pole-cancellation technique. Both of them consume the same current of 11 μ A with same load capacitance of 300 fF. The APP-SF with the pole-cancellation technique achieves around 100 MHz cutoff frequency, which is improved 59% compared to the APP-SF without the pole-cancellation techniques.

According to the basic principle of the proposed APP-SF, we construct three different types of the APP-SF, as described in Fig. 8. Fig. 8(a) is the type-A APP-SF, which has been discussed above. As shown in Fig. 8(b), by replacing the resistors R_1/R_2 as the MOSFET-based diodes $Mn3/Mp3$, we construct type-B APP-SF, where the MOSFET-based diode behaves a small resistance. Based on the type-B APP-SF, through substituting the resistors R_3/R_4 for the current sources $Mp1/Mn1$, type-C APP-SF is developed, where the R_3/R_4 are still much larger than the MOSFET-based diodes $Mn3/Mp3$. Type-A and type-B can be controlled by the adaptive bias voltages “VBP/VBN,” while type-C is self-biased. Thus, type-A and type-B have the possibility to be immune to PVT variations by adaptively controlling the bias voltages. This is the main reason we choose type-A and type-B APP-SF to implement the proposed opamps for the low-pass filters.

In order to promote the APP-SF suitable for the advanced CMOS process such as 65 nm CMOS, the techniques of posi-

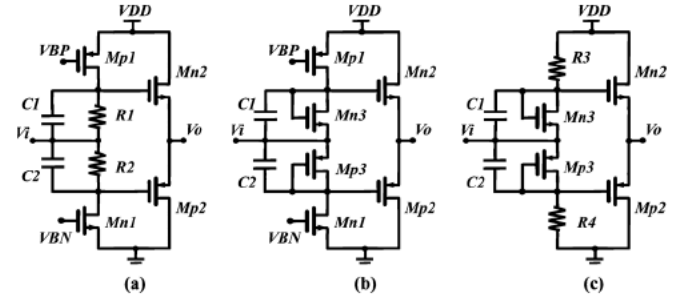


Fig. 8. The schematic of three types of the proposed pole-cancellation push-pull source-followers: (a) Type-A; (b) Type-B; (c) Type-C.

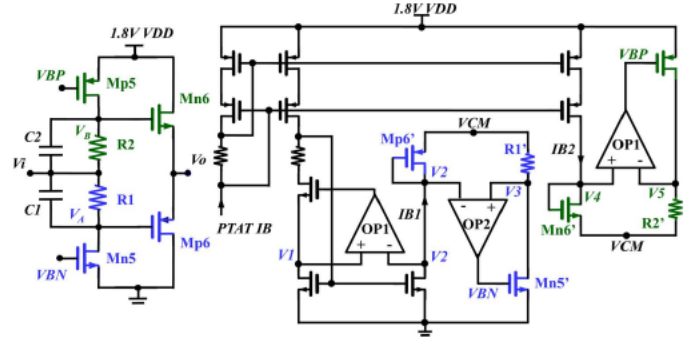


Fig. 9. The schematic of the adaptive bias circuit for the proposed adaptive-biased pole-cancellation push-pull source follower.

tive substrate-bias or enhancing the power supply voltage can be adopted to maintain the output swing. As shown in Fig. 8(a), the positive substrate-bias can be utilized to decrease the threshold voltage of the devices, so that the four-device stacked branch can still achieve a considerable swing under the low supply voltage of 1.2 V in advanced CMOS process, such as 65 nm CMOS. A little enhancement of the supply voltage can further increase the output swing. Based on these modifications of the APP-SF, the proposed generic-purpose solution of active-RC filters can be further evolved into more advanced CMOS techniques.

B. Adaptive Bias Circuit

An adaptive bias mechanism for the APP-SF was proposed to tolerate the PVT variations. If the APP-SF is controlled by fixed bias voltages, it would be very sensitive to the bias condition. As shown in Fig. 9, a tiny current mismatch in current source $Mp5/Mn5$ would lead to a large dc level shifting at the output node. PVT variations would also severely change the current in the push-pull source follower, which greatly impacts the bandwidth. For instance, at SF (NMOS slow and PMOS fast) or FS process corner, the output dc voltage will be shifted. At SS process corner, the APP-SF might be closed up, so that drastically degrade the bandwidth. At FF process corner, the power consumption will greatly increase. Besides, the supply voltage and temperature variations will also significantly affect the performance of the APP-SF.

To overcome this problem, as shown in Fig. 9, an adaptive bias mechanism through negative feedbacks and replicas from the APP-SF is proposed to keep the current consistent with the PTAT current source I_B , which can effectively sustain the stable

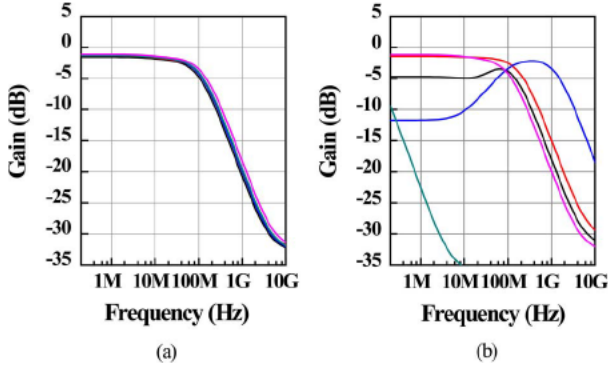


Fig. 10. The simulated magnitude response of the APP-SF: (a) with adaptive bias circuit in different process corner and (b) without adaptive bias circuit in different process corner.

bandwidth and current consumption. This approach is to generate adaptive bias voltages “VBP/VBN” to control the current source Mp5/Mn5, which provides adaptive voltages at node “A/B” and consequently forces the current in Mp6/Mn6 proportional to the PTAT IB. The dc level at input and output node of APP-SF is set as “VCM.” As demonstrated in Fig. 9, a negative feedback loop based on an operational amplifier OP1 is used to force the voltage “V2” the same as “V1,” which accordingly produces current IB1 proportional with PTAT IB. Another negative feedback through OP2 is utilized to force the voltage “V3” equal to “V2,” and generated the adaptive bias voltage “VBN.” Mn5, Mp6, and R1’ are proportionally duplicated from Mn5, Mp6, and R1, respectively. Because of the proportionally replicas, the voltage “V_A” is forced to be equal to “V3” as well as “V2.” Hence, the current in Mp6 is successfully kept consistent with the PTAT IB. The adaptive bias voltage “VBP” is generated by the same mechanism to hold the current in Mn6 proportional with the PTAT IB. From Fig. 10, we find the bandwidth of APP-SF with adaptive bias circuit only has negligible variance in different process corner (TT/SS/FF/SF/FS), but the magnitude response of APP-SF without adaptive bias circuit failed to be stable in different process corner.

C. Proposed Opamps

Based on the proposed APP-SF, we developed two opamps for the proposed low-bandwidth low-pass filters (LBW-LPF) and high-bandwidth low-pass filter (HBW-LPF).

1) *Opamps for the LBW-LPF*: As illustrated in Fig. 11, we constructed a highly power-efficient low-bandwidth opamp (LBW-Opamp-A), consisting of the amplifying stage, type-A APP-SF buffer stage, and CMFB. A complementary common-source amplifying stage is enough to provide over 30 dB gain, allowing us to choose small gate length to minimize parasitic capacitance. It only consumes 10 μ A current from 1.8 V supply voltage. It still has potential to further cut down the current consumption. But considering the matching among the main circuit, CMFB, and adaptive bias circuit, we did not further reduce the device size. Thanks to the effective isolation of the APP-SF buffer stage, the main pole of the opamp is determined by the capacitance at the output node of the amplifying stage. It is greatly smaller than the load capacitor, which is useful for the wide bandwidth. The secondary pole of the

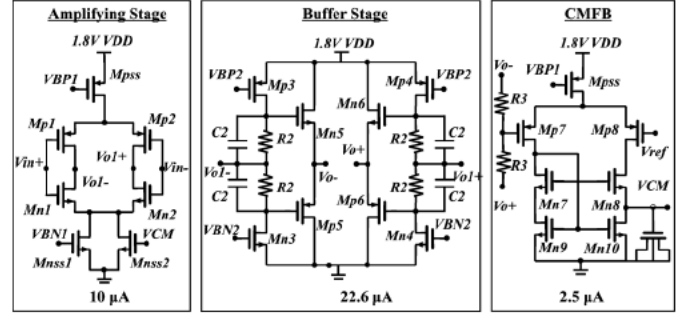


Fig. 11. The schematic of the proposed LBW-opamp-A with type-A APP-SF.

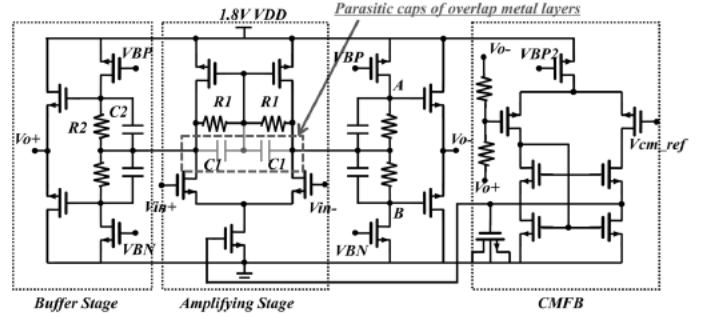


Fig. 12. The schematic of the proposed HBW-opamp.

opamp is at the output node of the APP-SF buffer stage. It is designed over twice than the main pole to achieve over 40° phase margin, which is larger than the minimum acceptable phase margin for the filter according to the analysis in [23]. The differential APP-SF buffer merely consumes 22.6 μ A current. The proposed LBW-Opamp-A consumes 35 μ A current totally, achieve 35 dB gain and 212 MHz GBW with 0.4 pF load capacitor.

By substituting the type-A APP-SF for the type-B APP-SF, another highly power-efficient low-bandwidth opamp (LBW-Opamp-B) was constructed. Since the parasitic capacitance to ground of MOSFET-based diodes Mn3/Mp3 in Fig. 8(b) is smaller than the resistors R1/R2 in Fig. 8(a), the current in the adaptive-bias branch can be further decreased. The LBW-Opamp-B only consumes 28.5 μ A current totally, while achieves 35 dB gain and 196 MHz GBW with 0.4 pF load capacitor. We also utilized this LBW-Opamp-B to implement an ultra-low power low-bandwidth active-RC low-pass filter for the demonstration, which will be discussed below.

2) *Opamp for the HBW-LPF*: As shown in Fig. 12, we constructed the high-bandwidth opamp (HBW-Opamp), which consists of the amplifying stage, type-A APP-SF buffer stage, and CMFB. The common-source configuration with self-biased load is able to provide around 30 dB gain. The self-biased current source load plays a role as a local common-mode feedback cooperating with the CMFB.

Generally, the differential topology with tail current source can realize the deep-negative common-mode rejection, which is indispensable for the common-mode stability. However, owing to the parasitic capacitance of the tail current source, the common-mode rejection degrades at high frequency, even changes to positive, which puts a big risk on the circuit stability.

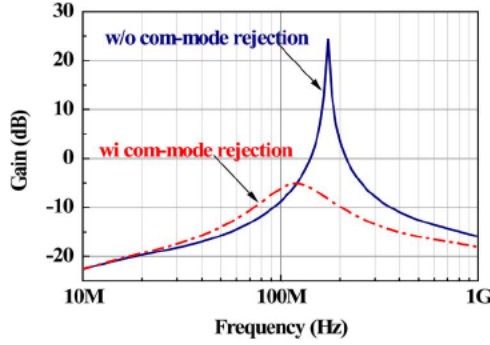


Fig. 13. The simulated common-mode magnitude response of: (a) without high-frequency common-mode rejection technique; (b) with high-frequency common-mode rejection technique.

Fortunately, as described in Fig. 12, it is well resolved by adding a small capacitor C_1 in parallel with R_1 to lead into a zero to suppress the common-mode gain at high frequency. As shown in Fig. 13, without the high-frequency common-mode rejection technique, the common-mode magnitude response has a large positive peak at around 170 MHz. While, if the small capacitor C_1 is added, the positive peak is suppressed by over 30 dB, and the common-mode magnitude response is all negative at all frequency, which removes the risk of the common-mode oscillation. The small capacitor C_1 is only about 10 fF, which has negligible influence on opamp bandwidth. But it is too small to realize by the MIM capacitor in standard CMOS process. Instead, we realized it by the parasitic capacitor through a small piece of two overlap metal layers.

The proposed HBW-Opamp achieves 1.8 GHz equivalent GBW at 0.3 pF load, but only consumes 450 μ A current. This HBW-Opamp is utilized to implement a low power high-bandwidth active-RC low-pass filter (HBW-LPF), which will be discussed below.

IV. FILTERS IMPLEMENTATION

Based on the proposed highly power-efficient opamps, an ultra-low power 6th-order 7 MHz-to-20 MHz tunable active-RC low-pass filter (LBW-LPF-A) using LBW-Opamp-A, an ultra-low power 6th-order 10 MHz active-RC low-pass filter (LBW-LPF-B) with LBW-Opamp-B, and an low-power 6th-order 240 MHz-to-500 MHz active-RC low-pass filter (HBW-LPF) with HBW-Opamp were implemented for the conceptual demonstration of the proposed generic-purpose solution of active-RC filters for wide bandwidth-range.

A. LBW-LPF-A and LBW-LPF-B

Fig. 14 gives the architecture diagram of the proposed active-RC filters. It consists of three cascaded biquad cells, and each biquad cell includes two opamps. The tunable frequency bands are realized by switching the capacitor bank. The low-gain of opamp will lead to loss in the filter, but it can be easily resolved by adjusting R_{g1} . Actually, the ratio of R_{g1} and R_1 can control the gain of biquad, implying that each biquad can be used as a PGA. We can simultaneously realize the functions of PGA and filter, which is also valuable for low power in analog baseband chain. The LBW-LPF-A is constructed by the LBW-Opamp-A. It achieves 7 MHz to 20 MHz tunable cutoff

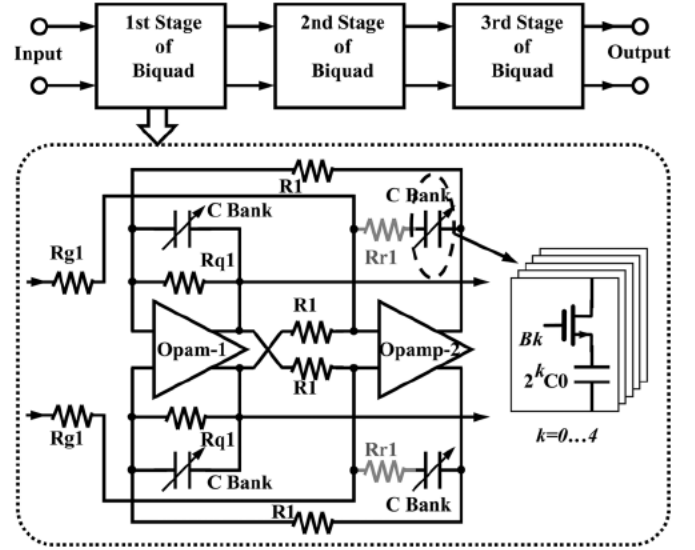


Fig. 14. The architecture of the proposed sixth-order active-RC low-pass filter.

frequency, but only consumes 260 μ A current from 1.8 V supply voltage. The LBW-LPF-B adopts the same architecture, and is constructed by the LBW-Opamp-B. It achieves 10 MHz cutoff frequency, merely consuming 220 μ A current from 1.8 V supply voltage.

B. HBW-LPF

1) *Customized Opamps*: The proposed HBW-LPF has the same architecture as depicted in Fig. 14. The 6th-order butterworth filter has three cascaded biquads, and the quality factor Q for the three biquads is 0.518, 0.707, and 1.932, respectively. The Q should satisfy the relationship as

$$GBW \geq 8 \cdot Q \cdot f_{\text{cutoff}} \quad (6)$$

where f_{cutoff} is the cutoff frequency of the filter. The different Q implies the different GBW requirement of the opamps. Thus, four opamps with scaled GBW and power are customized for different biquad to further save the power consumption.

2) *GBW Compensation Mechanism*: If the opamp GBW is not sufficient as the relationship (6), the transfer function of the filter will be distorted especially around the cutoff frequency. However, we noticed that the GBWs of the two opamps in the biquad have the opposite impacts on the transfer function. An opamp-based active-RC biquad with Q of 0.707 was constructed for analysis. As shown in Fig. 15, if the GBW of the first opamp in the biquad becomes smaller than the minimum GBW requirement, the magnitude response is rolled off around the cutoff frequency. While, if the GBW of the second opamp in the biquad becomes smaller, the magnitude response is rolled up around the cutoff frequency. If the GBW of the two opamps in the biquad has an appropriate relationship, the opposite impacts on the transfer function of the biquad can be cancelled out. This phenomenon can be employed to relax the opamp GBW requirement, which is beneficial for the low power. By analyzing and simulating, the relationships between the GBWs of the two opamps in the three cascaded biquads are determined. As a result, we customized four opamps with different GBW: Opamp-1

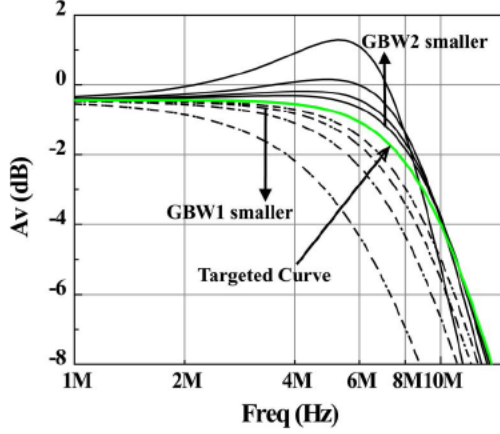


Fig. 15. The diagram of the opamp GBW compensation mechanism.

with 660 MHz GBW and 260 μA current; Opamp-2 with 950 MHz GBW and 300 μA current; Opamp-3 with 1.3 GHz GBW and 380 μA current; and Opamp-4 with 1.8 GHz GBW and 460 μA current. Opamp-1 and Opamp-3 are used for the first biquad with the Q of 0.518; Opamp-2 and Opamp-3 are adopted for the second biquad with the Q of 0.707; Opamp-2 and Opamp-4 are utilized for the third biquad with the Q of 1.932. Thanks to the GBW compensation mechanism, we customized four opamps with lower GBW, consequently save around 25% power consumption compared with the single-opamp solution.

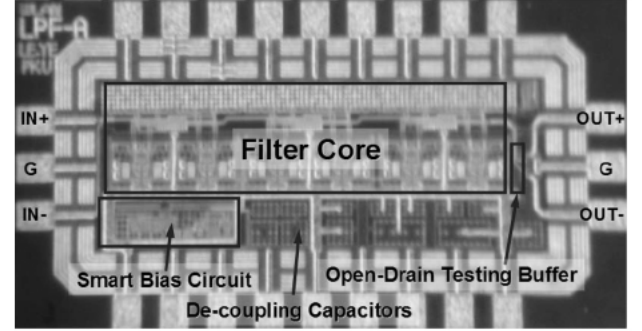
3) *Q-Degrading Scheme*: Moreover, a Q -degrading scheme by adding a resistor R_r is utilized to relax the Q factor requirement, which indicates the relaxed GBW requirement for the Opamps. Thus, we can use the Opamps with lower GBW and less power to construct the filter. Similar as [15], the proposed Q -degrading resistor locates at different position, as shown in Fig. 14. Since the GBW compensation mechanism is adopted to relax the opamp GBW requirement, this Q -degrading scheme plays an auxiliary role on relaxing the GBW requirement, which is not sensitive to PVT variations. So, Q -tuning circuit can be removed for saving power. Only the second and third biquads utilize the Q -degrading resistors.

V. MEASURED RESULTS

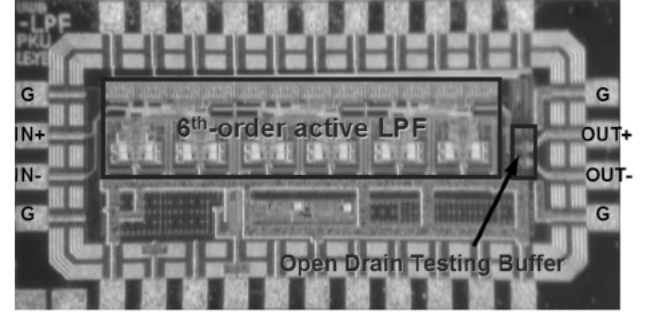
The proposed filters are fabricated in a standard 0.18 μm CMOS process. Two 50-to-200 Ω baluns are adopted for the differential-to-single transformation at the input and output of the chip. An open-drain testing buffer is integrated on chip to drive the 50 Ω load with unit gain and over 1 GHz bandwidth. The chips are directly bonded to the testing PCB board. The IIP3 of the testing buffer limits the measured linearity of the filter. But according to the cascade IIP3 formula in [24], the nonlinearity of the testing buffer can be easily excluded as relationship as

$$\text{IIP3}_{\text{filter}}^2 = \frac{\text{IIP3}_{\text{tot}}^2 \cdot \text{IIP3}_{\text{buffer}}^2}{\text{IIP3}_{\text{buffer}}^2 - \text{IIP3}_{\text{tot}}^2 \cdot G_{\text{filter}}^2} \quad (7)$$

where IIP3_{tot} , $\text{IIP3}_{\text{buffer}}$, $\text{IIP3}_{\text{filter}}$, and G_{filter} are the IIP3 of the chip with testing buffer, the IIP3 of the testing buffer, the actual IIP3 of the filter without testing buffer, and the gain of filter. They are all in the linear scale.



(a)



(b)

Fig. 16. The chip microphotograph of: (a) LBW-LPF-A; (b) HBW-LPF.

A. LBW-LPF-A and LBW-LPF-B

Fig. 16(a) demonstrates the chip microphotograph of the LBW-LPF-A using LBW-Opamp-A with type-A APP-SF buffer. The filter core occupies 0.21 mm^2 . It totally consumes 260 μA current from 1.8 V supply voltage, of which, 210 μA current is dissipated by the filter core and the other 50 μA current is consumed by the adaptive bias circuit.

Fig. 17 gives the measured magnitude response of the LBW-LPF-A with the selected frequency tuning bands. The -3 dB cutoff frequency can be tuned from 7.1 MHz to 20.3 MHz. The peaking in the passband edge is 5 dB for the maximum frequency band of 20.3 MHz. But it is less than 3 dB for the frequency bands of less than 17 MHz, which is acceptable for most wireless systems. Fig. 18 depicts the measured magnitude response of the LBW-LPF-B using LBW-Opamp-B with type-B APP-SF buffer. The filter achieves 10 MHz cutoff frequency, and merely consumes 220 μA current from 1.8 V supply voltage, of which, the filter core only dissipates 170 μA current, because the type-B APP-SF consumes less power than type-A APP-SF.

Fig. 19 describes the measured IP3 performance of the filter with the testing buffer, when the two-tone frequencies are 3 MHz and 5 MHz. According to (7), based on the measured 12.4 dBm (1.318 V) IIP3 of the chip, the measured 16 dBm (1.995 V) IIP3 of the standalone testing buffer, and -0.8 dB (0.912) gain of the filter, we can derive the actual IIP3 of the filter is 14.4 dBm (1.651 V) without the nonlinearity of the testing buffer. Additionally, the measured integrated input-referred noise (IRN) is 298 μV_{rms} , corresponding to 66.2 $\text{nV}/\sqrt{\text{Hz}}$ equivalent IRN density. It can be improved by using smaller feedback resistors and larger capacitors, resulting in a little higher power consumption of the opamp buffer to maintain the bandwidth. As for the

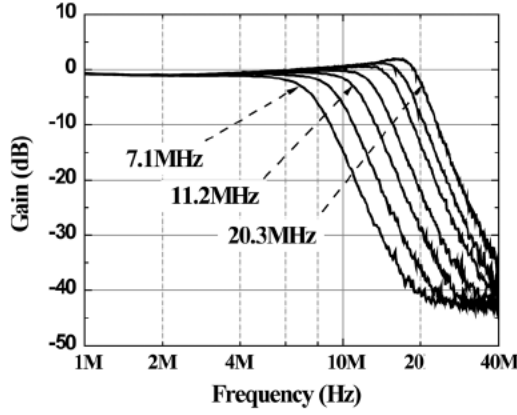


Fig. 17. The measured magnitude response of the LBW-LPF-A.

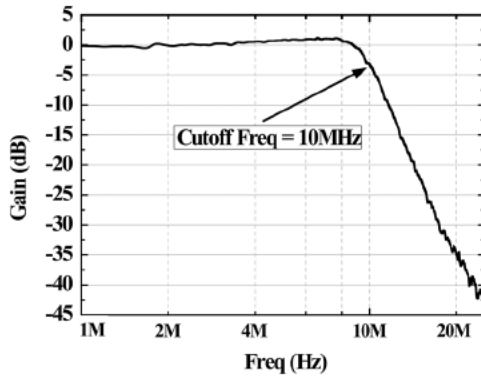


Fig. 18. The measured magnitude response of the LBW-LPF-B.

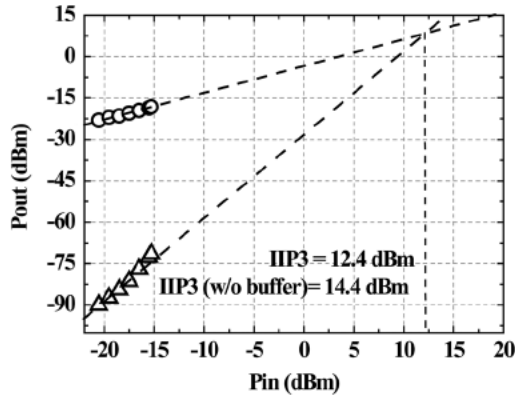


Fig. 19. The measured IIP3 performance of the LBW-LPF-A.

LBW-LPF-B, from the measured 12.1 dBm (1.274 V) IIP3 of the chip, the 16 dBm (1.995 V) IIP3 of the testing buffer, and 0 dB gain of filter, the actual IIP3 is 14.4 dBm (1.656 V) without the nonlinearity of the testing buffer. The IIP3 is nearly same as the LBW-LPF-A, because the MOSFET-based diodes in type-B APP-SF has very small affect on the linearity. The measured integrated IRN is 201 μV_{rms} , corresponding to 63.7 nV/ $\sqrt{\text{Hz}}$ equivalent IRN density.

Table I gives the comparison between this work and the state-of-the-art filters with the similar bandwidth. The normalized power of the proposed LBW-LPF-A and LBW-LPF-B are only 3.86 and 6.67 pW/pole/Hz, respectively, which are

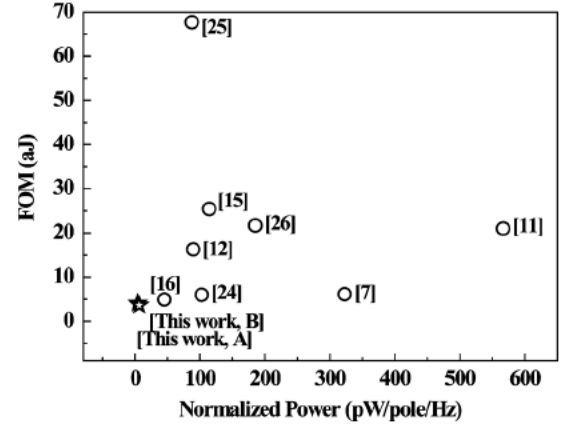


Fig. 20. Figure of merit versus normalized power among the recently published LBW-LPF.

significantly smaller than the others. For fair comparison, we use the widely-used figure-of-merit (FOM) [25], defined as follows:

$$\text{FOM} = \frac{P_C/N}{f_C \cdot (\text{SFDR} \cdot N^{4/3})} \quad (10)$$

where P_C is the power consumption of the filter, N is the filter order, f_C is the cutoff frequency, and $\text{SFDR} \cdot N^{4/3}$ is the normalized spurious free dynamic range, where SFDR is defined as

$$\text{SFDR} = (\text{IIP3}/P_N)^{2/3} \quad (11)$$

where P_N is the integrated IRN power of the filter. The FOM of the proposed LBW-LPF-A and LBW-LPF-B are 4.1 aJ and 3.6 aJ, respectively, which are much better than the recently published filters with the similar bandwidth. The noise and linearity of the proposed LPFs are not good, resulting in bad SFDR, because this work mainly focuses on the low power. The FOM of the proposed LBW-LPF-A and LBW-LPF-B are plotted versus the normalized power in Fig. 20 and fairly compared to the recently published works with the similar bandwidth.

B. HBW-LPF

Fig. 16(b) demonstrates the chip microphotograph of the HBW-LPF using HBW-Opamp with type-A APP-SF buffer. The filter core occupies 0.23 mm². Fig. 21 gives the measured magnitude response with the selected frequency tuning bands. The -3 dB cutoff frequency can be tuned from 240 MHz to 500 MHz. It totally consumes 2.3 mA current from 1.8 V supply voltage, of which 2 mA current is dissipated by the filter core and the other 0.3 mA current is consumed by the adaptive bias circuit. Although the GBWs of the opamps in HBW-LPF do not satisfy the requirement as (6), the ripple and the peak of the magnitude response are less than 1 dB, thanks to the opamp GBW compensation scheme and Q-degrading technique.

Fig. 22 describes the measured in-band IP3 performance of the HBW-LPF with the testing buffer, when the two tone frequencies are 115 MHz and 225 MHz. From the measured 9.7 dBm (0.966 V) IIP3 of the chip, 1.2 dB (1.148) voltage gain of the filter, and the 16 dBm (1.995 V) IIP3 of the testing buffer, we can calculate the actual IIP3 of the filter is 11.3 dBm (1.162 V)

TABLE I
COMPARISON OF THE RECENTLY THE STATE-OF-THE-ART LBW-LPFs

Parameters	This work		[7]	[26]	[15]	[11]	[27]	[28]	[12]	[16]
	A	B	JSSC 2006	ISSCC 2006	JSSC 2007	TCS-I 2007	JSSC 2009	JSSC 2009	JSSC 2011	JSSC 2011
Technology	0.18 μ m CMOS	0.18 μ m CMOS	0.13 μ m CMOS	0.18 μ m CMOS	0.13 μ m CMOS	0.35 μ m CMOS	0.13 μ m CMOS	0.18 μ m CMOS	0.09 μ m CMOS	0.18 μ m CMOS
Topology	active-RC	active-RC	active- Gm-RC	source-f ollower	active-RC	Gm-C	active-Gm- C	Gm-C	Gm-C	active-RC
VDD (V)	1.8	1.8	1.2	1.8	1.5	3.3	0.55	1.2	1	1.8
Order	6	6	4	4	5	5	4	3	6	5
Type	Butterworth	Butterworth	Bessel	Bessel	Chebyshev	Elliptic	Butterworth	Butterworth	Butterworth	Chebyshev
BW (MHz)	7.1~20.3	10	2.11/11	10	8.9~19.7	30	11.3	20	8.1~13.5	20
OIP3 (dBm)	13.6	14.4	25	14	18.3	NA	10	19	22.1	40.5
IRN (nV/ $\sqrt$ Hz)	66.2	63.7	10.9	7.5	30	21	33	12	75	219.1
SFDR (dB)	49.4	52.2	69.23	64.33	57.21	65	53.09	62.94	57.01	60.30
Power (mW)	0.47	0.4	14.2	4.1	11.25	85	3.5	11.1	4.35	4.5
Normalized Power (pW/pole/Hz)	3.86	6.67	322.73	102.50	114.21	566.67	87.50	185.00	89.51	45.00
Area (mm ²)	0.21	0.21	0.9	0.26	0.2	1.4	0.43	0.23	0.24	0.2
FOM (aJ)	4.1	3.6	6.1	6.0	25.4	21.0	67.7	21.7	16.3	4.9

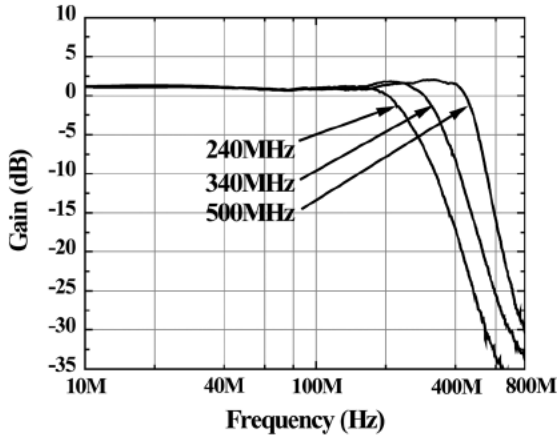


Fig. 21. The measured magnitude response of HBW-LPF with selected frequency-tuning bands.

without the nonlinearity of the testing buffer. As illustrated in Fig. 23, the measured out-of-band IIP2 performance is 34 dBm with two-tone frequencies of 450 MHz and 800 MHz, including the nonlinearity of the testing buffer. Additionally, Fig. 24 gives the measured IRN density. The integrated IRN power is 293 μ V_{rms}, corresponding to 13.1 nV/ $\sqrt$ Hz equivalent IRN density.

Table II gives the comparison between this work and the published state-of-the-art ultra-wideband filters. The normalized power is only 1.37 pW/pole/Hz, and the FOM is merely 1.66 aJ. Except the source-follower-based filter [30], the proposed 6th-order 240–500 MHz active-RC low-pass filter is the most power-efficient filter, in contrast with the opamp-based active-RC topology and even the Gm-C topology. The noise and linearity of the proposed LPFs are not good, resulting in bad SFDR, because this work mainly focuses on the low power. The FOM of the proposed HBW-LPF are plotted versus the normalized power in Fig. 26 and fairly compared to the recently published works with the similar bandwidth.

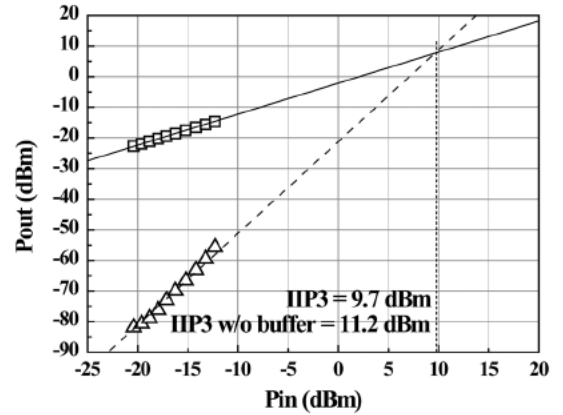


Fig. 22. The measured in-band IP3 performance of the HBW-LPF.

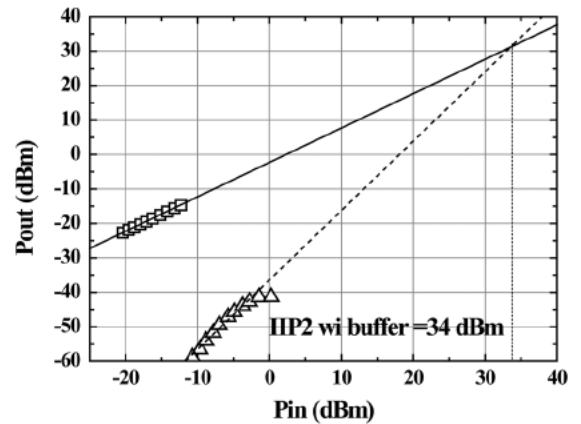


Fig. 23. The measured out-of-band IP2 performance of the HBW-LPF with testing buffer.

The proposed works in this paper have been used and verified in our developed wireless systems, such as the BD-II receiver for GNSS navigation [34], the ultra-low power transceiver for

TABLE II
COMPARISON OF THE RECENTLY THE STATE-OF-THE-ART HBW-LPFs

Parameters	This work	[17] ISSCC 2003	[29] ISSCC 2007	[30] ISSCC 2008	[31] TCS-I 2009	[18] TCS-I 2009	[32] A-SSCC 2009	[33] A-SSCC 2010
Technology	0.18 μ m CMOS	0.18 μ m CMOS	0.13 μ m CMOS	0.13 μ m CMOS	65nm CMOS	0.18 μ m CMOS	0.18 μ m CMOS	0.13 μ m CMOS
Topology	active-RC	active-RC	Gm-C	source-follower	Gm-C	active-RC	Gm-C	Gm-C
VDD (V)	1.8	1.8	1.2	1.2	1.2	1.8	1.8	1.5
Order	6	5	5	6	5	5	5	5
Type	Butterworth	Elliptic	NA	NA	Chebyshev	Chebyshev	Chebyshev	Chebyshev
BW (MHz)	240~500	500	240	280	275	44~300	250	70~280
OIP3 (dBm)	12.5	23.5	9.4	11	6.5/10	20.9~31.2	7.5	17
IRN (nV/ $\sqrt$ Hz)	13.1	18	7.7	33	7.8	49.6	10.5	14
SFDR (dB)	48.8	54.27	51.91	44.11	51.84	55.01	48.73	53.07
Power (mW)	4.1	90	24	0.12	36	54	34.2	21
Normalized Power (pW/pole/Hz)	1.37	36.00	20.00	0.07	26.18	36.00	27.36	15.00
Area (mm ²)	0.23	NA	0.34	0.018	0.21	0.21	0.48	0.12
FOM (aJ)	1.66	15.75	15.06	0.25	20.03	13.28	42.86	8.65

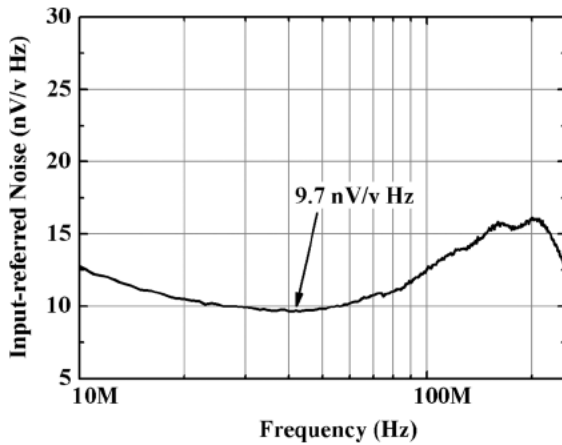


Fig. 24. The measured input-referred noise density of the HBW-LPF.

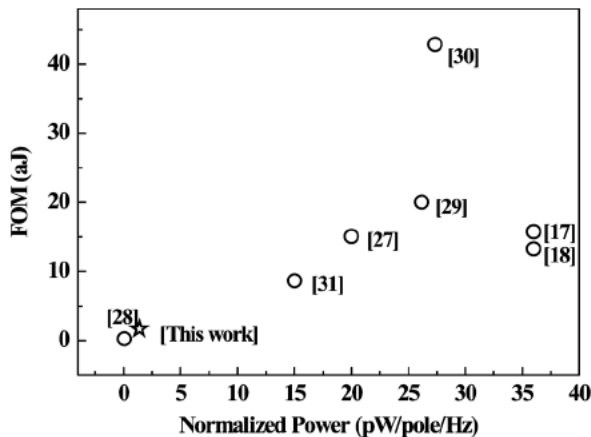


Fig. 25. Figure of merit versus normalized power among the recently published HBW-LPFs.

medical implant applications [35], and so on, which proves the ultra-low power performance and shows the practical value.

VI. CONCLUSION

This paper presents an ultra-low power 6th-order 7–20 MHz active-RC low-pass filter, an ultra-low power 6th-order 10 MHz active-RC low-pass filter, and an ultra-low power 6th-order 240–500 MHz active-RC low-pass filter in a standard 0.18 μ m CMOS process, which demonstrate the generic-purpose solution for the highly power-efficient active-RC filters suitable for wide bandwidth-range. The highly power-efficient opamps adopt the adaptive-biased pole-cancellation push-pull source follower (APP-SF) as the buffer stage to greatly reduce the power and extend the bandwidth. Due to the adaptive bias mechanism, the opamps are able to tolerate PVT variations. The high-bandwidth filter adopts the GBW compensation mechanism and the Q-degrading scheme to relax the opamp GBW requirement in the biquads, which further reduces the power consumption. The LBW-LPF-A and LBW-LPF-B achieves 7–20 MHz and 10 MHz cutoff frequency, 14.4 dBm in-band IIP3, and 66.2 nV/ $\sqrt$ Hz and 63.7 nV/ $\sqrt$ Hz equivalent input-referred noise density. But they only consume 260 μ A and 220 μ A current from 1.8 V supply voltage, corresponding to the normalized power of 3.86 and 6.67 pW/pole/Hz, and 4.1 aJ and 3.6 aJ FOM. The HBW-LPF realizes 240–500 MHz cutoff frequency, 11.3 dBm in-band IIP3, and 13.1 nV/ $\sqrt$ Hz input-referred noise density. But it merely dissipates 2.3 mA from 1.8 V supply voltage, corresponding to the normalized power of 1.37 pW/pole/Hz, and 1.66 aJ FOM. Among the recently published continuous-time filters with similar bandwidth, the proposed active-RC filters give us solution for low-pass filter with competitive power-efficiency.

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