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CURRENT EFFICIENT, LOW VOLTAGE, LOW DROP-OUT REGULATORS

A THESIS

Presented to the Academic Faculty

by

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CURRENT EFFICIENT, LOW VOLTAGE,

LOW DROP-OUT REGULATORS

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For the hopes of

peaceful coexistence and universal brotherhood !

FOREWORD

The research focuses on the realization of current efficient, low voltage, low drop-out regulators. These characteristics are driven by portable and battery operated products requiring compactness and low power. The approach adopted is to develop circuit techniques that allow maximum use of current existing process technologies. As a result, future and more advanced technologies will have even greater benefits. The dissertation is organized to reflect the necessary sequence of events that lead up to the complete design of a system.

Chapter 1 introduces low drop-out regulators. Their definition and motivation for existence are addressed here. The alternative, or in some cases the supplement, type of regulator is compared to further elucidate the demand of low drop-out regulators in today's market. A typical circuit architecture is illustrated along with a description of the basic characteristics inherent to the system and required by the loading circuits. Lastly, the chapter concludes by identifying and defining the objective of the research.

Chapter 2 discusses the considerations necessary to successfully design the circuits. The loading requirements, which partially determine the frequency response of the control loop, are identified. Their implications on circuit limitations and challenges are illustrated. This is followed by a transient analysis describing the typical response of the system along with the difficulties imposed by low voltage and low quiescent current flow. Finally, the specific circuit implications and requirements of the major blocks of the system are discussed, i.e., the pass device, the error amplifier, and the reference circuit.

A literature survey of the different prevailing topologies for low drop-out regulators is illustrated in chapter 3. The circuit realization of each topology is discussed.

The circuits highlighted are realized in relatively inexpensive technologies to constrain the research orientation to generalized circuit techniques and not towards manipulation of the processes. The main concepts are emphasized and evaluated for their appropriateness in a low voltage and low quiescent current atmosphere. Furthermore, circuit enhancement techniques are also studied to show the different ways that the system can be amended to yield improved performance on particular specification parameters.

Techniques that allow proper and practical realization of low drop-out regulators at low input voltages and low quiescent current flow are developed in chapter 4. The motivation and challenges are identified. The areas highlighted include current efficiency, current boosting, and load regulation enhancement. The advantages and the drawbacks of the circuits used to realize these concepts are discussed within the context of a low voltage environment.

Chapter 5 shows the development of a low voltage and curvature corrected bandgap reference. The development starts at the conceptual roots of zener references and first order bandgaps and continues on to curvature corrected references. Respective output structures are discussed and evaluated for their propriety in the system at hand. The chapter then illustrates the different curvature correcting schemes and concludes with the most suitable for the system.

The concepts developed in chapters 4 and 5 are used to design the actual circuit blocks. These circuits are described and illustrated in chapter 6. They include the composite pass device, the gain stage of the amplifier, the buffer stage of the amplifier, and the curvature corrected bandgap reference. The pass device is developed to reap the benefits of current boosting. The amplifier is designed to take advantage of the current efficiency and the load regulation enhancement concepts discussed in chapter 4. Lastly,

the design of the reference reflects the concepts cultivated in chapter 5. The chapter ends with a discussion of the trimming requirements of the bandgap reference.

All the circuit blocks designed in chapter 6 are used to realize the system in chapter 7. Physical design issues are discussed within the context of existing process technologies, such as CMOS, bipolar, and biCMOS processes. This is followed by a discussion of appropriate protection circuitry. The chapter then continues to show the experimental results of the prototype circuit fabricated in MOSIS 2 μm CMOS technology with an added p-base layer. Finally, a summary of the performance specifications obtained as well as those targeted are discussed and illustrated in a table.

Chapter 8 brings forth the conclusions of the research as well as the implications thereof. The enabling techniques for low voltage and low quiescent current flow operation are summarized and discussed in perspective of the overall system. The direction of market demand in terms of technology and circuit requirements is also discussed. The chapter ends with a few concluding statements pertaining to the research as well as recommendations for future work in the area.

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SUMMARY

Regulators are an essential part of any electrically powered system, which includes the growing family of applications of portable battery operated products. Regulators are required to reduce the large voltage variations of battery cells to lower and more acceptable levels. Absence of these power supplies can prove to be catastrophic in most high frequency and high performance circuit designs. As a result, low drop-out regulators and other power supply circuits are always in high demand. In fact, the increasing drive towards total chip integration (single chip solutions) demands that power supply circuits be included in every chip. This is a consequence of the public demand for smaller and less expensive portable products.

In particular, the increasing demand for portable battery operated products has driven power supply design towards low voltage and low quiescent current flow, i.e., cellular phones, pagers, camera recorders, laptops, etc. The thrust is towards reducing the number of battery cells, required to decrease cost and size, while minimizing quiescent current flow to increase battery life. Current efficiency is particularly important because at low load-current conditions the life of the battery is adversely affected by low current efficiency, in other words, high quiescent current flow. At high load-currents, on the other hand, current efficiency is typically high because load-current is significantly larger than quiescent current. In this low voltage environment, a low drop-out regulator is the most appropriate form of linear regulators. However, the prevailing designs do not work at input voltages suitable for single, low voltage battery cells. This research develops techniques that enable practical circuit realizations of low drop-out regulators at low input voltages and low quiescent current flow without sacrificing performance.

An intimate knowledge of the system reveals that the frequency stability requirements are dependent on load-current. As a result, a load dependent biasing buffer is designed to minimize current flow during low load-current conditions. Moreover, suitable biasing conditions result during transient load-current steps. This transient aid comes in the form of increased slew-rate current capabilities during conditions that warrant it. Another problem with low voltage in a CMOS environment is reduced gate drive for the power transistor. In other words, the output current capability per unit area of the power device under low voltage conditions is appreciably less than its higher voltage counterpart. However, gate drive can be effectively increased by reducing the threshold voltage. This is done by forward biasing the source to bulk junction of the power PMOS device and thus exploiting the bulk effect phenomenon. Yet another problem with low voltage is the realization of an accurate reference voltage. Typical bandgap references are restricted by input voltages greater than approximately 1.4 V (V_{sat} above the bandgap voltage). A circuit topology suitable for low voltages and curvature compensation is developed.

The overall system is designed, simulated, and experimentally evaluated. The process technology utilized is MOSIS 2 μm CMOS with a p-base layer. However, most of the techniques can be adapted to almost any technology ranging from bipolar and vanilla CMOS to relatively inexpensive and full blown biCMOS processes. As a result, the resulting system can be designed and optimized for low cost. The physical layout implications of the circuit realization are discussed with emphasis on reliability and performance. The findings show that a successful low voltage design is achieved by implementing the techniques developed. Furthermore, the techniques also showed that they are appropriate for maximizing performance of most linear regulator designs outside the realm of low voltage.

CHAPTER I

INTRODUCTION

The demand for low drop-out regulators has been driven by the portable electronics market as well as industrial and automotive applications. Most recently, the increasing demand for portable and battery operated products have forced these circuits to operate under lower voltage conditions. Furthermore, high current efficiency has also become necessary to maximize the lifetime of the battery. Battery life is determined by the total current drain composed of quiescent current and load-current. This chapter discusses the role and the characteristics of low drop-out regulators in today's market. The objective of the research is then identified and defined according to the demands that drive regulator design into the future.

1.1 Definition

A series low-drop-out regulator is a circuit that provides a well specified and stable dc voltage [1] whose input to output voltage difference is low [2]. The drop-out voltage is defined as the value of the input/output differential voltage where the control loop stops regulating. The term series comes from the fact that a power transistor (pass device) is connected in series between the input and the output terminals of the regulator [3]. The operation of the circuit is based on feeding back an amplified error signal to control the output current flow of the power transistor driving the load. This type of regulator has

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two inherent characteristics: (1) the magnitude of the input voltage is greater than the respective output and (2) the output impedance is low to yield good performance [2]. Low drop-out (LDO) regulators can be categorized as either low power or high power. Low power LDOs are typically those with a maximum output current of less than 1 A, exhibited by most portable applications. On the other hand, high power LDOs can yield currents that are equal to or greater than 1 A to the output, which are commonly demanded by many automotive and industrial applications [4].

1.2 Market Demand

Current Efficiency, Low Voltage, and Low Drop-out

As a result of high variations in battery voltage, regulators are demanded by virtually all battery operated applications. Furthermore, most designs find it necessary to include regulators and other power supply circuits as products achieve or approach total chip integration. Low drop-out regulator are appropriate for many circuit applications, namely, automotive, portable, industrial, and medical applications. In the automotive industry, the low drop-out voltage is necessary during cold-crank conditions where the battery voltage can drop below 6 V. The increasing demand, however, is readily apparent in mobile battery operated products, such as cellular phones, pagers, camera recorders, and laptops [5]. This portable electronics market requires low voltage and low quiescent current flow for increased battery efficiency and longevity [6]. As a result, high current efficiency is necessary to maximize battery life. Low voltage operation is also a consequence of the direction of process technology towards higher packing densities [7]. In particular, isolation barriers decrease as the component densities per unit area are increased thereby manifesting lower breakdown voltages [8, 9]. Minimization of drop-out voltages in a low voltage environment is also necessary to maximize dynamic range. This

is because the signal-to-noise ratio decreases as the power supply voltages decrease while noise typically remains constant [10, 11]. Consequently, low power and finer lithography drive regulators to operate at lower voltages, produce precise output voltages, and require low quiescent current flow [9]. By the year 2004, the power supply voltage is expected to be as low as 0.9 V in 0.14 μm technologies [9, 12]. Lastly, financial considerations also require that these circuits be fabricated in relatively simple processes, such as standard CMOS, bipolar, and stripped down biCMOS technologies [13].

Alternative: Switching Regulators

The alternatives to low drop-out regulators are dc-dc converters, switching regulators. Switching regulators are essentially mixed-mode circuits that feed back an analog error signal and digitally gate it to provide bursts of current to the output. The circuit is inherently more complex and costly than LDO realizations [9]. Furthermore, switching regulators can provide a wide range of output voltages including values that are lower or greater than the input voltage depending on the circuit configuration, buck or boost. The circuit, for the most part, requires a controller with an oscillator, pass elements, an inductor, capacitors, and diodes. Some switched-capacitor implementations do not require an inductor [14, 15].

The worst-case response time of a dc-dc converter is dependent on the oscillating frequency of the controller (approximately 20 to 200 kHz [16]) and circuit delay. As a result, the corresponding response time is roughly between 6 and 8 μs, whereas the LDO typically requires between 1 and 2 μs [12]. Since the pass elements switch high currents through an inductor at the rate of the oscillator, the output voltage is inherently noisy. This is especially true for boost configurations where RF noise tends to be worse [17]. The high noise present is a consequence of the rectified inductor voltage behavior of the

output of these converters. Furthermore, start-stop clock operation (on/off sleep-mode transitions) further aggravates the noise content of the output voltage [12].

On the other hand, switching regulators benefit from having high power efficiency and the ability to generate larger output voltages than the input. They can yield efficiencies between 80 and 95 % [18]. The efficiency of the LDO counterpart is limited by the quiescent current flow and the input/output voltages, and is expressed as

$$\text{Efficiency}_{\text{Power}} = \frac{I_o V_o}{[I_o + I_q] V_i} \leq \frac{V_o}{V_i}, \tag{1.1}$$

where I_o and V_o correspond to the output current and voltage, V_i is the input voltage, and I_q is the quiescent current or ground current. The main power issue in LDO design is battery life, in other words, the output current flow of the battery. When the load-current is low, which is the normal operating mode for many applications, the quiescent (ground) current becomes an intrinsic factor in determining the lifetime of the battery. Consequently, current efficiency is important during low load-current conditions. Power efficiency, on the other hand, becomes more pertinent during high load-current conditions where quiescent current is negligible relative to the output current.

If the maximum load-current is much greater than the ground current, then the maximum possible power efficiency is defined by the ratio of the output and the input voltages, as seen in equation (1.1). Power efficiency increases as the voltage difference between the input and the output decreases. Under these conditions, LDOs are better suited for many applications than switching regulators because of lower cost, complexity, and output noise. The choice becomes obscure, however, if the output current increases to the point where the LDO requires a heat sink [12]. A heat sink not only increases cost

by requiring an additional component but it also means more real estate area overhead on the board, which further increases cost. Applications that require high input/output voltage differentials with high output currents greatly benefit from the efficiency of dc-dc converters. Nevertheless, there are some cases where a high input/output voltage differential regulator is required to drive noise sensitive circuits. In these situations, a switching regulator is used to bring down the voltage and an LDO is cascaded to provide a low noise output [4, 18]. These conditions arise in mixed-mode designs where circuits that perform analog functions tend to be more sensitive to noise originated in the supply rails than the digital counterparts [17, 19]. Other applications require output voltages that are larger than the respective inputs. In these situations, dc-dc converters are necessarily used, be it in the form of a boost topology, a boosting switch capacitor implementation, or a charge pump structure. However, LDOs are still required in these applications to suppress noise generated by the switching pre-regulator. In summary, both LDOs and switching regulators have their place in today's market demand.

1.3 Characteristics

Block Level Description

Figure 1.1 illustrates the block level diagram of a generic series low drop-out regulator. The circuit is composed of a reference and associated start-up circuit, protection circuit and associated current sense element, an error amplifier, a pass element, and a feedback network. The reference provides a stable dc bias voltage with limited current driving capabilities. This is usually a zener diode or a bandgap reference. The zener diode finds its applications in high voltage circuits (greater than approximately seven volts) with relaxed temperature variation requirements [1, 3]. The bandgap, on the other hand, is better suited for low voltage and high accuracy applications. The protection

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circuitry ensures that the LDO operates in safe stable conditions. Some of its functions include over-current protection (typically a foldback current limiter [6]), thermal shutdown in case of self-heating (junction temperature increases beyond safety levels), and other similar functions. The error amplifier, the pass element, and the feedback network constitute the regulation loop. The temperature dependence of the reference and the amplifier's input offset voltage define the overall temperature coefficient of the regulator; hence, low drift references and low input offset voltage amplifiers are preferred [20, 21].

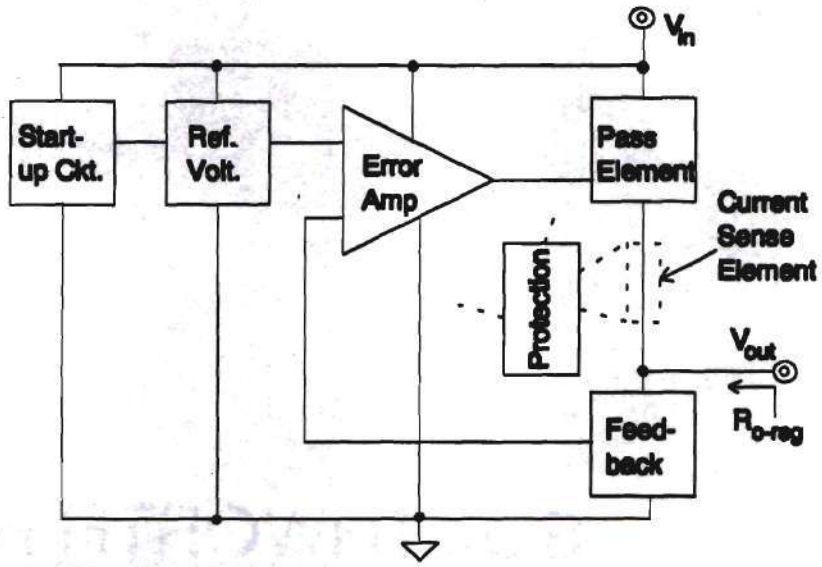


Figure 1.1. Generic low drop-out series linear regulator architecture.

Performance

Overall noise performance is strongly dependent on the physical layout of the chip and the respective process technology. In particular, the noise present at the output of the LDO is composed of three components, namely, noise injected from the system through the substrate and the input voltage, noise generated by the reference circuit, and noise associated with the output trace (lead) inductance and resistance [4]. Switching regulators

can typically be used to provide power to LDOs and can be integrated in the same chip as the LDO thereby injecting noise through the substrate and the input voltage, i.e., cellular phones. In these cases, physical layout isolation techniques and high power supply rejection ratio are intrinsic circuit characteristics for good noise performance. Transient load-current changes also affect the noise content seen by the load. This results from the parasitic resistance and inductance of the trace (lead) from the LDO's output to the load. Therefore, physical proximity of the LDO to its load must be minimized to reduce the noise seen by the load [12].

Low drop-out regulators tend to necessitate large output capacitors that occupy large board areas. Furthermore, typical LDOs require that these capacitors have low electrical series resistance (ESR). Consequently, capacitors play an intrinsic role in the cost of the LDO. High power LDOs may require heat sinks further aggravating the cost issue. However, a system level design choice may circumvent the need for a heat sink by utilizing several smaller LDOs distributed throughout the board [4]. Finally, the emergence of finer lithography and the increasing demand for low power cause low voltage operation to be a necessary condition. Therefore, there are some circuit design techniques that are discouraged, which give rise to more complex and possibly more expensive circuits. Some of the discouraged techniques include unnecessary cascoding, emitter followers, and Darlington configurations [10].

1.4 Specifications

System

The important aspects of the LDO can be summarized into three categories, namely, regulating performance, quiescent current flow, and operating voltages [22]. Some of the specifications that serve as metrics for the LDO include drop-out voltage, line

regulation, load regulation, tolerance over temperature, output voltage variation resulting from transient load-current steps, output capacitor and ESR range, quiescent current flow, maximum load-current, and input/output voltage range. The requirements of these performance characteristics often contradict each other giving rise to necessary compromises. The priority of the performance parameters is defined according to the particular application.

Drop-out voltage is the minimum input/output differential voltage where the circuit just ceases to regulate. This can be expressed in terms of switch "on" resistance, R_{on} [6],

$$V_{drop\text{-}out} = I_{Load} R_{on}. \tag{1.2}$$

Typical drop-out voltages range from 0.1 to 1.5 V [4]. The output voltage variation arising from a specific change in input voltage is defined as line regulation. Similarly, load regulation is the change in output voltage for specific changes in load-current [2]. Load regulation is essentially the output resistance of the regulator ($R_{o\text{-}reg}$),

$$R_{o-reg} = \frac{\Delta V_{LDR}}{\Delta I_o} = \frac{R_{o-pass}}{1 + A_{ol}\beta}, \tag{1.3}$$

where ΔV_{LDR} and ΔI_o are the output voltage and the load-current changes, $R_{o\text{-}pass}$ is the output resistance of the pass element, A_{ol} is the open-loop gain of the system, and β is the feedback factor [3]. Therefore, load regulation performance is improved as the dc open-loop gain is increased [12]. The temperature dependence of the output voltage is a

function of the temperature drift of the reference and that of the input offset voltage of the error amplifier,

$$TC = \frac{1}{V_O} \cdot \frac{\partial V_O}{\partial Temp} \approx \frac{1}{V_O} \cdot \frac{\Delta V_{TC}}{\Delta Temp} = \frac{\left[\Delta V_{TC_{ref}} + \Delta V_{TC_{Vos}}\right] \frac{V_O}{V_{ref}}}{V_O \Delta Temp}, \quad (1.4)$$

where TC is the temperature coefficient, ΔV_{TC} is the output voltage variation over the temperature range $\Delta Temp$, $\Delta V_{TC_{ref}}$ and $\Delta V_{TC_{Vos}}$ are the voltage variations of the reference and input offset voltage of the error amplifier, and V_O / V_{ref} is the ratio of the nominal output and reference voltages. Transient output voltage variations resulting from sudden load-current changes are dominated by the closed-loop bandwidth of the system, output capacitor, and load-current. The worst-case situation occurs when the load-current suddenly steps from zero to its maximum specified value. The resulting output voltage variation is described as

$$\Delta V_{tr} \approx \frac{I_{Load-max}}{C_O + C_b} \Delta t + \Delta V_{esr}, \quad (1.5)$$

where ΔV_{tr} is the output voltage change, $I_{Load-max}$ is the maximum specified load-current, C_O is the output capacitor, C_b refers to the bypass capacitors, ΔV_{esr} is the voltage variation resulting from the electrical series resistance (ESR) of the output capacitor, and Δt is the time required for the LDO to respond (approximately equal to the reciprocal of the closed-loop bandwidth (BW_{cl}) if internal slew-rate conditions are neglected). The voltage variation resulting from ESR results because of the momentary current (provided by C_O) flowing through the ESR. This is reduced by the high frequency nature of the

bypass capacitors (low ESR capacitors). In other words, the bypass capacitors (C_b) help filter out the effects of the output capacitor ESR. Consequently, fast response times and low ESR values are necessary to yield low transient output voltage variations. Low output voltage variations are desired to meet the overall accuracy requirements of the system, i.e., 150 - 300 mV [9]. Thus, the circuit as a whole benefits from the use of a high bandwidth amplifier in the feedback loop. A pivotal specification is the output capacitor and associated ESR range for which the LDO is stable. This can typically prove to be a difficult task if a wide range of values is to be allowed. The value of the load-current also affects the frequency response of the circuit. Lastly, long term stability and low external component count are also pertinent factors to keep in mind when designing LDOs.

The effects of line regulation, load regulation, temperature dependence, and transient output voltage variations can be summed up into one specification, accuracy. Accuracy refers to the total output voltage variation and can be described by the absolute minimum and maximum output voltages ($V_{o\text{-}min}$ and $V_{o\text{-}max}$), shown in the following equations:

$$V_{o-min} \le \Delta V_{LNR} + \Delta V_{LDR} + \Delta V_{TC} + \Delta V_{tr} + V_{reference}\left\langle \frac{V_o}{V_{ref}} \right\rangle \le V_{o-max}, \quad (1.6)$$

$$V_{reference} = V_{ref} + \Delta V_{TC_{ref}} + \Delta V_{LNR_{ref}} \pm V_{os}, \quad (1.7)$$

$$Accuracy_{system} = \left\langle \frac{V_{o-max} - V_{o-min}}{V_o} \right\rangle, \quad (1.8)$$

where ΔV_{LNR}, ΔV_{LDR}, ΔV_{TC}, ΔV_{tr}, ΔV_{TCref}, and ΔV_{LNRref} are voltage variations resulting from line regulation, load regulation, temperature dependence, worst-case transient load-current steps, reference circuit's temperature dependence, and reference circuit's line regulation respectively while V_{os} and V_o are the input offset voltage of the error amplifier and the nominal output voltage of the regulator. In specifying accuracy, the effect of the transient load-current step and the reference circuit is sometimes excluded but they are included here for completeness. Low voltage operation often implies more stringent specifications in the form of overall accuracy. Typical implementations achieve roughly 1 to 2 % total variation resulting from load regulation, line regulation, and temperature dependence while leaving some headroom for transient output voltage variations [12].

Reference

The specifications of the reference include line regulation, temperature dependence, quiescent current flow, and input voltage range. The effects of line regulation and temperature drift on system accuracy are shown in equations (1.6) - (1.7). Line regulation refers to the variation of the reference voltage arising from a unit change in input voltage. In the same token, the temperature coefficient of the reference (TC_{ref}) refers to the variation in output voltage as a result of unit changes in temperature and can be expressed as

$$TC_{ref} = \frac{1}{V_{ref}} \cdot \frac{\partial V_{ref}}{\partial Temp} \approx \frac{1}{V_{ref}} \cdot \frac{\Delta V_{TCref}}{\Delta Temp}, \qquad (1.9)$$

where ΔV_{TCref} is the reference voltage change resulting from a temperature variation equal to $\Delta Temp$ and V_{ref} is the nominal reference voltage. The overall accuracy of references is

determined by the combination of line regulation and temperature coefficient performance and is described as

$$\text{Accuracy}_{\text{reference}} = \frac{\Delta V_{TC_{ref}} + \Delta V_{LNR_{ref}}}{V_{ref}}, \qquad (1.10)$$

where $\Delta V_{TC_{ref}}$ and $\Delta V_{LNR_{ref}}$ are voltage variations resulting from temperature dependence and line regulation respectively. Load regulation is sometimes included in the accuracy of the reference but most appropriately specified for regulator structures.

1.5 Research Objective

The objective of this research is to enhance performance of low drop-out (LDO) regulators for battery powered electronics. This is targeted to fulfill the present commercial requirements as well as the projected demands of the future. Such an endeavor makes certain characteristics necessary, namely, low quiescent current flow for increased battery life, low voltage operation, and high output current. The techniques that are developed to overcome the aforementioned obstacles not only enhance the prevailing LDO circuit architecture but also push regulator design into the 21st century. This is done with existing standard technologies; thus, the designs take full advantage of all physical aspects of the process while maintaining fabrication costs to acceptable and competitive levels. Moreover, the new design techniques will be able to further exploit the benefits of more advanced technologies in the future.

The intrinsic issues in designing a current efficient (low quiescent current) and low drop-out linear regulator in a low voltage environment can be identified as stability, maximum output current, and regulating performance. Stability in a low quiescent current

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atmosphere is difficult to achieve because of the presence of potentially low frequency parasitic poles. These are easily circumvented by increasing bandwidth, which usually results at the expense of higher quiescent current flow. Maximum output current capabilities of regulators also becomes restricted under low voltage conditions. This results from the inherent reduction in gate drive for the pass element when input voltages are decreased. Finally, low voltage circuits tend to limit the regulating performance of regulators because of problems with headroom. As input voltages decrease, the use of common circuit techniques that enhance performance becomes restrained, i.e., cascoding, Darlington configurations, and source [emitter] followers [10]. In a battery powered environment, the number of devices connected from the input voltage to ground must be kept low [10]. The ultimate limit is one diode drop plus one output saturation voltage, V_{be} [V_{gs}] + $V_{ec\text{-}sat}$ [$V_{sd\text{-}sat}$].

An input voltage range appropriate for single, low voltage battery cells is targeted (0.9 to 1.5 V). The circuit technology is MOSIS 2 μm CMOS with an added p-base layer, a relatively inexpensive process. The minimum operating voltage possible for this technology is approximately between 1 and 1.1 V, $V_{sg\text{-}pmos}$ + $V_{ds\text{-}nmos}$. For maximized battery life, the circuits must be current efficient and micro-power. The zero-load quiescent current goal is approximately 60 to 65 μA including the reference and the regulating loop, 15 - 20 μA for the reference and 40 - 45 μA for the remainder. Since the thrust of the driving market demand lies in battery operated regulators, the output current range is defined to be between 50 and 100 mA for respective input voltages ranging from 1.2 to 1.5 V. The design criteria also focuses on minimizing transient output voltage variations resulting from fast load-current step transitions, less than 75 mV.

To further mitigate overall costs, standard tantalum capacitors are used for the output. These are among the least expensive with an electrical series resistance (ESR)

range of up to approximately 10 Ω [23]. The target range of ESR is extended to zero to cater to applications where low ESR is necessary. Low values of ESR are demanded for high power supply rejection ratio (PSRR) performance at high frequencies and minimized transient output voltage variations. The PSRR performance of LDOs (generically illustrated in Figure 1.2) at high frequencies is approximated to be

$$\mathrm{PSRR} = \frac{\Delta V_{supply}}{\Delta V_o} \cdot \frac{V_o}{V_{ref}} = \frac{\Delta V_{in}}{\Delta V_o} A_v(s) \approx \frac{R_{o-pass} + R_{esr}}{R_{esr}} A_v(s), \qquad (1.11)$$

where ΔV_{supply} is equivalent to ΔV_{in} for regulators, $A_v(s)$ is the open-loop gain from V_{ref} to V_o, and the terminology of Figure 1.2 is adopted. Consequently, PSRR at high frequencies, when $A_v(s)$ approaches unity, greatly benefits from low ESR values. This is

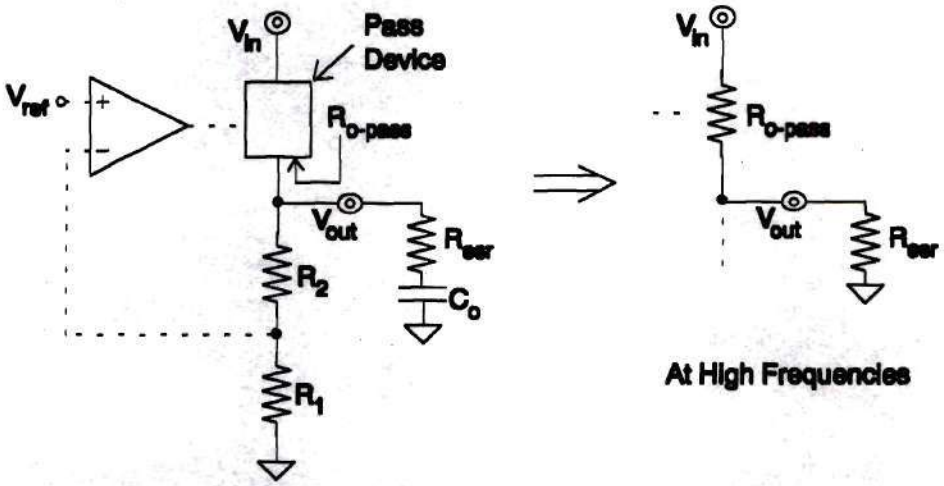


Figure 1.2. PSRR performance implications of high frequency operation.

especially important when considering that $R_{o\text{-}pass}$ for CMOS structures is relatively low because of short channel lengths, which result in poor early voltage performance. Power MOS transistors require shorter channel lengths to provide larger output currents. Power

supply rejection ratio performance at high frequencies is important in designs that integrate a switching regulator on to the same chip as the LDO. This results in injection of systematic noise to the output at the frequency of the clock , typically between 100 and 500 kHz.

The typical specifications for low voltage LDOs (≥ 2.3 V input voltage range) include drop-out voltages of 0.4 to 0.9 V at output currents of 40 mA and output voltage accuracy of 4 to 5 % [24, 25, 26]. The design target focuses on a drop-out voltage ranging from 0.2 to 0.3 V at a load-current of 50 to 100 mA (corresponding to an "on" resistance (R_{on}) of 2 to 6 Ω) with a total tolerance of roughly ± 3 to 5 %. Furthermore, the regulator's destination is the commercial market place with a temperature range of -10 to 90 °C, which includes customary temperature limits. Table 1.1 illustrates a summary of the objective performance parameters for this research.

1.6 Summary

This chapter has defined a low drop-out regulator (LDO) and discussed its standing in today's market. The characteristics that are most demanded by the growing number of applications were identified. This was followed by a discussion of switching regulators and their place alongside LDOs. The main building blocks of low drop-out regulators were described as well as some of their associated performance parameters. Moreover, the specifications that gauge these circuits were defined. Lastly, the research objective was identified and defined according to the growing requirements of current and future applications. Overall, this chapter forms the premise and establishes enough background to start analyzing the system under loading conditions and start considering the electrical implications of such an architecture.

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Table 1.1 Summary of the objective specifications.

Description	Specification
V_{in}	≥ 1.2 V
I_q	≤ 65 µA
$I_{out\text{-}max}$	≥ 50 mA
Accuracy	± 3 to 5 %
$V_{drop\text{-}out}$ @ I_{Load} = 50 - 100 mA	≤ 0.3 V
R_{on}	2 to 6 Ω
Transient $\Delta V_{o\text{-}for\ I_{Load\text{-}Step}}$	≤ 75 mV
Temperature	-10 to 90 °C
Output Capacitance	4.7 µF
ESR	0 to 10 Ω
Technology: MOSIS 2 µm n-well CMOS with added p-base layer	

CHAPTER II

SYSTEM DESIGN CONSIDERATIONS

Proper design of a low drop-out (LDO) regulator involves intricate knowledge of the system and its load. The tasks of maximizing load regulation, maintaining stability, and minimizing transient output voltage variations prove to be challenging and often conflicting. This arises from the innate characteristics of the regulator architecture and its associated working environment. This chapter discusses the relevant analyses that describe the system. Lastly, some of the circuit design issues surrounding the major components of the low drop-out regulator are illustrated in terms of circuit theory and system requirements; these building blocks include the pass device, the amplifier, and the reference.

2.1 AC Analysis

Loading Conditions

Figure 2.1 illustrates the intrinsic factors that determine the stability of the system, namely, an error amplifier, a pass element, feedback resistors, an output load-current and associated output impedance, an output capacitor and associated electrical series resistance (ESR), and bypass capacitors. It is assumed that there is no ac signal polarity inversion across the pass device, corresponding to n-type transistor implementations. The polarity of the error amplifier terminals would be reversed for p-type devices, which

introduce a polarity inversion ($-g_{mp}$ instead of g_{mp}). The ESR of the bypass capacitors can typically be neglected because they are usually high frequency capacitors; in other words, they have low ESR values [23]. The pass device is modeled as a circuit element exhibiting a transconductance of g_{mp} and an output impedance of $R_{o\text{-}pass}$. The value of R_2 is dependent on the desired value of the output voltage, i.e., R_2 is zero if V_{out} is desired to be equal to V_{ref}. The value of R_1, on the other hand, is designed to define the quiescent current flowing through resistors R_1 and R_2 ($R_1 = V_{ref} / I_{R1}$), which is typically high to minimize quiescent current overhead.

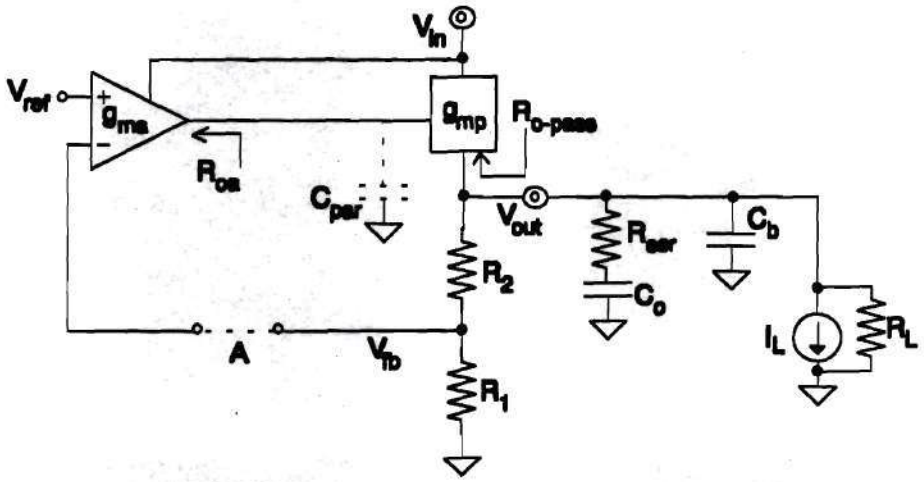


Figure 2.1. System model under loading conditions.

Frequency Response

For the purpose of analysis, the feedback loop can be broken at "A" in Figure 2.1. It is readily apparent that the system must be unity gain stable, considering V_{ref} and V_{fb} to be the input and the output voltages respectively. The open-loop gain can be described as

$$\frac{V_{fb}}{V_{ref}} = |A_v| = \frac{g_{ma} R_{oa} g_{mp} Z}{[1 + sR_{oa} C_{par}]} \cdot \frac{R_1}{[R_1 + R_2]}, \qquad (2.1)$$

where g_{ma} and g_{mp} refer to the transconductance of the amplifier and the pass element respectively, R_{oa} is the output resistance of the amplifier, C_{par} refers to the parasitic capacitance introduced by the pass element, and Z is the impedance seen at V_{out},

$$Z = R_x \| \frac{1 + sR_{esr} C_o}{sC_o} \| \frac{1}{sC_b} = \frac{R_x [1 + sR_{esr} C_o]}{s^2 R_x R_{esr} C_o C_b + s[R_x + R_{esr}] C_o + sR_x C_b + 1}, \qquad (2.2)$$

where C_o and R_{esr} are the capacitance and the ESR of the output capacitor, C_b represents the bypass capacitors, and R_x is the resistance seen from V_{out} back into the regulator defined as

$$R_x = R_{o-pass} \| (R_1 + R_2), \qquad (2.3)$$

where $R_{o\text{-}pass}$ is the output resistance of the pass element. The output resistance of the load (R_L) is commonly neglected because its value is considerably larger than R_x. If C_o is assumed to be reasonably larger than C_b (typical condition), then Z approximates to

$$Z \approx \frac{R_x [1 + sR_{esr} C_o]}{[1 + s(R_x + R_{esr}) C_o] \cdot [1 + s(R_x \| R_{esr}) C_b]}. \qquad (2.4)$$

It can be observed from equations (2.1) - (2.4) that the overall transfer function of the system consists of three poles and one zero, a potentially unstable system. For the

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majority of the load-current range, R_x simplifies to $R_{o\text{-}pass}$ since $R_1 + R_2$ is greater in magnitude (especially at high currents). The poles and the zero can thus be approximated to be the following:

$$P_1 \approx 1 / 2\pi R_{o\text{-}pass} C_o, \tag{2.5}$$

$$P_2 \approx 1 / 2\pi R_{esr} C_b, \tag{2.6}$$

$$P_3 \approx 1 / 2\pi R_{oa} C_{par}, \tag{2.7}$$

and

$$Z_1 \approx 1 / 2\pi R_{esr} C_o. \tag{2.8}$$

Figure 2.2 illustrates the typical frequency response of the system assuming that the output capacitor (C_o) is larger than the bypass capacitors (C_b). Figure 2.3 shows the simulation results of the circuit of Figure 2.1 using a macro-model for the amplifier, a PMOS device for the pass element, and a load-current of 70 mA. The simulation confirmed the overall behavior of the frequency response predicted by analysis with a dc open-loop gain of 43.6 dB, unity gain frequency of 3 MHz, and a phase margin of 29.5 °.

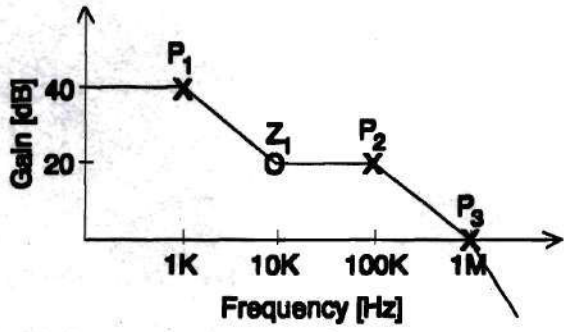


Figure 2.2. LDO frequency response under loading conditions.

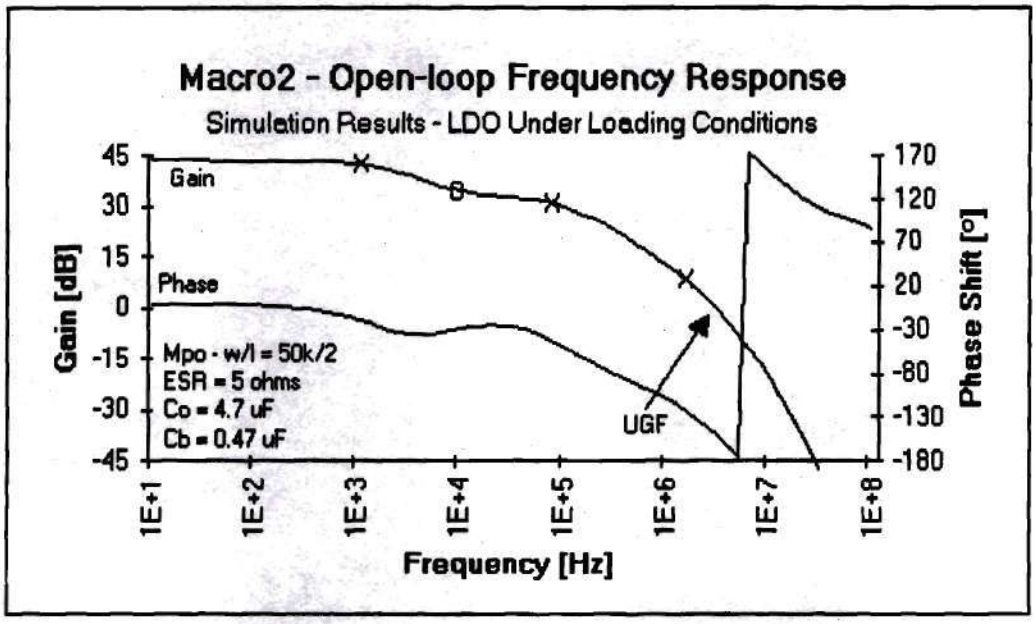


Figure 2.3. AC simulation results of an LDO under loading conditions.

Design Challenge

Worst-case Stability: The worst-case stability condition, given the set of elements shown in Figure 2.1, arises when the phase margin is at its lowest point, which occurs when the unity gain frequency is pushed out to higher frequencies where the parasitic poles reside. This happens when the load-current is at its peak value [23]. This is because the dominant pole (P_1) usually increases at a faster rate ($R_{o\text{-}pass}$ decreases linearly with increasing current, $1/\lambda I_o$ or V_a/I_o where λ is the channel length modulation parameter of MOS devices and V_a is the early voltage of bipolar transistors) than the gain of the system decreases ($g_{mp}R_{o\text{-}pass}$ decreases with the square root of the increasing current for an MOS device or stays constant for a bipolar transistor). The type and value of the output capacitor determine the location of P_1, P_2, and Z_1. Therefore, the

permissible range of values of ESR for a stable circuit is a function of load-current and circuit characteristics [5]. Simulations confirm the aforementioned tendencies.

Parasitic Pole Requirements: The parasitic poles of the system can be identified as P_3 and the internal poles of the error amplifier. These poles are required to be at high frequencies, at least greater than the unity gain frequency (UGF). The phase margin for the case where only one parasitic pole was at the vicinity of the UGF is approximately 45°. Ensuring that P_3 is at high frequencies is an especially difficult task to undertake in a low current environment. The pole is defined by the large parasitic capacitance (C_{par}) resulting from a large pass device (necessary trait for reasonable output current capabilities) and the output resistance of the amplifier (R_{oa}). The amplifier's output impedance is usually a function of the circuit topology and the bias current of its output stage. As a result, low quiescent current and frequency design issues have conflicting requirements that necessitate compromises.

Maximum Load Regulation Performance: Load regulation performance (output resistance of the regulator, R_o) is a function of the open-loop gain (A_{ol}) of the system and can be expressed as

$$R_o = \frac{\Delta V_{LDR}}{\Delta I_o} = \frac{R_{o-pass}}{1 + A_{ol}\beta}, \tag{2.9}$$

where ΔV_{LDR} is the output voltage variation arising from a load-current variation of ΔI_o, $R_{o\text{-}pass}$ is the output resistance of the pass device, and β is the feedback factor. Consequently, the regulator yields better load regulation performance as the open-loop gain increases [12]. However, the gain is limited by the closed-loop bandwidth of the system, equivalent to the open-loop unity gain frequency (UGF). The minimum UGF is

bounded by the response time required by the system during transient load-current variations, as discussed in the specifications section of chapter 1. Furthermore, the UGF is also bounded at the high frequency range by the parasitic poles of the system, i.e., the internal poles of the amplifier and pole P_3. If these parasitic poles are assumed to be located at higher frequencies than 1 MHz, then the gain at 1.0 kHz has to be less than approximately 35 - 45 dB depending on the location of Z_1 and P_2, as shown in Figures 2.2 and 2.3. In particular, the worst-case condition occurs when Z_1 is at low frequencies and P_2 is at high frequencies, which corresponds to the maximum value of ESR and the lowest bypass capacitance (C_b). Moreover, the pass element's associated input capacitance (error amplifier's load capacitance) is significantly large. This places a ceiling on the value of the amplifier's output resistance (R_{oa}). The pass element typically needs to be a large device to yield low drop-out voltages and high output current characteristics with limited voltage [current] drive in a low voltage and low power environment. Overall, load regulation is limited by the constrained open-loop gain of the system.

2.2 Transient Analysis

An important specification is the maximum allowable output voltage change for a full range transient load-current step. The application determines how low this value should be. For instance, a relatively relaxed specification for the peak output voltage variation can be tolerated if the regulator is used to provide power to digital circuits, which inherently have high noise margins [6]. However, this is not the case for many analog applications. Figure 2.4 shows the characteristic nature of the stimulus and the typical respective response for the typical system shown in Figure 2.1 [27].

Typical Response

The worst-case time required for the loop to respond (Δt_1, which is ideally the reciprocal of the closed-loop bandwidth) is specified by the maximum permissible output voltage variation (ΔV_{tr}), which is a function of the output capacitor (C_o), the electrical series resistance (ESR) of the output capacitor, the bypass capacitors (C_b), and the maximum load-current ($I_{Load\text{-}max}$),

$$\Delta V_{tr-max} \approx \frac{I_{Load-max}}{C_o + C_b} \Delta t_1 + \Delta V_{esr} \tag{2.10}$$

thus

$$\Delta t_1 \approx \frac{[C_o + C_b]}{I_{Load-max}} [\Delta V_{tr-max} - \Delta V_{esr}], \tag{2.11}$$

where ΔV_{esr} is the voltage variation resulting from the presence of the ESR (R_{esr}) of the output capacitor ($\Delta V_{esr} \propto R_{esr}$). The effects of ESR are reduced by the bypass capacitors

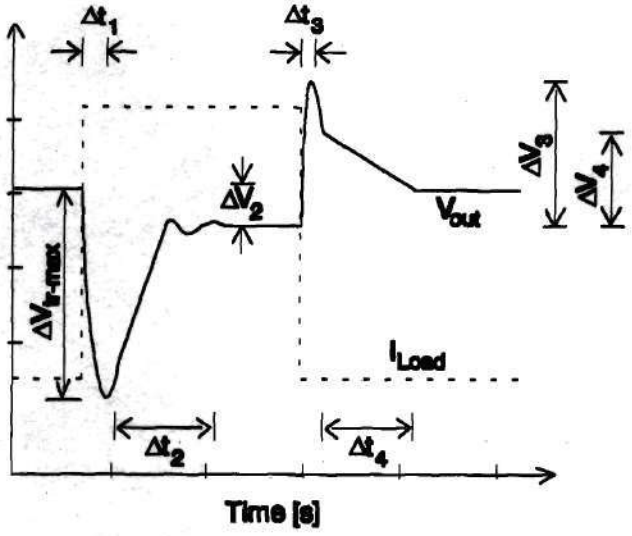


Figure 2.4. Typical LDO transient response to a load-current step.

(C_b), which are typically high frequency thereby exhibiting low ESR values. In typical implementations the time Δt_1 is not only a function of bandwidth but also defined by the internal slew-rate associated with the parasitic capacitance C_{par} of the pass element in Figure 2.1. The resulting time can be approximated to be

$$\Delta t_1 \approx \frac{1}{BW_{cl}} + t_{sr} = \frac{1}{BW_{cl}} + C_{par}\frac{\Delta V}{I_{sr}}, \tag{2.12}$$

where BW_{cl} is the closed-loop bandwidth of the system, t_{sr} is the slew-rate time associated with C_{par}, ΔV is the voltage variation at C_{par}, and I_{sr} is the slew-rate limited current. For instance, if BW_{cl} is 500 kHz, C_{par} is 200 pF, ΔV is 0.5 V, I_{sr} is 5 µA, C_o is 10 µF, R_{esr} is 0 Ω, and $I_{Load\text{-}max}$ is 100 mA, then the maximum output voltage variation is approximately 220 mV (equations (2.10) and (2.11)). If the slew-rate current is large enough, the reciprocal of the closed-loop bandwidth predominantly defines Δt_1. This would be at the cost of quiescent current flow, in other words, battery life. Once the slew-rate condition is terminated, the output voltage recovers and settles to its final value, ΔV_2 below the ideal value,

$$\Delta V_2 \approx R_{o-reg} I_{Load-max}, \tag{2.13}$$

where $R_{o\text{-}reg}$ is the closed-loop output resistance of the regulator. This is essentially the effect of load regulation performance on the output. The settling time (Δt_2) is dependent on the time required for the pass device to fully charge the load capacitors and the phase margin of the open-loop frequency response.

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The slew-rate limitation is usually unidirectional in nature thereby creating the asymmetrical response of Figure 2.4. The slew-rate condition typically occurs when the load-current steps from zero to full range. The direction for which this condition occurs is dependent on the configuration of the buffer and the output pass device. A typical topology is that of a class A buffer driving a PMOS pass element and associated parasitic capacitance (C_{par}). An example of this is illustrated in the simplified schematic of Figure 2.5 where the pass device is assumed to be a p-type transistor. A class A stage yields high current in one direction and limited dc current in the other, i.e., emitter [source] follower biased with a dc current source. More complex topologies, however, could be implemented for the buffer to realize high symmetrical slew-rate currents. The portion of

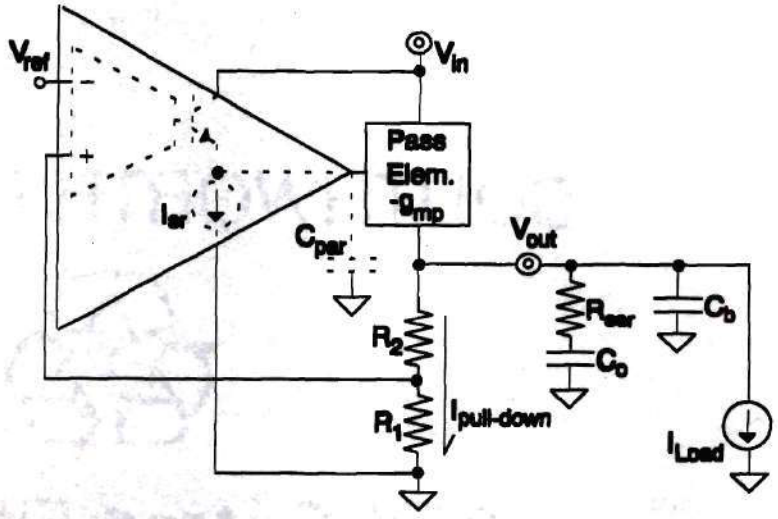


Figure 2.5. Simplified LDO schematic for the purpose of transient analysis.

the time response that does not experience internal slew-rate is dominated by the capacitors, the electrical series resistance (ESR) of the output capacitor, the bandwidth of the system, and the low pull-down current capability of the LDO's output ($I_{pull-down}$ in Figure 2.5). At first, the output voltage variation peaks at ΔV_3, whose magnitude is

defined by the voltage charged on the capacitors and the voltage generated across the ESR of the output capacitor. This results because the momentary current supplied by the power device ($I_{Load\text{-}max}$ until the circuit reacts to shut it off) flows to the output capacitor C_o and the bypass capacitors (the current is no longer flowing to the load). Consequently, the capacitors charge up and a temporary voltage drop is created across R_{esr}. This transient voltage can be approximtely described by

$$\Delta V_3 \approx \frac{I_{Load-max}}{C_o+C_b}\Delta t_3 + \Delta V_{esr} \approx \frac{I_{Load-max}}{C_o+C_b}\cdot\frac{1}{BW_{cl}} + \Delta V_{esr}, \qquad (2.14)$$

where the terminology of Figures 2.4 and 2.5 is adopted. When the output transistor is finally shut off (after Δt_3) the variation settles down to ΔV_4, the voltage charged on the capacitors ($\Delta V_4 \approx \Delta V_3 - \Delta V_{esr}$). At this point, the output voltage takes time Δt_4 to discharge to its final ideal value,

$$\Delta t_4 \approx \frac{C_o+C_b}{I_{pull-down}}\Delta V_4 = \frac{[C_o+C_b]R_1}{V_{ref}}\Delta V_4. \qquad (2.15)$$

Figure 2.6 illustrates the simulation results of an LDO transient response analysis. The circuit utilized employs the basic topology shown in Figure 2.5 using a macro-model for the amplifier and a PMOS pass device. The addition of high frequency bypass capacitors (capacitors with low ESR) reduce the peaks of the transient response, $\Delta V_{tr\text{-}max}$ and ΔV_3. This results because the current supplied by the output capacitor (C_o) during transient conditions is decreased as C_b is increased thereby exhibiting a lower voltage drop across

R_{esr}. The remaining current is furnished by the bypass capacitors, which typically have negligible ESR voltage drops.

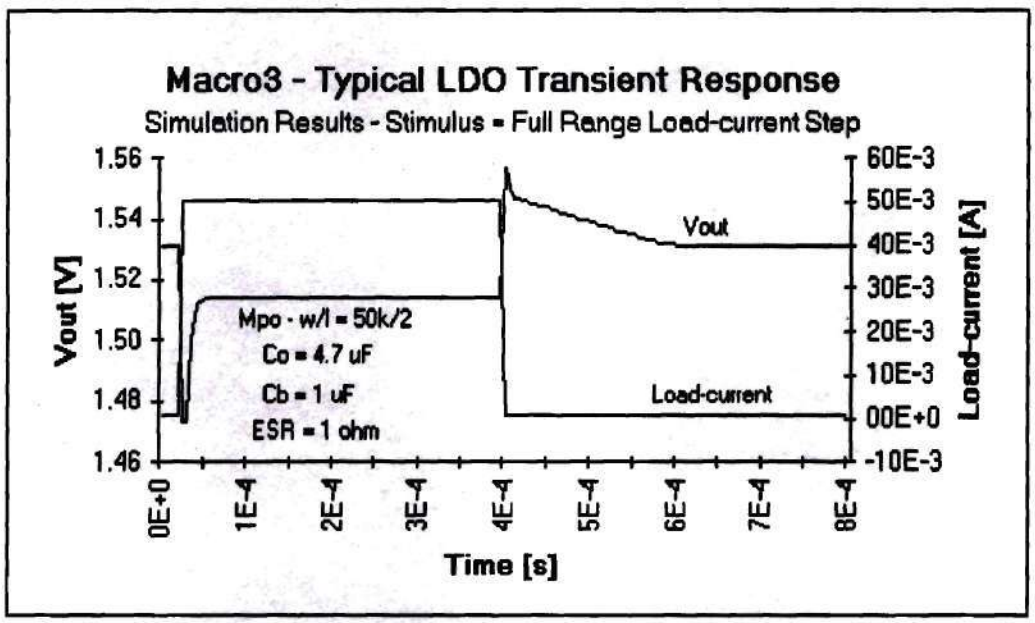


Figure 2.6. Simulated LDO transient response of a circuit similar to that of Figure 2.5.

Design Challenge

The worst-case output voltage variation is a function of the bandwidth and the slew-rate limit of the circuit. However, bandwidth and slew-rate limit are highly dependent on quiescent current flow. As bandwidth is demanded to increase, the parasitic poles are required to increase accordingly thereby necessitating more current flow to decrease associated impedances. Consequently, the error amplifier's quiescent current must necessarily increase to yield faster response times. Moreover, increasing slew-rate performance requires an increase in bias current on the circuit driving the slew-rate limited node. This affects the design of the output stage of the amplifier. As a result, the overall minimum quiescent current flow is limited by the maximum allowable output voltage variation arising from full range load-current steps.

2.3 Pass Device Design Issues

Designing in a low voltage and low current environment provides difficult challenges that contradict performance and stability [23]. The first aspect that is affected is the series pass element of the low drop-out regulator. It must provide large amounts of current while displaying low drop-out characteristics. Drop-out voltage is governed by the on resistance of the pass transistor ($V_{drop\text{-}out} = I_{Load}R_{on}$), which is inversely proportional to the physical size of the device. Drop-out voltage is further increased by series parasitic resistance inherent in the layout, such as the pass device's source [emitter] and drain [collector] contacts, metal traces, and diffusion links. As a result, the size of the transistor must be large under low voltage conditions, which translates to a large load capacitance for the error amplifier. A large device is further demanded because voltage drive is reduced as a result of decreased input voltages. This, in turn, causes the parasitic pole P_3 to move to lower frequencies effectively deteriorating phase margin and compromising the stability of the system. Moreover, the resulting increase in load capacitance for the feedback amplifier requires an increase in quiescent current flow. This is necessary to charge and discharge the capacitance quickly enough during slew-rate conditions, as discussed in the transient analysis section. For the case of MOS pass devices, sub-threshold currents can become appreciably large as the aspect ratio is increased. In other words, the transistor can be difficult to shut off thereby creating problems at zero-load conditions. Finally, the physical design of the large device must also take into account line resistance and capacitance, current density per line, heat distribution, and parasitic devices inherent to the layout. Thermal symmetry as well as equal current density distribution must be maintained for reliability and best performance. Overall, the size of the pass device must be large for increased current capabilities but

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restrained by stability and slew-rate requirements in a low quiescent current flow and low voltage environment.

The problem of handling large output currents or reducing the "on" resistance of MOS pass devices is sometimes cost efficiently resolved by using a dc-dc converter in addition to the LDO. The purpose of the switching regulator is to bring down the voltage thereby reducing the operating voltages of the LDO. As a result, devices with lower breakdown voltages can be used. In other words, the MOS pass device can reduce its channel length without posing any threat to the reliability of the circuit. Thus, larger aspect ratios per unit area and higher output currents are achieved. The additional cost of the switching regulator is offset by the potential cost of increasing the size of the pass device, increased area overhead. The point where this technique becomes valuable is dependent on the process technology, the application, and the associated specifications.

2.4 Amplifier Design Issues

The specifications of the amplifier that are relevant to the regulator as inferred from the previous discussions are: output impedance, gain, bandwidth, output slew-rate current, output voltage swing, and quiescent current. The output impedance must be low enough to place the parasitic pole P_3 (equation (2.7)) at a frequency greater than the unity gain frequency, thus maintaining stability. The requirement is stringent because of the large value of the load capacitance introduced by the vast pass device. This requires the use of a buffer to isolate the high output resistance of the gain stage (R_{og}) from the high load capacitance (C_{par}), as illustrated in Figure 2.7.

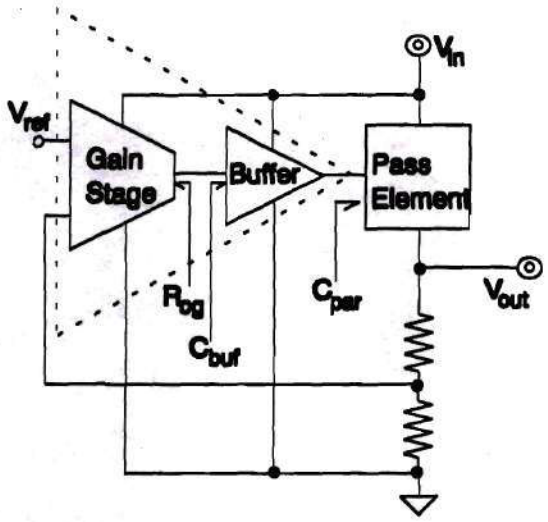


Figure 2.7. LDO buffered architecture.

Load regulation performance is enhanced as the open-loop gain of the system is increased, equation (2.9). However, the gain is limited by the unity gain frequency, as discussed in the ac analysis section. Therefore, caution must be exercised in designing the gain-bandwidth product (GBW) of the amplifier. This is dependent on the location of the output poles and the zero of the system, namely, P_1, P_2, and Z_1 (equations (2.5), (2.6), and (2.8)). It is further noted that the location of the dominant pole (P_1) varies with load-current, i.e., $R_{o\text{-}pass} \propto 1/I_{Load}$ for all pass elements except for the NMOS source follower, where $R_{o\text{-}NMOS} \propto 1/\sqrt{I_{Load}}$.

The topology and the biasing current of the buffer is designed according to the frequency and the transient response requirements of the system. Transient specifications tend to dominate the bias current demands of the buffer. In particular, the slew-rate current available to the output of the buffer partially determines the magnitude of the output voltage variation during transient load-current steps, as discussed in the transient analysis. The choice in topology also reflects the driving requirements of the pass device. For instance, a PMOS pass device requires a high negative voltage swing to yield

maximum gate drive and thus produce large output currents and low drop-out voltages. On the other hand, a sufficiently high positive swing is needed to shut off the device to the point where sub-threshold currents do not become a problem. A simple implementation of the buffer could be a source follower using a natural NMOS transistor, which is a non-threshold adjusted device exhibiting threshold voltages close to zero [3]. These devices are available at the possible cost of one extra mask in the process flow. The product of the input capacitance of the buffer (C_{buf}) and the output resistance of the gain stage (R_{og}) must be kept low to yield an internal frequency pole that is greater than the unity gain frequency of the system. Therefore, the ohmic resistance and line capacitance of the trace path in the layout between the output of the gain stage and the input of the buffer must be minimized.

The overall design of the amplifier must be kept as simple as the specifications will allow to necessitate low quiescent current flow. The limiting factors for low quiescent current are the amplifier's bandwidth and slew-rate requirements. A tradeoff between performance and power dissipation is therefore necessary. In a low voltage environment, such as the case for battery operated applications, the number of devices connected from the input voltage to ground must also be kept low [10]. The ultimate limit is one diode connected device and one saturation voltage drop, V_{be} [V_{gs}] + $V_{ec\text{-}sat}$ [$V_{sd\text{-}sat}$]. More flexibility may be allowed if the limiting factor lies elsewhere in the system, i.e., pass element's voltage drive requirements.

2.5 Reference Design Issues

The main issue involved in the design of the reference is accuracy and low voltage operation, input and output voltages included. Bandgap references are the most appropriate for low voltage. They are accurate circuits with typical output voltages of

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roughly 1.2 V. The respective input voltage limitation is roughly 1.4 - 1.5 V (a V_{sat} above the reference). Power supply rejection ratio is another important factor, especially in mixed-signal designs where noise is coupled from high speed digital circuits [13]. As a result, the noise floor must be kept low to maximize dynamic range. This translates to the design of low noise circuits. Typically, 1/f noise tends to be important in prevailing regulator designs [28].

The difficulties in designing a precise low voltage bandgap reference arise from maintaining accuracy at lower power supply voltages while keeping quiescent current at a minimum. The accuracy of references is determined by line regulation and temperature drift performance. Load regulation is sometimes included in the accuracy but is more appropriately specified for voltage regulators. Accuracy performance is sometimes limited by the effects of the package on the output voltage. The causes of this phenomenon are the physical stresses induced on the die by the package. As a result, the physical location of the reference with respect to the overall chip is important. Package induced drifts can be significant especially if trimming is performed at the wafer level. The performance can be improved if trimming is done at the post-package level. Lower dynamic range, a consequence of low voltage operation, demands that reference voltages be more accurate; as a result, bandgaps require curvature correcting schemes. Lower dynamic range results from reductions in power supply voltage, which decreases signal-to-noise ratio in an environment where the noise floor typically remains constant [10].

2.6 Summary

The electrical design considerations and implications of the system have been addressed in this chapter. The frequency and transient response have been analyzed when the system is under typical loading conditions. Their effects on design have been identified

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to fully understand the basic performance limitations of the regulator. The consequential requirements of the major circuit blocks were then discussed. This included comments of the parasitic effects of each block on the overall performance. The chapter, in essence, established a conceptual background for evaluating the prevailing circuit topologies.

CHAPTER III

REGULATOR TOPOLOGIES

The circuit architecture of a basic low drop-out regulator can take various forms. The design criterion for each implementation is determined by the specific application as well as by the process technology where the circuit is to be fabricated. However, they all have to function under similar loading conditions, namely, a load-current, an output capacitor and its associated electrical series resistance (ESR), and some bypass capacitors. Several of the prevailing design approaches are scrutinized in this chapter. Each structure is evaluated for its current efficiency and overall performance at low voltage. Moreover, some performance enhancing techniques are also illustrated and evaluated.

3.1 CMOS Topology

Figure 3.1 shows the circuit implementation of a CMOS low drop-out regulator [23]. The feedback amplifier has a single dominant pole and is located at its output, the gate of the output device Mpo (node "A"). The error amplifier is a single, class AB gain stage with a PMOS differential input pair. The class AB gain stage yields a rail-to-rail output voltage swing. Consequently, the power PMOS transistor can be shut off completely as well as be maximally driven to a gate drive approximately equal to the input voltage, $0 \leq V_{sg} \leq V_{in}$. The input voltage ($V_{in}$) for this circuit is limited by the common mode range characteristics of the same,

$$V_{in} \geq V_{ref} + V_{sg} + V_{sd}, \tag{3.1}$$

where V_{ref} is the reference voltage. For the case of an n-type input pair realization, the reference voltage is limited to be greater than or equal to $V_{gs} + V_{ds}$ while the input voltage of the circuit is limited to be greater than $V_{sg} + 2V_{ds}$. Furthermore, the input voltage requirement of the reference ($V_{in\text{-}ref}$) in the latter case would be at least one V_{sd} above the reference voltage, in other words,

$$V_{in-ref} \geq V_{sd} + V_{ref} \geq V_{sd} + V_{gs} + V_{ds} \approx V_{gs} + 2V_{ds}. \tag{3.2}$$

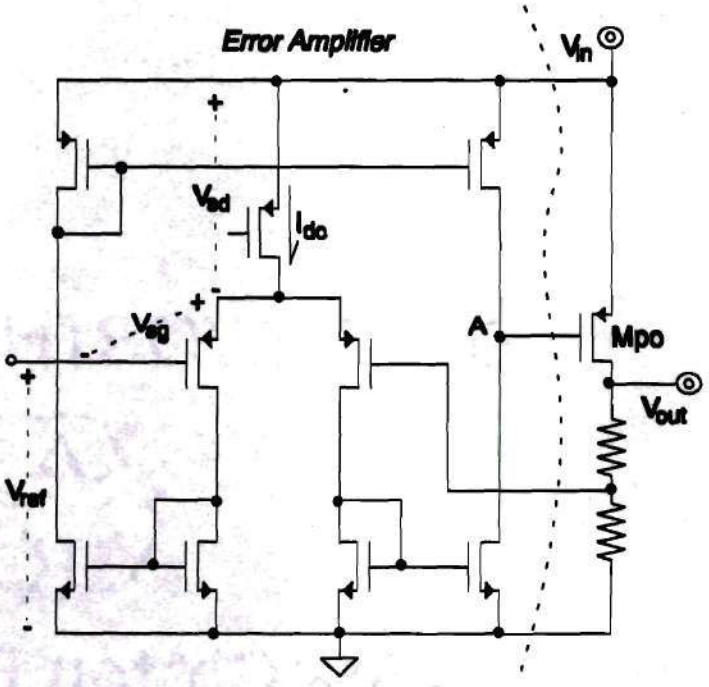


Figure 3.1. CMOS low drop-out regulator topology.

As a result, the input voltage restriction using an NMOS differential pair is dominated by the requirements of the reference and not the regulating loop.

The frequency response of this circuit is typical to most low drop-out regulator topologies. Under loading conditions, there are three poles and one zero, namely, the pole associated with the output capacitor, the pole introduced by the bypass capacitors, the parasitic pole at the output of the error amplifier, and the zero associated with the ESR of the output capacitor. The parasitic pole (P_3 from previous analysis) is the dominant pole of the feedback amplifier. The design reaps the benefits of not having any other significant poles in the amplifier. All the non-dominant poles of the amplifier are at low impedance nodes and therefore reside at high frequencies. Such architecture, however, still necessitates careful design because the dominant pole of the amplifier can easily be at low frequencies. This results from the characteristic high input capacitance of Mpo and the high output impedance of the amplifier. The capacitance can be in the order of 100s of pico farads since the size of Mpo is significantly large, which is a necessary trait for providing high output currents.

The circuit is not inherently current efficient. The bias current of the amplifier is dependent on the slew-rate performance of the same. For instance, the system may require a time response of 2 µs with a voltage swing at node "A" of 800 mV (gate voltage swing of Mpo) to react to a maximum load-current step change. Hence, the amplifier must charge and discharge node "A" with roughly 40 to 160 µA, assuming a gate capacitance of 100 to 400 pF. This places a significant lower limit on the bias current flow of the amplifier during zero load-current conditions, in other words, limit on current efficiency and battery life.

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3.2 Buffered Architecture

Figure 3.2 illustrates a topology that isolates the dominant pole of the amplifier from the input terminal of the power pass device. The implementation is intended for a series Darlington PNP pass transistor [29]. The basic topology is formed by a simple single stage amplifier cascaded onto a buffer driving the pass element. During low load-current conditions, the base current of the Darlington PNP structure is low. As a result, the bias current flows mostly through Mp1 and the resistor between the gate and the source of Mn1. At this point, the gate voltage of Mn1 is not high enough to significantly cause Mn2 to conduct current. During high load-current conditions, however, the base current of the Darlington becomes large. As a result, the voltage at the gate of Mn1 becomes large enough to notably turn Mn2 on, whose drain current is a nonlinear mirror ratio of Mn1. Hence, the current sinking capabilities of the buffer are increased as the load-current increases. The overall low voltage limit of the circuit is dominated by the buffer,

$$V_{in} \geq 2V_{sd} + 2V_r + V_{gs}. \qquad (3.3)$$

This presents a possible source of concern when single alkaline battery cells (0.9 to 1.5 V) are considered. Thus, the design is not optimum for low voltage.

On the other hand, the circuit benefits from having a good frequency response. This arises as a result of isolating the highly capacitive node (the pass device's input) from the highly resistive gain stage output (the dominant pole of the amplifier). This is done by the buffer, which provides a low impedance for the highly capacitive node and a low capacitance for the highly resistive node. Therefore, the poles at the two nodes can be at higher frequencies than the single pole of the unbuffered version, a sample of which is

embodied in the circuit of Figure 3.1. Consequently, the overall frequency response of the system exhibits higher phase margin and potentially higher bandwidth. In other words, the concept of buffering allows for faster response times, which translate to lower output voltage variations and higher accuracy.

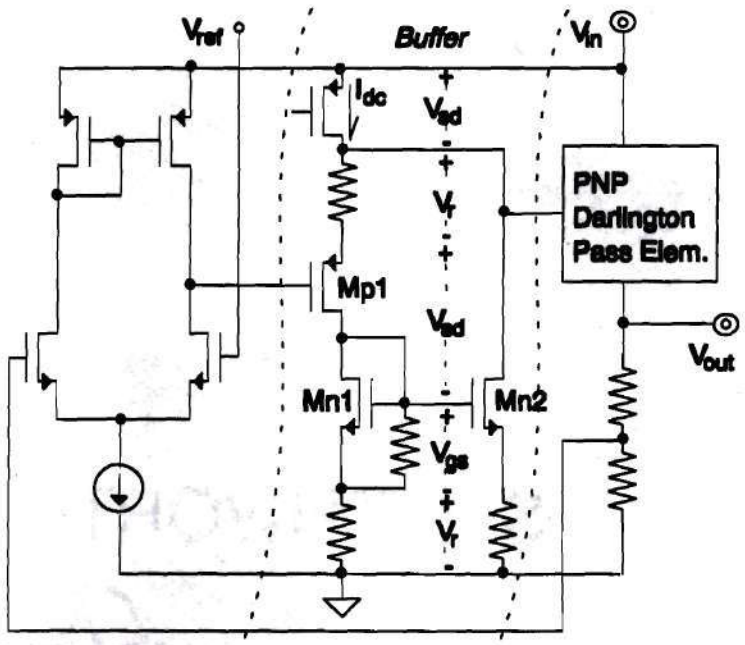


Figure 3.2. Buffered low drop-out regulator architecture.

3.3 All-in-one Approach

The reference and amplifier can be integrated into one circuit as shown in Figure 3.3, which is a modified version of the original circuit of [22] and whose concept is also used by some Analog Devices' parts [4]. The main idea, like before, revolves around defining the regulated voltage at the output and feeding back an error signal to control the pass device. However, instead of using a differential amplifier and a separate reference circuit, a first order bandgap is realized within the feedback circuit itself. The bandgap, defined at the output, feeds back an error signal through a single common emitter gain

stage back to the pass device. In essence, a voltage reference circuit with good load regulation characteristics is realized. Transistor Qn1 and resistor R_1 define the bandgap reference where the voltage across R_1 is proportional-to-absolute temperature (PTAT). Since the regulated output is a first order bandgap, the output voltage range does not have any flexibility in terms of magnitude adjustment and the minimum input voltage is defined by a bandgap and one saturation voltage, V_{bg} and V_{sd},

$$V_{in} \geq V_{bg} + V_{sd} \approx 1.4 - 1.5 \text{ V}. \tag{3.4}$$

This is a problem for single, low voltage battery cells whose voltages range from 0.9 to 1.5 V. The overall circuit can also be realized in a CMOS environment where the bandgap voltage can be generated by either using the bipolar parasitic transistor innate to the process or by using the temperature dependencies of different MOS devices [30, 31].

The frequency response of the circuit in Figure 3.3 is similar to that of Figure 3.1, which is characteristic to a single pole error amplifier. As a result, caution must be

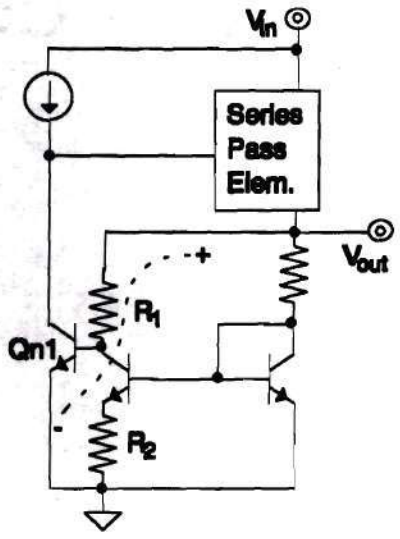


Figure 3.3. All-in-one regulator approach.

exercised to prevent this pole, parasitic pole of the system, from dropping to lower frequencies. This is done to yield good system bandwidth and phase margin. The topology enjoys the benefits of high current efficiency and low active chip area. This arises from a low component count. As a result, the number of current sensitive transistor paths to ground is low thereby exhibiting low quiescent current flow (high current efficiency) and relatively long battery life.

Another class of linear regulators are those that are internally compensated. These typically use some form of miller compensation to make an internal node the dominant pole of the system, such as the input node of the pass device (gate or base). Consequently, the pole associated with the output capacitor has stringent requirements, i.e., frequency location needs to exceed a specified value. Thus, the output capacitors for these regulators are smaller than externally compensated versions. The maximum specified output current is therefore lower for internally compensated linear regulators. This is the consequence of larger transient output voltage variations resulting from smaller output capacitors ($\Delta V_{tr\text{-}max} \propto 1 / C_o$). In summary, these regulators inherently yield lower output currents while exhibiting different frequency response characteristics and requirements.

Table 3.1 shows a qualitative comparison of the design approaches discussed. Internally compensated regulators are excluded because of their output current limitations. The lowest minimum input voltage is achieved by the CMOS topology. The buffered architecture offers the best frequency and transient response. The all-in-one approach achieves the best current efficiency and lowest active area. Unfortunately, the latter approach suffers from stringent input and output voltage range problems. Consequently, a combination of the former two designs can yield the best performance at low voltage, i.e.,

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circuit architecture similar in nature to that of the CMOS topology with a buffer between the amplifier and the pass device.

Table 3.1. Qualitative evaluation of regulator topologies.

Parameter	CMOS	Buffered	All-in-one
V_{in-min}	Good	Medium	Medium
Current Efficiency	Medium	Medium	Good
System Bandwidth	Medium	Good	Medium
Active Area	Medium	Medium	Good

3.4 System Enhancements

The circuit architecture of the regulators discussed in the previous section can be complemented with some system level performance enhancing techniques. Some of the attributes that can be ameliorated are maximum output current, response time, and output voltage range. However, the benefits arise at some cost, such as active area and/or current efficiency. Some of these techniques are introduced and evaluated for their performance and applicability in the portable electronics market, which demands low voltage and high current efficiency.

Mixed-mode Technique

The benefits of analog and digital operation can be combined to yield improved performance. Figure 3.4 illustrates one sample topology, which is a conceptual version of [32]. The analog section operates like most standard regulator topologies. The additional digital loop uses a feedback amplifier, similar to that of the analog section, to drive a digital inverter. Consequently, Mpod in Figure 3.4 sources a digital current that is

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dependent on the output voltage, a sense voltage that reflects load-current behavior. During low load-current conditions, the analog section sources all of the current. During high load-current conditions, however, the digital section sources a constant current that is lower in magnitude than the load-current. At this point, the analog feedback loop regulates the output voltage around the digital current through current I_a ($I_a = I_{Load} - I_d$). If the analog current component becomes zero and the digital current exceeds the load-current, then Mpod is shut off by the digital feedback path. As a result, the operation goes back to the low load-current state where the analog section is the sole supplier of output current.

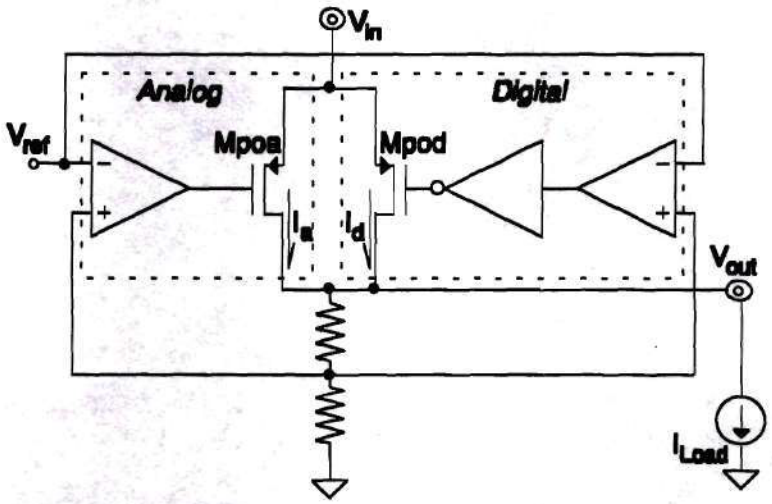


Figure 3.4. Mixed-mode regulator.

The advantage of the digital section is that it consumes less power (less quiescent current). The feedback amplifier in the digital section only drives the input capacitance of one inverter and not the large output PMOS transistor (Mpod). Thus, the slew-rate current performance of the amplifier is relaxed. Furthermore, the size of the output device in the analog section (Mpoa) is not as large as it would be had it been the only power

element. Consequently, the performance requirements of the amplifier in the analog feedback are relaxed. Moreover, the response time versus the quiescent current tradeoff is positively offset by the fast parallel digital signal path. However, caution must be exercised in designing the output voltage swing of the inverter for varying input voltages. If a simple inverter is used to work properly at 2 V, then the digital section would deliver an excessive amount of current at an input voltage of 10 V, corresponding to a gate drive increase from 2 to 10 V. This gate drive problem can be handled by designing the inverter as shown in Figure 3.5, which adds a drain-grounded PMOS device in series with the pull down transistor of an inverter as implemented by [32]. Unfortunately, the inverter realization is detrimental for operation at input voltages of 0.9 to 1.5 V because of voltage headroom problems, consequence of multiple series diode connected devices.

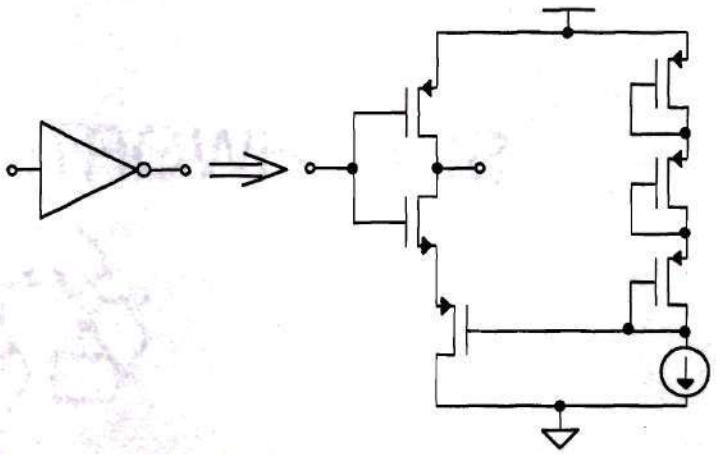


Figure 3.5. Digital inverter for the mixed-mode regulator.

Multi-pass Device Approach

A similar way of relaxing the output current requirement of a regulator is by adding another pass device that delivers a mirror ratio of the main output PMOS transistor. Figure 3.6 illustrates one such topology realized by [33]. The current through

the main output PMOS device (Mpo) is sensed and a mirror ratio is supplied by the additional pass device (Mpx). The mirror ratio is controlled by the resistor ratio of R_1 and R_2, one-tenth for Figure 3.6. The current control is accomplished by the PNP transistors and the load resistor R_{L1}. The voltage across R_2 is forced onto R_1 and the gate voltage of Mpx is controlled via a negative feedback path from the source to the gate of the same, $V_{gate}/V_{source} \approx g_{mpnp}R_{L1}$. The pole associated with the gate of Mpx must be at high enough frequencies such that the overall system response is not degraded, i.e., the pole requirements are similar to those of a single pole amplifier in a standard regulator topology.

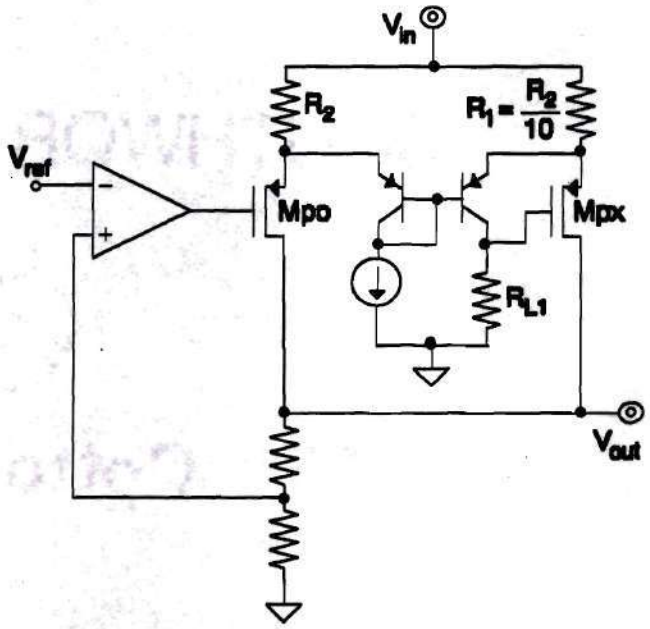


Figure 3.6. Multi-path device regulator.

The demands on the error amplifier in the main feedback are relaxed because the size of the output PMOS transistor is reduced. However, the drop-out voltage is increased by the series resistance of R_1 and R_2. Thus, these resistors need to have low

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values to mitigate their negative effects on drop-out voltage. Furthermore, care must be taken in designing the current flowing through the two PNP devices so that current efficiency is not degraded enough to unwarrant the use of the technique. The load resistor R_{L1} could be replaced by a current sink; however, the associated pole tends to go towards lower frequencies and possibly compromise stability when this is done.

Widely Adjustable Structure

The output voltage range of typical low drop-out regulator structures goes from the reference voltage up to approximately 200 mV below the input voltage. Figure 3.7 shows an architecture that extends the output voltage range down to roughly zero volts [34]. This is done by adjusting the voltage at node "A", which is typically connected to ground. As a result, the current flowing through the feedback resistors (I_r) can be manipulated to the point of reversing its direction. Consequently, the output voltage can be defined to be below the reference voltage. Amplifier A_1 is a buffer with a gain slightly greater than one. The second amplifier (A_2) forces a fraction of the reference voltage on node "A". When this fraction is greater than one, then I_r flows towards the output and the output voltage becomes less than the reference voltage,

$$V_{out} = \frac{V_A - V_{ref}}{R_2} R_1 \approx \frac{(k-1)V_{ref}}{R_2} R_1, \qquad (3.5)$$

where k is a constant defined by the gain of A_1, the gain of A_2, and the resistor tap of the input of A_2, i.e., $k \approx 0$ - 1.05 in Figure 3.7. A requirement for this structure is that the load-current be greater than or equal to I_r. This can be guaranteed by defining I_r to be small and by placing a constant current sink at the output that is greater than or equal to I_r, as illustrated by the dotted lines in Figure 3.7.