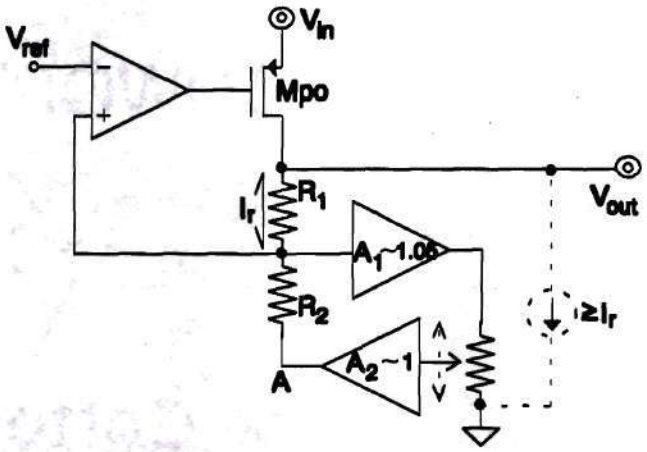


Figure 3.7. Widely adjustable low drop-out regulator structure.

The main disadvantage of the topology lies in current efficiency, in other words, quiescent current flow. The realization of two additional amplifiers comes at the cost of complexity, quiescent current, and active area. The technique is only useful when the application specifically warrants it. Most of the time, integrated circuit applications do not require the characteristics offered by this technique. In low voltage applications, however, this may be necessary if the input and the output voltage of the reference are greater than the input voltage of the regulator. This is a seldom occurrence that may arise during system level design when most of the circuit blocks are realized discretely. At this point, the whole exercise may be circumvented by integrating the reference onto the regulator chip if enough voltage headroom and chip area exist. This comes at the expense of quiescent current and possible design time.

3.5 Summary

This chapter has illustrated some of the prevailing circuit topologies for low drop-out regulators. They embody the basic concepts surrounding LDO design in CMOS,

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bipolar, and biCMOS process technologies. The circuits were described and evaluated within the context of low voltage and low quiescent current flow, which are the characteristics demanded by the growing market demand for battery operated products. Moreover, circuit techniques used to enhance particular performance specifications were also described and evaluated. All these approaches constitute the necessary basis for developing new circuit techniques that enable practical and suitable designs for a battery powered environment.

CHAPTER IV

PERFORMANCE ENHANCEMENTS

The general performance of low drop-out regulators deteriorates as input voltages decrease. This has an intrinsic impact on portable, low voltage, and battery operated equipment. Consequently, circuit designs benefit from extensive exploitation of available process technologies. In a battery operated environment, the aspects that need special attention are quiescent current flow, maximum output current capabilities, and regulation performance [35]. Low quiescent current is necessary to maximize current efficiency, which is important during low load-current conditions for prolonged battery life. As the input voltage is decreased, the output current capability of the pass device tends to diminish as a result of voltage headroom degradation. Although these issues are especially important in battery operated products, they are also prevalent in designs for higher input voltages. Consequently, enhancing performance without incurring significant costs in quiescent current or voltage headroom benefit the overall design of LDOs.

4.1 Current Efficiency

Motivation

Current efficiency is an important characteristic of battery powered products. It is defined as the ratio of the load-current and the total battery current drain, which is comprised of the load-current (I_{Load}) and the quiescent current (I_q) of the regulator,

$$\text{Efficiency}_{\text{current}} = \frac{I_{Load}}{I_{Load} + I_q}. \qquad (4.1)$$

Current efficiency determines how much the lifetime of the battery is degraded by the mere existence of the regulator. Battery life is restricted by the total battery current drain. During conditions where load-current is much greater than quiescent current, operation life is essentially determined by the load-current, which is an inevitable characteristic of linear regulators. On the other hand, the effects of quiescent current on battery life are most prevalent during low load-current conditions when current efficiency is low. This condition of low load-currents is the common operating mode of many applications. As a result, current efficiency plays a pivotal role in designing battery powered supply circuits. The two performance specifications that predominantly limit the current efficiency of low drop-out regulators are maximum load-current and transient output voltage variation. They typically require more quiescent current flow for increased performance.

Challenge

Output current and input voltage ranges directly affect the characteristics of the pass element in the regulator, which define the quiescent current requirements of the error amplifier. As the maximum load-current specification increases, the size of the pass device necessarily increases. Consequently, the error amplifier's load capacitance increases. This affects the circuit's frequency performance by reducing the value of the parasitic pole present at the output of the amplifier, pole P_3 from the discussion in chapter 2. Therefore, phase-margin degrades and stability is compromised unless the output impedance of the amplifier is reduced accordingly. As a result, more quiescent current flow in the buffer stage of the amplifier is required, be it a voltage follower or a more complicated circuit

architecture. In a similar manner, low input voltages require that MOS pass device structures increase in size and thus yield the same negative effects on frequency response and quiescent current flow as just described. This is because the gate drive decreases as the input voltages decrease thereby necessitating larger MOS pass elements to drive high output currents.

Further limits to low quiescent current arise from the transient requirements of the regulator, namely, the permissible output voltage variation in response to a maximum load-current step swing. The output voltage variation is determined by the response time of the circuit, the specified load-current, and the output capacitor, as discussed in chapter 2. The worst response time corresponds to the maximum output voltage variation. This time limitation is defined by the closed-loop bandwidth (BW_{cl}) and the slew-rate current (I_{sr}) capabilities of the system. These characteristic requirements become more difficult to realize as the size of the parasitic capacitor (C_{par}) at the output of the feedback amplifier increases, which results from low voltage operation and/or increased output current specifications. As a result, the quiescent current flow of the amplifier's gain stage is limited by a bandwidth minimum while the quiescent current flow of the amplifier's buffer stage is limited by the slew-rate current required to drive C_{par}.

Slew-rate Dependent Boost

The problem of handling an instantaneous load-current stimulus is translated to the slew-rate requirement of driving the pass device. This can be easily resolved by allowing higher quiescent current flow. However, this is not conducive toward the low quiescent current design goal. On the other hand, a cost efficient addendum in the form of slew-rate dependent bypass switches can be used to enhance the transient capabilities of the system. Figure 4.1 (a) shows one such slew-rate dependent boost circuit. In this case, two normally off switches are added around a unity gain buffer constituting the output stage of

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the amplifier. The switches conduct significant current only when the amplifier is slewing to the point where a voltage difference across the unity gain buffer develops to be large enough to turn either of the MOS devices on.

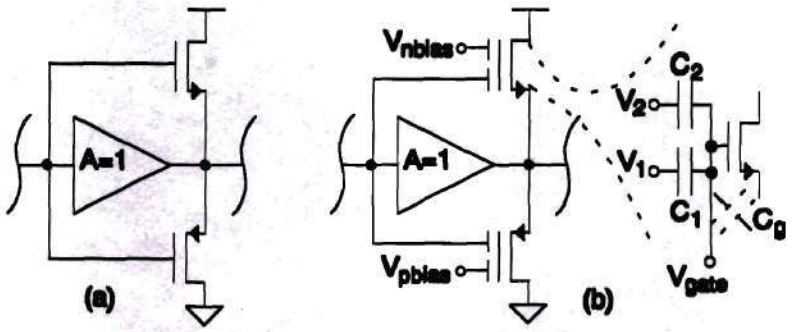


Figure 4.1. Slew-rate dependent boost circuit.

The ability to aid during slew-rate conditions, however, is limited by the large threshold voltage of the switches. Improved performance can be achieved if the threshold voltage (V_{th}) of these bypass transistors were lower, i.e., 0.25 - 0.5 V. This can be accomplished by forward biasing the source to bulk voltage (V_{sb}), for the case of a PMOS transistor, as dictated by the well known threshold voltage equation,

$$|V_{th}| = |V_{to}| + \gamma\left[\sqrt{2|\phi_f| - V_{sb}} - \sqrt{2|\phi_f|}\right], \qquad (4.2)$$

where $|V_{to}|$ is $|V_{th}|$ at $V_{sb} = 0$, γ is the body bias coefficient, and $|\phi_f|$ is the bulk Fermi potential [36, 37]. The complement of this can be done for the NMOS transistor case. The access to the bulk terminal of the NMOS device, however, is dependent on process technology. For instance, access cannot be obtained in a vanilla CMOS process because the bulk is the substrate of the chip. However, the opposite is true for twin well and biCMOS processes where access can be obtained by isolating the NMOS with a p-well, p-

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base diffusion, or a p-epi region insulated by a ring of deep n+ collector plug and a buried layer.

Another method of adjusting the threshold voltage is through the use of a double gate MOS device [38]. Figure 4.1 (b) shows the resulting scheme. The voltage at the floating gate (V_g), assuming that the source is grounded, is dictated by

$$V_g = \frac{V_1 C_1}{C_{total}} + \frac{V_2 C_2}{C_{total}}, \tag{4.3}$$

thus

$$V_{th1} = \frac{V_{th} C_{total}}{C_1} - \frac{V_2 C_2}{C_1}, \tag{4.4}$$

where V_1 and V_2 are the voltages at terminals one and two, C_{total} is $C_1 + C_2 + C_g$, V_{th1} is the effective threshold voltage of terminal one, and V_{th} is the threshold voltage seen at the floating gate. As a result, proper capacitor ratios can yield lower effective threshold voltages, i.e., if $C_1 = C_2 = 8C_g$, $V_2 = 1.0$ V, and $V_{th} = 0.7$ V then $V_{th1} = 0.49$ V. The disadvantage of this technique lies in generating the necessary bias voltages, V_{nbias} and V_{pbias} in Figure 4.1 (b), for maintaining the same effective threshold voltage over specified input voltage and load-current ranges. This is because the voltage at the source of the MOS bypass transistors is sensitive to the gate drive of the p-type pass device of the linear regulator, which is dependent on input voltage and output current.

Current Efficient Buffer

Another topology that achieves good current efficiency performance is illustrated in Figure 4.2. The operation is based on sensing the output current of the regulator and feeding back a ratio of the same to the slew-rate limited node of the circuit. Transistor

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Mps sources a fraction of the current flowing through the output transistor Mpo. During low load-current conditions, the current fed back (I_{boost}) is negligible thereby yielding high overall current efficiency and not aggravating battery life. Consequently, the current through the emitter follower is simply I_{bias} when load-current is low. During high load-current conditions, the current through the emitter follower is increased by I_{boost}, which is no longer negligible. The resulting increase in quiescent current flow has an insignificant impact on current efficiency because the load-current is, at this point, much greater in magnitude. However, the increase in current in the buffer stage aids the circuit by pushing the parasitic pole at its output (P_3) to higher frequencies and by increasing the current available for slew-rate conditions. Thus, the biasing conditions for the case of zero load-current can be designed to utilize a minimum amount of current, which yields maximum current efficiency and prolonged battery life.

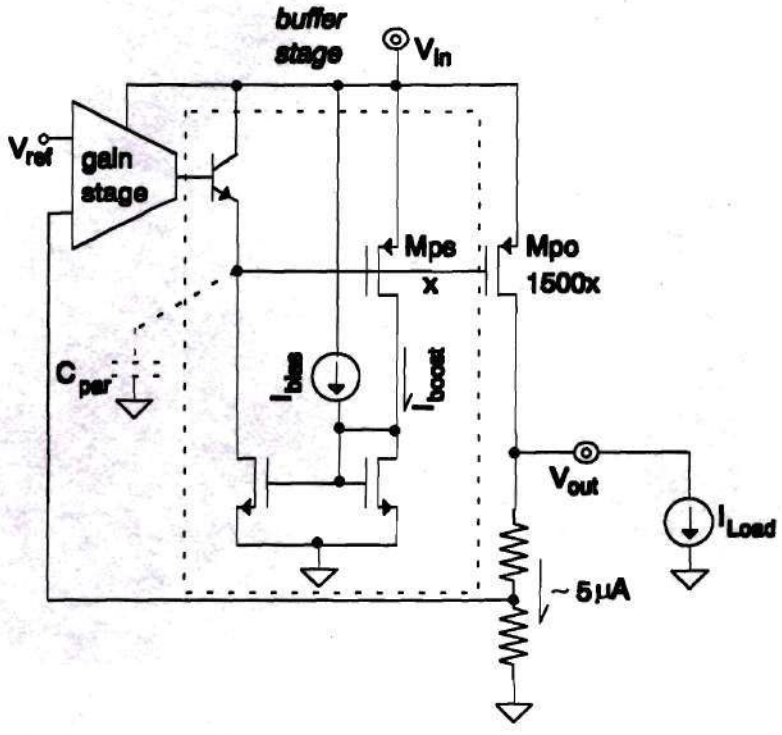


Figure 4.2. Current efficient-transient boost LDO buffer stage.

Frequency Response: The dominant pole of the system is determined by the output capacitor and the output impedance of the pass device, given by P_1 in the ac analysis section of chapter 2. When the load-current is low, the magnitude of this pole is at a minimum. This is because the output impedance of the pass device, which defines the pole for most conditions, is inversely proportional to the current flowing through it,

$$P_1 \approx \frac{1}{2\pi R_{o-pass} C_o} \approx \frac{\lambda I_{Load}}{2\pi C_o}, \tag{4.5}$$

where C_o is the output capacitance, $R_{o\text{-}pass}$ is the output resistance of Mpo in Figure 4.2, λ is the channel length modulation parameter, and I_{Load} is the load-current. Consequently, the unity gain frequency (UGF) is at low frequencies when the load-current is low, which relaxes the requirement of the parasitic pole P_3 (defined by the input capacitance of the pass device and the output impedance of the error amplifier) to be approximately greater than or equal to the minimum unity gain frequency (UGF_{min}). This corresponds to a phase margin of approximately 45 to 90 ° with the following design equation,

$$P_{3_{no-load-current}} \approx \frac{g_{m_{npn}}}{2\pi C_{par}} = \frac{I_{bias}}{2\pi V_t C_{par}} \geq UGF_{min}, \tag{4.6}$$

where $g_{m_{npn}}$ is the transconductance of the emitter follower and V_t is the thermal voltage.

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As load-current increases, however, the dominant pole increases linearly and consequently so does the UGF. The open-loop gain (A_v) is inversely proportional to the square root of the load current,

$$A_V \approx A_{amp} g_{mp} R_{o-pass} \propto \frac{\sqrt{I_{Load}}}{I_{Load}} = \frac{1}{\sqrt{I_{Load}}}, \tag{4.7}$$

where A_{amp} is the gain of the error amplifier while g_{mp} and $R_{o\text{-}pass}$ are the transconductance and the output resistance of the pass device respectively. Since the dominant pole (P_1) increases faster than the gain decreases with load-current, the unity gain frequency increases as the load-current increases (equations (4.5) and (4.7)). These consequential effects of load-current on frequency response are graphically illustrated in Figure 4.3. Therefore, the parasitic pole (P_3) is also required to increase with load-current, which is achieved by the load dependent boost current. This is apparent from the following equation,

$$P_3 \approx \frac{g_{m_{NPN}}}{2\pi C_{par}} = \frac{I_{bias}+I_{boost}}{2\pi V_t C_{par}} \approx \frac{I_{bias}+kI_{Load}}{2\pi V_t C_{par}}, \tag{4.8}$$

where k corresponds to a constant mirror ratio, i.e., 1/1500 for Figure 4.2. The circuit can be designed such that P_3 increases at a faster rate than the UGF with respect to load-current. This results in the following relation,

$$P_{3-rate} = \frac{\partial P_3}{\partial I_{Load}} \approx \frac{k}{2\pi V_t C_{par}} \geq P_{1-rate} \approx \frac{\lambda}{2\pi C_o} > UGF_{rate} \tag{4.9}$$

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or
$$k \geq \frac{\lambda V_t C_{par}}{C_o}, \tag{4.10}$$

where $P_{3\text{-rate}}$, $P_{1\text{-rate}}$, and UGF_{rate} are the rates with respect to load-current of pole P_3, pole P_1, and the unity gain frequency respectively. Thus, current efficiency can be maximized to accommodate the load dependent requirements of P_3. If the load dependence of P_3 is not incorporated into the circuit, then more current than necessary is used during low load-current conditions. The frequency response behavior was confirmed by simulations.

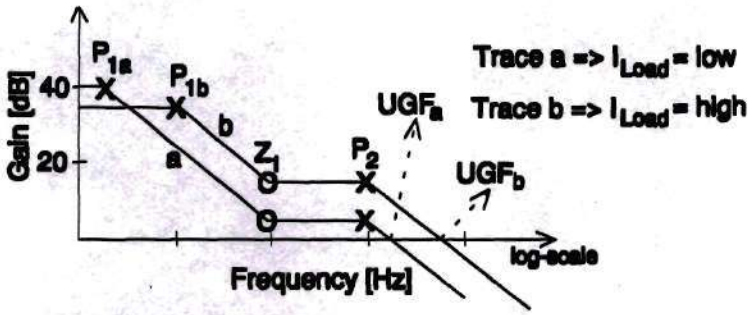


Figure 4.3. System frequency response as a function of load-current.

Transient Response: The circuit of Figure 4.2 exhibits the transient response illustrated in the transient analysis section of chapter 2 where a maximum load-current step swing is applied to the load. One of the parameters that determines the maximum output voltage variation is the response time (Δt_1) required for the system to react. However, the slew-rate current (I_{sr}), which partially determines Δt_1, is not constant for the circuit proposed, $I_{sr} = I_{bias} + kI_{boost}$. As a result, a slew-rate condition does not fully describe the operation of the circuit at hand. During a load-current transition from zero to

maximum value, the response time of the circuit is dominated by the bandwidth of the system and the transient response of the buffer stage. In particular, the response time is composed of the time required for the amplifier to respond (t_{amp}), for the sense PMOS transistor (Mps) to start conducting current ($t_{Mps\text{-}on}$), for the positive feedback circuit to latch up ($t_{latch\text{-}up}$), and for the output PMOS device (Mpo) to conduct the load-current (t_{Mpo}). This is illustrated in

$$\Delta t_1 \approx t_{amp} + t_{Mps-on} + t_{latch-up} + t_{Mpo} \approx \frac{1}{BW_{cl}} + t_{Mps-on} + t_{latch-up}, \qquad (4.11)$$

where BW_{cl} is the closed-loop bandwidth of the system (approximately $(t_{amp} + t_{Mpo})^{-1}$).

The composite buffer stage is essentially a localized positive feedback circuit. The system is stable because the positive feedback gain is less than one. Consequently, the circuit attempts to latch up until the output transistor is fully turned on; at which point, the error amplifier forces the circuit back into the linear region. As a result, the performance tradeoffs between the slew-rate and the quiescent current requirements of typical LDOs are circumvented. For instance, if the parasitic capacitance (C_{par}) is 200 pF, the voltage change required for the output PMOS transistor (ΔV_{sg}) is 0.5 V, the closed-loop bandwidth of the system is 1 MHz, and the response time (Δt_1) is confined to be less than 5 μs, then the slew-rate current ($I_{sr} = I_{bias}$) required for a class A buffer is approximately 25 μA (equation (2.11)). For the case of the circuit of Figure 4.2, a dc current bias (I_{bias}) of only 1 μA can provide the same performance. The dominant factor of Δt_1 is the time required for the sense transistor Mps to go from being off to sub-threshold and finally to strong inversion. Figure 4.4 illustrates the simulation results showing the effects of the

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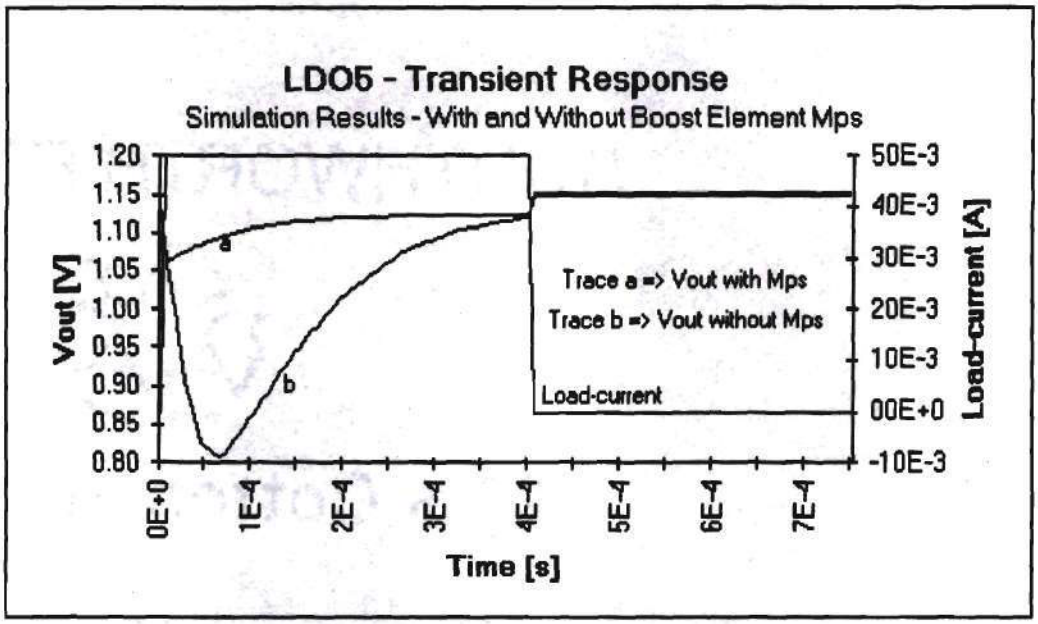


Figure 4.4. LDO output voltage variation with and without the boost element Mps in the current efficient buffer stage.

presence of the boost element Mps, in the circuit shown in Figure 4.2, on the output. It is observed that the output voltage variation is decreased as a result of a reduction in response time. This, however, does not come at the expense of additional quiescent current flow during zero load-current conditions thereby achieving maximum current efficiency and battery life.

4.2 Current Boosting

Motivation

Operation at low voltages is intrinsic in the battery operated products market. This is driven by the public demand for compactness and finer fabrication lithography. Thus, area efficient circuits and lower breakdown voltages necessitate the use of single, low voltage battery cells, i.e., 0.9 to 1.5 V. This limitation, however, could be eliminated from the low drop-out (LDO) regulator by utilizing a dc-dc converter, switching

regulator. Consequently, the dc-dc converter needs to be operable at low voltages. In other words, the problem is simply transposed to the dc-dc converter. Hence, the problem of low voltage cannot be avoided and must be handled at either the LDO or dc-dc converter level. The two main limitations of low voltage operation lie in the output current capabilities of the pass device (power switch) and voltage headroom.

Challenge

As the power supply voltages decrease, the gate drive available to the PMOS pass device decreases. As a result, the aspect ratio of the power transistor must be increased to provide acceptable levels of output current. However, the parasitic gate capacitance also increases as the size of the PMOS transistor increases. This constitutes an increase in C_{par} of Figure 4.2, which pulls its associated parasitic pole (P_3) down to lower frequencies. Consequently, the phase margin of the system is degraded and stability may be compromised. This presents a problem when working in a low quiescent current environment.

Composite Output Transistor

One way to improve gate drive without increasing input voltage or device size is by forward biasing the source to bulk junction of the PMOS pass device. This results in a reduction in threshold voltage, commonly referred as the bulk effect phenomenon. The threshold voltage (V_{th}) is described by equation (4.2). Consequently, the threshold voltage decreases as V_{sb} increases thereby effectively increasing the gate drive of the power PMOS transistor (pass device). This, in turn, permits the transistor to conduct more current under a given input voltage.

Maximum Output Current: For comparative analysis, the maximum current can be observed at the region where the power PMOS device is in saturation,

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which corresponds to non drop-out conditions. The corresponding drain current (I_{sd}) of the device is

$$I_{sd} \approx \frac{K_p W}{2L}\left[V_{sg}-V_{th}\right]^2 \approx \frac{K_p W}{2L}\left\langle V_{sg}-|V_{to}|-\gamma\left[\sqrt{2|\phi_f|-V_{sb}}-\sqrt{2|\phi_f|}\right]\right\rangle^2, \quad (4.12)$$

where K_p is the transconductance parameter of a PMOS transistor. Maximum output current results when the gate drive is at its peak, which occurs when the source to gate voltage (V_{sg}) is equal to the input voltage (V_{in}). Thus, if K_p is 15 $\mu A/V^2$, $|V_{to}|$ is 0.9 V, W/L is 30 kμm/μm, and V_{in} is 1.2 V, then the maximum output current ($I_{o\text{-}max}$) is 20 mA when the source to bulk junction is not forward biased. However, if the source to bulk junction is forward biased by 0.3 V, then $I_{o\text{-}max}$ is 38.5 mA (assuming that γ is 0.5 $V^{1/2}$ and $2|\phi_f|$ is 0.6 V). As a result, the output current capability of a PMOS device can be significantly increased by simply forward biasing the source to bulk junction. Figure 4.5 illustrates how this technique performs on the prototype circuit of Figure 4.2 where the aspect ratio of the power PMOS transistor is 2 kμm/μm. A battery is placed between the source and bulk of the output PMOS device and the load-current (I_{Load}) is swept from 0 to 500 μA. For the same input voltage, the maximum output current capability is increased as V_{sb} is increased, in other words, the circuit stays in regulation for an increased load-current range. At a forward biased junction voltage of 0.3 V, the output current is more than doubled compared to its non-forward biased state.

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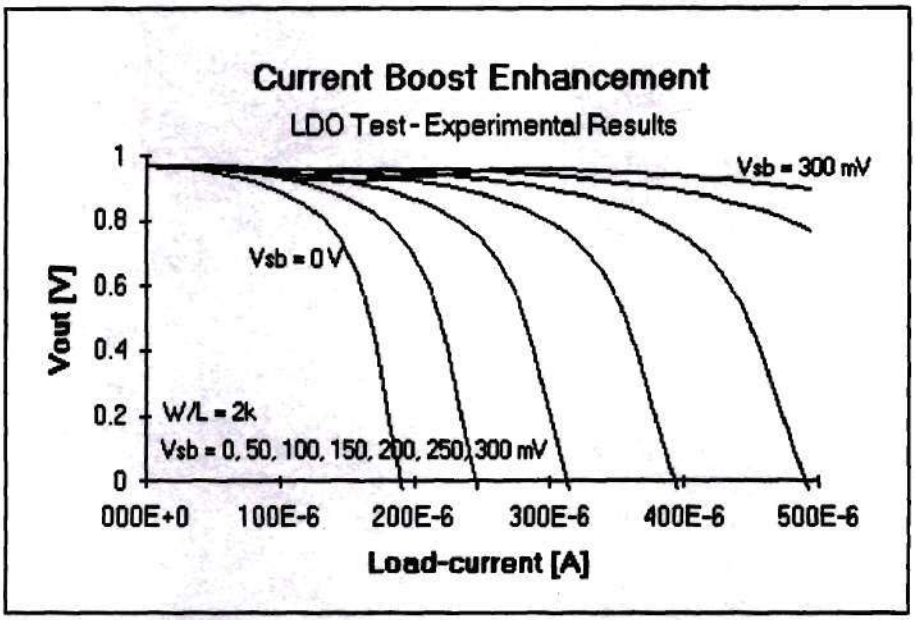


Figure 4.5. Maximum load-current performance of the current boost enhancement.

Figure 4.6 illustrates a successful implementation of the technique in a low drop-out regulator, a technique that could easily be extended to dc-dc converters. The forward biased junction is defined by the voltage drop across the schottky diode (Ds). This voltage drop has to be less than a base-emitter voltage to prevent the parasitic vertical PNP transistors of the power PMOS device (Mpo) from turning on and conducting notable ground current through the substrate via the well. The effects of the parasitic bipolar transistors are mitigated by placing a heavily doped buried layer underneath the well of the power PMOS transistor and/or by increasing the size of the schottky diode. However, the ability to shut off Mpo is not degraded since the forward bias voltage is a function of load-current. This is similar to the operation of the current efficient circuit of Figure 4.2. Thus, I_{boost} is low and V_{sb} is close to zero at low load-currents. At high load-currents, however, I_{boost} and V_{sb} increase thereby decreasing the threshold voltage and increasing the effective gate drive of the output PMOS device.

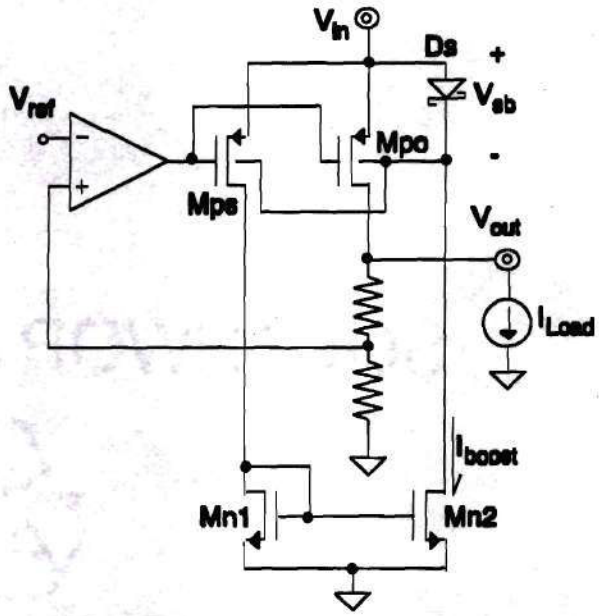


Figure 4.6. LDO with current boosting capabilities.

Drop-out Voltage: The method of forward biasing the source to bulk junction also yields lower drop-out voltages. In other words, the "on" resistance of the pass device (Mpo) is reduced. When the regulator is in drop-out, Mpo is characteristically in the triode region and exhibits the well known current relationship of

$$I_{sd} \approx \frac{K_p W}{2L}\left\langle \left[V_{sg} - V_{th}\right]V_{sd} - V_{sd}^2 \right\rangle \approx \frac{K_p W}{2L}\left[V_{sg} - V_{th}\right]V_{sd}. \qquad (4.13)$$

This current relationship can be manipulated to derive the "on" resistance (R_{on}) of the PMOS device to be approximately

$$R_{on} \approx \frac{V_{sd}}{I_{sd}} \approx \frac{2L}{K_p W}\cdot\frac{1}{\left[V_{sg} - V_{th}\right]} \approx \frac{2L}{K_p W}\cdot\frac{1}{\left\langle V_{sg} - |V_{to}| - \gamma\left[\sqrt{2|\phi_f| - V_{sb}} - \sqrt{2|\phi_f|}\right]\right\rangle} \qquad (4.14)$$

or the drop-out voltage (V_{do}) to be

$$V_{do} \approx R_{on} I_{Load} \approx \frac{2L}{K_p W} \cdot \frac{I_{Load}}{\left\langle V_{sg} - |V_{to}| - \gamma\left[\sqrt{2|\phi_f| - V_{sb}} - \sqrt{2|\phi_f|}\right]\right\rangle}. \qquad (4.15)$$

Therefore, if K_p is 15 $\mu A/V^2$, $|V_{to}|$ is 0.9 V, W/L is 30 kμm/μm, V_{in} is 1.2 V, and I_{Load} is 20 mA, then the drop-out voltage is 296 mV (corresponding to 14.8 Ω) when the source to bulk junction is not forward biased. However, if the source to bulk junction is forward biased by 0.3 V, then V_{do} becomes 216 mV (corresponding to 10.8 Ω) assuming that γ is 0.5 $V^{1/2}$ and $2|\phi_f|$ is 0.6 V. There is a theoretical improvement of approximately 27 %. Figure 4.7 illustrates the effects of forward biasing the source to bulk junction on the

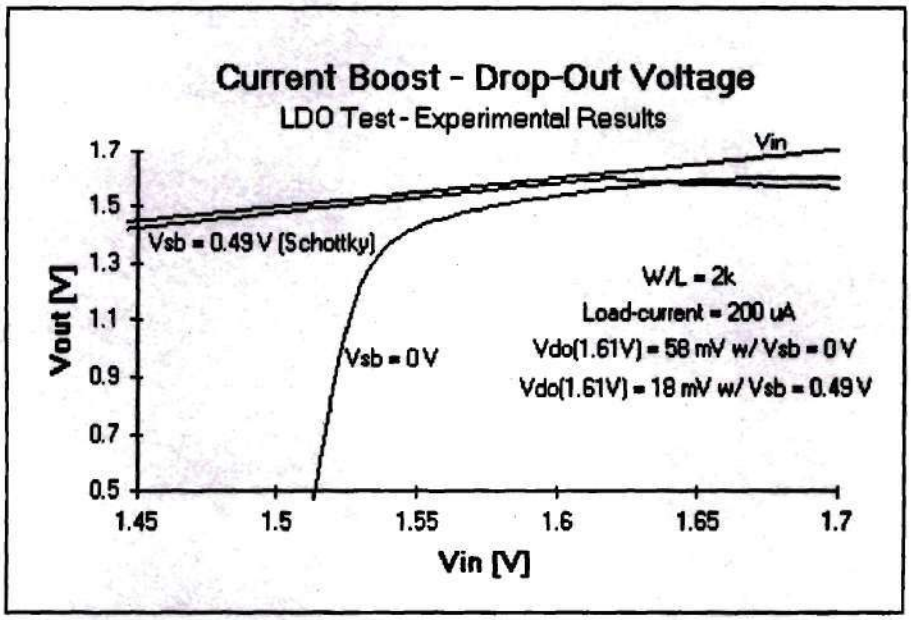


Figure 4.7. Drop-out voltage performance of the current boost topology.

drop-out performance of the prototype circuit of Figure 4.6 where the aspect ratio of Mpo is 2 kμm/μm. There is an experimental improvement of roughly 67 % with a forward bias voltage of 0.49 V.

Frequency Response: During low load-current conditions, the current through the sense transistor (Mps) and consequently the current through the schottky diode (Ds) is negligible. This is because of the high mirror ratio of the output and the sense transistor, Mpo and Mps in Figure 4.6. However, Mps and Ds start conducting appreciable currents at higher load-currents. Therefore, these elements constitute another ac signal path for the system. The effect of this path manifests itself through g_{mp} in the open-loop gain, as seen in equation (2.1). The effective transconductance of the composite pass device of the circuit in Figure 4.6 can be described as

$$g_{mp} \approx g_{m-o} + \frac{g_{mx} r_d g_{mb-o}}{[1+sr_d C_b]} \leq g_{m-o} + g_{mx} r_d g_{mb-o}, \tag{4.16}$$

where $g_{m\text{-}o}$ is the transconductance of Mpo, r_d is the resistance of diode Ds, C_b is the total bulk capacitance of Mpo and Mps, $g_{mb\text{-}o}$ is the channel conductance of the bulk of Mpo,

$$g_{mb-o} = \frac{\partial I_{sd}}{\partial V_{sb}} \approx \frac{K_p W}{L}\left[V_{sg} - V_{th}\right] \cdot \frac{\gamma}{2\sqrt{2|\phi_f| - V_{sb}}} = g_{m-o} \cdot \frac{\gamma}{2\sqrt{2|\phi_f| - V_{sb}}}, \tag{4.17}$$

and g_{mx} is

$$g_{mx} = \frac{g_{m-s} g_{m-n2}}{g_{m-n1}}, \tag{4.18}$$

where g_{m-s}, g_{m-n1}, and g_{m-n2} are the transconductances of Mps, Mn1, and Mn2 respectively. As a result of the high mirror ratio between Mpo and Mps, the effective transconductance of the PMOS pass device (g_{mp}) is virtually unaffected by the current boosting technique, $g_{mp} \approx g_{m-o}$. This can be illustrated by assuming that Mn1 and Mn2 have a 1:1 mirror ratio, W/L_s is 20 μm/μm, I_{Load} is 50 mA, and W/L_o is 30 kμm/μm; the effective transconductance of the composite PMOS device is roughly g_{m-o} (1 + 0.05) at dc, where $r_d \approx V_t / I_{diode}$, $K_p = 15\ \mu A/V^2$, $\gamma = 0.5\ V^{1/2}$, $2|\phi_f| = 0.6$ V, and $V_{sb} = 0.3$ V.

4.3 Load Regulation

Challenge

Load regulation is limited by the frequency response of a typical low drop-out regulator architecture under loading conditions. Load regulation is defined as the output voltage variation resulting from a unit load-current change, which is equivalent to the output resistance of the regulator (R_{o-reg}),

$$R_{o-reg} = \frac{\Delta V_{LDR}}{\Delta I_o} = \frac{R_{o-pass}}{1 + A_{ol}\beta}, \tag{4.19}$$

where ΔV_{LDR} and ΔI_o are the output voltage and the load-current changes respectively, R_{o-pass} is the output resistance of the pass element, A_{ol} is the open-loop gain of the system, and β is the feedback factor [3]. Thus, load regulation performance is determined by the open-loop gain of the system. Unfortunately, the dc gain is limited by the frequency response of the regulator, as discussed in chapter 2. Frequency analysis shows that there are three poles and one zero, illustrated in Figure 4.8. For a given unity gain frequency (UGF), the magnitude of the system's dc open-loop gain is restricted by the

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location of the poles and the zero, i.e., 40 dB for the response illustrated in Figure 4.8. The worst-case condition occurs when Z_1 is at low frequencies and P_2 is at high frequencies, which corresponds to high values of electrical series resistance (ESR) for the output capacitor and low values of bypass capacitance (C_b). The UGF, in particular, is determined by the maximum allowable response time and the frequency range where the parasitic poles of the system reside, such as the internal poles of the error amplifier.

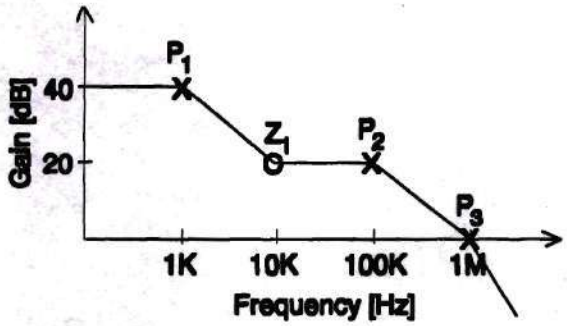


Figure 4.8. Linear regulator frequency response.

Pole/Zero Pair Generation

The dc open-loop gain of the system can be augmented, however, by adding a pole/zero pair as shown in Figure 4.9. For a given unity gain frequency (UGF), the upper limit of the open-loop gain can be increased by manipulating the frequency response as depicted by trace B of the Figure. The basic idea is for the gain to drop quickly as the frequency increases so that a larger dc gain is possible. Hence, regulation is improved while keeping the UGF away from parasitic poles. The placement of the extra pole and zero must take into account that P_1, P_2, and Z_1 are functions of the output capacitance, the electrical series resistance (ESR) of the output capacitor, and the load-current. However, the fact that P_2 and Z_1 track each other (both are inversely proportional to ESR) can be used to optimize the design. It is further noted that the phase shift must be

kept below 180 ° at frequencies equal to and lower than the UGF to maintain stability, as dictated by Nyquist criterion [39].

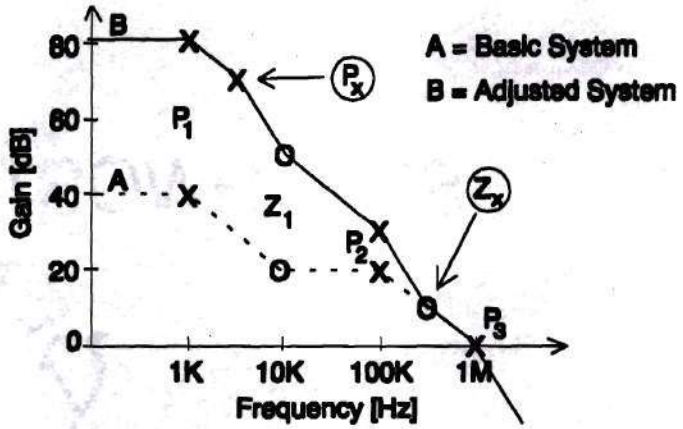


Figure 4.9. System's frequency response with an additional pole/zero pair.

Figure 4.10 illustrates the simulation results of an LDO incorporating the additional pole/zero pair. There is roughly a 17 dB improvement in the dc open-loop gain of the system with the additional pole/zero pair for a given unity gain frequency (UGF). Load regulation performance improved from approximately 41 to 12 mV / 100 mA, corresponding to a 71 % reduction. The design location of the additional pole and zero depends on the gain of the system and the variability of Z_1 and P_2. The achievement of maximum gain comes at the expense of restricted ESR range. This range is important for its variation is dependent on the type of capacitor and the fabrication process. Typically, relatively inexpensive capacitors exhibit the worst ESR variation. Given a constant UGF, maximum gain occurs when P_x and Z_x are maximally displaced from each other in frequency. This is because the drop in gain per decade of frequency in mid-band is larger when P_x is at lower frequencies and Z_x is at higher frequencies. Thus, maximum gain can be achieved efficiently if Z_1 and P_2 are guaranteed to be between P_x and Z_x throughout

their entire range. For this to be true, the ESR must be greater than some finite non-zero number. However, Z_1 and P_2 tend to infinity as the ESR is allowed to approach zero. Consequently, the frequency differential between P_X and Z_X is limited by the phase requirements of the system, less than 180° phase shift. If the ESR is bounded by a finite lower limit where Z_X is guaranteed to be greater than Z_1, the phase minimum is defined by P_X and Z_1, otherwise defined by P_X and Z_X.

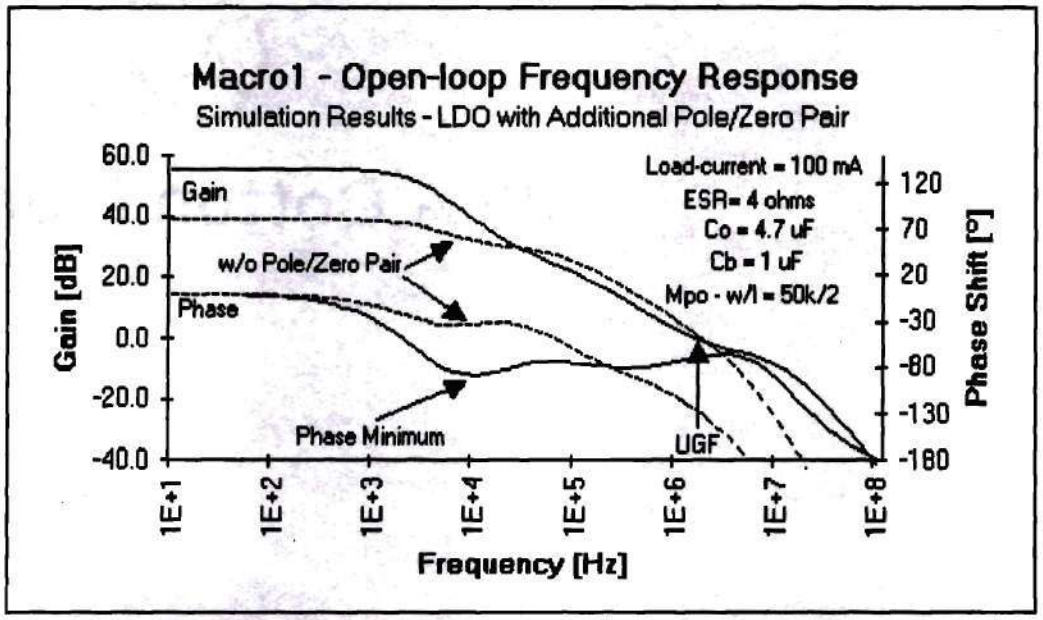


Figure 4.10. AC simulation of LDO with an additional pole/zero pair.

Circuit Realizations

The adjusted circuit architecture needs to provide a new function, namely, adding a pole/zero pair in the frequency response of the open-loop system. A customary method of adding a pole/zero pair is through the use of passive components at the output. Another way to achieve the same goal is to actually incorporate it into the frequency response of

the error amplifier via active components. In essence, the amplifier serves to shape the frequency behavior of the system as well as provide gain.

Parallel Amplifier Structure: One method of integrating the pole/zero pair response into the amplifier is to have dual amplifiers connected in parallel as shown in Figure 4.11. One amplifier has high gain and whose bandwidth determines the location of P_x while the other has lower gain (whose magnitude determines the location of Z_x) and higher bandwidth. The output impedances of both amplifiers need to be relatively low for proper operation. The main concept revolves around feed-forwarding the ac signal through a bypass path constituted by the amplifier with lower gain. The transfer function of both amplifiers and the resulting response of the system are shown in Figure 4.11 (b). The gain-bandwidth product of the high gain amplifier can be utilized to determine the necessary gain of the other amplifier to introduce Z_x at the desired frequency, as shown by the following relation,

$$GBW_1 = \frac{A_1}{2\pi P_x} = \frac{A_2}{2\pi Z_x} \quad \text{or} \quad \frac{A_1}{A_2} = \frac{P_x}{Z_x}, \tag{4.20}$$

where A_1 and A_2 correspond to the gain of amplifier one and two respectively while GBW_1 corresponds to the gain-bandwidth product of amplifier one. It is observed that the bandwidth of the second amplifier constitutes a parasitic pole in the overall system. Furthermore, the frequency of P_x is dependent on the dominant pole of amplifier one, which is subject to process variations. However, the ratio of P_x and Z_x exhibits less variation since it is mainly determined by component matching issues, if designed carefully. The main disadvantage of the circuit is complexity. Consequently, the realization of the two amplifiers may prove to be costly in terms of quiescent current flow. This results

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from more current sensitive transistor paths to ground because there are two amplifiers. Figure 4.10 shows the simulation results of a macro-model circuit implementing the parallel amplifier structure.

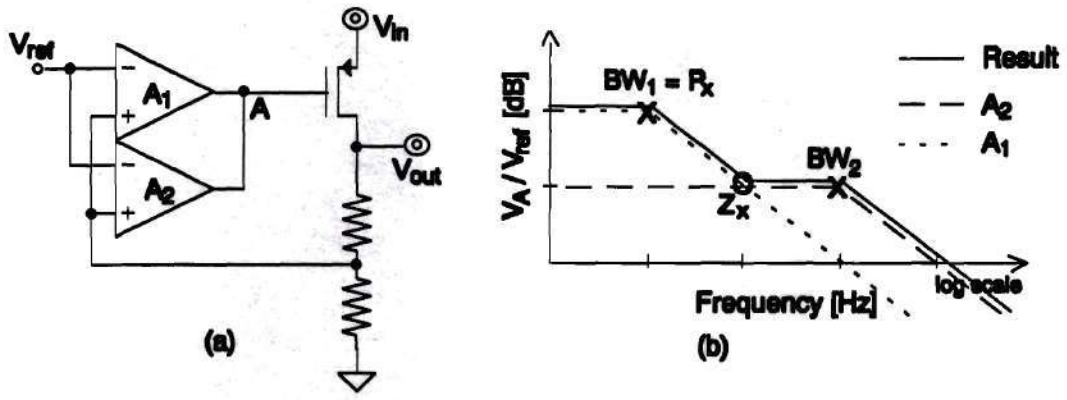


Figure 4.11. Parallel amplifier pole/zero pair realization.

Frequency Shaping Amplifier: A pole/zero pair can also be generated through the use of a feed-forward capacitor in a folded topology as shown in Figure 4.12 (a). At low frequencies, the amplifier is unaffected by the feed-forward capacitor (C_{ff}). Thus, the gain is that of a typical folded topology, which is characteristically high. At high frequencies, the capacitor acts like an electrical short giving rise to the gain of a non-cascoded architecture (lower gain). The corresponding small signal model of the circuit is represented in Figure 4.12 (b). The gain of the amplifier (A_v) is described by

$$A_v \approx g_{m1} R_o = g_{m1}[R_{Load} \| R_x] \approx g_{m1} R_x, \qquad (4.21)$$

where g_{m1} is the transconductance of Mp1, R_{Load} is the output resistance of the mirror load, and R_x is

$$R_X = \frac{r_{ds3}\left[1+g_{m3}r_{ds2}\right]}{1+sr_{ds3}C_{ff}} + r_{ds2} = \frac{\left\langle s+\dfrac{r_{ds2}+r_{ds3}\left[1+g_{m3}r_{ds2}\right]}{r_{ds3}r_{ds2}C_{ff}}\right\rangle r_{ds2}}{s+\dfrac{1}{r_{ds3}C_{ff}}}, \qquad (4.22)$$

where g_{m3} is the transconductance of Mn3 and r_{ds2} [r_{ds3}] is the output resistance of

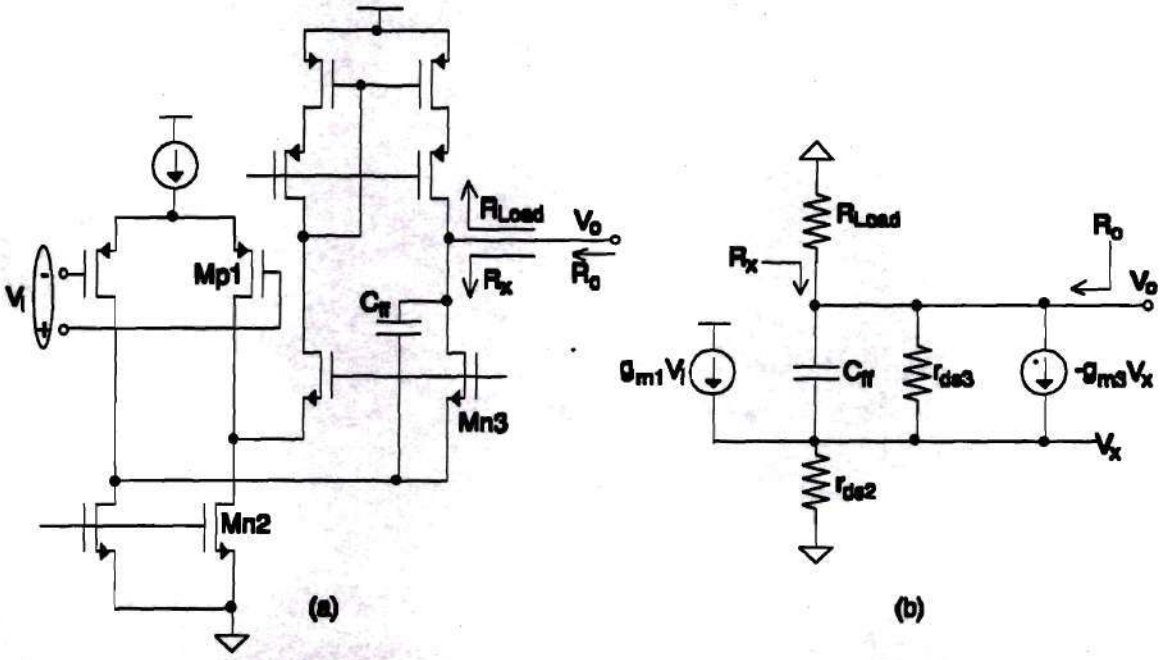


Figure 4.12. Pole/zero pair generation by a feed-forward capacitor.

transistor Mn2 [Mn3]. Consequently, the locations of the pole and the zero are

$$Z_x \approx \frac{g_{m3}}{2\pi C_{ff}} \qquad (4.23)$$

and $$P_x \approx \frac{1}{2\pi r_{ds3} C_{ff}}, \qquad (4.24)$$

where g_{m3} and r_{ds3} correspond to the transconductance and the output resistance of Mn3. The cascoding element's transconductance (g_{m3}) needs to be small, which implies the use of MOS devices instead of bipolar transistors in a biCMOS environment.

The frequency shaping amplifier can also take a couple of other forms within the same folded architecture, as is illustrated by the different loading structures in Figure 4.13. A variation of the feed-forward concept is embodied in the circuit of Figure 4.13 (a). Small signal analysis shows that the pole and the zero locations for this structure are described by

$$Z_x \approx \frac{1}{2\pi R C_{ff}} \qquad (4.25)$$

and $$P_x \approx \frac{1}{2\pi [R + r_{o3}] C_{ff}}, \qquad (4.26)$$

where r_{o3} is the output resistance of Qn3. Yet another realization of the pole/zero pair is illustrated in Figure 4.13 (b). This circuit takes advantage of the input and the output impedance of the mirror load, composed of Mp4 and Mp5, to help shape and define the frequency response of the amplifier. The corresponding pole and zero locations are described by

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$$Z_x = \frac{1}{2\pi\left\langle R + \frac{1}{g_{m5}}\right\rangle C} \tag{4.27}$$

and

$$P_x = \frac{1}{2\pi\left\langle R + \frac{1}{g_{m5}} + r_{ds4}\right\rangle C}, \tag{4.27}$$

where g_{m5} is the transconductance of Mp5 and r_{ds4} is the output resistance of Mp4.

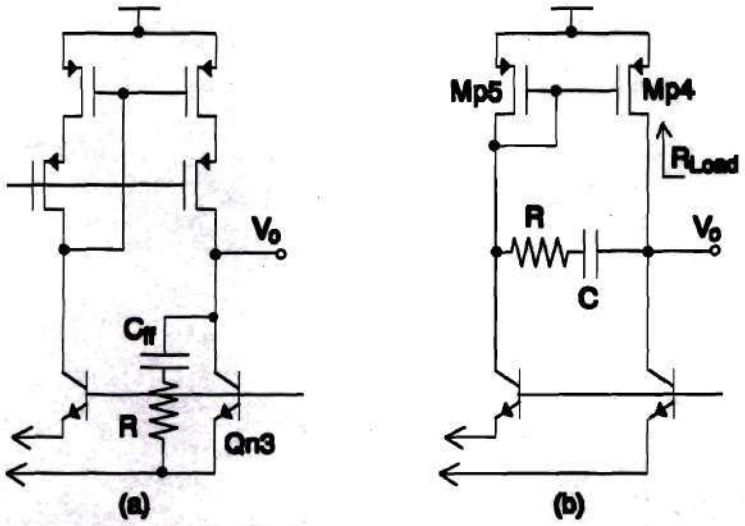


Figure 4.13. Variations of the frequency shaping amplifier.

The frequency response of the amplifiers introduce a single parasitic pole to the overall system. This parasitic pole is formed by the loading capacitor of the amplifier. This may be significantly large if the amplifier drives the gate of the large power PMOS transistor directly, pass device in the linear regulator structure. The severity of this

problem can be alleviated by buffering the output of the amplifier and thus isolating the large capacitive load from the amplifier. The effects of process variations on performance manifest themselves through deviations in transconductances and transistor output impedances, which in turn define the locations of the pole and the zero as well as the parasitic pole. Simulations confirmed the operation of the frequency shaping amplifier topologies showing results that closely resemble those illustrated in Figures 4.9 and 4.10.

4.4 Summary

This chapter has identified the challenges of designing in a low voltage and low quiescent current atmosphere and developed appropriate techniques for achieving the necessary performance requirements. Current efficiency was identified as an intrinsic regulator characteristic for prolonged battery life. This was followed by a circuit development culminating in a current efficient buffer circuit. The problems with output current capabilities under reduced gate drives were addressed, which led to the development of the composite current boosted pass device. Lastly, the inherent limit of load regulation was identified along with a technique used to enhance its performance, the addition of a pole/zero pair. Appropriate circuits were then developed climaxing in the frequency shaping amplifiers. At this point, all that is needed is a low voltage and low quiescent current reference. Chapter 5 develops the techniques necessary for generating such a reference.

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CHAPTER V

REFERENCE DEVELOPMENT

There are many reference topologies available for a variety of different applications and process technologies. Currently, a large portion of the market demand is driven by portable electronic products whose operating voltages range from 0.9 to 5 V and whose temperature drift requirements are in the order of 10 to 50 ppm/°C. In particular, the direction of the market is towards single, low voltage battery cell operation. As a result, the specifications become more stringent because of an inherent reduction in dynamic range. This chapter illustrates several of the prevailing concepts that lead to the development of low voltage references. The discussion places emphasis on performance and feasibility in a low voltage environment. This is followed by a description of the pertinent output structures and some of their circuit implications. Finally, the chapter concludes by portraying several curvature correcting schemes appropriate for second order bandgaps.

5.1 Topologies

Zener

One of the most common and simplest realizations of a reference circuit is through the use of a zener diode and a resistor [1, 21] as shown in Figure 5.1. When the diode is forward biased, the voltage across the diode exhibits the well known exponential

relationship to current. When the diode is reverse biased, the current through the diode becomes negligible. However, if enough reverse bias voltage is applied, the diode goes into the reverse breakdown region. In this mode of operation, significant changes in current lead to nearly negligible fluctuations in diode voltage. As a result, a low output impedance at the cathode of the diode arises varying typically from 10 to 300 Ω. Most common zener diodes have a breakdown voltage between 5.5 and 8.5 V and a positive temperature drift, approximately between +1.5 and +5 mV/°C. This temperature drift can be reduced by cascading a negative temperature coefficient element, i.e., a forward biased diode with a typical drift of roughly -2 mV/°C. This performance enhancement, however, comes at the expense of increased output voltage. As a result of high operating voltages, the zener diode is appropriately demanded by high voltage applications [1, 3].

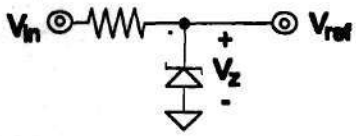


Figure 5.1. Zener diode reference.

First Order Bandgap

First order bandgap references are more accurate and suitable for low voltage operation than the zener counterparts. Typical bandgap references have an output voltage of approximately 1.2 V, which corresponds to the bandgap voltage. The operation is based on the temperature dependence of the base-emitter voltage of a bipolar transistor (V_{be}) or equivalently a forward biased diode. This dependence can be observed to have a linear and a nonlinear component with respect to temperature, as described by

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$$V_{be} \approx V_{go} - \frac{T}{T_r}\left[V_{go} - V_{be}(T_r)\right] - [\eta - x] V_t \ln \frac{T}{T_r}, \qquad (5.1)$$

where V_{go} is the bandgap voltage at 0 K (constant), T is the temperature, T_r is a reference temperature, $V_{be}(T_r)$ is the value of V_{be} at T_r, η is a process dependent constant, V_t is the thermal voltage, and x is determined by the temperature dependence of the collector current ($I_c \propto T^x$, i.e., x = 1 for $I_c = I_{PTAT} = CT^1$ where C is a constant). Appendix A describes the derivation of said equation, which is a variant of that offered by [40]. First order bandgaps compensate the linear component and ineffectively compensate the nonlinear component by summing a proportional-to-absolute temperature (PTAT) voltage and a base-emitter drop. The PTAT voltage increases linearly with temperature thereby efficiently canceling the effect of the negative linear temperature dependence of the base-emitter voltage. The resulting output voltage exhibits improved temperature variation performance, typically between 20 and 50 ppm/°C [41]. However, the extent of the improvement is limited by the nonlinear component embodied in the logarithmic term of equation (5.1) and whose effect is depicted by the curvature of V_{ref} in Figure 5.2.

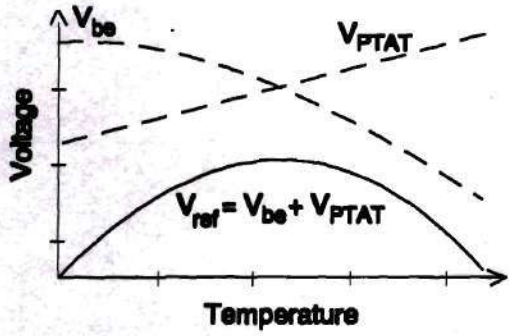


Figure 5.2. Temperature behavior of first order bandgaps.

Curvature Corrected Bandgap

Curvature corrected bandgaps attempt to approximately cancel the nonlinear component of the base-emitter voltage, typically referred to as a second order effect. The classical method of doing such compensation is through the addition of a squared PTAT term to the output voltage relation of first order bandgaps [42]. The idea is to offset the negative temperature dependence of the logarithmic term in V_{be} with a positive parabolic term. Figure 5.3 shows the typical temperature drift performance achieved by a squared PTAT term curvature corrected bandgap. The lower temperature range is predominantly controlled by the base-emitter voltage and the linear PTAT term (V_{be} + V_{PTAT}). However, the squared PTAT term ($V_{PTAT}2$) becomes considerably large as the temperature increases. This behavior is used to cancel the increasingly negative temperature dependence of the base-emitter voltage to yield the curvature depicted by V_{ref} in Figure 5.3. One implementation of the squared PTAT term is through the use of a Gilbert Multiplier cell and a PTAT current generator. Prevailing curvature corrected bandgaps achieve a temperature drift performance of roughly 1 to 20 ppm/°C [41].

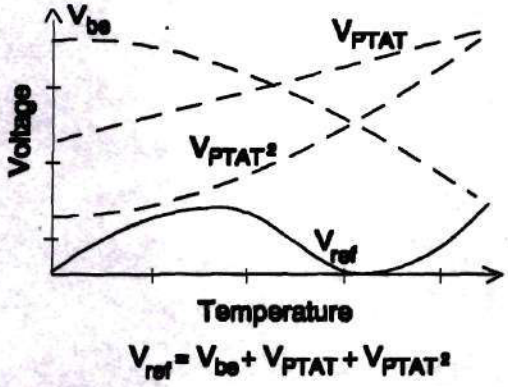


Figure 5.3. Squared PTAT curvature correction method for bandgaps.

5.2 Output Structures

V-mode and I-mode

Typical circuit realizations of references adopt a voltage-mode approach, labeled here as V-mode. In other words, the reference voltage is defined by the summation of temperature dependent voltages, as intimated by the previous discussion and realized by many curvature corrected bandgap references like that of [43]. This is also the case for zener and most bandgap references, i.e., $V_{be} + V_{zener}$ for compensated zener references or $V_{be} + V_{PTAT}$ for bandgaps as shown in Figure 5.4 (a). The resulting output voltage is approximately 1.2 V, which corresponds to the bandgap voltage at 0 °K (equation (5.1)). One benefit of this approach is that temperature compensation can be manipulated at the output by a simple adjustment, i.e., changing the resistor value in the reference circuit of Figure 5.4 (a). On the other hand, the magnitude of the reference voltage places a harsh limit on low voltage operation. The corresponding input voltage must be greater than or equal to approximately 1.4 V (a V_{sat} above the bandgap voltage). The driving market, unfortunately, demands single, low voltage battery cell operation. Consequently, there are applications that require and significantly benefit from references whose output voltages are less than 1.2 V.

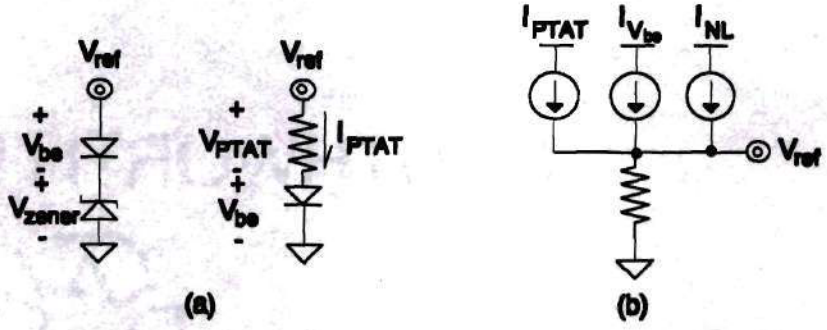


Figure 5.4. Output structures (a) voltage-mode and (b) current-mode.

Lower reference voltages can be achieved by the implementation of a current-mode topology, depicted here as I-mode. The technique relies on summing temperature dependent currents into a resistor, as shown in Figure 5.4 (b). For the case of curvature corrected bandgaps, the temperature dependencies of the current components are PTAT, base-emitter voltage, and some nonlinear behavior (NL). The value of the output voltage is determined by the product of the magnitude of the currents and the resistor. Consequently, the output voltage for this configuration is flexible enough to accommodate a wide range of values ranging from a few millivolts to several volts. Such a circuit is realized and embodied in the bipolar, low voltage reference design of [40]. If designed properly, the temperature dependence of the resistor is canceled out by the nature of the currents, which are defined by resistors of equal type. This is illustrated by the relationship of the reference voltage and the temperature dependence of the resistor where the values of the currents reflect how they are physically generated,

$$V_{ref} = \left(I_{V_{be}} + I_{PTAT} + I_{NL}\right)R = \left(K_a \frac{V_{be}}{R_a} + K_b \frac{V_t}{R_b} + I_{NL}\right)R, \qquad (5.2)$$

where K_a and K_b are constants, R_a and R_b are resistors (same type as R), and the terminology of Figure 5.4 (b) is adopted. The temperature dependence of the resistors can be described as

$$R(T) = R(T_r)\cdot\left[1 + A(T - T_r) + B(T - T_r)^2\right], \qquad (5.3)$$

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where T is temperature, A and B are the linear and the quadratic temperature coefficients, and $R(T_r)$ is the resistance at room temperature (T_r). Consequently, the reference voltage can be re expressed as

$$V_{ref} = \left\langle K_a \frac{V_{be}}{R_a(T_r)} + K_b \frac{V_t}{R_b(T_r)} + I_{NL} \right\rangle \frac{R(T_r)\cdot\left[1 + A(T - T_r) + B(T - T_r)^2\right]}{1 + A(T - T_r) + B(T - T_r)^2} \quad (5.4)$$

or

$$V_{ref} = \left\langle K_a \frac{V_{be}}{R_a(T_r)} + K_b \frac{V_t}{R_b(T_r)} + I_{NL} \right\rangle R(T_r), \quad (5.5)$$

where I_{NL} is redefined to absorb the temperature dependence of the resistor. Hence, the temperature coefficients of the resistors are canceled as long as R_a, R_b, and R are all the same type, i.e., base-diffusion resistors.

IV-mode

The benefits of a current-mode and a voltage-mode topology can be combined to generate a widely flexible structure. Such a structure is illustrated in Figure 5.5 and referred as an IV-mode structure. The resulting architecture complements the basic current-mode topology with a voltage-mode ladder. The current-mode approach offers the possibility of lower reference voltages while the voltage-mode ladder gives greater temperature compensation maneuverability. Hence, a low voltage reference is realized whose individual temperature components can be optimized during the trimming process. The resulting relation of the reference voltage (V_{ref}) can be described by

$$V_{ref} = I_{V_{be}}[R_1 + R_2 + R_3] + I_{PTAT}[R_1 + R_2] + I_{NL} R_1, \quad (5.6)$$

where I_{Vbe}, I_{PTAT}, and I_{NL} correspond to the base-emitter, PTAT, and nonlinear temperature dependent currents respectively. The temperature dependence of the resistors is canceled by the nature of the currents, similar to the current-mode case. A trimming algorithm for this type of structure is shown in appendix B.

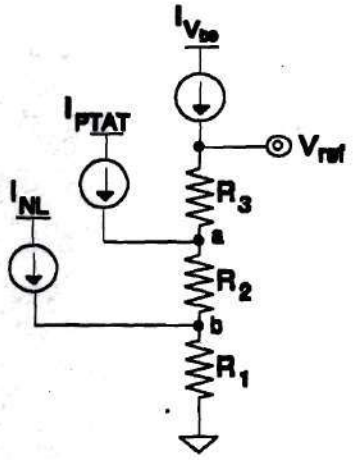


Figure 5.5. IV-mode output topology.

5.3 Bandgap Curvature Correction Techniques

The consequence of the growing demand for low voltage operation is reduced voltage swings as well as reduced dynamic range [10]. This results because the noise floor does not decrease linearly with reductions in power supply voltage. As a result, precise references are necessary. Thus, curvature correction techniques for bandgap circuits need to be scrutinized. The typical correction technique of generating a squared PTAT term is effective but its circuit realization tends to be expensive in terms of component count and quiescent current flow. Alternative methods include a base-emitter voltage loop, beta (β) compensation, quasi-nonlinear cancellation, temperature dependent resistor ratio, and current subtraction.

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V_{be} Loop

Through the combination of different temperature dependent currents and a base-emitter voltage loop a nonlinear current component can be effectively generated [40]. This technique is appropriate for I-mode and IV-mode output topologies. The circuit realization is illustrated in Figure 5.6. The nonlinear current component (I_{NL}) is defined by the temperature dependent currents and by the transistor loop formed by Qn1 and Qn2,

$$I_{NL} = \frac{V_t}{R_3} \ln \frac{I_{c1} A_2}{A_1 I_{c2}} = \frac{V_t}{R_3} \ln \frac{2I_{PTAT}}{I_{NL} + I_{constant}}, \tag{5.7}$$

where $I_{constant}$ is a quasi-temperature independent current that is subject to the temperature coefficient of the resistors,

$$I_{constant} = I_{NL} + I_{PTAT} + I_{V_{be}} \approx I_{NL} + \frac{V_t}{R_x} + \frac{V_{be}}{R_2}, \tag{5.8}$$

where V_t is the thermal voltage, I_{c1} [I_{c2}] and A_1 [A_2] are the collector currents and areas of Qn1 [Qn2] respectively, and R_x is a resistor used to define I_{PTAT}. The current I_{NL} is a logarithmic function of itself thereby exhibiting a nonlinear behavior. The resulting reference voltage (V_{ref}) of this current-mode circuit is

$$V_{ref} = \left\langle \frac{V_{be}}{R_2} + \frac{V_t}{R_3} \ln \frac{2I_{PTAT}}{I_{NL} + I_{constant}} + I_{PTAT} \right\rangle R_1. \tag{5.9}$$

Although the method is appropriate for high accuracy in a low voltage environment, the circuit's complexity is conducive towards relatively high quiescent current flow. The physical realization of the circuit by [40] achieved a temperature coefficient (TC) of roughly ± 3.0 ppm/°C with a total quiescent current flow of 95 µA.

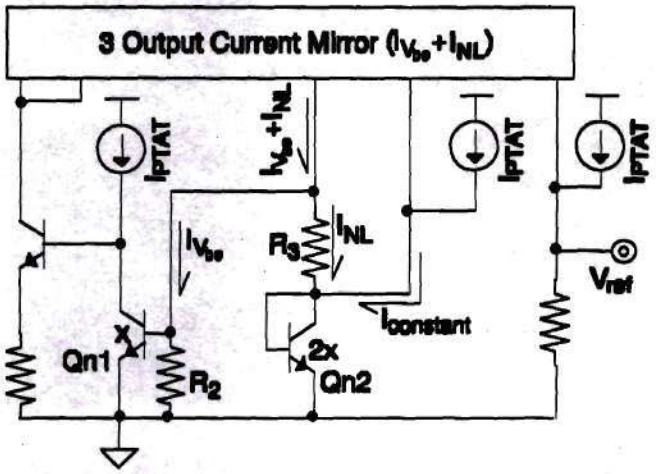


Figure 5.6. V_{be} loop curvature correction method.

β Compensation

Another technique for correcting the nonlinear behavior of the base-emitter voltage is by exploiting the exponential temperature dependence of the NPN transistor's forward current gain (β), $\beta \propto e^{-1/T}$ [44]. Figure 5.7 illustrates a simple circuit realization that takes advantage of this relationship to temperature. The circuit implements a negative reference but its translation to a positive voltage architecture is simply achieved by designing the complement of the structure. The resulting reference voltage is

$$V_{ref} = -\left(AT + \frac{BT}{\beta}\right)R - V_{be}, \qquad (5.10)$$

where A and B are constants and T refers to temperature. The circuit has the advantage of being simple and achieving good performance at low quiescent currents. However, the circuit falls within the category of a voltage-mode topology. Consequently, it is not appropriate for low voltage operation because the input voltage is limited by the bandgap voltage, $V_{in} \geq |V_{ref}| + V_{sat} = V_{go} + V_{sat} \approx 1.4$ V. A more complex circuit would be required to transform the topology into a low voltage, current-mode structure.

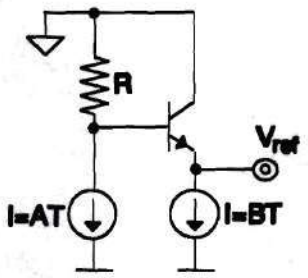


Figure 5.7. β curvature corrected bandgap.

Nonlinear Cancellation

The ideal method of performing curvature correction lies in completely correcting the nonlinear behavior of a bandgap reference by eliminating the nonlinear term of the base-emitter voltage relationship, the logarithmic term of equation (5.1). This can be accomplished by manipulating the variable x to equal the extrapolated process dependent constant η, which is approximately four [45]. In particular, x is dependent on collector current; thus, when the collector current for an NPN device is PTAT ($I_c \propto T^1$) x is equal to one. On the other hand, x is equal to zero when the collector current is independent of temperature ($I_c \propto T^0$). This behavior is exploited in the circuit illustrated in Figure 5.8 where an NPN diode loop is implemented. The resulting reference voltage can be described by

$$V_{ref} = V_{PTAT} + 4V_{be}(I_{PTAT}) - 3V_{be}(I_{constant}), \tag{5.11}$$

where $V_{be}(I_{PTAT})$ and $V_{be}(I_{constant})$ are base-emitter voltages with I_{PTAT} and $I_{constant}$ as collector currents respectively. If equation (5.1) is substituted into (5.11), the reference voltage becomes

$$V_{ref} = V_{go}\left[1 - T_r^{-1}\right] + V_{PTAT} + T\frac{V_{be}(T_r)}{T_r} - [\eta - 4]V_t \ln\frac{T}{T_r}; \tag{5.12}$$

however, η - 4 approximately cancels to zero yielding a theoretically linear relationship with respect to temperature,

$$V_{ref} \approx V_{go}\left[1 - T_r^{-1}\right] + V_{PTAT} + T\frac{V_{be}(T_r)}{T_r}. \tag{5.13}$$

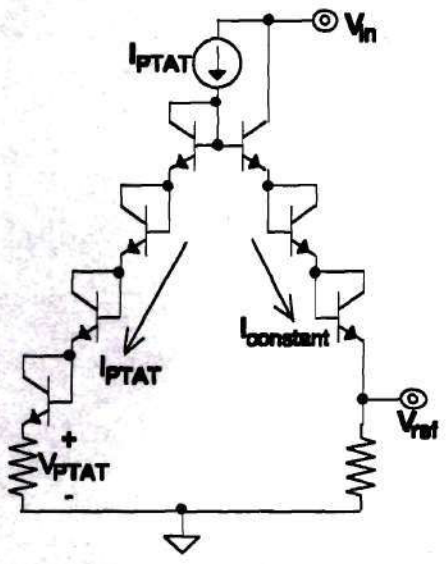


Figure 5.8. Quasi-nonlinear term cancellation bandgap reference.

This relation, unfortunately, is susceptible to two non idealities, namely, the effects of the temperature coefficient of the resistors in the circuit and the non integer nature of the value of η. Nevertheless, the circuit provides an accurate reference voltage with potentially low quiescent current flow. The major drawback, however, is that the circuit topology is not appropriate for low voltage operation. This a result of the stack of multiple base-emitter voltages,

$$V_{in} \geq V_{PTAT} + 4V_{be} + V_{current\text{-}source}. \tag{5.14}$$

Temperature Dependent Resistor Ratio

A nonlinear component can be generated by exploiting the temperature dependence of resistors in a given process. Typically, this is either canceled or considered a parasitic in most circuit realizations. Figure 5.9 illustrates how the temperature coefficient (TC) of resistors can be used in an IV-mode bandgap reference for curvature correction. The idea is to temperature compensate by generating a squared PTAT term (classical curvature correction method) without incurring a significant cost in quiescent current flow. The reference voltage of the sample circuit is

$$V_{ref} = \frac{AV_{be}}{R_1}R_4 + \frac{AV_t}{R_2}R_4 + \frac{AV_t}{R_2}R_3, \tag{5.15}$$

where A and B are constants, V_t corresponds to the thermal voltage, and all the resistors are the same type except for R_3. Thus, the temperature dependence of the resistor ratio of R_3 and R_2 must be roughly linearly positive to generate an approximated $PTAT^2$ term. This can be achieved by choosing two appropriate resistor types. Consequently, the third

term of equation (5.15) corresponds to the curvature correcting component while the first two correspond to a first order bandgap. The architecture has the advantage of being simple to realize as well as not require any additional quiescent current. The circuit suffers from a subtle disadvantage, namely, the large mismatch between the two types of resistors. This simply translates to more stringent trimming procedures. A significant disadvantage, however, lies in successfully finding two types of resistors whose ratio has a positive and linear temperature dependence within a given process technology.

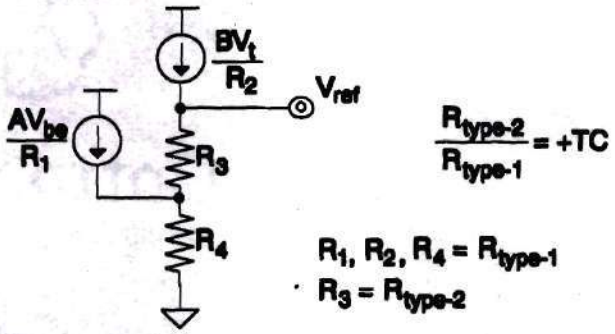


Figure 5.9. Temperature dependent resistor ratio curvature correction.

Current Subtraction

A curvature correcting nonlinear component can also be realized by manipulating different temperature dependent currents via ordinary transistors. Figure 5.10 shows how a current subtraction circuit can generate this nonlinear component (I_{NL}). The essence of the circuit revolves around current subtraction and the innate characteristics of non ideal transistors. Transistor Mp1 acts like a non ideal current source of a current that is proportional to a base-emitter voltage. At the lower half of the temperature range, the PTAT current sunk (I_{PTAT}) is less than the supplied V_{be} dependent current (I_{Vbe}). As a result, Mp2 is off and Mp1 becomes non-saturated and provides only the PTAT current. At the upper half of the temperature range, however, the current sunk becomes larger than

the V_{be} dependent current supplied by Mp1. Consequently, Mp1 becomes saturated and only supplies the V_{be} dependent current while Mp2 sources the current difference. The resulting current through Mp3 (mirror ratio of Mp2) is nonlinear, off during the first half of the temperature range and on during the latter half. This behavior can be described by

$$I_{NL} = \begin{cases} 0 & I_{V_{be}} \geq I_{PTAT} \\ I_{PTAT} - I_{V_{be}} & I_{V_{be}} < I_{PTAT} \end{cases}. \tag{5.16}$$

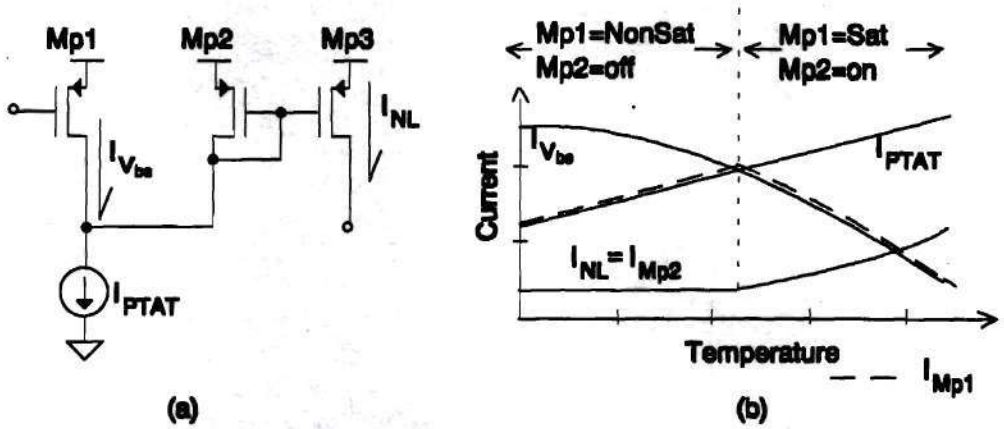


Figure 5.10. Current subtraction method for generating I_{NL}.

Figure 5.10 (b) graphically illustrates the operation of the circuit throughout the temperature range. Curvature correction is achieved by combining the three temperature dependent elements to yield an output that is stable over temperature. These components can be used to temperature compensate by partitioning the temperature range in two, the portion for which the nonlinear current component is (1) zero and (2) non-zero. As a result, the reference voltage (V_{ref}) can be temperature compensated to exhibit a behavior that is graphically described by Figure 5.11. The lower temperature range is basically a first order bandgap, since the nonlinear component (I_{NL}) is zero. At higher temperatures,

the resulting behavior is similar to that of the lower temperatures but the operation is not. The nonlinear behavior of I_{NL} (equivalent to I_{Vbe} - I_{PTAT}) attempts to diminish the effects of the nonlinear term of I_{Vbe}. Consequently, the addition of these two currents (I_{NL} + I_{Vbe}) and I_{PTAT}, at the upper temperature range, generate a curvature corrected trace whose behavior is depicted by V_{ref} in Figure 5.11. Overall, the circuit benefits from being simple, process independent, and appropriate for low voltage operation.

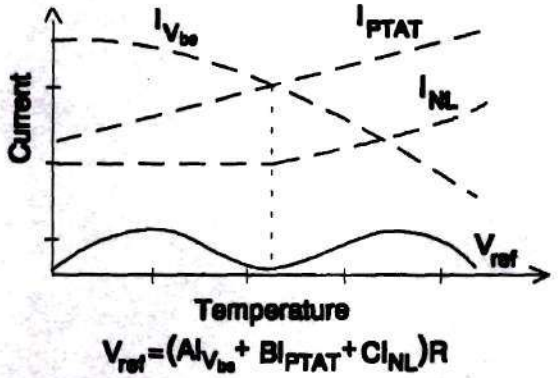


Figure 5.11. Temperature dependence of the curvature corrected bandgap.

5.4 Summary

The chapter has presented the prevailing reference topologies ranging from simple zener realizations to more complex curvature corrected bandgap references. They were evaluated for their temperature drift performance in a low voltage environment. As a result of stringent accuracy requirements, it was concluded that a curvature corrected bandgap reference was necessary. Appropriate output structures were then illustrated culminating in a mixture of voltage and current mode structures (IV-mode), which produced the best combined characteristics. This was followed by a discussion of the different methods of performing curvature correction. These were gauged with respect to low voltage and low quiescent current flow. The least expensive technique in terms of

component count, voltage overhead, and additional quiescent current flow was the current subtraction technique. Therefore, the bandgap circuit implementing the IV-mode output structure and the current subtraction curvature correction method is suitable for low voltage and low quiescent current applications. At this point, the concepts developed in this chapter and those discussed in the previous chapter can be used to do the actual circuit design, whose development is described in the following chapter.

CHAPTER VI

CIRCUIT DESIGN

The problems of low voltage operation typically emerge in the form of voltage headroom, common mode range, dynamic range, and voltage swings. Appropriate design techniques must be therefore implemented to approach the practical low voltage limits of a given process technology. Some of the techniques that are generally recommended are complementary input amplifiers and common source [emitter] gain stages. On the other hand, some of the discouraged techniques are unnecessary cascoding, Darlington configurations, and source [emitter] followers [10]. At the end, however, the choice of circuit topology and configuration depends on the specific application and process technology. The theoretical headroom limit for low voltage operation is a transistor stack of one diode connected device and one saturation voltage drop ($V_{gs}[V_{be}] + V_{ds}[V_{ce}]$), which approximately ranges between 0.9 and 1.1 V in most of today's standard technologies.

The theoretical headroom limit of low voltage for the MOSIS process technology is approximately 1 to 1.1 V (corresponding to $V_{sg\text{-}pmos} + V_{ds\text{-}nmos}$). The threshold voltage of MOS devices in this technology ranges from roughly 0.88 to 0.9 V. The same process also offers a p-base layer for the realization of vertical NPN transistors; however, the respective saturation voltage is large as a consequence of high series collector resistance. The absence of a highly doped buried layer prevents this series resistance from

decreasing to more favorable levels. Consequently, NPN saturation voltages are avoided in transistor stacks that define the headroom limit of low voltage.

In a purely CMOS environment, the absence of NPN transistors tends to yield more complex and/or lower quality circuits. The reference, in such processes, uses available pn junction diodes to generate base-emitter voltages as well as proportional-to-absolute temperature currents (PTAT). In an attempt to fully utilize the technology, however, the threshold implant diffusion (p-type for n-well processes) can be used as a p-type base [46]. As a result, a vertical NPN device can be formulated by using the n+ diffusion as the emitter, the threshold implant diffusion as the p-base, and the n-well as the collector (assuming an n-well technology). The resulting device has the advantage of high forward current gain (β) arising from low base-widths. The drawback, however, is high saturation voltage resulting from the absence of a buried layer, as is the case for the MOSIS technology. This concept can also be exploited in biCMOS technologies to reduce the number of masks required in the process flow. Consequently, relatively inexpensive products can be manufactured. Other device structures that can be utilized in vanilla CMOS processes are lateral and substrate bipolar transistors.

The block level diagram of the proposed low drop-out (LDO) regulator is illustrated in Figure 6.1. The circuit takes advantage of the performance enhancement techniques developed in chapter 4 and the low voltage reference circuit ideas discussed in chapter 5. The pass device is a PMOS composite structure that reaps the benefits of the current boosting technique. The amplifier is composed of a frequency shaping gain stage and a current efficient buffer. The gain stage effectively adds a pole/zero pair to the system's frequency response for the purpose of enhancing load regulation performance. The reference is composed of a low voltage, IV-mode, curvature corrected bandgap and a crude pre-regulator circuit. The output structure of the reference (IV-mode) is a mixture

of a current-mode and a voltage-mode topology. Lastly, a protection circuit block is added for completeness but its design is not included in this chapter. Protection circuitry is discussed in chapter 7 where the assembly of the system is addressed.

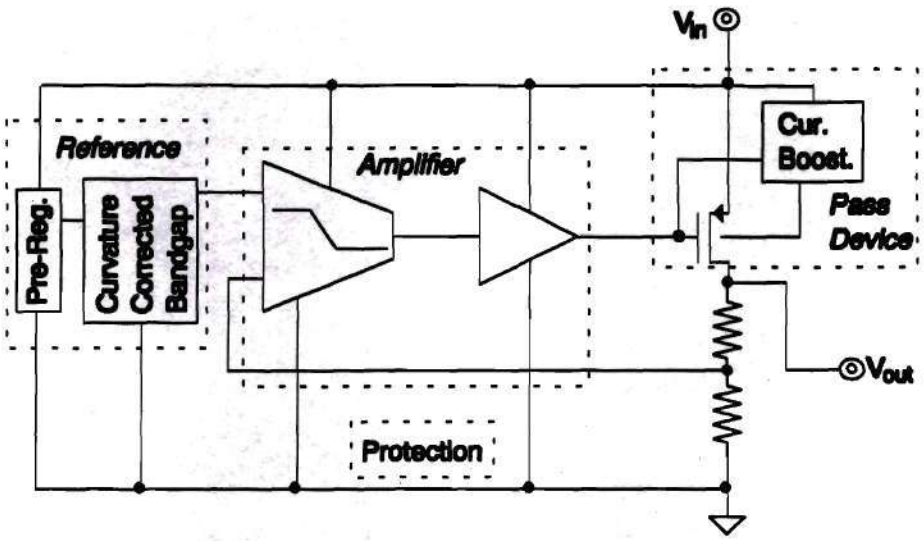


Figure 6.1. Block level diagram of the system.

6.1 Control Loop

Pass Device

The five basic possible configurations for the pass element are illustrated in Figure 6.2, namely, NPN Darlington, NPN emitter follower, common emitter lateral PNP, NMOS source follower, and common source PMOS transistor [4]. The degree of freedom for the choice of topology is dependent on the process technology and the required specifications of the LDO. Multiple transistor structures are also possible candidates for pass devices. However, the intrinsic performance characteristics of these structures revolve around the transistor that actually delivers the output current. The remaining devices can be grouped into the output stage of the error amplifier, otherwise referred as the buffer stage.

Table 6.1 shows a comparison between the different pass elements with respect to their applicable LDO performance parameters. Bipolar devices are capable of delivering the highest output currents for a given supply voltage. The output current capabilities per unit area of MOS transistors exhibit limited performance with high dependencies on aspect ratio and gate drive. However, the voltage driven nature of MOS devices is beneficial in minimizing quiescent current flow. Bipolar transistors are current driven devices with finite forward current gains (β) that can be as low as 20 A/A over process variations. As a result, the error amplifier that drives a bipolar pass element must be able to source or sink relatively high base currents during high load-current conditions. The base current of the NPN transistor, however, flows to the output while that of the PNP counterpart is lost as ground current. Consequently, NPN structures are better suited for low quiescent current designs than PNP realizations. Moreover, the quiescent current flow during drop-out conditions for PNP pass devices can become significantly large. The fastest response, needed for transient load-current steps, is achieved by the NPN structures. PNP transistors, on the other hand, are commonly created as lateral devices and thus exhibit inherently slower response times. Vertical PNP structures yield fast response times but their availability in standard process technologies is limited. MOS transistors are typically slower than vertical bipolar devices but faster than lateral PNP realizations.

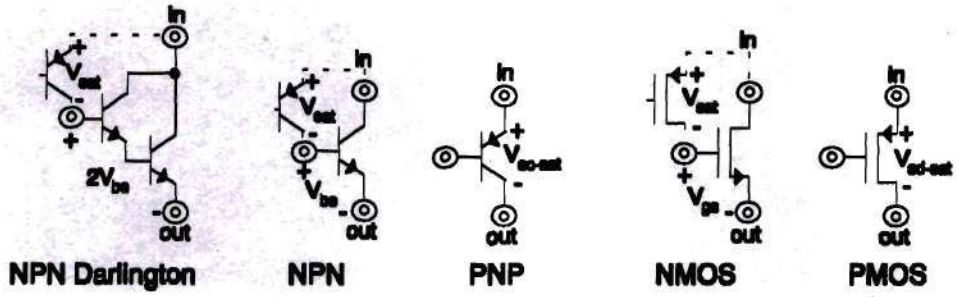


Figure 6.2. Pass element structures.

Table 6.1. Comparison of pass element structures.

Parameter	Darlington	NPN	PNP	NMOS	PMOS
$I_{o\text{-}max}$	High	High	High	Medium	Medium
$I_{quiescent}$	Medium	Medium	Large	Low	Low
$V_{drop\text{-}out}$	$V_{sat}+2V_{be}$	$V_{sat}+V_{be}$	$V_{ec\text{-}sat}$	$V_{sat}+V_{gs}$	$V_{sd\text{-}sat}$
Speed	Fast	Fast	Slow	Medium	Medium

Lowest drop-out voltages are achieved by PMOS ($V_{sd\text{-}sat}$) and PNP ($V_{ec\text{-}sat}$) transistors, approximately between 0.1 and 0.4 V. The NPN Darlington, NPN, and NMOS structures involve at least one V_{be} [V_{gs}] in addition to one $V_{ec\text{-}sat}$ [$V_{sd\text{-}sat}$] with a minimum drop-out voltage of roughly 0.8 to 1.2 V. However, the drop-out voltage of these pass devices can be improved by utilizing a charge pump. The disadvantage of this technique lies in complexity and cost. It requires an oscillator thereby increasing quiescent current overhead, noise injection, and circuit complexity. Excluding the charge pump method, PMOS transistors exhibit the lowest drop-out voltages because of their characteristically variable resistance, V_{sd} changes with gate drive and aspect ratio. On the other hand, PNP devices have a constant saturation voltage of approximately 200 mV. In conclusion, PMOS devices are typically the best overall choice yielding a good compromise of drop-out voltage, quiescent current flow, output current, and speed.

A composite PMOS pass device implementing the current boosting technique discussed in chapter 4 is illustrated in the schematic of Figure 6.3. The size of the schottky diode must be sufficiently large to ensure that its voltage drop is kept below one base-emitter drop. This is to prevent the parasitic vertical PNP transistors inherent in the layout of a PMOS device within an n-well from conducting appreciable currents. The

parasitic collector current flows from the source through the well and finally to the substrate (ground). This phenomenon can be further mitigated by placing a heavily doped buried layer underneath the PMOS device to reduce the forward current gain of the parasitic PNP transistors. The effect of forward biasing this source to bulk junction on the characteristics of the PMOS transistor is lower effective threshold voltage. The width of the metal traces for the source [emitter] and drain [collector] terminals must be large enough to handle the high current density required. Furthermore, series parasitic resistance inherent in the layout must be low to prevent drop-out voltages from significantly degrading, such culprits include the pass device's terminal contacts, metal traces, and diffusion links. The drive requirements of the pass device can generally define the minimum input voltage of the regulator, i.e., the gate drive of the PMOS transistor necessary to yield high output currents and low drop-out voltages ($V_{in} \geq V_{sg} + V_{ds}$, where V_{ds} corresponds to the voltage overhead of a current sink transistor).

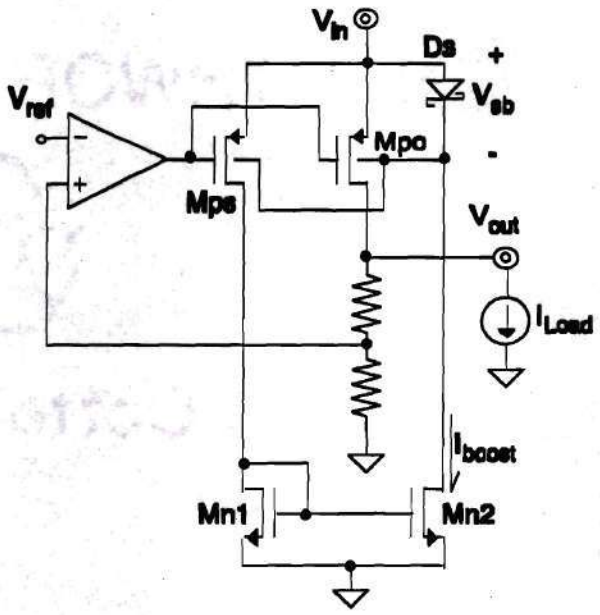


Figure 6.3. Composite PMOS pass device.

Drop-out Handicap: Ground current for the structure shown in Figure 6.3 can become significantly large during drop-out conditions when the nominal output voltage is greater than one V_{gs}. This results because the output PMOS transistor (Mpo) and the sense device (Mps) are in different regions of operations. For instance, if the output voltage is nominally 3.6 V and the input voltage is 3.65 V, then Mpo is in triode (V_{sd} = 0.05 V) and Mps is in saturation ($V_{sd} = V_{in} - V_{gs\text{-}Mn1} \approx 2.2 - 2.65$ V). As a result, the quality of the mirror is degraded and Mps conducts more current than predicted by the mirror ratio, possibly up to 1 mA. This is illustrated by a simulation whose results are shown in Figure 6.4 for a 2 µm CMOS MOSIS design where the current through Mps peaks at roughly 950 µA. Consequently, the source to bulk voltage of the PMOS transistor is increased and the overall current efficiency of the circuit is decreased thereby reducing battery life. The only way to ensure proper mirror operation during drop-out conditions is by forcing the source to drain voltages of Mpo and Mps to be equal.

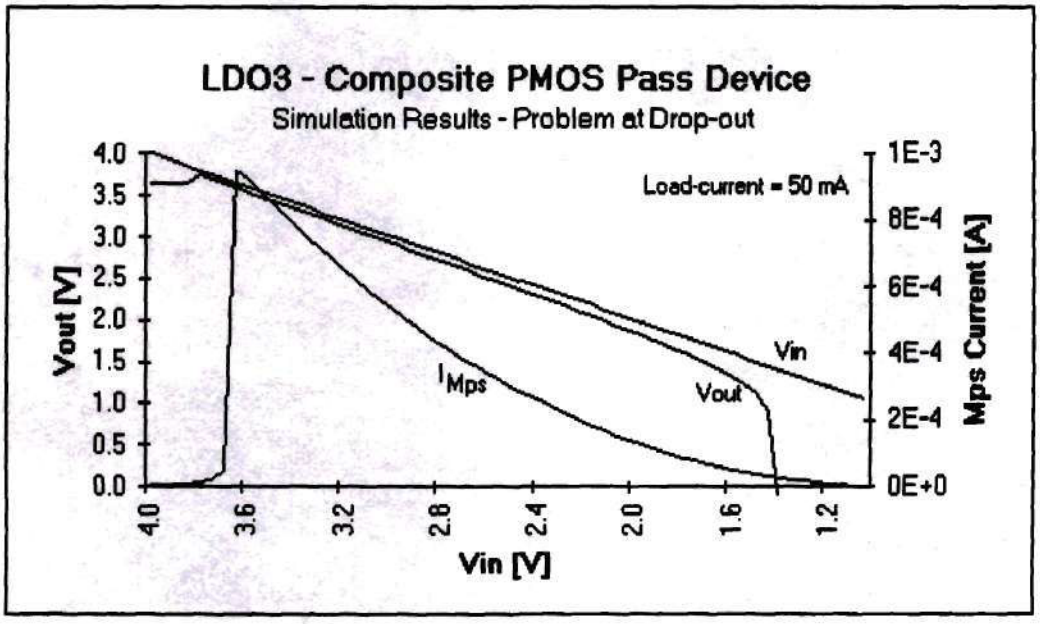


Figure 6.4. Simulation of current sensing problem at drop-out.

Solution: Figure 6.5 illustrates the development of a current replica mirror into a cost-efficient circuit that ensures that Mpo and Mps are in the same region of operation (V_{sg} and V_{sd} for both devices are equal). The concept is to sense the voltage at the output terminal (drain of Mpo) and force that voltage onto the drain of Mps. The lateral PNP transistors (Qp1 and Qp2) in Figure 6.5 (b) are used for this purpose. The drain of the sense transistor is cascoded by a lateral PNP device defining its drain voltage to be equal to that of transistor Mpo via a V_{be} loop. The current used to bias Qp2 can be small,

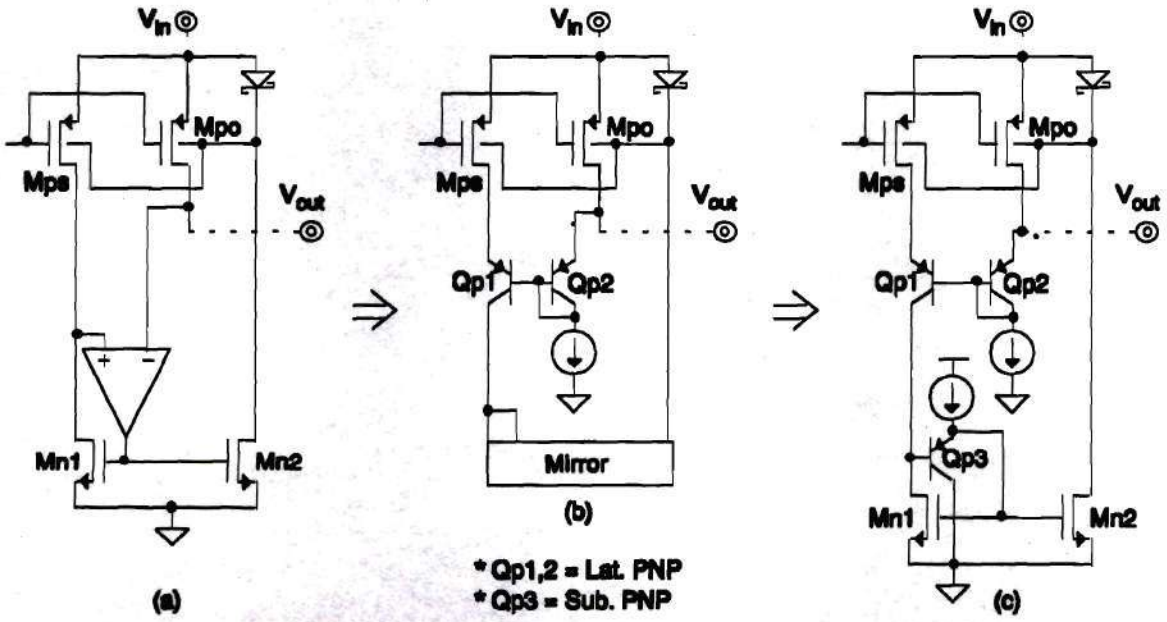


Figure 6.5. Pass device design development for efficient current sensing.

i.e., 0.5 - 1.0 μA. Unfortunately, a regular n-type mirror load for Qp1 is not appropriate for a low voltage environment. For instance, if a standard NMOS mirror is used, then the input voltage is limited to be greater than approximately 1.2 to 1.3 V ($V_{sd\text{-}Mps} + V_{ec\text{-}Qp1} + V_{gs\text{-}Mirror}$). Consequently, a low voltage mirror is necessary for the proper realization

of the circuit. Figure 6.5 (c) shows the final version of the composite PMOS pass device with accurate current sensing capabilities using a low voltage mirror. Transistors Mn1, Mn2, and Qp3 basically constitute a standard mirror with a V_{eb} level shift. The voltage across the drain and source of Mn1 is V_{gs} - V_{eb}, which can be roughly between 0.15 and 0.3 V assuming that $V_{th\text{-}mos}$ is between 0.75 - 0.9 V. Transistor Qp3 can be a substrate bipolar device thereby exhibiting good frequency response and more compact layout characteristics than a lateral device. Simulated results show that the current through Mps is a proper mirror ratio of Mpo, even during drop-out conditions.

Amplifier

The circuit design of an LDO is thoroughly affected by the physical characteristics of the pass device. The pass device must be physically large to yield high output currents and low drop-out voltage characteristics. This translates to a large load capacitance for the error amplifier, characterized as C_{par} in the ac analysis section of chapter 2. Consequently, the parasitic pole at the output of the amplifier is pulled to lower frequencies thereby degrading the phase margin and possibly compromising the stability of the system. Moreover, leakage currents increase as the size of the device increases, i.e., MOS sub-threshold currents. This places an upper limit on device size, a lower limit on quiescent current flow, and/or more stringent requirements on the error amplifier.

Buffer: A buffer is necessary to isolate the gain stage of the amplifier from the large power transistor since the gate of the output pass element is characterized by high capacitance. The idea is to insulate the large capacitor from the large resistance associated with the output of the gain stage. Therefore, the requirements of the buffer are low input capacitance and low output impedance. Furthermore, the output voltage swing needs to extend from as low as possible to the point where it will cause the pass device to discontinue conducting current ($V_{ds} \leq V_{o\text{-}swing} \leq V_{in}$ - 0.7 V). The lower limit is defined

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to provide maximum gate drive for the pass element (PMOS transistor). On the other hand, the upper limit is set by the voltage necessary to shut off the pass device, i.e., extend to just beyond the threshold voltage.

The buffer can be implemented in one of several ways. The most apparent method is through the use of a differential amplifier in a feedback configuration as illustrated in Figure 6.6 (a) and (b). Using a buffer in unity gain configuration demands that the output voltage swing requirements of the gain stage be as stringent as those of the buffer. However, a typical non-unity gain amplifier structure (gain of 5 to 10 V/V) reduces the output swing requirements of the gain stage by a factor equal to the gain of the buffer.

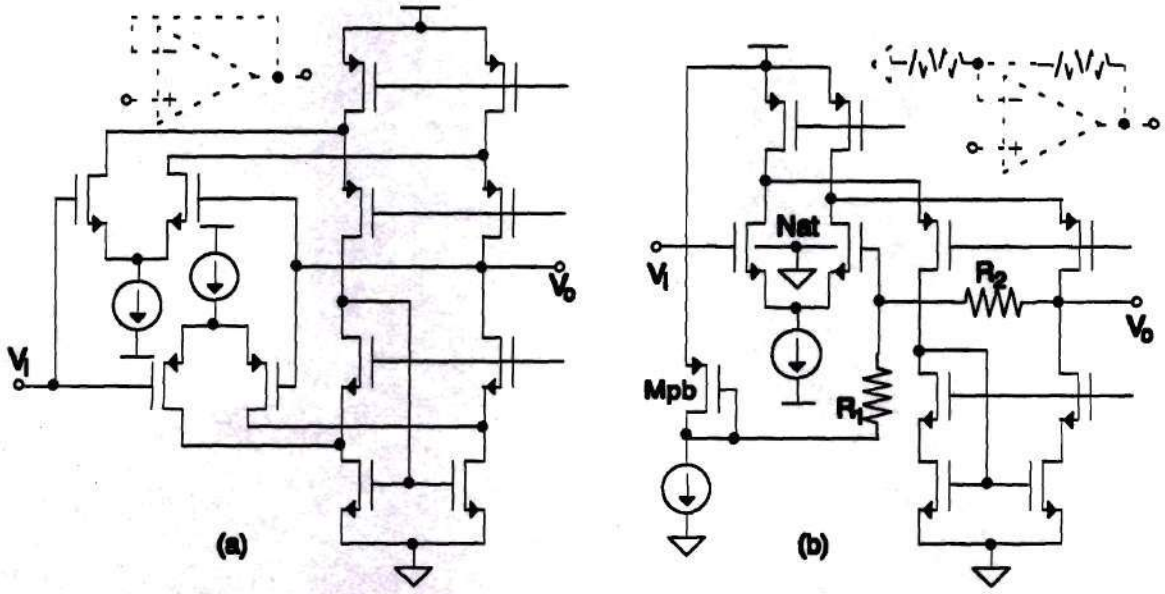


Figure 6.6. Non-inverting amplifier topologies.

This, unfortunately, comes at the expense of chip area and power consumption. In addition to the quiescent current flow associated with several transistor paths to ground, there can be a large current flowing through the feedback resistors at high input voltages. This is because the output voltage of the buffer goes up with increasing input voltage since

its magnitude is defined by the pass device to be one V_{sg} below the input voltage. As a result, the voltage across the grounded resistor in the feedback network is increased accordingly with a current flow equal to $(V_{in} - V_{sg}) / R$, i.e., 90 μA for V_{in} = 10 V, V_{sg} = 1 V, and R = 100 kΩ. Figure 6.6 (b) shows a topology that minimizes the current flow through the resistors by using an alternate ac ground whose dc value is dependent on the input voltage. The low impedance node is defined by a p-type diode connected device (Mpb). The differential pair for this alternate amplifier topology is composed of two natural NMOS transistors (non threshold adjusted devices). The threshold voltage for these natural transistors is approximately zero volts [3] thereby exhibiting good common mode range performance.

Two other amplifier buffer structures are illustrated in Figure 6.7. These circuits exploit the low threshold voltage nature of natural NMOS transistors. The circuit in Figure 6.7 (a) utilizes a current sensing resistor (R) to provide a feedback loop to the current sinking device (Mn2) via an amplifier. The resulting output impedance is

$$R_o = \left\langle \frac{R + r_{ds}}{1 + [R + r_{ds}]g_{m1}} \right\rangle \cdot \left\langle \frac{1}{1 + RAg_{m2}} \right\rangle \approx \frac{1}{RAg_{m1}g_{m2}}. \qquad (6.1)$$

This configuration has a slight advantage over the non-inverting configurations of Figure 6.6, namely, relaxed common mode range requirements for the differential amplifiers. An NPN transistor could also be used in place of the natural NMOS device if voltage swings permit. Figure 6.7 (b) shows a unique configuration where an NMOS transistor is also used as a Channel JFET (CJFET) [47]. The device operates by first creating an inversion layer in response to an applied gate to source voltage. A subsequent change in bulk to source voltage effectively modulates the depletion region. As a result, the inversion layer

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is modulated accordingly thereby causing the drain current to change. The input impedance of the bulk (CJFET's input) is high as long as the bulk to source junction is not forward biased enough to turn on the parasitic bipolar transistors inherent in the device (V_{bs} < 0.5 V). In summary, the circuit takes advantage of the availability of a bulk terminal by using it as a feedback path. Consequently, the resulting device utilizes the gate terminal for forward signal propagation while using the bulk terminal for feedback control. The output impedance of this configuration is derived to be

$$R_o = \frac{r_{ds}}{1+[g_m+g_{mb}]r_{ds}+Ag_{mb}r_{ds}} \approx \frac{1}{Ag_{mb}}. \qquad (6.2)$$

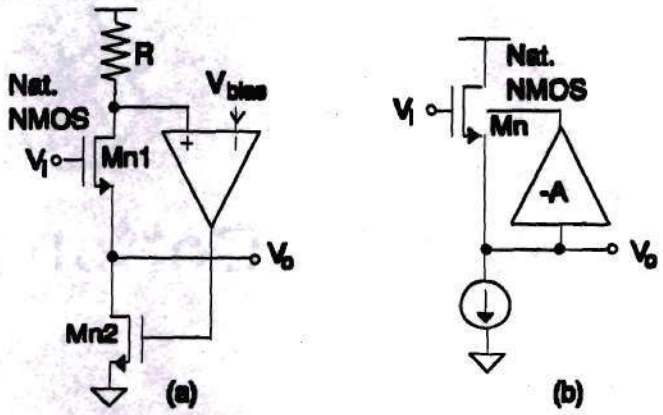


Figure 6.7. Feedback buffer structures.

The disadvantage of this configuration lies in ensuring that the bulk to source voltage of Mn is not forward biased more than 0.4 - 0.5 V. Furthermore, the bulk needs to be isolated from the substrate, which is not readily accomplished in n-well processes. However, this can be done by using a buried layer and deep n+ plugs (typically used for the collector of NPN transistors) in a doughnut configuration. As a result, a p-epi region is isolated in which a natural NMOS device can be built. Isolation can also be achieved by

using the p-base layer of NPN transistors as a p-type well. The device performance, however, is affected by the different well depth and doping density profile of the base relative to the epitaxial region.

The circuits of Figures 6.6 and 6.7 make use of a feedback amplifier to reduce output impedance without incurring excessive costs in quiescent current. However, minimum quiescent current flow is limited by the required bandwidth of the buffer, which constitutes a parasitic pole in the overall frequency response of the system. As a result, current efficiency at low load-currents is adversely affected. If the current efficient buffer introduced in chapter 4 is utilized, however, the need for a feedback amplifier within the buffer is avoided and quiescent current flow is kept at a minimum. The proposed circuit is illustrated in Figure 6.8 where the accurate current sensing circuit developed for the pass device is shared. Consequently, only two additional transistors are required to implement the current efficient buffer, namely, Qn1 and Mn3.

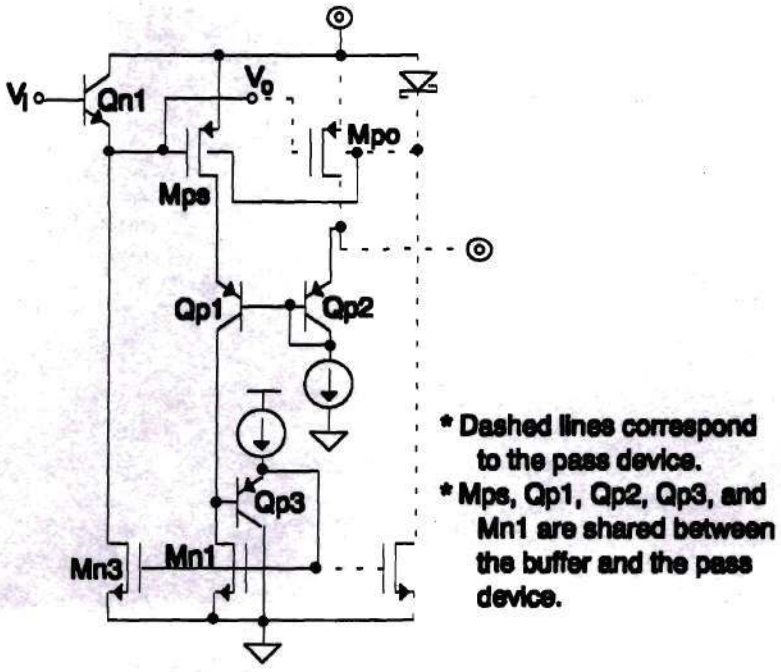


Figure 6.8. Current efficient buffer.

The buffer is essentially a class A NPN emitter follower whose bias current is dependent on load-current. The bias current dependence is achieved by a PMOS sense transistor, labeled Mps in the schematic of the current efficient buffer. Consequently, the parasitic pole introduced by the buffer exhibits the same load-current dependence as the unity gain frequency of the system. In other words, the architecture uses the minimum bias current required for stability throughout the load-current range thereby achieving maximum current efficiency and consequently yielding prolonged battery life. The load-current dependence of the quiescent current is illustrated in the simulation results of Figure 6.9 for a low drop-out regulator implementing the current efficient buffer with a simple, single stage amplifier.

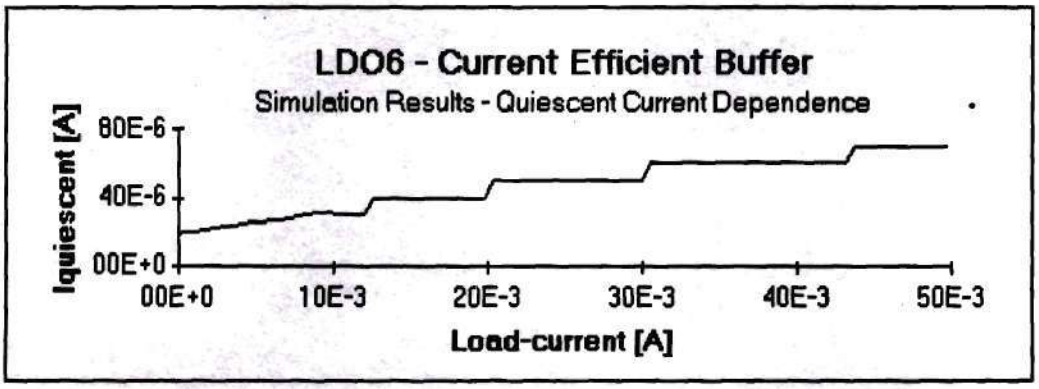


Figure 6.9. Quiescent current dependence of buffer on load-current.

Gain Stage: The gain stage of the amplifier needs a relatively small common mode range and an output swing that includes the positive supply voltage, if the current efficient buffer is assumed to be the load. The common mode range is defined around the reference voltage (V_{ref}), which in turn can be designed to be almost any value [48]. Low voltage bandgap reference topologies are discussed in chapter 5. As a result, the best device choice for a low voltage differential pair is the NPN transistor (for the case of

MOSIS). This is because its base-emitter voltage drop is approximately 0.6 - 0.7 V whereas the gate to source voltage of MOS devices is roughly 0.9 V. Thus, a 0.85 - 0.9 V reference is necessary to accommodate the voltage headroom requirements of the NPN differential pair in a low voltage environment.

The choice of amplifier topology, however, is limited if the theoretical low voltage limit is to be approached ($V_{sg} + V_{ds}$). Figure 6.10 illustrates some appropriate amplifier topologies where the pole/zero pair generation discussed in chapter 4 is realized by the dashed resistor and capacitor. The single stage, five-transistor amplifier shown in Figure 6.10 (a) is simple enough to yield good frequency response for a given amount of quiescent current flow. However, a regular current mirror load presents a problem for low voltage operation. A regular mirror load, as seen in the figure, yields a transistor stack whose associated voltage drop is $V_{sg} + V_{ce} + V_{ds}$, which is approximately between 1.4 and 1.5 V in the MOSIS technology. Therefore, a low voltage mirror load that yields the theoretical low voltage limit for the MOSIS technology is proposed ($V_{sg} + V_{ds} \approx 1$ - 1.1 V) and illustrated in Figure 6.10 (b). The mirror is the complement of the version used in the composite PMOS pass device and current efficient buffer. It is essentially a standard mirror with a V_{be} level shift achieved by an emitter follower. The current through the NPN device is designed such that the parasitic pole at the gate of the PMOS transistor is at high frequencies. This parasitic pole ($P_{parasitic}$) is approximated to be

$$P_{parasitic} \approx \frac{g_{m_{npn}}}{2\pi} \cdot \frac{1}{2C_{gs}}, \tag{6.3}$$

where $g_{m_{npn}}$ is the transconductance of the NPN transistor and C_{sg} is the gate to source capacitance of each PMOS device in the mirror. Among the amplifiers in Figure 6.10, this

topology exhibits the best systematic offset performance because the voltages at the collectors of both NPN transistors in the differential pair are the same, V_{in} - V_{sg} + V_{be}. This results because the voltage at the input of the buffer stage (or output of the gain stage) is defined by a PMOS pass device and an emitter follower, as seen in the current efficient buffer shown in Figure 6.8. Another possible topology for the amplifier is that of a folded architecture, Figure 6.10 (c). This circuit also works properly at the theoretical limit of V_{gs} + V_{sd} (equivalent to V_{sg} + V_{ds}). However, systematic offset performance for this circuit is poor. Furthermore, bandwidth performance per given total quiescent current flow is not as favorable as that of the circuit shown in Figure 6.10 (b) because there are more current sensitive transistor paths to ground.

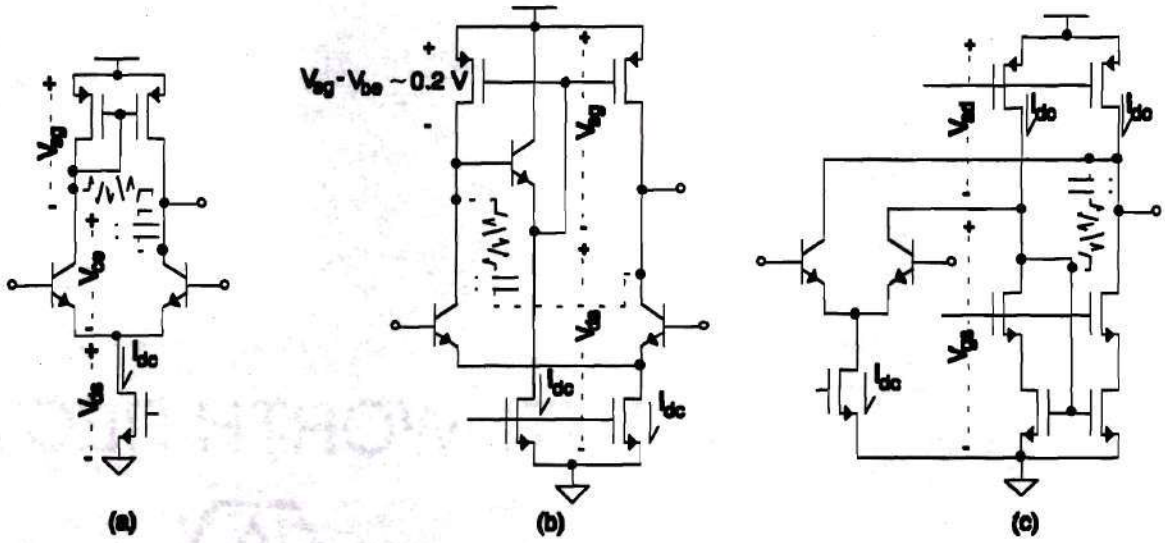


Figure 6.10. Gain stage topologies.

6.2 Reference

Current Components

An IV-mode output structure, curvature corrected bandgap reference is illustrated in Figure 6.11 (a). The proportional-to-absolute temperature (PTAT) current component

is realized by Qn1, Qn2, Qn3, and R_p, which constitute a typical V_{be} loop. The base-emitter dependent current is defined by the base-emitter voltage of Qn3 and R_b. This is controlled by the negative feedback loop comprised of Qn3, Qn5, and the PMOS current mirror of Mpb1 and Mpb2. Capacitor C_c and resistor R_c are used to frequency compensate this internal feedback loop thereby ensuring stability, miller compensation. In designing the values of the capacitor and the resistor, the additional loop path composed

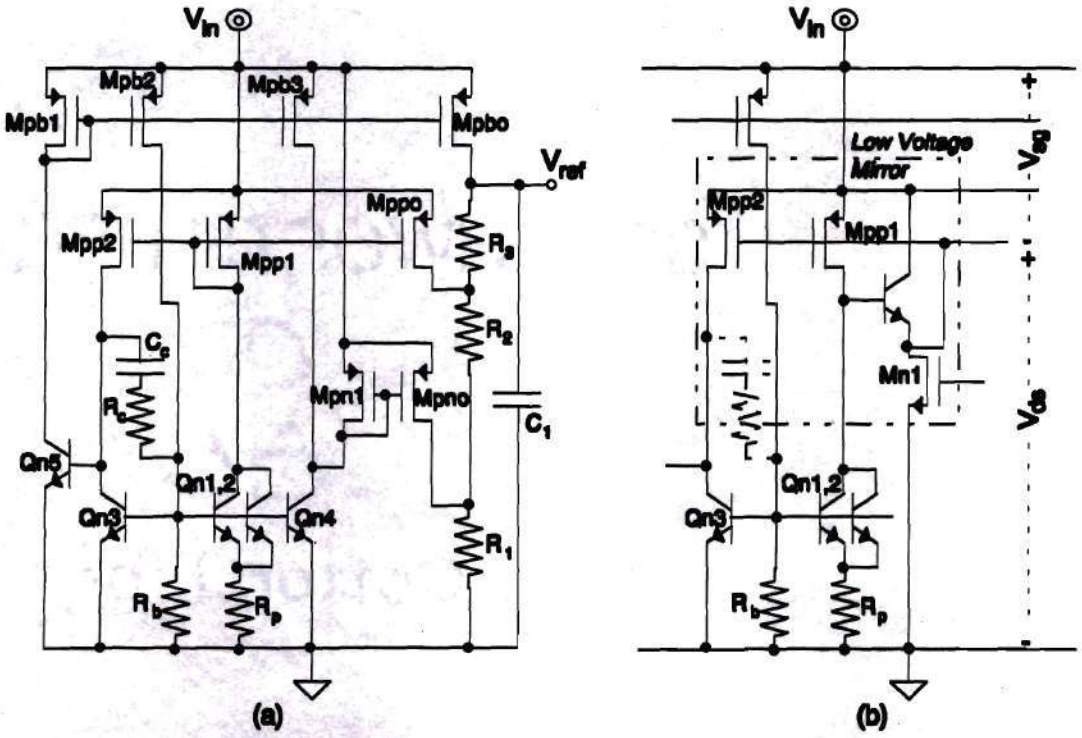


Figure 6.11. Bandgap with current subtraction curvature correction.

of Qn1, Qn2, Mpp1, and Mpp2 must be considered. Capacitor C_1 is used to limit the noise bandwidth of the reference circuit thereby reducing the overall noise content at the output of the regulator, in other words, enhancing noise performance. Finally, the nonlinear temperature dependent current is formed by Qn4 (PTAT current sink), Mpb3 ($I_{V_{be}}$ current source), Mpn1, and Mpno, which implement the current subtraction

technique discussed in chapter 5. Transistors Qn3 and Qn4 constitute a linear current mirror and so do transistors Mpb1, Mpb2, and Mpb3. A resistor could be placed between the emitter of Qn4 and ground thereby making a linear current mirror with Qn1, Qn2, and R_p. The circuit simulated to have a temperature drift performance of 3.1 μV/°C and is illustrated in Figure 6.12.

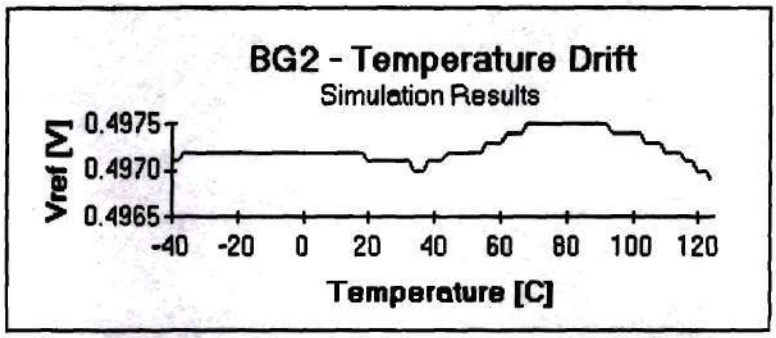


Figure 6.12. Temperature drift performance of the bandgap reference.

The realization of this circuit in MOSIS 2 μm CMOS n-well technology with a p-base layer can benefit from the use of the low voltage mirror used in the gain stage of the amplifier of Figure 6.10 (b). The minimum input voltage ($V_{in\text{-}min}$) for the bandgap cell in Figure 6.11 (a) is

$$V_{in-min} = V_{sg-Mpp1} + V_{ce-Qn1} + V_{R_p}, \qquad (6.4)$$

where the voltage across R_p is relatively small, Mpp1 is in sub-threshold, and $V_{ce\text{-}Qn1}$ is approximately 0.3 V. The high saturation voltage of the NPN transistor is inherent to technologies that do not offer a heavily doped buried layer, which is the case for MOSIS. The buried layer effectively decreases the series collector resistance. Figure 6.11 (b) illustrates the circuit implications of adopting a low voltage current mirror for all PMOS

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mirrors used in the schematic shown in Figure 6.11 (a). The new corresponding minimum input voltage is

$$V_{in-min} = V_{sg-Mpp1} + V_{ds-Mn1}, \quad (6.5)$$

where Mn1 is simply used as a current source. Consequently, the minimum input voltage is improved by isolating the high saturation voltage of the NPN transistor from the transistor stack that determines the voltage headroom limit, which corresponds to an improvement of roughly 100 - 150 mV over the previous circuit. Thus, the minimum input voltage limit for weak-to-moderate inversion operation can be as low as 0.9 V in the MOSIS process technology. Unfortunately, the drawback is that the temperature stability of the reference is degraded because at high temperatures the input PMOS transistor, Mpp1 in Figure 6.11 (b), can go into the triode region. This results because the base-emitter voltage of the NPN device in the mirror drops faster with temperature than the source to gate voltage of the PMOS transistor. As a result, the voltage across the source and drain terminals of Mpp1 is significantly decreased at high temperatures. When this occurs, the accuracy of the mirrors defining the temperature dependent currents is reduced, which in turn degrade the ability to minimize output voltage variations throughout the specified temperature range. Consequently, reducing the minimum input voltage of this cell from roughly 1 to 0.9 V comes at the expense of accuracy.

Line Regulation Enhancement

The straight forward implementation of the current-mode bandgap relies on the high and finite output impedance of the current mirrors. Consequently, the output voltage varies as the input voltage changes because of the finite output impedance of the transistors sourcing the currents. One way to increase this output impedance is by actively