cascoding the mirrors. However, a more effective method is to pre-regulate the supply voltage of the bandgap, as illustrated in Figure 6.13, which is similar in concept to the circuit in [13]. As a result, line regulation performance is ameliorated. The pre-regulator basically provides a first order voltage-mode bandgap reference. The current through the diode connected transistor (q_1) and the resistor (R_2) is proportional-to-absolute temperature (PTAT). Consequently, the pre-regulated supply voltage of the bandgap is equal to a diode on top of a PTAT voltage drop. The disadvantage of this circuit is that the common mode range of the amplifier needs to include ground and approximately 0.5 - 0.6 V above ground, corresponding to a pre-regulated supply of 1.1 - 1.2 V. This would require the use of a complementary input amplifier to yield the desired common mode range in a low voltage environment, 1 - 1.5 V. Moreover, complementary differential pair amplifiers tend to limit the power supply voltage to approximately 1.3 V ($V_{be\text{-}NPN} + V_{eb\text{-}PNP}$) or 1.5 V ($V_{gs\text{-}NMOS} + V_{sg\text{-}PMOS}$) [47].

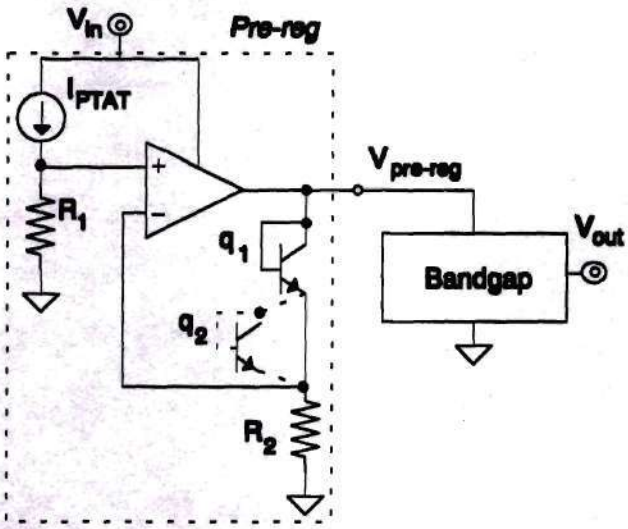


Figure 6.13. Pre-regulated supply voltage realization.

On the other hand, the pre-regulator does not need to be well temperature compensated. The current mirrors in the bandgap will have high enough output impedance to effectively reject small voltage fluctuations experienced by the pre-regulated supply ($V_{pre\text{-}reg}$). Therefore, an appropriate variation of the circuit discussed would be to use two diodes instead of one; this corresponds to adding q_2 in Figure 6.13. As a result, a more crude and less expensive circuit is achieved (in terms of complexity and component count for the amplifier). The voltage across the resistor needs to be small thereby only requiring the use of a simple PMOS differential pair in the feedback amplifier. The new pre-regulated supply ($V_{pre\text{-}reg}$) is the sum of two diode-connected NPN transistors with PTAT collector current and one small PTAT voltage drop. This corresponds to a first order bandgap with poor temperature compensation. It is noted that $V_{pre\text{-}reg}$ (in both circuit versions) begins to decay as the input voltage approaches 1.1 - 1.2 V. Consequently, the effective line regulation of the bandgap exhibits its worst performance when the input voltage is lower than 1.2 V. Lastly, the minimum input voltage of the overall reference circuit is only degraded by one $V_{sd\text{-}sat}$ incurred between the input voltage and the pre-regulated supply. As a result, the minimum input voltage for the complete circuit is roughly 1 to 1.1 V for the MOSIS technology. Cascoding the current mirrors would have had the same effect on the minimum input voltage.

The implementation of the overall circuit is illustrated in Figure 6.14. The effects of the pre-regulated supply on line regulation performance are illustrated in Figure 6.15, 1.8 mV / 9 V and 175 mV / 9 V for the circuit with and without the pre-regulator. All the resistors can be made of any material as long as they are all the same type. Base-diffusion resistors are recommended because of their high sheet resistance and their ability to be isolated from the substrate via a well. The capacitors can be stacked to minimize area, i.e., second polysilicon layer (poly 2), first polysilicon layer (poly 1), and base-diffusion

Aptiv Services US, LLC Exhibit 1015 Page 132

capacitors with poly 1 as one terminal and poly 2/base-diffusion as the other terminal. The n-well insulating the capacitor and the resistors can be connected to the pre-regulated supply for minimized line regulation effects. The p-channel JFET can be implemented with a long p-base as the channel, n+ diffusion as the top gate, and n-well as the bottom gate; the top and bottom gates are electrically shorted together. The only purpose of the JFET is to provide some current for the start-up circuit to work, between 0.5 and 3 μA. The operation of the start-up circuit is based on sensing the base-emitter voltage of the NPN transistors generating and defining the temperature dependent currents and ensuring that they are operating at a non zero state by feeding back a current, typical concept of bi-stable start-up circuits.

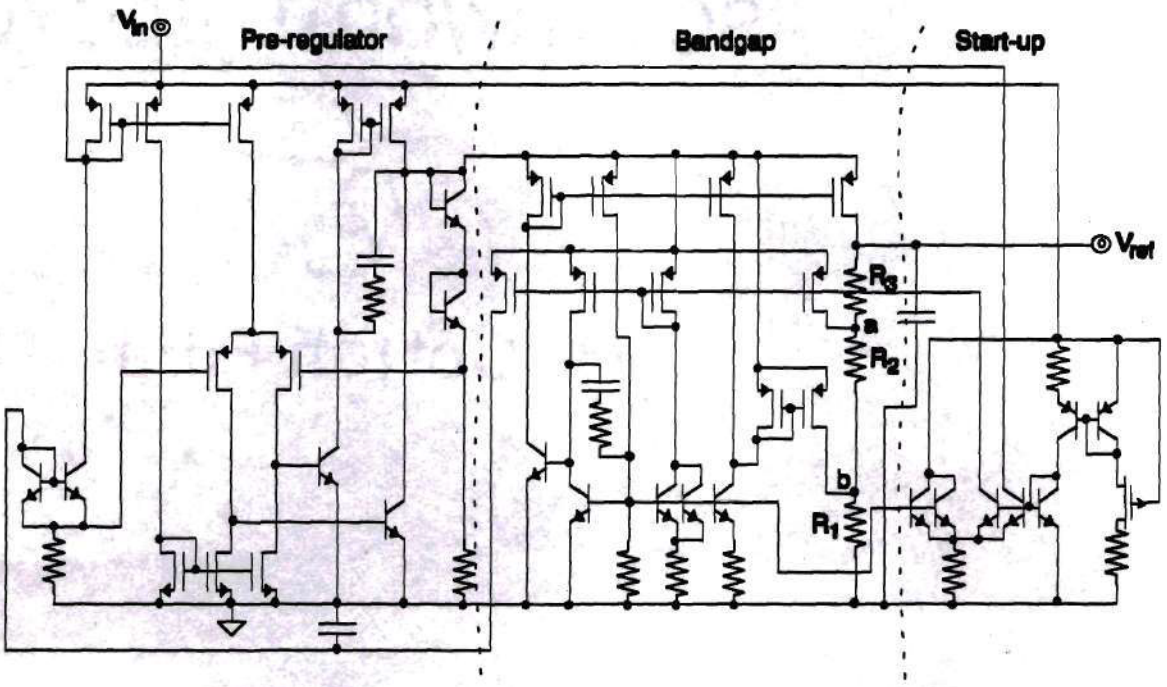


Figure 6.14. Low voltage curvature corrected bandgap.

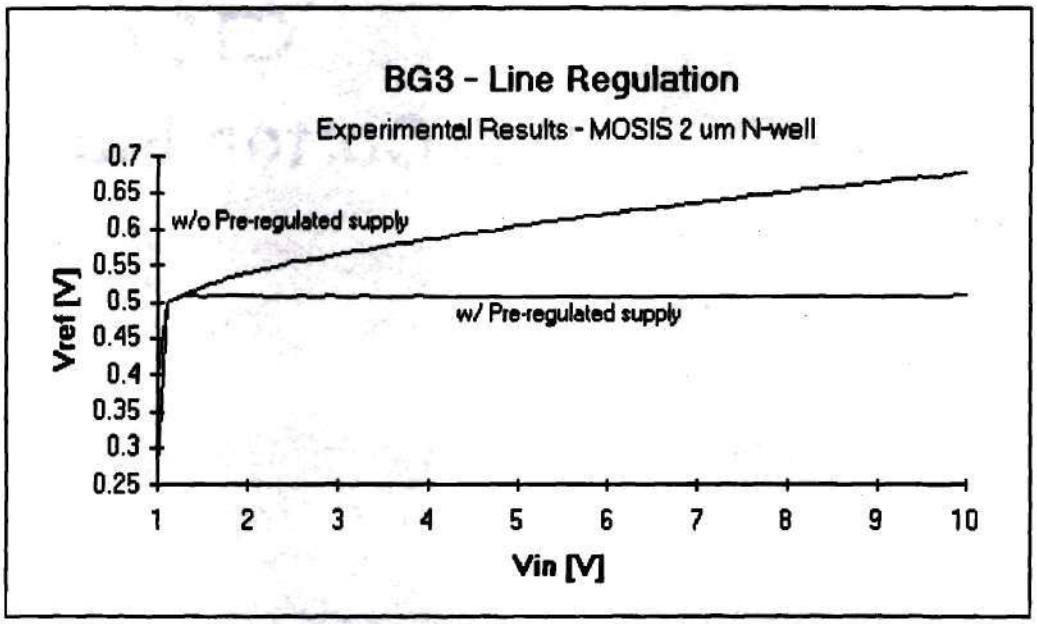


Figure 6.15. Line regulation performance of the bandgap with and without the pre-regulator.

Trimming

The output voltage as well as the temperature coefficients of the individual components can be trimmed by simply changing the resistor ratios at the output. Temperature compensation is achieved by trimming throughout the temperature range. Data points are collected for the voltages at V_{ref}, node "a", and node "b" (from Figure 6.14) throughout the temperature sweep. At this point, the currents multiplied by an initial reference resistor can be extrapolated since the initial resistor ratios and the voltages across the resistors are known,

$$I_{V_{be}} R_{2_{initial}} = \frac{V_{ref} - V_a}{\left\langle \frac{R_3}{R_2} \right\rangle_{initial}}, \qquad (6.6)$$

$$I_{PTAT} R_{2_{initial}} = [V_a - V_b] - I_{V_{be}} R_{2_{initial}}, \tag{6.7}$$

and

$$I_{NL} R_{2_{initial}} = \frac{V_b}{\left\langle \frac{R_1}{R_2} \right\rangle_{initial}} - [V_a - V_b], \tag{6.8}$$

where $I_{V_{be}}$, I_{PTAT}, and I_{NL} are the temperature dependent currents flowing through the output resistors R_1, R_2, and R_3 while V_a and V_b correspond to the voltages at nodes "a" and "b". These derived voltages exhibit temperature characteristics that are independent of the temperature coefficient of the resistors, as discussed in the IV-mode output structure section of chapter 5. Thus, the coefficients of each component can be extracted and manipulated to yield proper temperature compensation by means of a computer. The reference voltage can be expressed as

$$V_{ref} = I_{V_{be}}[R_1 + R_2 + R_3] + I_{PTAT}[R_1 + R_2] + I_{NL} R_1. \tag{6.9}$$

This relationship can be adjusted to use the values derived in equations (6.6) - (6.8) and illustrate the appropriate coefficients that can be manipulated to yield a curvature corrected reference voltage,

$$V_{ref}\frac{R_{2_{initial}}}{R_2} = I_{V_{be}}\left\langle\frac{R_1}{R_2}+\frac{R_2}{R_2}+\frac{R_3}{R_2}\right\rangle R_{2_{initial}} +$$

$$I_{PTAT}\left\langle\frac{R_1}{R_2}+\frac{R_2}{R_2}\right\rangle R_{2_{initial}} + I_{NL}\left\langle\frac{R_1}{R_2}\right\rangle R_{2_{initial}}, \qquad (6.10)$$

or $$V_{ref}\frac{R_{2_{initial}}}{R_2} = AI_{V_{be}}R_{2_{initial}} + BI_{PTAT}R_{2_{initial}} + CI_{NL}R_{2_{initial}} \qquad (6.11)$$

where A, B, and C are the extracted coefficients. Once values for these coefficients are obtained by using a computer, new resistor ratios for R_1/R_2 and R_3/R_2 can be derived.

The next and final step in the trimming procedure is to adjust the magnitude of the output voltage at room temperature or at whatever temperature desired. This can be accomplished by changing the ratio of the initial and the final values of R_2 ($R_{2_{initial}}/R_2$). This value is determined by using the resistor ratios previously derived and the voltages obtained at room temperature (V_{ref}, $I_{V_{be}}R_{2_{initial}}$, $I_{PTAT}R_{2_{initial}}$, and $I_{NL}R_{2_{initial}}$) and solving for $R_{2_{initial}}/R_2$. It is noted that knowledge of the absolute value of the resistors is not necessary. Instead, the intrinsic parameters that require control are the ratios of the resistors. The trimming algorithm has been successfully implemented by way of a spreadsheet and whose procedure is described in appendix B.

The procedure not only trims the absolute magnitude of the reference but it also performs temperature compensation. The disadvantage of this algorithm lies in the cost involved, namely, spending the time and allocating the equipment to trim the circuit over a specified temperature range. This could be avoided by only trimming for the voltage magnitude at room temperature and relying on simulations for proper temperature

Aptiv Services US, LLC Exhibit 1015 Page 136

compensation. Typical trimming procedures only do the latter. Furthermore, the aforementioned trimming technique can optimize temperature compensation for any set of current components independently of their individual temperature dependencies by merely adjusting resistor ratios at the output.

6.3 Summary

This chapter used the concepts developed in chapters 4 and 5 to design the circuits for the control loop and the reference of the system. Different devices were considered for the pass device leading to the conclusion that PMOS transistors are the most appropriate for low drop-out voltage performance and low quiescent current flow. This was followed by the implementation of the current boosting technique. Different architectures were also studied for the buffer of the amplifier. This culminated in the realization of the class A current efficient buffer. A circuit was also designed for the frequency shaping gain stage. The circuit development of the reference was then addressed. Lastly, the chapter discussed the trimming implications of the reference circuit designed. The process of translating the circuit blocks designed into a system is described in chapter 7.

Aptiv Services US, LLC Exhibit 1015 Page 137

CHAPTER VII

SYSTEM DESIGN

In assembling the circuits onto a system, there are several issues that need special attention. Physical layout design and circuit protection techniques are two such issues. General layout notes pertaining to the circuit blocks and associated interconnects are therefore discussed in this chapter. A section is also allocated to illustrate the different methods of protection, such as overload current, reverse battery, and thermal protection. Their feasibility in a low voltage and low quiescent current environment is evaluated. Lastly, experimental results of the system designed are illustrated and evaluated.

7.1 Block Level Diagram

The low voltage and low quiescent current circuits developed in chapters 4 and 5 and designed in chapter 6 are used to assemble the system illustrated in Figure 7.1. The reference is composed of a pre-regulator and a curvature corrected bandgap cell. There is also a start-up circuit associated with the overall reference. The amplifier is composed of a frequency shaping gain stage and a current efficient buffer. The pass device is a PMOS power transistor whose performance is enhanced by a current boosting circuit. Part of the circuit forming the pass device is common to the current efficient buffer but is distinctly separated in the figure for clarity. Finally, three common forms of protection are included in the drawing. They include overload current protection, reverse battery protection, and

Aptiv Services US, LLC Exhibit 1015 Page 138

thermal shutdown protection. As a whole, they ensure that the system operates under safe and stable conditions. Most of the protection, however, revolves around the power transistor. This is because the pass device is usually the most susceptible to extreme environmental and loading conditions.

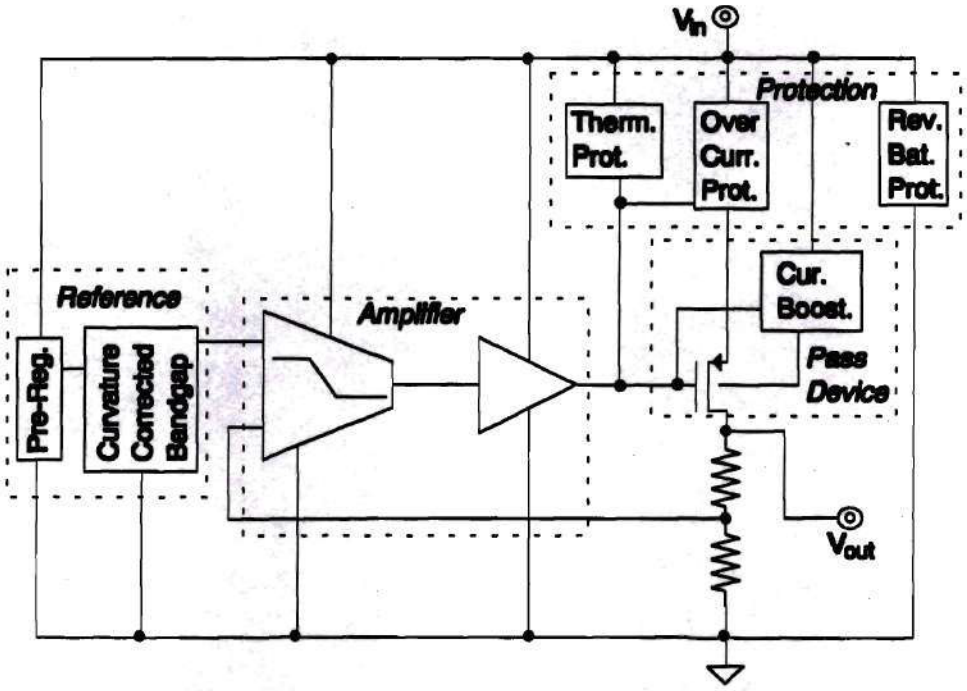


Figure 7.1. Complete system block level diagram.

7.2 Physical Design Issues

The effects of parasitic devices inherent in the layout could prove to be catastrophic for the overall performance of the system. This is especially true when considering the current density, the power dissipation, and the generated heat associated with power supply circuits. Furthermore, stray capacitance, parasitic resistance, and lead inductance can affect the system by altering the frequency response behavior and possibly causing spurious oscillations [21]. As a result, the layout should be compact and lead

lengths should be kept short. Moreover, ground loops must be avoided [19]. Their effects can be mitigated by careful element placement and by ensuring that ground contacts and interconnect paths are low resistance. Heat distribution, especially throughout the area where the power transistor lies, also deserves attention. This is to prevent "hot spots" from being generated on the power device that could cause second breakdown. Moreover, reliability issues with current density in the input and the output terminals of the regulator are intrinsic to the life of the circuit.

The output noise of the system can be significantly degraded by poor layout techniques, especially in mixed-signal integrated circuits. Digital functions in mixed-signal chips are significant sources of noise for analog circuits. They exhibit large momentary surges of current that produce noise on the supply lines and the substrate. Two techniques that are appropriate for minimizing this injected noise are separation of power supply lines and physical layout isolation of circuits. The digital and analog supply lines can be separated throughout the chip and connected externally or at the package level [19]. This is to prevent most of the noise voltage generated by the large surges of current flowing through stray inductors and parasitic resistors from appearing in the analog lines. Isolation can be used to relieve the noise injected through the substrate. This can be realized by placing a deep diffusion ring around the analog circuits and by placing the analog traces as far away as possible from any digital line. Noise at the load is also negatively affected by series lead inductance and resistance. This noise manifests itself in the form of voltage drops across the line resulting from dc and transient load-current changes ($\Delta I_{Load}R_{Lead} + L_{Lead}\partial I_{Load}/\partial t$). Thus, this type of noise is reduced by keeping the output lead to the load short and by reducing its resistance [19].

Almost all parasitic devices in the power pass device serve to degrade the overall performance of the low drop-out regulator. Series source and drain resistance associated

Aptiv Services US, LLC Exhibit 1015 Page 140

with the metal traces, diffusion links, and contacts increase the drop-out voltage; in other words, they increase the "on" resistance of the transistor. Thus, low resistive paths for the source and drain terminals are necessary. The parasitic capacitance of the gate of the power PMOS is especially important for system stability. The result of increased capacitance can be spurious oscillations. Consequently, unnecessary gate area should be eliminated. The parasitic effects of the bipolar transistors inherent in the power PMOS transistor are especially apparent when the source to bulk junction is forward biased, which is done for current boosting. Therefore, a highly doped buried layer, if available, should be placed underneath the whole device to decrease the current gain of the parasitic bipolar transistors as well as decrease the bulk resistance. Well contacts should be placed throughout the device to aid in reducing bulk resistance. Lower bulk resistance prevents excessive bulk to source forward biasing conditions thereby minimizing the parasitic effects of the bipolar devices. Furthermore, the size of the schottky diode used to forward bias this junction needs to be large enough to exhibit a voltage drop that is well below a base-emitter voltage, i.e., $V_{schottky} \approx 0.3$ V. This leads to a reduction in unnecessary ground current. Consideration must also be given to thermal symmetry of the overall physical layout. The power device may be divided in two and the other circuit blocks may be placed in the center. Moreover, current densities must be equally distributed throughout the pass device to prevent "hot spots" from developing.

The placement and particular layout of the reference and error amplifier also require scrutiny. The reference circuit should be close to the input of the amplifier. This is especially true for the output capacitor of the reference. This is to reduce the noise content generated by the reference circuit and parasitic trace resistance, which is seen by the input of the amplifier and reflected to the output of the regulator. The location of the reference with respect to the overall chip also merits consideration. This influences the

package induced drifts. The variation of the reference voltage is degraded by the physical stresses exerted on the chip by the package. These effects can be minimized if post-package trimming is allowed. The input pair and the mirror load of the amplifier's gain stage should be well matched to minimize input offset voltages, which degrade overall accuracy performance. The integrated capacitors utilized throughout the chip can be stacked to minimize area overhead. These capacitors are implemented by using three parallel plates (poly 2, poly 1, and p-base diffusion) isolated by an n-well. The bottom plate (p-base diffusion) and the top plate (poly 2) are electrically shorted together and constitute one terminal of the capacitor; the other terminal is the middle plate (poly 1). The terminal composed of the extreme plates should be connected to the lowest impedance node to minimize the effects of the innate parasitic capacitance to the n-well. The output of the gain stage and the input of the buffer should be as close as possible. This is to reduce stray capacitance that could pull the respective parasitic pole to low frequencies. Similarly, the buffer should be placed as close as possible to the power PMOS pass device. This not only affects stability by pole movement but also affects maximum output voltage variation arising from transient load-current steps by degrading slew-rate performance. It is important to keep in mind, however, that the gate capacitance associated with the power transistor usually overwhelms the interconnect capacitance between the buffer and the pass device.

The location and the layout of the protection circuits should reflect minimal effects on regulator performance. The current sensing device associated with the overload current protection is typically a series element. Thus, its associated voltage drop must be minimized to prevent it from significantly increasing drop-out voltage. As a result, low resistive terminals capable of handling large current densities should be implemented for the current sense device. Lastly, the temperature sensing element associated with thermal

shutdown protection should be placed as close as possible to the power device to ensure proper operation of the protection circuit.

7.3 Protection

An important aspect to consider when designing regulators is protection against undesirable factors that are inherent to the working environment of the application. Since the power pass device dissipates the most power, protection usually revolves around its operating conditions. The operating limits of the device are defined by power dissipation, output current range, breakdown voltage, temperature rating, and second breakdown effects [1]. Second breakdown results from the presence of "hot spots" or large thermal gradients, a consequence of uneven distribution of current densities throughout the power transistor. Protection circuitry is typically inactive during safe operating conditions and becomes active only if a safety limit is violated. The most common forms of protection include overload current protection, reverse battery protection, thermal shutdown protection, and electrostatic discharge (ESD) protection. The safety limits of output current and voltage drop across a transistor are combined to describe the safe operating area (SOA), typically illustrated by a graph of $V_{ec}[V_{sd}]$ versus $I_c[I_d]$ [21]. Protection against overheating, current overloading, and extreme voltages constitute the "watchdog" circuitry otherwise known as SOA protection. In other words, SOA protection ensures that the power transistor works within safety limits. Most of these circuits are realized easily and in a cost efficient manner. However, caution must be exercised not to significantly degrade the performance of the regulator during normal conditions by the mere presence of the protection. For instance, current limiting typically requires a current sense resistor in series with the power transistor. As a result, the drop-out voltage of the regulator is deteriorated by the load dependent voltage drop across the resistor.

Aptiv Services US, LLC Exhibit 1015 Page 143

Overload Current Protection

Overload protection ensures that the current through the power transistor stays within a specified range. A violation of this could result in damage or destruction of the device. The simplest form of overload current protection is a fuse-link [49]. When the load-current exceeds the rated current of the fuse, the heat generated melts the metallic link thereby causing an open circuit. The drawback of this method is that replacement of the link is necessary once the fuse is blown, which is not acceptable for most integrated power supply applications. Figure 7.2 (a) illustrates a more appropriate structure for integrated circuits [1, 2, 3, 6]. The maximum current is defined by the bipolar transistor and the resistor, $I_{o\text{-}max} = V_{be} / R_s$. Transistor Qn1 [Qp1] is off during normal operating conditions. However, when the load-current increases to the point where the voltage drop across R_s is roughly 0.7 V (equivalent to one V_{be}), then the transistor conducts current.

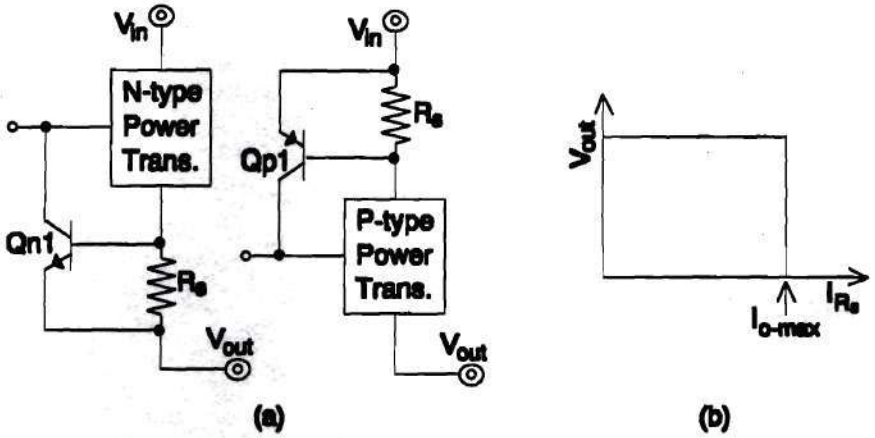


Figure 7.2. Current limiting circuit protection.

The device pulls down [pulls up] the input terminal of the power device to prevent it from conducting more current. The resulting voltage to current relationship is illustrated in Figure 7.2 (b). The maximum power dissipation of the power transistor occurs when the

output is short circuited to ground, which corresponds to a voltage drop across the device equal to the input voltage,

$$P_{o-max} = [V_{in} + V_{out}] I_{o-max} = V_{in} I_{o-max}, \tag{7.1}$$

where the terminology of the figure is adopted. One disadvantage of this configuration is the deterioration of the drop-out voltage by the voltage drop across the resistor R_s.

The drop-out voltage loss can be minimized by implementing the circuit of Figure 7.3 (a) [6, 50]. In this case, R_s can be small because the threshold voltage (voltage across R_s, $V_{threshold}$) needed to activate the protection circuit can be defined to be small by appropriately proportioning resistors R_1 through R_4,

$$V_{threshold} = V_{in}\left\langle 1 - \frac{R_2[R_3+R_4]}{R_4[R_1+R_2]}\right\rangle. \tag{7.2}$$

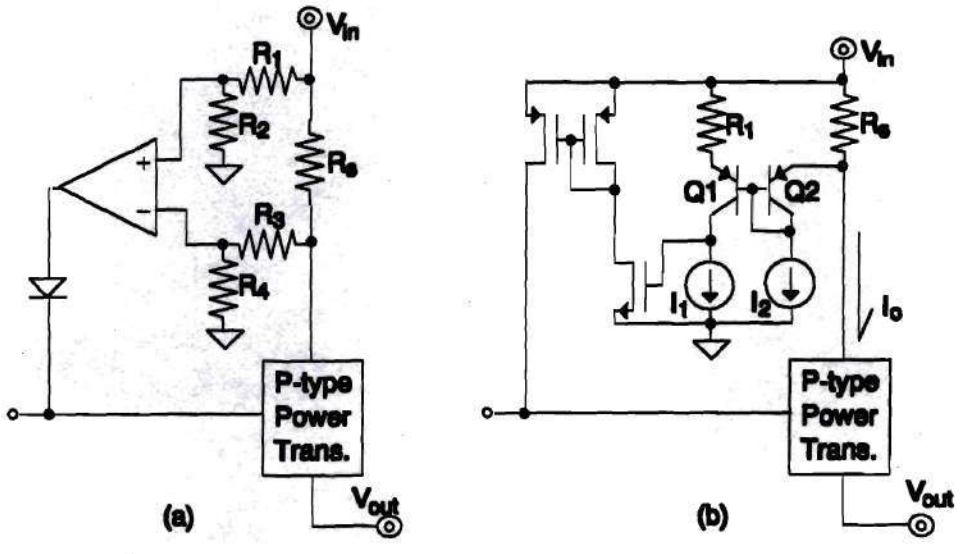


Figure 7.3. Low voltage current limiting circuit protection.

The drawback of this low voltage circuit is the additional quiescent current flow and chip area associated with the amplifier and the resistors. Figure 7.3 (b) illustrates one somewhat simpler form where quiescent current flow is appreciably low, approximately $I_1 + I_2$. Circuit elements Q1, Q2, and R_1 constitute a comparator whose threshold voltage is defined by I_1R_1 and triggered by I_oR_s.

The maximum power dissipation rating for a power transistor, constrained by the input voltage and the maximum output current ($V_{in}I_{o\text{-}max}$) for the case of Figures 7.2 and 7.3, determines the maximum output current capability of the regulator ($I_{o\text{-}max}$). This restriction could be relaxed, however, if a foldback current limiting scheme is implemented, as illustrated in Figure 7.4 [2]. The idea is to make the maximum allowed output current, during overload conditions, a function of the output voltage. Consequently, the maximum current permitted (current through R_s, I_{R_s}) is reduced as the output voltage is decreased. The resulting relationship can be expressed as

$$I_{R_s} = \frac{V_{be}[R_a + R_b]}{R_b R_s} + \frac{V_{out} R_a}{R_b R_s} = I_1 + \frac{V_{out} R_a}{R_b R_s} \qquad (7.3)$$

and graphically illustrated in Figure 7.4 (b) where I_1 is the maximum current allowed when the output is electrically shorted to ground. The worst-case power dissipation can be designed to be $V_{in}I_1$ as opposed to the higher $V_{in}I_{o\text{-}max}$ of the non foldback configuration. Consequently, the maximum output current only occurs when the output voltage is at its nominal value and not when the output is short circuited to ground. In other words, the maximum power dissipation for a given maximum output current is lower for a foldback current limiting scheme than other common realizations. Figure 7.4 (c)

Aptiv Services US, LLC Exhibit 1015 Page 146

shows another implementation of the foldback technique adopting the low voltage concept of the circuit illustrated in Figure 7.3 (a). The corresponding threshold voltage for this configuration is a function of the output voltage and is expressed as

$$V_{threshold} = V_{out}\left\langle \frac{R_4[R_1+R_2]}{R_2[R_3+R_4]} - 1 \right\rangle. \qquad (7.4)$$

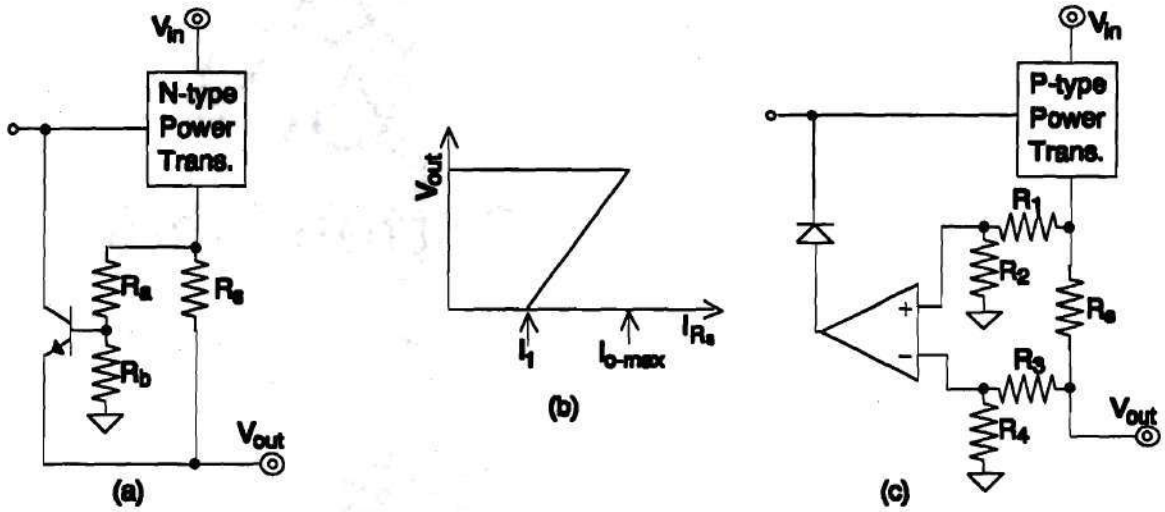


Figure 7.4. Foldback current limiting circuit protection.

Reverse Battery Protection

The backward installation of batteries is a common occurrence that could irreparably damage a chip if precautions are not taken. Figure 7.5 illustrates different forms of circuit protection against battery reversal [49]. The first one is a diode in series with the battery, Figure 7.5 (a). When the battery is reversed, the diode is reversed biased and therefore discontinues to conduct current. The drawback of this circuit, however, is the diode voltage loss during normal operation; in other words, the voltage seen by the circuits is V_{in} - V_{be} instead of V_{in}. This is especially detrimental to low drop-out

regulators. The second version uses a shunt diode between the terminals of the battery, Figure 7.5 (b). In this case, there is a large amount of current flowing through the diode when the battery is reversed. Though this is an effective method of protection, the battery could be totally drained during prolonged periods of reverse battery operation. On the other hand, the input voltage is not degraded during normal operating conditions.

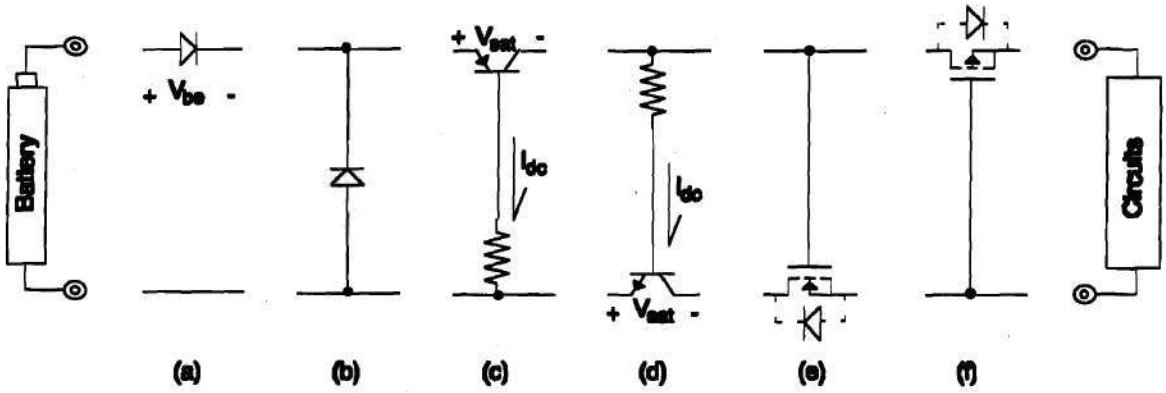


Figure 7.5. Reverse battery protection circuits.

Other forms of reverse battery protection include the use of three terminal switches, such as bipolar and MOS transistors. Figure 7.5 (c) shows a high side PNP transistor switch. During normal operation, the transistor is in the forward active region exhibiting a small voltage loss equal to one V_{sat}. During reverse battery operation, the emitter-base junction is reversed biased and the transistor discontinues current flow. The voltage loss across the transistor during normal conditions, though small, can be notable in a low voltage environment. Furthermore, the current flow through the resistor during proper operating conditions may be significant enough to increase the quiescent current overhead. As a result, the current efficiency of the loading circuits is decreased thereby reducing battery life. A low side version of the PNP configuration is implemented in Figure 7.5 (d). The advantage of the low side circuit, is that the forward current gain (β)

of the power NPN transistor is typically larger than that of the PNP counterpart, which leads to lower quiescent current flow. This, however, comes at the expense of a non-zero voltage for the ground terminal of the loading circuits.

Figures 7.5 (e) and (f) show the MOS versions of reverse battery protection. It is noted that the bulk terminals are connected to the drains instead of the sources. This is done to prevent any current from flowing through the intrinsic diode (formed by the p-bulk and the n+ diffusion) to the loading circuits during reverse battery operation. If this was not the case, current could still flow through the switch. The advantage of the MOS configurations over the bipolar versions is that there is no net current loss during normal operating conditions thereby leaving quiescent current flow and battery life intact. However, MOS devices need to be large to exhibit low resistance, in other words, low saturation voltage at high currents. This is especially cumbersome in a low voltage environment where gate drive is diminished. This could be alleviated by the use of a charge pump at the cost of complexity, quiescent current flow, and chip area. Consequently, the low side version using the NMOS device is more appropriate because of its inherently lower "on" resistance.

The series diode, bipolar switches, and MOS switches are not well suited for a low voltage, low drop-out regulator. The series diode and the high side switches of Figures 7.5 (a), (c), and (f) exhibit voltage losses that degrade the drop-out voltage of the regulator by a V_{be}, a V_{sat}, or a $V_{sd\text{-}sat}$ respectively. The low side switch versions, Figures 7.5 (d) and (e), similarly exhibit voltage losses on the ground terminal. For instance, if the minimum input voltage of the regulator is 1 V, then the battery voltage must be greater than 1 V + V_{sat} [$V_{ds\text{-}sat}$], which can be approximately 1.1 - 1.2 V. Furthermore, the dc current loss in the bipolar switch versions of Figures 7.5 (c) and (d) are inappropriate for a low quiescent current environment. As a result, the most appropriate circuit for current

Aptiv Services US, LLC Exhibit 1015 Page 149

efficient, low voltage, low drop-out regulators is the shunted diode of Figure 7.5 (b). The only disadvantage of this circuit is that its current flow during reverse battery operation is large. However, this would only drain the battery considerably if the reverse battery condition persists for a prolonged period of time.

Thermal Shutdown Protection

Environmental or loading conditions can cause the regulator and most specifically the power transistor to operate under extreme temperatures that can cause damage to the circuit. Thermal shutdown protection circuits prevent such an occurrence from happening. The main concept is to sense the temperature of the chip and trigger a protective course of action only when the temperature exceeds a specified value. Figure 7.6 illustrates one such configuration where an NPN transistor is used as a sense switch, a

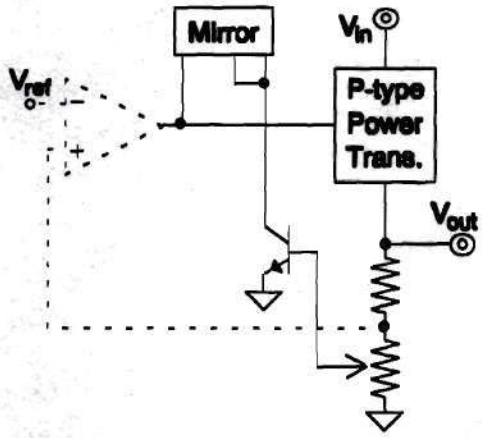


Figure 7.6. Thermal shutdown protection circuit.

modified version of [1]. The temperature dependence of the base-emitter voltage of the transistor can be approximated to be -2.2 mV/°C. Thus, if the threshold temperature is roughly 150 °C, then the base of the transistor must be biased at a voltage of approximately 400 mV. Consequently, the NPN device is off when the temperature is

below 150 °C. When the temperature limit is exceeded, however, the transistor conducts current and shuts off the power device. The threshold temperature is not accurate because the bias voltage of the base may exhibit considerable temperature drift. Accurate performance is most likely specified only for a lower temperature range. Furthermore, the trigger temperature increases during drop-out conditions. This can be avoided by taking the bias voltage of the base from the reference circuit instead of the output of the regulator. Lastly, the thermal sensing transistor must be physically close to the power device. This is done to accurately sense the temperature of the device.

7.4 Experimental Performance

Figures 7.7 and 7.8 illustrate the circuit realization of the system shown in Figure 7.1 with the exception of the protection circuit. These were fabricated in MOSIS 2 μm CMOS technology with an added p-base layer. The plots of the layout are illustrated in appendix C. The protection circuitry was not included in the circuit for two reasons: (1) it is not the focus of the research and (2) its presence could hamper the evaluation of the circuit techniques implemented in the design. However, electrostatic discharge (ESD) protection was included to ensure reliability during laboratory experiments. The passive components of the reference (Figure 7.8) and the schottky diode of the control loop (Figure 7.7) were implemented discretely for greater testing and trimming flexibility.

Figures 7.9 through 7.23 describe the performance achieved by the system designed. Figure 7.9 illustrates the line regulation performance of the control loop, roughly 1.05 mV/V. The performance was approximately the same with and without implementing the current boosting technique. However, the minimum input voltage improved from 1.32 to 1.2 V for a maximum load-current of 50 mA by using the current boosting technique, corresponding to an improvement of roughly 10 %. Figure 7.10

shows the minimum operating voltage of the control loop. The circuit works down to a voltage of approximately 1 V while generating an output current of 19 mA. The minimum input voltage for the non current boosted version was approximately 1.125 V. The drop-out voltage performance is depicted by Figure 7.11. The circuit achieved a drop-out voltage of 232 mV at 60 mA of load-current, which corresponds to an improvement of roughly 17 % over its non current boosted counterpart. In other words, the pass device exhibited an "on" resistance of 3.9 Ω.

The circuit achieved a load regulation performance of roughly 0.38 mV/mA, which is illustrated in Figure 7.12. The figure shows the performance at 1 and 1.2 V as well as with and without implementing the current boosted technique. The maximum load-current for an input voltage of 1 and 1.2 V is 18 and 50 mA respectively. This is approximately a 67 to 85 % improvement over its non current boosted version. Figure 7.13 shows the quiescent current flow as a function of load-current. Quiescent current at zero load-current was 23 μA whereas it peaked at 230 μA during maximum load-current conditions. The increase in current is expected because of the load-dependent current flow of the buffer and the schottky diode. The maximum quiescent current without implementing the current boosting technique was approximately 50 μA. The non current boosted circuit's quiescent current flow started dropping at a load-current of 30 mA, which corresponds to its maximum output current capabilities. The large difference in maximum quiescent current flow between both circuit versions results from the parasitic ground current flowing through the vertical bipolar devices inherent in the layout of the power PMOS transistor. This was considerable because the schottky diode was not large enough to exhibit lower diode voltage drops, $V_{diode} \approx 0.45 - 0.5$ V. The absence of a buried layer also aggravated the phenomenon by not degrading the current gain of the parasitic bipolar devices.

Aptiv Services US, LLC Exhibit 1015 Page 152

Figure 7.14 illustrates the transient performance of the circuit upon a load-current step transition. The load-current was stepped from 0 to 50 mA and vice versa. The maximum output voltage variation of the circuit was 19 mV, shown by trace B. The same circuit but without the aid of load dependent biasing in the current efficient buffer showed a variation of 148 mV. Therefore, the benefits of the current efficient buffer in the LDO for a given amount of quiescent current flow can be roughly quantified to yield an improvement of 87 %. In other words, the quiescent current flow at low load-currents for a given output voltage variation is significantly reduced by utilizing the current efficient buffer. Figure 7.15 shows the output noise voltage of the control loop. The noise voltage peaks at roughly 3 $\mu V/\sqrt{Hz}$ at 100 Hz and continuously drops as the frequency increases. This 1/f noise behavior is typical to linear regulators and appropriate for the frequency response of the system. Table 7.1 summarizes the parameters that were affected by the current boosting technique and the load dependent biasing of the current efficient buffer. The only drawback to the enhancing techniques developed is the large quiescent current flow during high load-current conditions. Its effect on battery life, however, is negligible because the total current drain is dominated by the large load-current, $I_{drain} = I_{Load} + I_{quiescent} \approx I_{Load}$ (high current efficiency).

The behavior of the temperature dependent current components of the reference are shown in Figure 7.16. The nonlinear component (I_{NL}) performs as expected, off during the first part of the temperature range and on during the latter part. The resulting, untrimmed temperature drift performance is roughly 32 $\mu V/°C$, as illustrated in Figure 7.17. This was improved to approximately 8.6 $\mu V/°C$ after the trimming procedure was implemented, as shown in Figure 7.18. The resulting performance was not as good as theoretically predicted by simulations. This may be attributed to the temperature effects of the start-up circuit. The effect of the temperature drift of the input offset voltage of the

Aptiv Services US, LLC Exhibit 1015 Page 153

error amplifier could have been diminished by trimming the reference to compensate for it. As is, trimming for the bandgap reference did not take this into account. This would have improved the overall temperature drift performance of the system. Figure 7.19 shows the proper functioning of the start-up circuit. The input voltage was slowly ramped from 0 to 1.3 V and the reference voltage reached its specified value at an input voltage of approximately 1.1 V.

Figure 7.20 shows the line regulation performance of the reference, which was approximately 204 μV/V. Figure 7.21 shows a close-up to demonstrate the corresponding minimum input voltage of roughly 1.1 V. Line regulation performance exhibits the worst degradation as the input voltage approaches 1.1 V. This was expected because the voltage of the pre-regulated supply within the reference is defined to be between 1.1 and 1.2 V. As a result, the pre-regulator goes into drop-out when the input voltage reaches 1.1 V. Figure 7.22 shows the quiescent current of the reference as a function of input voltage. The current peaks at 14 μA, which corresponds to an input voltage of 1.1 V. It peaks at this value because the pre-regulator goes into drop-out. This current does not include the current incurred by the JFET in the circuit. The JFET was implemented discretely but its realization in MOSIS can be made by a p-base channel, an n+ diffusion top gate, and an n-well bottom gate. The p-base can be laid out as a resistor exhibiting high resistance. The p-channel JFET can be designed to define a current between 0.5 and 3 μA in the configuration shown in the schematic of the reference. Consequently, the maximum quiescent current flow of the reference including the JFET is approximately 17 μA.

Figure 7.23 shows the output noise voltage performance of the reference. The circuit shows some 1/f noise as well as significant thermal noise. The 1/f noise comes from the PMOS transistors defining the temperature dependent currents flowing through

the output. Appreciable thermal noise results from the use of large resistors at the output of the reference. The noise bandwidth is defined by the load capacitor of the reference. The resulting output noise voltage starts to drop at a frequency between 6 and 10 kHz and at a rate of roughly 20 dB/dec. The overall noise content can be improved by simply reducing the noise bandwidth, which is achieved by increasing the load capacitance of the reference.

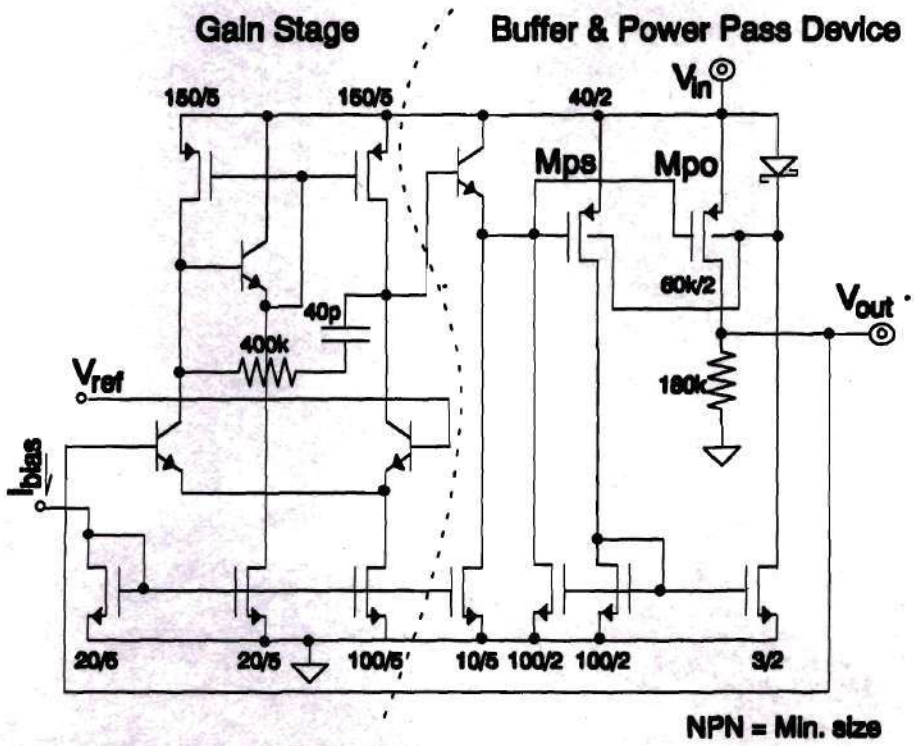


Figure 7.7. Schematic of the control loop circuit.

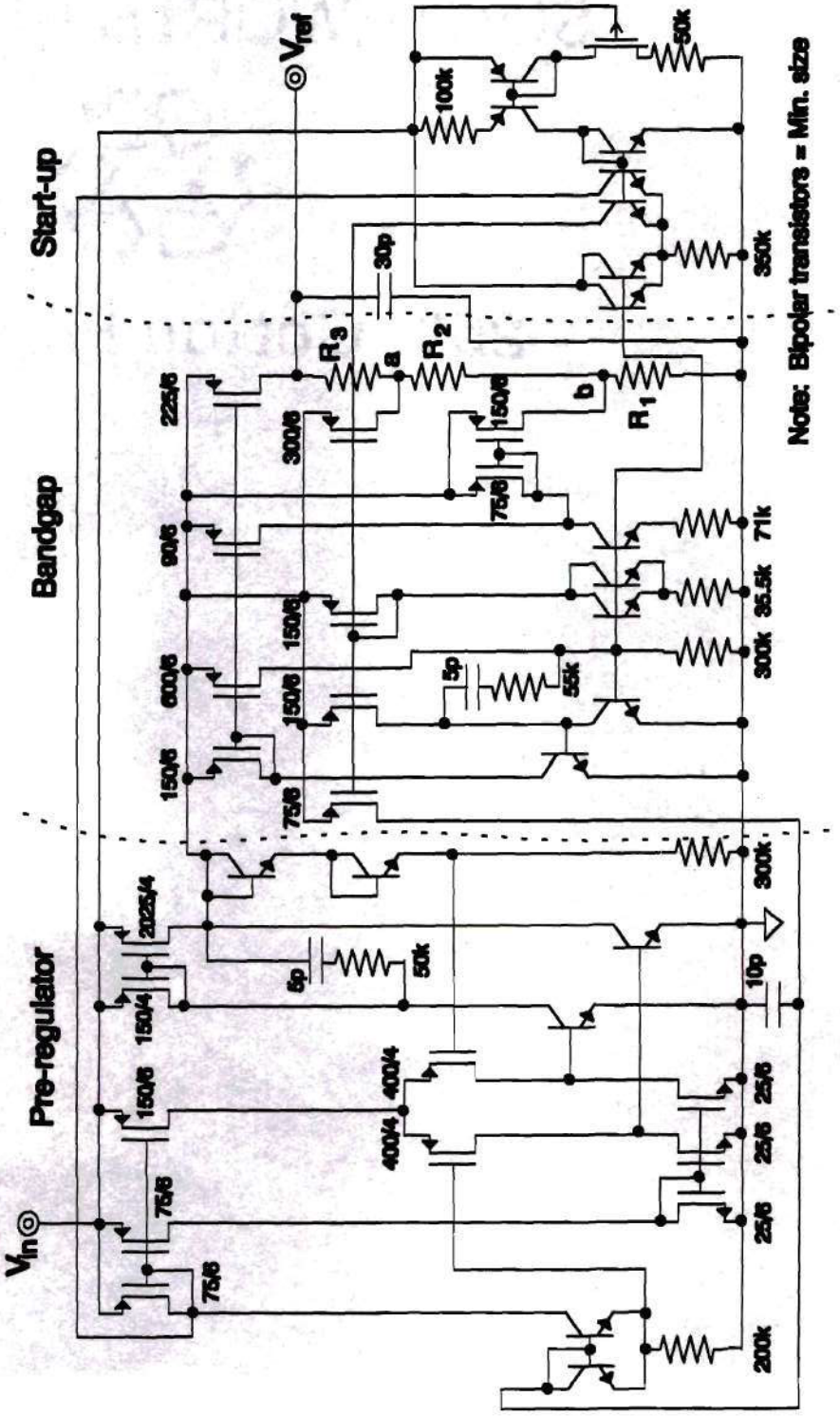


Figure 7.8. Schematic of the reference circuit.

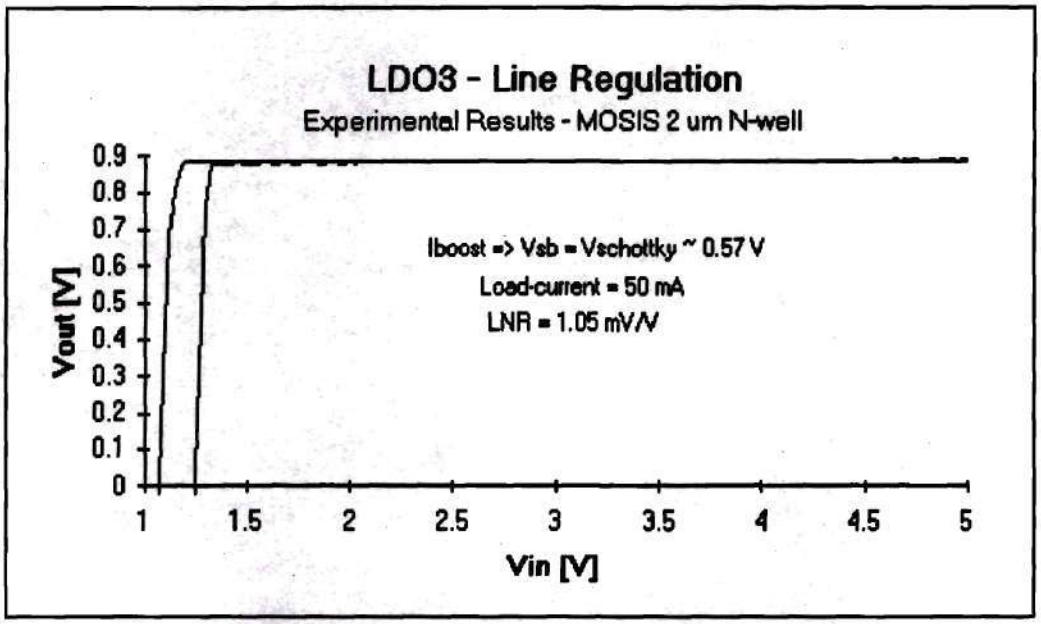


Figure 7.9. Line regulation performance of the control loop.

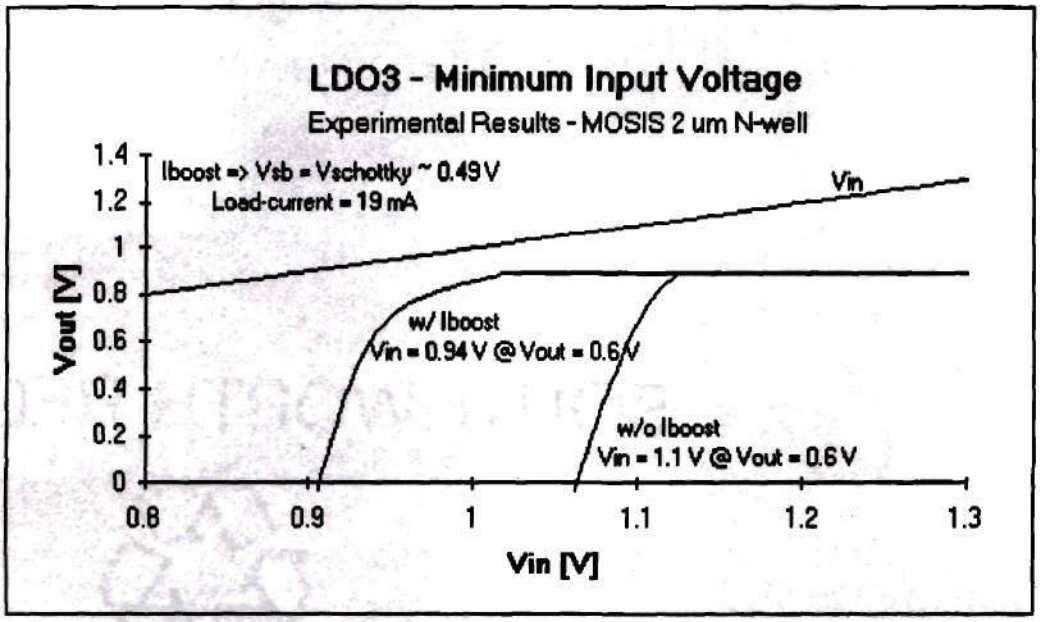


Figure 7.10. Minimum input voltage of the control loop.

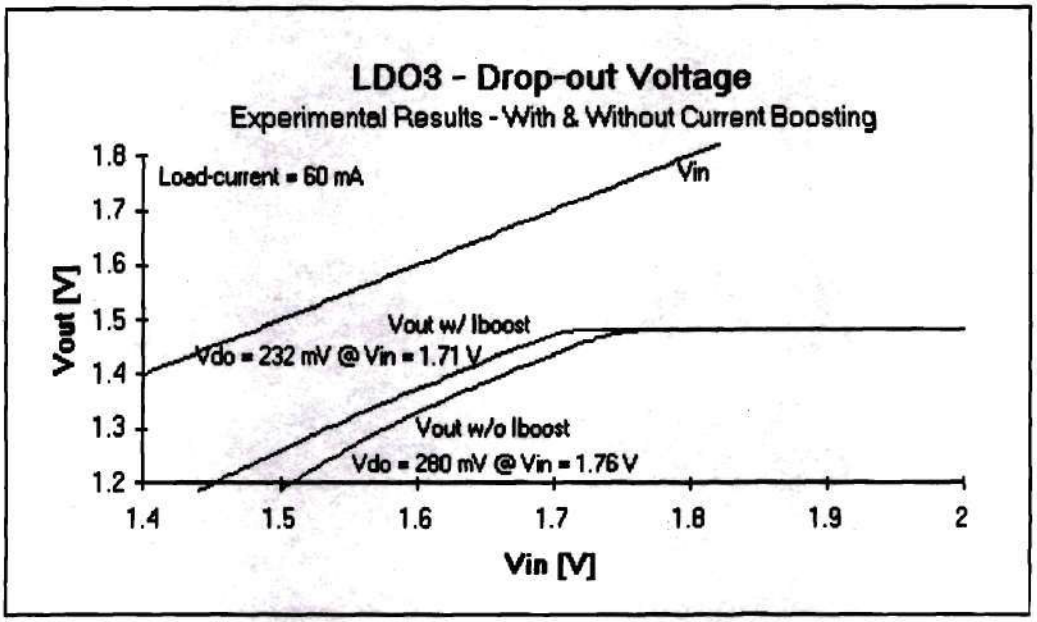


Figure 7.11. Drop-out voltage performance.

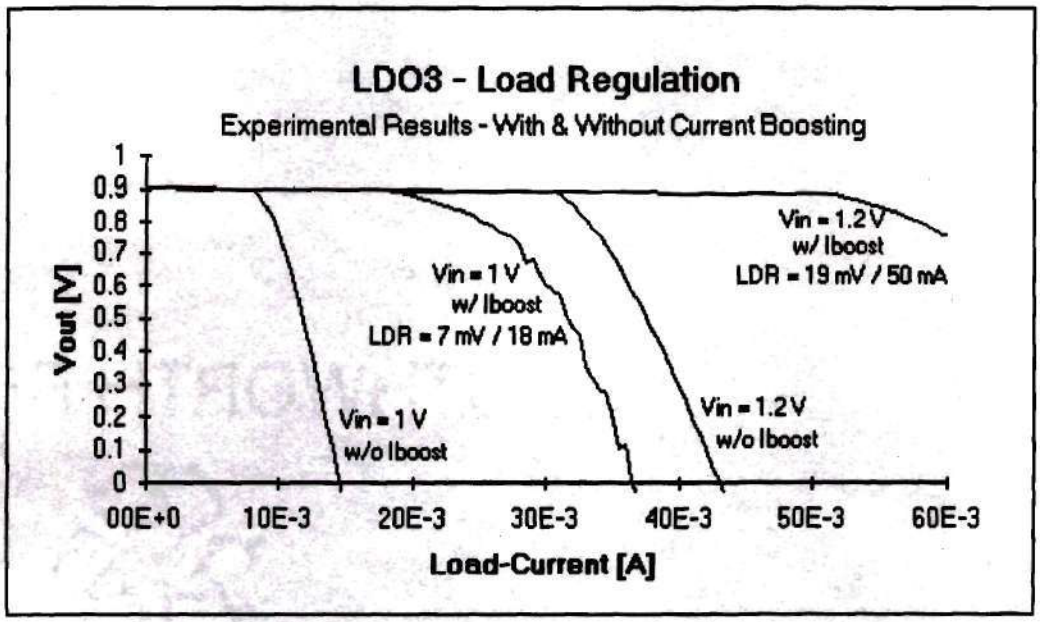


Figure 7.12. Load regulation performance.

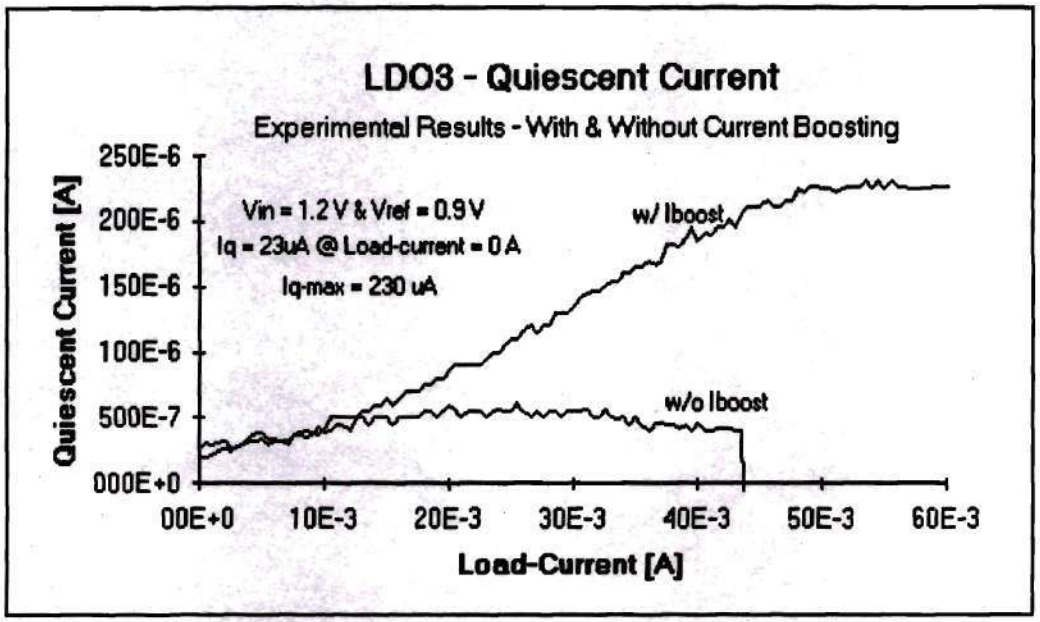


Figure 7.13. Quiescent current flow of the control loop.

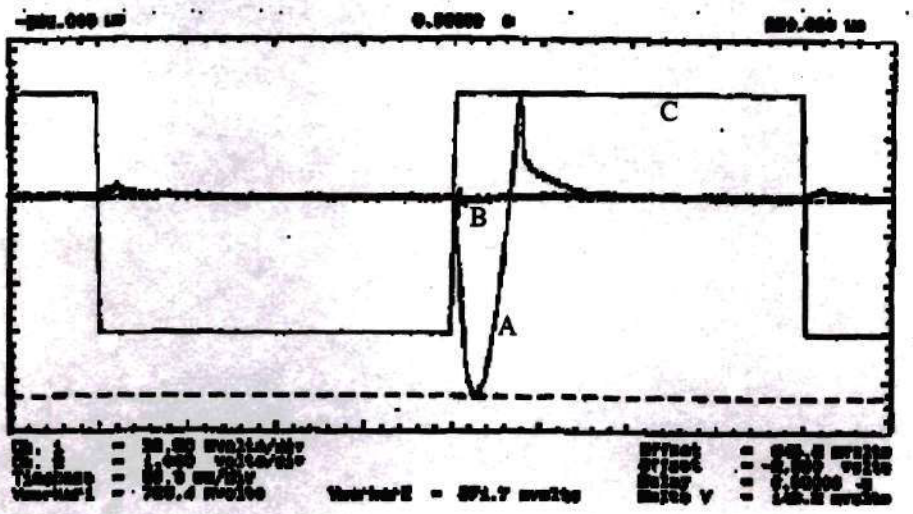


Figure 7.14. Transient response to a full range load-current step (A) with and (B) without the aid of load dependent biasing in the current efficient buffer.

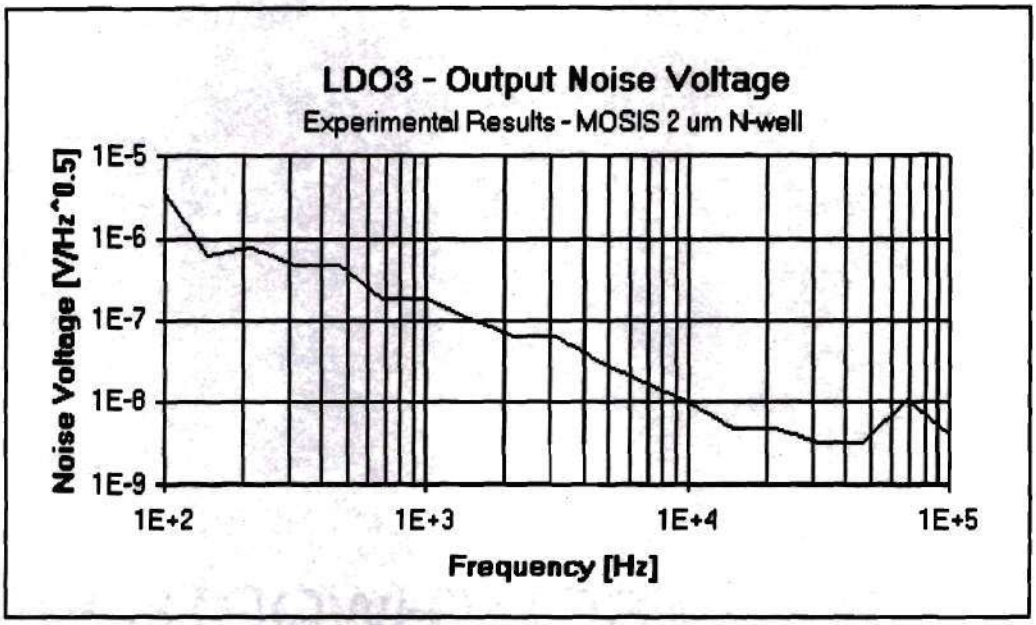


Figure 7.15. Control loop output noise voltage performance.

Table 7.1. Table of parameters affected by the current boosted pass device and the current efficient buffer.

Specification	LDO	LDO w/o Current boost	LDO w/o Load dependent biasing
$I_{quiescent}$ @ no-load	23 µA	23 µA	23 µA
$I_{quiescent-max}$	230 µA	50 µA	200 µA
I_{o-max} @ V_{in}= 1.2V	50 mA	32 mA	50 mA
@ V_{in}= 1V	18 mA	8 mA	18 mA
$V_{drop-out}$ @ 60mA	232 mV	280 mV	232 mV
R_{on}	3.9 Ω	4.7 Ω	3.9 Ω
$\Delta V_{o-Transient}$	19 mV	19 mV	148 mV

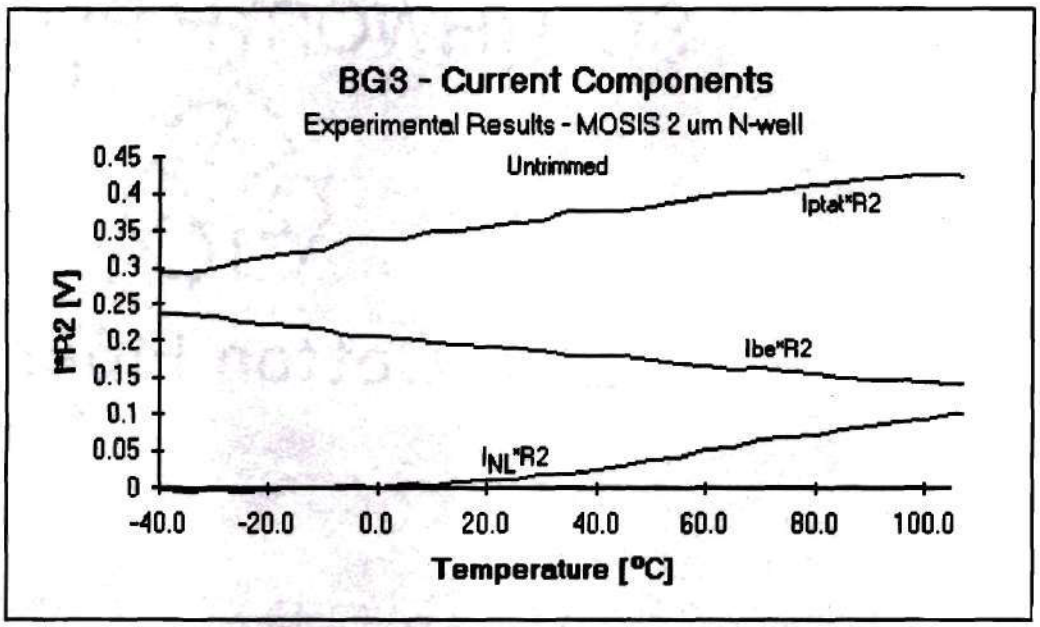


Figure 7.16. Temperature dependent currents in the reference.

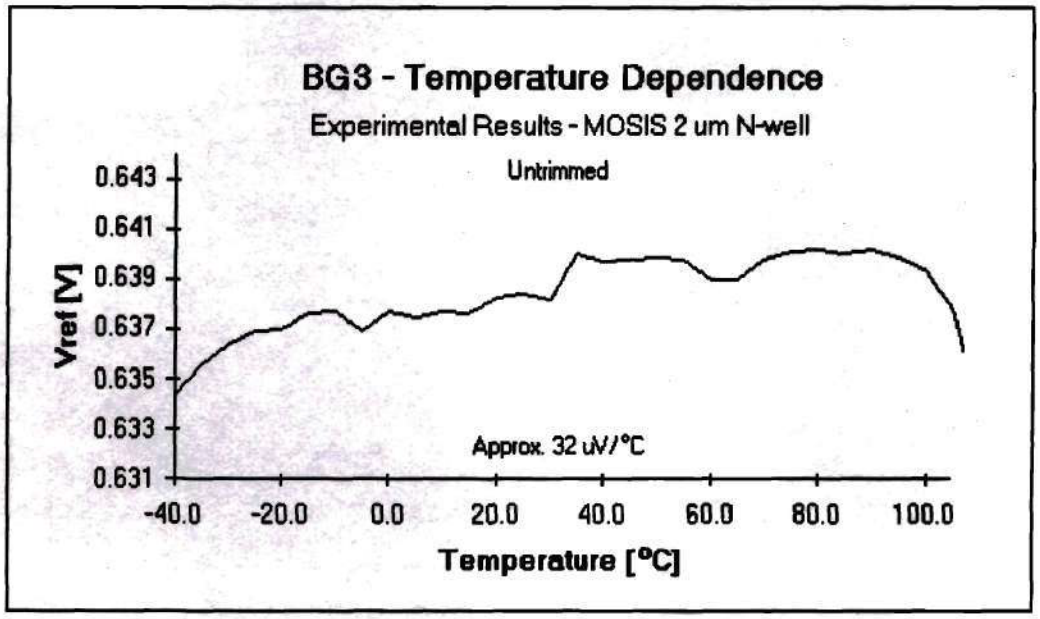


Figure 7.17. Temperature drift performance of the untrimmed reference.

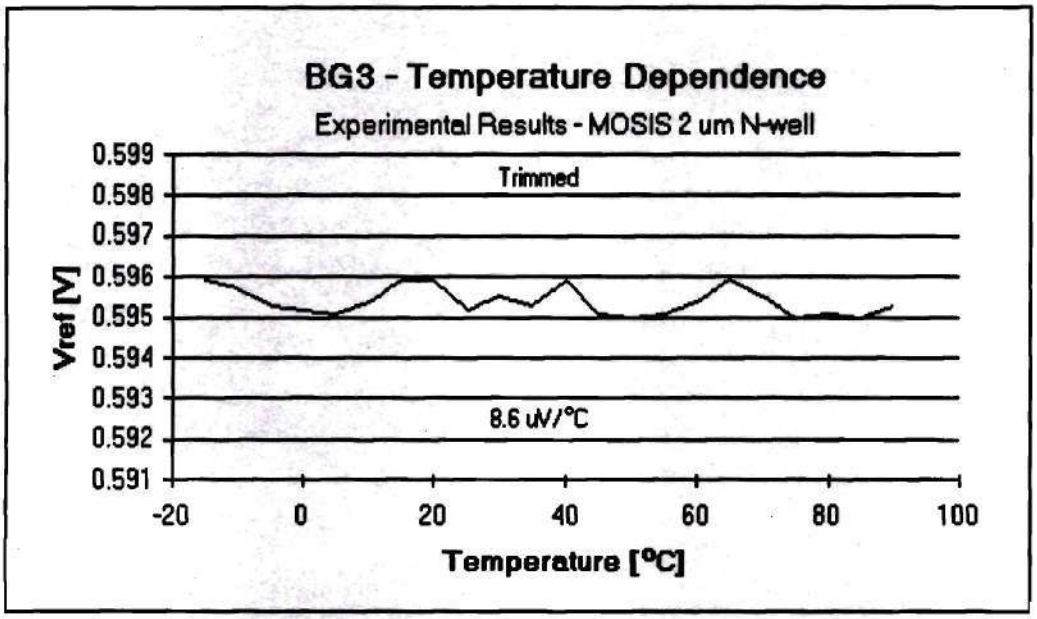


Figure 7.18. Temperature drift performance of the trimmed reference.

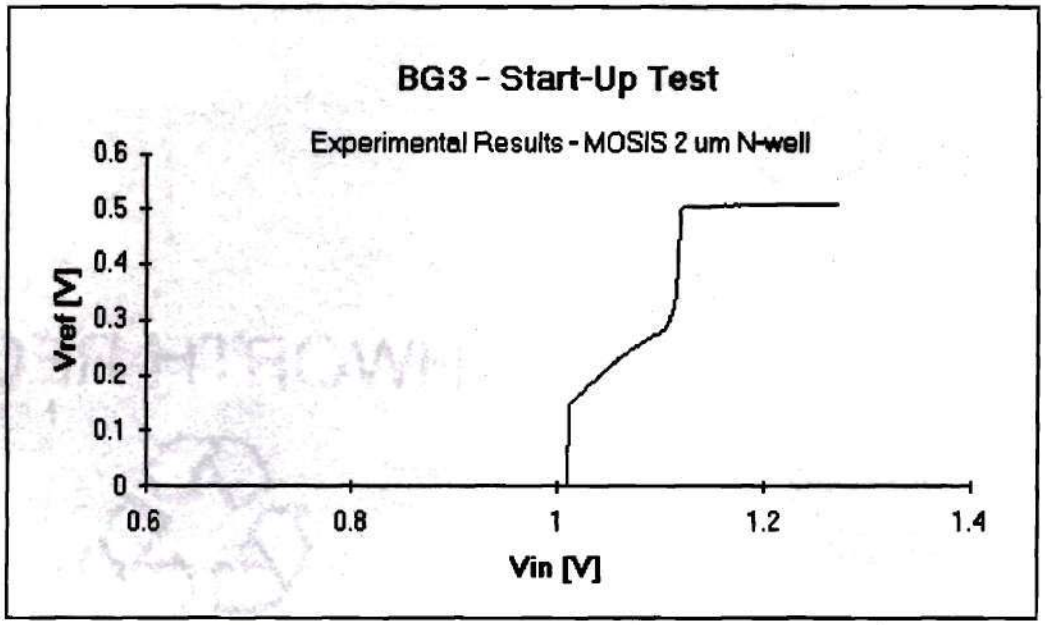


Figure 7.19. Reference start-up test.

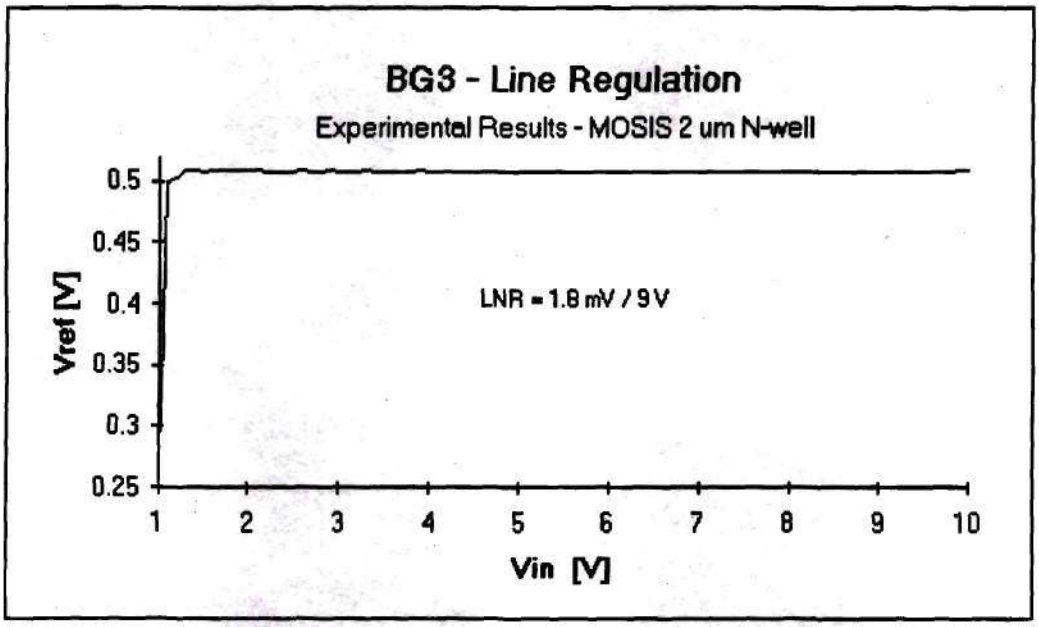


Figure 7.20. Line regulation performance of the reference.

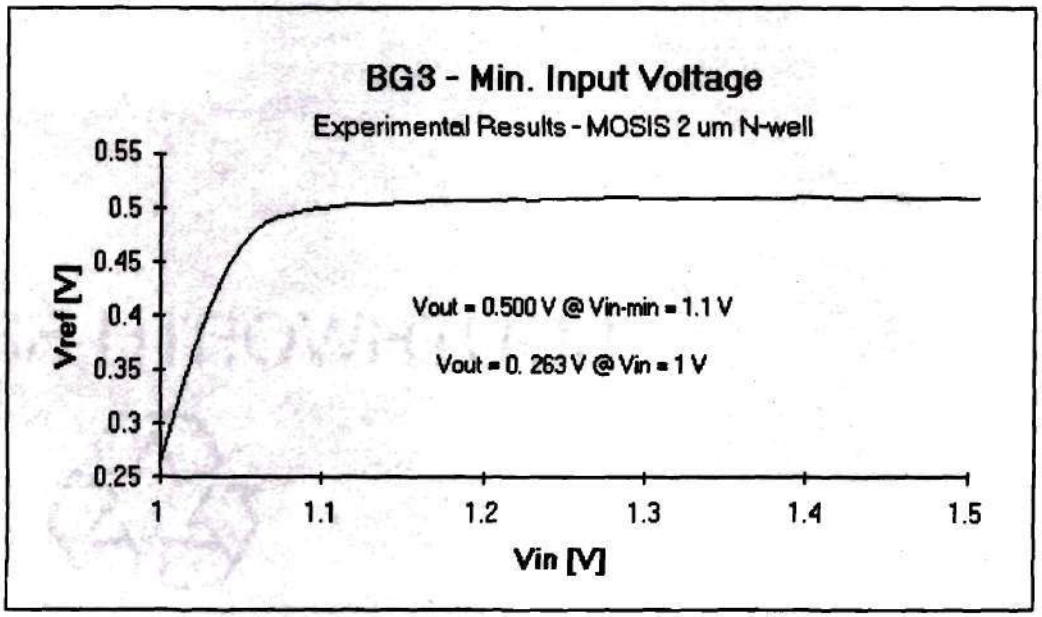


Figure 7.21. Minimum input voltage of the reference.

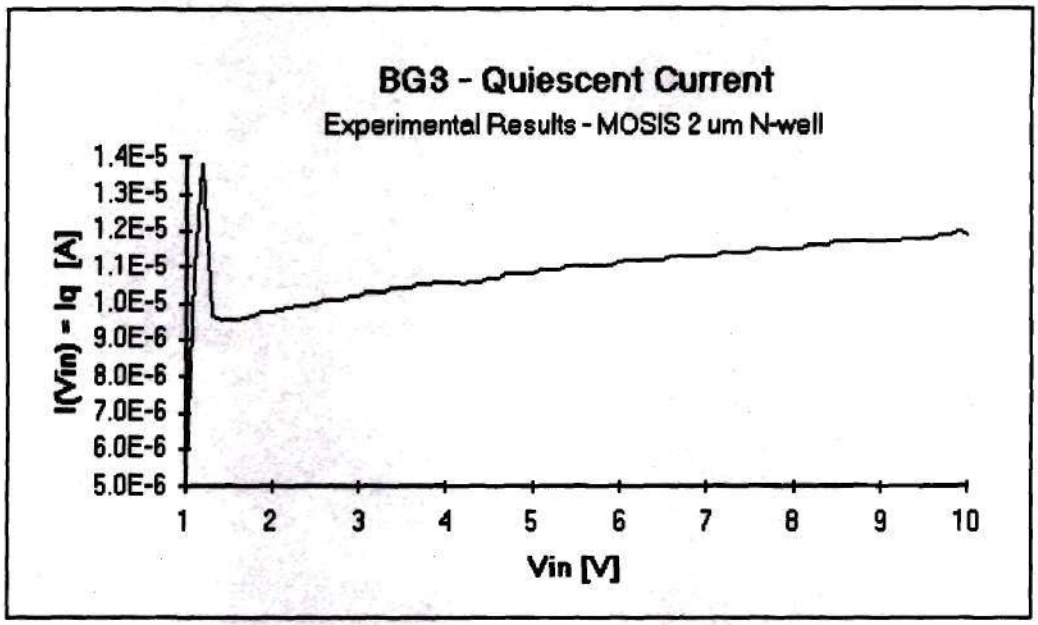


Figure 7.22. Quiescent current flow of the reference.

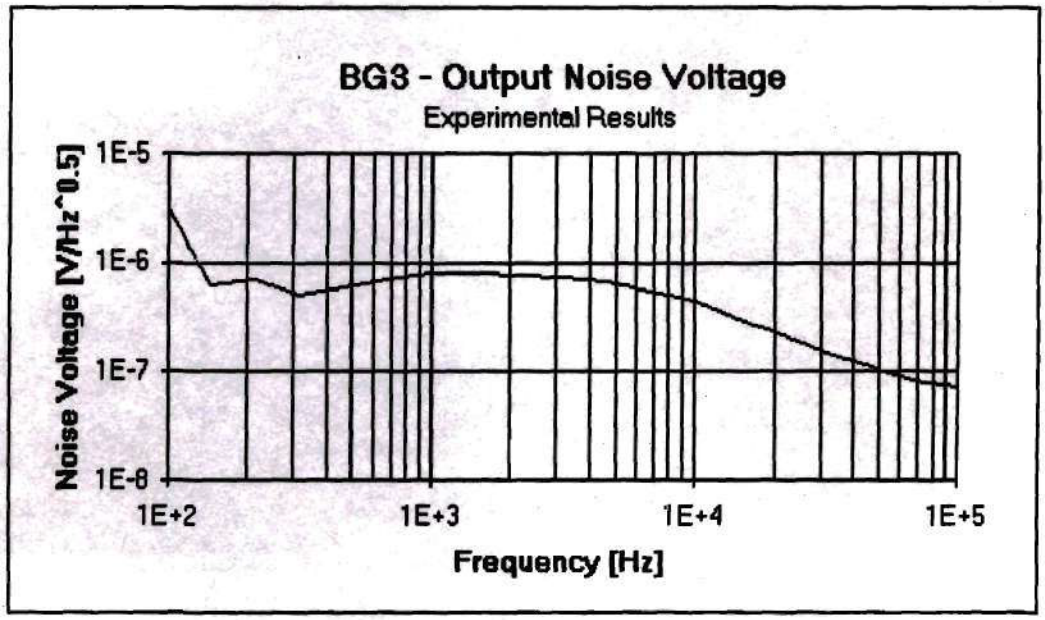


Figure 7.23. Reference output noise voltage performance.

7.5 Summary

This chapter has demonstrated the system design issues in assembling a low drop-out regulator circuit. It started by exploring the different circuit blocks and continued to discuss the physical layout characteristics and requirements of the system. Particular attention was given to those layout issues that affect performance and reliability. A description of the protection circuits followed. The discussion included overload current protection, reverse battery protection, and thermal shutdown protection. Lastly, the chapter concluded with the results of a prototype circuit fabricated in MOSIS 2 μm CMOS technology with an added p-base layer. The results verified the appropriateness of the enhancing techniques and the low voltage circuits developed in the previous chapters. Table 7.2 shows the resulting performance parameters of the system relative to the target specifications defined in chapter 1. Overall accuracy was met while minimum input voltage, quiescent current flow at zero-load current, and drop-out voltage performance requirements exceeded the original projections.

Aptiv Services US, LLC Exhibit 1015 Page 165

Table 7.2. Performance summary.

Specification	Control Loop	Reference	System	Target
V_{in}	≥ 1 V	≥ 1.1 V	≥ 1.1 V	≥ 1.2 V
$I_{quiescent}$ (no load)	23 µA	17 µA	40 µA	≤ 65 µA
$I_{quiescent}$ (I_o=50mA)	230 µA	17 µA	247 µA	-
$V_{drop-out}$ (I_o=60mA)	232 mV	n/a	232 mV	≤ 0.3 V
R_{on}	3.9 Ω	n/a	3.9 Ω	2 to 6 Ω
I_{o-max} @ V_{in}=1V	18 mA	n/a	18 mA	-
I_{o-max} @ V_{in}=1.2V	50 mA	n/a	50 mA	≥ 50 mA
C_{output}	4.7 µF	n/a	4.7 µF	4.7 µF
ESR range	0 to 10+ Ω	n/a	0 to 10+ Ω	0 to 10 Ω
Temperature	-10 to 90 °C	-10 to 90 °C	-10 to 90 °C	-10 to 90 °C
$\Delta V_{o-Transient}$	19 mV	n/a	19 mV	≤ 75 mV
Temperature Drift	16.7 µV/°C	8.6 µV/°C	25.3 µV/°C*	-
Line Regulation	1.05 mV/V	204 µV/V	1.25 mV/V	-
Load Regulation	0.38 mV/mA	n/a	0.38 mV/mA	-
V_{offset}	4 mV	n/a	4 mV	-
Accuracy	± 3 % (V_{out} = V_{ref} = 0.9 V)			± 3 to 5 %

* TC is improved by trimming the reference to compensate the control loop's TC.

CHAPTER VIII

CONCLUSIONS

On the basis of the literature survey and the results of the research, several conclusions and projections can be formulated. This chapter starts with a summary of the obstacles and the techniques developed to enable practical realizations of low drop-out regulators (LDO) appropriate for single, low voltage battery cell operation. This is followed by a discussion of the direction of technology and the consequential effects on low drop-out regulators within the context of prevailing designs and the research at hand. The chapter concludes with general comments about the research and recommendations for the continuation of this work.

8.1 Obstacles

The main objective of this research was to develop techniques that allow low drop-out regulators to work in a battery operated environment. This is driven by the market demand for portable and compact products, such as cellular phones, pagers, camera recorders, etc. As a result, low voltage and low battery current drain are intrinsic characteristics. A single, low voltage battery cell requires operation at voltages between 0.9 and 1.5 V. Furthermore, drain current must be necessarily low to prolong battery life. However, this is virtually impossible during conditions of high load-current when current drain is dominated by load-current while quiescent current flow is negligible. On the other

Aptiv Services US, LLC Exhibit 1015 Page 167

hand, current drain can be reduced during conditions of low load-current where quiescent current is a significant portion of the total current drain. By the way, many applications demand low load-currents for the majority of the time while high load-currents are only demanded briefly. As a result, low quiescent current at low load-currents (high current efficiency) is an important parameter that determines the longevity of a battery.

The problems associated with low input voltages manifest themselves in voltage headroom and output current capabilities. Low voltage affects the reference circuit, the error amplifier, and the pass device. Most references have output voltages of approximately 1.2 V (bandgap voltage). This forces the input voltage to be approximately 1.4 V, in other words, at least one saturation voltage above the reference voltage. Furthermore, references operating at these voltages tend to have poor line regulation performance because of the finite output impedance of uncascoded transistors. Moreover, developing a curvature corrected bandgap without incurring significant quiescent current flow at low voltage is a difficult task. The error amplifier suffers from limitations in flexible circuit architectures. The requirements of the amplifier include high gain, bandwidth, and output voltage swing. The gain affects load regulation while bandwidth influences the transient response of the system. These are laborious objectives to achieve with characteristically low quiescent current flow when considering that circuit techniques such as cascoding, voltage followers, and Darlington configurations are discouraged. Lastly, the performance of the pass device is greatly diminished when the input voltage is decreased. This results from reductions in gate drive, which decreases output current capabilities as well as increases drop-out voltages. These circuit limitations were addressed by the research and were categorized in four distinct areas, namely, current efficiency, current boosting, load regulation enhancement, and referencing. In the implementation of the circuits developed, novel circuit techniques were designed that

exploited the characteristics of the given process technology. This is not only beneficial to designs in existing technologies but also to future and more advanced processes by being fully exploited.

8.2 Enabling Techniques

Current Efficiency

The main issue with quiescent current flow revolves around the control loop of the regulator. In particular, the limitation has been identified to be the buffer of the error amplifier. This is because during transient load-current step transitions the buffer needs to drive quickly the parasitic gate capacitance of the pass device. This capacitance, unfortunately, is characteristically high because the size of the pass element is created large to generate low drop-out voltages and high output currents. Consequently, the slew-rate current of the buffer and therefore the quiescent current flow of the overall amplifier is limited by the transient specification of the system. Thus, a slew-rate dependent boost is developed. The idea is to aid the circuit only during transient conditions. The boost circuit essentially uses a unity gain buffer with low threshold bypass switches. The buffer is still required but its demands are driven by the frequency response and not the slew-rate requirements of the system. Further scrutiny showed that the ac demands of the system were dependent on load-current. As a result, a minimized quiescent current design was developed that not only met the requirements of stability but also aided the slew-rate current demands during transient load-current transitions. The resulting architecture was the current efficient buffer.

Current Boosting

The problem of output current capabilities resides in the power PMOS pass device. At low input voltages, the gate drive of the transistor is diminished and consequently so is

Aptiv Services US, LLC Exhibit 1015 Page 169

its output current and "on" resistance. This problem is circumvented by increasing the input voltage and/or increasing the size of the transistor. The former is counterproductive for low voltage operation. The latter causes the parasitic gate capacitance to increase, which increases the slew-rate current requirements of the buffer in the amplifier. This, in turn, places a harsher limitation on quiescent current flow. The only way to improve performance without sacrificing area or low voltage performance is by decreasing the threshold voltage of the transistor thereby effectively increasing gate drive. This is achieved by the composite PMOS pass device. The main concept of the circuit is to reduce the threshold voltage of the transistor by forward biasing the source to bulk junction during conditions of high load-current, which is based on the bulk effect phenomenon.

Load Regulation Enhancement

Load regulation performance is limited by the dc open-loop gain of the control loop. This open-loop gain, in turn, is limited by the required bandwidth of the system and the frequency response implications of the loading circuits. The bandwidth is then limited by the transient response requirements and the parasitic poles of the system. The parasitic poles tend to be at lower frequencies because the circuits are designed with minimum quiescent current flow. As a result, load regulation performance is also limited. This is ameliorated by adding a pole/zero pair to the ac response of the system. The main idea is to promote the rapid drop of gain per decade of frequency. As a result, the dc gain can be increased while simultaneously maintaining the unity gain frequency below the frequencies where the parasitic poles reside. Two error amplifier topologies were developed to achieve this, namely, parallel path amplifiers and frequency shaping gain structures. The former utilizes one amplifier to introduce the pole (dominant pole of the main amplifier) and another amplifier to introduce a zero (parallel amplifier is used as a feed forward

Aptiv Services US, LLC Exhibit 1015 Page 170

path). The frequency shaping gain structures use a single, one stage amplifier topology to generate a frequency response exhibiting a pole/zero pair behavior. Among the two, the latter is the most appropriate for low quiescent current flow.

Low Voltage Reference

Most bandgap reference circuits utilize a voltage mode approach. They create the reference voltage by adding a base-emitter and a proportional-to-absolute temperature (PTAT) voltage. The result of this is a minimum input voltage requirement of one saturation voltage plus a bandgap voltage. Furthermore, if good line regulation performance is required, the minimum input voltage requirement is degraded by another saturation voltage. The input voltage is ultimately limited to be greater than 1.5 - 1.6 V. Thus, a mixture of a voltage-mode and a current-mode topology is developed that allows the realization of a low voltage reference with flexible temperature compensation maneuverability. An appropriate trimming procedure is also successfully developed. The only problem left to overcome was to implement a curvature correcting technique that incurs small chip area and low quiescent current flow. A technique was developed that did not incur any additional quiescent current flow, namely, the resistor ratio method. The concept is to choose two different types of resistors whose ratio yields a PTAT temperature coefficient. As a result of running a PTAT current defined by one type of resistor through another type of resistor, a PTAT squared term is generated. This constitutes one of the classical methods of curvature correction. The drawback to this circuit is actually finding two resistors with the necessary characteristics in a particular process technology. Consequently, the current subtraction scheme was developed. This method is not dependent on technology and its realization only requires one additional transistor path to ground thereby requiring minimum additional quiescent current flow.

Aptiv Services US, LLC Exhibit 1015 Page 171

The main concept of the circuit lies in the subtraction of a base-emitter dependent current from a PTAT current and the finite output impedance of transistors.

Table 8.1 summarizes the original contributions of this research. The overall study led to several paper submissions. Two of these were indirectly related to the research but necessary and appropriate for the successful development of the same. They are titled (1) "A 1V CMOS op amp using bulk-driven MOSFETs" and (2) "Low-Voltage Analog Circuits Using Standard CMOS Technologies" and they were published in *IEEE International Solid-State Circuits Conference Digest* and *Proc. International Symposium on Low Power Design* respectively. Four other papers were submitted and whose

Table 8.1. Summary of original contributions.

Concept	Technique
Current Efficiency	Slew-rate dependent boost
	Current efficient buffer
Current Boosting	Composite output PMOS transistor
Load Regulation Enhancement	Parallel amplifier topology
	Frequency shaping amplifier
Low Voltage Reference	IV-mode output structure & associated trimming procedure
	Resistor ratio curv. corr. method
	Current subtraction curv. corr. method
Low voltage circuit practices (amplifier and reference topologies)	

content had a direct impact on LDOs. Their titles are (1) "Study and Design of Low Drop-out Regulators," (2) "Optimized Frequency Shaping Circuit Topologies for LDOs," (3) "A Low Voltage, Low Quiescent Current, Low Drop-out Regulator," and (4) "A Novel Low Voltage, Micro-Power Curvature Corrected Bandgap Reference." The first two papers were submitted to *IEEE Transactions on Circuits and Systems* and the other two were submitted to *IEEE Journal of Solid-State Circuits.*

8.3 Direction of Market Demand

Technology

Process technologies are driven by the digital and the mixed-signal markets, which demand higher packing densities [7]. As a result, lithography is reduced and associated breakdown voltages are decreased [8, 9]. In other words, the technology trend is forcing circuits to operate at lower power supply voltages. In fact, 0.14 μm process technologies are expected to be in effect by the year 2004 and the operating voltage range is expected to be as low as 0.9 V [9, 12]. The thrust of the market has been driven in the recent past by digital applications. Consequently, vanilla CMOS processes have become relatively inexpensive and associated threshold voltages are being reduced. The threshold voltage, however, is not expected to decrease below 0.5 or 0.6 V. This is a characteristic imposed by digital circuits. Pure bipolar processes will still be demanded for specific applications but they will not drive the market.

Fully integrated products, on the other hand, are currently launching a more vociferous campaign that is affecting the demands on technology. Mixed-signal products are the result of complete circuit integration. A peaceful coexistence of analog and digital circuits is possible in a purely CMOS environment but with degraded analog performance. The use of bipolar devices, though extinct in prevailing digital designs, is still prevalent in

many analog circuits for enhanced performance. As a result, the demand on technology is slowly being shifted towards biCMOS processes. The high demand will eventually reduce costs to the level of current CMOS technologies. The bipolar features that will most likely be demanded are a p-base layer, a buried layer, and a deep highly doped well plug for the creation of decent quality NPN transistors. Some of the current and relatively inexpensive versions have modified a vanilla CMOS process to include an additional p-base layer thereby offering NPN transistors with high saturation voltages.

LDO Implications

The consequence of lower breakdown voltages in future technologies will force regulator design to work with lower input voltages. This is aggravated by the growing demand for single, low voltage battery cell operation. Furthermore, quiescent current flow and drop-out voltage will be demanded to decrease as well. The demand for higher packing densities will also require low drop-out regulators (LDOs) to occupy less chip area. Low drop-out regulators can be and have been designed in purely CMOS and bipolar process technologies. However, performance can be significantly enhanced by designing in a biCMOS environment. The simple and relatively inexpensive addition of a p-base layer to a CMOS process offers the capability of vertical bipolar devices, which enhance the frequency response and the circuit topology characteristics of the LDO. This is corroborated by the low quiescent current flow demands of MOS pass devices, which are voltage driven in nature. In conclusion, the push towards biCMOS technologies with finer fabrication lithographies will be beneficial for the circuit design of LDOs. At the same time, however, more stringent requirements will be bestowed upon regulators, such as operation with lower input voltages, lower quiescent current flow, smaller chip area, and lower drop-out voltages.

8.4 Conclusion and Recommendations

Circuit techniques have been developed and verified that permit the practical realizations of low drop-out regulators in a single, low voltage battery cell environment to be feasible in current existing technologies. These are also pertinent techniques for higher voltage, high performance LDO designs. Furthermore, switching regulators and other applications can also use these contributions to enhance their performance. For instance, the current boosting technique can be readily utilized for boosting the output current drive of amplifiers or for enhancing the switch performance of dc-dc converters. The research has demonstrated the effectiveness of the concepts by designing and testing circuit prototypes through MOSIS 2 μm CMOS technology with an added p-base layer, a relatively inexpensive process.

The research has focused primarily on developing concepts that make low voltage and low quiescent current operation possible. However, the effects of the protection circuitry, though discussed, were not tested or measured. Thus, the next logical step is to study, develop, implement, and experimentally test the effects of overload current protection, thermal shutdown protection, and reverse battery protection on the overall performance of the LDO. The temperature dependence of the input offset voltage of the error amplifier should be included in the trimming procedure to yield improved overall accuracy. Moreover, reliability issues should be investigated such as performance over hours of operation (burn-in tests). Work can also be done to characterize the effects of current boosted transistors on switching regulators and amplifier output stages. Switching regulators can use complementary current boosted devices if realized in a biCMOS environment. The bulk of the PMOS transistor is extracted by an n-well while that of the NMOS device can be extracted through a p-base or an isolated p-epi region. The p-base layer used for NPN transistors can be used as a p-well. The p-epi region can be isolated

by using the buried layer as vertical isolation and a deep n+ collector plug ring as horizontal isolation. Amplifier output stages can also use the complementary structure with expected higher harmonic distortion levels and parasitic ac effects.

APPENDIX A

V_{BE} TEMPERATURE DEPENDENCE

The collector current of a bipolar transistor exhibits an exponential relationship to the base-emitter voltage and is nominally expressed as

$$I_c = I_s \exp \frac{V_{be}}{V_t}, \qquad \text{(A.1)}$$

where I_c is the collector current, I_s is the saturation current in the forward-active region, V_{be} is the base-emitter voltage, and V_t is the thermal voltage. The effects of early voltage are neglected for this derivation. Consequently, V_{be} is derived to be

$$V_{be} = V_t \ln \frac{I_c}{I_s}. \qquad \text{(A.2)}$$

The saturation current I_s is defined by the electron charge q (1.6×10^{-19} coulomb), the intrinsic carrier concentration n_i (approximately 1.5×10^{10} cm^{-3} at 300° K for silicon), the diffusion constant for electrons D_n, the emitter cross-sectional area A_e, the effective width of the base W_B, and the base doping density N_A (assumed to be constant) [3],

$$I_s = \frac{q n_i^2 D_n A}{W_B N_A} = \frac{q n_i^2 \overline{D_n} A_e}{Q_B}, \qquad (A.3)$$

where Q_B is the number of doping atoms in the base per unit area of emitter and $\overline{D_n}$ is the average effective value of the electron diffusion constant in the base. In turn, the temperature dependence of the intrinsic carrier concentration and the average electron diffusion constant can be described by [51]

$$n_i^2 = AT^3 \exp\frac{-V_{go}}{V_t}, \qquad (A.4)$$

and

$$\overline{D_n} = V_t \overline{\mu_n}, \qquad (A.5)$$

where A is a temperature independent constant, T is temperature, V_{go} is the extrapolated bandgap voltage at 0° K, and $\overline{\mu_n}$ is the average mobility for minority carriers in the base,

$$\overline{\mu_n} = BT^{-n}, \qquad (A.6)$$

where B and n are temperature independent constants. The relationship for the saturation current I_s is more explicitly expressed by substituting equations (A.4) - (A.6) in (A.3) and resulting in

$$I_s = \frac{q\left\langle AT^3 \exp\frac{-V_{go}}{V_t}\right\rangle \cdot \left\langle V_t BT^{-n}\right\rangle A_e}{Q_B} \qquad (A.7)$$

or $$I_S = CT^{(4-n)} \exp\frac{-V_{go}}{V_t} = CT^{(4-n)} \exp\frac{-V_{go}}{V_t}, \qquad (A.8)$$

where C is a temperature independent constant defined by all the constants in equation (A.7), such as q, A, B, A_e, Q_B, and k/q from the thermal voltage term (V_t = kT/q where k is Boltzmann's constant, 8.62 x 10^{-5} eV/°K). Lastly, the collector current can be assumed to have a temperature dependence whose behavior can be described by

$$I_C = DT^x, \qquad (A.9)$$

where D is a constant and x is an arbitrary number defined by the temperature dependence of the current forced through the collector, i.e., x is one for a proportional-to-absolute temperature (PTAT) current, $I_c \propto T^1$. Consequently, the temperature dependence of the base-emitter voltage can be re expressed by substituting equations (A.8) - (A.9) in (A.2) and resulting in

$$V_{be} = V_t \ln\left\langle \frac{D}{C} T^{[x-(4-n)]} \exp\frac{V_{go}}{V_t} \right\rangle = V_{go} + V_t \ln\frac{D}{C} - [(4-n)-x] V_t \ln T. \qquad (A.10)$$

However, a more appropriate form of the base-emitter relationship, for the purpose of design, is its temperature dependence as a function of a reference temperature (T_r). This can be done by obtaining the relation of the base-emitter voltage (V_{be}) at a reference temperature (T_r), solving for a constant, and substituting it back in equation (A.10). The relation of V_{be} at T_r is

$$V_{be}(T_r) = V_{go} + V_{tr} \ln \frac{D}{C} - [(4-n)-x] V_{tr} \ln T_r, \qquad (A.11)$$

where V_{tr} is the thermal voltage evaluated at the reference temperature (T_r). At this point, the constant can be derived to be

$$\ln \frac{D}{C} = \frac{V_{be}(T_r) - V_{go} + [(4-n)-x] V_{tr} \ln T_r}{V_{tr}}. \qquad (A.12)$$

Now, equation (A.12) can be substituted back in (A.10) to yield the well-known temperature dependence relationship of the base-emitter voltage,

$$V_{be} = V_{go} + \frac{T}{T_r}\left[V_{be}(T_r) - V_{go}\right] - [(4-n)-x] V_t \ln \frac{T}{T_r}. \qquad (A.13)$$

It is sometimes useful to develop the Taylor series expansion for the logarithmic term and substitute it back in equation (A.13). The purpose for this is to more accurately design the curvature correcting component of the bandgap reference. The process dependent constant (4 - n) is sometimes expressed as η with an approximate value between 3.6 and 4 [40].

APPENDIX B

IV-MODE BANDGAP TRIMMING PROCEDURE

The output structure of an IV-mode curvature corrected bandgap reference is illustrated in Figure B.1. Magnitude trimming is done at room temperature while temperature compensation is achieved by trimming throughout the specified temperature range. The following procedure illustrates how trimming, in general, can be done for this circuit architecture.

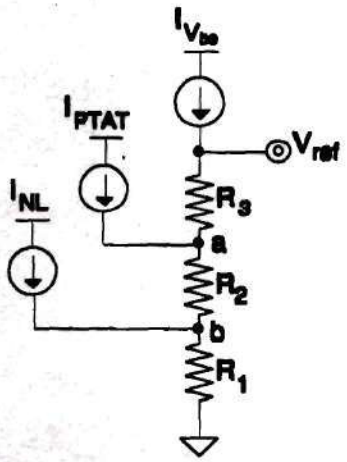


Figure B.1. IV-mode bandgap output structure.

Step 1: The reference voltage (V_{ref}) for this topology can be expressed as

$$V_{ref} = I_{V_{be}}[R_1+R_2+R_3]+I_{PTAT}[R_1+R_2]+I_{NL}R_1, \qquad (B.1)$$

where $I_{V_{be}}$, I_{PTAT}, and I_{NL} are the base-emitter voltage, proportional-to-absolute temperature (PTAT), and nonlinear temperature dependent currents respectively. Alternatively, this can be re expressed as

$$V_{ref}\frac{R_{2_{initial}}}{R_1+R_2}=\left\langle I_{V_{be}}[R_1+R_2+R_3]+I_{PTAT}[R_1+R_2]+I_{NL}R_1\right\rangle\frac{R_{2_{initial}}}{R_1+R_2} \quad \text{(B.2)}$$

or
$$V_{ref}\frac{R_{2_{initial}}}{R_1+R_2}=AI_{V_{be}}R_{2_{initial}}+BI_{PTAT}R_{2_{initial}}+CI_{NL}R_{2_{initial}}, \quad \text{(B.3)}$$

where A, B, and C are the coefficients of the temperature dependent current components,

$$A=\frac{R_1+R_2+R_3}{R_1+R_2}, \quad \text{(B.4)}$$

$$B=\frac{R_1+R_2}{R_1+R_2}=1, \quad \text{(B.5)}$$

and
$$C=\frac{R_1}{R_1+R_2}. \quad \text{(B.6)}$$

The temperature coefficient of the resistors is canceled because they are ratioed and made out of the same material, i.e.,

Aptiv Services US, LLC Exhibit 1015 Page 182

$$\frac{R_1(T)}{R_2(T)} = \frac{R_1(T_r)\cdot\left[1+A(T-T_r)+B(T-T_r)^2\right]}{R_2(T_r)\cdot\left[1+A(T-T_r)+B(T-T_r)^2\right]} = \frac{R_1(T_r)}{R_2(T_r)}, \qquad \text{(B.7)}$$

where T is temperature, A and B are the linear and the quadratic temperature coefficients of the resistor, and T_r is the reference temperature (typically room temperature).

Step 2: Data points are collected for the reference voltage (V_{ref}), node "a" (V_a), and node "b" (V_b) throughout the temperature range desired.

Step 3: Since the initial resistor ratios are known and the voltage across each resistor has been collected throughout the temperature sweep, the currents multiplied by the initial resistance of R_2 can be derived for the entire temperature range,

$$I_{V_{be}} R_{2_{initial}} = \frac{V_{ref} - V_a}{\left\langle \frac{R_3}{R_2} \right\rangle_{initial}}, \qquad \text{(B.8)}$$

$$I_{PTAT} R_{2_{initial}} = [V_a - V_b] - I_{V_{be}} R_{2_{initial}}, \qquad \text{(B.9)}$$

and

$$I_{NL} R_{2_{initial}} = \frac{V_b}{\left\langle \frac{R_1}{R_2} \right\rangle_{initial}} - [V_a - V_b]. \qquad \text{(B.10)}$$

Step 4: Equation (B.3) is temperature adjusted via a spreadsheet by using the values derived in equations (B.8) - (B.10) and adjusting the coefficients A and C (B is pre defined to be one) to yield the lowest temperature variation performance over the desired temperature range. This is a trial and error process whose results come in the form of extracted values for coefficients A and C.

Step 5: At this point, new resistor ratios for R_1/R_2 and R_3/R_2 can be derived by manipulating equations (B.4) and (B.6),

$$\frac{R_1}{R_2} = \frac{C}{1-C} \tag{B.11}$$

and

$$A = \frac{R_1+R_2+R_3}{R_1+R_2} = \frac{\frac{R_1}{R_2}+1+\frac{R_3}{R_2}}{\frac{R_1}{R_2}+1} \tag{B.12}$$

or

$$\frac{R_3}{R_2} = (A-1)\left\langle\frac{R_1}{R_2}+1\right\rangle. \tag{B.13}$$

Step 6: The values of the currents multiplied by the initial resistance of R_2 at room temperature are identified from step 3, i.e., $(I_{V_{be}}R_{2_{initial}})_{T_r}$, $(I_{PTAT}R_{2_{initial}})_{T_r}$, and $(I_{NL}R_{2_{initial}})_{T_r}$ whose values are evaluated at T_r.

Step 7: Equation (B.1) can be re expressed as

$$V_{ref}\frac{R_{2_{initial}}}{R_2} = \left\langle I_{V_{be}}[R_1+R_2+R_3]+I_{PTAT}[R_1+R_2]+I_{NL}R_1\right\rangle\frac{R_{2_{initial}}}{R_2} \qquad (B.14)$$

and consequently yield the following at room temperature,

$$V_{ref}(T_r)\cdot\frac{R_{2_{initial}}}{R_2} = (I_{V_{be}}R_{2_{initial}})_{T_r}\left\langle\frac{R_1}{R_2}+1+\frac{R_3}{R_2}\right\rangle+$$

$$(I_{PTAT}R_{2_{initial}})_{T_r}\left\langle\frac{R_1}{R_2}+1\right\rangle+(I_{PTAT}R_{2_{initial}})_{T_r}\left\langle\frac{R_1}{R_2}\right\rangle. \qquad (B.15)$$

As a result, the ratio of $R_{2initial}$ and R_2 can be derived for any desired value of $V_{ref}(T_r)$.

Step 8: If the temperature drift needs further adjustment, then the process can be repeated from step 2. An additional iteration may be warranted if the magnitude of the reference is changed significantly from its non trimmed to its trimmed state. This is because the output impedance of the mirrors generating the temperature dependent current components is finite. If the only parameter that needs adjustment is the magnitude of the reference voltage at room temperature, then the process is still repeated from step 2. However, a temperature sweep and step 4 are skipped and the values of A and C from the previous iteration are maintained. As a result, all the measurements are simply made at room temperature.

Notes: Knowledge of the absolute value of the resistors is not necessary. Instead, the intrinsic parameters that require control are the ratios of the resistors. Furthermore, if only magnitude trimming at room temperature is desired, then the procedure is the same except that measurements are only obtained at room temperature and step 4 is skipped altogether. Moreover, the values of A and C for the procedure are obtained from circuit simulations.

APPENDIX C

LAYOUT PLOTS



Figure C.1. Layout of the curvature corrected bandgap and associated start-up circuit.

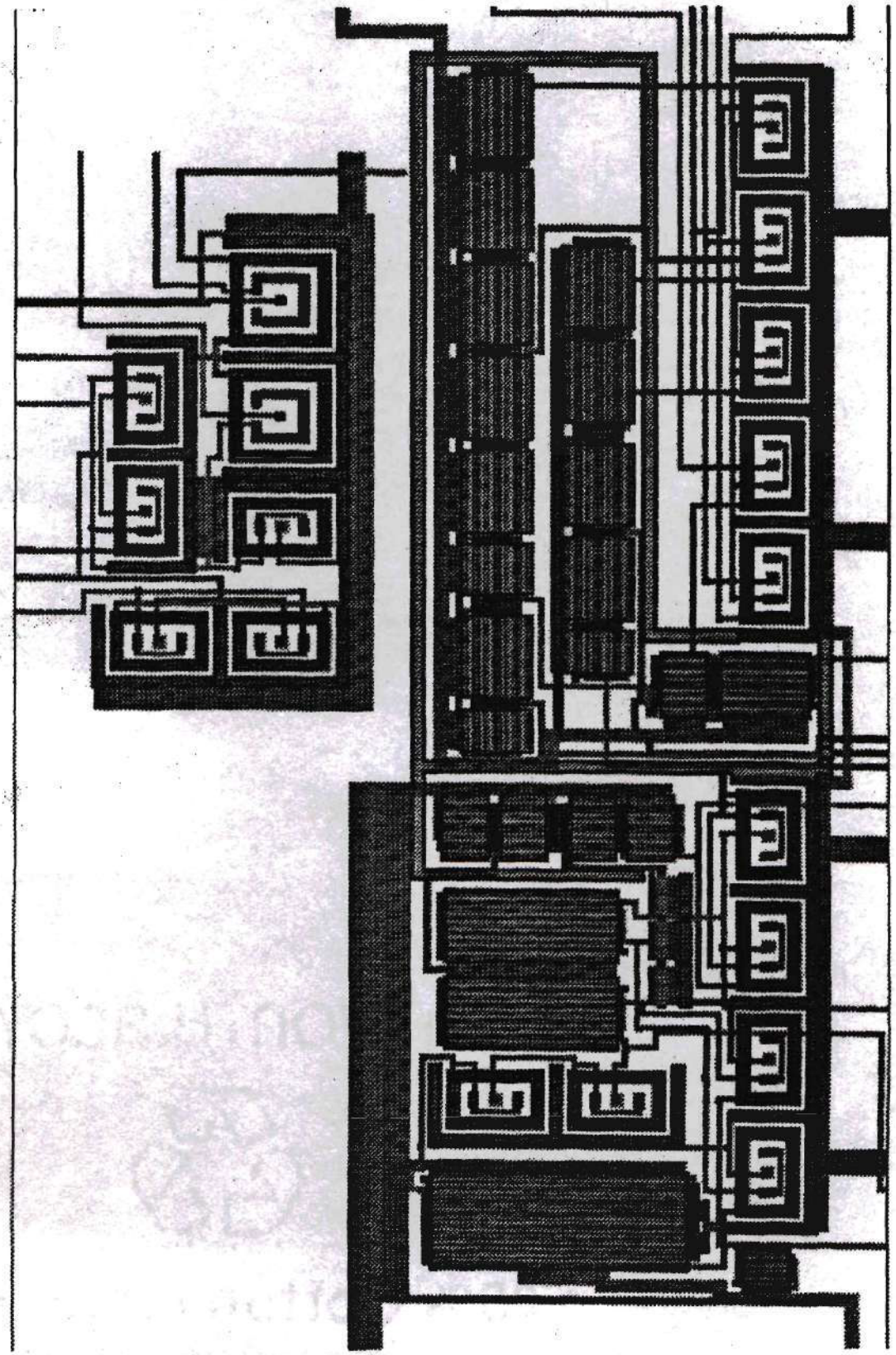


Figure C.2. Zoom-in plot of the start-up and reference (290 x 173 μm & 798 x 280 μm).

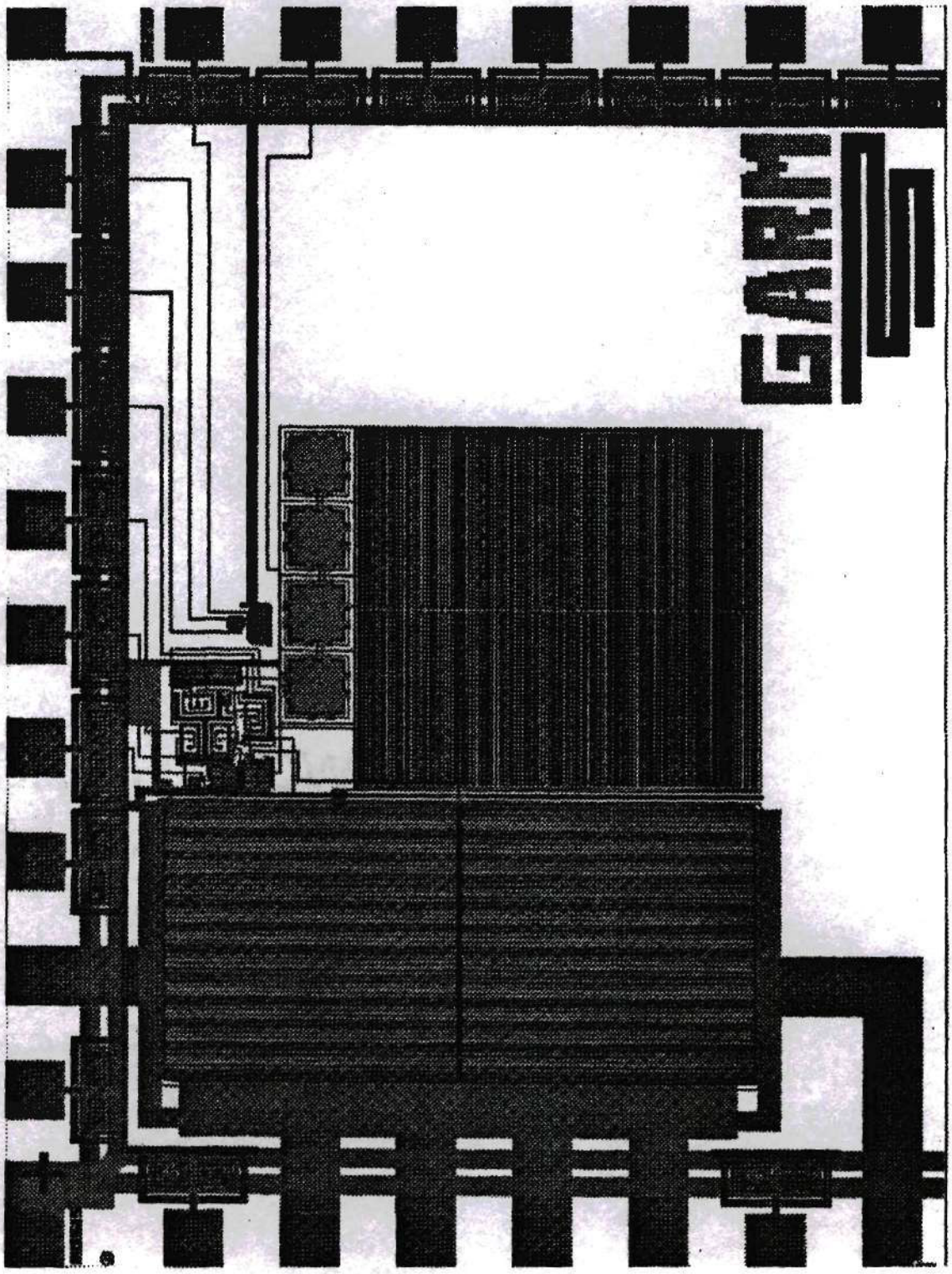


Figure C.3. Layout of the control loop (1103 x 1250 μm).

REFERENCES

[1] S. Franco, *Design with Operational Amplifiers and Analog Integrated Circuits.* New York: McGraw-Hill Publishing Company, 1988.

[2] M.M. Cirovic, Integrated Circuits: *A User's Handbook.* Reston, Virginia: Reston Publishing Company, Inc., 1977.

[3] P.R. Gray and R.G. Meyer, *Analysis and Design of Analog Integrated Circuits.* New York: John Wiley & Sons, Inc., 1993.

[4] F. Goodenough, "Low Dropout Linear Regulators," *Electronic Design*, pp. 65-77, May 13, 1996.

[5] T. Regan, "Low Dropout Linear Regulators Improve Automotive And Battery-Powered Systems," *Powerconversion and Intelligent Motion*, pp. 65-69, February 1990.

[6] J. Wong, "A Low-Noise Low Drop-Out Regulator for Portable Equipment," *Powerconversion and Intelligent Motion*, pp. 38-43, May 1990.

[7] R. Cavin and W. Liu, *Emerging Technologies, Designing Low Power Digital Systems.* Piscataway, NJ: Institute of Electrical and Electronics Engineers, 1996.

[8] M. Ismail and T. Fiez, *Analog VLSI Signal and Information Processing.* New York: McGraw-Hill, Inc., 1994.

[9] F. Goodenough, "Fast LDOs And Switchers Provide Sub-5-V Power," *Electronic Design*, vol. 43 #18, pp. 65-74, September 5, 1995.

[10] A. Matsuzawa, "Low Voltage Mixed Analog/Digital Circuit Design for Portable Equipment," *1993 Symposium on VLSI Circuits Digest of Technical Papers*, pp. 49-54, 1993.

[11] E. Nash, "Take Advantage of Fast Rail-To-Rail Op Amps in low-Voltage Systems," *Electronic Design Analog Applications Issue*, pp. 26-39, June 24, 1996.

[12] F. Goodenough, "Power-Supply Rails Plummet and Proliferate," *Electronic*

Design, pp. 51-55, July 24, 1995.

[13] K.M. Tham and K. Nagaraj, "A Low Supply Voltage High PSRR Voltage Reference in CMOS Process," *IEEE Journal of Solid-State Circuits*, vol. 30 #5, pp. 586-590, May 1995.

[14] H. Chung and A. Ioinovici, "Switched-Capacitor-Based DC-toDC Converter with Improved Input Current Waveform," *IEEE International Symposium on Circuits and Systems*, vol. 1, pp. 541-544, May 1996.

[15] G. Zhu and A. Ioinovici, "Switched-Capacitor Power Supplies: DC Voltage Ratio Efficiency, Ripple, Regulation," *IEEE International Symposium on Circuits and Systems*, vol. 1, pp. 553-556, May 1996.

[16] F. Goodenough, "90 % - Efficient 1.5 - A IC Switchers Run At 1 Mhz," *Electronic Design*, pp. 77-84, May 30, 1995.

[17] B.D. Moore, "Circuit trade-offs minimize noise in battery-input power supplies," *EDN*, pp. 107-112, January 18, 1996.

[18] F. Goodenough, "Off-Line and One-Cell IC Converters Up Efficiency," *Electronic Design*, pp. 55-64, June 27, 1994.

[19] M. Sauerwald, "Keeping Analog Signals Pure In A Hostile Digital World," *Electronic Design Analog Applications Issue*, pp. 57-64, June 24, 1994.

[20] P.E. Allen and D.R. Holdberg, *CMOS Analog Circuit Design*. New York: Holt, Rinehart and Winston, 1987.

[21] *Linear/Switchmode Voltage Regulator Handbook*. Fourth edition, 1989.

[22] R.J. Widlar, "New Developments in IC Voltage Regulators," *IEEE Journal of Solid-State Circuits*, vol. SC-6 #1, pp. 2-7, February 1971.

[23] M. Kay, "Design and Analysis of an LDO Voltage Regulator with a PMOS Power Device," Preliminary paper pending publication, Texas Instruments.

[24] *National Power IC's Databook*. 1995 edition.

[25] *MAXIM 1995 New Releases Data Book*. Vol. IV, 1995.

[26] *Texas Instruments, Linear Circuits*. Vol. 3, 1992.

[27] G.A. Rincon-Mora and P.E. Allen, "Study and Design of Low Drop-out Regulators," submitted to *IEEE Transactions on Circuits and Systems*.

[28] C.D. Motchenbacher and J.A. Connelly, *Low-Noise Electronic System Design*. New York: John Wiley & Sons, Inc., 1993.

[29] R.S. Wrathall, "A 5V 10A CMOS/PNP Linear Regulator," *IEEE International Solid-State Circuits Conference Digest*, pp. 144-145, February 14, 1985.

[30] R.A. Blauschild *et. al.*, "A New NMOS Temperature-Stable Voltage Reference," *IEEE Journal of Solid-State Circuits*, vol. SC-13 #6, pp. 767-774, December 1978.

[31] S.M. Yoo, *et. al.*, "Variable V_{cc} Design Techniques for Battery-Operated DRAM's," *IEEE Journal of Solid-State Circuits*, vol. 28 #4, pp. 499-501, April 1993.

[32] T. Osishi, *et. al.*, "A Mixed-Mode Voltage Down Converter with Impedance Adjustment Circuitry for Low-Voltage High-Frequency Memories," *IEEE Journal of Solid-State Circuits*, vol. 31 #4, pp. 575-584, April 1996.

[33] R. Buono, " MOSFET circuit ups regulator's output current," *Electronic Design*, pp. 140-142, February 1, 1996.

[34] G.L. Kmetz, "Regulator Adjusts From 0 V to 25 V," *Electronic Design*, pp. 106-108, May 13, 1996.

[35] G.A. Rincon-Mora and P.E. Allen, "A Low Voltage, Low Quiescent Current, Low Drop-out Regulator.," submitted to *IEEE Journal of Solid-State Circuits*.

[36] P.E. Allen, B.J. Blalock, and G.A. Rincon, "Low-Voltage Analog Circuits Using Standard CMOS Technologies," *Proc. International Symposium on Low Power Design*, pp. 209-214, 1995.

[37] J.P. Uyemura, *Fundamentals of MOS Digital Integrated Circuits*. Massachusetts: Addison-Wesley, 1988.

[38] T. Shibata and T. Ohmi, "A Functional MOS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations", *IEEE Transactions on Electron Devices*, vol. 39 #6, pp. 1444-1455, June 1992.

[39] A.S. Sedra and K.C. Smith, *Microelectronic Circuits*. New York: Holt, Rinehart and Winston, Inc., 1987.

[40] M. Gunawan *et. al.*, "A Curvature-Corrected Low-Voltage Bandgap Reference," *IEEE Journal of Solid-State Circuits*, vol. 28 #6, pp. 667-670, June 1993.

[41] R.J. Reay, *et. al.*, "A Micromachined Low-Power Temperature-Regulated Bandgap Voltage Reference," *IEEE Journal of Solid-State Circuits*, vol. 30 #12, pp. 1374-1381, December 1995.

[42] P. Gray, "Advanced Analog Integrated Circuits," Lecture Notes and Diagrams from the University of California at Berkeley, 1991.

[43] W.T. Holman, "A New Temperature Compensation Technique for Bandgap Voltage References," *IEEE International Symposium on Circuits and Systems*, vol. 1, pp.385-388, 1996.

[44] I. Lee *et. al.*, "Exponential Curvature-Compensated BiCMOS Bandgap References," *IEEE Journal of Solid-State Circuits*, vol. 29 #11, pp. 1396-1403, November 1994.

[45] G.M. Meijer *et. al.*, "A New Curvature-Corrected Bandgap Reference," *IEEE Journal of Solid-State Circuits*, vol. SC-17 #6, pp. 1139-1143, December 1982.

[46] J.I. Miyamoto *et. al.*, "A High-Speed 64K CMOS RAM with Bipolar Sense Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. SC-19 #5, pp. 557-563, October 1984.

[47] P.E. Allen, B.J. Blalock, and G.A. Rincon, "A 1V CMOS op amp using bulk-driven MOSFETs," *IEEE International Solid-State Circuits Conference Digest*, pp. 192-193, February 1995.

[48] G.A. Rincon-Mora and P.E. Allen, "A Novel Low Voltage, Micro-Power Curvature Corrected Bandgap Reference," submitted to *IEEE Journal of Solid-State Circuits*.

[49] D. Davis, "Overload and reverse-current circuitry protects battery and load," *Electronic Design*, pp. 165-170, March 1, 1996.

[50] W. Jung and A. Garcia, "Solve Your Low-Voltage System Design Problems," *Electronic Design Analog Applications Issue*, pp. 8-23, November 20, 1995.

[51] Y.P. Tsividis, "Accurate Analysis of Temperature Effects in I_C-V_{be} Characteristics with Application to Bandgap Reference Sources," *IEEE Journal of Solid-State Circuits*, vol. SC-15 #6, pp. 1076-1084, December 1980.

Aptiv Services US, LLC Exhibit 1015 Page 193

VITA

Gabriel Alfonso Rincon-Mora was born in Caracas, Venezuela, on January 30, 1972, to Gilberto and Gladys M. Rincon. Gabriel was raised in Maracay, Venezuela after his family moved there in 1974. His family moved to the United States in 1983 and resided in North Miami Beach, Florida. He attended North Miami Beach Senior High School where he graduated in 1989 with High Honors and at the top of his class. Among other honors, Gabriel was awarded a Certificate for scholastic excellence in Mathematics, a Certificate for scholastic excellence in Science, and the Presidential Academic Fitness Award signed by President George Bush. This resulted in three scholarships to attend college, namely, Faculty Scholars' from Florida International University, Florida Undergraduate Scholars' from the state of Florida, and the Insignis Scholarship from the University of Detroit. He attended Florida International University from 1989 to 1992 where he received a Bachelor of Science in Electrical Engineering with High Honors, graduating at the top of his class. Amid the honors bestowed upon him, Gabriel was in the Florida International University Dean's List, was given Honorary Award Recognition in the National Dean's List, and was given Honorable Mention by the National Science Foundation. In 1993, Gabriel went to Georgia Institute of Technology to pursue a Master of Science in Electrical Engineering, which he received in June of 1994. He remained at Georgia Institute of Technology to pursue a Ph.D. in Electrical Engineering, which he received in December of 1996. The work at Georgia Institute of Technology resulted in the submission of seven papers to various journal publications. During his graduate program, he worked one summer for Northern Telecom and six months for Texas Instruments Incorporated, which led to the application of four patents, three of which have

been issued and one is still pending. Gabriel is a member of IEEE, Tau Beta Pi, Alpha Omega Chi, and Eta Kappa Nu, where he served as secretary of the local chapter in Florida International University. Upon graduation, Gabriel accepted a position with the standard linear design group at Texas Instruments Incorporated in Dallas, Texas.