

Patent No. 9,471,074
Petition For *Inter Partes* Review

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APTIV SERVICES US, LLC
Petitioner,

v.

MICROCHIP TECHNOLOGY, INC.
Patent Owner.

Patent No. 9,471,074

Case No. IPR2024-00646

DECLARATION OF DR. MICHAEL S. CHEN

Inter Partes Review of U.S. Patent No. 9,471,074

I, Dr. Michael S. Chen, make this declaration in connection with the proceeding identified above.

I. INTRODUCTION

1. I have been retained by counsel for Aptiv Services US, LLC (“Aptiv”) as a technical expert in connection with the proceeding identified above. I submit this declaration in support of Aptiv’s Petition for *Inter Partes* Review of United States Patent No. 9,471,074 (the “’074 patent”). I have personal knowledge of the facts and opinions set forth in this declaration and believe them to be true. If called upon to do so, I would testify competently thereto. I have been warned that willful false statements and the like are punishable by fine or imprisonment, or both.

2. I am being paid at an hourly rate for my work on this matter. I have no personal or financial stake or interest in the outcome of the present proceeding.

3. I have reviewed and am familiar with the ’074 patent. I understand that all 18 claims of the ’074 patent are being challenged.

4. In this declaration, I present certain opinions regarding the knowledge and skill of a person of ordinary skill in the art (“POSITA”), and regarding whether such a person would have found the claims of the ’074 patent obvious in view of the prior art as of the patent’s claimed priority date of March 14, 2013. I conclude that a POSITA would have found each claim obvious under both petitioned grounds.

5. I note that some of my opinions assume specific interpretations of claim elements with which I do not necessarily agree. I present these opinions because I have been asked to consider whether a POSITA would find the claims obvious over the petitioned grounds if these interpretations applied. I will identify these opinions as they arise below.

II. QUALIFICATIONS

6. I am a tenured full professor of Electrical Engineering at the University of Southern California, where I have been a faculty member since 2011. As a professor, I research and teach electrical circuit design. My research focuses on analog mixed-signal and RF circuit architectures for data converters (both ADC and DAC), clock generation (such as PLL and DLL), digital VLSI, SoC, mostly-digital circuits, artificial intelligence (AI) and machine learning (ML) accelerators, analog CAD, and power amplification (PA). My research has been applied to wireless, wireline communications, computing, IoT systems, autonomous vehicles, etc.

7. I earned my Ph.D. and M.Sc. in Electrical Engineering and Computer Science from the University of California, Berkeley in 2006 and 2002 respectively. I received my B.S. degree from National Taiwan University, where I graduated as the top student in the upper division.

8. My work has been recognized by both academic and commercial entities. I have published over 90 conference, journal, magazine articles, including

multiple publications in the IEEE International Solid State Circuits Conference (ISSCC), IEEE Symposium on VLSI Circuits (VLSIC), IEEE Custom Integrated Circuits Conference (CICC), IEEE European Conference on Solid-State Circuit (ESSCIRC), IEEE Radio Frequency Integrated Circuits Symposium (RFIC), IEEE Journal of Solid-State Circuits (JSSC), and Transactions on Circuit and System I (TCAS-I). My research has been funded by the National Science Foundation (NSF), ONR, IARPA, SRC, DARPA and various industry companies. I have also served as a technical consultant for companies including Qualcomm, Tetramem, BAE Systems and Samsung.

9. I have received recognition for my work and research. In 2024, I was honored with the grade of IEEE Fellow to recognize my technical contributions in solid-state circuit society. This grade is reserved for 0.1% of IEEE members. In 2023, I was the co-recipient of the ISSCC Jack Kilby Award for significant advances in analog mixed-signal circuits. In 2022, I was a co-recipient for the RFIC 2022 Best Student Paper Award for my work with students in my laboratory on a circuit prototype. From 2021 to 2023, I was the IEEE Solid-State Circuit Society (SSCS) Distinguished Lecturer. I have been invited to offer seminars, workshops, keynote talks, and panel discussions in major IEEE conferences, IEEE SSCS chapters, and universities on a range of topics covering fundamental to advanced integrated circuit design and how to improve the performance and/or reduce cost of a circuit or system.

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In 2019, I was also the recipient of Qualcomm Faculty Award, and in 2014 both the NSF Faculty Early Career Development (CAREER) Award and DARPA Young Faculty Award (YFA). As a student, I was the recipient of a UC Regents' Fellowship at Berkeley in 2000 and the Analog Devices Outstanding Student Award for IC design in 2006.

10. I have extensive experience and familiarity with voltage regulators. Most of my past and ongoing research and industry projects have incorporated or used voltage regulators, as they provide a fundamental power management block needed to regulate a supply voltage for proper circuit operation. In addition, I have been teaching various circuit courses at USC, and basic voltage regulator models such as the low-dropout regulator is a common circuit example I use to illustrate for my students how feedback circuits and various related components can be designed and implemented.

11. A copy of my curriculum vitae is attached as Appendix A.

III. MATERIALS CONSIDERED

12. In preparing this declaration, I have reviewed, among other things, the following materials:

Document	Exhibit #
U.S. Patent No. 9,471,074	1001

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Prosecution History of U.S. Patent No. 9,471,074	1003
Mohammad Al-Shyoukh, et al., “A Transient-Enhanced Low-Quiescent Current Low-Dropout Regulator with Buffer Impedance Attenuation,” <i>IEEE Journal of Solid-State Circuits</i> , Vol. 42, No. 8 (Aug. 2007) (“Al-Shyoukh”)	1004
U.S. Patent No. 6,400,207 (“Ivanov”)	1005
U.S. Patent No. 6,710,583 (“Stanescu”)	1006
Miranda J. Ha, “A Low-Power, High-Bandwidth LDO Voltage Regulator with No External Capacitor” (May 23, 2008) (“Ha”)	1007
Le Ye, et al., “Highly Power-Efficient Active-RC Filters with Wide Bandwidth-Range Using Low-Gain Push-Pull Opamps,” <i>IEEE Transactions on Circuits and Systems—I: Regular Papers</i> , Vol. 60, No. 1 (Jan. 2013) (“Ye”)	1008
Mikhail Popovich, “High Performance Power Distribution Networks with On-Chip Decoupling Capacitors for Nanoscale Integrated Circuits” (2007) (“Popovich”)	1009
U.S. Patent No. 7,345,547 (“Wang”)	1010
Micrel Inc., MIC59300 Datasheet (Jan. 2009) (“MIC59300”)	1011
U.S. Patent No. 7,644,217 (“Butler”)	1012
U.S. Patent No. 6,046,577 (“Rincon-Mora”)	1013
Gabriel A. Rincon-Mora, “A Low-Voltage, Low Quiescent Current, Low Drop-Out Regulator,” <i>IEEE Journal of Solid-State Circuits</i> , Vol. 33, No. 1 (Jan. 1998) (“Rincon-Mora Paper”)	1014
Gabriel A. Rincon-Mora, “Current Efficient, Low Voltage, Low Dropout Regulators” (Nov. 1996) (“Rincon-Mora Dissertation”)	1015
U.S. Patent No. 6,084,475 (“Rincon-Mora ’475”)	1016

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Michael Day, “Understanding Low Drop Out (LDO) Regulators,” 2006 Texas Instruments Portable Power Design Seminar (2006) (“Day”)	1017
Chester Simpson, “Linear and Switching Voltage Regulator Fundamental Part I” (2011) (“Simpson”)	1018
U.S. Provisional Patent Application No. 61/780,985	1019

13. I have also reviewed the Petition for *Inter Partes* Review of the '074 patent, to which my declaration relates.

IV. DEFINITIONS AND STANDARDS

14. I have been informed and understand that claims are construed from the perspective of a POSITA at the time of the claimed invention, and that during *inter partes* review, claims are given their broadest reasonable construction consistent with the specification.

15. I have been informed and understand that the subject matter of a patent claim is obvious if the differences between the subject matter of the claim and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains.

16. I have been informed that the framework for determining obviousness involves considering the following factors: (i) the scope and content of the prior art;

(ii) the differences between the prior art and the claimed subject matter; (iii) the level of ordinary skill in the art; and (iv) any objective evidence of non-obviousness.

17. I understand that the claimed subject matter would have been obvious to one of ordinary skill in the art if, for example, it results from the combination of known elements according to known methods to yield predictable results, the simple substitution of one known element for another to obtain predictable results, use of a known technique to improve similar devices in the same way or applying a known technique to a known device ready for improvement to yield predictable results. I have also been informed that the analysis of obviousness may include recourse to logic, judgment and common sense available to the person of ordinary skill in the art that does not necessarily require explication in any reference.

V. TECHNICAL BACKGROUND

18. In the following sections, I present some background principles from analog circuit design that would have been known to a POSITA in March 14, 2013.

A. Voltage Regulators

19. The '074 patent relates to a voltage regulator, and specifically a type of linear voltage regulator that was known in the art as a low-dropout voltage regulator, or "LDO," as of 2013. The following paragraphs provide a brief overview of voltage regulators as they were understood in the art at that time. I note, however, that these principles of voltage regulator operation had been known long before 2013, as will

be evident from my discussion of specific prior art references in later sections of this declaration.

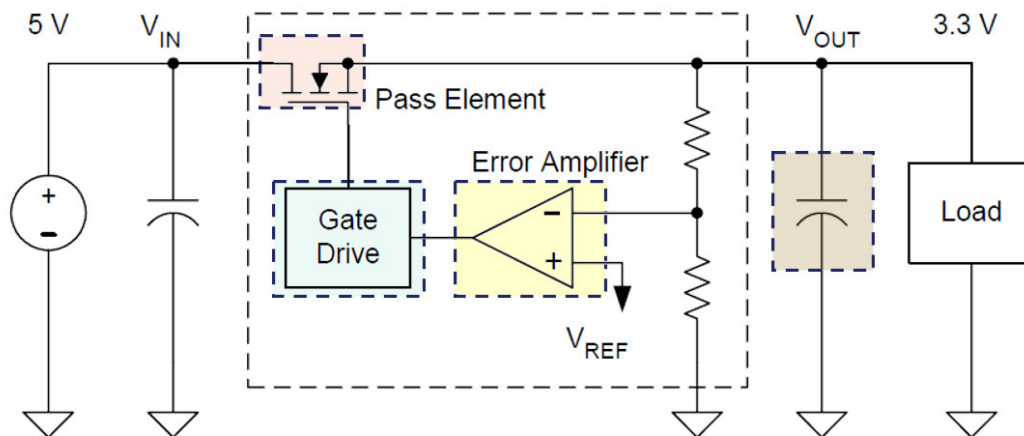
20. Power supplies for electronics, such as batteries, were typically subject to wide variations in voltage and current when operating under changing conditions. In an integrated circuit, for example, a supply could be required to power a variety of components that draw different amounts of energy at different times, depending on their usage. These changing conditions introduced frequency fluctuations to the circuit. Thus, it was common to use a component known as a “voltage regulator” to absorb and eliminate these fluctuations and output a constant and stable voltage.

21. A well-known structure for voltage regulators in 2013 was the “linear voltage regulator,” comprising an operational amplifier (or “op-amp”), and an output pass device driven by the output of the op-amp. The pass device could, for example, be a MOSFET or bipolar junction transistor (“BJT”), and output the desired voltage to the load. The op-amp’s two differential voltage inputs would have been a voltage reference and a feedback input coupled to the output of the pass device. In this way, the op-amp could sense what voltage the load was receiving and correct it as needed.

22. LDOs were a well-known type of linear voltage regulator. Unlike the standard linear regulator, an LDO could operate with a low dropout voltage, as the name suggests. “Dropout voltage” means the difference between the supply voltage and the output voltage. This was important because the power efficiency of a linear

regulator depends on the dropout voltage and quiescent current. A smaller dropout voltage leads to higher power efficiency for the voltage regulator.

23. A typical LDO structure is shown below:



As with linear regulators generally, the LDO comprises an amplifier (highlighted in yellow) driving a pass device (red), the output of the pass device feeding back to one of the amplifier's differential inputs. The figure above also shows something called a "gate drive" (green), which is the element through which the amplifier drives the pass device. This element can be, for example, a buffer driver, as in the '074 patent. (I have adapted the figure above from a paper by Michael Day of Texas Instruments that I understand was presented at a seminar in 2006. (See EX1017, Fig. 2.) I note that although the copy of this paper accessed through the Texas Instruments website at <https://www.ti.com/lit/slup239> on February 18, 2024 bears a copyright stamp of 2019, I can confirm based on my personal knowledge that the general LDO structure

shown above was widely known in the field in 2006, and certainly by 2013. In any event, I use the figure here simply to present my own opinions and expertise on the background of the art.)

24. LDOs also work with a capacitor (highlighted in brown above) coupled to the output in parallel to the load. The purpose of this capacitor is to stabilize the circuit when responding to changes in load by providing a dominant pole that can improve the phase margin (see below).

B. Frequency Response

25. A circuit's "frequency response" is the behavior of the gain and phase of the circuit's transfer function in response to changes in frequency. The frequency response is useful for assessing the stability of the circuit, among other things. A critical point in the frequency response is the "unity gain frequency" or "UGF," the frequency at which gain is a factor of 1 (or 0 dB). If the corresponding phase at UGF is at or less than -180° (*i.e.*, the "phase margin," or difference between phase at UGF and -180° is not positive), the circuit will become unstable because it will effectively form a positive feedback loop, causing the circuit to saturate or oscillate (forms of instability).

26. Furthermore, a frequency response can include points known as "poles" and "zeros." These are best understood by expressing the Laplace transform of a

circuit's continuous-time transfer function $H(s)$ as a ratio of a numerator function $N(s)$ and a denominator function $D(s)$:

$$H(s) = N(s)/D(s)$$

The poles of the transfer function are the roots of $D(s)$, while the zeros are the roots of $N(s)$. When evaluating the frequency response, a POSITA would have known to substitute the variable s with $j\omega$, where j is the imaginary unit and ω is the frequency. With this substitution, the magnitude of gain and the phase of the transfer function $H(j\omega)$ is often represented as a Bode plot (*e.g.*, Fig. 1 of the '074 patent), where poles and zeros at different locations can be seen introduces magnitude and phase changes as the frequency increases. The poles and zeros combined to determine the phase at UGF, and thus the phase margin. A POSITA would have understood that judiciously adjusting the poles and zeros of a circuit could improve phase margin and thus the overall stability of the circuit.

27. In a voltage regulator, the dominant pole is typically located at the output of the regulator. This pole varies based on the load because the pole depends on the output resistance of the pass device, which is a function of the load current. In addition, a voltage regulator has another pole at the gate of the pass device, caused by parasitic capacitance from components internal to the voltage regulator. If this parasitic pole is located at a low frequency (*i.e.*, well within the UGF), it can cause

instability because it would add additional phase shift to that of the dominant pole, degrading the phase margin.

28. Furthermore, output capacitors have an equivalent series resistance (or “ESR”) due to the material that makes up the capacitor. This ESR introduces another pole, and a zero. Because the value of ESR can affect the location of the added zero and pole, the ESR can destabilize the circuit (*i.e.*, cause poor phase margin at UGF), if its value is outside an acceptable range. The output capacitor must therefore be chosen carefully to match the design of the LDO.

C. Transconductance

29. Transconductance, or “gm,” is an electrical characteristic that describes the current output by a circuit component relative to the input voltage imposed across the input terminal. Transconductance is generally calculated as the derivative of output current (I_{out}) over input voltage (V_{in}):

$$gm = \frac{dI_{out}}{dV_{in}}$$

30. In a bipolar junction transistor (BJT), the output current is the collector current (I_c) and the input voltage (V_{be}) is applied between the BJT’s base and emitter terminals. The transconductance is given below, where K is the Boltzman constant and T is the absolute temperature:

$$gm = \frac{\partial I_c}{\partial V_{be}} = \frac{I_c}{VT} = \frac{qI_c}{KT}$$

31. In a MOSFET, the output current is the drain current (I_d) and the input voltage (V_{gs}) is applied between the gate and source terminals. Assuming a square-law device for the MOSFET, transconductance is given as:

$$gm = \frac{\partial I_d}{\partial V_{gs}} = \sqrt{2\mu C_{ox} \frac{W}{L} I_d} = \frac{2I_d}{V_{gs} - V_{th}}$$

Here, μ is the mobility, C_{ox} is the gate capacitance per unit area, W is channel width, L is channel length, and V_{th} is the threshold voltage of the MOSFET. Thus, as with BJTs, the transconductance increases with the current flowing through the device.

VI. THE '074 PATENT

32. The '074 patent is directed to an LDO that is based on the conventional LDO model I have described above. As shown in Figure 2, the '074 patent's LDO includes an amplifier (shown in yellow) that controls a pass device (red) via a gate drive (green), the pass device feeding back to the amplifier via a feedback loop, and a capacitor (brown) coupled to the pass device and the load:

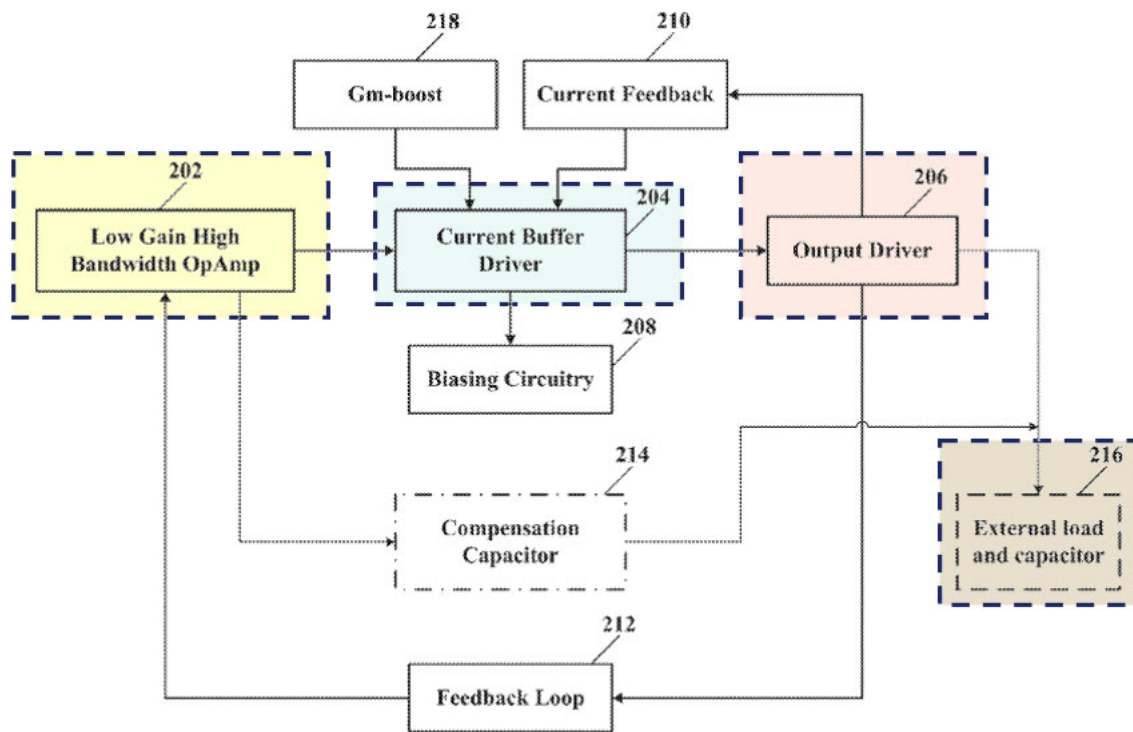


FIGURE 2

(EX1001, Fig. 2 (annotated).)

33. As I understand it, the problem that the '074 patent purports to solve is that for capacitor-less applications, “[a]n external [output] capacitor is needed,” but “[t]he external capacitor may have very different ESR (equivalent series resistance) values ranging from a few milliohms to tens of ohms causing the output pole-zero locations to shift drastically.” (EX1001, 3:18-25.) In other words, the '074 patent identifies applications where, because the output capacitor must be external to the voltage regulator, the properties of the capacitor (such as ESR) are unpredictable. If the ESR is outside the range that the regulator can accommodate, then the shifting

“pole-zero locations” in the regulator’s frequency response can create instability in the circuit. In addition, according to the patent, this problem is compounded by the fact that the parasitic “gate pole” of the output driver (*i.e.*, pass device) tends to be at a lower frequency when the output driver is large, because its gate capacitance is large. (*Id.*, 3:8-14, 4:6-11.) As noted above, a low-frequency parasitic pole can lead to instability. Thus, the patent seeks “to push the gate pole of the last stage PMOS power transistor [(*i.e.*, the output driver or pass device)] to a higher frequency.” (*Id.*, 3:25-28.) This, the patent claims, would “significantly improve the range of external capacitors with small to large ESR [(equivalent series resistance)] values” that the regulator can accommodate. (*Id.*, 1:55-59.)

34. The proposed method of pushing the gate pole to a higher frequency is increasing the buffer driver’s transconductance (“gm”), as doing so would lower the output impedance of the buffer, on which the gate pole depends. (EX1001, 4:6-15.) In particular, the patent proposes a “gm-boost circuit” with a “gm-boost technique” involving a “current feedback” between the output driver and the buffer. (*Id.*, 4:15-20, 4:64-5:7.) Doing so, according to the patent, reduces the voltage regulator to “a pseudo ‘one-pole’ system that is independent from the output pole changing so long as it falls within the bandwidth of the system,” and “the range of ESR is extended along with the output capacitance.” (*Id.*, 5:40-46.)

35. Although the patent does not explain in much detail how its “gm-boost technique” operates, a POSITA would have understood it as follows: Reproduced below is Figure 3B of the patent, with the buffer driver highlighted in green, and the current feedback circuit in blue:

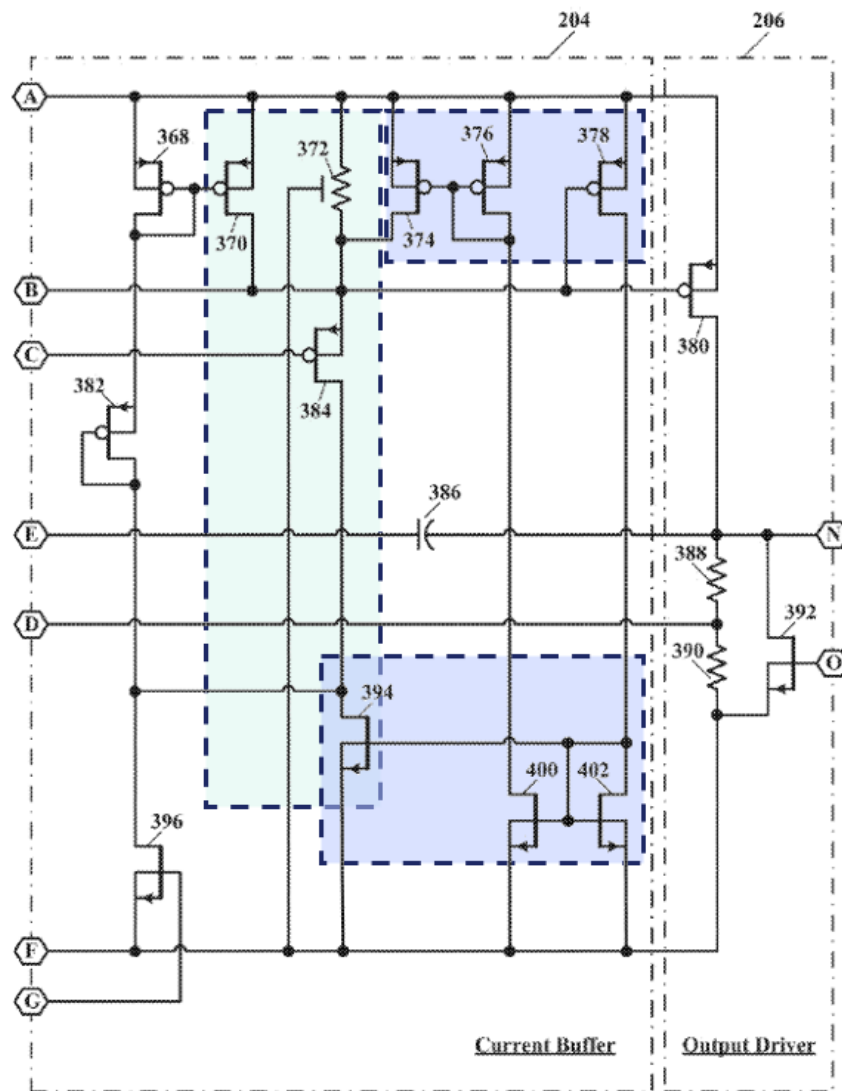


FIGURE 3B

(*Id.*, Fig. 3B (annotated).) This coloration follows the patent’s identification of what circuit elements are part of what component (the buffer driver or the current feedback circuit.) (*Id.*, 5:10-15.)

36. When the current at the power output transistor 380 of the output driver changes, transistor 378 senses the change because it is coupled to the gate of 380 at node B. This causes the current of 378 to change; for example, when adding a load, the output driver outputs more current, causing the voltage at node B to decrease. Transistor 378 then outputs more current because its source-gate voltage increases. The current from 378 then flows to transistor 402 and is mirrored to transistors 394 and 400. This increases the current in transistor 384, because 394 pulls current from 384. And as 384 is the driver transistor of the buffer driver, the boost in current also boosts gm. The patent describes this transistor as a “source follower.” (*Id.*, 4:36.) In addition, the current in transistor 400 pulls current from transistor 376, which mirrors to transistor 374, which provides current to transistor 384. Thus, the circuit boosts gm a second way.

37. There is a third way in which the “gm-boost stage” boosts gm, although the patent does not define the transistors involved to be part of the “current feedback circuit.” (*Id.*, 5:8-24.) Transistors 368 provides current not only to transistor 394 (part of the current feedback circuit), but also to transistor 396, whose current is set by the gate voltage provided by the bias network at node G. Under some conditions,

an increase in current at transistor 394 may cause a corresponding increase in current at transistor 368, which itself is mirrored to transistor 370. As transistor 370 provides current to driver transistor 384, this third pathway also provides a gm boost.

VII. LEVEL OF ORDINARY SKILL IN THE ART

38. In my opinion, a POSITA in the field of the '074 patent in 2013 would have had at least a Master's Degree in Electrical Engineering, or a Bachelor's Degree in Electrical Engineering plus two years of experience working on analog circuit design.

VIII. ANALYSIS OF THE PETITIONED GROUNDS

39. I understand that Aptiv challenges claims 1-18 of the '074 patent based on a first ground of obviousness based on Al-Shyoukh, Ivanov, and Stanescu, and a second ground of obviousness based on three related references authored by Rincon-Mora, Al-Shyoukh, Ivanov, and Stanescu. My opinions regarding these grounds are presented below.

A. Ground 1 (Al-Shyoukh, Ivanov, and/or Stanescu)

40. I have reviewed Exhibit 1004 to the Petition, which is a paper written by Mohammad Al-Shyoukh, *et al.*, and published the *IEEE Journal of Solid-State Circuits* in 2006. I will refer to this paper as "Al-Shyoukh." Having compared Al-Shyoukh's disclosures to the '074 patent's claims, it is my opinion that the claims are obvious over Al-Shyoukh in view of the background knowledge of a POSITA

and two prior art patents: U.S. Patent No. 6,400,207 to Ivanov (“Ivanov”), and U.S. Patent No. 6,710,583 to Stanescu (“Stanescu”).

1. Summary of Al-Shyoukh

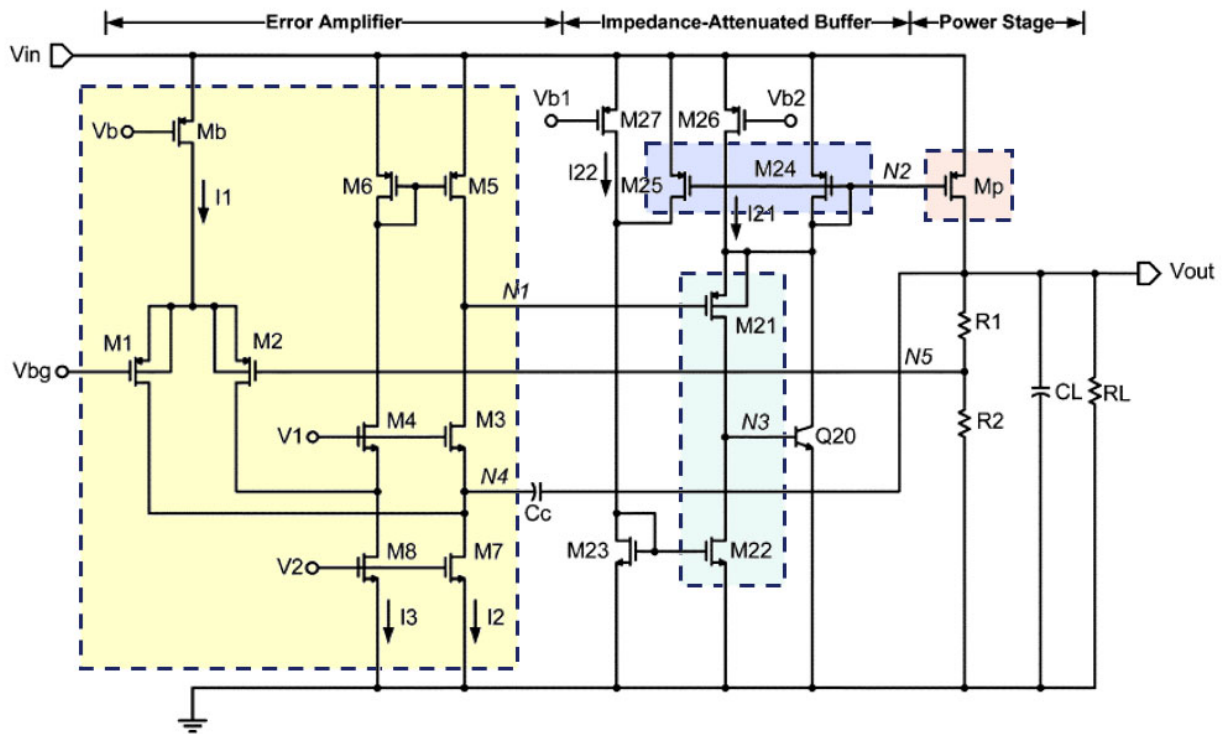
41. Al-Shyoukh is about a “transient-enhanced low-quiescent current low-dropout regulator with buffer impedance attenuation.” (EX1004, Title.) At a high level, it is concerned with power efficiency, especially in “battery-powered portable devices such as cellular phones and PDAs” where one must “reduce the standby power [to] prolong the battery runtime.” (*Id.*, 1732.) Al-Shyoukh identifies LDOs as suitable voltage regulators for these applications because “they can provide regulated low-noise and precision supply voltages for noise-sensitive analog blocks.” (*Id.*) It also notes that the high “level of integration” in these applications require the LDO to “deliver high load current,” while reducing “no-load quiescent current,” for “current efficiency.” (*Id.*)

42. Al-Shyoukh explains further that in an LDO “the ability to source high load current while achieving low dropout voltage requires the use of a large size pMOS transistor as the pass device.” (*Id.*) But this means that the transistor’s large gate capacitance creates a “low-frequency non-dominant pole within the unity-gain frequency of the regulation loop,” in addition to the “low-frequency dominant pole generated by the output capacitor.” (*Id.*) This can lead to instability in the circuit, as explained above.

43. To solve this problem, Al-Shyoukh's proposes an LDO design that uses an "impedance-attenuated buffer" to provide "[g]ood load transient response with small output-voltage variation," two things that are "critical to prevent an accidental turn off or resetting of the portable device." (*Id.*, 1732-33.) The result, Al-Shyoukh explains, is that the LDO can operate with "only a single pole is realized within the unity-gain frequency," a "good phase margin is achieved for the entire load current range with a small compensation capacitor," and the LDO exhibits "good transient settling behavior and small output-voltage variation even if a small output capacitor is used." (*Id.*, 1733.)

44. A POSITA would thus have found the problems laid out by the '074 patent and Al-Shyoukh to be closely related (pertaining to a low-frequency parasitic pole caused by a need for a large pass device), the solutions to be largely identical (providing current feedback to push the parasitic pole to higher frequencies), and the benefits to be similar (reduced internal compensation capacitance and a wider range of permissible capacitors). (EX1001, 1:55-59, 3:40-45, 5:45-49.)

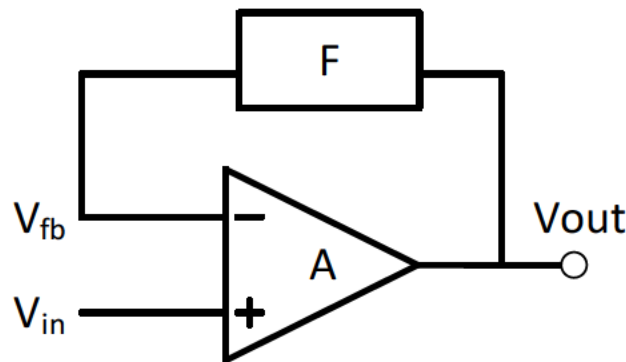
45. The layout of Al-Shyoukh's LDO is shown below:



(EX1004, Fig. 8 (annotated).) Like the typical LDO and the '074 patent, this LDO comprises an error amplifier (highlighted in yellow), a buffer driver (green), and a pass device (red), which supplies the output voltage V_{out} and is driven by the buffer. The buffer further includes circuit elements (blue) that provide current feedback in the same way that the current feedback circuit of the '074 patent does, as discussed further below.

46. Al-Shyoukh's amplifier has a single-stage folded cascode operational amplifier structure, with "a simple diode-connected active load using transistors M_5 and M_6 ." (*Id.*, 1738.) One of the differential inputs is a reference voltage V_{bg} , (*e.g.*, from a "1-V bandgap voltage reference"). (*Id.*, Fig. 8.) The other is feedback from

the pass device via node N₅. (*Id.*) The amplifier outputs a voltage at node N₁ to the gate of transistor M₂₁ of the impedance-attenuated buffer's driver. (*Id.*) Configured in this way, the error amplifier keeps the voltage regulator's output voltage close to the reference voltage. This can be understood using the simplified circuit diagram below which shows the error amplifier, buffer driver and output power driver stages grouped together as a feedforward amplifier with overall gain A, and the resistor ladder (R₁ and R₂ above) providing a feedback voltage (V_{fb}) with a feedback ratio of F, where V_{fb} is the voltage of node N₅ and V_{in} is the reference voltage V_{bg}:



As a POSITA would have understood, the ratio V_{fb}/V_{in} under this configuration can be expressed as:

$$\frac{A \times F}{1 + A \times F}$$

Therefore, when the feedforward gain A is sufficiently large, this ratio approaches 1, bringing V_{fb} very close to V_{in} (*i.e.*, the LDO's output feedback voltage at node N₅ would be brought very close to the reference voltage).

47. The current feedback circuit in Al-Shyoukh operates as follows: When the load current through pass device M_p increases (such as when going from no load to full load), the voltages at nodes N_1 and N_2 to decrease, which increases the source-gate voltage of M_{24} , which increases the current in M_{24} , which increases the current mirrored in M_{25} , which increases the current in M_{23} , which increases the current mirrored in M_{22} , and, finally, increases the current in M_{21} , which boosts g_{m21} , the transconductance of M_{21} . (*Id.*, 1734.) By contrast, when the LDO goes from full load to no load, the voltage increases at N_1 . (*Id.*) M_{24} provides “extra transient current to charge C_p ” (*i.e.*, the capacitance at N_2), and to “increase the voltage at N_2 to follow the voltage change at N_1 with a faster slewing.” (*Id.*, 1735.) Thus, Al-Shyoukh’s current feedback circuit improves “slewing of the gate drive at N_2 during load transients,” moves parasitic pole p_2 to “high frequencies under different load currents,” and allows the regulator to dissipate “low quiescent current at no-load.” (*Id.*)

48. The following paragraphs contain my opinions regarding Al-Shyoukh’s disclosure of the claim elements of the ’074 patent on an element-by-element basis.

2. Claim-by-Claim Analysis

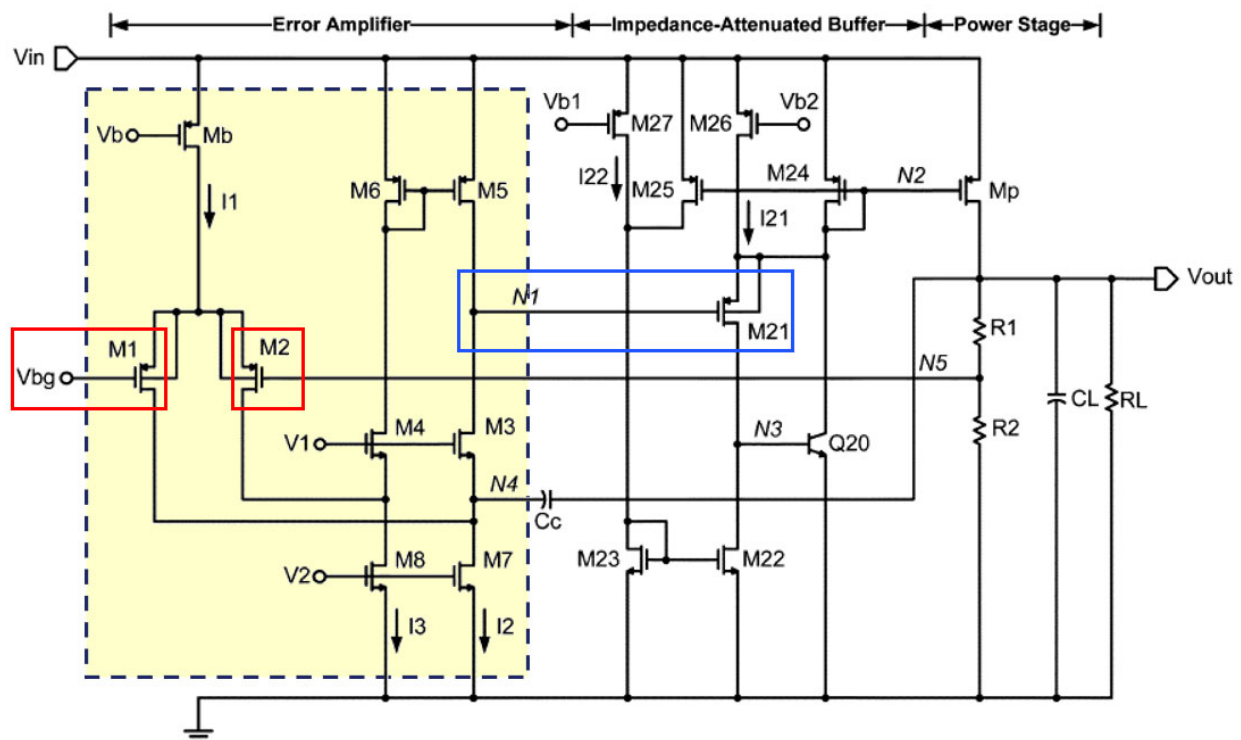
Claim 1 A voltage regulator, comprising:

49. I have explained above that Al-Shyoukh discloses an LDO-type voltage regulator. (EX1004, Abstract.)

[a] an operational amplifier;

50. An operational amplifier, as a POSITA would have understood it, is a device that receives two input voltages (called a “differential input”) and outputs a voltage that is a multiple of the difference between the inputs.

51. Al-Shyoukh’s error amplifier is an operational amplifier. (EX1004, 1738, Fig. 8.) Highlighted in yellow below, the error amplifier has differential input voltages at transistors M₁ and M₂ (red), and outputs a voltage at node N₁ to the gate of transistor M₂₁ (blue):

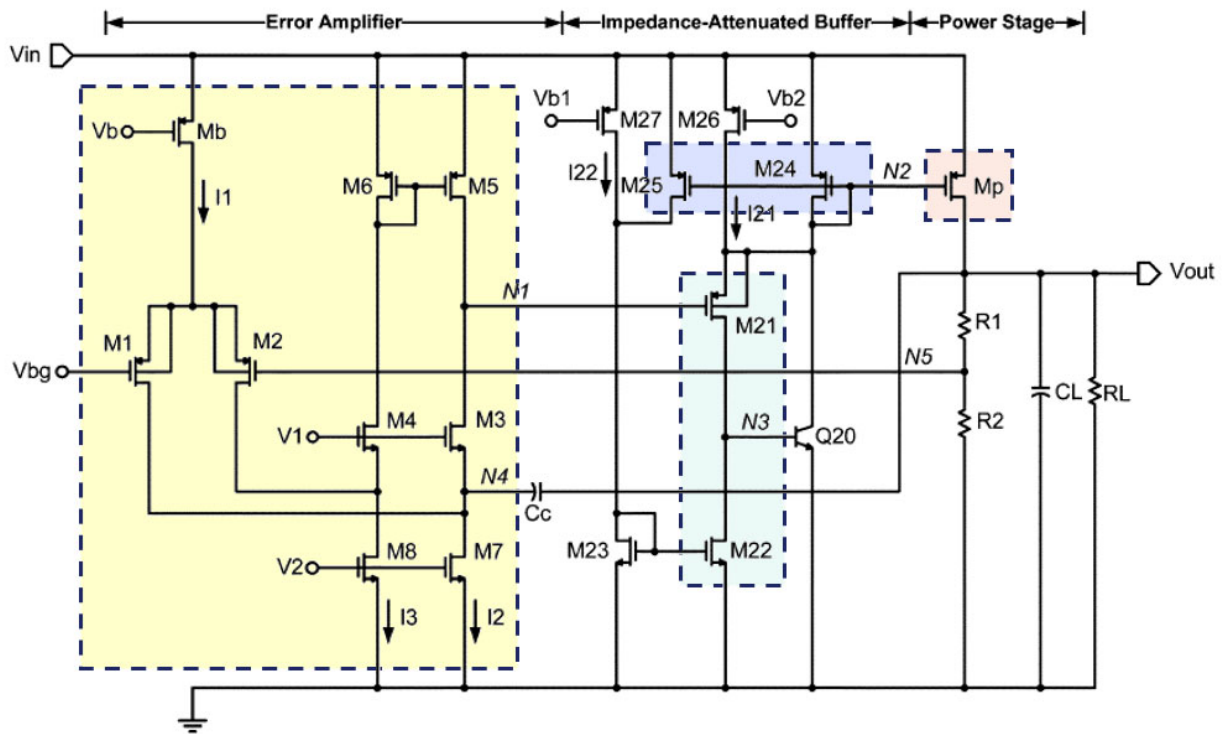


(*Id.*, Fig. 8 (annotated).) I note also that Al-Shyoukh cites various papers relating to operational amplifiers to explain its circuit. (*Id.*, 1741.) A POSITA would therefore have recognized this error amplifier to be an operational amplifier.

52. A POSITA would also have understood that the primary purpose of Al-Shyoukh's error amplifier is to amplify the error between the reference voltage V_{bg} and the feedback voltage at N_5 , and use the amplified error to correct the output of the LDO. This mechanism has been explained in paragraph 46 above. And for this to work, the error amplifier must have sufficient loop gain. As a POSITA would have recognized, one of the basic properties of op-amps is relatively high gain, and in a feedback circuit, high loop gain. Thus, op-amps were known to be a suitable and conventional choice for the design of an error amplifier in a voltage regulator. This aligns with the design of Al-Shyoukh's error amplifier.

[b] a gm enhanced current buffer driver;

53. I have explained above in my summary of Al-Shyoukh how its circuit includes a current feedback system that enhances the gm of transistor M_{21} , which is the core component of the buffer driver shown in green below:



(EX1004, Fig. 8 (annotated); *see also id.*, 1733-35, Figs. 3, 4.)

54. I note that the '074 patent does not actually seem to describe or disclose a “current buffer driver” in its description of the supposed invention. What the '074 patent calls a “current buffer” is something a POSITA would have recognized as a *voltage* buffer. According to the patent, its voltage regulator has a “low-impedance current buffer driver 204” centered at transistor 384, which “creates a low impedance environment using the current buffer (transistors 384 and 394, and resistor 372) to separate the poles seen on the big power output driver.” (EX1001, 3:57, 4:64-5:1.) But a low output impedance was conventionally understood to be a characteristic of voltage buffers, in contrast with current buffers, which have high output impedance.

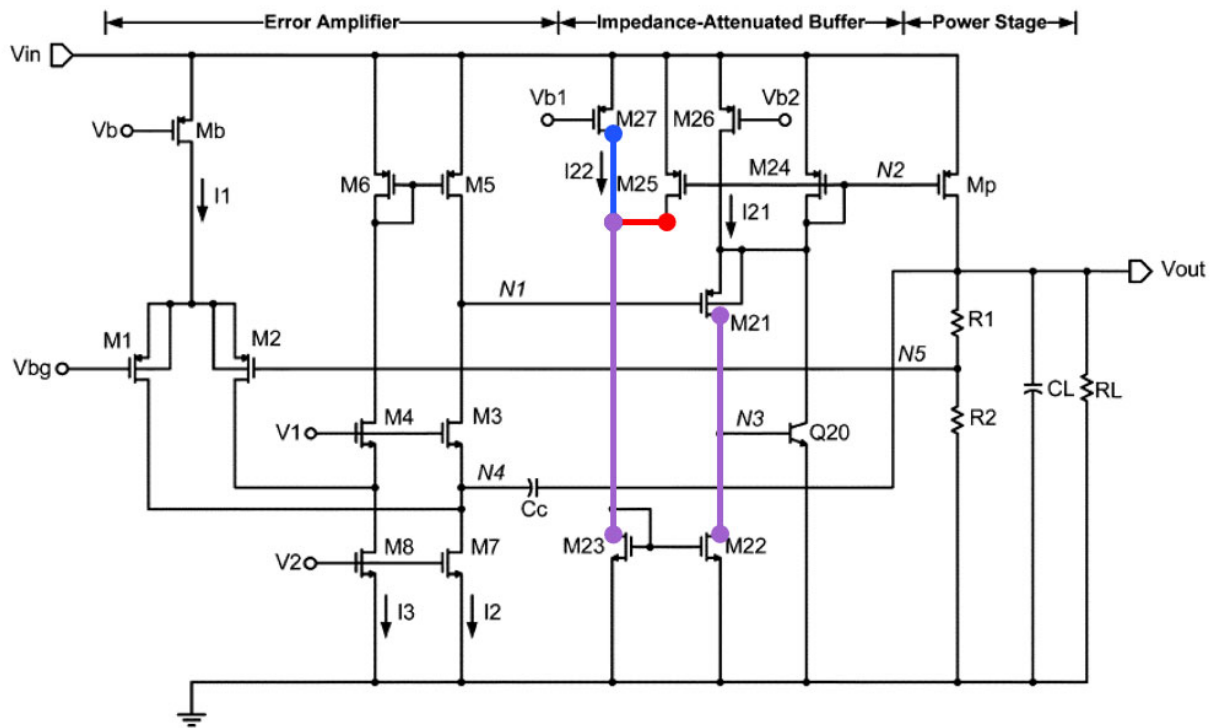
Furthermore, the patent describes transistor 384 as a “source follower.” (*Id.*, 4:36.)

A POSITA would have known that a voltage buffer was a common application for source followers, which have high input impedance but low output impedance.

55. Al-Shyoukh’s buffer has these same characteristics. Its output is a “low impedance node” with parasitic pole p_2 “located at a very high frequency under the full range of the load current,” away from dominant pole p_o . (EX1004, 1735.) Also, Al-Shyoukh’s buffer driver transistor M_{21} is, like the ’074 patent’s transistor 384, a “source-follower.” (*Id.*, 1734.) Thus, it is my view that regardless of what precisely is meant by “current buffer driver,” Al-Shyoukh discloses the same current buffer driver that the ’074 patent discloses.

[c] a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver;

56. As I have explained above in my summary of Al-Shyoukh, one of the ways that its circuit boosts the gm of the buffer driver transistor M_{21} is by increasing the current at transistor M_{22} (which pulls current from M_{21}), which is in turn done by increasing current at M_{23} , which mirrors to M_{22} . M_{23} receives a sum of two currents: a current I_{22} provided by transistor M_{27} , which receives at its gate a bias voltage V_{b1} , and a current provided by transistor M_{25} , which mirrors the current from transistor M_{24} and is thus a feedback current. This is shown below:



(EX1004, Fig. 8 (annotated).) Here, the I_{22} current generated by the bias voltage is in blue. A POSITA reading Al-Shyoukh would have understood that, although not shown, the voltage V_{b1} at the gate of M27 is provided by a biasing circuit. In addition, the figure above shows the feedback current from M25 in red, and the summed current flowing into M23, and mirrored to M22, in purple. (A basic principle in the analysis of circuits is that the sum of the input currents at a node must be equal to the sum of the output currents. This is known as Kirchhoff's Current Law.)

57. In my opinion, this discloses “a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver.” This is based on the fact that the '074 patent's own biasing circuit sets a “biasing ratio for

gm-boost” in exactly the same way. The patent describes a bias network “fixed by transistor 396,” such that the current from the bias network is “ratio’ed in transistors 368 and 370” with the feedback current. (EX1001, 5:15-24.) This is shown below, where Figure 3B of the patent has been annotated with colors corresponding to my description of Al-Shyoukh above:

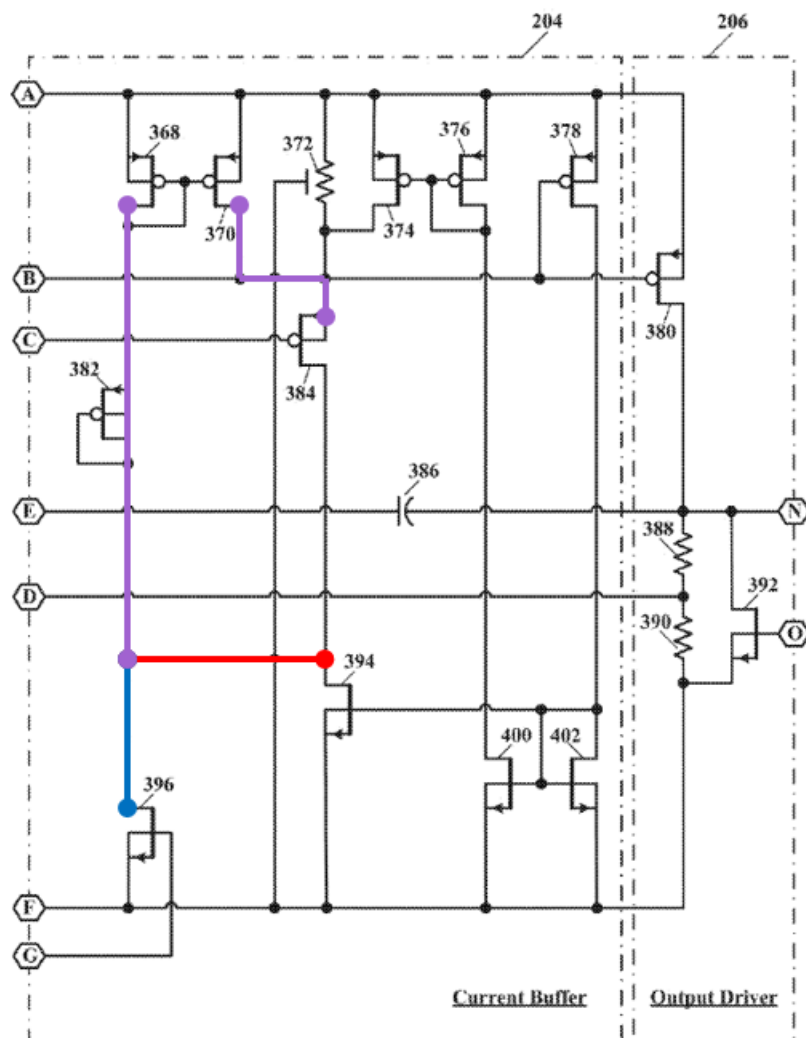


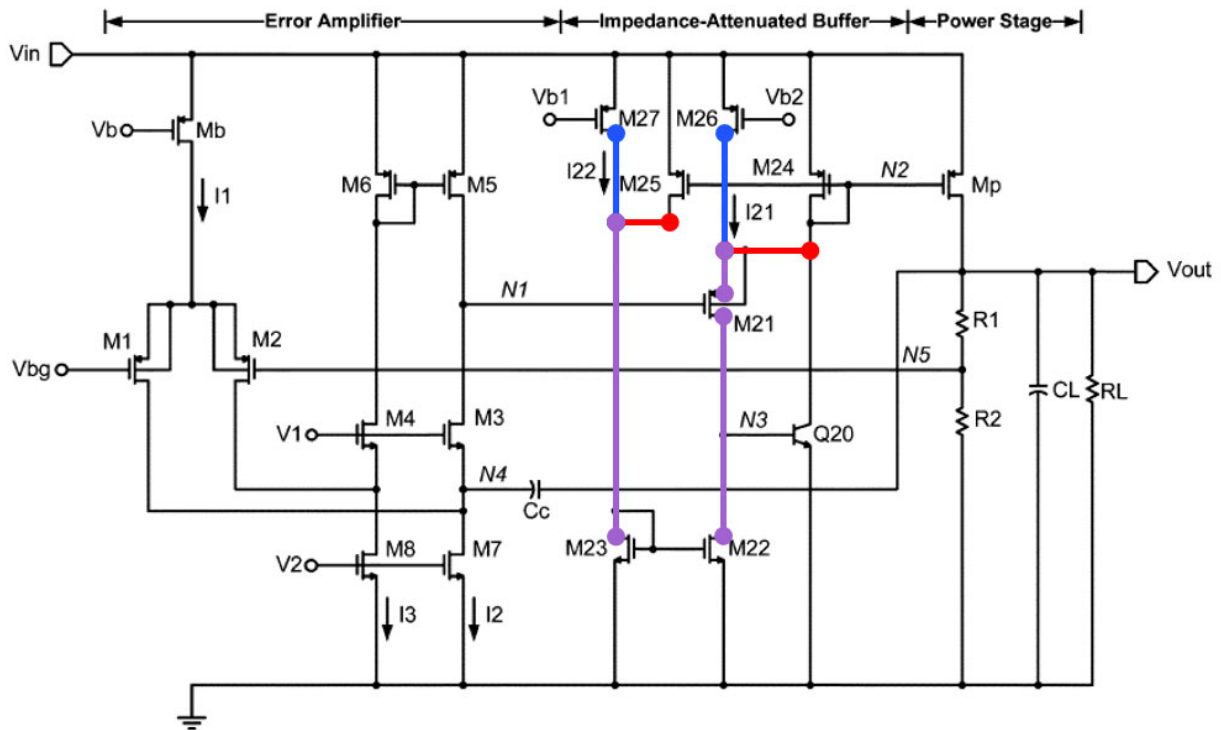
FIGURE 3B

(*Id.*, Fig. 3B (annotated).) Here, the current through transistor 368 (shown in purple) is the sum of the bias current fixed by transistor 396 (blue) and another current that flows to transistor 394 (red). The red current is a feedback current because transistor 394 is mirrored with transistor 402, which receives current from transistor 378, the transistor that senses changes at the output driver 380. (The '074 patent also defines the current feedback circuit to include 394. (*Id.*, 5:13-14.)) Thus, the purple current is a sum (by Kirchhoff's Current Law) of a bias current and a feedback current. This sum is "ratio'ed in transistors 368 and 370" to increase current in, and thus provide a "gm-boost" to, the buffer driver transistor 384. (*Id.*, 5:21-23.)

58. In the same way, the current mirror M_{22} and M_{23} in Al-Shyoukh "ratio" a current that is the sum of a bias current and a feedback current. And because M_{22} draws current from M_{21} , M_{21} receives a gm boost. (EX1004, 1734.)

59. I understand that in the District of Delaware litigation between Aptiv and Patent Owner, Patent Owner argues that "biasing ratio" should be understood to mean a ratio of current that the current buffer draws from DC relative to the current feedback circuit. If such a meaning were to apply, it is my opinion that Al-Shyoukh would still disclose "a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver." Al-Shyoukh's biasing circuit provides voltages V_{b1} at transistor M_{27} and V_{b2} at transistor M_{26} . (EX1004, Fig. 8.) V_{b1} and V_{b2} determine bias currents I_{22} and I_{21} . And as shown in below, I_{22} and I_{21}

(blue) add to feedback currents from M_{25} and M_{24} (red) to provide a gm-boost to the buffer driver at M_{21} :



(*Id.*, 1734, Fig. 8 (annotated).) A POSITA would have known that a circuit designer could set bias voltages V_{b1} and V_{b2} , and thus a ratio of current drawn from DC and current drawn from feedback.

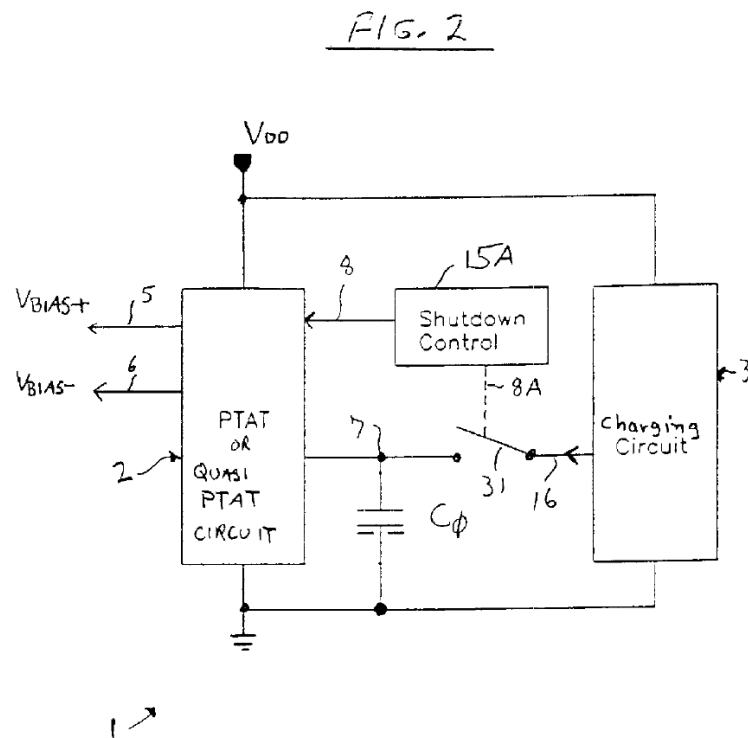
[d] an enable/disable function to enable/disable the biasing circuit for reducing standby current;

60. Al-Shyoukh's LDO receives various inputs from biasing circuitry, such as V_{b1} and V_{b2} . (*Id.*, Fig. 8.) Biasing circuits were a basic and ubiquitous electronics component, because electronic devices typically require constant voltage or current inputs at various locations. Assuming familiarity with biasing circuits, Al-Shyoukh

does not describe the design of its own biasing circuit in detail. But a POSITA would have recognized that it could be implemented using any of a variety of conventional and well-understood methods.

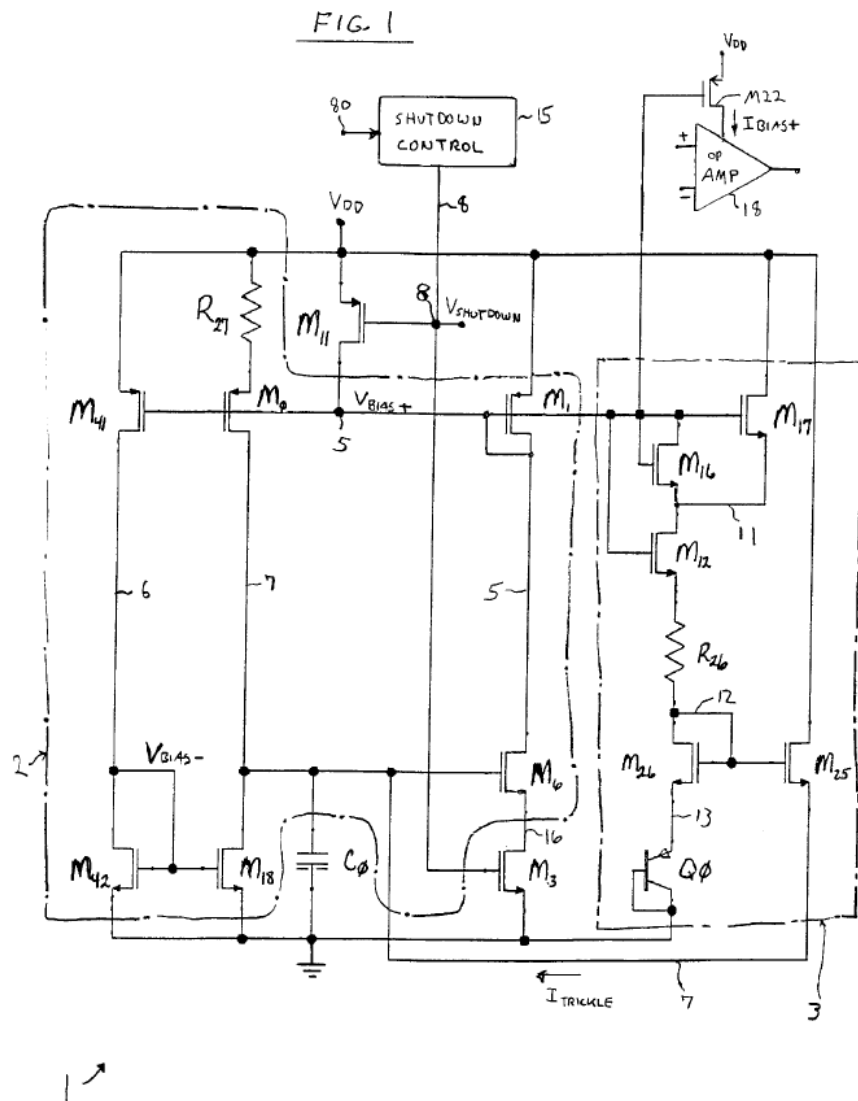
61. Ivanov, for example, describes a biasing circuit architecture that would have been suitable for Al-Shyoukh. Ivanov presents “a quick turn-on disable/enable bias control circuit” for use in “integrated circuit applications.” (EX1005, 1:6-9.) According to Ivanov, “[i]n certain types of electrical circuits,” there are “nodes that need to be quickly charged to a predetermined voltage level.” (*Id.*, 1:12-18.) At the same time, “[t]o minimize power consumption, portions of the circuitry are designed to be disabled so as to be in a quiescent, low-power state until fully functional circuit operation is needed.” (*Id.*) Ivanov thus proposes a “fast disable/enable bias control circuit that is very suitable for fast disabling and subsequent fast enabling of the bias circuitry” for “applications such as voltage regulators.” (*Id.*, 6:47-52.)

62. Ivanov’s bias control mechanism is shown in Figure 2:



(*Id.*, Fig. 2.) The bias core circuit, represented as block 2, is “coupled between V_{DD} and ground.” (*Id.*, 4:26-29.) It produces two bias voltages, V_{BIAS+} on conductor 5 and V_{BIAS-} on conductor 6, and is coupled to shutdown control circuit 15A, which controls it through conductor 8. (*Id.*, 4:30-33.)

63. Corresponding to the block diagram of Ivanov’s Figure 2 is the detailed, exemplary implementation of the biasing circuit shown in Figure 1:



(*Id.*, Fig. 1.) As shown here, Ivanov’s circuit includes a “P-channel bias core disable transistor M11,” whose drain is connected to the bias core circuit 2 at node 5, whose source is connected to V_{DD} , and whose gate receives via node 8 “an external signal $V_{SHUTDOWN}$ produced by an external shutdown control circuit 15 in response to an external control signal applied to an external input 80 thereof.” (*Id.*, 3:43-49.)

64. Ivanov's bias circuit creates a voltage $V_{\text{BIAS+}}$, "produced on conductor 5 by bias core circuit 2 when it is active," where conductor 5 is connected to the gate of transistor M22, which "has its source connected to V_{DD} and its drain connected to supply a bias current $I_{\text{BIAS+}}$ to CMOS operational amplifier 18." (*Id.*, 3:54-63.) This $I_{\text{BIAS+}}$ current is therefore the output bias current of this bias circuit.

65. If the shutdown control circuit wants to disable the bias current "so as to dissipate a minimum amount of power," it "produces a low value of V_{SHUTDOWN} ," or disable signal. (*Id.*, 5:19-24.) This "turns on transistor M11," which "pulls [the voltage of] conductor 5 close to V_{DD} ." (*Id.*, 5:24-25.) This brings the source-gate voltage of transistor M22 close to zero, shutting it off and disabling $I_{\text{BIAS+}}$.

66. In the other direction, the shutdown control circuit can produce a high value of V_{SHUTDOWN} , or an enable signal, which "turns transistor M11 off and turns transistor M3 on." (*Id.*, 6:6-11.) Then the "voltage maintained across capacitor C0, i.e., the voltage on conductor 7, then is such that the current through transistors M3, M6 and M1 very rapidly pulls the voltage on conductor 5 down to a level which turns transistors M0 and M41 on and thereby re-establishes the feedback loops" of the circuit. (*Id.*, 6:11-16.) This produces "the desired value of $V_{\text{BIAS+}}$ on conductor 5, and therefore also on the gate of the current mirror transistor M22," turning M22 on so that it outputs $I_{\text{BIAS+}}$. (*Id.*, 6:16-22.)

67. In my opinion, a POSITA would have recognized Ivanov's bias circuit model, including its disable/enable control mechanism, to be useful and suitable for Al-Shyoukh's LDO. One of Al-Shyoukh's primary overall objectives is to improve power efficiency and reduce quiescent current. (EX1004, 1732.) Ivanov describes a convenient and ready-to-use way to shut off circuitry that would otherwise draw power even when not in use, explaining that this provides "a quiescent, low-power state until fully functional circuit operation is needed." (EX1005, 1:6-18.) Ivanov also states that "voltage regulators" are among the intended applications for its bias circuit. (*Id.*, 6:47-54.)

68. Implementing Ivanov's bias circuit with Al-Shyoukh's regulator would not have caused undue experimentation; a POSITA could simply have used Ivanov's circuit, with conventional modifications so that the circuit could provide each of the different bias voltages that Al-Shyoukh's circuit requires. For example, a POSITA would have recognized that transistor M22 in Ivanov (which receives V_{BIAS+} at its gate and outputs a bias current I_{BIAS+}) could correspond to Al-Shyoukh's transistor M₂₇ (which likewise receives V_{b1} at its gate and outputs a bias current I_{22}). Further, Ivanov teaches that in addition to M22, "other similar current mirror transistors, not shown" in its figures could also receive V_{BIAS+} , to generate as many bias currents as needed. (*Id.*, 6:19-20.) Thus, a POSITA could have easily used Ivanov's circuit to provide each of the voltage inputs required in Al-Shyoukh. A POSITA could also

easily have chosen the different components in Ivanov's circuit, including resistors, capacitors, and transistors, to generate the desired bias voltages or currents required for Al-Shyoukh. These would all have been well within the skill and knowledge of a POSITA.

69. For these reasons, Al-Shyoukh's LDO coupled to Ivanov's bias circuit would have had "an enable/disable function to enable/disable the biasing circuit for reducing standby current." I note that the '074 patent describes this "enable/disable function" only in one place—column 4, lines 52-54—where it states that "Node M" of Figure 3 "is the enable signal coming to the regulator circuit so that the module can be turned off when disabled." (EX1001, 4:52-54.) I have reproduced Figure 3 below, side-by-side with Ivanov's bias circuit:

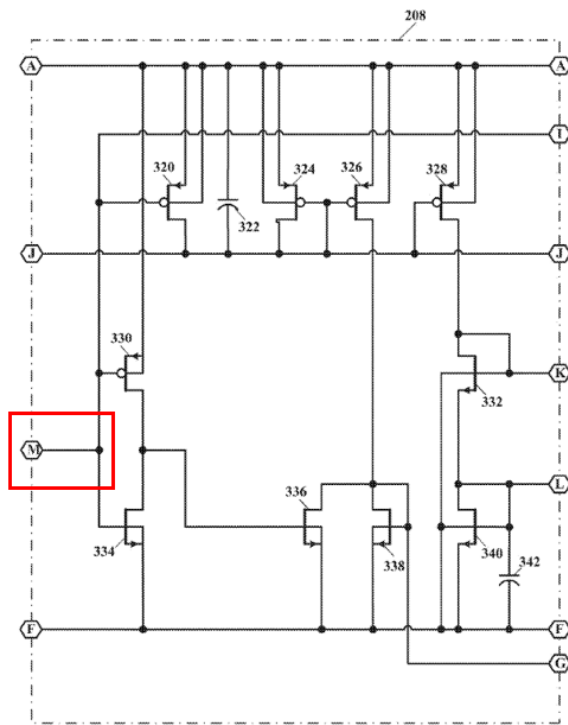


FIGURE 3

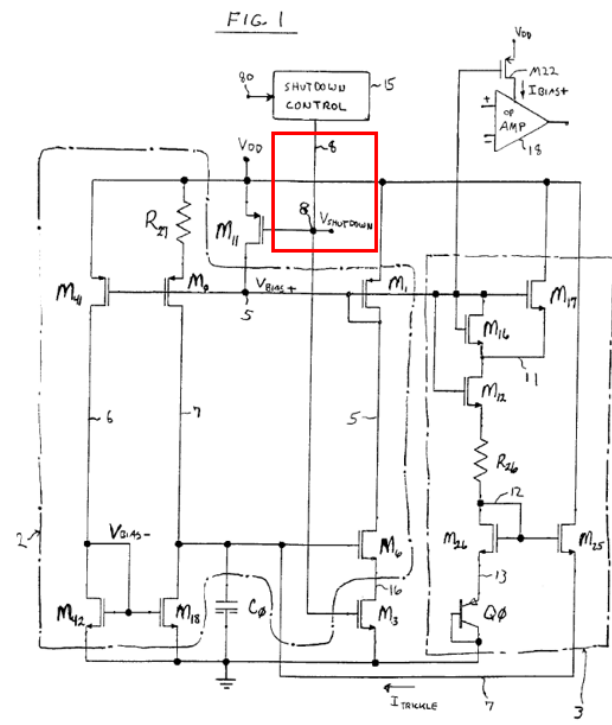


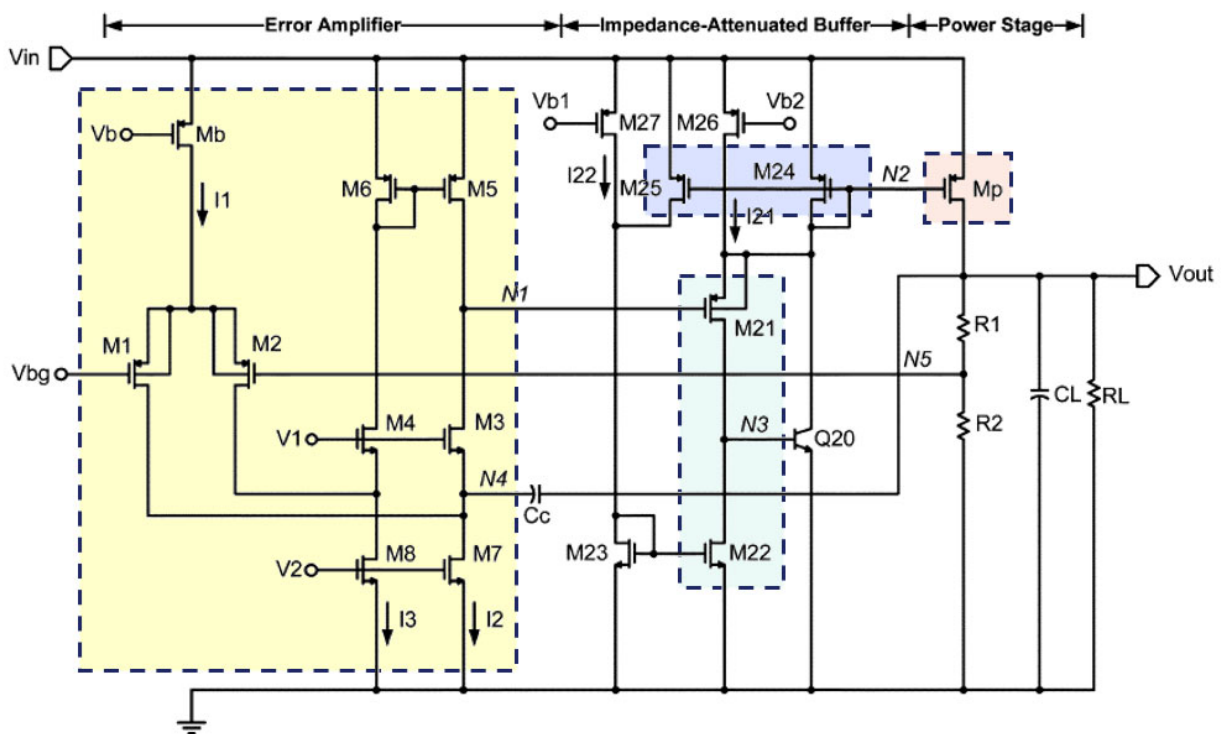
FIG. 1

(EX1001, Fig. 3 (annotated); EX1005, Fig. 1 (annotated).) As indicated by the red boxes, Ivanov's node 8 corresponds to node M, and the V_{SHUTDOWN} signal provided by its shutdown control circuit corresponds to the patent's "enable signal."

70. I note further that the concept of an enable/disable for biasing circuitry was known widely beyond Ivanov. Power efficiency was a basic concern in analog circuit design, and it was well known that a way to save energy was to disable parts of a circuit that were not in use, biasing circuitry being a frequent candidate. Thus, I believe that it would have been obvious to a POSITA, independently of Ivanov, to implement Al-Shyoukh's biasing circuitry with an enable/disable function to reduce the standby current.

[e] an output power driver, wherein the current buffer driver is coupled between the operational amplifier and the output power driver;

71. My summary of Al-Shyoukh's LDO above explains that the transistor M_p serves as the voltage regulator's pass device, or output power driver. (EX1004, 1732, Fig. 8.) And as shown below, Al-Shyoukh's buffer driver (green) is coupled between the operational amplifier (yellow) and the output power driver (red):



(EX1004, Fig. 8 (annotated).)

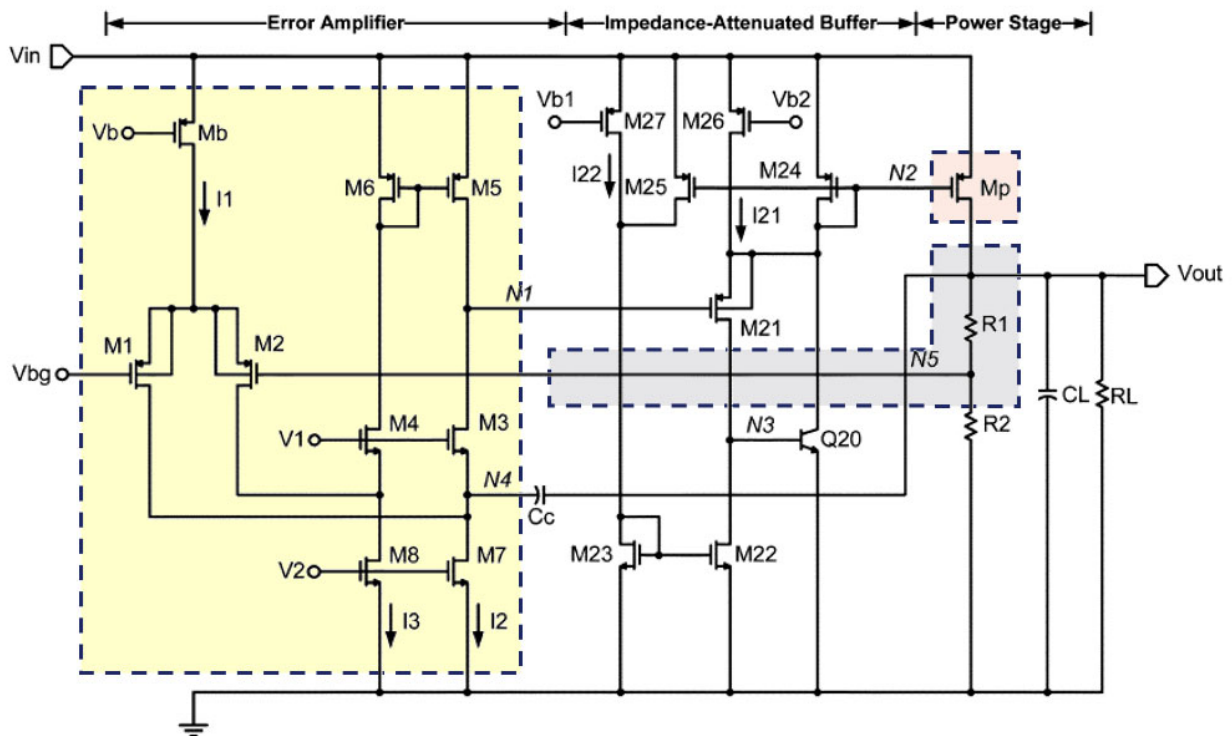
[f] a current feedback circuit coupled between the output power driver and the current buffer driver; and

72. Referring to the figure above (and as discussed in my earlier summary of Al-Shyoukh), Al-Shyoukh's LDO has a current feedback circuit (shown in blue)

that is coupled between its output power driver (red) and the buffer driver (green).
(EX1004, 1734, Fig. 8.)

[g] a feedback loop coupled between the output power driver and the operational amplifier.

73. Al-Shyoukh's output power driver (or pass device) M_p feeds back to a differential input of the operational amplifier through node N_5 . This pathway, which includes resistor R_1 , is highlighted in gray below (with the operational amplifier in yellow and the output power driver in red).



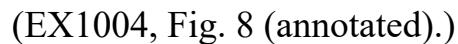
(EX1004, Fig. 8 (annotated).)

Claim 2 The voltage regulator according to claim 1, further comprising a gm-boost circuit coupled to the current buffer driver.

74. In my opinion, Al-Shyoukh's LDO includes a gm-boost circuit because its current feedback circuit boosts gm of the buffer driver. (EX1004, 1734, Fig. 8.)

75. The '074 patent does not define "gm-boost circuit," but it does describe an embodiment where the "gm-boost stage" comprises "transistors 368, 370, 374, 376, 378, 382, 396, 394, 400, 402, 384 and resistor 372," in reference to Figure 3B. (EX1001, 5:8-10.) This includes each component of the "current driver," which the patent explains comprises "transistors 370, 384, and 394, and resistor 372" (*id.*, 5:10-12), as well as the current feedback circuit, which comprises "transistors 374, 376, 378, 400, 402, and 394" (*id.*, 5:12-14). Based on this example—the sole example in the patent's specification—I understand that the "gm-boost circuit" may include the current feedback circuit and the buffer driver.

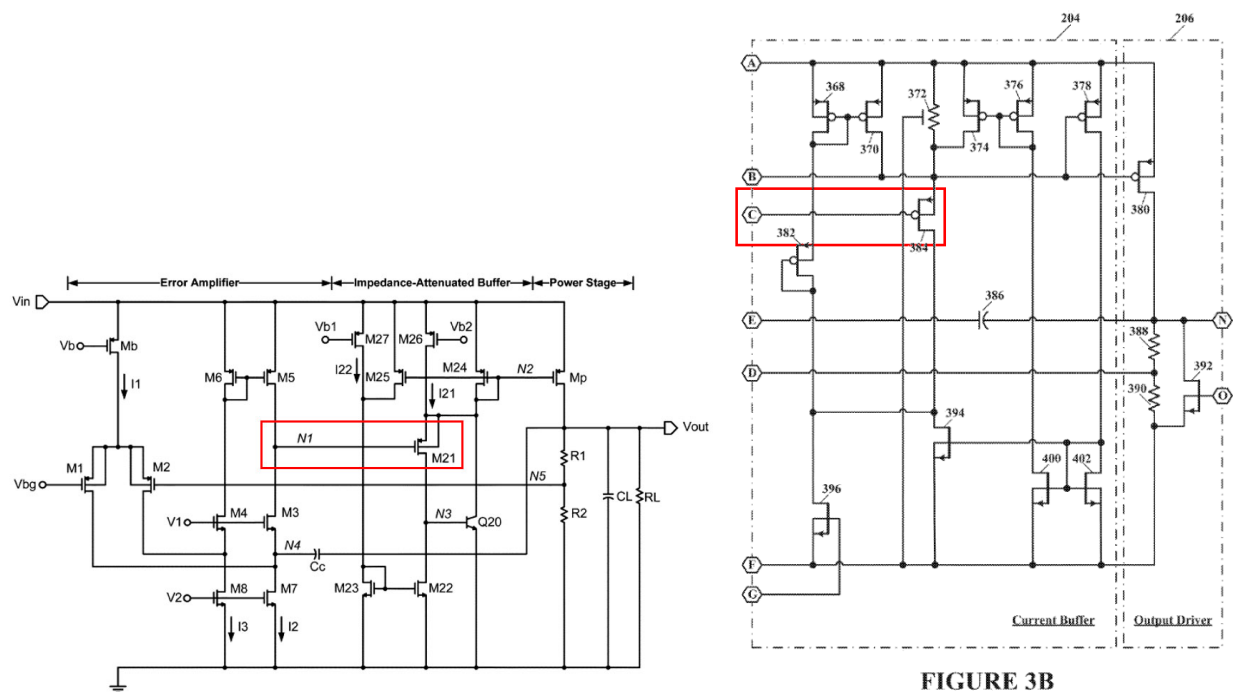
76. Thus, Al-Shyoukh's LDO has a gm-boost circuit (highlighted in purple below) that includes its buffer driver (green), its current feedback circuit (blue), and the circuitry that couples to the biasing circuit (*e.g.*, transistors M₂₆ and M₂₇):



77. I understand that in the District of Delaware litigation between Aptiv and Patent Owner, Patent Owner argues that claim 3 refers to a gm-boost circuit that, by providing current feedback, and thereby reducing the current that the input must supply, increases the input impedance at the point where the operational amplifier connects to the buffer driver. If such a meaning were to apply, it is my opinion that a POSITA would have understood Al-Shyoukh's LDO to be a voltage regulator in

which “the gm-boost circuit increases the current buffer driver input impedance,” as explained below.

78. In Al-Shyoukh, N_1 is the point where the operational amplifier connects to the buffer driver. This corresponds to node C in the '074 patent, which is where the operational amplifier provides an output voltage to the gate of driver transistor 384, just as Al-Shyoukh's error amplifier provides a voltage to the gate of M_{21} :



(*Id.*, Fig. 8 (annotated); EX1001, Fig. 3B (annotated).) And as explained above in my summary of Al-Shyoukh and in my analysis for claims 1 and 2, Al-Shyoukh's gm-boost circuit provides its buffer driver with current feedback, just as the '074 patent's gm-boost circuit does. A POSITA would thus have found the two circuits to be substantially identical, such that to the extent the '074 patent's gm-boost circuit

provides current feedback, reduces current needed from the input, and thus increases input impedance at the point where the operational amplifier connects to the buffer driver, so, too, does Al-Shyoukh's gm-boost circuit.

79. I have also been asked to consider an alternative interpretation of claim 3, under which the phrase "the gm-boost circuit increases the current buffer driver input impedance" means that because of the current feedback provided by the gm-boost circuit, a transistor with relatively higher input impedance may be chosen for the buffer driver. It is my opinion that, under this meaning, Al-Shyoukh has such a gm-boost circuit, as explained below.

80. Al-Shyoukh explains that a goal of its feedback circuit is to reduce the output resistance r_{ob} of the buffer driver to stabilize the circuit, because the parasitic pole associated with the buffer driver is inversely proportional to r_{ob} and reducing r_{ob} would push the pole higher. (EX1004, 1733-34.) Al-Shyoukh reduces r_{ob} using transistor M_{24} , as shown below, where g_{m21} and g_{m24} are the transconductances of transistors M_{21} and M_{24} , respectively:

$$r_{ob} = \frac{1}{g_{m21}(1 + \beta) + g_{m24}}$$

(*Id.*, 1734.) As Al-Shyoukh explains, this reduces the quiescent current needed at M_{21} , which means that the size of M_{21} can be chosen to be smaller, which in turn means a lower input capacitance of the buffer. (*Id.*) A POSITA would have known

that this is because the input capacitance of the buffer is essentially the parasitic capacitance associated with transistor M₂₁, which increases with the transistor size. In addition, a POSITA would have known that the impedance (Z_c) of a capacitor (C) can be modeled as shown below, where ω is the frequency of interest:

$$Z_c = 1/j\omega C$$

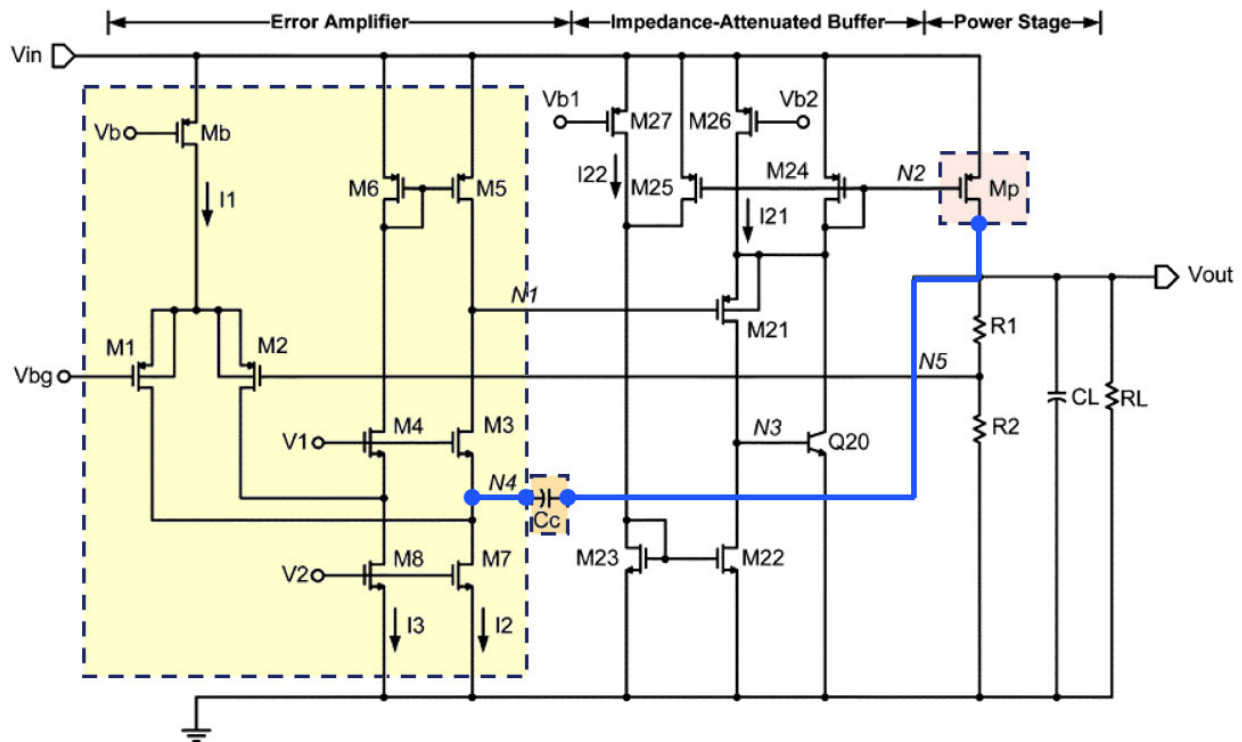
Thus, for a given frequency, the impedance of a capacitor is inversely proportional to its capacitance value. This means the current feedback provided by Al-Shyoukh's gm-boost circuit allows the LDO to use a transistor with relatively higher input impedance as its buffer driver due to its reduced input capacitance.

Claim 4 The voltage regulator according to claim 2, wherein the gm-boost circuit enables the current buffer driver to have a large gm value.

81. I understand that in the District of Delaware litigation between Aptiv and Patent Owner, Patent Owner argues that the term “enables the current buffer driver to have a large gm value” means “increases the gm value of the current buffer driver.” If such a meaning were to apply, it is my opinion that Al-Shyoukh discloses a voltage regulator “wherein the gm-boost circuit enables the current buffer driver to have a large gm value.” As explained in my analysis above for claims 1 and 2, Al-Shyoukh's gm-boost circuit increases the current at the buffer driver transistor M₂₁, thus increasing its gm value. (*Id.*, 1734.)

Claim 5 The voltage regulator according to claim 1, further comprising a compensation capacitor coupled between the output power driver and a cascode node of the operational amplifier.

82. Al-Shyoukh's LDO includes a capacitor C_c (shown in orange below) coupled to the output power driver M_p (red) and the operational amplifier (yellow):



(EX1004, Fig. 8 (annotated).) The electrical connections linking the capacitor to the output power driver and the operational amplifier are shown in blue.

83. C_c is a compensation capacitor. As Al-Shyoukh explains, C_c provides “current-buffer (or cascode-Miller) frequency compensation” to split “poles p_1 at N_1

and p_o at the LDO output in order to achieve stability in the full range of the load current.” (*Id.*, 1735.)

84. In addition, N_4 , where C_c meets the operational amplifier, is a cascode node. A cascode node is a node that couples to a cascode device. Al-Shyoukh’s operational amplifier has a “single-stage folded-cascode structure,” where M_1 is part of the folded device and M_3 is part of the cascode device. (*Id.*, 1735, Fig. 8.) This makes N_4 , at the source terminal of M_3 , a cascode node.

85. I note that the ’074 patent shows exactly the same topology, as marked by corresponding annotations (yellow for the amplifier, orange for the compensation capacitor, red for the output power driver, and blue for the connections) below:

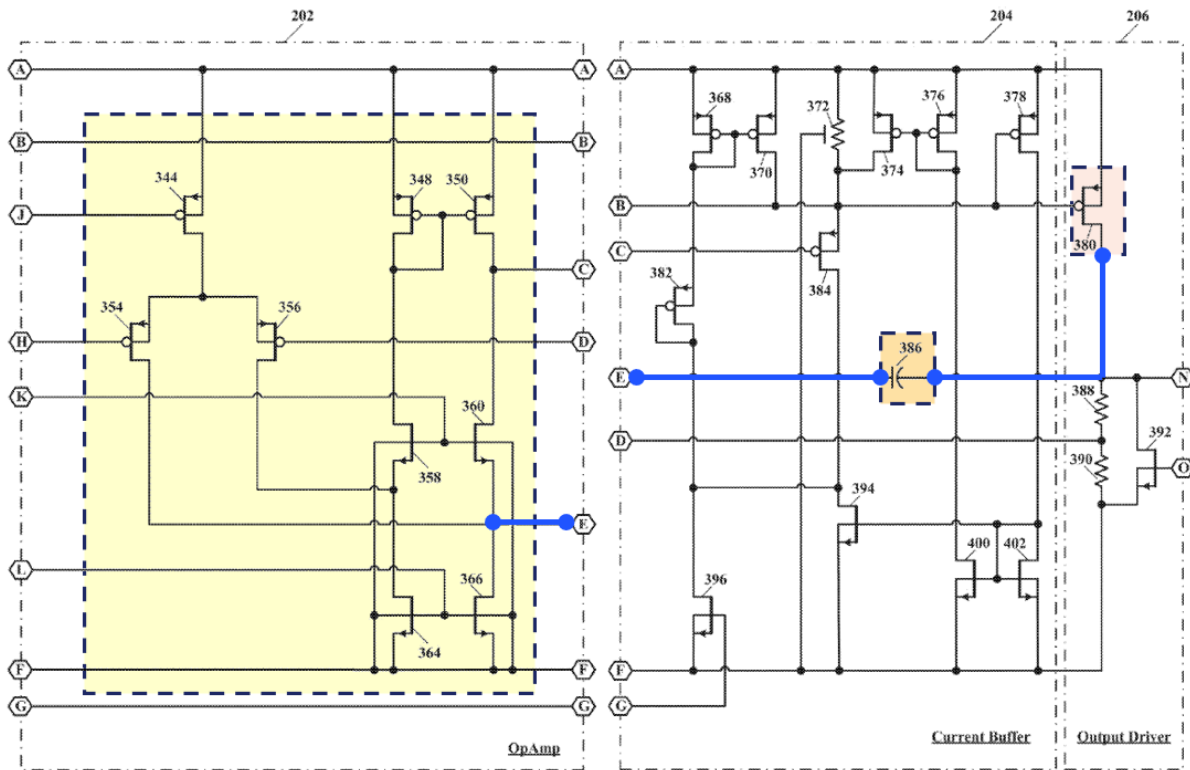


FIGURE 3A

FIGURE 3B

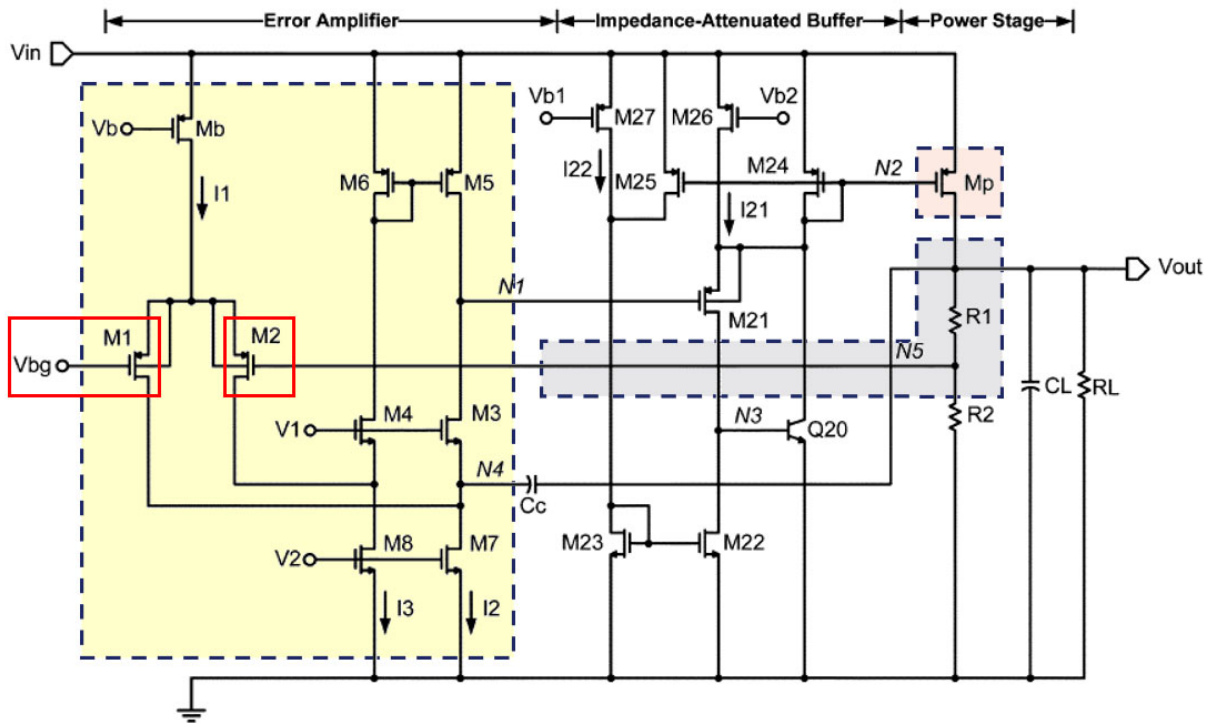
(EX1001, Figs. 3A, 3B (annotated).) This shows that compensation capacitor 386 couples at node E to transistors 354 and 360 of the amplifier the same way C_c in Al-Shyoukh couples at N_4 to transistors M_1 and M_3 .

Claim 6 The voltage regulator according to claim 1, wherein the voltage regulator is a low drop out (LDO) voltage regulator.

86. Al-Shyoukh's voltage regulator is "a low-dropout regulator (LDO)." (EX1004, 1732.).

Claim 7 The voltage regulator according to claim 1, wherein the operational amplifier has a first input adapted for coupling to a voltage reference, and a second input coupled to the feedback loop.

87. Al-Shyoukh's operational amplifier (highlighted in yellow below) has a first input adapted for coupling to voltage reference V_{bg} and a second input coupled to the feedback loop (gray):

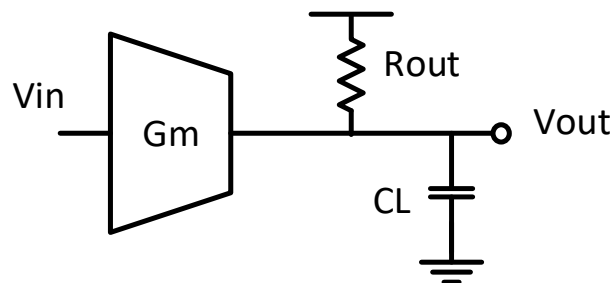


(EX1004, Fig. 8 (annotated).) I also refer to my summary of Al-Shyoukh and my opinions regarding limitation 1[g] above.

Claim 8 The voltage regulator according to claim 1, wherein the operational amplifier is a low gain and high bandwidth amplifier.

88. I understand that in the District of Delaware litigation between Aptiv and Patent Owner, Patent Owner argues “a low gain and high bandwidth amplifier” is one “optimized for high bandwidth with a commensurate reduction of gain.” If such a meaning were to apply, it is my opinion that it would have been obvious to a POSITA to implement Al-Shyoukh with such an amplifier, as explained below.

89. It was well-understood that gain and bandwidth are characteristics that trade off with each other in an operational amplifier. Below is a basic single-stage operational amplifier model that consists of a transconductance input stage and an output load, where V_{in} is the input voltage of the operational amplifier, G_m is the transconductance input stage that converts input voltage to an output current, R_{out} is the output resistance of the operational amplifier, CL is the output/load capacitance of the operational amplifier, and V_{out} is output voltage of the operational amplifier:



The gain of this operational amplifier is equal to the product of G_m and R_{out} , while the bandwidth is equal to the reciprocal of the product of R_{out} and CL . Thus, an

operational amplifier with high R_{out} would have high gain and low bandwidth, and one with low R_{out} would have the opposite—low gain and high bandwidth.

90. A POSITA would have known that determining the tradeoff between gain and bandwidth (*e.g.*, through selection of R_{out}) was a basic step in designing and implementing an operational amplifier, with some of the many conventional, readily available designs having lower gain and higher bandwidth than others. A POSITA would therefore have recognized that choosing an op-amp that is “optimized for high bandwidth with a commensurate reduction of gain” for Al-Shyoukh’s error amplifier would have been a simple matter of design choice.

91. A POSITA would also have been generally aware of the benefits of an operational amplifier with high bandwidth (and commensurately low gain), as this was acknowledged throughout the art. For example, a 2008 Master’s Thesis written by Miranda J. Ha, called “A Low-Power, High-Bandwidth LDO Voltage Regulator with No External Capacitor,” explains that bandwidth is an “important specification in voltage regulator design,” and that “[t]he higher the bandwidth of a regulator, the more quickly it can react to changes in input and power supply and keep the output voltage constant.” (EX1007, 8.) A POSITA would have understood this principle to apply to Al-Shyoukh, which also presents an LDO designed to respond quickly to changes in load. (EX1004, 1734-35.)

92. As another example, a paper by Ye, *et al.*, published in January 2013 by *IEEE Transactions on Circuits and Systems* states that a relatively low-gain op-amp with high gain-bandwidth product can improve power efficiency for a high bandwidth closed-loop circuit. (EX1008, 96-97.) A closed-loop circuit is a type of circuit configuration with a feedback loop. Al-Shyoukh's LDO is an example of a closed-loop circuit in which power efficiency is a chief concern. (EX1004, 1732.)

93. Thus, not only would using a low-gain, high-bandwidth amplifier in Al-Shyoukh have been obvious as a matter of design choice, but a POSITA would also have found motivation to do so based on the known advantages of high bandwidth.

94. I further understand that in the District of Delaware litigation between Aptiv and Patent Owner, Patent Owner has argued that a folded cascode operational amplifier with a single stage of gain (comprising a differential input and a cascode load) is "a low gain and high bandwidth amplifier" within the meaning of claim 8. In that case, Al-Shyoukh's amplifier is "a low gain and high bandwidth" amplifier because it has a "single-stage folded-cascode structure." (*Id.*, 1735.)

Claim 9 The voltage regulator according to claim 8, wherein the low gain and high bandwidth amplifier is a folded-cascode amplifier.

95. As I have just discussed for claim 8, Al-Shyoukh's error amplifier has "a single-stage folded-cascode structure." (*Id.*, 1735.) In fact, it has the same single-

stage folded cascode structure as the amplifier in the '074 patent. This is clear from the side-by-side comparison below:

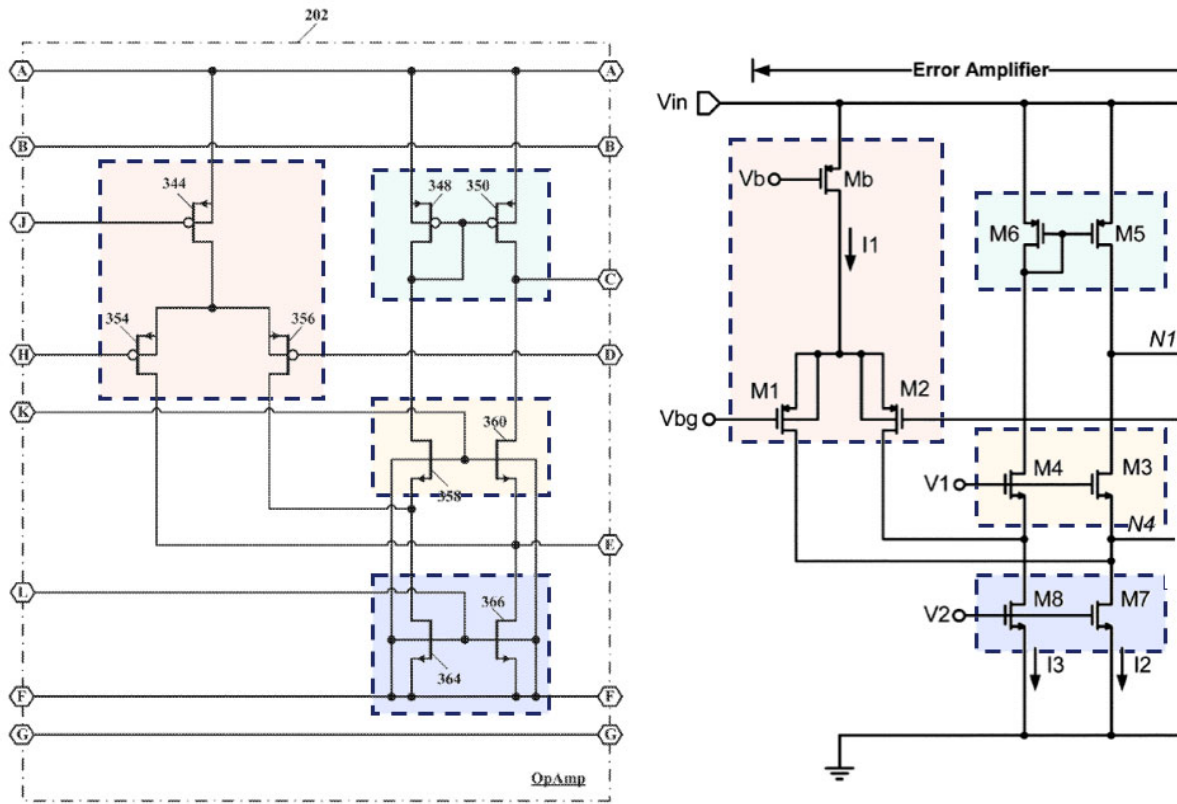


FIGURE 3A

(EX1001, Fig. 3A (annotated); EX1004, Fig. 8 (excerpted and annotated).) As this comparison shows, the two amplifiers have the same folded component (shown in red), the same active load component (green), the same current sink component (blue) and the same cascode component (yellow). I note that nodes J, H, K, and L are all biasing inputs provided by the biasing circuit, and thus correspond to the bias voltages V_b , V_{bg} , V_1 , and V_2 of Al-Shyoukh, respectively. (EX1001, Fig. 3; EX1004, Fig. 8.)

Claim 10 The voltage regulator according to claim 9, wherein the operational amplifier comprises diode connected PMOS transistors for lowering an output impedance of the folded-cascode amplifier.

96. Al-Shyoukh states that its “single-stage folded-cascode error amplifier” uses “a simple diode-connected active load using transistors M₅ and M₆,” resulting in “a smaller output resistance of the error amplifier r_{o1} as compared to a cascode load.” (EX1004, 1738.) This is shown in the above figure. M₆ and its mirror pair, M₅, correspond directly to the ’074 patent’s diode-connected PMOS transistor 348 and its mirror pair 350.

Claim 11 The voltage regulator according to claim 1, wherein the current buffer driver is an operational transconductance amplifier (OTA).

97. In my opinion, a POSITA would have found it obvious to modify Al-Shyoukh to use an OTA as its buffer driver, as taught by Stanescu.

98. Like Al-Shyoukh, Stanescu discloses an LDO. According to Stanescu, some prior art LDOs (as of Stanescu’s priority date in 2001) implemented the buffer as a “foldback cascode operational amplifier with NPN input transistors and an NPN common-collector output stage.” (EX1006, 2:12-14.) But, Stanescu points out, this could be expensive and suffer from “limited closed-loop bandwidth” as well as a “non-ideal transient response, even at a low ESR, due to a low slew-rate.” (*Id.*, 2:42-54.) Stanescu thus proposes using an OTA as the buffer, as illustrated below:

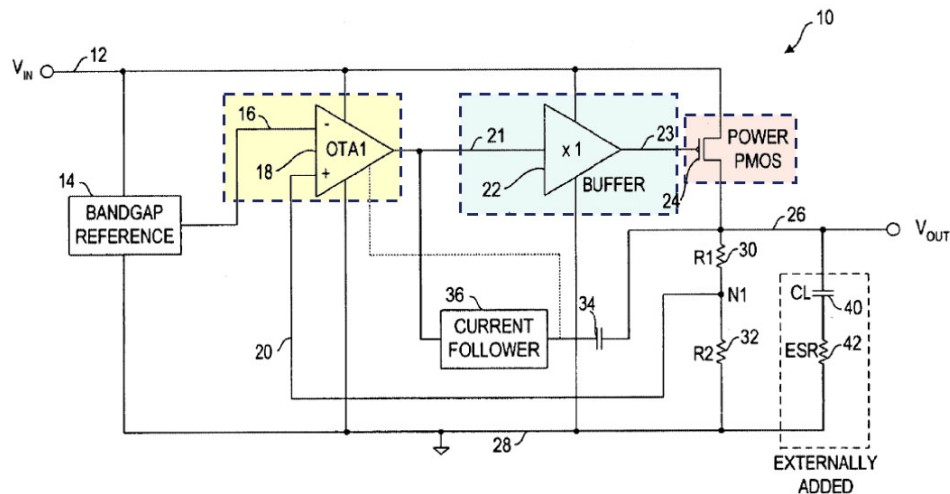


FIG. 1 (PRIOR ART)

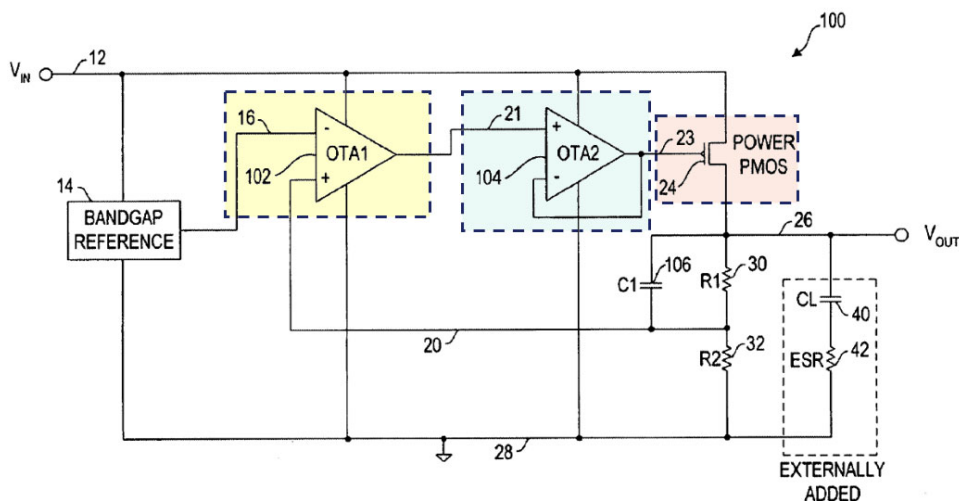


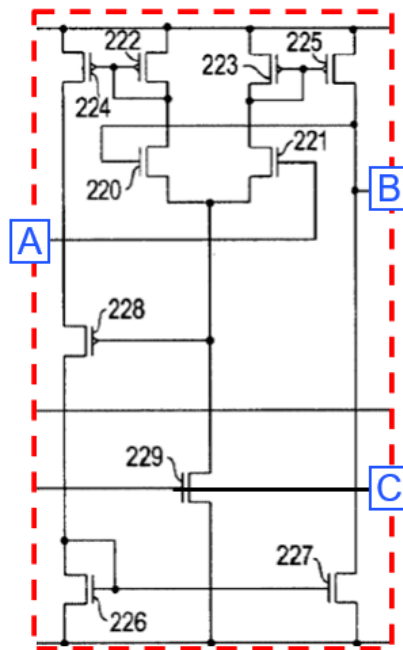
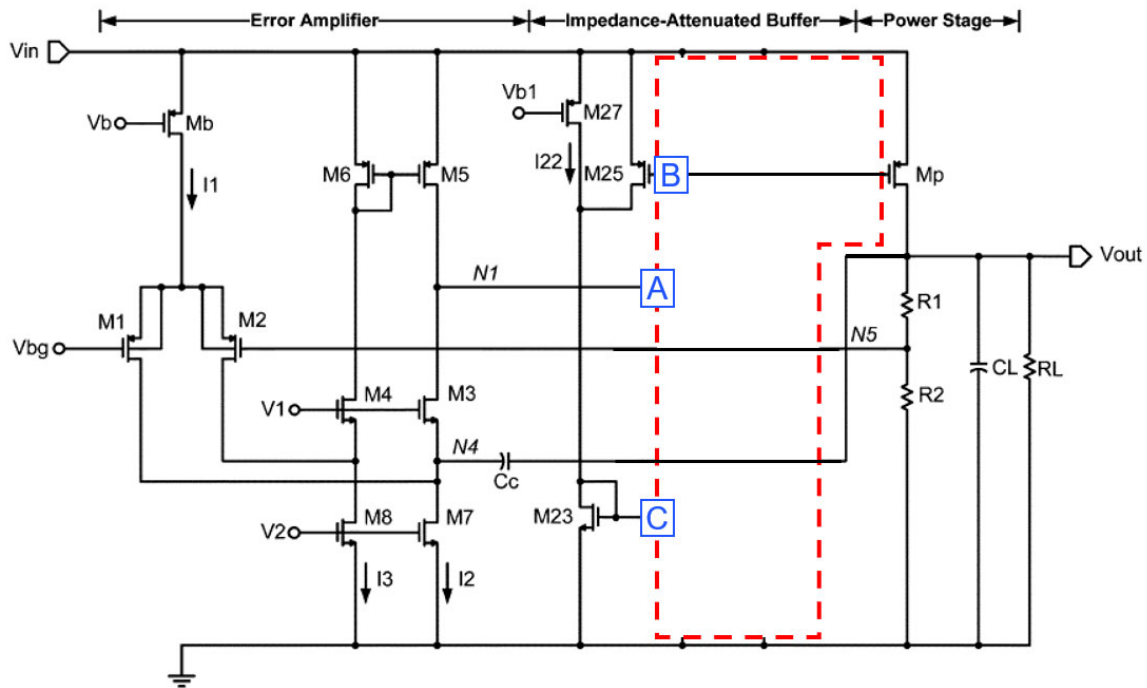
FIG. 2

(*Id.*, Figs. 1, 2 (annotated).) Figure 1 above shows the prior art LDO using an op-amp as the buffer. Figure 2 is Stanescu's LDO, with an OTA in its place. This OTA is a voltage follower with its output coupled back to its inverting input. (*Id.*, 3:2-4.) Thus, it has unity gain feedback. As a POSITA would have understood, unity gain feedback produces a low output impedance because it forms a series-shunt feedback

loop, lowering the OTA's output impedance by $(1+T)$, where T is the loop gain. A POSITA would also have understood that unity gain feedback is advantageous in an LDO because it less-than-unity gain would degrade the gain provided by the error amplifier, making the LDO's voltage feedback mechanism less effective in keeping its output constant at the desired voltage.

99. It would have been obvious to modify Al-Shyoukh to use an OTA as its buffer driver, following Stanescu. The two references are analogous art, directed to a low-dropout voltage regulator for use in portable battery-powered devices, and designed to save power by minimizing quiescent current. (EX1004, 1732; EX1006, 1:17-28, 7:64-8:3.) Thus, a POSITA would have considered Stanescu's teachings, including its identified advantages, to apply to Al-Shyoukh. Moreover, a POSITA would have understood that using Stanescu's voltage follower OTA would further Al-Shyoukh's goal of pushing the parasitic pole to higher frequencies by lowering the buffer's output impedance (EX1004, 1733-35), because the OTA has low output impedance. A POSITA would also have understood that an OTA with unity gain feedback would help keep the output voltage of Al-Shyoukh's LDO constant.

100. An exemplary combined circuit using Stanescu's OTA is shown below:



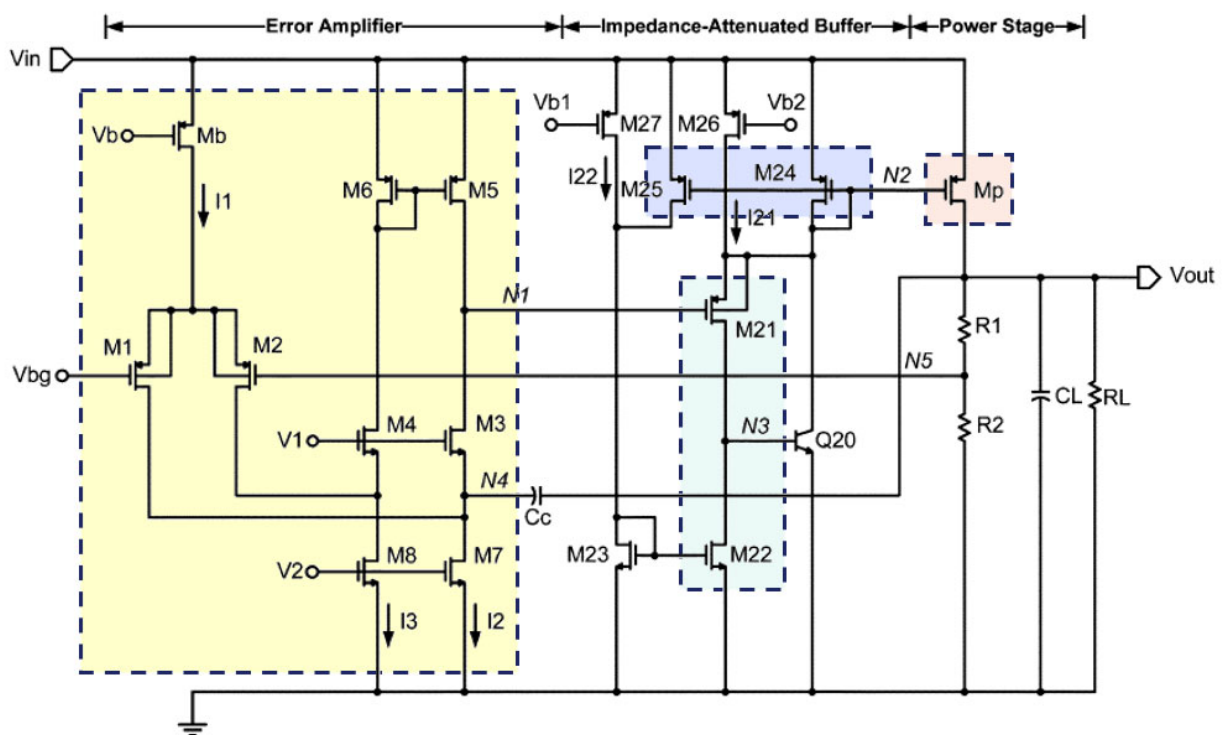
The first figure shows a modified version of Al-Shyoukh's circuit, where Stanescu's OTA would fit into the area marked by the red dotted line. The second figure shows

how Stanescu's OTA would couple to that area. Thus, transistor 221 would receive an input from node A, meeting Al-Shyoukh's N_1 . The output of Stanescu's OTA at node B would be in common with the gates of Al-Shyoukh's output driver transistor M_p and current feedback transistor M_{25} . Transistor 229 of the OTA would mirror to Al-Shyoukh's M_{23} across node C.

101. This combined circuit would preserve Al-Shyoukh's current feedback mechanism because transistor M_{25} (like M_{25} and M_{24} in the unmodified Al-Shyoukh circuit) would sense a current change at the output transistor through node B. For example, a voltage drop at B would cause M_{25} to output more current, thus increasing current at M_{23} , increasing the current mirrored to transistor 229 across node C. Because 229 pulls current from transistors 220 and 221, this boosts gm of the OTA/buffer. This circuit is one example of many variants that a POSTIA could have arrived at without undue experimentation when integrating Stanescu's unity-feedback OTA into Al-Shyoukh's LDO, given the small number of necessary connections, the well-known structure of Stanescu's OTA, and the clear purposes of each transistor.

Claim 12 The voltage regulator according to claim 1, wherein the current feedback circuit senses a current change at the output power driver.

102. As explained in my summary of Al-Shyoukh and my analysis of claim 1 above, Al-Shyoukh's current feedback circuit (highlighted in blue below) produces feedback by sensing a current change at the output power driver M_p :



(EX1004, Fig. 8 (annotated).) The gates of M_{24} and M_{25} are coupled to the gate of M_p via node N_2 . A change in current through M_p would cause the voltage at N_2 to change. For example, when a load is added from a no-load state, M_p would need to output more current. This would cause its source-gate voltage to increase, and thus

its gate voltage—the voltage at N_2 —to drop. The current feedback circuit senses that decrease along N_2 . (*Id.*, 1734-35.)

Claim 13 The voltage regulator according to claim 1, wherein the current feedback circuit provides transient enhancement for improved load regulation.

103. Al-Shyoukh describes, as its title states, a “Transient-Enhanced Low-Quiescent Low-Dropout Regulator with Buffer Impedance Attenuation.” What this means is that the current feedback circuit built into Al-Shyoukh’s buffer enhances the transient response of the LDO to changes in load. As Al-Shyoukh explains, the LDO minimizes “maximum output-voltage variation” during “load transients even if a small output capacitor is used.” (*Id.*, 1732.)

104. Al-Shyoukh’s current feedback circuit also “improve[s] slewing of the gate drive at N_2 during load transients.” (*Id.*, 1734.) For example, in the transition from no load to full load, the voltages at nodes N_1 and N_2 to decrease, causing (via M_{24} and M_{25}), the current of M_{21} to increase. (*Id.*) And when the LDO goes from full load to no load, the voltage at N_1 increases, causing transistor M_{24} to provide “extra transient current to charge C_p and increase the voltage at N_2 to follow the voltage change at N_1 with a faster slewing.” (*Id.*, 1734-35.)

105. Al-Shyoukh also discusses experimental results reflecting the improved transient response provided by its proposed current feedback circuit. (*Id.*, 1738-40.)

A POSITA would have understood all of this to demonstrate “transient enhancement for improved load regulation.”

Claim 14 The voltage regulator according to claim 1, wherein the current feedback circuit provides a feedback voltage from an output voltage node.

106. From my review of the '074 patent, the only time the phrase “feedback voltage” appears (excluding the claims and the part of the “Summary” section that echoes the claim language) is at column 5, lines 29-34, which state: “This feedback network 212 provides feedback voltage to one differential input (transistor 356, FIG. 3A, node D) of the OpAmp to compare with a reference voltage (from a voltage reference not shown) connected to the other differential input (transistor 354, Fig. 3A, node H).” (EX1001, 5:29-34.) As this sentence indicates, “feedback network 212” is not the “current feedback circuit” of claim 14, but rather the “feedback loop” of limitation 1[g]. (*Id.*, Fig. 2.)

107. Similarly, I did not find the terms “output voltage” and “output voltage node” outside of the claims and summary section. I note that the patent does refer to an “output node” once, as part of the phrase “output node N.” (*Id.*, 5:37.) But as with the “feedback voltage” provided by the “feedback network 212,” this “output node N” is unrelated to the “current feedback circuit” of claim 14. The patent states that the current feedback circuit comprises “transistors 374, 376, 378, 400, 402, and 394,” but none of these are connected to output node N, as shown below:

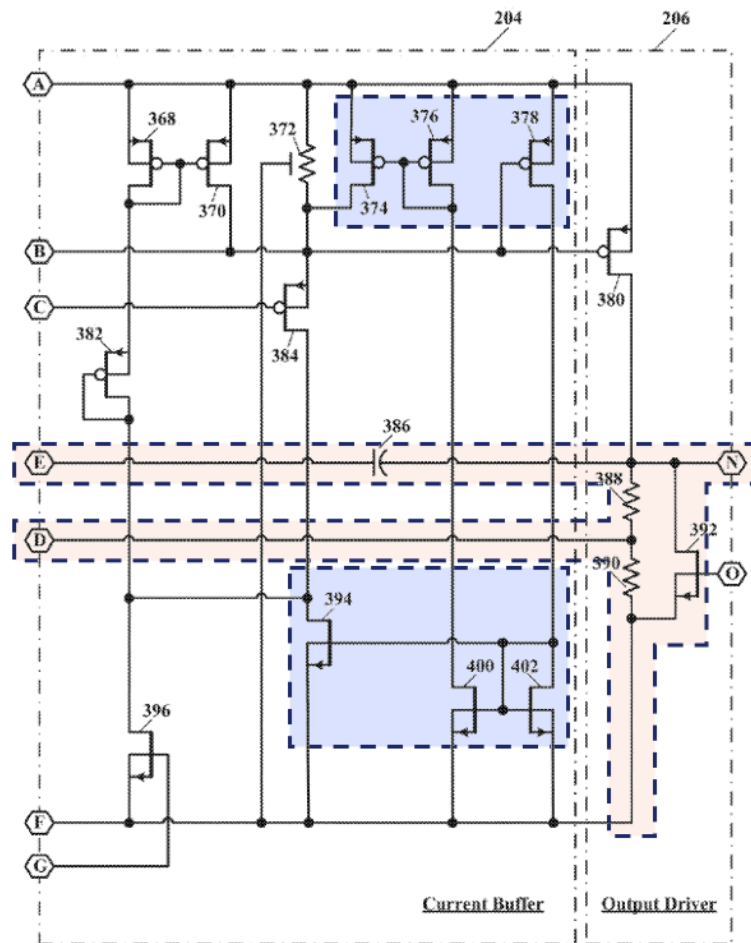
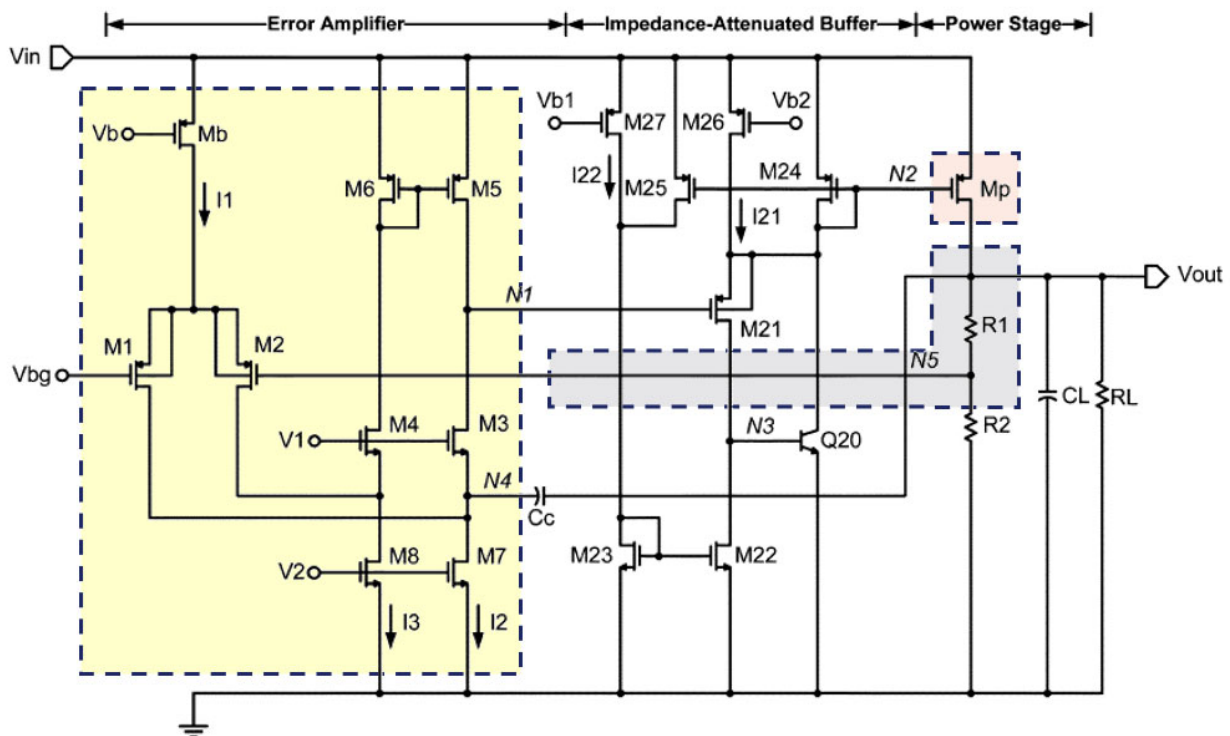


FIGURE 3B

(*Id.*, 5:13-14, Fig. 3B (annotated).) Node D, which *is* coupled to node N, is part of the feedback loop. Thus, I do not believe that a POSITA reading claim 14 in view of the rest of the specification would have been able to make sense of a “feedback voltage from an output voltage node” being provided by the “current feedback circuit.” At most, a POSITA might have tried to make sense of the claim by assuming that the applicant meant to refer to the “feedback loop” recited in limitation 1[g] instead of “the current feedback circuit.”

108. With that understanding of claim 14 in mind, it is my opinion that Al-Shyoukh's LDO meets the claim. Its feedback loop (shown in gray below) provides a feedback voltage (the voltage at N5, which is V_{out} less the voltage drop across R_1) from the output voltage node to the error amplifier (yellow):



(EX1004, Fig. 8 (annotated).)

109. I have also been asked to consider an alternative interpretation of claim 14, under which the term “current feedback circuit” does refer to the actual current feedback circuit, and the term “an output voltage node” refers to a node that provides a feedback voltage. It is my opinion that, under this meaning, Al-Shyoukh includes a current feedback circuit that provides a feedback voltage from an output voltage

node. Al-Shyoukh's current feedback circuit provides a voltage to transistors M_{24} and M_{25} at node N_2 . (*Id.*) That voltage is a "feedback voltage" because it responds to changes in the current of the output power driver at M_p . (*Id.*, 1734-35.)

Claim 15 The voltage regulator according to claim 1, wherein the current buffer driver has a low output impedance.

110. Al-Shyoukh's buffer driver has low output impedance. In fact, one of the goals of Al-Shyoukh's LDO is to reduce the output resistance of the buffer. As Al-Shyoukh explains, its proposed "technique greatly reduces the output resistance of the buffer through dynamically-biased shunt feedback." (*Id.*, 1733.) In addition, as I have explained above in my summary of Al-Shyoukh and my analysis of claim 3 above, Al-Shyoukh's current feedback circuit seeks to reduce r_{ob} , *i.e.*, the buffer's output impedance. (*Id.*, 1733-35.)

111. I note that while Al-Shyoukh uses the term "output resistance" rather than "output impedance," a POSITA would have understood these two terms to be interchangeable in this context, as resistance is the DC analogue of impedance.

Claim 16 The voltage regulator according to claim 1, further comprising capacitors in the biasing circuit for improving noise immunity thereof.

112. As I have discussed under limitation 1[d], biasing circuits were a basic and ubiquitous electronics component, and Al-Shyoukh does not describe the design of its own biasing circuit in detail, assuming the reader's familiarity with biasing

circuits. A POSITA would have recognized that Al-Shyoukh's biasing circuit could be implemented using conventional and well-understood methods.

113. Those conventional and well-understood methods included using what were known as “decoupling capacitors” or “bypass capacitors” to insulate the bias circuit from noise caused by other circuit components. This is because capacitance is inversely proportional to voltage, given an amount of charge. In the context of electrical noise, the voltage of a disturbance V_{dist} is given by Q_{noise} divided by C_{bypass} , where Q_{noise} is the amount of excess or deficient charge associated with the noise and C_{bypass} is the capacitance of the bypass capacitor. Thus, adding bypass capacitor to a circuit node reduces variations in voltage.

114. These principles were discussed widely in the art, and would have been well-known to a POSITA. For example, a 2007 dissertation by Mikhail Popovich taught that the “power and signal integrity problems in the overall system” caused by noise from one component propagating to another can be solved by “decoupling capacitors” placed at different points in the circuit. (EX1009, 12 & 217.) U.S. Patent No. 7,345,547 (“Wang”) discloses a bias circuit with “a bypass capacitor, which is coupled to an RF ground” so that it “holds the second terminal at a constant voltage despite fluctuations in the RF signal.” (EX1010, 2:64-3:1.) Wang further explains that in “common battery-powered applications,” the bias voltage is often connected to a power supply by “a suitable network of decoupling capacitors.” (*Id.*, 4:59-61.)

As a third example, a datasheet published in January 2009 by Micrel Inc. for an “Ultra High Speed 3A LDO” called MIC59300 explains that recommends using “[s]mall ceramic capacitors from VBIAS-to-ground [to] help reduce high frequency noise from being injected into the control circuitry from the bias rail and constitute good design practice,” noting that “[g]ood bypass techniques typically include one larger capacitor” and “smaller valued capacitors” in parallel with the larger capacitor “to decouple the bias supply.” (EX1011, 10.)

115. Given how the use of decoupling capacitors was a conventional practice with well-known noise immunity benefits, particularly in a bias circuit that must reliably output a constant voltage, a POSITA would have found it obvious to include them when implementing Al-Shyoukh’s voltage regulator.

Claim 17 The voltage regulator according to claim 1, wherein the voltage regulator is a USB voltage regulator.

116. A POSITA would have considered a USB voltage regulator to be an obvious application for Al-Shyoukh’s LDO.

117. As Al-Shyoukh explains, LDOs were “one of the most critical power management modules.” (EX1004, 1732.) A POSITA would have considered power management to be a key consideration in designing a USB voltage regulator, because USBs often required the host device to supply power. This is noted in U.S. Patent No. 7,644,217 Butler (“Butler”), for example. (EX1012, 1:17-27.) Butler proposes

a “method for conserving power” in a USB capable device that includes the step of providing “a USB voltage regulator.” (*Id.*, 2:29-33.)

118. In addition, LDOs like Al-Shyoukh’s could provide “regulated low-noise and precision supply voltages for noise-sensitive analog blocks.” (EX1004, 1732.) A POSITA would have recognized these benefits to be desirable for a USB voltage regulator.

Claim 18 The voltage regulator according to claim 1, wherein the current buffer driver has low input impedance and provides a high frequency pole that does not substantially affect the voltage regulator dominant pole.

119. Al-Shyoukh identifies three poles in its LDO structure, located at “the output of the error amplifier (N_1), the output of the buffer (N_2), and the output of the LDO (V_{out}).” (*Id.*, 1733.) These poles are given by the equations below:

$$\begin{aligned}p_{1|N_1} &= 1/(r_{o1}C_1) \\p_{2|N_2} &= 1/(r_{ob}C_p) \\p_{o|V_{out}} &= 1/(R_{oeq}C_L)\end{aligned}$$

(*Id.*) Here, r_{o1} is the output resistance (roughly equivalent to output impedance, as I have noted above under claim 15) of the error amplifier. (*Id.*) C_1 is “the equivalent capacitance at N_1 which is dominated by the input capacitance of the buffer C_{ib} .” (*Id.*) r_{ob} is the output resistance of the buffer. (*Id.*) In addition, p_o is the “dominant pole generated by the output capacitor.” (*Id.*, 1732.)

120. Al-Shyoukh teaches that “to achieve single-pole loop response,” p_1 and p_2 should be located at frequencies “much higher than the unity-gain frequency of the regulation loop.” (*Id.*, 1733.) It explains further that this can be accomplished by making C_{ib} (and thus C_1) and r_{ob} “very small” using the feedback mechanism I have discussed above under claim 3. (*Id.*, 1734-36.)

121. Thus, Al-Shyoukh’s buffer driver provides high frequency poles p_1 and p_2 that do not substantially affect the dominant pole p_o . As Al-Shyoukh explains, “[i]n addition to the BIA technique, current-buffer compensation allows the LDO to achieve only a single pole within the unity-gain bandwidth of the regulation loop and a good phase margin with a small compensation capacitor.” (*Id.*, 1740.)

122. The patent does not explain what it means for the current buffer driver to have “low input impedance.” But as I have noted under claim 3, I understand Patent Owner to have read the term “current buffer driver input impedance” to mean the input impedance at the point where the operational amplifier connects to the current buffer driver. Applying this same understanding to claim 18, such that “low input impedance” refers to the impedance at the point where the operational amplifier connects to the buffer driver, it is my opinion that a POSITA would have found that Al-Shyoukh’s buffer driver “has low input impedance” as claimed.

123. The input node of Al-Shyoukh’s buffer driver is N_1 , which is the output of Al-Shyoukh’s error amplifier. A POSITA would have understood that as an op-

amp, the error amplifier would have low output impedance. A POSITA would also have recognized that pole p_1 could be shifted to a higher frequency by lowering the output impedance r_{o1} of the error amplifier, in line with Al-Shyoukh's goal of setting that pole higher than the unity-gain frequency. A POSITA would have understood to implement Al-Shyoukh such that the impedance at node N_1 is relatively low.

B. Ground 2 (Rincon-Mora, Al-Shyoukh, Ivanov, and/or Stanescu)

124. I have reviewed Exhibit 1013 to the Petition, which is U.S. Patent No. 6,046,577 to Gabriel A. Rincon-Mora. I will refer to this patent as "Rincon-Mora." I have also reviewed Exhibit 1014, a related paper by Rincon-Mora published in a January 1998 issue of the *IEEE Journal of Solid-State Circuits*, entitled "A Low-Voltage, Low Quiescent Current, Low Drop-Out Regulator." I will refer to this as the "Rincon-Mora Paper." When describing these related references as a collective, I will use the term "Rincon-Mora References."

125. Having compared the disclosures of the Rincon-Mora References to the '074 patent's claims, it is my opinion that the claims are obvious over the Rincon-Mora References in view of the background knowledge of a POSITA, Al-Shyoukh, Ivanov, and/or Stanescu.

1. Summary of the Rincon-Mora References

126. The Rincon-Mora References all relate to a proposed LDO that uses a "transient response boost circuit" to improve the device's response to load changes.

This transient response boost circuit provides feedback to boost the gm of the buffer driver of the LDO.

127. As Rincon-Mora explains, there was a known problem in LDO design where conventional LDOs exhibited an “output voltage ‘glitch’” when undergoing a “full range load current step” (for example, going from no load to full load). (EX1013, 1:31-33.) The glitch was caused by the “relatively large gate terminal of the LDO voltage regulator series-connected power pass transistor.” (*Id.*, 1:33-40.) This created a “slew-rate limited node” that was slow to respond to voltage changes at the output. (*Id.*) In addition, as the Rincon-Mora Paper notes, the size of the pass device affected “the circuit’s frequency performance by reducing the value of the parasitic pole present at the output of the amplifier.” (EX1014, 37.)

128. One known way of addressing the slew-rate limitation was to add more current to the node “so as to charge and to discharge the associated capacitance of the gate.” (EX1013, 1:41-44.) But just adding current was “generally not feasible in those typical applications in which low quiescent current flow is either necessary or desired” because “the current boost to the slew-rate limited node of the LDO voltage regulator is not limited solely to ‘on demand’ conditions.” (*Id.*, 1:44-49.) The “typical applications” where this was a problem would have included “portable, battery powered applications such as laptop computers, pagers[,] cellular phones and the like.” (*Id.*, 1:21-30.)

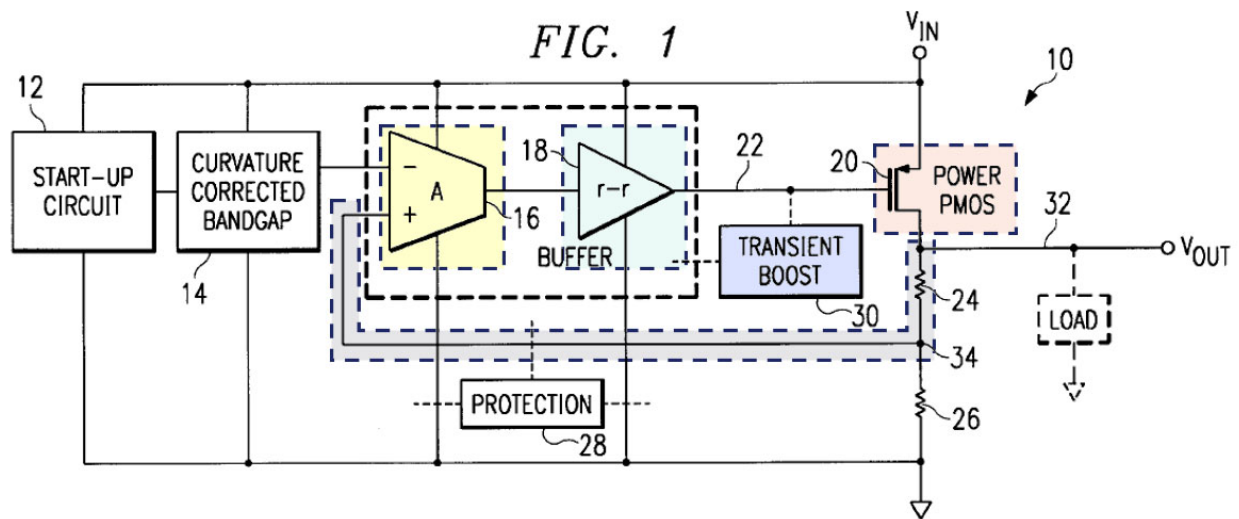
129. To address the output voltage “glitch” while minimizing the quiescent current, Rincon-Mora proposes a circuit that would “selectively apply current to a slew-rate limited node and yet requires no standby current during zero output current load conditions.” (*Id.*, 1:12-17.) Effectively, this transient response boost circuit pushes the parasitic pole associated with the gate of the pass device out to a higher frequency. (*Id.*, 4:54-61.)

130. For a stable circuit “with a phase margin of $\geq 45^\circ$,” this parasitic pole “must be greater than or equal to the unity gain frequency.” (*Id.*, 4:13-29, 4:41-51.) A POSITA would have understood that the unity gain frequency is a function of the output capacitance of the LDO because the LDO’s output pole is typically serves the dominant pole of a closed-loop frequency response. Thus, as Rincon-Mora states, keeping the parasitic pole greater than or equal to the unity gain frequency, the LDO can accommodate a wider range of output capacitance value because the parasitic pole would cause limited or negligible loop gain and phase disturbance within the unity gain frequency.

131. A POSITA would thus have found the problems laid out by the ’074 patent and Rincon-Mora to be closely related, as both are concerned with contending with a large output driver transistor that introduces a low-frequency gate pole. Their proposed solutions are also highly similar, as both use a buffer stage with current feedback circuits to push the parasitic gate pole to higher frequencies. And they

provide similar benefits, including a more stable circuit with improved power efficiency and a wider range of output capacitor values. (EX1001, 3:15-18, 3:44-49, 5:45-54, Abstract.)

132. The high-level topology of the Rincon-Mora LDO is shown below:



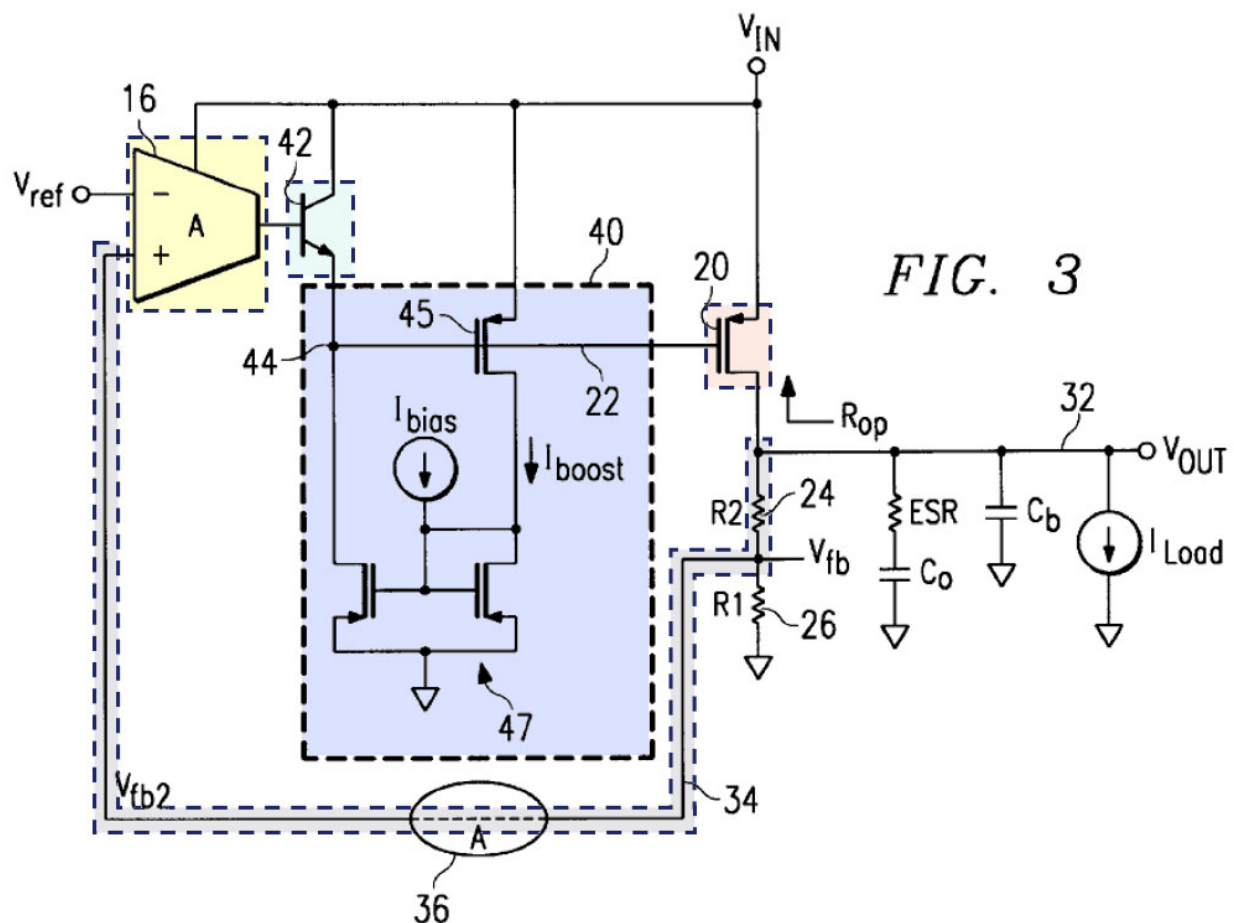
(EX1013, Fig. 1 (annotated).)

133. Rincon-Mora’s LDO includes a “start-up circuit 12” with “an external enabling input to a logic block,” and a “curvature corrected bandgap circuit 14” that can be “operatively monitored by the start-up circuit.” (*Id.*, 3:26-35.) The bandgap circuit is coupled to an input of an error amplifier 16 (shown in yellow in the above figure) “to provide a reference signal thereto.” (*Id.*, 3:35-39.)

134. The error amplifier outputs a signal to a buffer 18 (in green above) to supply a gate drive voltage to the control terminal of output transistor 20 (red) via

node 22. (*Id.*, 3:39-43.) A transient boost circuit 30 (blue) is “coupled to the slew-rate limited node 22 at the gate of transistor 20.” (*Id.*, 3:55-58.) Finally, through “node 34 intermediate resistors 24, 26,” the output transistor signal is “coupled back to a second feedback input of the error amplifier 16” (gray). (*Id.*, 3:58-62.)

135. Below is an exemplary embodiment of the Rincon-Mora LDO in more detail, with coloring annotations to match the annotations for Figure 1 above:



(*Id.*, Fig. 3 (annotated).) As shown, the error amplifier 16 outputs to a “buffer 42,” implemented here as an NPN bipolar junction transistor with its emitter terminal

coupled to “node 44 at the input of the transient boost circuit 40,” and to the gate of the pass device 20 at node 22 (which is in common with node 44). (*Id.*, 4:33-40.)

136. Rincon-Mora’s transient boost circuit is “a localized positive feedback loop to enhance transient capabilities.” (*Id.*, 4:62-65.) Through node 22, transistor 45 senses any change in the output transistor’s gate voltage. (*Id.*, 5:5-7.) Transistor 45 then delivers “a ratio of the current,” set by its size relative to the output transistor, to “current mirror 47.” (*Id.*, 5:7-8.) Thus, when the LDO is unloaded, such that there is zero output current, only a quiescent current will flow from the output transistor. (*Id.*, 5:4-7.) If transistor 45 is small relative to the output transistor, the current into current mirror 47 would be negligible in this no-load state. (*Id.*, 5:8-10.) But when the voltage regulator is suddenly loaded, the voltage change causes transistor 45 to deliver a boost current (“ I_{boost} ”) to the current mirror. (*Id.*, 5:10-16.) As the current mirror couples back to nodes 22 and 44, this feedback loop causes the amplifier to sink more current to the buffer. (*Id.*) The transient response boost circuit therefore causes the buffer to output more current, boosting gm.

137. Based on my review, each of the Rincon-Mora References describes substantially the same LDO with transient response boost circuit, and I believe a POSITA would have considered the disclosures of all three of these references when implementing the LDO.

2. Claim-by-Claim Analysis

Claim 1 A voltage regulator, comprising:

138. Rincon-Mora's LDO is a voltage regulator. (EX1013, Abstract.)

[a] an operational amplifier;

139. Rincon-Mora's LDO includes an error amplifier. (*Id.*, 3:35-43, 7:19-21, Figs. 1, 3.) In the exemplary embodiment that Rincon-Mora uses to explain its proposed LDO, the error amplifier is implemented as an OTA that drives a buffer implemented as an NPN bipolar transistor. (*Id.*, 4:33-35.) But a POSITA would not have understood Rincon-Mora to limit the design of the error amplifier to a particular amplifier topology. Claims 1 and 2 of Rincon-Mora simply recite "an error amplifier having first and second inputs and a reference output thereof," where the output is coupled to the "control input" of an "output switching device" with "a buffer circuit interposed between said reference output of said error amplifier and said output switching device." (*Id.*, 7:19-44.)

140. Thus, the error amplifier could just as easily have been implemented as an operational amplifier. As I have explained above in my analysis of limitation 1[a] under Ground 1, an LDO's error amplifier must have sufficient loop gain, and one of the basic properties of an operational amplifier, as would have been known to a POSITA, was high gain. Thus, a POSITA would have considered an op-amp to be amplifier a suitable and conventional option for Rincon-Mora's error amplifier.

141. I note that Rincon-Mora similarly does not limit other components of its LDO to specific types of devices. Thus, for example, the “buffer circuit” that is “interposed between” the error amplifier and the output switching device need not be an NPN bipolar transistor. (*Id.*, 7:19-21.) A POSITA would have known that there were many conventional ways to implement the buffer circuit, including using an NMOS transistor as the buffer driver, configured to receive the output of the error amplifier at its gate. One benefit of using only MOSFETs and not BJTs would have been cost savings, as CMOS technology was less expensive than BiCMOS.

[b] a gm enhanced current buffer driver;

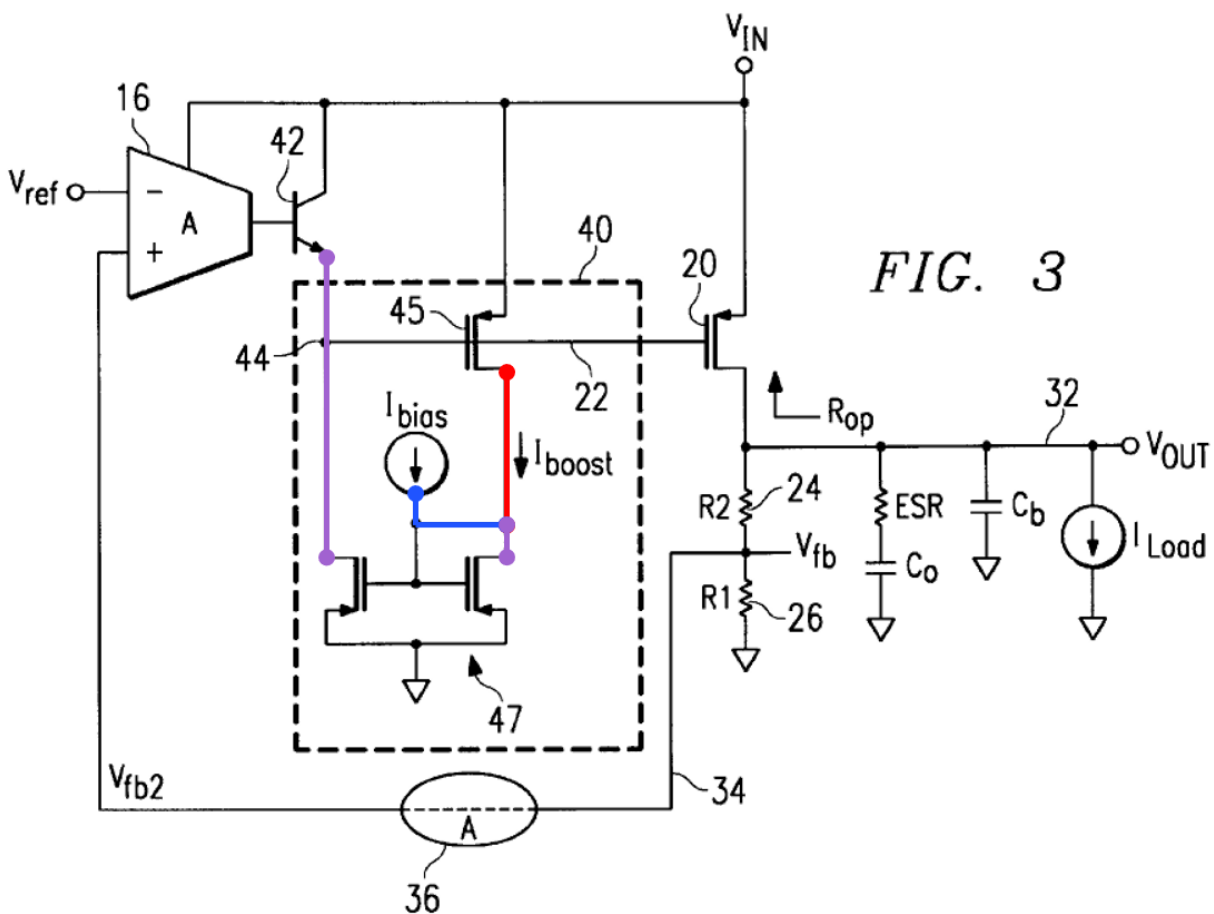
142. I have explained above in my summary of Rincon-Mora how its circuit includes a current feedback system (shown in blue below) that enhances the gm of the buffer driver (green):

But a low output impedance was conventionally understood to be a characteristic of voltage buffers, in contrast with current buffers, which have high output impedance. Furthermore, the patent describes transistor 384 as a “source follower.” (*Id.*, 4:36.) A POSITA would have known that a voltage buffer was a common application for source followers, which have high input impedance but low output impedance.

144. Rincon-Mora’s buffer has these same characteristics. If implemented as an “emitter follower connected NPN type bipolar transistor” (as in the exemplary embodiment shown in Figure 3), the buffer would have high input impedance and low output impedance (properties of an emitter follower). (*Id.*, 4:35-37.) Or, as a POSITA would have recognized, Rincon-Mora’s buffer could also be implemented as an NMOS source follower, the equivalent topology to emitter followers, but for MOSFETs. Whether a BJT or a MOSFET, Rincon-Mora’s buffer should have “low input capacitance and low output impedance” in order to “isolate the large capacitor associated with the gate of the power PMOS transistor from the large resistance of the output of” the error amplifier. (EX1014, 42.) Given that Rincon-Mora’s buffer and the ’074 patent’s buffer are both structurally and functionally similar, a POSITA would have understood Rincon-Mora’s buffer to be a “current buffer” to the same extent that the ’074 patent’s buffer is a “current buffer.”

[c] a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver;

145. As I have explained above in my summary of Rincon-Mora's LDO, its transient response boost circuit provides a gm-boost to the buffer driver. This boost is provided by a combination of a feedback current and a bias current, as shown in the figure below:



(EX1013, Fig. 3 (annotated).) Shown here in red is feedback current I_{boost} , provided by transistor 45 based on a change in voltage at the gate of the output transistor 20.

(*Id.*, 4:62-5:16.) In blue is the bias current I_{bias} , provided by a biasing circuit that is external to the LDO (and thus not shown in the figure).

146. Both these currents flow into the right-side transistor of current mirror 47. The combined current is shown in purple. This causes the left-side transistor of the current mirror to draw more current from the buffer driver transistor 42, boosting the gm of the buffer driver. As the Rincon-Mora Paper explains, this boost increases the slew-rate current of the error amplifier as $I_{\text{sr}} = I_{\text{bias}} + I_{\text{boost}} = I_{\text{bias}} + kI_{\text{load}}$, where I_{load} is the load current and k is the mirror ratio between transistors 20 and 45. (EX1014, 38.) I note that a POSITA would understand that the current mirror 47 further provides a current ratio of one in this case. I also note that, although the Rincon-Mora Paper at one point gives the slew-rate current as $I_{\text{bias}} + kI_{\text{boost}}$, a POSITA would have understood this to be a typographical error, and that the correct equation would be the one given above, which is consistent with equation (5) in the Rincon-Mora Paper, which equates I_{boost} with kI_{load} .

147. In my opinion, this discloses “a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver.” This is based on the fact that the ’074 patent’s own biasing circuit sets a “biasing ratio for gm-boost” in exactly the same way. The patent describes a bias network “fixed by transistor 396,” such that the current from the bias network is “ratio’ed in transistors 368 and 370” with the feedback current. (EX1001, 5:15-24.) This is shown below,

where Figure 3B of the patent has been annotated with colors corresponding to my description of Rincon-Mora's LDO above:

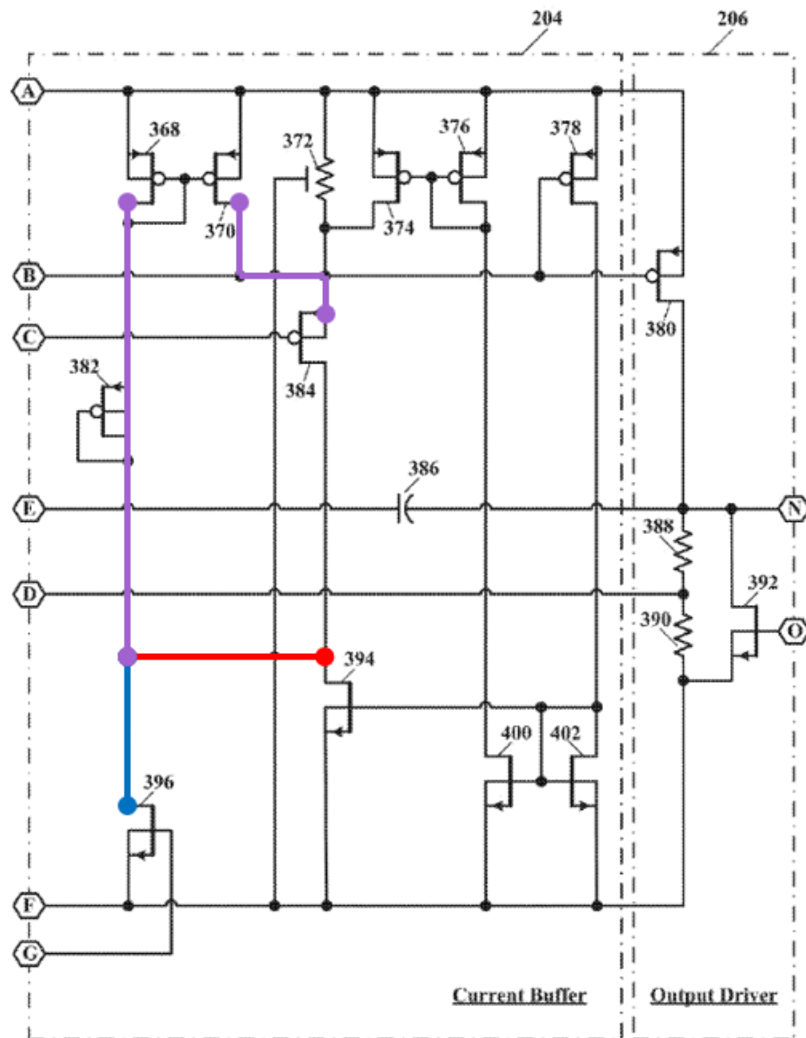


FIGURE 3B

(*Id.*, Fig. 3B (annotated).) Here, the current through transistor 368 (shown in purple) is the sum of the bias current fixed by transistor 396 (blue) and another current that flows to transistor 394 (red). The red current is a feedback current because transistor 394 is mirrored with transistor 402, which receives current from transistor 378, the

transistor that senses changes at the output driver 380. (The '074 patent also defines the current feedback circuit to include 394. (*Id.*, 5:13-14.)) Thus, the purple current is a sum (by Kirchhoff's Current Law) of a bias current and a feedback current. This sum is "ratio'ed in transistors 368 and 370" to increase current in, and thus provide a "gm-boost" to, the buffer driver transistor 384. (*Id.*, 5:21-23.)

148. In the same way, the current mirror 47 in Rincon-Mora's LDO "ratios" a current that is the sum of a bias current and a feedback current. And because the buffer driver transistor 42 is biased by the left-side transistor of the current mirror, transistor 42 receives a gm boost. (EX1004, 1734.)

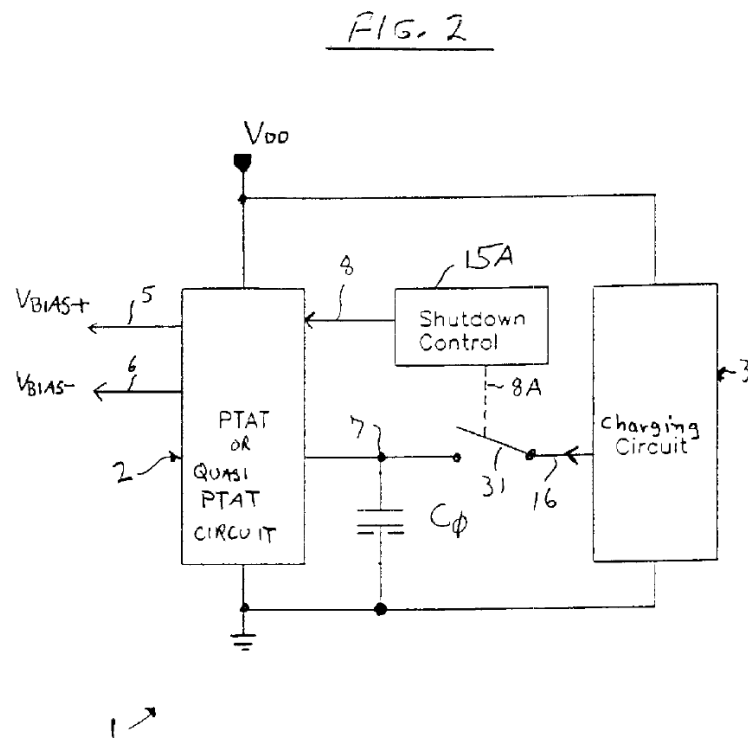
149. I understand that in the District of Delaware litigation between Aptiv and Patent Owner, Patent Owner argues that "biasing ratio" should be understood to mean a ratio of current that the current buffer draws from DC relative to the current feedback circuit. If such a meaning were to apply, it is my opinion that the Rincon-Mora References would still disclose "a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver." The Rincon-Mora LDO's biasing circuit provides a bias current I_{bias} , and a POSITA would have understood that adjusting the biasing circuit to set I_{bias} would have allowed the circuit designer to set a ratio of current drawn from DC and current drawn from the feedback circuit (I_{boost}). (EX1013, Fig. 3.)

[d] an enable/disable function to enable/disable the biasing circuit for reducing standby current;

150. Rincon-Mora's LDO receives a bias current I_{bias} from a biasing circuit, a basic and ubiquitous electronics component used to provide a constant voltage or current to various parts of an electronic device. Assuming familiarity with biasing circuits, Rincon-Mora does not describe the design of its own biasing circuit. But a POSITA would have recognized that it could be implemented using any of a variety of conventional and well-understood methods.

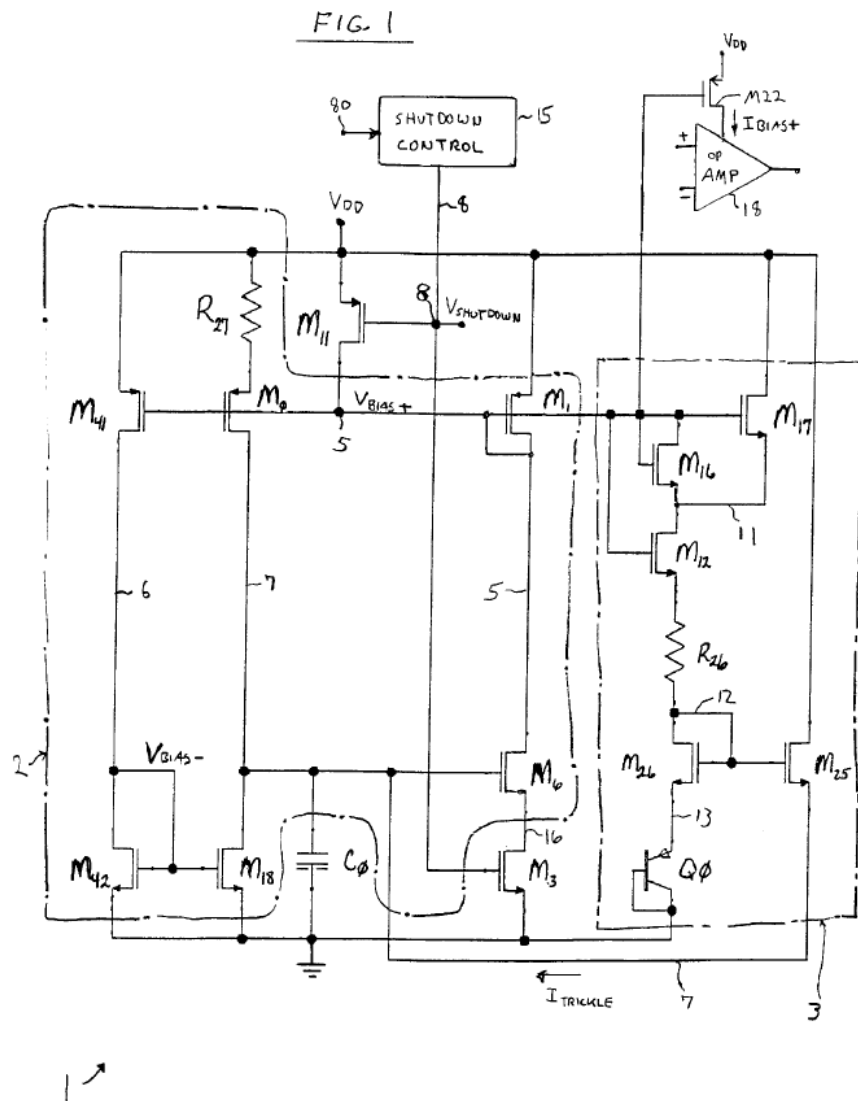
151. Ivanov, for example, describes a biasing circuit architecture that would have been suitable for use with Rincon-Mora's LDO to provide the bias current I_{bias} ; specifically, Ivanov presents "a quick turn-on disable/enable bias control circuit" for use in "integrated circuit applications." (EX1005, 1:6-9.) Ivanov explains that "[i]n certain types of electrical circuits," there are "nodes that need to be quickly charged to a predetermined voltage level." (*Id.*, 1:12-18.) At the same time, "[t]o minimize power consumption, portions of the circuitry are designed to be disabled so as to be in a quiescent, low-power state until fully functional circuit operation is needed." (*Id.*) Ivanov thus proposes a "fast disable/enable bias control circuit that is very suitable for fast disabling and subsequent fast enabling of the bias circuitry" for "applications such as voltage regulators." (*Id.*, 6:47-52.)

152. Ivanov's bias control mechanism is shown in Figure 2:



(*Id.*, Fig. 2.) The bias core circuit, represented as block 2, is “coupled between V_{DD} and ground.” (*Id.*, 4:26-29.) It produces two bias voltages, V_{BIAS+} on conductor 5 and V_{BIAS-} on conductor 6, and is coupled to shutdown control circuit 15A, which controls it through conductor 8. (*Id.*, 4:30-33.)

153. Corresponding to the block diagram of Ivanov’s Figure 2 is the detailed, exemplary implementation of the biasing circuit shown in Figure 1:



(*Id.*, Fig. 1.) As shown here, Ivanov's circuit includes a "P-channel bias core disable transistor M11," whose drain is connected to the bias core circuit 2 at node 5, whose source is connected to V_{DD} , and whose gate receives via node 8 "an external signal $V_{SHUTDOWN}$ produced by an external shutdown control circuit 15 in response to an external control signal applied to an external input 80 thereof." (*Id.*, 3:43-49.)

154. Ivanov's bias circuit creates a voltage V_{BIAS+} , "produced on conductor 5 by bias core circuit 2 when it is active," where conductor 5 is connected to the gate of transistor M22, which "ha[s] its source connected to V_{DD} and its drain connected to supply a bias current I_{BIAS+} to CMOS operational amplifier 18." (*Id.*, 3:54-63.) This I_{BIAS+} current is therefore the output bias current of this bias circuit.

155. If the shutdown control circuit wants to disable the bias current "so as to dissipate a minimum amount of power," it "produces a low value of $V_{SHUTDOWN}$," or disable signal. (*Id.*, 5:19-24.) This "turns on transistor M11," which "pulls [the voltage of] conductor 5 close to V_{DD} ." (*Id.*, 5:24-25.) This brings the source-gate voltage of transistor M22 close to zero, shutting it off and disabling I_{BIAS+} .

156. In the other direction, the shutdown control circuit can produce a high value of $V_{SHUTDOWN}$, or an enable signal, which "turns transistor M11 off and turns transistor M3 on." (*Id.*, 6:6-11.) Then the "voltage maintained across capacitor C0, i.e., the voltage on conductor 7, then is such that the current through transistors M3, M6 and M1 very rapidly pulls the voltage on conductor 5 down to a level which turns transistors M0 and M41 on and thereby re-establishes the feedback loops" of the circuit. (*Id.*, 6:11-16.) This produces "the desired value of V_{BIAS+} on conductor 5, and therefore also on the gate of the current mirror transistor M22," turning M22 on so that it outputs I_{BIAS+} . (*Id.*, 6:16-22.)

157. In my opinion, a POSITA would have recognized Ivanov's bias circuit model, including its disable/enable control mechanism, to be useful and suitable for Rincon-Mora's LDO. One of Rincon-Mora's main objectives is to improve power efficiency and reduce quiescent current. As Rincon-Mora explains, its LDO seeks to "only sink[] current upon demand" and thus "yield[] maximum current efficiency and prolonged battery life." (EX1013, Abstract, 1:18-30, 5:18-21; EX1014, 37.) Similarly, the Rincon-Mora Paper explains that "the biasing conditions for the case of zero load-current can be designed to utilize a minimum amount of current[.]" (EX1014, 37.) Ivanov, meanwhile, provides a convenient and ready-to-use way to shut off circuitry that would otherwise draw power even when not in use, explaining that this provides "a quiescent, low-power state until fully functional circuit operation is needed." (EX1005, 1:6-18.) Ivanov also states that "voltage regulators" are among the intended applications for its bias circuit. (*Id.*, 6:47-54.)

158. Implementing Ivanov's bias circuit with Rincon-Mora's LDO would not have caused undue experimentation; a POSITA could simply have used Ivanov's circuit to generate I_{BIAS+} at the desired value for Rincon-Mora's I_{BIAS} . It would have been well within the skill and knowledge of a POSITA to choose the components in Ivanov's circuit, including resistors, capacitors, and transistors, so that the circuit would generate that desired value.

159. Furthermore, Rincon-Mora's LDO is coupled to a "start-up circuit" that provides an "external enabling input to a logic block within the regulator." (EX1013, 3:27-32.) This logic block could, as a POSITA would have recognized, be Ivanov's external shutdown control circuit, or alternatively provide the "external input 80" into the shutdown control circuit. (EX1005, 3:48-49.) Rincon-Mora thus discloses structures analogous to those in Ivanov, for convenient integration of the two circuits.

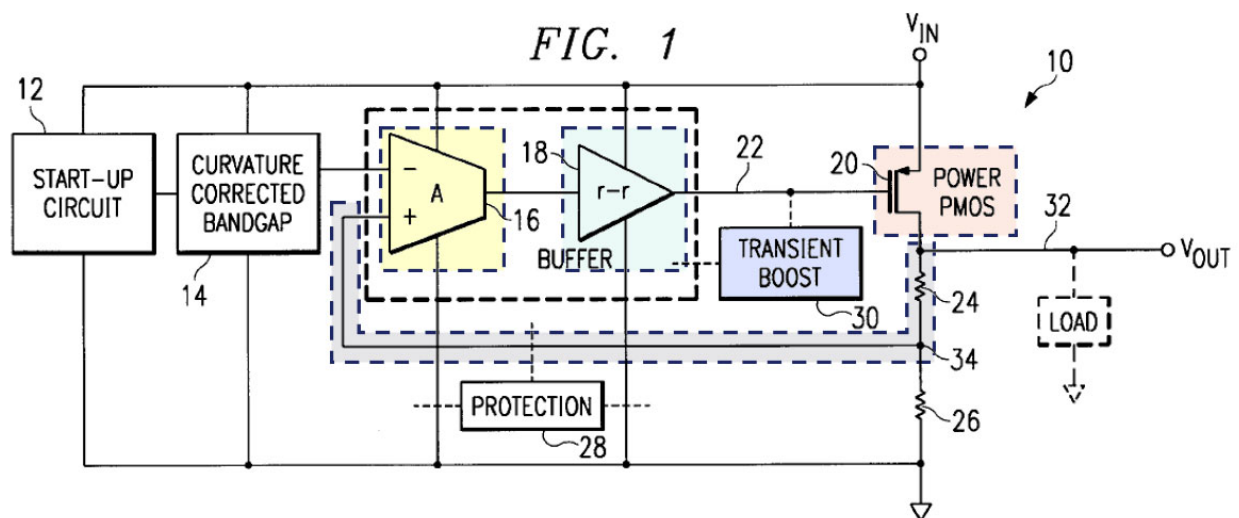
160. For these reasons, Rincon-Mora's LDO coupled to Ivanov's bias circuit would have had "an enable/disable function to enable/disable the biasing circuit for reducing standby current." I note that the '074 patent describes this "enable/disable function" only in one place—column 4, lines 52-54—where it states that "Node M" of Figure 3 "is the enable signal coming to the regulator circuit so that the module can be turned off when disabled." (EX1001, 4:52-54.) I have reproduced Figure 3 below, side-by-side with Ivanov's bias circuit:



161. I note further that the concept of an enable/disable for biasing circuitry was known widely beyond Ivanov. Power efficiency was a basic concern in analog circuit design, and it was well known that a way to save energy was to disable parts of a circuit that were not in use, biasing circuitry being a frequent candidate. Thus, I believe that it would have been obvious to a POSITA, independently of Ivanov, to implement the biasing circuitry for Rincon-Mora's LDO with an enable/disable function to reduce the standby current.

[e] an output power driver, wherein the current buffer driver is coupled between the operational amplifier and the output power driver;

162. Rincon-Mora's LDO has an output power driver (the power PMOS 20 shown in red below), with the buffer driver (green) coupled between its amplifier (yellow) and the output power driver (red):

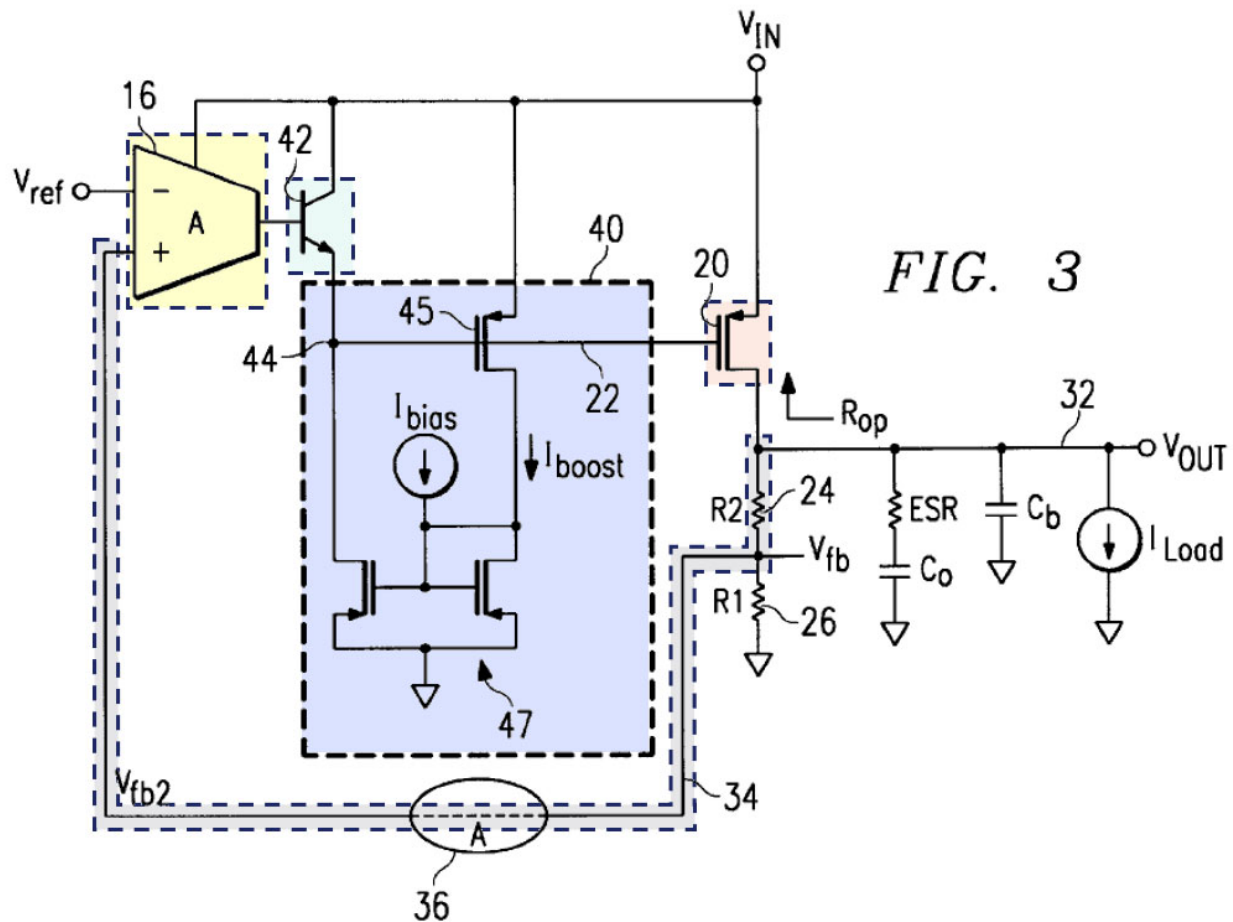


(EX1013, 3:39-47, 7:22-44, Fig. 1 (annotated).) As I have explained above in my analysis for limitation 1[a], an operational amplifier would have been one obvious option for the error amplifier.

[f] a current feedback circuit coupled between the output power driver and the current buffer driver; and

163. Referring to the figure above (and as discussed in my earlier summary of the Rincon-Mora References), Rincon-Mora's LDO has a current feedback circuit (the "transient boost" circuit shown in blue) that is coupled between its output power

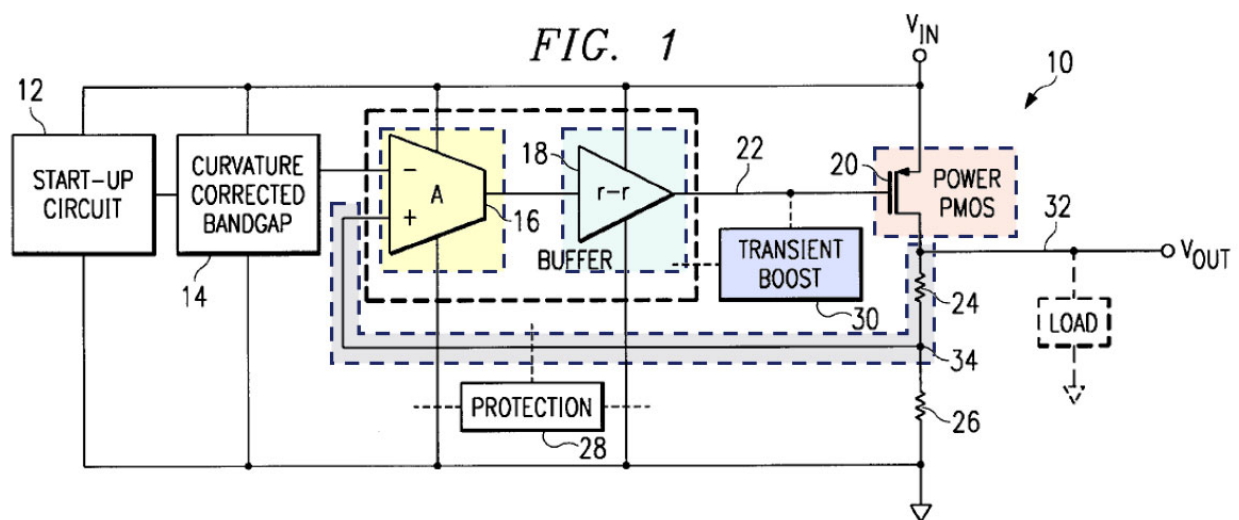
driver (red) and the buffer driver (green). (*Id.*, 4:62-5:21, Fig. 1.) Rincon-Mora also shows the details of an exemplary transient response boost circuit in Figure 3, shown below. This “current feedback circuit” includes transistor 45 and current mirror 47:



(*Id.*, Fig. 3 (annotated).) I refer back to my summary of the Rincon-Mora References and to my discussions of limitations 1[b] and 1[c] for further detail about how this current feedback circuit provides feedback to boost gm.

[g] a feedback loop coupled between the output power driver and the operational amplifier.

164. Rincon-Mora's output power driver (PMOS transistor 20, shown in red below) feeds back to a differential input of the amplifier (shown in yellow) through the pathway shown in gray:



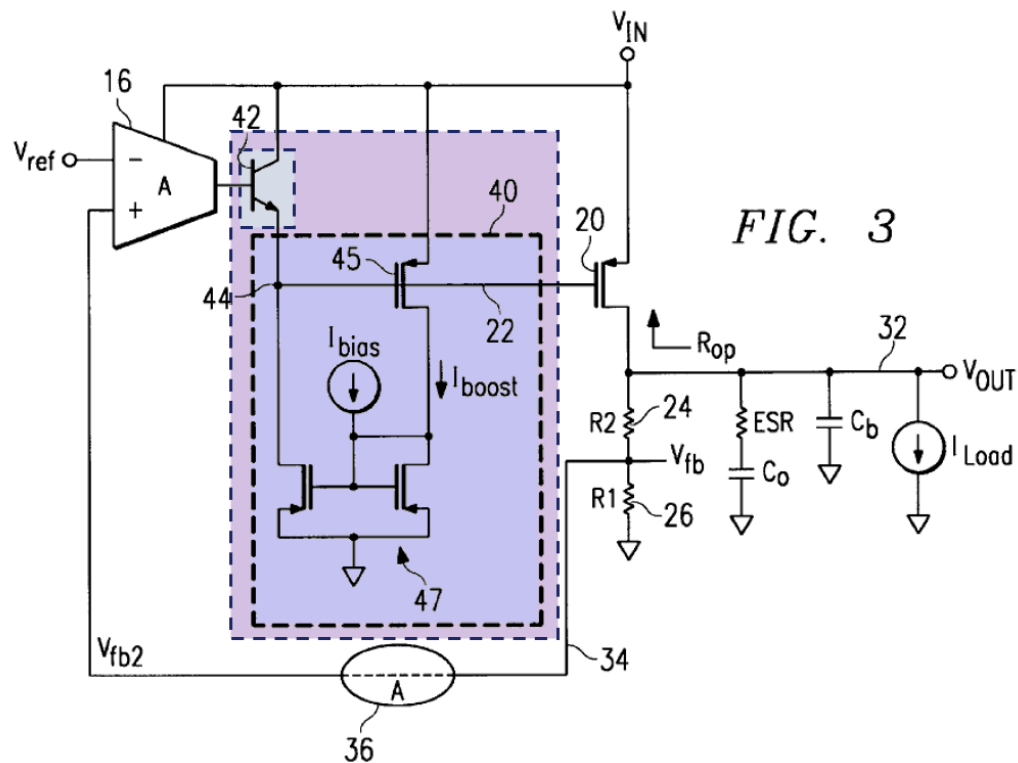
(*Id.*, Fig. 1 (annotated).) Rincon-Mora states that one of the amplifier's differential inputs is a reference voltage from a curvature corrected bandgap circuit (*Id.*, 3:26-39), while the other is a voltage from the output transistor that is “coupled back to . . . the error amplifier” via node 34 (*id.*, 3:58-62) of the gray pathway. And as explained above in my analysis for limitation 1[a], an operational amplifier would have been one obvious option for the error amplifier. Thus, the gray pathway is a “feedback loop coupled between the output power driver and the operational amplifier.”

Claim 2 The voltage regulator according to claim 1, further comprising a gm-boost circuit coupled to the current buffer driver.

165. In my opinion, Rincon-Mora's LDO has a gm-boost circuit because its current feedback circuit boosts gm of the buffer driver. (*Id.*, 4:62-5:21, Figs. 1, 3.)

166. The '074 patent does not define "gm-boost circuit," but it does describe an embodiment where the "gm-boost stage" comprises "transistors 368, 370, 374, 376, 378, 382, 396, 394, 400, 402, 384 and resistor 372," in reference to Figure 3B. (EX1001, 5:8-10.) This includes each component of the "current driver," which the patent explains comprises "transistors 370, 384, and 394, and resistor 372" (*id.*, 5:10-12), as well as the current feedback circuit, which comprises "transistors 374, 376, 378, 400, 402, and 394" (*id.*, 5:12-14). Based on this example—the sole example in the patent's specification—I understand that the "gm-boost circuit" may include the current feedback circuit and the buffer driver.

167. Thus, Rincon-Mora's LDO has a buffer driver (highlighted in green), a current feedback circuit (blue), comprising a gm-boost circuit (purple):



(EX1013, Fig. 3 (annotated).)

Claim 3 The voltage regulator according to claim 2, wherein the gm-boost circuit increases the current buffer driver input impedance.

168. I have been asked to consider a potential interpretation of claim 3 where the phrase “the gm-boost circuit increases the current buffer driver input impedance” is understood to mean that because of the current feedback provided by the gm-boost circuit, a transistor with relatively higher input impedance may be chosen for the buffer driver. It is my opinion that, under this meaning, Rincon-Mora’s LDO, when implemented with an NMOS transistor as its buffer, would be a voltage regulator with such a gm-boost circuit.

169. I have noted above in my analysis for limitation 1[a] that Rincon-Mora does not limit its “buffer circuit” to specific types of devices, even if the buffer is a BJT in the exemplary embodiment. (*Id.*, 7:19-21.) A POSITA would have known of many conventional ways to implement the buffer, including with an NMOS as the buffer driver. Cost savings, for example, would have been one easily recognizable advantage of an NMOS over a BJT.

170. Under this obvious implementation of Rincon-Mora’s LDO, the current feedback circuit (and thus the gm-boost circuit) would reduce the quiescent current that the buffer must supply by adding their own current. (I refer back to my summary of the Rincon-Mora References and to my discussions of limitations 1[b] and 1[c] for further detail about how this current feedback circuit provides feedback to boost gm.) A POSITA would have recognized that, as a result, a smaller NMOS may be used in the buffer, with lower input capacitance and hence higher input impedance. (*Id.*)

Claim 4 The voltage regulator according to claim 2, wherein the gm-boost circuit enables the current buffer driver to have a large gm value.

171. I understand that in the District of Delaware litigation between Aptiv and Patent Owner, Patent Owner argues that the term “enables the current buffer driver to have a large gm value” means “increases the gm value of the current buffer driver.” If such a meaning were to apply, it is my opinion that the Rincon-Mora

LDO is a voltage regulator “wherein the gm-boost circuit enables the current buffer driver to have a large gm value.” As explained above for claims 1 and 2, Rincon-Mora’s gm-boost circuit increases the current at the buffer driver transistor 42, and thus increases its gm value. (*Id.*, 1734.)

Claim 5 The voltage regulator according to claim 1, further comprising a compensation capacitor coupled between the output power driver and a cascode node of the operational amplifier.

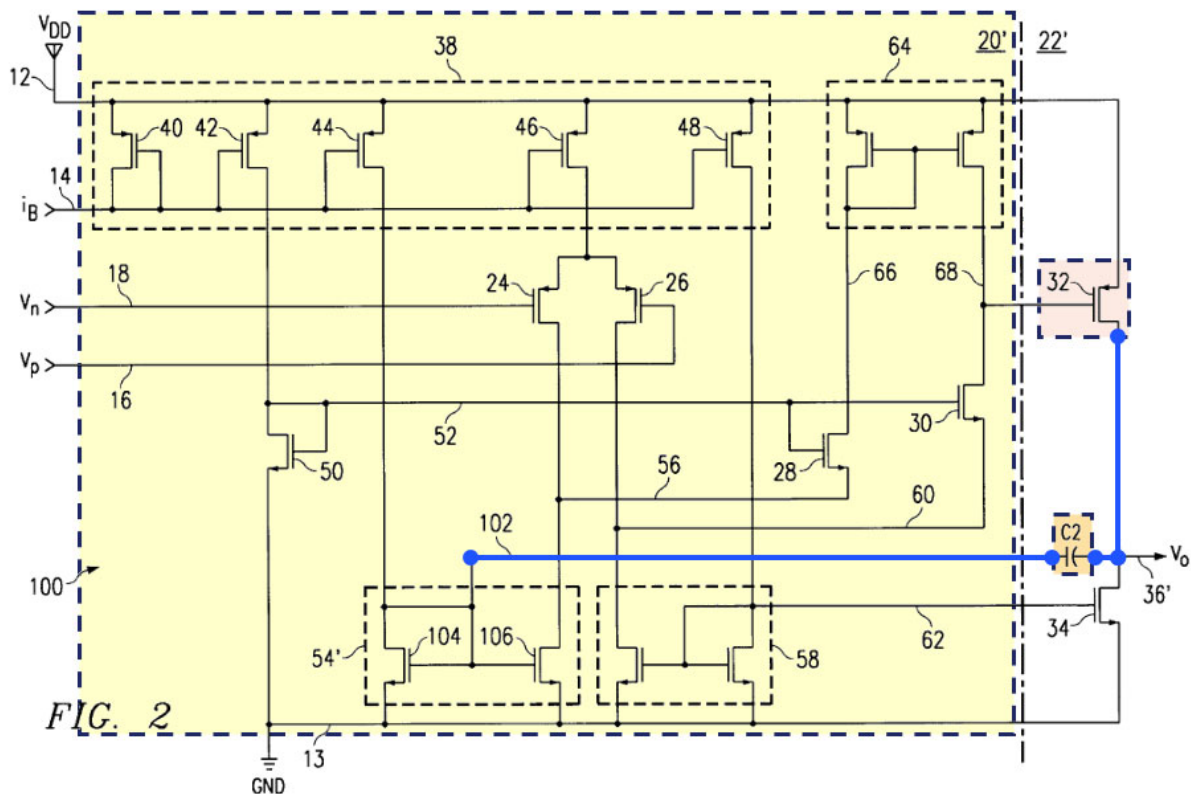
172. Compensation capacitors, *e.g.*, Miller capacitors, were well-known and used conventionally to improve the frequency response of a circuit by increasing the phase margin. In particular, Miller compensation was a common technique for pole splitting to stabilize a closed loop circuit. This technique works as follows: When a compensation capacitor is added between the input and output node of an inverting amplifier, that capacitance value will be effectively amplified by $(1 + A_v)$, where A_v is the absolute gain of the amplifier. This is because the current flowing through this compensation capacitor is increased by the amplifier’s gain. And because this amplified capacitance will load the input node, it can cause the frequency pole at the input node to be significantly lower and become the dominant pole, while pushing the frequency pole at the output node to higher frequency. This circuit technique is often called “pole splitting,” as the frequency spacing between the input and output poles increases. Separating the two frequency poles helps stabilize the circuit when

this inverting amplifier is used in a closed loop configuration, such as in a voltage regulator.

173. As a POSITA would have understood, however, Miller compensation could introduce a right half plane (RHP) zero due to the feedforward current through the Miller capacitor. An RHP zero is a frequency zero that sits in the right half plane (*i.e.*, the real part of the frequency zero is positive) of the pole-zero plot, which is a graphical representation of a system's transfer function in the complex plane. The feedforward current is the current that flows from the input to the output node of the inverting amplifier through the Miller capacitor. If the RHP zero is not sufficiently high, it would degrade the closed-loop circuit's stability. A common technique for resolving this issue was to couple the capacitor to the cascode node of an amplifier. Doing so would remove the RHP zero because the cascode device of the amplifier would block the feedforward current through Miller capacitor.

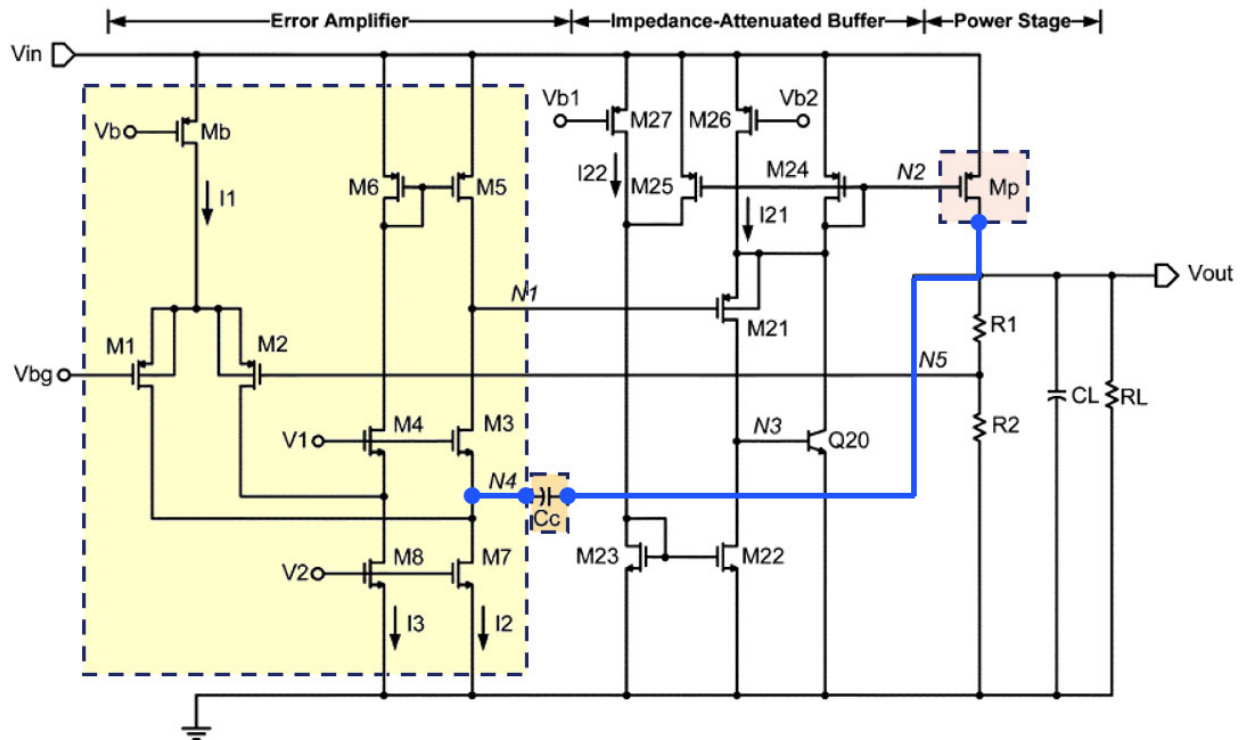
174. These principles would have been well-known to a POSITA and are reflected in the art. Dr. Rincon-Mora's doctoral dissertation on "Current Efficient, Low Voltage Low Drop-out Regulators," for example, discusses using a capacitor C_c in the curvature corrected bandgap reference supplying a voltage reference to an LDO to provide stability. (EX1015, 109.) U.S. Patent No. 6,084,475 (a second patent to Gabriel A. Rincon-Mora, which I will refer to as "Rincon-Mora '475") similarly states that a "Miller-compensating capacitance" would have been a "well

known technique for improving phase margin” and the stability of a feedback circuit. (EX1016, 1:11-16, 3:1-9.) As shown below, Rincon-Mora '475 discloses a circuit with such a capacitor (orange) between an output PMOS (red) and an amplifier (yellow):



(*Id.*, Fig. 2 (annotated).) A POSITA would have understood that the connection to node 102 and then current mirror device 106 effectively couples the Miller capacitor C2 to the cascode node 56 of the amplifier, and that the cascode device 28 that would block the feedforward current through the Miller capacitor and hence eliminate the RHP plane zero.

175. And as explained in my analysis above for this claim under Ground 1, Al-Shyoukh also uses a Miller capacitor to “achieve stability in the full range of the load current”:



(EX1004, 1735, Fig. 8 (annotated).) The connection point, N₄, is a cascode node because it connects to the cascode device at M₃. I refer to my analysis under Ground 1 for further detail regarding Al-Shyoukh’s compensation capacitor.

176. Thus, the benefits of Miller compensation were well-known and widely applied in the art before 2013. The same benefits would have been applicable to the Rincon-Mora LDO, because, as Rincon-Mora explains, the LDO must remain stable, for example by keeping the phase margin at or above 45°. (EX1013, 4:27-29.) A

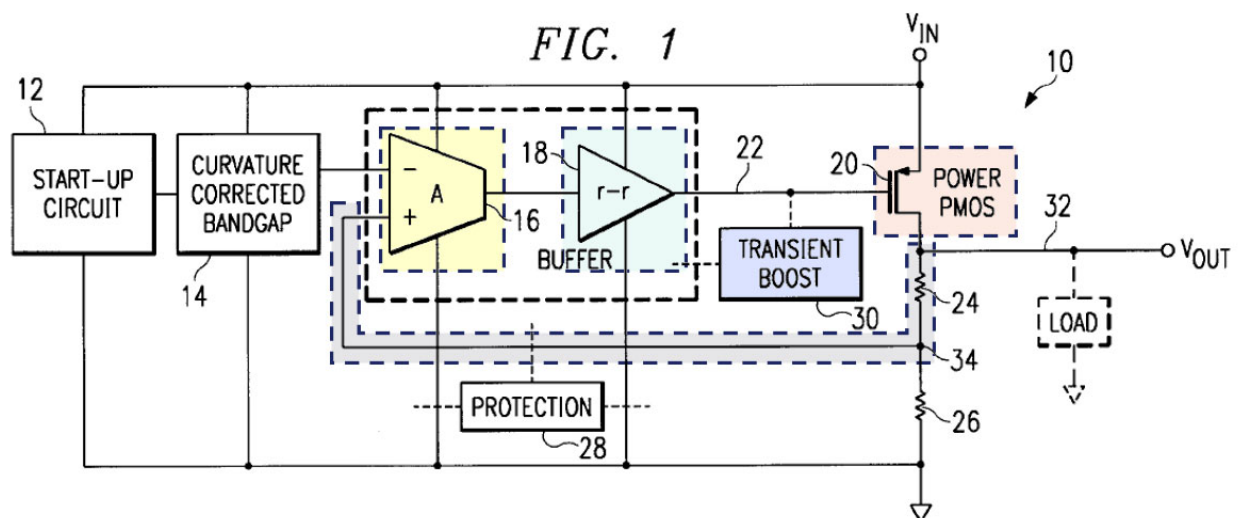
POSITA would therefore have been motivated to place a Miller capacitor between Rincon-Mora's output transistor 20 and a cascode node of the error amplifier when implementing the LDO, and could have done so without undue experimentation and with a reasonable expectation of success.

Claim 6 The voltage regulator according to claim 1, wherein the voltage regulator is a low drop out (LDO) voltage regulator.

177. Rincon-Mora's voltage regulator is an LDO. (*Id.*, Abstract.)

Claim 7 The voltage regulator according to claim 1, wherein the operational amplifier has a first input adapted for coupling to a voltage reference, and a second input coupled to the feedback loop.

178. Rincon-Mora's error amplifier (highlighted in yellow below) has a first input adapted for coupling to a voltage reference (*i.e.*, from a "curvature corrected bandgap circuit") and a second input coupled to the feedback loop (gray):

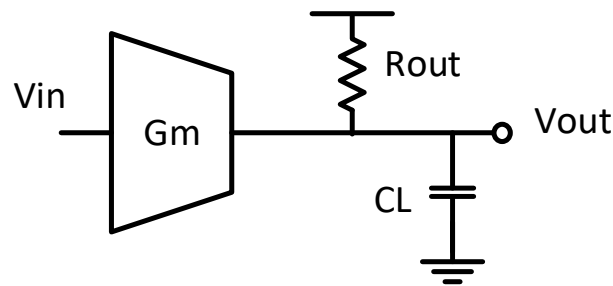


(*Id.*, 3:35-39, 7:19-21, Fig. 1 (annotated).) I also refer to my summary of the Rincon-Mora References and my opinions regarding limitation 1[g] above.

Claim 8 The voltage regulator according to claim 1, wherein the operational amplifier is a low gain and high bandwidth amplifier.

179. I understand that in the District of Delaware litigation between Aptiv and Patent Owner, Patent Owner argues “a low gain and high bandwidth amplifier” is one “optimized for high bandwidth with a commensurate reduction of gain.” If such a meaning were to apply, it is my opinion that it would have been obvious to a POSITA to implement Rincon-Mora’s LDO with such an amplifier, as explained below.

180. It was well-understood that gain and bandwidth are characteristics that trade off with each other in an operational amplifier. Below is a basic single-stage operational amplifier model that consists of a transconductance input stage and an output load, where V_{in} is the input voltage of the operational amplifier, G_m is the transconductance input stage that converts input voltage to an output current, R_{out} is the output resistance of the operational amplifier, C_L is the output/load capacitance of the operational amplifier, and V_{out} is output voltage of the operational amplifier:



The gain of this operational amplifier is equal to the product of G_m and R_{out} , while the bandwidth is equal to the reciprocal of the product of R_{out} and C_L . Thus, an operational amplifier with high R_{out} would have high gain and low bandwidth, and one with low R_{out} would have the opposite—low gain and high bandwidth.

181. A POSITA would have known that determining the tradeoff between gain and bandwidth (*e.g.*, through selection of R_{out}) was a basic step in designing and implementing an operational amplifier, with some of the many conventional, readily available designs having lower gain and higher bandwidth than others. A POSITA would therefore have recognized that choosing an op-amp that is “optimized for high bandwidth with a commensurate reduction of gain” for the error amplifier in Rincon-Mora’s LDO would have been a simple matter of design choice. (*Id.*)

182. A POSITA would also have been generally aware of the benefits of an operational amplifier with high bandwidth (and commensurately low gain), as this was acknowledged throughout the art. For example, a 2008 Master’s Thesis written by Miranda J. Ha, called “A Low-Power, High-Bandwidth LDO Voltage Regulator with No External Capacitor,” explains that bandwidth is an “important specification

in voltage regulator design,” and that “[t]he higher the bandwidth of a regulator, the more quickly it can react to changes in input and power supply and keep the output voltage constant.” (EX1007, 8.) A POSITA would have understood this principle to apply to Rincon-Mora, which also presents an LDO designed to respond quickly to changes in load. (EX1013, 1:10-59; EX1014, 36-38.)

183. As another example, a paper by Ye, *et al.*, published in January 2013 by *IEEE Transactions on Circuits and Systems* states that a relatively low-gain op-amp with high gain-bandwidth product can improve power efficiency for a high bandwidth closed-loop circuit. (EX1008, 96-97.) A closed-loop circuit is a type of circuit configuration with a feedback loop. Rincon-Mora’s LDO is a closed-loop circuit in which power efficiency is a chief concern. (EX1013, 1:10-59; EX1014, 36-38.)

184. Thus, not only would using a low-gain, high-bandwidth amplifier in the Rincon-Mora LDO have been obvious as a matter of design choice, but a POSITA would also have found motivation to do so based on the known advantages of high bandwidth.

185. I further understand that in the District of Delaware litigation between Aptiv and Patent Owner, Patent Owner has argued that a folded cascode operational amplifier with a single stage of gain (comprising a differential input and a cascode load) is “a low gain and high bandwidth amplifier” within the meaning of claim 8.

Under such a reading of the claim, it is my opinion that the Rincon-Mora LDO, as modified to use Al-Shyoukh's error amplifier (as discussed below under claim 9), would have rendered claim 8 obvious because Al-Shyoukh's amplifier has a single-stage folded-cascode structure.

Claim 9 The voltage regulator according to claim 8, wherein the low gain and high bandwidth amplifier is a folded-cascode amplifier.

186. In my opinion, a POSITA would have recognized Al-Shyoukh's error amplifier (an operational amplifier with a single-stage folded-cascode structure, as I discuss under Ground 1 above) to be a suitable design choice for the error amplifier in Rincon-Mora's LDO.

187. Again, as a POSITA would have understood, Rincon-Mora does not limit the error amplifier to OTAs or any other topology. Claims 1 and 2 of Rincon-Mora recite "an error amplifier having first and second inputs and a reference output thereof," where the output is coupled to the "control input" of an "output switching device" with "a buffer circuit interposed between said reference output of said error amplifier and said output switching device." (EX1013, 7:19-44.)

188. A POSITA would not have encountered undue experimentation when adding Al-Shyoukh's error amplifier to Rincon-Mora's LDO. The connections were simple—an input from a voltage reference, an input from feedback, an output to the buffer driver, and a connection to the supply voltage. They were also conventional

connections present in the typical LDO configuration, as discussed in my discussion of the technical background above.

189. Moreover, a POSITA would have found Al-Shyoukh's error amplifier to be especially suitable for Rincon-Mora's LDO because Al-Shyoukh and Rincon-Mora are highly analogous art. The two LDOs have the same topology, comprising an error amplifier, a buffer circuit, and an output driver that feeds back to one of the differential inputs of the amplifier. The references discuss the same goals of power efficiency and improving the LDO's transient response. They also propose the same general approach (using feedback mechanisms to boost current at the buffer driver) to achieve these goals. In fact, Al-Shyoukh's first citation (in a part of the paper that explains the motivations behind the proposed LDO) is to the Rincon-Mora Paper. (EX1004, 1732 (noting how an "increased level of integration in portable devices" requires an LDO to deliver high load current while also maintaining a low no-load quiescent current to improve current efficiency").) In addition, a POSITA would have known that a single-stage folded cascode structure is easier to stabilize and more power efficient as compared to a multi-stage structure, while still being able to provide sufficient DC gain. This would have provided further motivation to use a single-stage folded-cascode structure like Al-Shyoukh's with Rincon-Mora's LDO.

Claim 10 The voltage regulator according to claim 9, wherein the operational amplifier comprises diode connected PMOS transistors for lowering an output impedance of the folded-cascode amplifier.

190. As discussed under claim 9, it is my opinion that a POSITA would have found it obvious to use Al-Shyoukh's error amplifier as the error amplifier in the Rincon-Mora LDO. And as discussed under Ground 1, this error amplifier includes "a simple diode-connected active load using transistors M_5 and M_6 ," resulting in "a smaller output resistance of the error amplifier r_{o1} ." (EX1004, 1738.) A POSITA would have recognized that including these diode-connected transistors to reduce the amplifier's output resistance would have been advantageous in Rincon-Mora's LDO. The Rincon-Mora Paper points out, for example, that as the maximum load-current specification increases, so does the size of the pass device, meaning a higher load capacitance for the amplifier. (EX1014, 37.) It goes on to explain that to keep the phase margin from degrading and the regulator from becoming unstable, the amplifier's output impedance should be reduced. (*Id.*, 37.)

Claim 11 The voltage regulator according to claim 1, wherein the current buffer driver is an operational transconductance amplifier (OTA).

191. In my opinion, a POSITA would have found it obvious to modify the Rincon-Mora LDO to use an OTA as its buffer driver, as taught by Stanescu.

192. Stanescu discloses an LDO, much like the Rincon-Mora References. According to Stanescu, some prior art LDOs (as of Stanescu's priority date in 2001) implemented the buffer as a "foldback cascode operational amplifier with NPN input transistors and an NPN common-collector output stage." (EX1006, 2:12-14.) But, Stanescu points out, this could be expensive and suffer from "limited closed-loop bandwidth" as well as a "non-ideal transient response, even at a low ESR, due to a low slew-rate." (*Id.*, 2:42-54.) Stanescu thus proposes using an OTA as the buffer, as illustrated below:

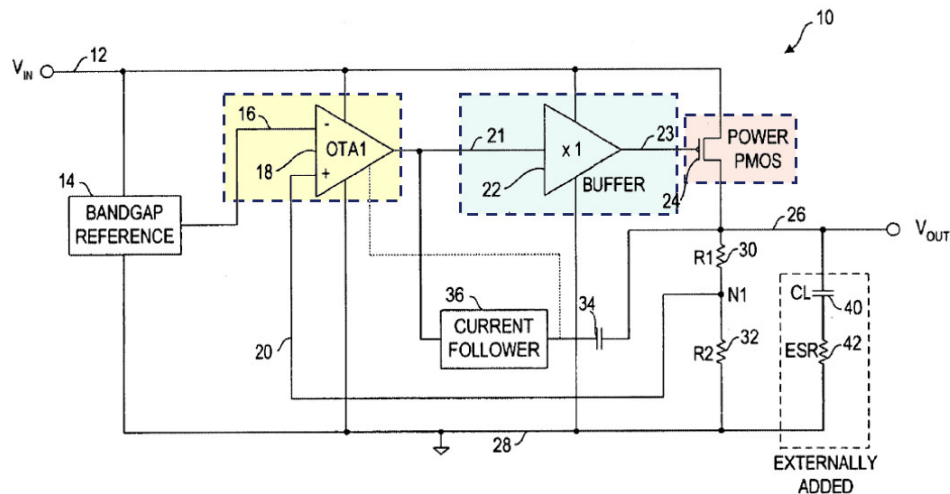


FIG. 1 (PRIOR ART)

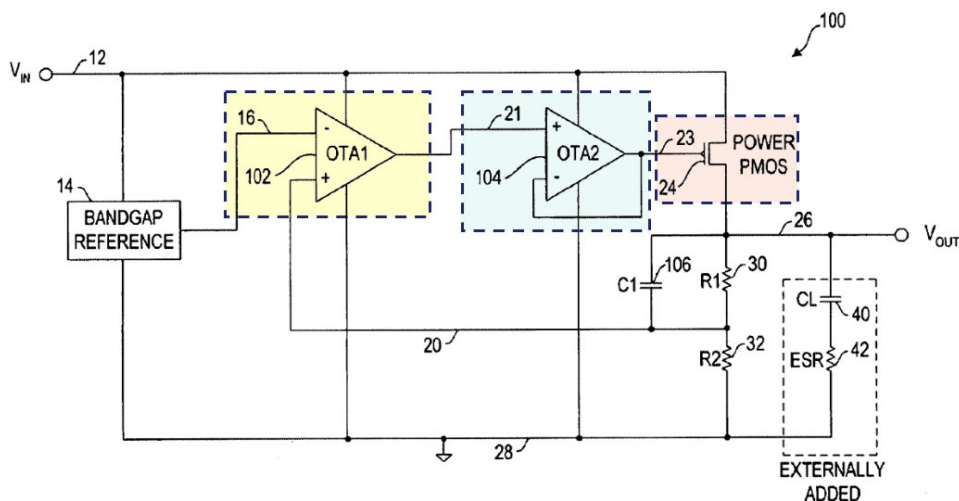


FIG. 2

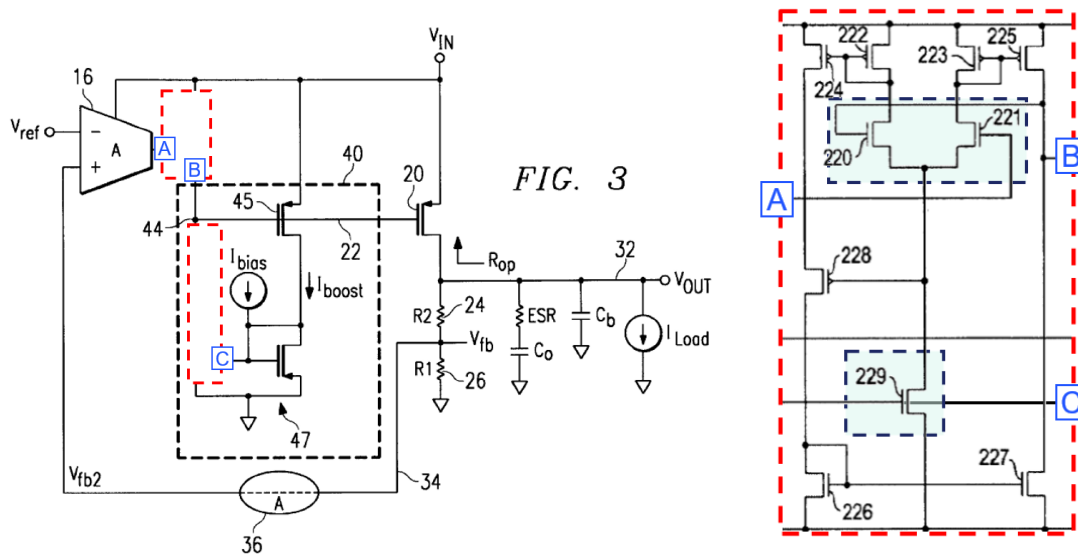
(*Id.*, Figs. 1, 2 (annotated).) Figure 1 above shows the prior art LDO using an op-amp as the buffer. Figure 2 is Stanescu's LDO, with an OTA in its place. This OTA is a voltage follower with its output coupled back to its inverting input. (*Id.*, 3:2-4.) Thus, it has unity gain feedback. As a POSITA would have understood, unity gain feedback produces a low output impedance because it forms a series-shunt feedback

loop, lowering the OTA's output impedance by $(1+T)$, where T is the loop gain. A POSITA would also have understood that unity gain feedback is advantageous in an LDO because it less-than-unity gain would degrade the gain provided by the error amplifier, making the LDO's voltage feedback mechanism less effective in keeping its output constant at the desired voltage.

193. It would have been obvious to a POSITA to implement the buffer in the Rincon-Mora LDO as an OTA, following Stanescu. As noted above under limitation 1[a], Rincon-Mora does not limit its "buffer circuit" to specific types of devices, even if the buffer is a BJT in the exemplary embodiment. (EX1013, 7:19-21.) And a POSITA would have recognized that Stanescu's OTA as a suitable option. In fact, Stanescu identifies Rincon-Mora's LDO as a prior-art LDO on which it improves. (EX1006, 2:18-21.) As Stanescu explains, the buffer in Rincon-Mora's exemplary embodiment "is built in a biCMOS process," which can be a drawback because it is expensive. (*Id.*, 2:18-21, 2:42-44.) Furthermore, a POSITA would have considered Stanescu and the Rincon-Mora References to be highly analogous art. Both describe LDOs for use in portable battery-powered devices, and designed to save power by minimizing quiescent current. (EX1004, 1732; EX1006, 1:17-28, 7:64-8:3.) Thus, a POSITA would have considered Stanescu's teachings, including its identified advantages, to apply to Rincon-Mora. Moreover, a POSITA would have understood that using Stanescu's voltage follower OTA would further Rincon-Mora's goal of

pushing the parasitic pole to higher frequencies (EX1013, 4:13-29, 4:41-61; EX1014, 37-38), because the OTA with unity feedback has low output impedance.

194. An exemplary combined circuit using Stanescu's OTA is shown below:



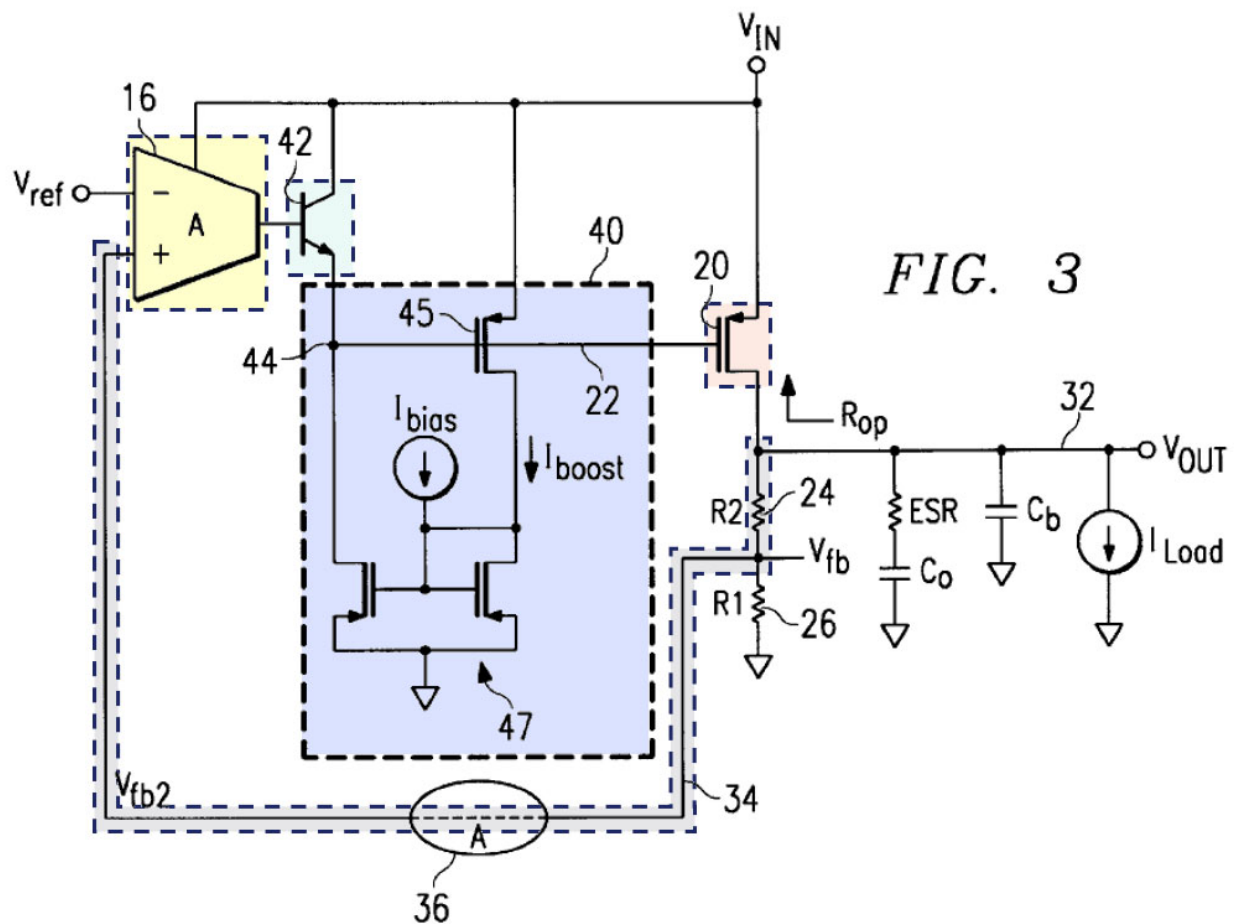
The figure on the left shows a modified version of Rincon-Mora's circuit, with red dotted lines marking the areas into which Stanescu's OTA would fit. The figure on the right shows how Stanescu's OTA would couple to those areas; transistor 221 would receive an input from Rincon-Mora's error amplifier at node A, the output of the OTA would couple to Rincon-Mora's node 44 via node B, and transistor 229 would form the left side of Rincon-Mora's current mirror 47 via node C.

195. This combined circuit would preserve the feedback mechanism of the Rincon-Mora LDO because transistor 45 continues to sense a current change at the output transistor via node 22, generating a feedback current I_{boost} that is mirrored,

along with the bias current I_{bias} , in current mirror 47. The left-side transistor of the current mirror becomes Stanescu's transistor 229, which pulls further current from transistors 220 and 221 as a result of the feedback, boosting gm of the OTA/buffer. This circuit is one example of many variants that a POSTIA could have arrived at without undue experimentation when integrating Stanescu's unity-feedback OTA into Rincon-Mora's LDO, given the small number of necessary connections, the well-known structure of Stanescu's OTA, and the clear purposes of each transistor.

Claim 12 The voltage regulator according to claim 1, wherein the current feedback circuit senses a current change at the output power driver.

196. As explained in my summary of the Rincon-Mora References and my analysis of claim 1 above, the current feedback circuit in Rincon-Mora's LDO (in blue below) produces feedback by sensing a current change at output transistor 20:



(EX1013, Fig. 3 (annotated).) Transistors 45 and 20 are connected at their gates to node 22 (which is in common with node 44). Transistor 45 senses changes in current at transistor 20 by sensing a corresponding voltage change at node 22. And because the gate-to-source voltage of transistors 20 and 45 are exactly the same, the current flow in transistor 45 would track that of transistor 20. The Rincon-Mora Paper also explains this, noting that the boost circuit operates by “sensing the output current of the regulator and feeding back a ratio of the current to the slew-rate limited node of

the circuit,” such that transistor 45 (“Mps” in the Paper) “sources a fraction of the current flowing through the output transistor.” (EX1014, 37.)

Claim 13 The voltage regulator according to claim 1, wherein the current feedback circuit provides transient enhancement for improved load regulation.

197. Rincon-Mora’s LDO is, as the title indicates, a “Low-Dropout Voltage Regulator Incorporating a Current Efficient Transient Response Boost Circuit.” (EX1013, Title.) And as Rincon-Mora explains, the primary goal of the boost circuit is to improve the voltage regulator’s “transient response” to sudden changes in load. (*Id.*, 1:31-49.) Rincon-Mora’s boost circuit allows the regulator to “selectively apply current to a slew-rate limited node and yet requires no standby current during zero output current load conditions.” (*Id.*, 1:12-17.) Thus, a POSITA would have found Rincon-Mora’s transient response boost circuit to be a current feedback circuit that provides transient enhancement for improved load regulation.

Claim 14 The voltage regulator according to claim 1, wherein the current feedback circuit provides a feedback voltage from an output voltage node.

198. From my review of the ’074 patent, the only time the phrase “feedback voltage” appears (excluding the claims and the part of the “Summary” section that echoes the claim language) is at column 5, lines 29-34, which state: “This feedback network 212 provides feedback voltage to one differential input (transistor 356, FIG. 3A, node D) of the OpAmp to compare with a reference voltage (from a voltage

reference not shown) connected to the other differential input (transistor 354, Fig. 3A, node H).” (EX1001, 5:29-34.) As this sentence indicates, “feedback network 212” is not the “current feedback circuit” of claim 14, but rather the “feedback loop” of limitation 1[g]. (*Id.*, Fig. 2.)

199. Similarly, I did not find the terms “output voltage” and “output voltage node” outside of the claims and summary section. I note that the patent does refer to an “output node” once, as part of the phrase “output node N.” (*Id.*, 5:37.) But as with the “feedback voltage” provided by the “feedback network 212,” this “output node N” is unrelated to the “current feedback circuit” of claim 14. The patent states that the current feedback circuit comprises “transistors 374, 376, 378, 400, 402, and 394,” but none of these are connected to output node N, as shown below:

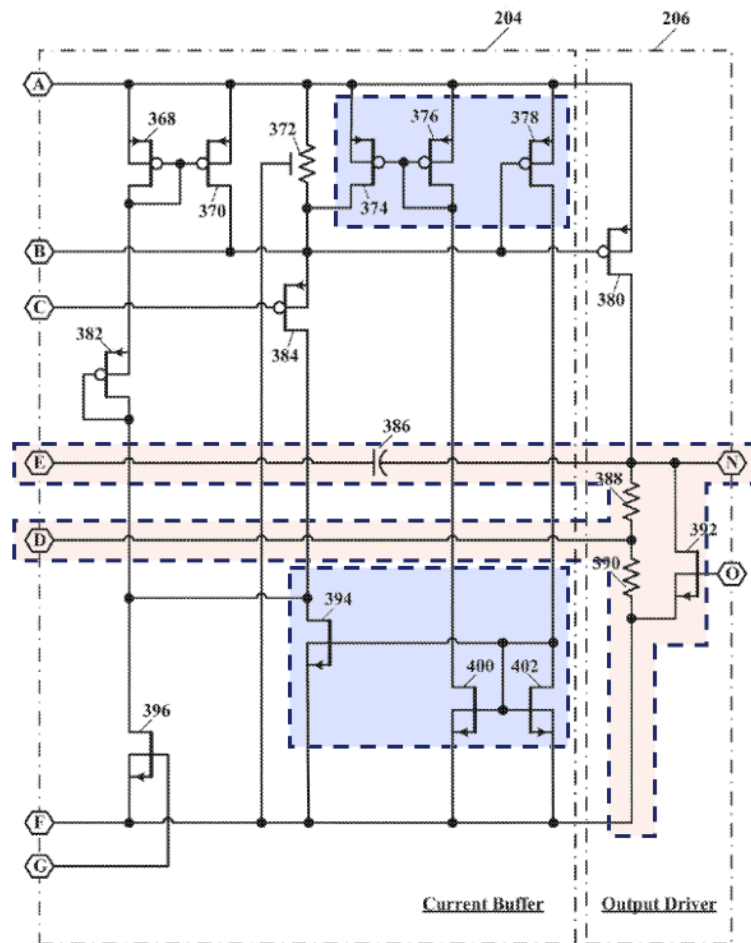
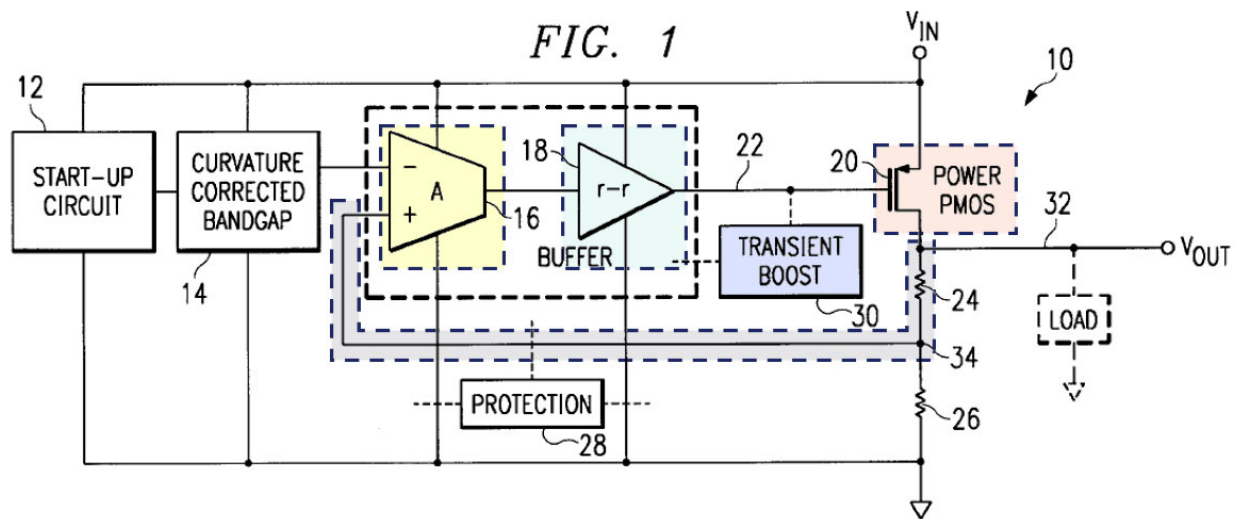


FIGURE 3B

(*Id.*, 5:13-14, Fig. 3B.) Node D, which is coupled to node N, is part of the feedback loop. Thus, I do not believe that a POSITA reading claim 14 in view of the rest of the specification would have been able to make sense of a “feedback voltage from an output voltage node” being provided by the “current feedback circuit.” At most, a POSITA might have tried to make sense of the claim by assuming that the applicant meant to refer to the “feedback loop” recited in limitation 1[g] instead of “the current feedback circuit.”

200. With that understanding of claim 14 in mind, it is my opinion that the Rincon-Mora LDO meets the claim. As shown below, the feedback loop (in gray) provides a feedback voltage—the output voltage of the output driver transistor 20 (red) less the voltage drop across resistor 24—to the error amplifier (yellow):



(EX1013, Fig. 1 (annotated).)

201. I have also been asked to consider an alternative interpretation of claim 14, under which the term “current feedback circuit” does refer to the actual current feedback circuit, and the term “an output voltage node” refers to a node that provides a feedback voltage. It is my opinion that, under this meaning, the Rincon-Mora LDO includes a current feedback circuit that provides a feedback voltage from an output voltage node. The current feedback circuit provides a voltage to transistor 45 at node 44, that node being an “output voltage node” because it responds to changes in the

current of the output power driver 20. I also refer to my opinions under claims 1 and 12 above, as well as to my summary of the Rincon-Mora References.

Claim 15 The voltage regulator according to claim 1, wherein the current buffer driver has a low output impedance.

202. The buffer driver in Rincon-Mora's LDO has low output impedance. As the Rincon-Mora Paper explains, "[t]he idea of the buffer is to isolate the large capacitor associated with the gate of the power PMOS transistor from the large resistance of the output of [the amplifier]'s gain stage." (EX1014, 42.) Thus, the paper states, "the buffer needs low input capacitance and low output impedance" (*id.*), teaching a POSITA to implement Rincon-Mora with a buffer that has those properties. In addition, as I have explained above in my summary of the Rincon-Mora References and my analysis of claim 3 above, Rincon-Mora's current feedback circuit boosts the gm of the buffer driver by increasing its current. A POSITA would have understood that this would decrease output impedance, because of the inverse relationship between current and impedance.

Claim 16 The voltage regulator according to claim 1, further comprising capacitors in the biasing circuit for improving noise immunity thereof.

203. As I have discussed under limitation 1[d], biasing circuits were a basic and ubiquitous electronics component, and Rincon-Mora does not provide a specific design for its own biasing circuit, assuming familiarity with biasing circuits and their

implementation. A POSITA would have recognized that the biasing circuit for the Rincon-Mora LDO could be implemented using conventional and well-understood methods.

204. Those conventional and well-understood methods included using what were known as “decoupling capacitors” or “bypass capacitors” to insulate the bias circuit from noise caused by other circuit components. This is because capacitance is inversely proportional to voltage, given an amount of charge. In the context of electrical noise, the voltage of a disturbance V_{dist} is given by Q_{noise} divided by C_{bypass} , where Q_{noise} is the amount of excess or deficient charge associated with the noise and C_{bypass} is the capacitance of the bypass capacitor. Thus, adding bypass capacitor to a circuit node reduces variations in voltage.

205. These principles were discussed widely in the art, and would have been well-known to a POSITA. For example, a 2007 dissertation by Mikhail Popovich taught that the “power and signal integrity problems in the overall system” caused by noise from one component propagating to another can be solved by “decoupling capacitors” placed at different points in the circuit. (EX1009, 12 & 217.) Wang discloses a bias circuit with “a bypass capacitor, which is coupled to an RF ground” so that it “holds the second terminal at a constant voltage despite fluctuations in the RF signal.” (EX1010, 2:64-3:1.) Wang further explains that in “common battery-powered applications,” the bias voltage is often connected to a power supply by “a

suitable network of decoupling capacitors.” (*Id.*, 4:59-61). As a third example, a datasheet published in January 2009 by Micrel Inc. for an “Ultra High Speed 3A LDO” called MIC59300 explains that recommends using “[s]mall ceramic capacitors from VBIAS-to-ground [to] help reduce high frequency noise from being injected into the control circuitry from the bias rail and constitute good design practice,” noting that “[g]ood bypass techniques typically include one larger capacitor” and “smaller valued capacitors” in parallel with the larger capacitor “to decouple the bias supply.” (EX1011, 10.) Finally, Dr. Rincon-Mora’s dissertation discloses such a use of capacitors in the curvature corrected bandgap circuit, which supplies the reference voltage to the error amplifier of an LDO, to limit “noise bandwidth of the reference circuit” and thus “enhanc[e] noise performance.” (EX1015, 109.)

206. Given how the use of decoupling capacitors was a conventional practice with well-known noise immunity benefits, particularly in a bias circuit that must reliably output a constant voltage, a POSITA would have found it obvious to include them when implementing the Rincon-Mora LDO.

Claim 17 The voltage regulator according to claim 1, wherein the voltage regulator is a USB voltage regulator.

207. A POSITA would have considered a USB voltage regulator to be an obvious application for Rincon-Mora’s LDO. Rincon-Mora explains that its LDO

is suited for “portable, battery powered applications” where “standby and quiescent current flow are major concerns.” (EX1013, 1:18-25; EX1014, 36.) A POSITA would have identified the same concerns in a USB voltage regulator because USBs often required the host device to supply power. This is explained, for example, in Butler, which proposes a “method for conserving power” in a USB capable device that includes the step of providing “a USB voltage regulator.” (EX1012, 1:17-27, 2:29-33.)

Claim 18 The voltage regulator according to claim 1, wherein the current buffer driver has low input impedance and provides a high frequency pole that does not substantially affect the voltage regulator dominant pole.

208. The Rincon-Mora LDO has a dominant pole P_1 given as:

$$P_1 \approx \frac{1}{2\pi C_o R_{o-pass}} \approx \frac{\lambda I_{Load}}{2\pi C_o}$$

where C_o is the output capacitance, R_{o-pass} is the output resistance of the pass device (*i.e.*, output power driver), λ is the channel length modulation parameter, and I_{Load} is the load current. (EX1014, 37.) In addition, the parasitic pole P_3 is given as:

$$P_3 \approx \frac{g_{mNPN}}{2\pi C_{par}} = \frac{I_{bias} + I_{boost}}{2\pi V_t C_{par}} \approx \frac{I_{bias} + kI_{Load}}{2\pi V_t C_{par}}$$

where C_{par} is the parasitic capacitance at the output of buffer (node 22/44 in Figure 3 of Rincon-Mora), $g_{m(npn)}$ is the transconductance of the buffer transistor, I_{bias} is the

bias current, I_{boost} is the boost current, V_t is the thermal voltage, and k is the constant mirror ratio between the output driver and the transistor of the transient boost circuit that mirrors the output driver. (*Id.*, 37-38, Fig. 2; EX1013, Fig. 3 (k is the ratio of transistors 20 and 45).)

209. Thus, the circuit “can be designed such that P_3 increases at a faster rate than the UGF with respect to load-current.” (EX1014, 38.) Because the parasitic pole can be designed to increase at a faster rate a POSITA would have understood that Rincon-Mora’s current buffer driver provides a high frequency pole that does not substantially affect the dominant pole. (EX1013, 4:10-29, 4:41-61.)

210. The patent does not explain what it means for the current buffer driver to have “low input impedance.” But as I have noted under claim 3, I understand Patent Owner to have read the term “current buffer driver input impedance” to mean the input impedance at the point where the operational amplifier connects to the current buffer driver. Applying this same understanding to claim 18, such that “low input impedance” refers to the impedance at the point where the operational amplifier connects to the buffer driver, it is my opinion that a POSITA would have found that Al-Shyouch’s buffer driver “has low input impedance” as claimed.

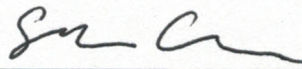
211. The input node of Rincon-Mora’s buffer driver is coupled to the output node of its error amplifier. If implemented as an operational amplifier (one of the readily available and suitable options as discussed above under limitation 1[a]), this

error amplifier would have low output impedance (a property of an op-amp, as a POSITA would have known). In addition, a POSITA would have understood that the “product of the input capacitance of the buffer (C_{buf}) and the output resistance of the gain stage [*i.e.*, the error amplifier] (R_{og}) must be kept low to yield an internal frequency pole” greater than the unity gain frequency (EX1015, 32), because this is consistent with the Rincon-Mora LDO’s design objective of pushing the parasitic pole (P_3) to a frequency well above the unity gain frequency. A POSITA would thus have understood to choose an error amplifier with a relatively low output impedance, *i.e.*, a relatively low impedance at the input node of the buffer driver.

Inter Partes Review of U.S. Patent No. 9,471,074

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code.

Dated: 3/7/24



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Curriculum Vitae

EDUCATION

University of California, Berkeley 2002 – 2006

- PhD in Electrical Engineering and Computer Science
- Dissertation: “High-Speed, Low-Power A/D Converter for a Low-Cost UWB Sub-sampling Radio”
- Advisor: Robert W. Brodersen

University of California, Berkeley 2000 – 2002

- Master of Science in Electrical Engineering and Computer Science
- Thesis: “Ultra Wideband Baseband Design and Implementation”

National Taiwan University 1994 – 1998

- Bachelor of Science in Electrical Engineering
- Top 1 student for upper division

ACADEMIC EXPERIENCE

- Professor, Department of Electrical Computer Engineering, University of Southern California, 2021 – Present.
- Associate Professor, Department of Electrical Engineering, University of Southern California, 2017 – 2021.
- Colleen and Roberto Padovani Early Career Chair, USC, 2014 – 2021
- Assistant Professor, Department of Electrical Engineering, University of Southern California, 2011 – 2017.
- Graduate Student Researcher, Berkeley Wireless Research Center, Berkeley, CA, 2001 – 2006.

WORK EXPERIENCE

- Analog Senior Technical Staff, Atheros Communications, Santa Clara, CA, 2006–2010.
-Designed RF, analog mixed-signal circuits for various wireless products

HONORS and AWARDS

- IEEE Fellow (Class of 2024 via Solid-State Circuit Society)
- ISSCC 2022 Jack Kilby Award (co-recipient)

- RFIC 2022 Best Student Paper Award – First Place (co-recipient)
- IEEE Solid-State Circuit Society (SSCS) Distinguished Lecturer 2021-2023.
- Qualcomm Faculty Award, 2019.
- DARPA Young Faculty Award (YFA), 2014.
- NSF Faculty Early Career Development (CAREER) Award, 2014.
- Analog Devices Outstanding Student Award, 2006
- UC Regents Fellowship, UC Berkeley, 2000
- Lin's Foundation Award for Top 1 engineering college student over the academic year, 1996-1997
- Presidential Awards, National Taiwan University, 1996-1998
- Member of National Mathematics Team of Taiwan, awarded with Honourable Mention in Asian Pacific Mathematics Olympiad, 1994.

KEY TECHNICAL CONTRIBUTIONS

Analog Mixed-Signal and RF circuit architectures/techniques for data converters, clock generation and PA.

- Asynchronous SAR ADC (since 2006)
- Embedded TDC scheme for Digital PLL (since 2010)
- Nonuniform sampling (NUS) ADCs and NU DSP (since 2012)
- Direct spur/pulling cancellation for Digital PLL (since 2014)
- Dual-rate hybrid DAC (since 2014)
- Sub-harmonic switching (SHS) PA (since 2018)
- Time-Approximation Filter (TAF) for Transceiver (since 2019)
- Two-Point DTC Calibration scheme for Multiplying DLL (since 2021)
- Delay-tracking pipelined SAR TDC (since 2022)

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9. J. Liu, M. Hassanpourghadi, and **M. S.-W. Chen**, “A 10GS/s 8b 25fJ/c-s $2850\mu\text{m}^2$ Two-Step Time-domain ADC Using Delay-Tracking Pipelined-SAR TDC with 500fs Time Step in 14nm CMOS Technology“, *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2022.
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29. S. Su and **M. S-W Chen**, "A 16-bit 12GS/s Single/Dual-Rate DAC with Successive Bandpass Delta-Sigma Modulator Achieving <-67dBc IM3 within DC to 6GHz Tunable Passbands," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2018.

30. C.R. Ho, **M. S-W Chen**, "A digital frequency synthesizer with dither-assisted pulling mitigation for simultaneous DCO and reference path coupling," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2018.
31. C.R. Ho, **M. S-W Chen**, "A fractional-N digital PLL with background dither noise cancellation loop achieving $<-62.5\text{dBc}$ worst-case near-carrier fractional spur in 65nm CMOS," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2018.
32. R. Rasul, P. Teimouri, and **M. S-W Chen**, "A Time Multiplexed Network Architecture for Large-Scale Neuromorphic Computing," *IEEE MWSCAS*, August 2017.
33. C.R. Ho, **M. S-W Chen**, "Interference-Induced DCO Spur Mitigation for Digital Phase Locked Loop in 65-nm CMOS," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, Sep. 2016.
34. J.W. Nam, M. Hassanpourghadi, A. Zhang, **M.S-W Chen**, "A 12-bit 1.6 GS/s Interleaved SAR ADC with Dual Reference Shifting and Interpolation Achieving 17.8 fJ/conv-step in 65nm CMOS," *IEEE Symposia on VLSI Technology and Circuits (VLSIC)*, June 2016.
35. C.R. Ho, **M. S-W Chen**, "A Digital PLL with Feedforward Multi-Tone Spur Cancellation Loop Achieving $<-73\text{dBc}$ Fractional Spur and $<-110\text{dBc}$ Reference Spur in 65nm CMOS," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2016.
36. S. Su, **M. S-W. Chen**, "A 12b 2GS/s Dual-Rate Hybrid DAC with Pulsed Timing-Error Pre-Distortion and In-Band Noise Cancellation Achieving $>74\text{dBc}$ SFDR up to 1GHz in 65nm CMOS," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2016.
37. T.F. Wu, C.R. Ho, **M. S.-W. Chen**, "A Flash-Based Non-Uniform Sampling ADC Enabling Digital Anti-Aliasing Filter in 65nm CMOS," *IEEE Custom Integrated Circuits Conference (CICC)*, Sep 2015.
38. S. Su, T. Tsai, P. Sharma, **M. S.-W. Chen**, "A 12-bit Hybrid DAC with 8GS/s Unrolled Pipeline Delta-Sigma Modulator achieving $>75\text{dB}$ SFDR over 500MHz in 65nm CMOS," *IEEE Symposia on VLSI Technology and Circuits (VLSIC)*, June 2014.
39. C.R. Ho, **M. S.-W. Chen**, "A Fractional-N DPLL with Adaptive Spur Cancellation and Calibration-Free Injection-Locked TDC in 65nm CMOS," to be presented at *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June, 2014.
40. J.W. Nam, D. Chiong, and **M. S.W. Chen**, "A 95-MS/s 11-bit 1.36-mW Asynchronous SAR ADC with Embedded Passive Gain in 65nm CMOS," *IEEE Custom Integrated Circuits Conference (CICC)*, Sep. 2013
41. P.K. Sharma, and **M. S.W. Chen**, "A 6b 800MS/s 3.62mW Nyquist AC-coupled VCO Based ADC in 65nm CMOS ," *IEEE Custom Integrated Circuits Conference (CICC)*, Sep. 2013
42. **M. S.W. Chen**, "Trend of High-Speed SAR ADC towards RF Sampling," *10th International Conference on Sampling Theory & Applications (SampTA)* (Invited), July. 2013.
43. D. Hand, and **M. S.W. Chen**, "A Non-Uniform Sampling ADC Architecture with Embedded Alias-Free Asynchronous Filter," *Global Telecommunications Conference (GLOBECOM)*, Dec. 2012.

44. **M. S.W. Chen**, "Overhead Minimization Techniques for Digital Phase-Locked Loop Frequency Synthesizer, " IEEE MWSCAS (Invited Session), Aug. 2012.
45. **M.S.W. Chen**, **D. Su**, S. Mehta, "A Calibration-Free 800MHz Fractional-N Digital PLL with Embedded TDC," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2010.
46. Nathawad, L.; Zargari, M.; Samavati, H.; Mehta, S.; Kheirkhahi, A.; Chen, P.; Gong, K.; Vakili-Amini, B.; Hwang, J.; **Chen, M.S.W.**; Terrovitis, M.; Kaczynski, B.; Limotyrakis, S.; Mack, M.; Gan, H.; Lee, M.; Abdollahi-Alibeik, S.; Baytekin, B.; Onodera, K.; Mendis, S.; Chang, A.; Jen, S.; Su, D.; **Wooley, B.**, "A Dual-Band CMOS MIMO Radio SoC for IEEE 802.11n Wireless LAN," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2008.
47. A. Fort, **M. S.-W. Chen**, R.W. Brodersen, C. Desset, P. Wambacq, **L. Van Biesen**, "Impact of Sampling Jitter on Mostly-Digital Architectures for UWB Bio-Medical Applications," *IEEE International Conference on Communications (ICC)*, June 2007.
48. A. Fort, **M. S.-W. Chen**, C. Desset, P. Wambacq, **L. Van Biesen**, "Clock offset tracking for subsampling UWB architectures in a body area network," *IEEE International Conference on Ultra-Wideband (ICUWB)*, Sep. 2007.
49. **M. S.-W. Chen** and R. W. Brodersen, "Digital Complex Signal Processing Techniques for Impulse Radio," *Global Telecommunications Conference (GLOBECOM)*, Nov. 2006.
50. **M. S.-W. Chen** and R. W. Brodersen, "Implementation Considerations for a Sub-sampling Impulse Radio," *IEEE International Conference on Ultra-Wideband (ICUWB)*, Sep. 2006.
51. **M. S.-W. Chen** and R. W. Brodersen, "A 6b 600MS/s 5.3mW Asynchronous ADC in 0.13 μ m CMOS," *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2006.
52. D. Cabric, **M. S.-W. Chen**, D. Sobel, J. Yang, and R. Brodersen, "Future Wireless Systems: UWB, 60 GHz, and Cognitive Radios," (Invited paper) at *Custom Integrated Circuits Conference (CICC)*, Sep. 2005
53. **M. S.-W. Chen**, R. W. Brodersen, "The Impact of a Wideband Channel on UWB System Design," *Military Communication Conference (MILCOM)*, Nov. 2004.
54. **M. S.-W. Chen**, R. W. Brodersen, "A Subsampling UWB Radio Architecture by Analytic Signaling," *International Conference on Acoustics, Speech, and Signal Processing (ICASSP)*, May 2004.
55. I. O'Donnell, **M. S.-W. Chen**, S. Wang, R. W. Brodersen, "An Integrated, Low-Power, Ultra-Wideband Transceiver Architecture for Low-Rate, Indoor Wireless Systems," *IEEE CAS Workshop on Wireless Communications and Networking*, Sep. 2002.

Journals

1. W. Song, M. Rao, Y. Li, C. Li, Y. Zhuo, F. Cai, M. Wu, W. Yin, Z. Li, Q. Wei, S. Lee, H. Zhu, L. Gong, M. Barnell, Q. Wu, P. Beerel, **M. S.-W. Chen**, N. Ge, M. Hu, Q. Xia, J. Yang, "Programming memristor arrays with arbitrarily high precision for analog computing," *Science*, 2024. (in press)

2. Q. Zhang, H.-C. Cheng, S. Su, and **M. S.-W. Chen**, "Fractional-N Digital MDLL with Injection-Error Scrambling and Calibration," *IEEE J. Solid-State Circuits*, 2023. (in press)
3. C. Yang, S. Su, and **M. S.-W. Chen**, "Millimeter-Wave Receiver with Non-Uniform Time-Approximation Filter," *IEEE J. Solid-State Circuits*, May 2023.
4. J. Liu, M. Hassanpourghadi, and M. S.-W. Chen, "A 10-GS/s 8-bit 2850- μm^2 Two-Step Time-Domain ADC With Speed and Efficiency Enhanced by the Delay-Tracking Pipelined-SAR TDC," *IEEE J. Solid-State Circuits*, 2022.
5. S. Su and **M. S.-W. Chen**, "SAW-Less Direct RF Transmitter with Multi-Mode Noise Shaping and Tri-Level Time-Approximation Filter," *IEEE J. Solid-State Circuits*, Mar. 2022.
6. Q. Zhang, S. Su, C.-R. Ho, and **M. S.-W. Chen**, "A Fractional-N Digital MDLL With Background Two-Point DTC Calibration," (Invited) *IEEE J. Solid-State Circuits* (JSSC), Jan. 2022.
7. M. Hassanpourghadi, R. A. Rasul, and **M. S. W. Chen**, "A Module-Linking Graph Assisted Hybrid Optimization Framework for Custom Analog and Mixed-Signal Circuit Parameter Synthesis" *ACM Transactions on Design Automation of Electronic Systems*, June 2021.
8. X. Yan, J. Ma, T. Wu, A. Zhang, J. -B. Wu, M. Chin, Z. Zhang, M. Dubey, W. Wu, **M. S.-W. Chen**, J. Guo, H. Wang "Reconfigurable Stochastic Neurons Based on Tin Oxide/MoS₂ Hetero-memristors for Simulated Annealing and the Boltzmann Machine" *Nature Communications*, 12, Article number: 5710 (2021)
9. S. Su, **M. S.-W. Chen**, "A Time-approximation Filter for Direct RF Transmitter," *IEEE J. Solid-State Circuits* (JSSC) 2021.
10. J.W. Nam, **M. S.-W. Chen**, "A 12.8-Gbaud ADC-based Wireline Receiver with Embedded IIR Equalizer," (Invited) *IEEE J. Solid-State Circuits* (JSSC), Mar. 2020.
11. A. Zhang, **M. S.-W. Chen**, "A Watt-Level Phase-Interleaved Multi-Subharmonic Switching Digital Power Amplifier," (Invited) *IEEE J. Solid-State Circuits* (JSSC) Nov., 2019.
12. A. Zhang, **M. S.-W. Chen**, "A Subharmonic Switching Digital Power Amplifier for Power Back-Off Efficiency Enhancement," (Invited) *IEEE J. Solid-State Circuits* (JSSC) Feb., 2019.
13. T.F. Wu, **M. S.-W. Chen**, "A VCO-Based Nonuniform Sampling ADC with Phase-Domain Level Crossing," (Invited) *IEEE J. Solid-State Circuits* (JSSC) Mar., 2019.
14. S. Su, **M. S.-W. Chen**, "A 16-bit 12GS/s Single/Dual-Rate DAC with a Successive Bandpass Delta-Sigma Modulator Achieving <-67dBc IM3 within DC to 6GHz Tunable Passbands," (Invited) *IEEE J. Solid-State Circuits* (JSSC) Dec., 2018.
15. T.F. Wu, **M. S.-W. Chen**, "A Subranging-Based Nonuniform Sampling ADC With Sampling Event Filtering," *IEEE Solid-State Circuits Letters* (SSC-L) April, 2018.
16. J.W. Nam, M. Hassanpourghadi, A. Zhang, **M.S-W Chen**, "A 12-bit 1.6/3.2/6.4 GS/s 4 b/cycle Time-interleaved SAR ADC with Dual Reference Shifting and Interpolation," *IEEE J. Solid-State Circuits* (JSSC), June, 2018.

17. T.F. Wu, C.R. Ho, **M. S.-W. Chen**, "A Flash-Based Non-Uniform Sampling ADC With Hybrid Quantization Enabling Digital Anti-Aliasing Filter," *IEEE J. Solid-State Circuits* (JSSC) Sep., 2017.
18. M. Hassanpourghadi, P.K. Sharma, and **M. S.-W. Chen**, "A 6-bit Nyquist AC-coupled VCO Based ADC at 800MS/s," *IEEE Transactions on Circuits and Systems* (TCAS-I) 2017.
19. C.R. Ho, **M. S.-W. Chen**, "A Digital PLL with Feedforward Multi-Tone Spur Cancellation Loop Achieving $<-73\text{dBc}$ Fractional Spur and $<-110\text{dBc}$ Reference Spur in 65nm CMOS," (Invited) accepted for *IEEE J. Solid-State Circuits* (JSSC) Dec., 2016.
20. S. Su, **M. S.-W. Chen**, "A 12b 2GS/s Dual-Rate Hybrid DAC with Pulsed Timing-Error Pre-Distortion and In-Band Noise Cancellation Achieving $>74\text{dBc}$ SFDR up to 1GHz in 65nm CMOS," (Invited) accepted for *IEEE J. Solid-State Circuits* (JSSC) Dec., 2016.
21. J.W. Nam, **M. S.-W. Chen**, "An Embedded Passive Gain Technique for Asynchronous SAR ADC Achieving >10 ENOB, 1.36 mW at 95MS/s in 65nm CMOS," accepted by *IEEE Transactions on Circuits and Systems* (TCAS-I) 2016
22. T.F. Wu, S. Dey, **M. S.-W. Chen**, "A Non-Uniform Sampling ADC Architecture with Reconfigurable Digital Anti-aliasing Filter," accepted by *IEEE Transactions on Circuits and Systems* (TCAS-I) 2016
23. C.R. Ho, **M. S.-W. Chen**, "A Fractional-N DPLL with Calibration-free Multi-phase Injection-locked TDC and Adaptive Single-tone Spur Cancellation Scheme," accepted by *IEEE Transactions on Circuits and Systems* (TCAS-I) 2016
24. S. Su, T. Tsai, P. Sharma, **M. S.W. Chen**, "A 12-bit 1GS/s Dual-Rate Hybrid DAC with an 8GS/s Unrolled Pipeline Delta-Sigma Modulator Achieving $>75\text{dB}$ SFDR over the Nyquist Band," (Invited) *IEEE J. Solid-State Circuits*, April, 2015.
25. Y. Cao, J. Velamala, K. Sutaria, **M. S.W. Chen**, J. Ahlbin, I. Esqueda, M. Bajura, M. Fritze, "Cross-Layer Modeling and Simulation of Circuit Reliability", *IEEE Transactions on CAD of Integrated Circuits and Systems*, Jan. 2014.
26. **M.S.W. Chen**, D. Su, S. Mehta, "A Calibration-Free 800MHz Fractional-N Digital PLL with Embedded TDC," (Invited) *IEEE Journal of Solid-State Circuits*, Dec. 2010.
27. Zargari, M.; Nathawad, L.Y.; Samavati, H.; Mehta, S.S.; Kheirkhahi, A.; Chen, P.; Gong, K.; Vakili-Amini, B.; Hwang, J.A.; **Chen, S.-W.M.**; Terrovitis, M.; Kaczynski, B.J.; Limotyrakis, S.; Mack, M.P.; Gan, H.; MeeLan Lee; Chang, R.T.; Dogan, H.; Abdollahi-Alibeik, S.; Baytekin, B.; Onodera, K.; Mendis, S.; Chang, A.; Rajavi, Y.; Jen, S.H.-M.; Su, D.K.; Wooley, B.A., "A Dual-Band CMOS MIMO Radio SoC for IEEE 802.11n Wireless LAN," *IEEE J. Solid-State Circuits*, Dec. 2008.
28. **M.S.W. Chen**, R. W. Brodersen, "A Subsampling Radio Architecture for Ultrawideband Communications," *IEEE Transactions on Signal Processing*, Oct. 2007.
29. **M.S.W. Chen**, R. W. Brodersen, "A 6-bit 600-MS/s 5.3-mW Asynchronous ADC in 0.13-um CMOS," *IEEE J. Solid-State Circuits*, Dec. 2006.
30. **M.S.W. Chen**, R. W. Brodersen, "A Subsampling UWB Impulse Radio Architecture Utilizing Analytic Signaling," (Invited Paper) *IEICE Trans. on Electronics*, June 2005.

31. D. Cabric, **M. S.-W. Chen**, D. Sobel, S. Wang, J. Yang, and R. W. Brodersen, "Novel Radio Architectures for UWB, 60GHz, and Cognitive Wireless Systems," *EURASIP J. on Wireless Communcations and Networking*, 2006.

Magazine

1. **M. S.-W. Chen**, "Trend and New Opportunities in Digital PLL Design", (Invited) *IEEE Solid State Circuit Magazine*, 2020 winter issue.
2. C.R. Ho, **M. S.-W. Chen**, "Clock Generation in the future with Digital Signal Processing Technique for Mitigating Spur and Interference," *IEEE Microwave Magazine* 2019.
3. Sankaran, S.G.; Zargari, M.; Nathawad, L.Y.; Samavati, H.; Mehta, S.S.; Kheirkhahi, A.; Chen, P.; Ke Gong; Vakili-Amini, B.; Hwang, J.; **Chen, S.-W.M.**; Terrovitis, M.; Kaczynski, B.J.; Limotyakis, S.; Mack, M.P.; Gan, H.; Lee, M.; Chang, R.T.; Dogan, H.; Abdollahi-Alibeik, S.; Baytekin, B.; Onodera, K.; Mendis, S.; Chang, A.; Rajavi, Y.; Jen, S.H.-M.; Su, D.K.; Wooley, B., "Design and implementation of a CMOS 802.11n soc –[integrated circuits for communications]," *Communications Magazine*, April 2009.
4. D. Cabric, I. O'Donnell, **M. S.-W. Chen**, and R.W. Brodersen, "Spectrum Sharing Radios," (Invited) *IEEE Circuits and Systems Magazine*, 2006.

Book Chapter

1. C.R. Ho, **M. S.-W. Chen**, "Fractional-N spur reduction techniques for DPLL," *Phase-Locked Frequency Generation and Clocking: Architectures and Circuits for Modern Wireless and Wireline Systems*, IET 2019 (under preparation).
2. **M. S.-W. Chen**, "Challenges and Emerging Trend of DSP Enabled Frequency Synthesizer," *Digitally-Assisted Analog and Analog-Assisted Digital IC Design*. Chapter4, 2015, Cambridge University Press.
3. **M. S.-W. Chen**, "Energy-Efficient ADC Topology Enabled with Asynchronous Techniques," *Circuits for Nanoscale: Communications, Imaging, and Sensing*. Chapter14, Sep. 2008.

Patent

1. **M.S.W. Chen**, C.R. Ho, "Adaptive spur cancellation techniques and multi-phase injection locked TDC for digital phase locked loop circuit," US patent #9941891, 2018.
2. **M. S.W. Chen**, "Non-uniform Sampling Analog to Digital Converter (ADC) Architecture with Digital Reconfigurable Anti-Aliasing Filter," filed for provisional patent application, No. 61/911,261, Dec., 2013.
3. **M. S.W. Chen**, D. Su, "Fractional and Integer PLL Architectures," US patent #8289086, 2012.

INVITED TALKS/TUTORIALS/WORKSHOPS

1. ITRI, Taiwan, "New Opportunities in Mixed-Signal ICs", June, 2011.

2. UMC, Taiwan, "New Opportunities in Mixed-Signal ICs", June, 2011.
3. HRL Laboratories, LLC: "Enhancing A-to-D Conversion Efficiency". July 2nd, 2012
4. "Analog-to-Digital Interface: A Time Approach" 2013 CMOS Emerging Technologies Research Symposium, Whistler, July 2013.
5. "Path towards High-Speed High-Resolution Data Converters with Diminishing Cost", Sep. 2013, Broadcom.
6. "Analog-Digital Interface Research, really?" Sep. 2013, Qualcomm-Atheros.
7. "Re-shape Future Mixed-Signal IC Design" Oct. 2013. Qualcomm.
8. "Path towards High-Speed High-Resolution Data Converters with Diminishing Cost", Nov. 2013, UT Dallas.
9. "Path towards High-Speed High-Resolution Data Converters with Diminishing Cost", Nov. 2013, Texas Instrument.
10. "Power efficient ADC Topologies towards RF Sampling" 2014 RFIC Tutorial.
11. "Path Towards Direct RF Synthesis: A Hybrid Digital-to-Analog Converter Architecture" 2014 IEEE MWSCAS Conference, Distinguished Speaker Series.
12. "Asynchronous SAR ADC: Past, Present and Beyond" 2014 IEEE MWSCAS Conference Tutorial
13. "Exploring Limits of Mixed-Signal ICs" Sep. 2014, MaxLinear Corp.
14. "Rethinking Analog-Digital Interface Circuit Architectures" Oct. 2014, IC Seminar, Columbia University, NY.
15. "Rethinking Analog-Digital Interface Circuit Architectures" Mar. 2015, IC Seminar, UC Berkeley, CA.
16. "Rethinking Analog-Digital Interface Circuit Architectures" Dec. 2015, IC Seminar, National Taiwan University(NTU)/IEEE Chapter, Taipei, Taiwan.
17. "Rethinking Analog-Digital Interface Circuit Architectures" Feb. 2016, IC Seminar, UT Austin, Texas.
18. "Asynchronous SAR ADC: Past, Present and Beyond", Feb. 2016, EE department Colloquium, UT Austin/IEEE Chapter.
19. "Rethinking Analog-Digital Interface Circuit Architectures" Feb. 2016, IC Seminar, University of Michigan, Ann Arbor.
20. "Rethinking Analog-Digital Boundary from Circuit to System Level towards Reconfigurability of Everything" Mar. 2016, SystemX Seminar, Stanford
21. "Rethinking Analog-Digital Interface Circuit Architectures" April. 2016, EE department Colloquium. Carnegie Mellon University (CMU).
22. "Rethinking Analog-Digital Interface Circuit Architectures" April. 2016, IC Seminar, University of California, Los Angeles (UCLA).
23. "IC Research overview," TSMC, 2017
24. "IC Research overview," Intel Lab, 2017
25. "IC Research overview," InPhi, 2017
26. "Advancing Low-Power High-Speed Analog-to-Digital Converters: An Asynchronous Design Approach", VLSI DAT tutorial, 2017
27. "Generic spur cancellation for digital PLL," Qualcomm 2017
28. "Evolutions of SAR ADC: from High Resolution to High Speed Regime," IEEE CICC 2018 tutorial.
29. "Emerging Opportunities in Analog Mixed-Signal Circuit Design Automation," ACM/IEEE ICCAD 2018 workshop.

30. "Analog-to-Digital Converter Architecture Opportunities in Emerging Wireless Systems," RFIC 2018 workshop
31. "How can hardware designers reclaim the spotlight?" moderator/co-organizer of ISSCC 2019 evening panel.
32. "Fundamentals of Analog-to-digital conversion," 2-day tutorial in Shanghai, China 2019.
33. "Digital Fractional-N Phase Locked Loop Design," tutorial, ISSCC Feb 2020
34. "Digital Fractional-N Phase Locked Loop Design," ISSCCedu Feb 2020
35. "Low Spur PLL architectures," MEAD tutorial in EPFL, 2021 (to appear)
36. "Low Spur PLL architectures and techniques," IEEE CICC 2020
37. "New Opportunities in Nonuniform Sampling," IEEE SSCS Webinar Oct 2020.
38. "High-Performance Digital-to-Analog Converter Design: A Path towards Digital Transmitter," ISESD Keynote June 2021
39. "ADC Evolution via Architectural Rethinking: from Asynchronous SAR to Non-uniform Sampling ADC," IEEE SSCS Tainan Chapter, Oct 2021
40. "High-Performance Digital-to-Analog Converter Design: A Path towards Digital Transmitter," IEEE SSCS Atlanta Chapter, Nov. 2021
41. "Asynchronous SAR ADC: Past, Present and Beyond," IEEE Southern Alberta Chapter, Nov. 2021
42. "Non-Uniform Sampling Data Converters: A Journey to Uncharted Circuits and Systems" IEEE VLSI-DAT April 2022
43. "Asynchronous SAR ADC: Past, Present and Beyond," IEEE Swiss Chapter, May 2022
44. "New Opportunities in Nonuniform Sampling," IEEE Penang Chapter, July 2022
45. "Trend in Digital PLL Design and New Opportunities in Spur Cancellation," IEEE Southern Alberta Chapter, Sep. 2022
46. "High-Performance Digital-to-Analog Converter Design: A Path towards Digital Transmitter," IEEE Egypt Chapter Nov. 2022
47. "New Opportunities in Nonuniform Sampling," IEEE Taipei Chapter, Dec. 2022
48. "Trend in Digital PLL Design and New Opportunities in Spur Cancellation," IEEE Tainan Chapter, Dec. 2022

PROFESSIONAL SERVICES

Review Panel:

1. IEEE SSCS James D. Meindl Innovators Award
2. NSF Panelist
3. Samsung Research

Journal article review:

1. IEEE Journal of Solid-State Circuits
2. IEEE Transactions on Signal Processing
3. IEEE Transactions on Communications
4. IEEE Transactions on Circuits and Systems I
5. IEEE Transactions on Circuits and Systems II
6. IEEE Transactions on Vehicular Technology

7. IEEE Communications Letters
8. Journal of VLSI Signal Processing Systems

USC Department Services:

1. Munishian Series Committee
2. EFC
3. EE Festival reviewer

Conference TPC:

IEEE European Conference on Solid-State Circuit (ESSCIRC) (2022- present)
IEEE International Solid State Circuits Conference (ISSCC) (2018 - 2023)
IEEE Symposium on VLSI Circuits (VLSIC) (2017 - 2020)
IEEE Custom Integrated Circuits Conference (CICC) (2015 - 2019)
IEEE GlobalSIP (2014)

Organized/Participated Panel/Forum/Workshops for SSCS:

1. Forum: “Emerging Design Techniques for Data Converters” served as organizer at CICC 2017
2. Panel: “What can/should Circuit Designers do to Ride on the Wave of Machine Learning?” served as co-organizer and moderator at CICC 2018
3. Panel: “How can hardware designers reclaim the spotlight?” served as co-organizer and moderator at ISSCC 2019
4. Panel: “Favorite circuit design and testing mistakes of starting engineers?” served as co-organizer at ISSCC 2021
5. VLSI Symposia Mentoring Event June 2021
6. Panel: “How to choose career path, academia, industry, startups?” served as panelist at CICC 2022
7. Panel: “Open Source Systems, Circuits, and Design: Is It the Future?” served as panelist at CICC 2022
8. Panel: “AI/ML-based wireless system design and operation - hope or hype?”, served as Panelist at IMS/RFIC 2023

Associate Editor:

SSC-L, TCAS-II

Guest Editor:

JSSC

CURRENT, PRIOR, AND PENDING RESEARCH GRANTS**Current Research Grants**

Proposal Title: SpecEES: Switched-Capacitor Radiofrequency Signal Processing for Spectrally-Agile Low-Energy Wireless Transceivers
 Source of Support: NSF: ECCS-1824442
 Project Location: USC PI: Hossein Hashemi, Co-PI: Mike Chen
 Total Award Amount: \$675,000 (Chen's share: \$313,991)
 Starting Date: 09/01/2018 Ending Date: 08/31/2023

Proposal Title: Bio-inspired hybrid computing platform for micro-unmanned vehicles
 Source of Support: IARPA: 2021-21090200005
 Project Location: USC PI: Wei Wu, Co-PIs: Mike Chen, Quan Nguyen
 Total Award Amount: \$3,000,000 (Chen's share: \$1,100,000)
 Starting Date: 09/27/2021 Ending Date: 10/26/2023

Proposal Title: High-Speed Multi-GS/s Time-based ADC
 Source of Support: MediaTek Inc.
 Project Location: USC PI: Mike Chen
 Total Award Amount: \$160,000
 Starting Date: 01/01/2022 Ending Date: 01/01/2024

Proposal Title: Center for Ubiquitous Connectivity (CUbiC)
 Source of Support: Columbia University (Prime: SRC): 2023-JU-3132
 Project Location: USC PI: Mike Chen
 Total Award Amount: \$1,250,000
 Starting Date: 01/01/2023 Ending Date: 12/31/2027

Proposal Title: High-Speed DAC with High Output Power and Linearity
 Source of Support: University of Texas at Dallas (Prime: SRC): 2023-AM-3160
 Project Location: USC PI: Mike Chen
 Total Award Amount: \$270,000
 Starting Date: 01/01/2023 Ending Date: 12/31/2025

Proposal Title: Machine-Learning Based Analog Mixed-signal Design Tool
 Source of Support: University of Texas at Dallas (Prime: SRC): 2023-AM-3160
 Project Location: USC PI: Mike Chen, Co-PIs: Sandeep Gupta, Anthony Levi
 Total Award Amount: \$285,000 (Chen's share: \$259,568)
 Starting Date: 01/01/2023 Ending Date: 12/31/2025

Proposal Title: Design Automation of Low Phase Noise PLL
 Source of Support: University of Texas at Dallas (Prime: SRC): 2023-AM-3160

Project Location: USC PI: Mike Chen, Co-PIs: Sandeep Gupta, Anthony Levi
Total Award Amount: \$270,000 (Chen's share: \$244,568)
Starting Date: 01/01/2023 Ending Date: 12/31/2025

Prior Research Grants

Proposal Title: Techniques Estimating Reliability in COTS ICs (Phase 1)
Source of Support: DARPA: HR0011-11-C-0067 CLIN0001
Project Location: USC PI: Michael Fritze, Co-PI: Mike Chen
Total Award Amount: \$2,428,225 (Chen's share: \$299,153)
Starting Date: 07/21/2011 Ending Date: 03/07/2013

Proposal Title: Techniques Estimating Reliability in COTS ICs (Phase 2)
Source of Support: DARPA: HR0011-11-C-0067 CLIN0002
Project Location: USC PI: Michael Fritze, Co-PI: Mike Chen
Total Award Amount: \$1,787,093 (Chen's share: \$47,783)
Starting Date: 02/20/2013 Ending Date: 09/20/2014

Proposal Title: Silicon-Based Monolithic Digital RF Memory
Source of Support: ONR: N00014-11-1-0819
Project Location: USC PI: Hossein Hashemi, Co-PI: Mike Chen
Total Award Amount: \$1,200,000 (Chen's share: \$600,000)
Starting Date: 08/01/2011 Ending Date: 09/30/2015

Proposal Title: Multi-Tier Reconfigurable Transceivers for Hand-Portable Radio and
Micro Base Stations
Source of Support: DARPA: HR0011-12-C-0094
Project Location: USC PI: Hossein Hashemi, Co-PI: Mike Chen
Total Award Amount: \$3,257,252 (Chen's share: \$400,000)
Starting Date: 08/20/2012 Ending Date: 07/15/2017

Proposal Title: Computational Leverage Against Surveillance Systems (CLASS)
Source of Support: Itt Exelis (Prime: DARPA): 473685J
Project Location: USC PI: Mike Chen
Total Award Amount: \$287,125
Starting Date: 06/12/2013 Ending Date: 12/22/2014

Proposal Title: Design of Integrated Circuit for Intravascular Radial Arrays
Source of Support: Texas Instruments Inc.
Project Location: PI: K. Kirk Shung, Co-PI: Mike Chen
Total Award Amount: \$150,000 (Chen's share: \$29,332)
Starting Date: 02/01/2014 Ending Date: 01/31/2015

Proposal Title: Dual-Channel UWB Impulse-Based Interconnect Towards Large-Scale Plastic Neural Network
Source of Support: DARPA YFA (SPANAVWAR): N66001-14-1-4049
Project Location: USC PI: Mike Chen
Total Award Amount: \$500,000
Starting Date: 09/04/2014 Ending Date: 09/03/2017

Proposal Title: Computational Leverage Against Surveillance Systems (CLASS) Phase 2
Source of Support: NexGen (Prime: DARPA): 004897-00001
Project Location: USC PI: Mike Chen
Total Award Amount: \$450,000
Starting Date: 10/01/2014 Ending Date: 03/31/2016

Proposal Title: R2 Transceiver Integration
Source of Support: Google: R2-USC-01
Project Location: USC PI: Mike Chen
Total Award Amount: \$800,000
Starting Date: 04/23/2015 Ending Date: 03/31/2016

Proposal Title: R2 2.0 Transceiver Integration - 2016 (Statement of Work #R2-USC-02)
Source of Support: Google: 349783
Project Location: USC PI: Mike Chen
Total Award Amount: \$600,000
Starting Date: 04/01/2016 Ending Date: 12/31/2016

Proposal Title: Wideband High-Dynamic Arbitrary Signal Generator for Electronic Warfare Integrated Systems Research
Source of Support: ONR (DURIP): N00014-15-1-2817
Project Location: USC PI: Hossein Hashemi, Co-PI: Mike Chen
Total Award Amount: \$189,500
Starting Date: 09/29/2015 Ending Date: 09/27/2017

Proposal Title: Calibration and Characterization of High-Speed Data Converter and Clock Generator
Source of Support: ONR: N00014-15-1-2864
Project Location: USC PI: Hossein Hashemi, Co-PI: Mike Chen
Total Award Amount: \$150,000 (Chen's share: \$100,383)
Starting Date: 09/30/2015 Ending Date: 06/30/2016

Proposal Title: Support for April 2017 Connectivity CDF

Source of Support: Airbus: SWLA00034
Project Location: USC PI: Mike Chen
Total Award Amount: \$20,000
Starting Date: 04/26/2017 Ending Date: 05/31/2017

Proposal Title: CAREER: Asynchronous Analog-to-Digital Converters with Non-Uniform Discrete-Time Signal Processing
Source of Support: NSF: ECCS-1351956
Project Location: USC PI: Mike Chen
Total Award Amount: \$400,000
Starting Date: 02/15/2014 Ending Date: 01/31/2020

Proposal Title: EARS: Enabling Opportunistic Environmental Monitoring with Non-Uniform Sampling and Processing Circuits
Source of Support: NSF: ECCS-1643004
Project Location: USC PI: Mike Chen, Co-PIs: Mahta Moghaddam, Keith Chugg
Total Award Amount: \$899,998 (Chen's share: \$300,000)
Starting Date: 10/01/2016 Ending Date: 09/30/2021

Proposal Title: Automated Analog Mixed-Signals (AMS) Intellectual Property Generator for Complementary Metal Oxide Semiconductor (CMOS) Technologies
Source of Support: DARPA (account managed by AFRL): FA8650-18-2-7853
Project Location: USC PI: Anthony Levi, Co-PIs: Mike Chen, Sandeep Gupta, Wes Hanford
Total Award Amount: \$6,028,731 (Chen's share: \$1,930,468)
Starting Date: 06/25/2018 Ending Date: 12/30/2022

Proposal Title: Discrete-time mm-wave Processors for Scalable Digital Arrays
Source of Support: DARPA (account managed by AFRL): FA8650-19-1-7996
Project Location: USC PI: Hossein Hashemi, Co-PI: Mike Chen
Total Award Amount: \$1,200,000 (Chen's share: \$600,000)
Starting Date: 10/09/2018 Ending Date: 01/10/2023

Pending Research Grants

Proposal Title: CMOS Integrated Warm Electronics for Large Format Far Infrared Detectors
Source of Support: Jet Propulsion Laboratory (Prime: NASA)
Project Location: USC PI: Mike Chen
Total Award Amount: \$393,294
Starting Date: 10/01/2023 Ending Date: 09/30/2026

Proposal Title: SHF: Medium: Transistors to Algorithm Hardware Acceleration of Boolean Satisfiability (SAT) and NP Complete Problems
Source of Support: NSF
Project Location: USC PI: Sandeep Gupta, Co-PIs: Pierluigi Nuzzo, Mike Chen, Tony Levi
Total Award Amount: \$1,199,994 (Chen's share: \$259,544)
Starting Date: 10/01/2023 Ending Date: 09/30/2026

Proposal Title: ACED Fab: 3D memristor/CMOS Hybrid Field-programmable Analog Arrays for Signal Processing from RF to Baseband
Source of Support: NSF
Project Location: USC PI: Mike Chen, Co-PIs: Joshua Yang, Qiangfei Xia
Total Award Amount: \$600,000 (Chen's share: \$420,000)
Starting Date: 07/01/2023 Ending Date: 06/30/2026

Proposal Title: EFRI BRAID: Efficient learning in strongly-biased memristor-based neural architectures
Source of Support: NSF
Project Location: USC PI: Bartlett Mel, Co-PIs: Joshua Yang, Mike Chen, Greg Ver Steeg
Total Award Amount: \$1,996,702 (Chen's share: \$94,202)
Starting Date: 08/16/2023 Ending Date: 08/15/2027

LECTURED USC COURSES

Semester	Course No.	Course Title	Credit Hours	No. of Students	Instructor Rating (Max=5)
Spring 11	EE536B	Mixed Signal IC Design	3	38	4.09
Spring 12	EE536B	Mixed Signal IC Design	3	24	3.9
Fall 12	EE536B	Mixed Signal IC Design	3	15	3.5
Spring 13	EE536B	Mixed Signal IC Design	3	8	4.17
Fall 13	EE479	Analog Integrated Circuit Design	3	18	4.5
Fall 14	EE536B	Mixed Signal IC Design	3	27	3.7
Spring 15	EE479	Analog Integrated Circuit Design	3	17	3.82(mean) 4(median)
Fall 15	EE479	Analog Integrated Circuit Design	4	39	4.33(mean) 5(median)
Spring 16	EE536B	Mixed Signal IC Design	4	13	4.2 (mean) 5(median)
Fall 16	EE536A	Mixed Signal IC Design	4	31	4.73 (mean) 5(median)
Spring 17	EE536B	Mixed Signal IC Design	4	14	4.2 (mean)
Fall 17	EE 479	Analog Integrated Circuit Design	4	19	5 (mean)
Spring 18	EE 536B	Mixed Signal IC Design	4	6	5 (mean)
Spring 19	EE 536B	Mixed Signal IC Design	4	7	4.88 (mean)
Spring 20	EE 536B	Mixed Signal IC Design	4	15	4.29 (mean)
Fall 20	EE 479	Analog Integrated Circuit Design	4	24	4.4 (mean)

Spring 21	EE 536B	Mixed Signal IC Design	4	11	4.33 (mean)
Fall 21	EE 536A	Analog Integrated Circuits	4	46	4.57 (mean)
Spring 22	EE 631	Mixed Signal IC	4	18	4.4 (mean)
Fall 22	EE 582	Nano Neuromorphic Circuits	4	14	5 (mean)
Spring 23	EE631	Mixed Signal IC Design	4	13	4.83 (mean)

PAST SUPERVISED PHD RESEARCHERS

Name	Graduation	IEEE Awards (during PhD)	Current Position	Affiliation
Cheng-Ru Ho	Dec. 2017	SSCS pre-doctoral award 2017	Manager	D-matrix
Jaewon Nam	May 2019	CICC Best student paper award 2019	Assistant Professor	Seoul National University of Science and Technology, Korea
Shiyu Su	Dec. 2019	SSCS pre-doctoral award 2018	Assistant Professor	University of Waterloo, Canada
Tzu Fan Wu	Dec. 2019	SSCS pre-doctoral award 2020	Engineer	Marvell
Aoyang Zhang	Dec. 2020	SSCS pre-doctoral award 2021	Assistant Professor	Tsinghua University, China
Mohsen Hassanpourghadi	May 2021	ISSCC Jack Kilby award 2022	Engineer	Marvell
Qiaochu Zhang	Dec 2023	SSCS pre-doctoral award 2023	Assistant Professor	University of Virginia
Juzheng Liu	Dec 2023	ISSCC Jack Kilby award 2022, SSCS pre-doctoral award 2024	Post-doc	USC
Ce Yang	Dec 2023	RFIC Best student paper award 2022 (first place)	TBD	TBD
Rezwan Rasul	Dec 2023	N/A	TBD	TBD