

Patent No. 9,471,074
Petition For *Inter Partes* Review

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APTIV SERVICES US, LLC
Petitioner,

v.

MICROCHIP TECHNOLOGY, INC.
Patent Owner.

Patent No. 9,471,074

Case No. IPR2024-00646

PETITION FOR *INTER PARTES* REVIEW

UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.100 *et seq.*

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Exhibit List

Exhibit Description	Exhibit #
U.S. Patent No. 9,471,074	1001
Declaration of Dr. Michael S. Chen	1002
Prosecution History of U.S. Patent No. 9,471,074	1003
Mohammad Al-Shyoukh, et al., “A Transient-Enhanced Low-Quiescent Current Low-Dropout Regulator with Buffer Impedance Attenuation,” <i>IEEE Journal of Solid-State Circuits</i> , Vol. 42, No. 8 (Aug. 2007) (“Al-Shyoukh”)	1004
U.S. Patent No. 6,400,207 (“Ivanov”)	1005
U.S. Patent No. 6,710,583 (“Stanescu”)	1006
Miranda J. Ha, “A Low-Power, High-Bandwidth LDO Voltage Regulator with No External Capacitor” (May 23, 2008) (“Ha”)	1007
Le Ye, et al., “Highly Power-Efficient Active-RC Filters with Wide Bandwidth-Range Using Low-Gain Push-Pull Opamps,” <i>IEEE Transactions on Circuits and Systems—I: Regular Papers</i> , Vol. 60, No. 1 (Jan. 2013) (“Ye”)	1008
Mikhail Popovich, “High Performance Power Distribution Networks with On-Chip Decoupling Capacitors for Nanoscale Integrated Circuits” (2007) (“Popovich”)	1009
U.S. Patent No. 7,345,547 (“Wang”)	1010
Micrel Inc., MIC59300 Datasheet (Jan. 2009) (“MIC59300”)	1011
U.S. Patent No. 7,644,217 (“Butler”)	1012
U.S. Patent No. 6,046,577 (“Rincon-Mora”)	1013
Gabriel A. Rincon-Mora, “A Low-Voltage, Low Quiescent Current, Low Drop-Out Regulator,” <i>IEEE Journal of Solid-State Circuits</i> , Vol. 33, No. 1 (Jan. 1998) (“Rincon-Mora Paper”)	1014

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Gabriel A. Rincon-Mora, “Current Efficient, Low Voltage, Low Dropout Regulators” (Nov. 1996) (“Rincon-Mora Dissertation”)	1015
U.S. Patent No. 6,084,475 (“Rincon-Mora ’475”)	1016
Michael Day, “Understanding Low Drop Out (LDO) Regulators,” <i>2006 Texas Instruments Portable Power Design Seminar</i> (2006) (“Day”)	1017
Chester Simpson, “Linear and Switching Voltage Regulator Fundamental Part I” (2011) (“Simpson”)	1018
U.S. Provisional Patent Application No. 61/780,985	1019

Petitioner Aptiv Services US, LLC (“Aptiv”) petitions for *inter partes* review of claims 1-18 of U.S. Patent No. 9,471,074 (the “’074 patent”) (EX1001), in accordance with 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42.100 *et seq.*

I. INTRODUCTION

The ’074 patent relates to a low-dropout voltage regulator (“LDO”). By the claimed priority date of March 14, 2013¹, LDOs had long been a basic electronics component with a common conventional structure. The ’074 patent’s LDO uses that structure, comprising an error amplifier, a buffer driver, and an output driver that feeds back to one of the error amplifier’s differential inputs.

Equally well known by 2013 was the ’074 patent’s alleged improvement to this basic LDO design: A current feedback circuit that responds to changes in load by sensing changes in current at the output driver and boosting the transconductance (or “gm”) of the buffer driver. Al-Shyoukh, the primary basis for Ground 1 of this Petition, disclosed such a circuit in 2007. Rincon-Mora, the basis for Ground 2, did so in 1997.

¹ Aptiv disputes this priority date, but notes that whether this date, or the later date of March 11, 2014, is applied, the references underlying the petitioned grounds are nevertheless prior art under pre-AIA or post-AIA Section 102.

In fact, Patent Owner conceded during prosecution that Al-Shyoukh disclosed the feedback circuit that the patent proposes. In response to rejections based on Al-Shyoukh, Patent Owner amended the claims to include an “enable/disable function” for the bias circuit, a component that was separate from the feedback circuit. Patent Owner did not challenge the examiner’s view that Al-Shyoukh discloses the other claim elements—because it does. But even the “enable/disable function” was a well-known component used routinely in the field—so much so that the patent discusses it in just one sentence. A person of ordinary skill in the art (“POSITA”) would have found it obvious to include this component when implementing Al-Shyoukh’s and Rincon-Mora’s circuits.

Thus, the claimed invention was merely a well-known variant of a standard LDO, using conventional components in a conventional way. Aptiv submits that the claims of the ’074 patent should be canceled as unpatentable.

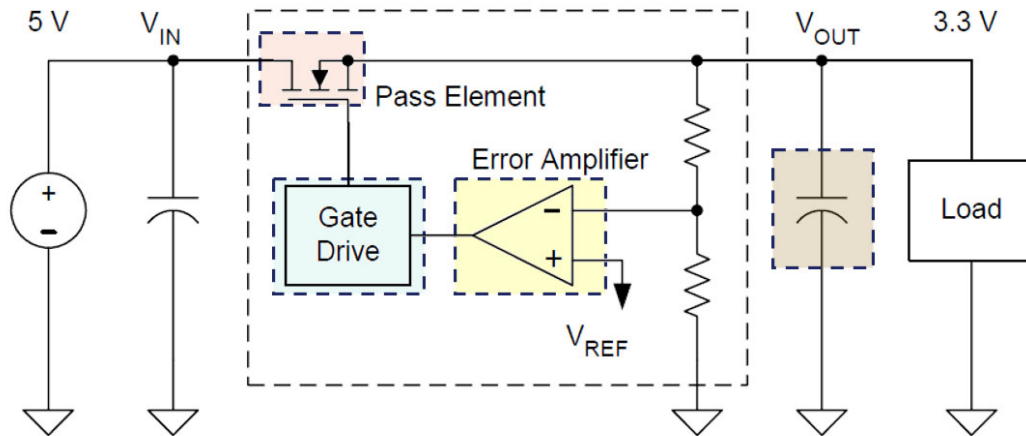
II. SUMMARY OF THE ’074 PATENT

A. Linear Voltage Regulators

Long before the claimed priority date, linear voltage regulators were a basic building block in electronics used to provide a constant output voltage regardless of changes in input or load. (EX1002 ¶¶ 19-24.)

The low-dropout regulator was one of the many well-known linear regulator models. (*Id.* ¶ 19.) Typical LDOs comprised an error amplifier coupled to a pass

element via a gate drive, with the output of the pass element feeding back to one of the error amplifier's differential inputs (the other input being a reference voltage):



(*Id.* ¶ 23; EX1017, Fig. 2 (annotated).) Because the output voltage feeds back to the error amplifier (shown in yellow above), the amplifier can regulate the output of the pass element (red) and thus allow the LDO to output a constant voltage to the load. (EX1002 ¶¶ 22-23.)

A typical LDO also works with a capacitor (shown in brown above) coupled to the output to stabilize the circuit when responding to changes in load. (*Id.*) This capacitor must be chosen carefully, as its equivalent series resistance (“ESR”) affects the circuit’s frequency response, causing instability if it is outside an acceptable ESR range. (*Id.* ¶¶ 25-28.) These basic principles of LDOs were well understood in the field as of March 14, 2013. (*Id.* ¶¶ 18-28; EX1018, 18-19.)

B. The '074 Patent

The '074 patent follows the conventional LDO model, with an amplifier that controls an output driver through a buffer driver, the output driver feeding back to the amplifier, and a capacitor coupled to the output driver and load:

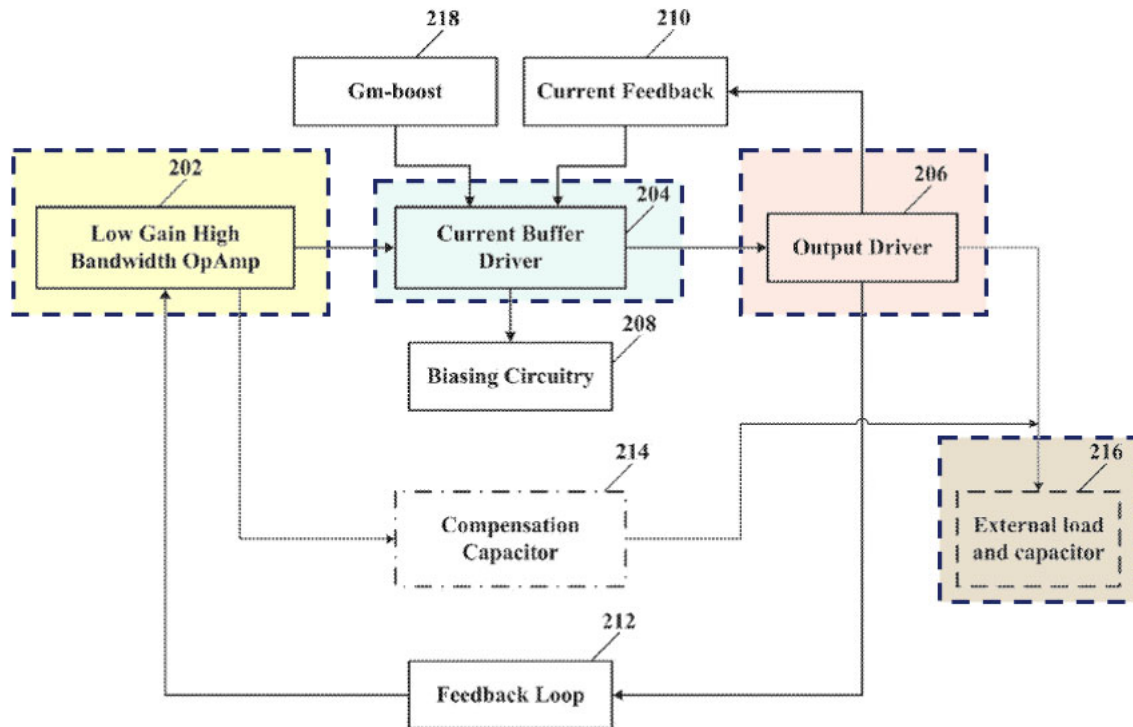


FIGURE 2

(EX1001, Fig. 2 (annotated); *see also* EX1002 ¶ 32.)

The patent purports to build on the standard LDO by expanding “the range of external capacitors with small to large ESR values” that the LDO can accommodate. (EX1001, 1:55-59.) According to the patent, LDOs must handle load changes that affect the pole at the output and thus the stability of the circuit. (*Id.*, 3:8-14.) One

way to improve stability is to separate this “dominant” pole from the “parasitic” gate pole of the output driver. (EX1002 ¶¶ 25-27, 33.) But this separation can be more difficult when the output driver is large (which is necessary to accommodate a “large transition range in load currents”), because the driver’s gate capacitance increases with size, lowering the frequency of the gate pole. (EX1001, 3:8-18, 4:6-11.) The patent thus identifies a need to increase that frequency. (*Id.*, 3:25-28.) To be clear, these were basic principles that a POSITA would have known. (EX1002 ¶¶ 25-28.)

To increase the frequency of the gate pole, the ’074 patent proposes increasing the transconductance (“gm”) of the buffer driver, as this would decrease the buffer’s output impedance, which has an inverse relationship with the gate pole. (EX1001, 4:6-15.) The patent’s LDO thus uses a “gm-boost circuit” with “current feedback” between the output driver and the buffer. (*Id.*, 4:15-20, 4:64-5:7.) This mechanism, the patent claims, effectively makes the LDO “a pseudo ‘one-pole’ system that is independent from the output pole changing so long as it falls within the bandwidth of the system.” (*Id.*, 5:40-45.) And as a result, “the range of ESR is extended along with the output capacitance.” (*Id.*, 5:40-46; *see also* EX1002 ¶¶ 25-28, 33-34.)

The patent does not explain in detail how its “gm-boost technique” works, but a POSITA would have understood it as follows. Shown below is Figure 3B of the patent, annotated to show its buffer driver in green and its “current feedback circuit” in blue:

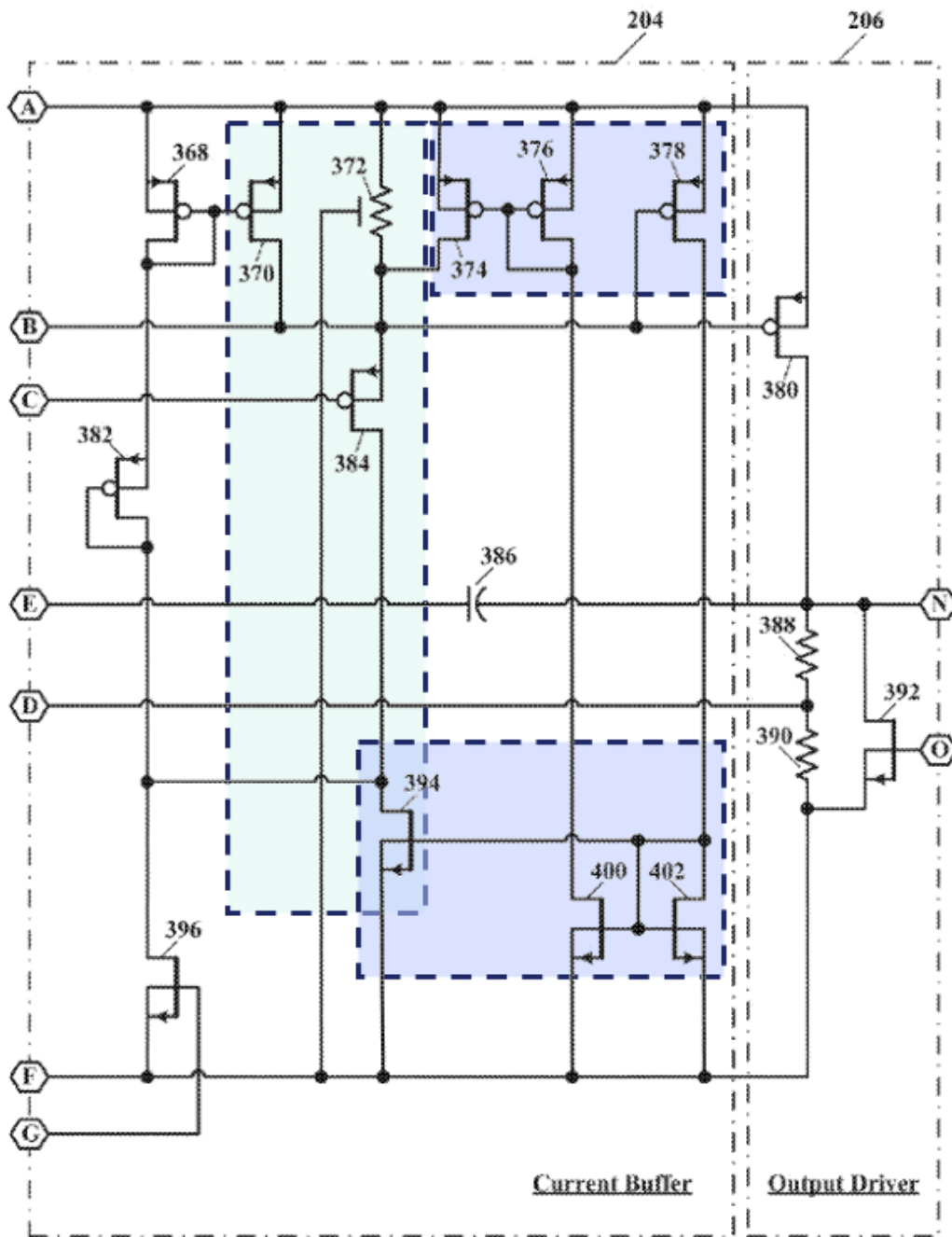


FIGURE 3B

(EX1001, Fig. 3B (annotated); *id.*, 5:10-15.) Transistor 378 senses changes in the output current of the power output transistor 380 because it is coupled to the gate of

transistor 380 at node B. (EX1002 ¶ 36.) This causes the current of transistor 378 to change in the same direction as the change in current of the output transistor; for example, if the output current increases, so does the current of transistor 378. (*Id.*) This increased current then flows to transistor 402 and is mirrored to transistors 394 and 400. (*Id.*) Because transistor 394 pulls current from transistor 384 (the buffer driver transistor), this in turn increases the current at transistor 384, boosting its gm. (*Id.*) Similarly, the current in transistor 400 pulls current from transistor 376, which mirrors current to transistor 374, which provides current to transistor 384, and thus boosts gm. (*Id.*)

The patent does not define transistors 368, 382, and 396 as part of this current feedback circuit, although it does include them in the broader “gm-boost stage.” (EX1001, 5:8-24.) A POSITA would have understood that these also contribute to the gm boost of the driver transistor 384. (EX1002 ¶ 37.) Transistors 394 (part of the feedback circuit) and 396 (whose current is set by the gate voltage provided by the bias network at node G) both draw current from transistor 368, which mirrors to transistor 370, which provides current to driver transistor 384. (*Id.*) Thus, increased current in transistor 394 adds to the gm boost in this other way. (*Id.*)

C. Prosecution History

Patent Owner filed the application for what became the '074 patent on March 11, 2014, claiming priority to a provisional application filed on March 14, 2013. As with the issued patent, the original application had a single independent claim.

In an office action dated August 31, 2015, the examiner rejected claims 1-4, 7-17, and 19-20 as anticipated by or obvious over U.S. Patent No. 6,246,221 (the "'221 patent") and U.S. Patent Pub. No. 2013/0241505. (EX1003, 142-151.) The examiner indicated that original claims 5, 6, and 18 would be allowable if they were not dependent on rejected claim 1. (*Id.*, 150.) Patent Owner responded that the '221 patent lacked the claimed "current buffer driver." (*Id.*, 130.)

In a second office action dated March 4, 2016, the examiner rejected claims 1-5, 7-17, and 20 as anticipated by Al-Shyoukh, and claim 19 as obvious over Al-Shyoukh, while indicating that claims 6 and 18 would be allowable if they did not depend from rejected claim 5. (*Id.*, 102-111.) Patent Owner did not dispute this.

Instead, it amended claim 1 to cover the same subject matter as claim 6. (*Id.*, 93-98.) Original claim 5, from which original claim 6 depended, recited "a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver." (*Id.*, 126.) Original claim 6 had recited "an enable/disable function to enable/disable the biasing circuit for reducing standby current." (*Id.*,

127.) Patent Owner added these two limitations to claim 1. (*Id.*, 94.) The examiner then allowed the amended claims.

Thus, the sole difference between original claim 5 (rejected over Al-Shyoukh) and claim 1 as issued was the “enable/disable function” for the biasing circuitry. It was *not* what the patent proffers as novel: a circuit that boosts the buffer driver’s gm.

In addition, the “enable/disable function” was not disclosed in the provisional application to which the ’074 patent claims priority. (*See* EX1019.) The effective filing date of the challenged claims is therefore no earlier than March 11, 2014.

III. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA in the field of the ’074 patent in 2013 would have had at least a Master’s Degree in Electrical Engineering, or alternatively a Bachelor’s Degree in Electrical Engineering and two years of experience working on analog circuit design. (EX1002, ¶ 38.)

IV. PRECISE REASONS FOR RELIEF REQUESTED

Pursuant to 37 C.F.R. § 42.104(b), asserts the following grounds, with the primary prior art references for each ground in italics:

Ground	35 U.S.C. §	Claims	Prior Art
1	103	1-18	<i>Al-Shyoukh (EX1004)</i> Ivanov (EX1005) Stanescu (EX1006)
2	103	1-18	<i>Rincon-Mora (EX1013)</i>

			<i>Rincon-Mora Paper (EX1014)</i> Al-Shyoukh (EX1004) Ivanov (EX1005) Stanescu (EX1006)
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A. Ground 1

The challenged claims were obvious over Al-Shyoukh in combination with Ivanov and/or Stanescu. Each reference is prior art under at least pre-AIA Sections 102(a) and 102(b) or post-AIA Section 102(a)(1). Ivanov and Stanescu are also prior art under pre-AIA Section 102(e) or post-AIA Section 102(a)(2).

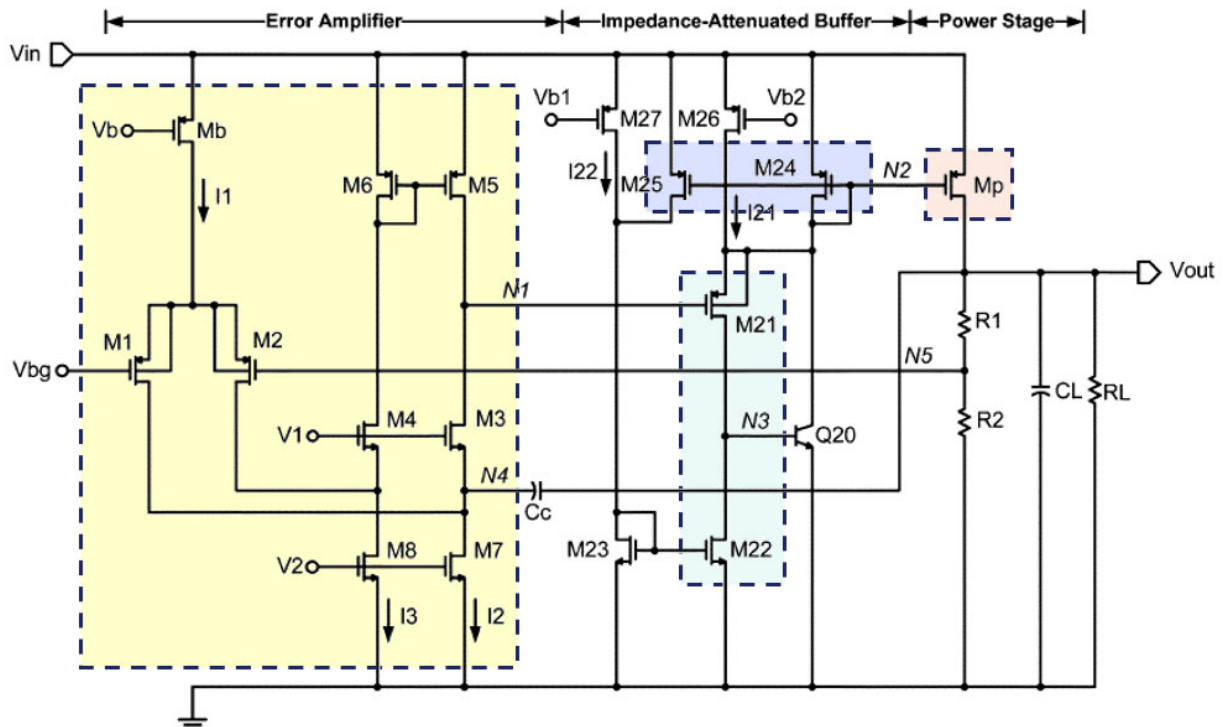
1. Summary of Al-Shyoukh

Al-Shyoukh discloses an LDO suitable for “battery-powered portable devices such as cellular phones and PDAs in order to reduce the standby power and prolong the battery runtime.” (EX1004, 1732.) Due to “the increased level of integration” in such devices, the LDO must “deliver high load current” while keeping “the no-load quiescent current” low for efficiency. (*Id.*; see also EX1002 ¶¶ 41-42.)

To meet these goals, Al-Shyoukh proposes an “impedance-attenuated buffer” for “[g]ood load transient response with small output-voltage variation,” two things that are “critical to prevent an accidental turn off or resetting of the portable device.” (EX1004, 1732.) Al-Shyoukh thus addresses the same problem and proposes the same solution as the ’074 patent: As noted above, the patent claims to improve the range of external capacitors and reduce the internal compensation capacitance value

by pushing the pole of output power driver to a higher frequency. (Section II.B, *supra*; EX1001, 1:55-58, 3:25-27.) Likewise, Al-Shyoukh's buffer makes it so that there is "only a single pole" in range of "the unity-gain frequency," achieving a "good phase margin" for "the entire load current range with a small compensation capacitor." (EX1004, 1733.) Al-Shyoukh's LDO also increases the range of output capacitors by providing "good transient settling behavior and small output-voltage variation even if a small output capacitor is used." (*Id.*; see also EX1001, 3:40-45 (discussing how the claimed circuit "allows reduced external capacitor size").) Al-Shyoukh thus disclosed a way to extend external capacitor range and reduce internal compensation capacitor size long before the '074 patent. (EX1002 ¶¶ 41-44.)

Al-Shyoukh's voltage regulator is shown below:



(EX1004, Fig. 8 (annotated).) This shows in yellow a single-stage folded cascode error amplifier, with “a simple diode-connected active load using transistors M_5 and M_6 .” (*Id.*, 1738.) One of the differential inputs is reference voltage V_{bg} ; the other is a feedback signal through node N_5 , coming from the output of the pass device that supplies the output voltage (in red). (*Id.*, Fig. 8; *see also* EX1002 ¶¶ 45-46.) The amplifier outputs a voltage at node N_1 to the gate of transistor M_{21} of the impedance-attenuated buffer’s driver, which is shown in green above. (EX1004, Fig. 8.)

The voltage regulator further includes a current feedback circuit comprising transistors M_{24} and M_{25} (*Id.*, 1734; *see also* EX1002 ¶ 46), which operate as follows: If there is an increase in load current flowing through pass device M_p (*e.g.*, when going from no load to full load), the voltages at nodes N_1 and N_2 drop, increasing the source-gate voltage of M_{24} , increasing current through M_{24} , which is mirrored through M_{25} , increasing current through M_{21} (via M_{22} and M_{23}), and thus increasing transconductance g_{m21} . (EX1004, 1734.) In the other direction (full load to no load), the voltage increases at N_1 , which causes M_{24} to provide “extra transient current to charge C_p [(capacitance at N_2)] and increase the voltage at N_2 to follow the voltage change at N_1 with a faster slewing.” (EX1004, 1735; *see also* EX1002 ¶ 47.)

Thus, the additional currents provided by M_{24} and M_{25} improve “slewing of the gate drive at N_2 during load transients,” move the parasitic pole p_2 to “high

frequencies under different load currents,” and allow the LDO to operate with “low quiescent current at no-load.” (EX1004, 1735; *see also* EX1002 ¶ 47.)

2. 35 U.S.C. § 325(d) Does Not Apply

Although Al-Shyoukh was before the examiner during prosecution, Ground 1 is not subject to discretionary denial under 35 U.S.C. § 325(d). Ground 1 challenges each of the '074 patent's claims based not on Al-Shyoukh alone, but on Al-Shyoukh in combination with Ivanov. Ivanov was not before the examiner and disclosed the limitation Patent Owner added to overcome Al-Shyoukh. (*See* EX1003, 94, 109; *see also* Section IV.A.3, 1[d], *infra*.)

The Board in *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH* set a two-part test for applicability of Section 325(d). No. IPR2019-01469, Paper 6, 8 (PTAB Feb. 13, 2020). Both steps preclude discretionary denial.

Starting with the first step, neither the same nor substantially the same art or arguments underlying Ground 1 was previously before the PTO. That “one piece of art” in a combination “was previously presented and/or argued” is “insufficient to satisfy the first prong of *Advanced Bionics*.” *Thorne Research, Inc. v. Trustees of Dartmouth Coll.*, No. IPR2021-00491, Paper 18, 8 (PTAB Aug. 12, 2021) (no denial where other reference in combination was not before the examiner); *Samsung Elecs. Co. v. Headwater Rsch. LLC*, No. IPR2023-01226, Paper 9, 6-7 (PTAB Feb. 8, 2024) (same); *BMW of N. Am., Inc. v. Mich. Motor Techs., LLC*, No. IPR2023-01031,

Paper 12, 13 (PTAB Jan. 23, 2024) (same). Nor is Ivanov cumulative; its primary subject is the very limitation that the examiner did not find disclosed in Al-Shyoukh. (See Section IV.A.3, 1[d], *infra*.) Thus, the inquiry should end here.

To the extent Ivanov *is* cumulative of any previously presented art—it is not—the second step of the *Advanced Bionics* inquiry—whether the examiner erred in a manner material to patentability—would still preclude discretionary denial. This is because, to the extent Ivanov is cumulative, the examiner’s rejections were not based on the hypothetical cumulative art; in fact, the examiner never rejected the claims containing the “enable/disable function” outright. (See Section II.C, *supra*.) Thus, the examiner would have erred materially by “overlooking something persuasive.” *Advanced Bionics*, 9-10; see also *InductEV, Inc. v. WiTricity Corp.*, No. IPR2023-01208, Paper 9, 6-7 (PTAB Feb. 20, 2024) (material error where record of PTO’s prior consideration of art “is not well developed or silent”); *Google LLC v. Geoscope Techs. Pte. Ltd.*, No. IPR2023-01212, Paper 14, 19-21 (PTAB Feb. 20, 2024) (no denial due to lack of evidence that examiner “fully considered all the disclosure” in petitioned reference); *CODE200, UAB v. Bright Data Ltd.*, No. IPR2022-00353, Paper 8, 10 (PTAB July 1, 2022) (fact that reference was not the basis of a rejection weighs “strongly against” denial). As explained below, Ivanov disclosed the claimed “enable/disable function” in far greater detail than the ’074 patent itself, and there existed ample motivation to add it to Al-Shyoukh, which Patent Owner

conceded during prosecution disclosed every other limitation. (See Section IV.A.3, 1[d], *infra*.)

3. Analysis

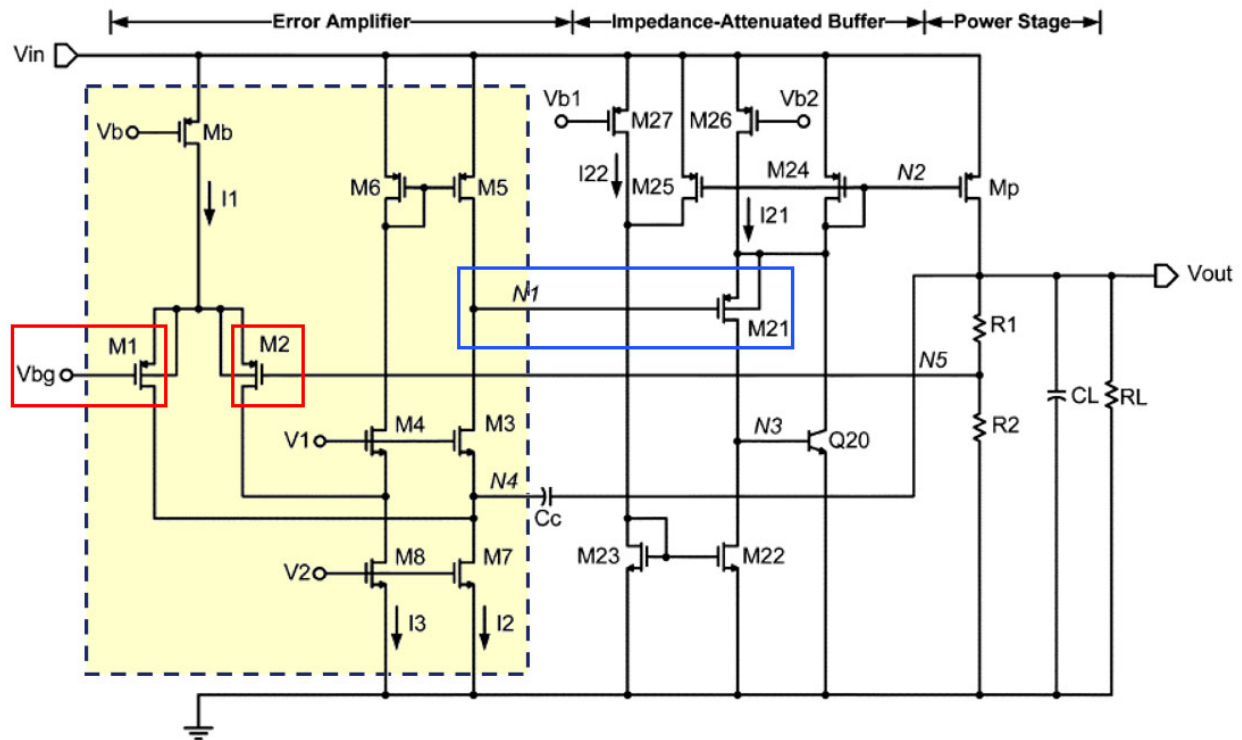
A POSITA would have found each claim of the '074 patent to be obvious over Al-Shyoukh in view of Ivanov and/or Stanescu.

Claim 1 A voltage regulator, comprising:

Al-Shyoukh discloses a “low-dropout regulator,” which is a voltage regulator. (EX1004, Abstract.)

[a] an operational amplifier;

Al-Shyoukh’s LDO includes an error amplifier, which a POSITA would have understood to be an operational amplifier. (EX1004, 1738, Fig. 8; *see also* EX1002 ¶¶ 50-52.) As shown below, the op-amp (yellow) receives differential input voltages at transistors M₁ and M₂ (red) and outputs a voltage at node N₁ to transistor M₂₁ (blue):



(EX1004, Fig. 8 (annotated); *see also id.*, 1741 (explaining the voltage regulator by citing to papers discussing the properties of operational amplifiers); EX1002 ¶¶ 50-52.) Operational amplifiers were also a conventional design for an error amplifier. (EX1002 ¶ 52.) Al-Shyoukh thus discloses or renders obvious limitation 1[a].

[b] a gm enhanced current buffer driver;

Al-Shyoukh’s buffer driver discloses this limitation. Centered on the driver transistor M₂₁, Al-Shyoukh’s buffer is “gm enhanced” because it receives a gm boost from a current feedback circuit comprising M₂₄ and M₂₅, as detailed above. (Section IV.A.1, *supra*; EX1004, 1733-35, Figs. 3, 4, 8; *see also* EX1002 ¶ 53.)

To the extent Patent Owner argues that Al-Shyoukh’s buffer is not a *current* buffer, it should be noted that the ’074 patent describes only the same kind of buffer

as Al-Shyoukh's. The patent describes a "low-impedance current buffer driver 204" centered at the driver transistor 384, which "creates a low impedance environment" to "separate the poles seen on the big power output driver." (EX1001, 3:57, 4:64-5:1.) Transistor 384 is a "source follower." (*Id.*, 4:36.) A POSITA would therefore have understood the patent to be using what was conventionally known as a *voltage* buffer, which provides low output impedance and was a well-known application for source followers. (EX1002 ¶ 54.)

Al-Shyoukh's buffer is equivalent to the '074 patent's buffer: Its output is a "low impedance node" with parasitic pole p_2 "located at a very high frequency under the full range of the load current," *i.e.*, separated from dominant pole p_o . (EX1004, 1735; EX1002 ¶ 55.) It is also implemented with "source-follower M_{21} ." (EX1004, 1734.) A POSITA would thus have understood Al-Shyoukh to disclose limitation 1[b] in the same way the patent does. (EX1002 ¶ 55.)

[c] a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver;

Al-Shyoukh's LDO uses a biasing circuit coupled to the buffer driver to set a voltage V_{b1} at the gate of transistor M_{27} , providing a bias current I_{22} that is mirrored across transistors M_{23} and M_{22} to set a biasing ratio for gm-boost of the current buffer driver. (EX1002 ¶¶ 56-58; EX1004, Fig. 8.)

This matches the patent's description of a bias network "fixed by transistor 396" such that the current from the network is "ratio'ed in transistors 368 and 370"

with a feedback current. (EX1001, 5:15-24.) As shown below, the current of 368 (purple) is the sum of the current in 396 (blue) and another current flowing to 394 (red):

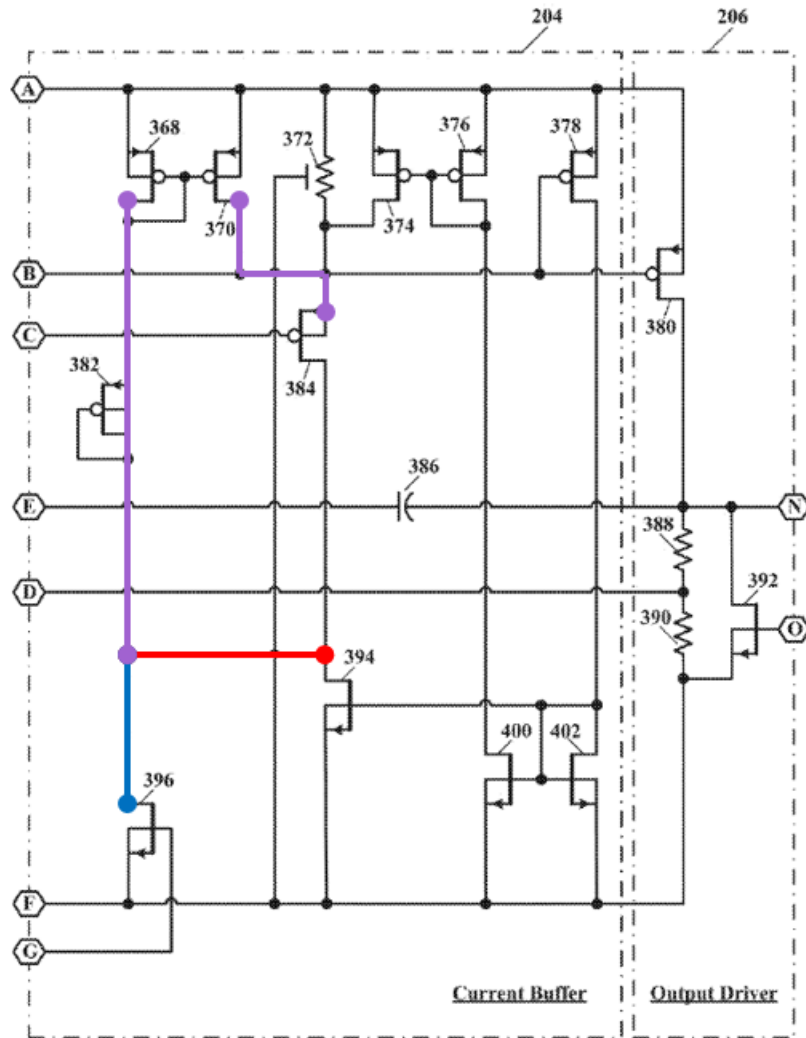
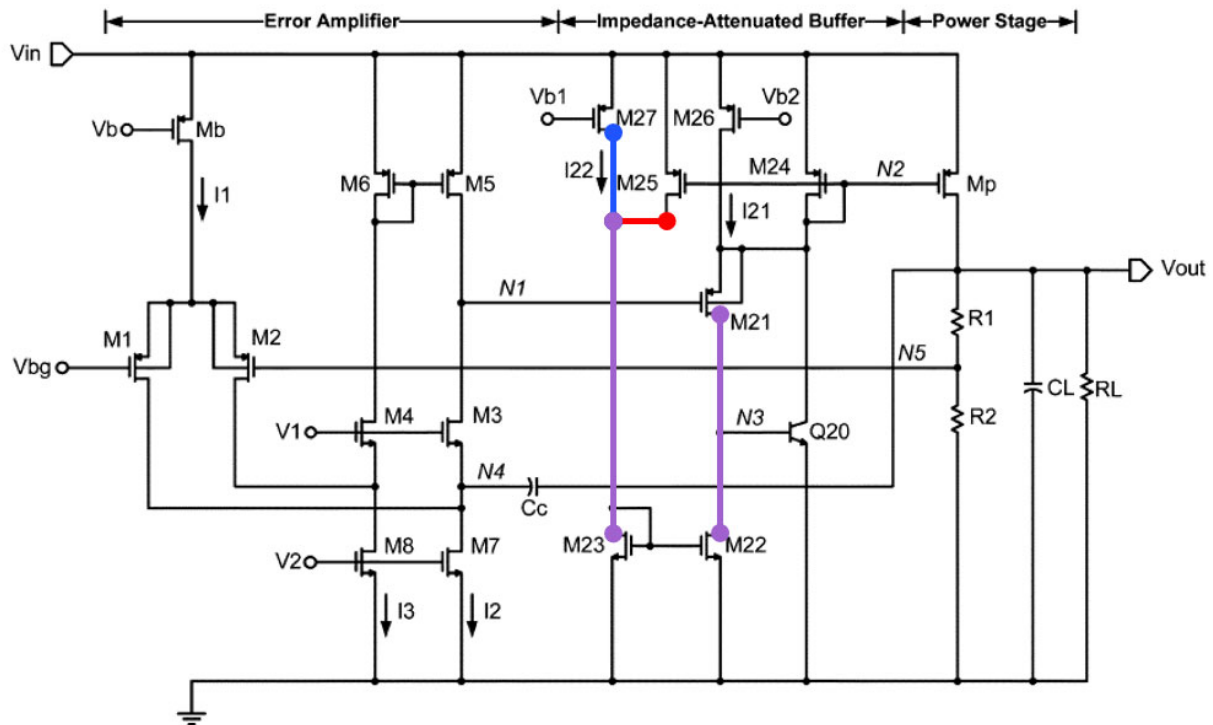


FIGURE 3B

(EX1001, Fig. 3B (annotated); EX1002 ¶ 57.) The red current is a feedback current because 394 mirrors 402, which draws current from 378 and thus reacts to changes at the output transistor 380. (*Id.*, 5:13-14, Fig. 3B; EX1002 ¶ 57.) This makes the

purple current a sum of a bias current and a feedback current. (EX1002 ¶ 57.) It is this sum that is “ratio’ed in transistors 368 and 370” to provide current, and thus a “gm-boost,” to the buffer driver at transistor 384. (*Id.*; see also EX1001, 5:21-23.)

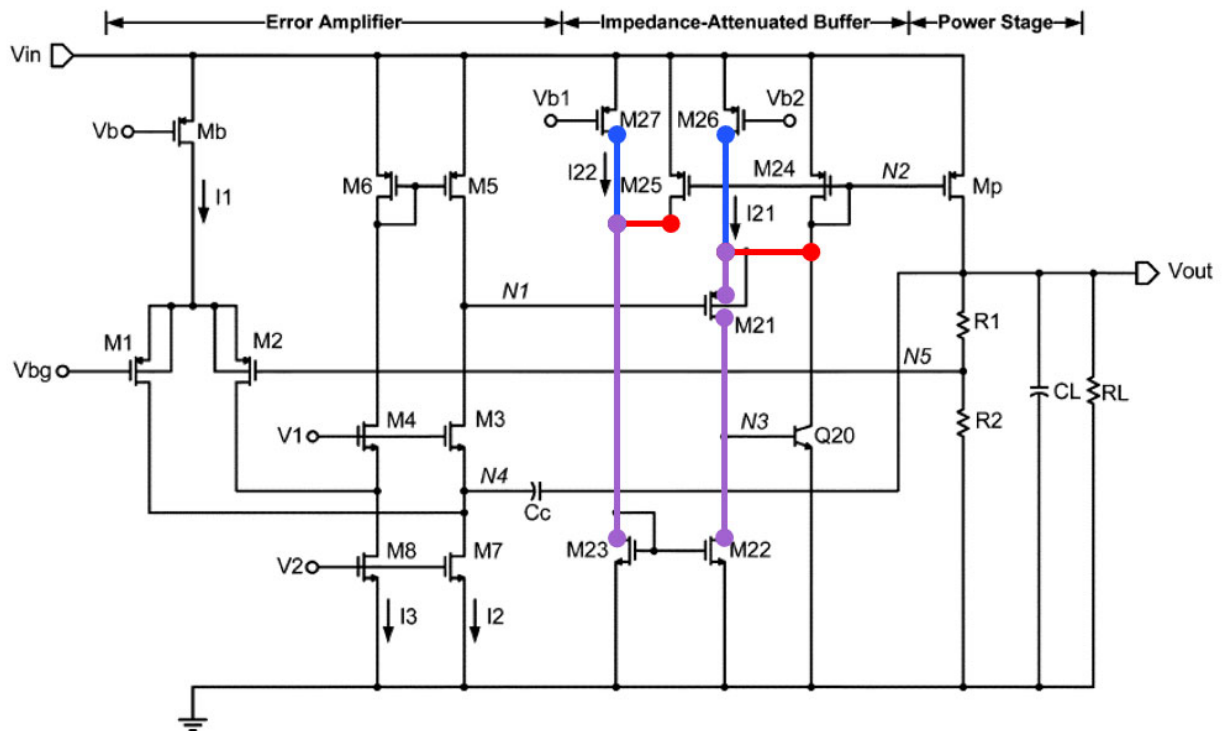
Al-Shyoukh’s LDO sets “a biasing ratio for gm-boost” in the same way:



(EX1004, Fig. 8 (annotated); EX1002 ¶ 56.) This bias current (blue) joins another current, provided by M25 (red), to form a sum current (purple) that flows to transistor M23. The red current is a feedback current, as M25 is part of Al-Shyoukh’s feedback circuit. (EX1002 ¶ 56; see also Section IV.A.1, *supra*.) Thus, M22 and M23 “ratio” a sum current that includes a bias current and a feedback current. (EX1002 ¶ 56.) Because M22 draws current from the buffer driver transistor M21, the driver receives a gm boost. (*Id.*; see also EX1004, 1734.)

Alternatively, to the extent Patent Owner argues that “biasing ratio” should be understood to mean a ratio of current that the current buffer draws from DC relative to the current feedback circuit,² a POSITA would have read Al-Shyoukh to disclose this limitation through the biasing circuit that provides voltages V_{b1} at transistor M_{27} and V_{b2} at transistor M_{26} . (EX1004, Fig. 8.) V_{b1} and V_{b2} determine the bias currents I_{22} and I_{21} , respectively, and as shown below, I_{22} and I_{21} (blue) add to feedback currents from M_{25} and M_{24} (red) to provide a gm-boost to the buffer driver at M_{21} :

² For some limitations, Aptiv will show why the challenged claims are unpatentable under Patent Owner’s expected claim constructions. The Board has approved this approach. *See, e.g., 3Shape A/S v. Align Tech., Inc.*, No. IPR2020-00174, Paper 14, 11-12 (PTAB Jun. 12, 2020) (petitioner need not hold “subjective belief of the correctness of the construction[s] asserted”); *W. Digit. Corp. v. SPEX Techs., Inc.*, No. IPR2018-00084, Paper 14, 11 (PTAB Apr. 25, 2018) (an argument based on Patent Owner’s constructions in district court meets 37 C.F.R. § 104(b)(3)); *see also Gen. Elec. Co. v. Vestas Wind Sys. A/S*, No. IPR2018-00928, Paper 9, 14 (PTAB Nov. 9, 2018) (petitioner can argue “more than one construction, including one that it believes is incorrect, such as patent owner’s”).



(EX1004, Fig. 8 (annotated); *see also* EX1002 ¶ 59.) A POSITA would have known that the biasing circuit could be adjusted to set V_{b1} and V_{b2} , and thus a ratio of current drawn from DC and current drawn from feedback. (EX1002 ¶ 59.)

[d] an enable/disable function to enable/disable the biasing circuit for reducing standby current;

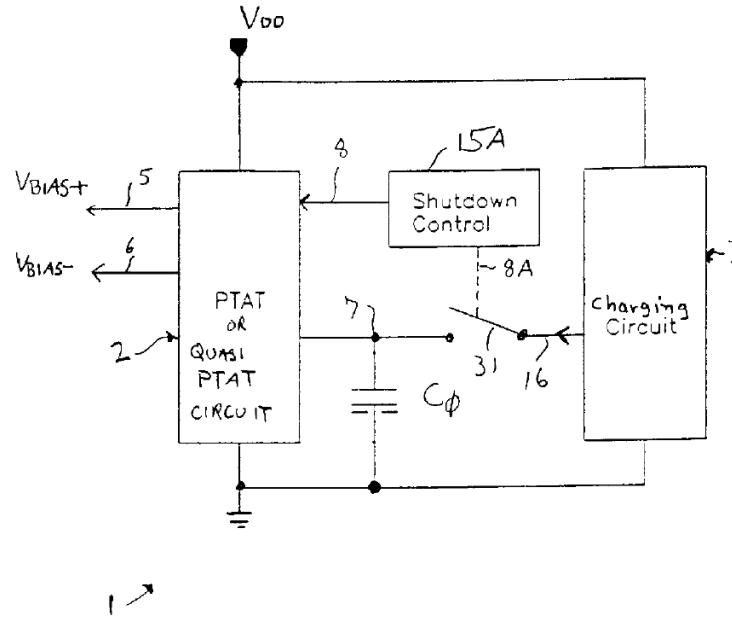
From the parallel district court proceeding, Aptiv understands Patent Owner to contend that 1[d] is not a means-plus-function element under Section 112 ¶ 6, and to the extent it is, the claimed function is to enable/disable the biasing circuit for reducing standby current, and the corresponding structure is the signal input line at

node M in Figure 3. Under that construction, Al-Shyoukh with Ivanov discloses 1[d].³

Al-Shyoukh discloses inputs from a biasing circuit into its LDO but does not specify a design. A POSITA would have understood that the biasing circuit could be implemented using conventional, well-understood methods and would have seen that Ivanov disclosed one such method. (EX1002 ¶¶ 60-70.)

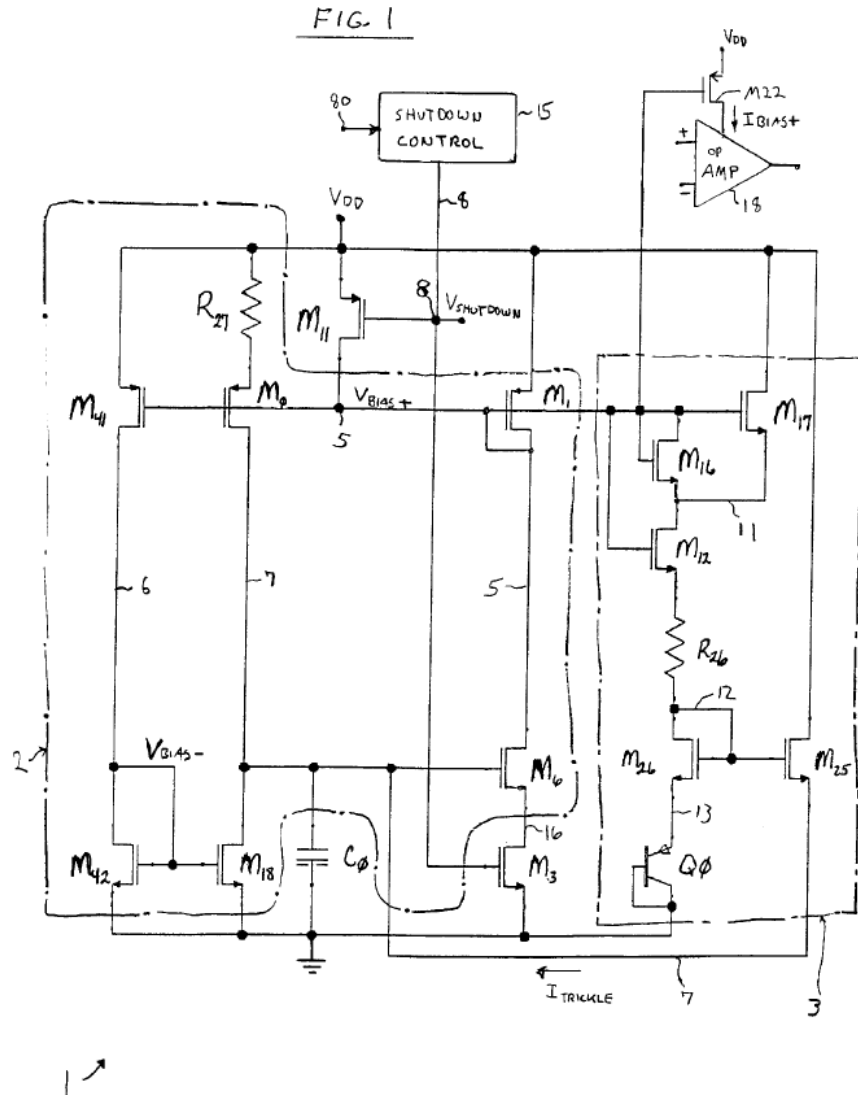
Ivanov discloses “a quick turn-on disable/enable bias control circuit” for use in “integrated circuit applications.” (EX1005, 1:6-9.) According to Ivanov, circuits often have “nodes that need to be quickly charged to a predetermined voltage level.” (*Id.*, 1:12-18.) But power efficiency also requires keeping circuitry “in a quiescent, low-power state until fully functional circuit operation is needed.” (*Id.*, 1:12-18.) To address these concerns, Ivanov presents an enable/disable mechanism “suitable for fast disabling and subsequent fast enabling of the bias circuitry” for “applications such as voltage regulators”:

³ Aptiv does not concede that this or any other claim satisfies 35 U.S.C. § 112, which is not an available ground in *inter partes* review. 35 U.S.C. § 311(b).



(*Id.*, 6:47-52, Fig. 2.) Here, the bias core circuit (block 2) is “coupled between V_{DD} and ground.” (*Id.*, 4:26-29.) It produces V_{BIAS+} and V_{BIAS-} and receives a control input from shutdown control circuit 15A. (*Id.*, 4:30-33; *see also* EX1002 ¶¶ 61-62.)

Figure 1 of Ivanov shows more detail:



(EX1005, Fig. 1.) As shown, this circuit generates a voltage V_{BIAS+} at node 5 that is coupled to the gate of transistor M22, which outputs bias current I_{BIAS+} . (EX1002 ¶ 64; EX1005, 3:54-63.)

The lynchpin of the enable/disable mechanism is “P-channel bias core disable transistor M11,” which receives at its gate “an external signal $V_{SHUTDOWN}$ produced by an external shutdown control circuit 15 in response to an external control signal applied to an external input 80 thereof.” (*Id.*, 3:43-49; *see also* EX1002 ¶ 63.) If

the shutdown control circuit wants to disable I_{BIAS+} “so as to dissipate a minimum amount of power,” it sends a disable signal to M11 by setting $V_{SHUTDOWN}$ low. (*Id.*, 5:19-24.) This “turns on transistor M11,” which “pulls conductor 5 close to V_{DD} ,” which shuts M22 off, disabling I_{BIAS+} . (*Id.*, 5:24-25.) And if the shutdown control circuit wants to enable I_{BIAS+} , it sends an enable signal by setting $V_{SHUTDOWN}$ high, which “turns transistor M11 off” and returns the voltage of conductor 5 to the “desired value of V_{BIAS+} ” so that M22 outputs I_{BIAS+} . (*Id.*, 6:7-22; *see also* EX1002 ¶¶ 65-66.)

A POSITA would have been motivated to use Ivanov’s disable/enable control mechanism for Al-Shyoukh’s biasing circuit. Al-Shyoukh is highly concerned with power efficiency, and Ivanov’s mechanism saves power by shutting off circuitry when it is not needed. (*Compare* EX1004, 1732 (describing LDOs as “critical power management modules” and identifying “low no-load quiescent current” as a major performance requirement of the LDO) *with* EX1005, 1:6-18 (proposing disabling not-in-use circuitry for “a quiescent, low-power state”).) Ivanov, moreover, identifies voltage regulators as an intended application for its circuit. (EX1005, 6:47-54.) Furthermore, a POSITA could have integrated Ivanov’s enable/disable function into Al-Shyoukh without undue experimentation because Ivanov provides a ready-to-use circuit that would have required only conventional modifications to

accommodate each of the bias voltages required by Al-Shyoukh's LDO. (EX1002 ¶¶ 67-68.)

Thus, Al-Shyoukh combined with Ivanov would have had a signal provided by a shutdown control circuit for enabling and disabling the biasing circuit to reduce standby current, disclosing 1[d] under Patent Owner's proposed construction in the parallel district court proceeding. And to the extent 1[d] is a means-plus-function limitation, that signal is identical to Patent Owner's alleged corresponding structure (the signal input line at node M), as shown below:

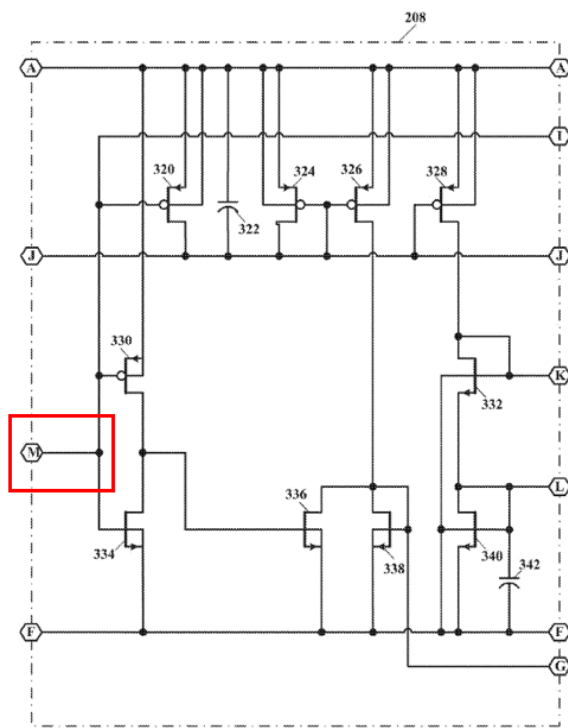
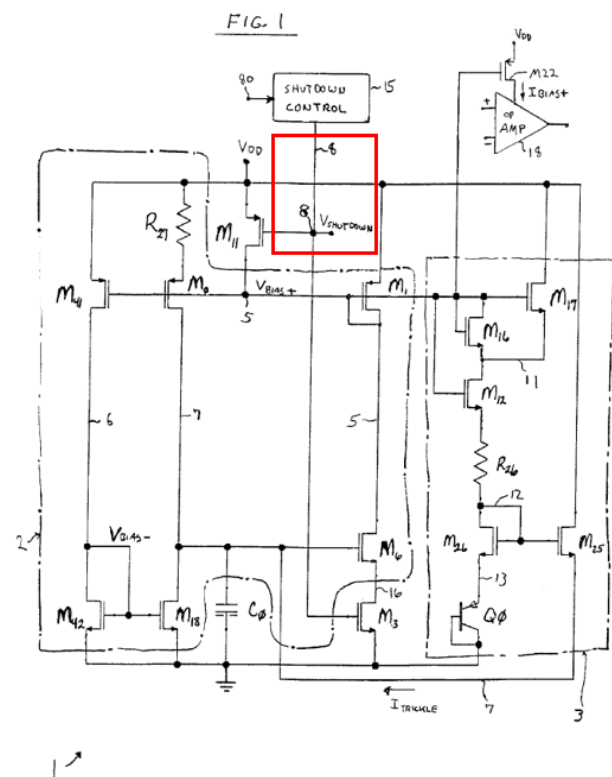
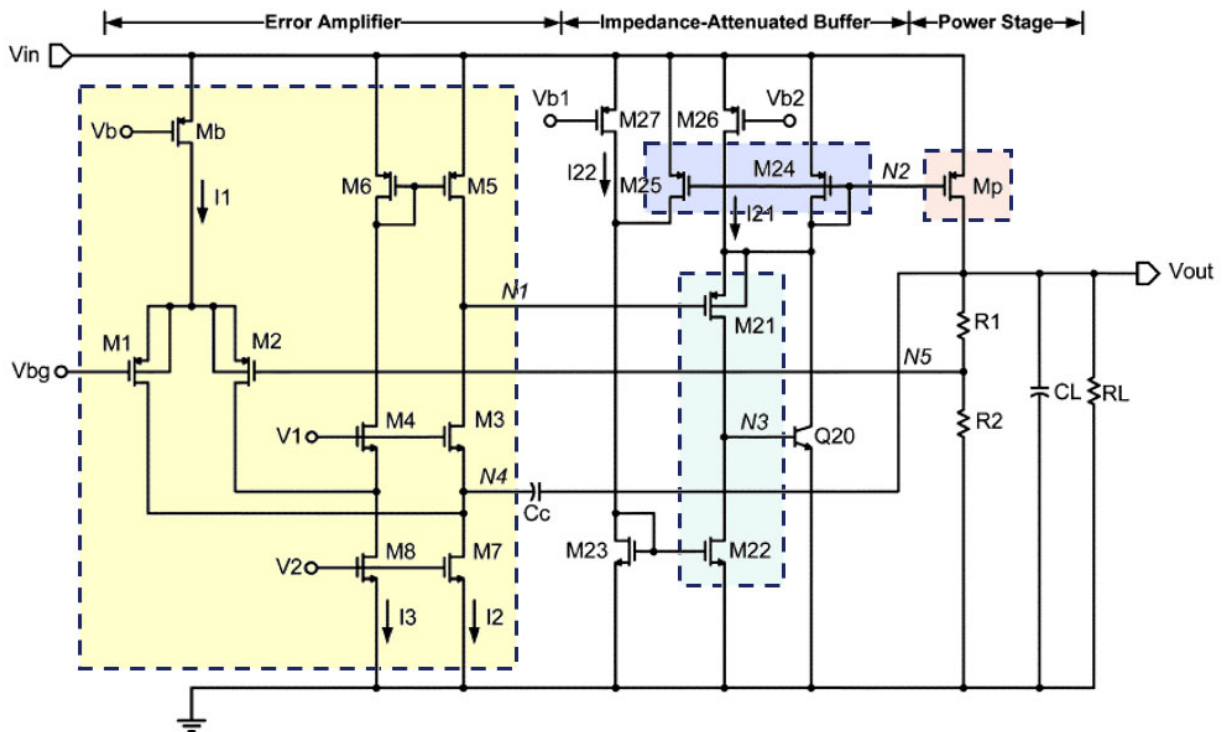


FIGURE 3



[e] an output power driver, wherein the current buffer driver is coupled between the operational amplifier and the output power driver;

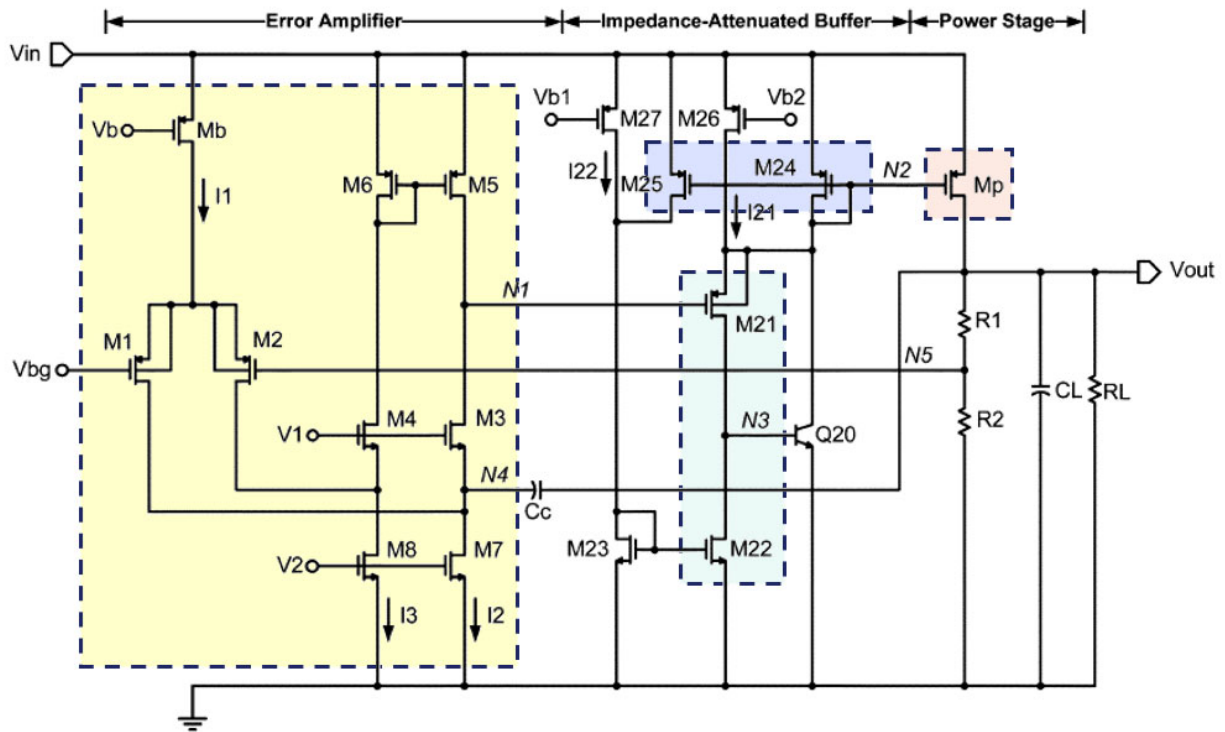
Al-Shyoukh's LDO has an output power driver M_p . (EX1004, 1732, Fig. 8; see also EX1002 ¶ 71.) The buffer driver (in green below) is coupled between the operational amplifier (yellow) and the output power driver (red):



(EX1004, Fig. 8 (annotated); see also EX1002 ¶ 71.)

[f] a current feedback circuit coupled between the output power driver and the current buffer driver; and

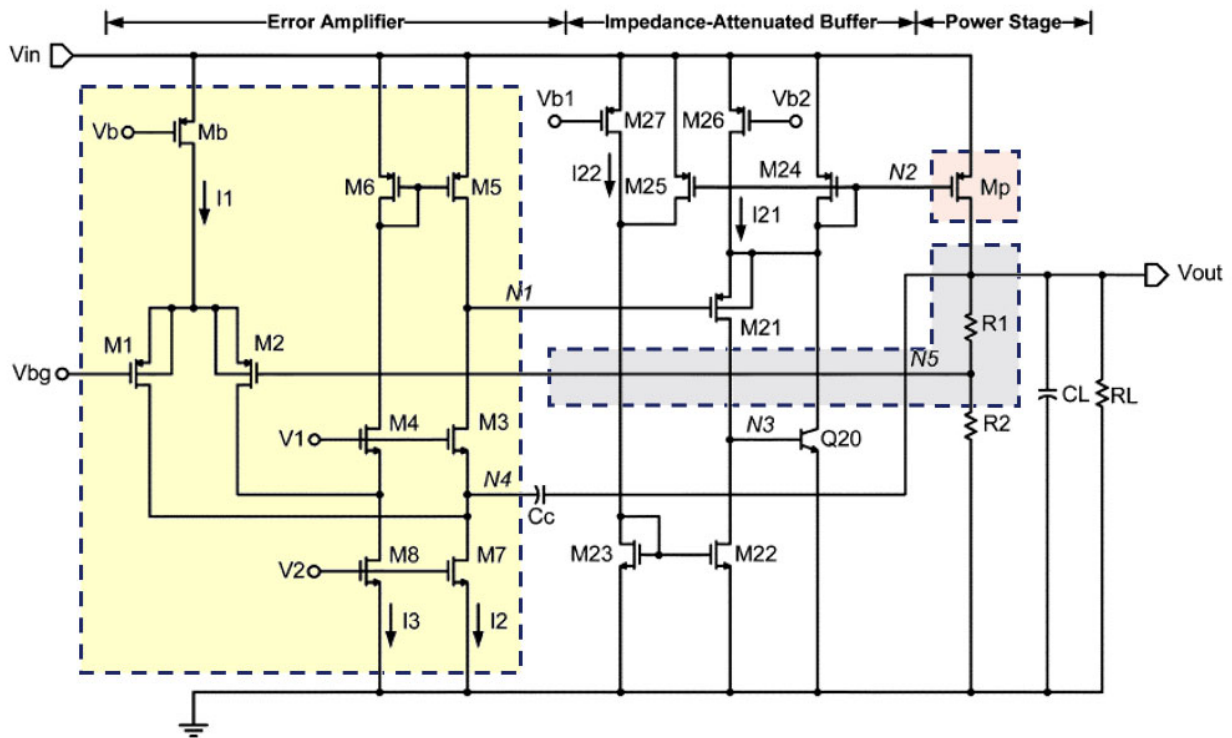
As discussed above in the summary of Al-Shyoukh's LDO and shown below, the LDO includes a current feedback circuit (blue) coupled between its output power driver (red) and the buffer driver (green):



(EX1004, 1734, Fig. 8 (annotated); see also EX1002 ¶ 72; Section IV.A.1.)

[g] a feedback loop coupled between the output power driver and the operational amplifier.

Al-Shyoukh's LDO has a feedback loop coupled between the output power driver and the operational amplifier. As noted above for 1[a], one of the differential inputs to the amplifier is a feedback signal from the pass device, as shown below:



(EX1004, Fig. 8 (annotated); *see also* EX1002 ¶ 73; Section IV.A.3, 1[a], *supra*.)

Here, the feedback loop (gray) is coupled between the operational amplifier (yellow) and the output power driver (red), as claimed.

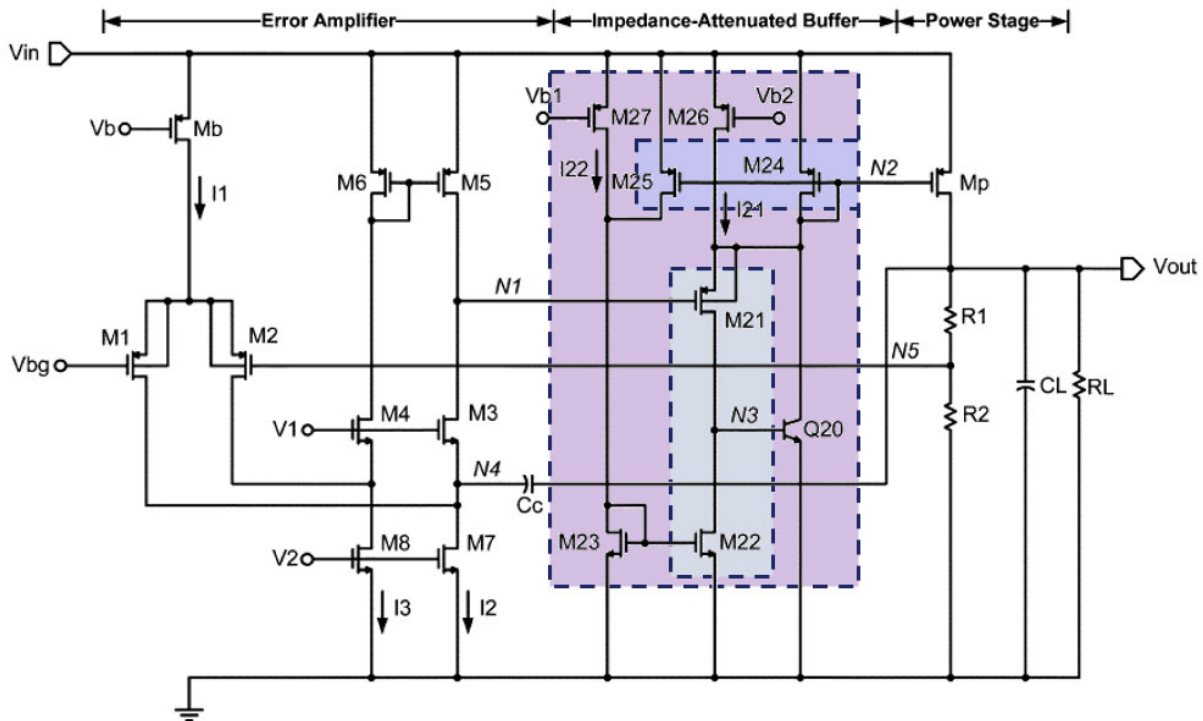
Claim 2 The voltage regulator according to claim 1, further comprising a gm-boost circuit coupled to the current buffer driver.

Al-Shyoukh’s LDO has a gm-boost circuit in the form of a current feedback circuit coupled to the buffer driver. (EX1004, 1734, Fig. 8; *see also* Section IV.A.1, *supra*; EX1002 ¶¶ 74-76.)

While the ’074 patent does not define the term “gm-boost circuit,” it identifies a “gm-boost stage 218” comprising “transistors 368, 370, 374, 376, 378, 382, 396,

394, 400, 402, 384 and resistor 372.” (EX1001, 5:8-10.) This gm-boost stage thus includes each of the components that comprise the current buffer driver (transistors 370, 384, and 394, and resistor 372 (*id.*, 5:10-12)) and the current feedback circuit (transistors 374, 376, 378, 394, 400, and 402 (*id.*, 5:13-14)). Thus, a POSITA would have understood that the “gm-boost circuit coupled to the current buffer driver” may include both the buffer driver and the current feedback circuit. (EX1002 ¶ 75.)

Al-Shyoukh’s LDO likewise includes a gm-boost circuit (shown in purple below) that includes a buffer driver (green) and a current feedback circuit (blue):

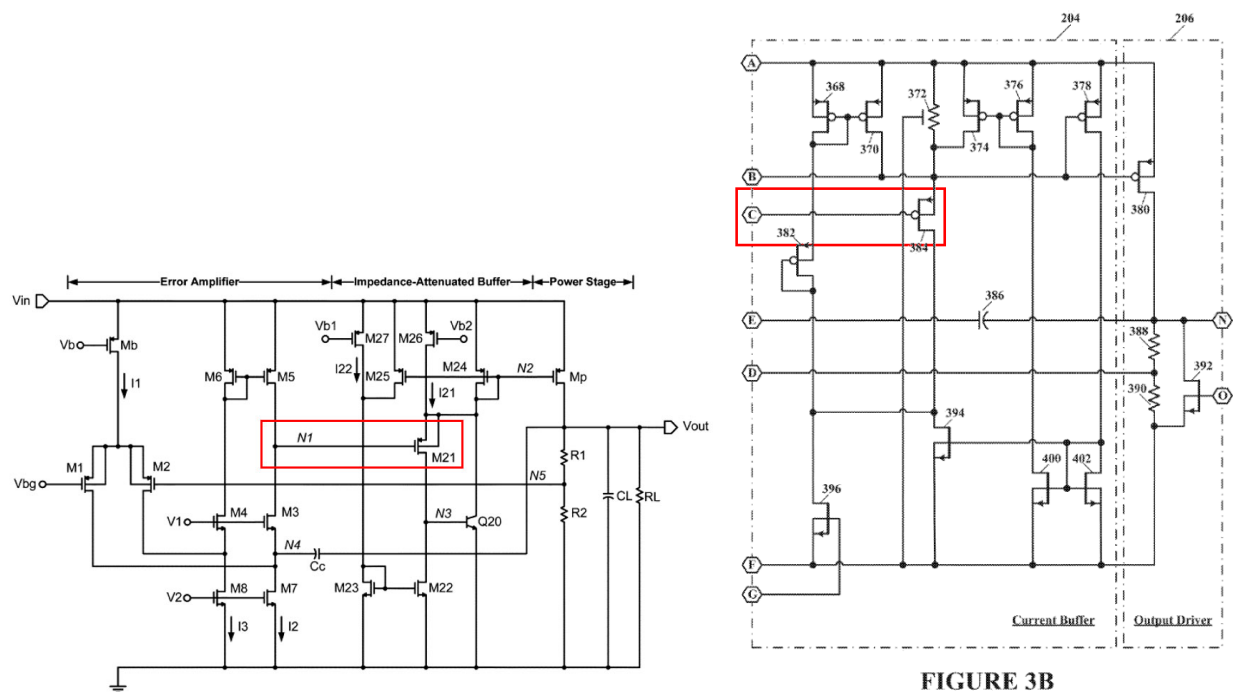


(EX1004, Fig. 8 (annotated); *see also* EX1002 ¶ 76.) As explained above, this gm-boost circuit “boosts” the gm of the buffer driver. (*See* Sections IV.A.1, IV.A.3, 1[b], 1[c], *supra*.)

Claim 3 The voltage regulator according to claim 2, wherein the gm-boost circuit increases the current buffer driver input impedance.

From the parallel district court proceeding, Aptiv understands Patent Owner to read claim 3 as claiming a gm-boost circuit that, by providing current feedback—and thereby reducing the current that the input must supply—increases the input impedance at the point where the operational amplifier connects to the current buffer driver. To the extent claim 3 is understood this way, Al-Shyoukh renders it obvious.

Al-Shyoukh’s operational amplifier connects to the buffer driver by providing a voltage at the gate of M₂₁, just as the ’074 patent’s amplifier provides a voltage at the gate of 384, as shown below:



(EX1004, Fig. 8 (annotated); EX1001, Fig. 3B (annotated); EX1002 ¶ 78.) Also, Al-Shyoukh’s gm-boost circuit provides the buffer driver with current feedback (see

Section IV.A.1, *supra*), just as the '074 patent's gm-boost circuit does. (Ex 1002. ¶ 78.) Given these parallel structures, a POSITA would have found Al-Shyoukh's gm-boost circuit to "increase input impedance at the point where the operational amplifier connects to the current buffer driver" in the same way that the '074 patent does. (*Id.*)

Alternatively, to the extent "wherein the gm-boost circuit increases the current buffer driver input impedance" means that because of the current feedback provided by the gm-boost circuit, a transistor with relatively higher input impedance may be used as the buffer driver, Al-Shyoukh discloses this requirement. Its feedback circuit (comprising M₂₄ and M₂₅) seeks to reduce the output resistance r_{ob} of the buffer driver as given below, where g_{m21} and g_{m24} are the transconductances of transistors M₂₁ and M₂₄:

$$r_{ob} = \frac{1}{g_{m21}(1 + \beta) + g_{m24}}$$

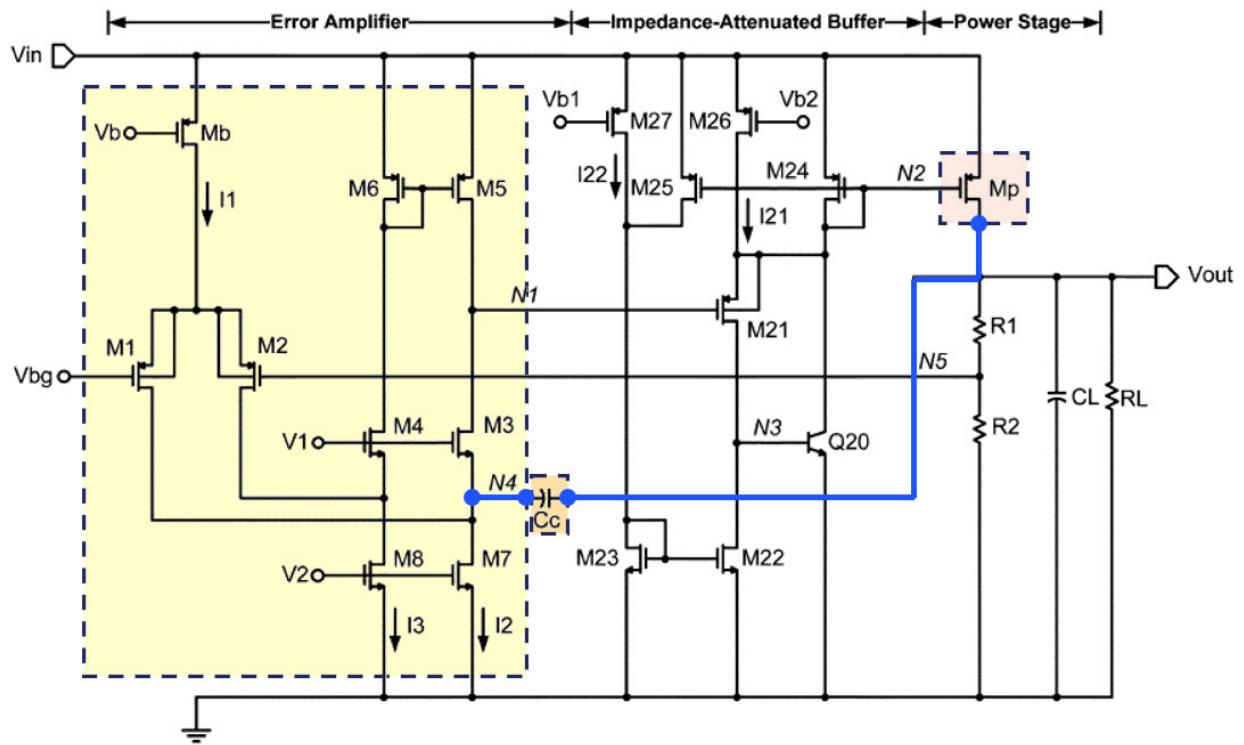
(EX1004, 1734.) Al-Shyoukh explains that this lowers the quiescent current needed at M₂₁, meaning M₂₁ itself can be a smaller transistor, with higher impedance. (*Id.*; EX1002 ¶¶ 79-80.) A POSITA would therefore have understood that Al-Shyoukh's gm-boost circuit allows for its buffer driver's input impedance to increase.

Claim 4 The voltage regulator according to claim 2, wherein the gm-boost circuit enables the current buffer driver to have a large gm value.

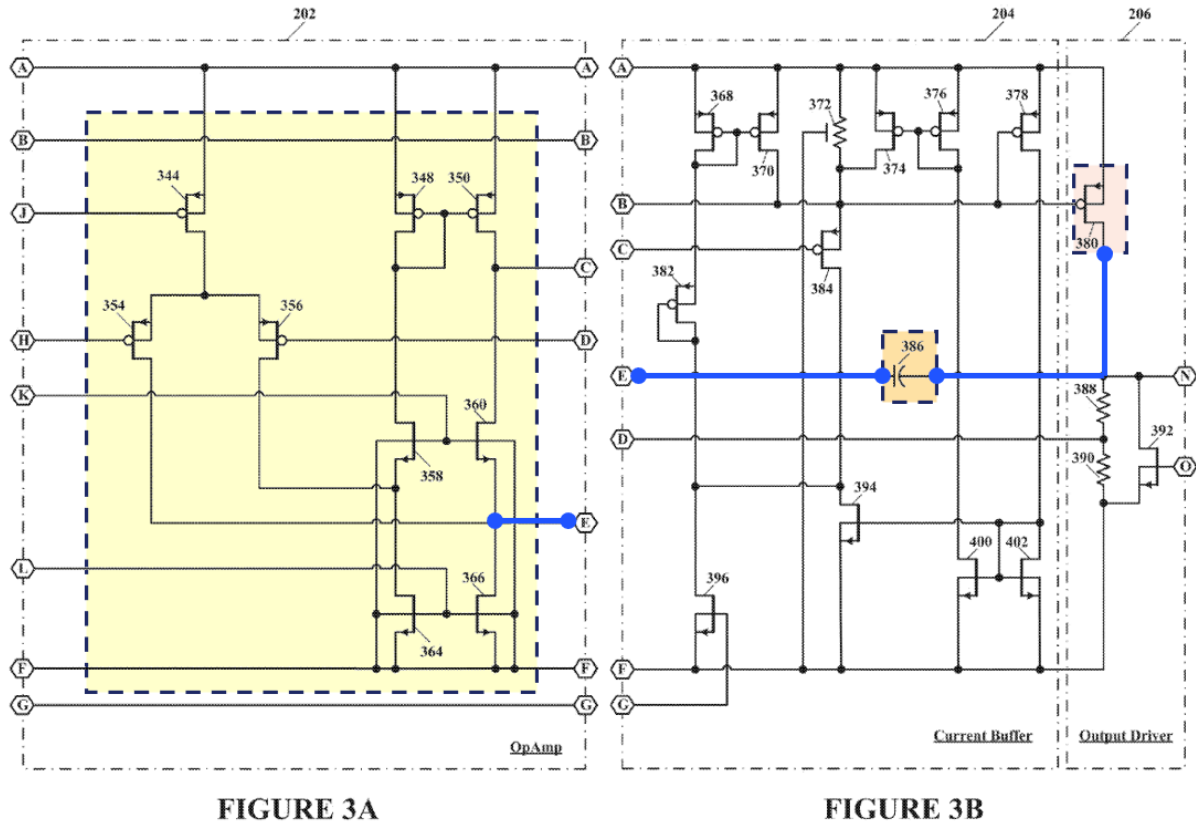
The '074 patent does not explain what “large” means in claim 4. To the extent Patent Owner contends that “enables the current buffer driver to have a large gm value” should be read to mean “increases the gm value of the current buffer driver,” Al-Shyoukh discloses claim 4 because its gm-boost circuit increases the gm value of the buffer driver M_{21} by increasing its current through the feedback mechanism comprising transistors M_{24} and M_{25} . (EX1002 ¶¶ 41-47, 53-59, 81; EX1004, 1734-35; *see also* Sections IV.A.1, IV.A.3, 1[b], 1[c], *supra*.)

Claim 5 The voltage regulator according to claim 1, further comprising a compensation capacitor coupled between the output power driver and a cascode node of the operational amplifier.

Al-Shyoukh’s LDO includes a compensation capacitor C_c (shown in orange below) coupled between the output power driver (red) and the operational amplifier (yellow):



(EX1004, Fig. 8 (annotated); *see also* EX1002 ¶¶ 82-85.) Capacitor C_c provides “current-buffer (or cascode-Miller) frequency compensation” to split “two poles p_1 at N_1 and p_o at the LDO output in order to achieve stability in the full range of the load current.” (*Id.*, 1735.) A POSITA would have recognized node N_4 , where C_c couples to the amplifier, as a cascode node because it is coupled to the output of M_3 , which is part of the cascode device in the amplifier’s “single-stage folded-cascode structure.” (*Id.*; *see also* EX1002 ¶ 84.) The ’074 patent notably discloses the same topology:



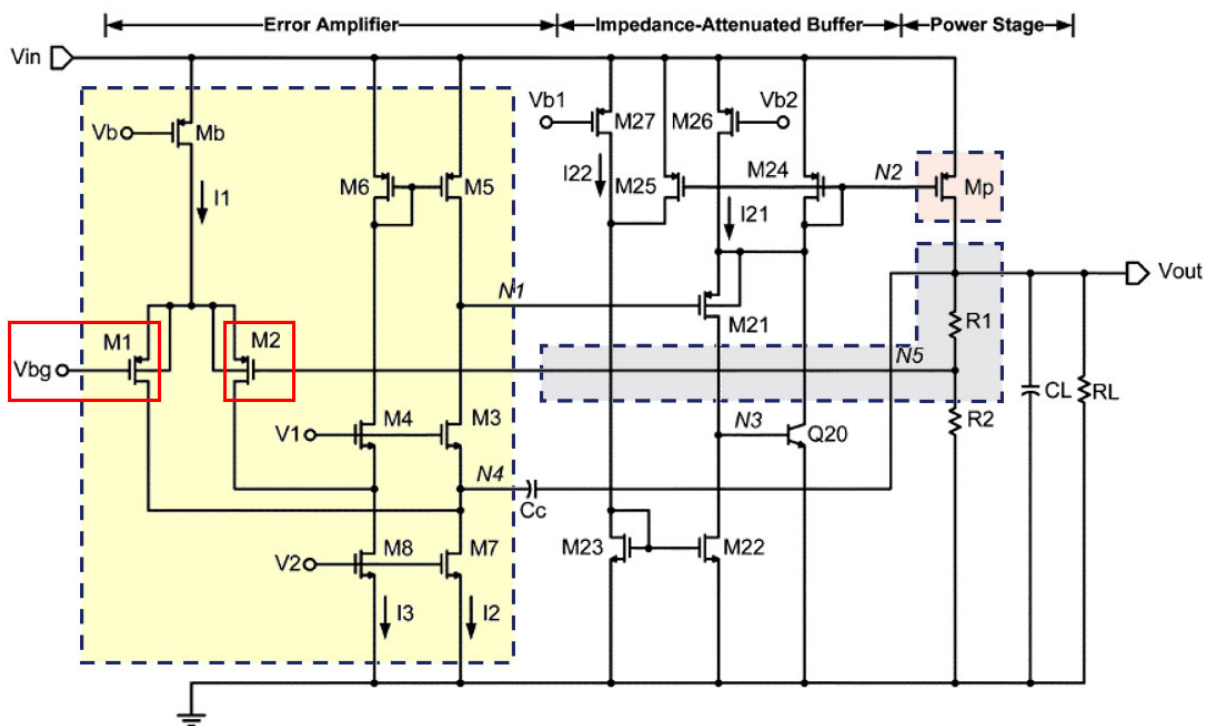
(EX1001, Figs. 3A, 3B (annotated).) Compensation capacitor 386 couples at node E to transistors 354 and 360 of the amplifier the same way C_c in Al-Shyoukh couples at N_4 to transistors M_1 and M_3 . (EX1002 ¶ 85.)

Claim 6 The voltage regulator according to claim 1, wherein the voltage regulator is a low drop out (LDO) voltage regulator.

Al-Shyoukh “presents a low-dropout regulator (LDO).” (EX1004, 1732.)

Claim 7 The voltage regulator according to claim 1, wherein the operational amplifier has a first input adapted for coupling to a voltage reference, and a second input coupled to the feedback loop.

Al-Shyoukh's operational amplifier (in yellow below) has a first input adapted for coupling to voltage reference V_{bg} and a second input coupled to the feedback loop discussed above under 1[g] (gray):



(EX1004, Fig. 8 (annotated); EX1002 ¶ 87.)

Claim 8 The voltage regulator according to claim 1, wherein the operational amplifier is a low gain and high bandwidth amplifier.

The '074 patent does not explain what “low” or “high” means in claim 8. To the extent Patent Owner contends that “a low gain and high bandwidth amplifier” is

“optimized for high bandwidth with a commensurate reduction of gain,” it would have been obvious to use such an amplifier with Al-Shyoukh. (EX1002 ¶¶ 88-94.)

It was well understood that gain and bandwidth are characteristics that trade off with each other in an operational amplifier. (*Id.* ¶ 89.) Determining that tradeoff was a basic step in implementing an op-amp, with some designs necessarily having lower gain and higher bandwidth than others. (*Id.* ¶ 90.) Thus, implementing an operational amplifier in Al-Shyoukh that was “optimized for high bandwidth with a commensurate reduction of gain” would have been a simple matter of design choice that a POSITA would have been well equipped to make. (*Id.*)

Moreover, the benefits of using a high-bandwidth operational amplifier for an LDO were well known. (*Id.*) Ha, for example, explains that bandwidth is important “in voltage regulator design,” and that the higher the bandwidth, “the more quickly it can react to changes in input and power supply.” (EX1007, 8.) Ye also notes that a relatively low-gain op-amp with high gain-bandwidth product improves power efficiency for a high-bandwidth closed-loop circuit (*e.g.*, an LDO). (EX1008, 96-97; EX1002 ¶ 92.) Because Al-Shyoukh shares these concerns (*see, e.g.*, EX1004, 1732 (power efficiency), 1734-35 (fast response to load changes)), a POSITA would have been motivated to optimize its error amplifier for high bandwidth. (EX1002 ¶¶ 92-93.)

Alternatively, from the parallel district court proceeding, Aptiv understands Patent Owner to argue that a folded cascode operational amplifier with a single stage of gain (comprising a differential input and a cascode load) is necessarily a low gain and high bandwidth amplifier under claim 8. This would make Al-Shyoukh's error amplifier a low gain and high bandwidth amplifier, because it has a "single-stage folded-cascode structure." (EX1004, 1735; *see also* EX1002 ¶ 94.)

Claim 9 The voltage regulator according to claim 8, wherein the low gain and high bandwidth amplifier is a folded-cascode amplifier.

Al-Shyoukh's error amplifier has "a single-stage folded-cascode structure"—the same structure, in fact, as the '074 patent's amplifier, as shown below:

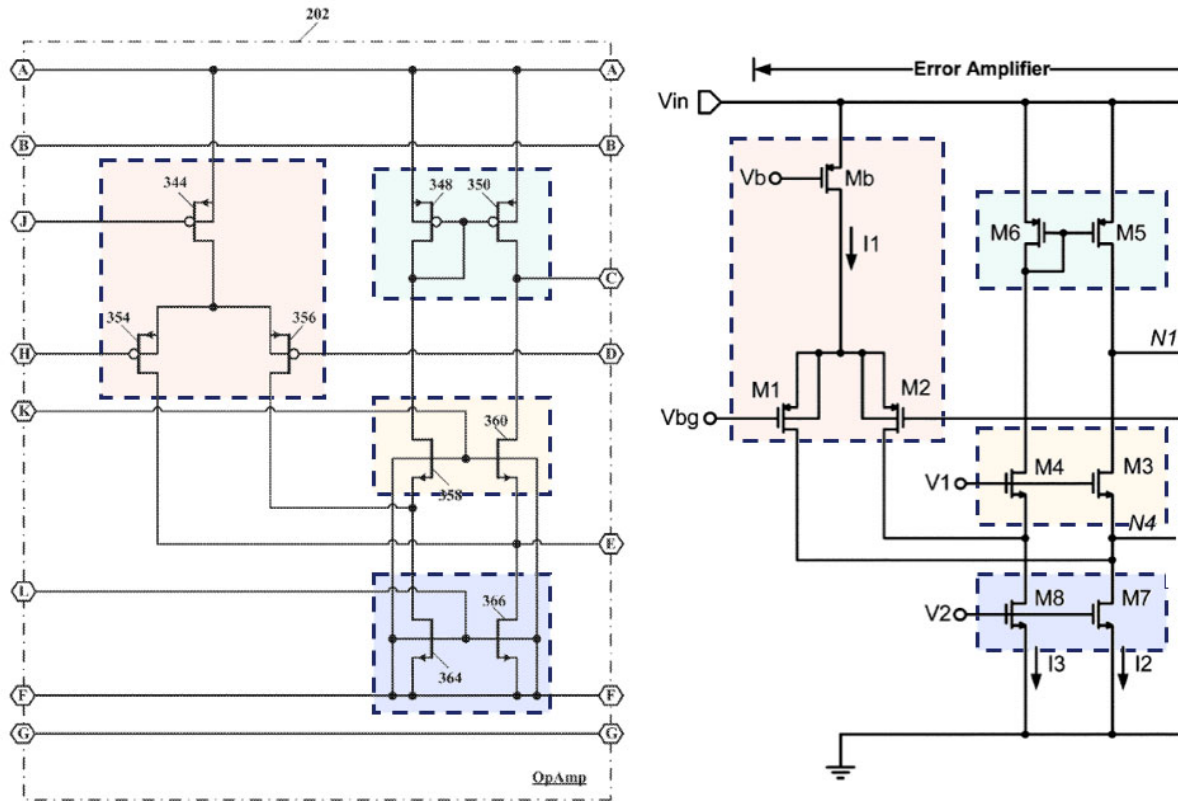


FIGURE 3A

(EX1001, Fig. 3A (annotated); EX1004, 1735, Fig. 8 (excerpted and annotated); EX1002 ¶ 95.) Al-Shyoukh thus renders claim 9 obvious.

Claim 10 The voltage regulator according to claim 9, wherein the operational amplifier comprises diode connected PMOS transistors for lowering an output impedance of the folded-cascode amplifier.

Al-Shyoukh's folded-cascode amplifier includes the claimed diode connected PMOS transistor M₆ for lowering the amplifier's output impedance:

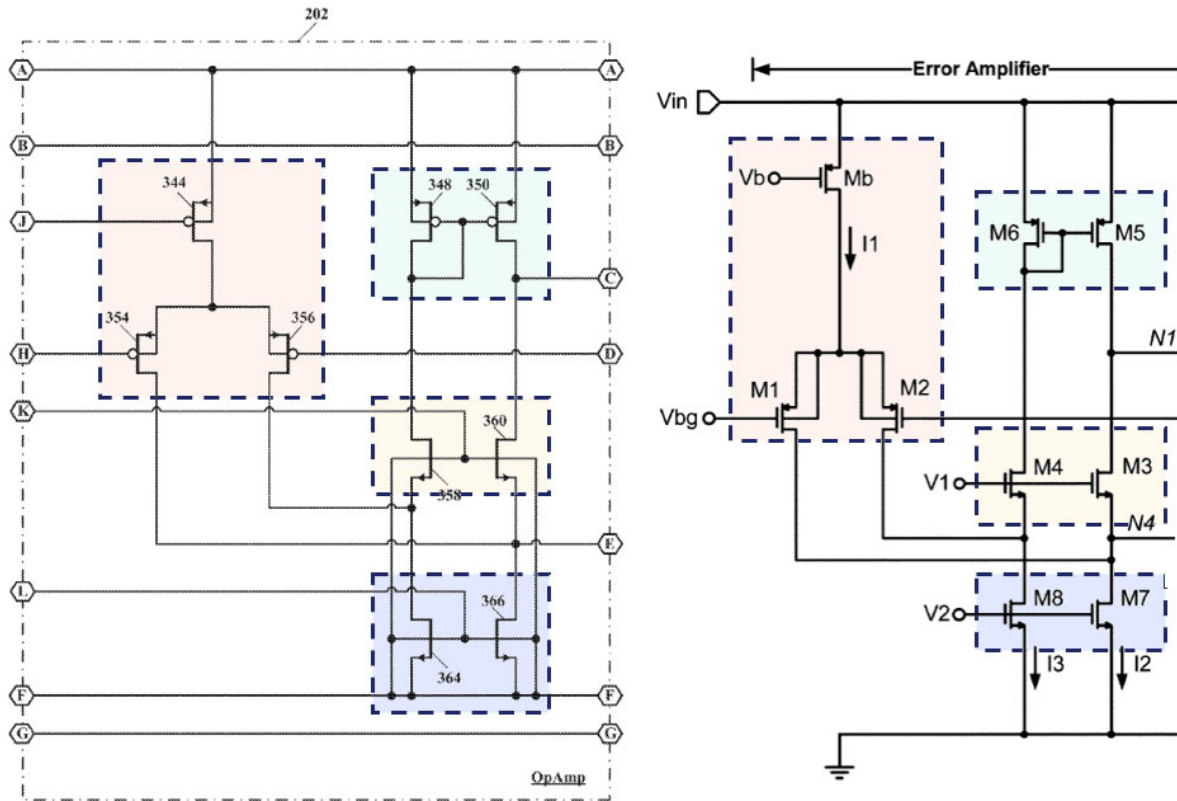


FIGURE 3A

(EX1001, Fig. 3A (annotated); EX1004, 1738, Fig. 8 (excerpted and annotated); EX1002 ¶ 96.) As shown here, Al-Shyoukh’s diode-connected PMOS transistor M_6 corresponds directly to the patent’s diode-connected PMOS transistor 348. (EX1002 ¶ 96.) Furthermore, Al-Shyoukh explains that in its amplifier includes “a simple diode-connected active load using transistors M_5 and M_6 .” (EX1004, 1738; *see also* EX1002 ¶ 96.) Thus, Al-Shyoukh discloses claim 10.

Claim 11 The voltage regulator according to claim 1, wherein the current buffer driver is an operational transconductance amplifier (OTA).

Al-Shyoukh as modified by Stanescu includes a current buffer driver that is an operational transconductance amplifier. Stanescu discloses an LDO that uses an OTA as the buffer driving the output power stage, replacing the prior art op-amp, as shown in green below:

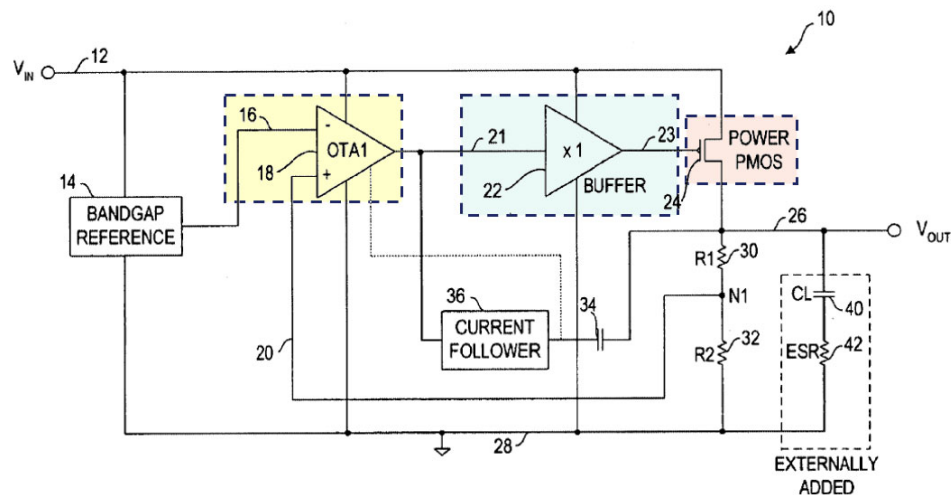


FIG. 1 (PRIOR ART)

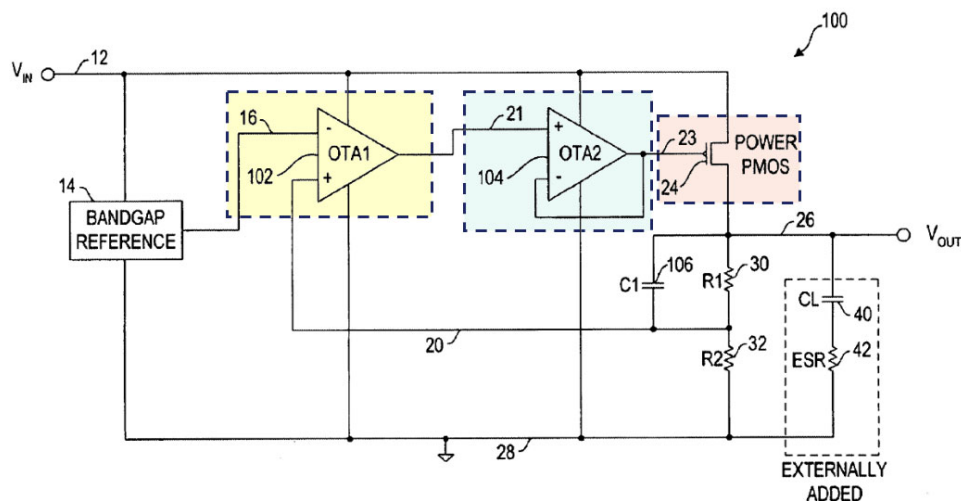
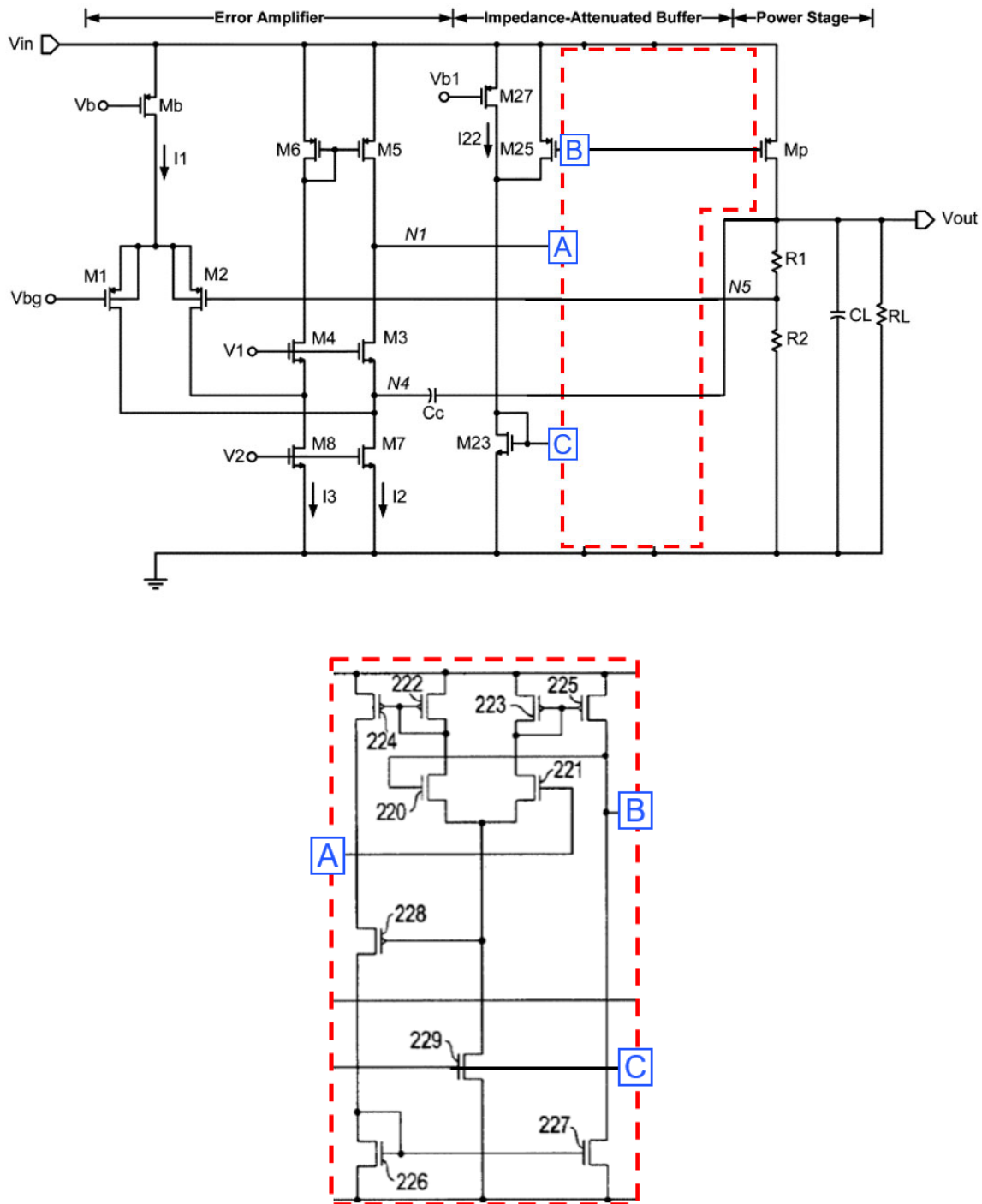


FIG. 2

(EX1006, Figs. 1, 2 (annotated).) Stanescu recommends this OTA because the prior art buffer could suffer from “limited closed-loop bandwidth” as well as a “non-ideal transient response, even at a low ESR, due to a low slew-rate.” (*Id.*, 2:44-53; *see also* EX1002 ¶ 98.) In addition, a POSITA would have recognized that, as a voltage follower, Stanescu’s OTA provides unity gain, and that unity gain is advantageous in an LDO because it has low output impedance and helps to keep the output voltage constant. (EX1002 ¶ 98.)

A POSITA would have been motivated by Stanescu to modify Al-Shyoukh to use an OTA as the buffer driver in the Al-Shyoukh LDO. (EX1002 ¶ 99.) Stanescu is analogous art to Al-Shyoukh because it is directed to an LDO for portable battery-powered devices (*see* EX1006, 1:17-28) that saves power by lowering the quiescent current (*see id.*, 7:64-8:3). Thus, a POSITA would have found the advantages of Stanescu’s OTA readily applicable to Al-Shyoukh’s LDO. (EX1002 ¶ 99.) The low output impedance of an OTA with unity gain feedback, for example, would have been helpful toward Al-Shyoukh’s goal of lowering the buffer’s output impedance. (*Id.*) Likewise, the unity gain of Stanescu’s OTA would have helped Al-Shyoukh’s LDO in maintaining the desired output voltage. (*Id.*)

An exemplary combined circuit using Stanescu’s OTA is shown below:



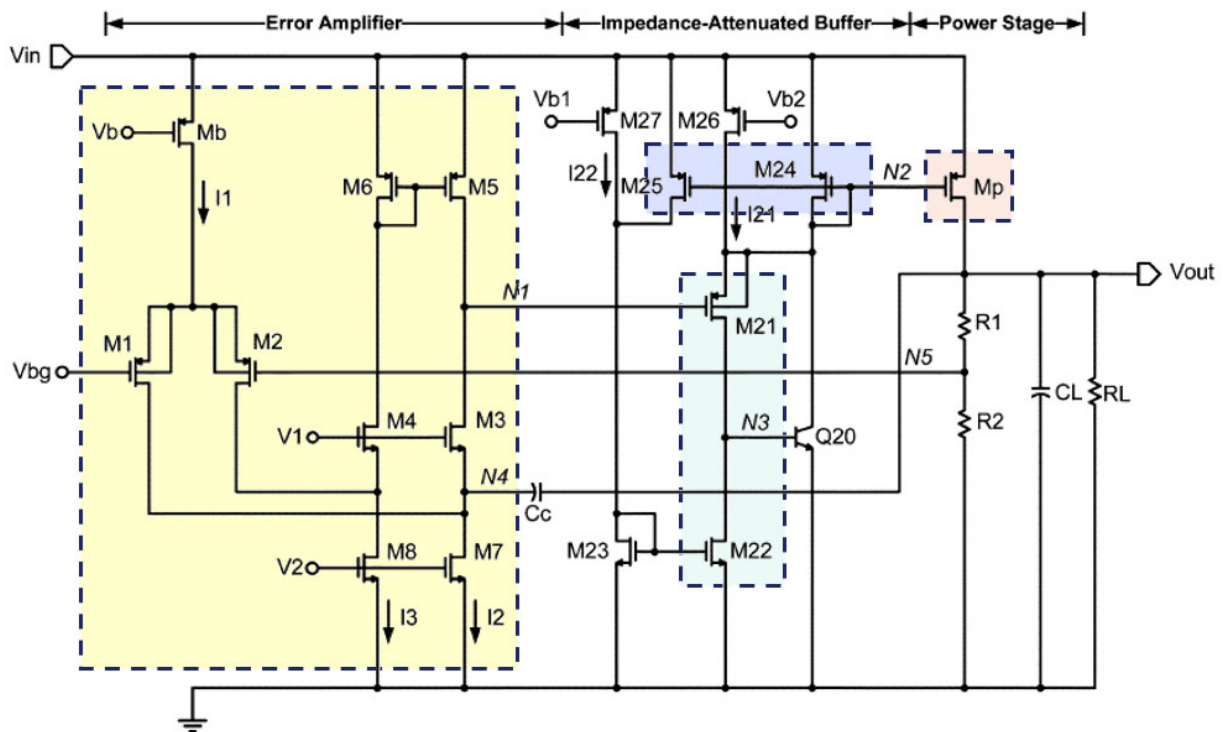
(EX1004, Fig. 8 (modified); EX1006, Fig. 3 (excerpted and modified); *see also* EX1002 ¶ 100.) The first figure is Al-Shyoukh's LDO, modified to show how the OTA would fit in. (EX1002 ¶ 100.) The second figure is Stanescu's OTA. (*Id.*) In

the combined circuit, transistor 221 would receive an input from A (Al-Shyoukh's N_1); the output of the OTA would couple to Al-Shyoukh's transistor M_{25} and the output driver M_p at B; and transistor 229 would mirror to transistor M_{23} across C. (*Id.*)

This circuit preserves Al-Shyoukh's feedback mechanism because M_{25} (like transistor M_{24} in the unmodified Al-Shyoukh circuit) would sense a current change at the output transistor through B. For example, if the current of M_p increases, then the voltage at B would drop, and the current at M_{25} would increase, increasing the current at M_{23} , and thus the current at 229. (*Id.* ¶ 101.) This would increase current in 220 and 221, from which 229 draws current, boosting the gm of the OTA/buffer. (*Id.*) A POSITA would have arrived at the above circuit or an equivalent one without undue experimentation. (*Id.*)

Claim 12 The voltage regulator according to claim 1, wherein the current feedback circuit senses a current change at the output power driver.

Al-Shyoukh's current feedback circuit senses a current change at its output power driver. As explained above under 1[f], the current feedback circuit (shown in blue below) comprises M_{24} and M_{25} , and M_p is the output power driver (red):



(EX1004, Fig. 8 (annotated).) The gate of each of these transistors is connected to node N_2 . (*Id.*; see also EX1002 ¶ 102.) When the current through M_p changes, the transistor's source-gate voltage changes in the same direction. (EX1002 ¶ 102.) The transistors of the current feedback circuit then sense that voltage change on N_2 , as claimed. (*Id.*)

Claim 13 The voltage regulator according to claim 1, wherein the current feedback circuit provides transient enhancement for improved load regulation.

Al-Shyoukh's current feedback circuit seeks to reduce the "maximum output-voltage variation" during "load transients even if a small output capacitor is used." (EX1004, 1732; see also *id.*, Title.) It does so by "improv[ing] the slewing of the gate drive at N_2 during load transients." (*Id.*, 1734-35; 1738-40 (experimental results

showing improvement).) A POSITA would have considered this improved transient response—discussed in detail above (*see* Section IV.A.1, *supra*)—to be a “transient enhancement for improved load regulation.” (EX1002 ¶¶ 103-105.)

Claim 14 The voltage regulator according to claim 1, wherein the current feedback circuit provides a feedback voltage from an output voltage node.

The '074 patent does not explain what “feedback voltage” or “output voltage node” means in claim 14. The only appearance of “feedback voltage” outside of the claim language (or the summary section that merely repeats the claim language) is at column 5, which states that “feedback network 212 provides feedback voltage to one differential input (transistor 356, FIG. 3A, node D) of the OpAmp.” (EX1001, 5:29-31.) This concerns the feedback loop of 1[g], not the current feedback circuit. As for “output voltage node,” the phrase does not appear at all outside of the claims and summary section, although “output node” appears once, describing “output node N.” (*Id.*, 5:37.) But again, this relates to the feedback loop. No component of the “current feedback circuit” connects to output node N, but node D, which is part of the feedback loop, does, as shown below:

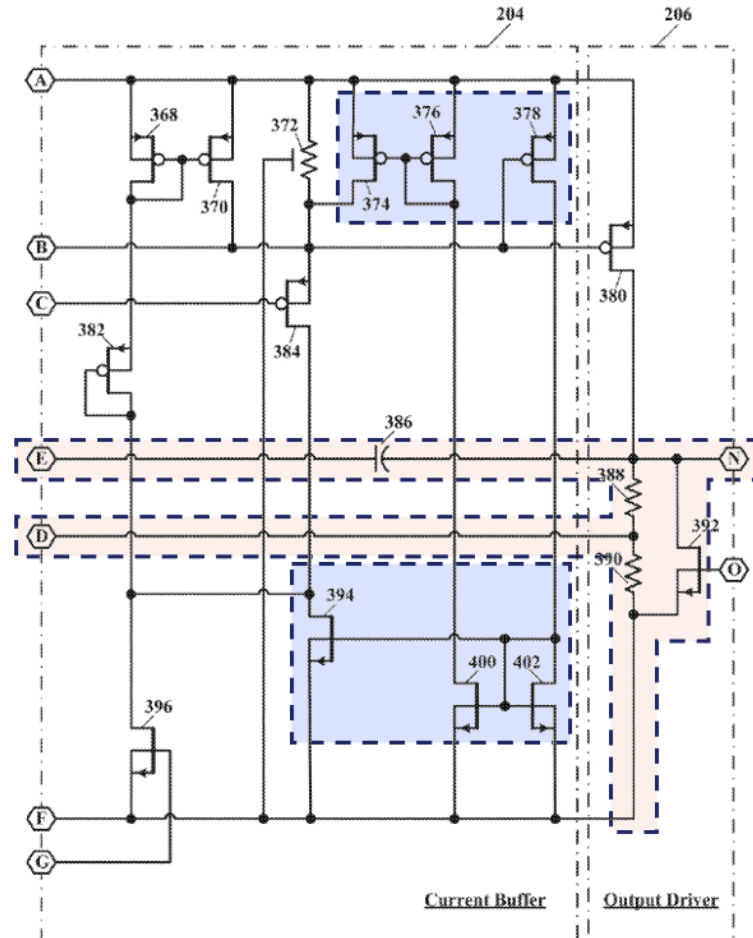
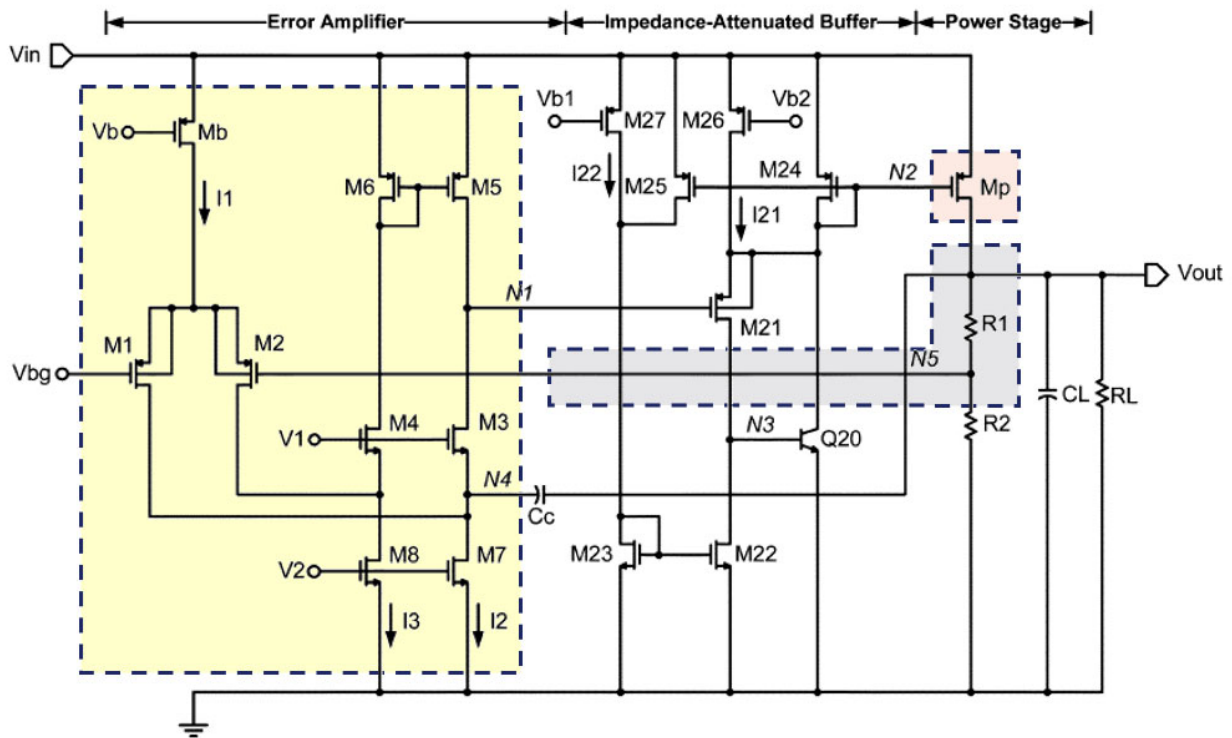


FIGURE 3B

(*Id.*, 5:13-14, Fig. 3B (annotated); EX1002 ¶ 107.) Thus, a POSITA would have been unable to make sense of claim 14 without assuming that the applicant meant to refer to 1[g]’s “feedback loop” rather than “the current feedback circuit.” (EX1002 ¶¶ 106-107.)

Under this interpretation, Al-Shyoukh discloses claim 14 because its feedback loop (shown in gray below) provides a feedback voltage (the voltage at N₅, which is the output voltage V_{out} less the drop across resistor R₁) from the output voltage node to the error amplifier (yellow):



(EX1004, Fig. 8 (annotated); EX1002 ¶ 108.)

To the extent Patent Owner contends that the claim was actually meant to refer to the “current feedback circuit,” a POSITA reviewing the rest of the specification would have understood “an output voltage node” to mean any node that provides a feedback voltage, because the ’074 patent does not identify any specific output node associated with the current feedback circuit. (EX1002 ¶ 109.) Under such a reading, Al-Shyoukh discloses claim 14 because its current feedback circuit provides a voltage at node N₂, that voltage being a “feedback voltage” because it responds to changes in the current of the output power driver M_p. (*Id.*; see also claim 12, *supra*.)

Claim 15 The voltage regulator according to claim 1, wherein the current buffer driver has a low output impedance.

Al-Shyoukh's current buffer driver has low output impedance. In fact, one of Al-Shyoukh's goals is to reduce the buffer's output impedance. (See EX1004, 1733 ("The proposed BIA technique greatly reduces the output resistance of the buffer through dynamically-biased shunt feedback."); *id.*, 733-35 (current feedback circuit reduces output resistance r_{ob}); EX1002 ¶ 110; *see also id.* ¶ 111 (explaining that a POSITA would have understood "output resistance" to mean "output impedance" in this context).)

Claim 16 The voltage regulator according to claim 1, further comprising capacitors in the biasing circuit for improving noise immunity thereof.

It would have been obvious to a POSITA to use capacitors in the bias circuit for Al-Shyoukh's LDO to improve noise immunity. (EX1002 ¶¶ 112-15.)

Referred to as "decoupling capacitors" or "bypass capacitors," such capacitors were well-understood and routinely used to insulate a circuit from noise caused by other circuit components. (*Id.* ¶¶ 113-14.) Popovich, for example, teaches that the "power and signal integrity problems in the overall system" caused by noise from one component propagating to another can be solved using "decoupling capacitors" placed at different points in the circuit. (EX1009, 12 & 217.) In addition, Wang teaches that in "common battery-powered applications," the bias voltage is often connected to a power supply by "a suitable network of decoupling capacitors."

(EX1010, 4:59-61; *see also id.*, 2:64-3:1.) And MIC59300 similarly recommends “[s]mall ceramic capacitors from VBIAS-to-ground [to] help reduce high frequency noise from being injected into the control circuitry from the bias rail.” (EX1011, 10; *see also* EX1002 ¶ 114.)

In short, a POSITA would have recognized that decoupling capacitors were a conventional solution for reducing noise, especially in bias circuits that must reliably output a fixed voltage. (EX1002 ¶ 115.) Using these capacitors in Al-Shyoukh’s bias circuit was therefore obvious.

Claim 17 The voltage regulator according to claim 1, wherein the voltage regulator is a USB voltage regulator.

It would have been obvious to use Al-Shyoukh’s voltage regulator as a USB voltage regulator. (*Id.* ¶¶ 116-18.) Al-Shyoukh teaches that “[p]ower management is essential in all battery-powered portable devices,” and that LDOs like its own were among “the most critical power management modules.” (EX1004, 1732.) And, as a POSITA would have known, USB devices often required the host device to supply power, making power management a key design concern. (EX1002 ¶ 117; *see also* EX1012, 2:29-33 (proposing a USB voltage regulator as part of a method for saving power).) Furthermore, a POSITA would have considered “regulated low-noise and precision supply voltages for noise-sensitive analog blocks”—additional benefits of an LDO identified by Al-Shyoukh—to be advantageous for USBs. (EX1004, 1732;

EX1002 ¶ 118.) Thus, it would have been obvious to use Al-Shyoukh's LDO as a USB voltage regulator.

Claim 18 The voltage regulator according to claim 1, wherein the current buffer driver has low input impedance and provides a high frequency pole that does not substantially affect the voltage regulator dominant pole.

Al-Shyoukh's buffer driver discloses claim 18. Al-Shyoukh discusses three poles at "the output of the error amplifier (N_1), the output of the buffer (N_2), and the output of the LDO (V_{out})," given by the equations below:

$$\begin{aligned}p_1 | N_1 &= 1/(r_{o1}C_1) \\p_2 | N_2 &= 1/(r_{ob}C_p) \\p_o | V_{out} &= 1/(R_{oeq}C_L)\end{aligned}$$

(EX1004, 1733.) r_{o1} is the error amplifier's output resistance, C_1 is "the equivalent capacitance at N_1 , which is dominated by the input capacitance of the buffer C_{ib} ," and r_{ob} is the output resistance of the buffer. (*Id.*; EX1002 ¶ 119.) Al-Shyoukh states that "to achieve single-pole loop response," p_1 and p_2 should be at frequencies "much higher than the unity-gain frequency of the regulation loop," which can be done by making C_{ib} (and thus C_1) and r_{ob} small. (EX1004, 1733; EX1002 ¶ 120.) And as explained above, Al-Shyoukh's feedback circuit decreases r_{ob} . (*See* Section IV.A.1, claim 3, *supra*; *see also* EX1002, ¶ 120; EX1004, 1734-36.) Thus, a POSITA would have understood that Al-Shyoukh's buffer driver provides high-frequency poles p_1 and p_2 that do not substantially affect the dominant pole, p_o . (EX1002 ¶¶ 119-121;

see also EX1004, 1740 (noting that the proposed LDO exhibits a single pole within the unity-gain bandwidth of the regulation loop and a good phase margin”).)

The '074 patent does not explain what it means for the current buffer driver to have “low input impedance” under claim 18. But as noted under claim 3, Patent Owner has interpreted (in the district court proceeding) “current buffer driver input impedance” to mean the input impedance at the point where the operational amplifier connects to the current buffer driver. Applying this same understanding to claim 18, a POSITA would have found that Al-Shyoukh discloses it. (EX1002 ¶¶ 122-23.) Low output impedance was a well-known property of operational amplifiers. (*Id.* ¶ 123.) A POSITA would also have recognized that a low output impedance for the amplifier would be desirable, as this would shift pole p_1 to a higher frequency, consistent with Al-Shyoukh’s goal of setting the pole higher than the unity-gain frequency. (*Id.*) Thus, it would have been obvious to implement Al-Shyoukh’s LDO such that the impedance at node N_1 —the point at which the operational amplifier connects to the buffer driver—has low impedance. (*Id.*)

B. Ground 2

The challenged claims were obvious in view of two related references that describe the same LDO:

- U.S. Patent No. 6,046,577 (“Rincon-Mora”); and

- Gabriel A. Rincon-Mora, “A Low-Voltage, Low Quiescent Current, Low Drop-Out Regulator,” *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 1 (Jan. 1998) (the “Rincon-Mora Paper”).

These references (collectively, the “Rincon-Mora References”), in combination with Al-Shyoukh, Ivanov, and/or Stanescu, render obvious each claim of the ’074 patent. Each reference is prior art to the ’074 patent under at least pre-AIA Sections 102(a) and 102(b) or post-AIA Section 102(a)(1). Rincon-Mora, Ivanov, and Stanescu are also prior art under pre-AIA Section 102(e) or post-AIA Section 102(a)(2).

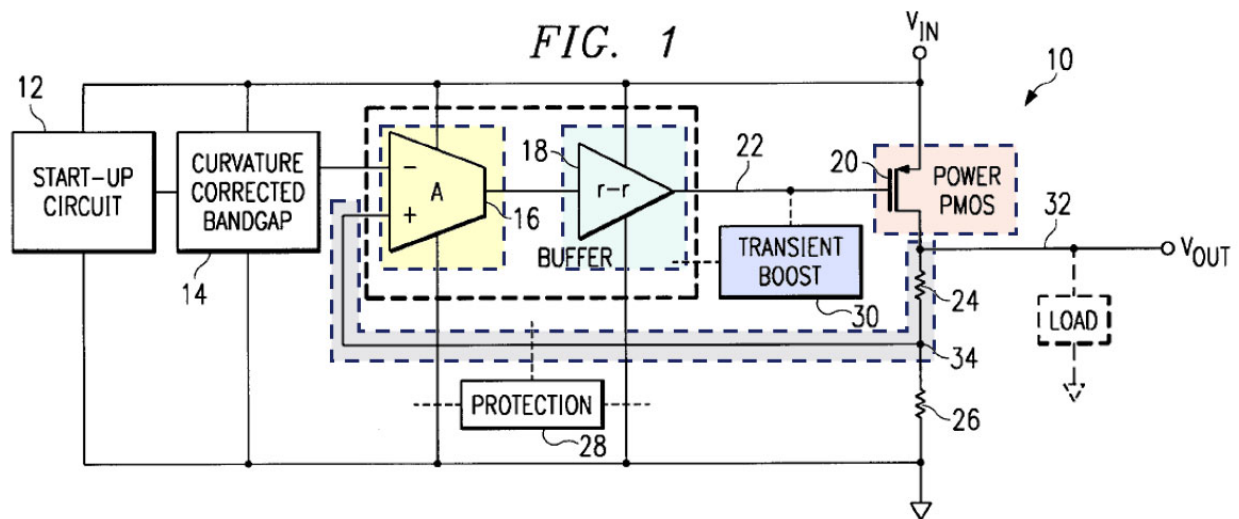
1. Summary of the Rincon-Mora References

The Rincon-Mora References describe an LDO that uses a “transient response boost circuit,” which provides a feedback mechanism to boost the gm of the LDO’s buffer driver. (EX1002 ¶¶ 126-37.)

Rincon-Mora explains that a known problem with conventional LDOs was an “output voltage ‘glitch’” that occurred with large changes in load. (EX1013, 1:31-33.) This was due to the “relatively large gate terminal of the LDO voltage regulator series-connected power pass transistor” (*i.e.*, output driver), which created a “slew-rate limited node” that was slow to respond to voltage changes. (*Id.*, 1:33-40.) While this could be “offset by adding more current,” increasing the quiescent current would have wasted power, which was especially undesirable in “portable, battery powered applications such as laptop computers, pagers[,] cellular phones and the like.” (*Id.*, 1:21-30, 1:41-49.) Thus, Rincon-Mora’s transient response boost circuit is designed

to “selectively apply current to a slew-rate limited node” while requiring “no standby current during zero output current load conditions.” (*Id.*, 1:12-17; *see also* EX1002 ¶¶ 127-30.) In particular, the circuit pushes the parasitic pole at the gate of the pass device to a higher frequency, improving the phase margin and allowing the LDO to remain stable over a broader range of output capacitors. (*Id.* ¶¶ 129-30; EX1013, 4:13-61.) Rincon-Mora thus achieved the purported benefit of the ’074 patent (an increased “range of external capacitors” (EX1001, 1:55-58)) in much the same way (by pushing the parasitic gate pole to a higher frequency (*id.*, 3:25-27)), but 16 years earlier. (EX1002 ¶¶ 129-31.)

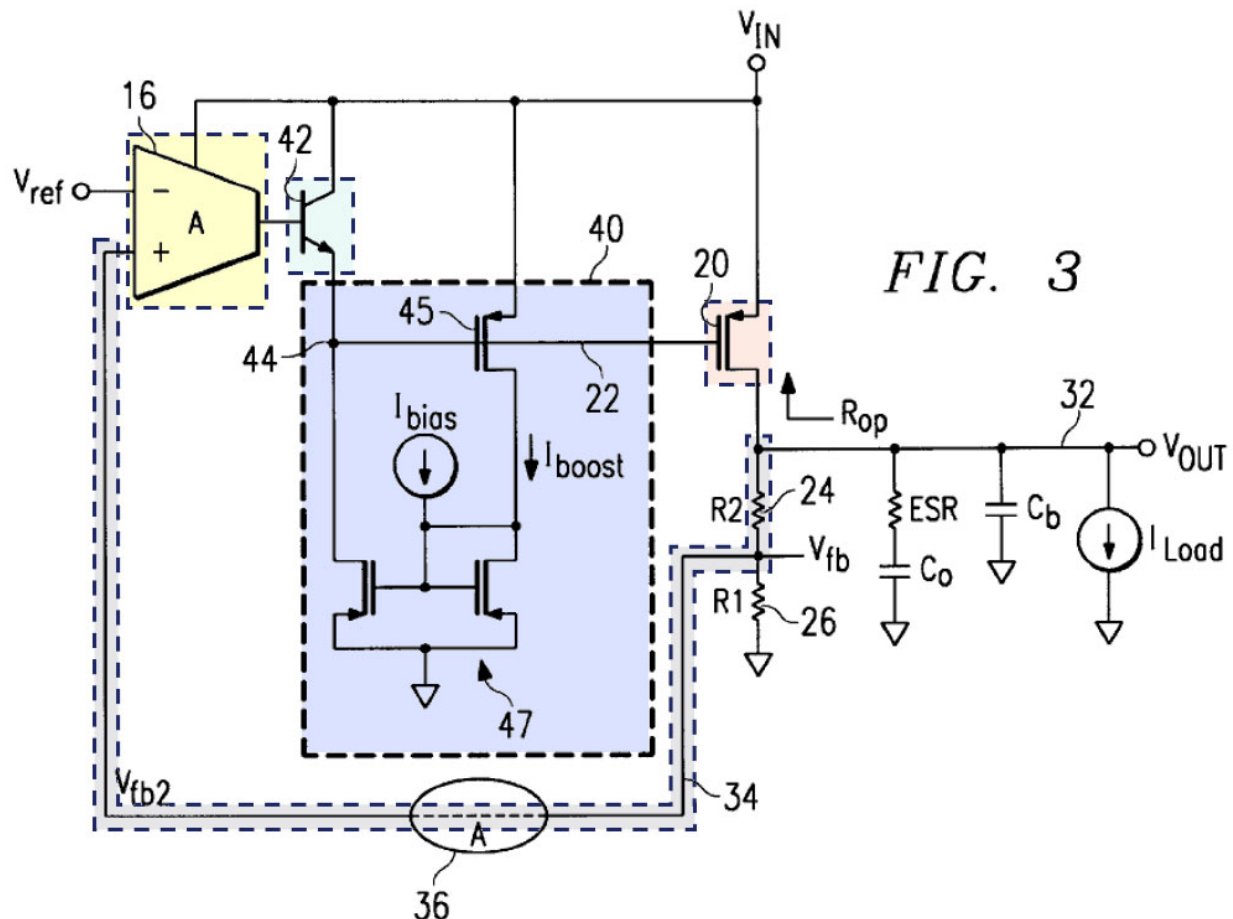
The high-level structure of Rincon-Mora’s LDO is shown below:



(EX1013, Fig. 1 (annotated).) The LDO includes a “start-up circuit 12” with “an external enabling input to a logic block,” and a “curvature corrected bandgap circuit 14” that can be “operatively monitored by the start-up circuit 12.” (*Id.*, 3:26-35.)

The bandgap circuit provides a reference signal to an input of the error amplifier 16 (shown in yellow), with the other input being a feedback input (gray) from the output driver transistor 20 (red). (*Id.*, 3:35-62.) The error amplifier outputs a signal to the buffer 18 (green) to supply a gate drive voltage to the output driver. (*Id.*, 3:39-43.) Finally, a transient boost circuit 30 (blue) is “coupled to the slew-rate limited node 22 at the gate of transistor 20.” (*Id.*, 3:55-58; *see also* EX1002 ¶¶ 132-34.)

An embodiment of this LDO is shown in greater detail below:



(EX1013, Fig. 3 (annotations consistent with Fig. 1 above).) In this case, the error amplifier is “an operational transconductance amplifier (‘OTA’) in conjunction with

a buffer 42,” which is an NPN bipolar junction transistor (or “BJT”) whose emitter terminal is coupled to “node 44 at the input of the transient boost circuit 40,” and to the gate of the output transistor at node 22. (*Id.*, 4:33-40; *see also* EX1002 ¶ 135.)

The transient boost circuit is “a localized positive feedback loop to enhance transient capabilities.” (EX1013, 4:62-65.) At node 22, transistor 45 senses changes in the output transistor’s gate voltage, and delivers “a ratio of the current,” as set by its size relative to the output transistor, to “current mirror 47.” (*Id.*, 5:5-8.) Thus, if transistor 45 is sufficiently small, its quiescent current in a no-load state is negligible and thus power-efficient. (*Id.*, 5:4-10.) But when the LDO is suddenly loaded, the change in voltage causes transistor 45 to provide a boost current I_{boost} to the current mirror. (*Id.*, 5:10-16.) This aids the amplifier in “sinking more current” into the buffer driver transistor 42 due to the feedback loop established at node 44. (*Id.*) In short, Rincon-Mora’s transient boost circuit increases the output current, and thus g_m , of the buffer driver. (EX1002 ¶ 136.)

Because the Rincon-Mora Paper discloses substantially the same LDO, a POSITA implementing the LDO would have considered both of the Rincon-Mora References to understand the invention, including the transient boost circuit, fully. (*Id.* ¶ 137.)

2. Analysis

A POSITA would have found each claim of the '074 patent to be obvious over the Rincon-Mora References in view of Ivanov, Al-Shyoukh, and/or Stanescu.

Claim 1 A voltage regulator, comprising:

Rincon-Mora discloses a “low-dropout (‘LDO’) voltage regulator,” which is a voltage regulator. (EX1013, Abstract.)

[a] an operational amplifier;

Rincon-Mora’s LDO comprises an error amplifier, which a POSITA would have understood could be an operational amplifier. (*Id.*, 3:35-43, 7:19-21, Figs. 1, 3; *see also* EX1002 ¶¶ 139-40.) Rincon-Mora does not limit its error amplifier to a particular structure. Its claims simply recite “an error amplifier having first and second inputs and a reference output thereof,” where the output is coupled to the “control input” of an “output switching device” with “a buffer circuit interposed between said reference output of said error amplifier and said output switching device.” (EX1013, 7:19-44.) Thus, even the exemplary embodiment discussed in Rincon-Mora uses an OTA as the error amplifier, a POSITA would have understood that it could just as well be implemented as an operational amplifier without altering the material aspects of the LDO. (EX1002 ¶¶ 139-40.) Indeed, it was well known that an LDO’s error amplifier should have sufficient loop gain, and op-amps were known to have high gain. (*Id.* ¶¶ 52, 140.) Rincon-Mora thus renders 1[a] obvious.

[b] a gm enhanced current buffer driver;

Rincon-Mora's buffer driver is "gm enhanced" because the transient boost circuit, comprising transistor 45 and current mirror 47, increases its gm. (See Section IV.B.1, *supra*; EX1013, 3:38-43, 4:33-38, 5:10-13, 7:42-44, Fig. 3; *see also* EX1002 ¶¶ 126-36, 142-44.)

As discussed above under Ground 1 for this limitation, the patent describes its "current" buffer as a "source follower" that "creates a low impedance environment," which are two characteristics of *voltage* buffers. (EX1001, 4:36, 4:64-5:1; EX1002 ¶ 143; *see also* Section IV.A.3, 1[b], *supra*.) In any case, Rincon-Mora's buffer has the same characteristics: It is an "emitter follower" if implemented as a BJT (*see* EX1014, 37), functionally equivalent to a MOSFET being used as a source follower (EX1002 ¶ 144). A POSITA would also have understood that the buffer could be implemented as an NMOS source follower, because Rincon-Mora does not specify a particular structure, and an NMOS would have been a readily available and well-known option with recognizable benefits like cost savings. (*Id.* ¶ 141.) Either way, Rincon-Mora points out that its buffer should have "low input capacitance and low output impedance" to "isolate the large capacitor associated with the gate of the power PMOS transistor from the large resistance of the output of" the error amplifier

(EX1014, 42), like the patent’s buffer, which achieves low output impedance by separating “the poles seen on the big power output driver” (EX1001, 4:64-5:1). A POSITA would therefore have understood Rincon-Mora to disclose a “gm enhanced current buffer driver” in the same way the ’074 patent does.

[c] a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver;

Rincon-Mora’s LDO uses a biasing circuit coupled to the buffer driver to set a bias current I_{bias} that is mirrored in current mirror 47 to set a biasing ratio for gm-boost of the buffer driver. (EX1013, 3:55-62, 4:30-65, 7:35-41, Figs. 1, 3; EX1002 ¶¶ 145-49.)

As discussed under Ground 1 for this limitation, the ’074 patent describes a bias network that provides a current that is “ratio’ed in transistors 368 and 370” with a current provided by the feedback circuit. (EX1001, 5:15-24; Ex. 1002 ¶ 147; *see also* Section IV.A.3, 1[c], *supra*.) This is shown in the figure below; the current in transistor 368 (purple) is the sum of the bias current at transistor 396 (blue) and a feedback current that flows to transistor 394 (red):

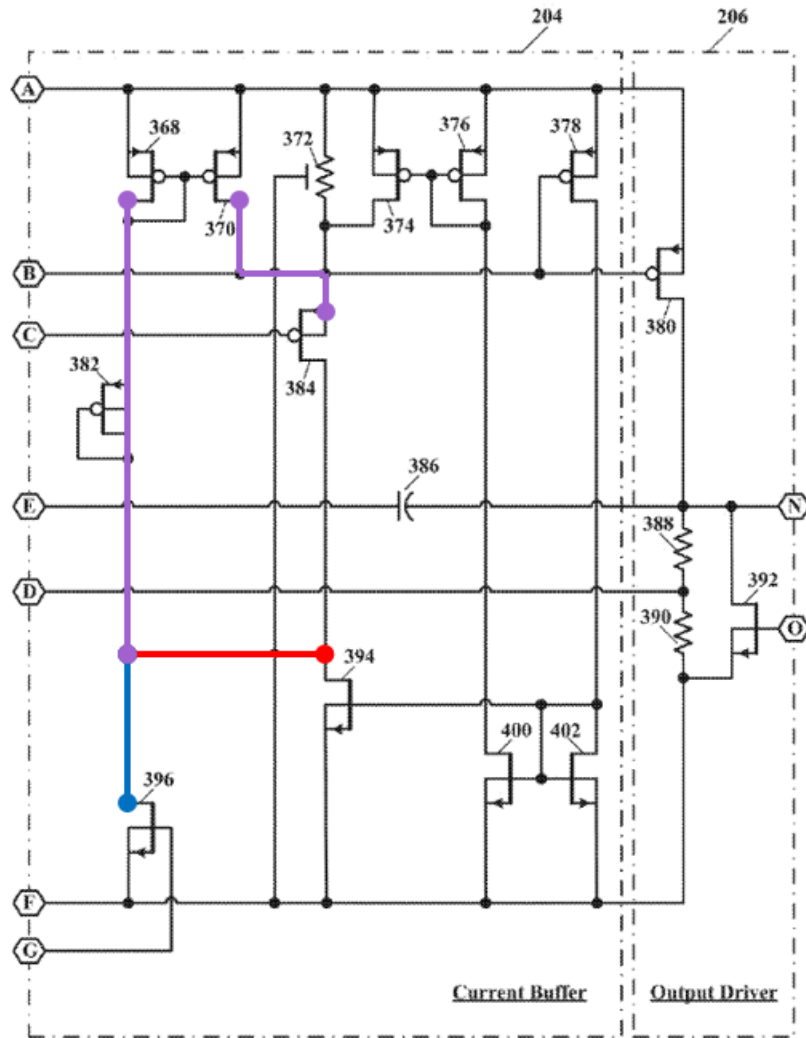
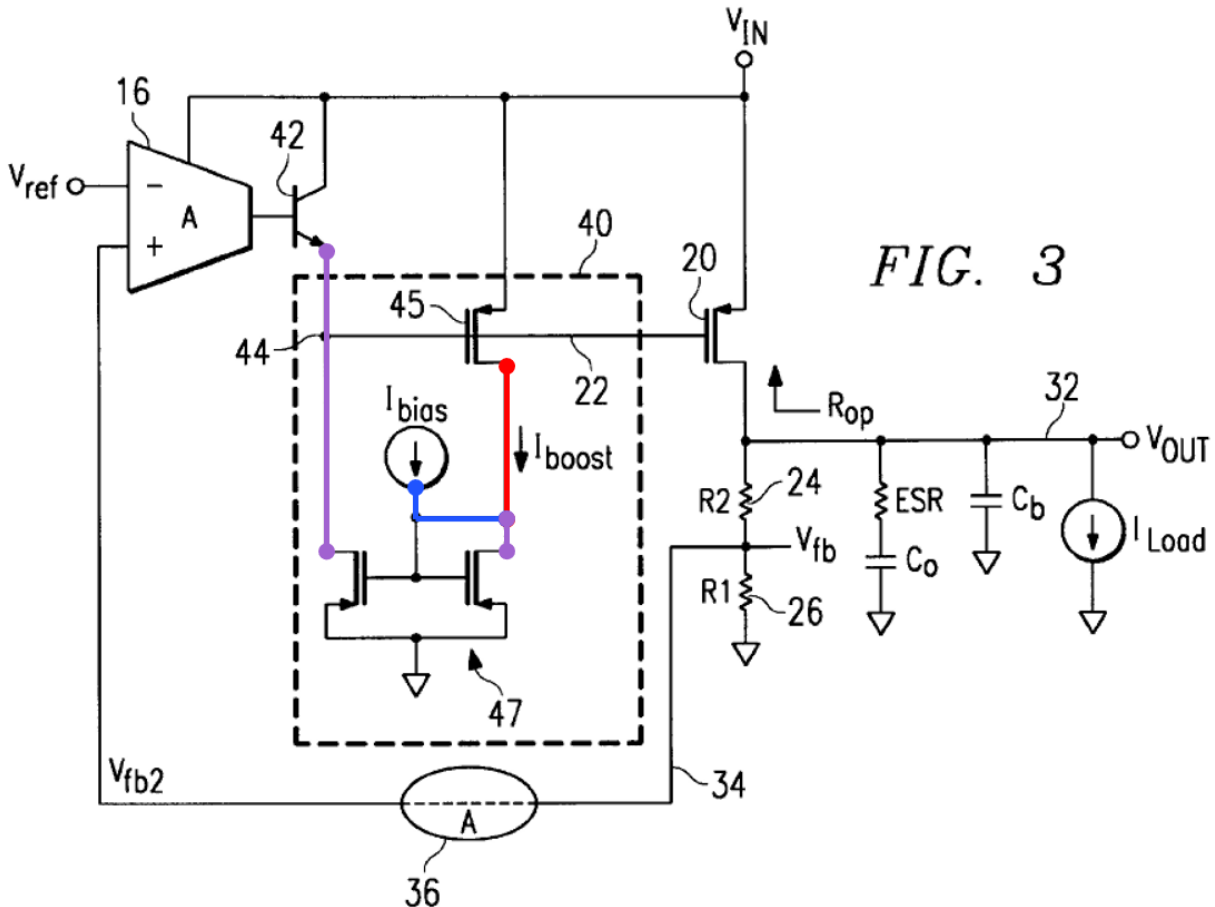


FIGURE 3B

(EX1001, Fig. 3B (annotated); *see also* EX1002 ¶ 147.)

The same occurs in Rincon-Mora's LDO. Shown below using the same color scheme is a sum current (purple) made up of a bias current I_{bias} (blue) and a current from feedback I_{boost} (red):



(EX1013, Fig. 3 (annotated); *see also id.*, 4:62-5:16; EX1002 ¶¶ 145-46; Section IV.B.1, *supra.*) This sum current is “ratio’ed” in current mirror 47. (EX1002 ¶¶ 146, 148.) And because the mirrored current is drawn from the buffer driver (transistor 42), the buffer driver receives a gm boost. (*Id.*; *see also* EX1014, 38.)

Alternatively, to the extent Patent Owner argues that “biasing ratio” should be understood to mean a ratio of current that the current buffer draws from DC relative to the current feedback circuit, Rincon-Mora discloses this limitation. A biasing circuit provides a bias current I_{bias} , and a POSITA would have understood that

adjusting the biasing circuit to set the value of I_{bias} would have allowed one to set a ratio of current from DC and current from feedback (I_{boost}). (EX1002 ¶ 149.)

[d] an enable/disable function to enable/disable the biasing circuit for reducing standby current;

As noted above under Ground 1, Aptiv understands Patent Owner to contend that 1[d] is not means-plus-function, but to the extent it is, the claimed function is to enable/disable the biasing circuit for reducing standby current, and the structure is the signal input line at node M of Figure 3. Under that construction, Rincon-Mora's LDO in combination with Ivanov discloses 1[d].

Rincon-Mora discloses the bias current I_{bias} , but does not prescribe any design for the biasing circuit. A POSITA would therefore have understood that the biasing circuit could be implemented according to conventional, well-understood methods, including Ivanov's. (EX1002 ¶¶ 150-61.)

Ivanov provides "a quick turn-on disable/enable bias control circuit" for use in "applications such as voltage regulators" so that the device's biasing circuitry can be kept in "a quiescent, low-power state until fully functional circuit operation is needed." (EX1005, 1:12-18, 6:47-52; Section IV.A.3, 1[d], *supra*.) As discussed above under Ground 1, key to this disable/enable mechanism is an external shutdown control circuit 15, which uses V_{SHUTDOWN} to enable or disable the biasing circuit through transistor M11, as shown below:

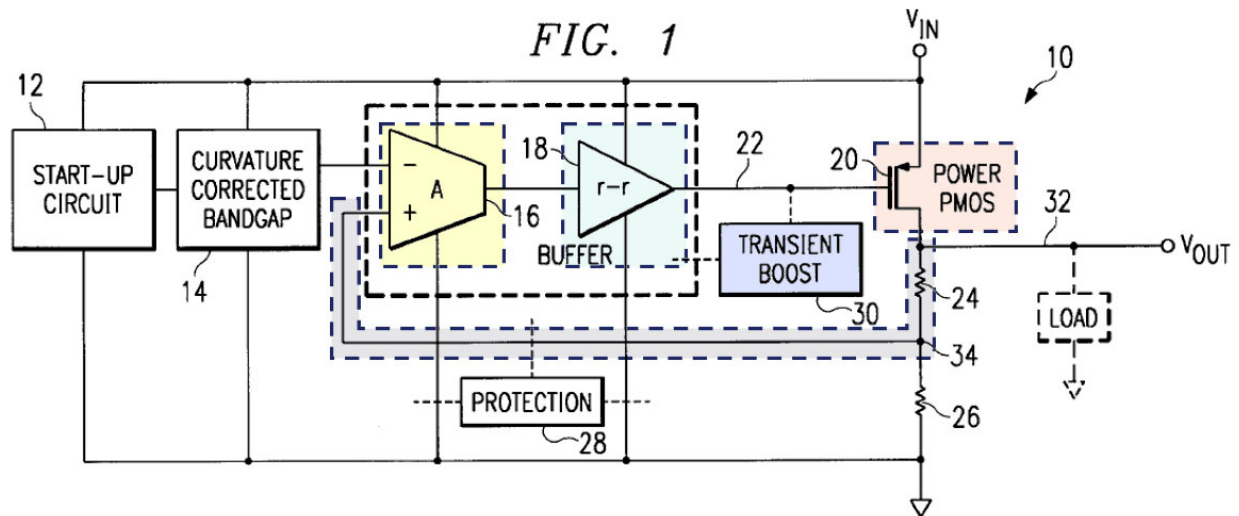
A POSITA would have been motivated to use Ivanov's disable/enable control mechanism for the biasing circuit for Rincon-Mora's LDO. Both Rincon-Mora and Ivanov are highly concerned with power efficiency, and Ivanov's mechanism saves power by shutting off unused circuitry. (*Compare* EX1013, 1:18-30 (noting that "standby and quiescent current flow are major concerns" in LDO design), 5:18-21 (explaining that a benefit of the proposed transient response boost circuit is that it is "power efficient" because "it only sinks current upon demand") *with* EX1005, 1:6-18 (proposing disabling not-in-use circuitry for "a quiescent, low-power state"); *see also* EX1014, 37 ("Thus, the biasing conditions for the case of zero load-current can be designed to utilize a minimum amount of current, which yields maximum current efficiency and prolonged battery life.").) In addition, Ivanov specifically states that voltage regulators were an intended application for its circuit. (EX1005, 6:47-54; *see also* EX1002 ¶ 157.)

Furthermore, a POSITA could have integrated Ivanov's biasing circuit and its enable/disable function with Rincon-Mora's LDO without undue experimentation because Ivanov provides a ready-to-use circuit. (EX1002 ¶¶ 158.) As a POSITA would have recognized, Ivanov's components could be chosen so that I_{BIAS+} is set to the desired value of I_{BIAS} in Rincon-Mora. (*Id.*) Rincon-Mora also discloses a "start-up circuit" that provides an "external enabling input to a logic block within the regulator." (EX1013, 3:27-32.) A POSITA would have seen that this logic block

a common concern and disabling circuitry that was not in use was an obvious and conventional way of saving power. (EX1002 ¶ 161.) Thus, even without Ivanov, a POSITA would have found it obvious to implement the biasing circuit for Rincon-Mora's LDO with the claimed enable/disable function. (*Id.*)

[e] an output power driver, wherein the current buffer driver is coupled between the operational amplifier and the output power driver;

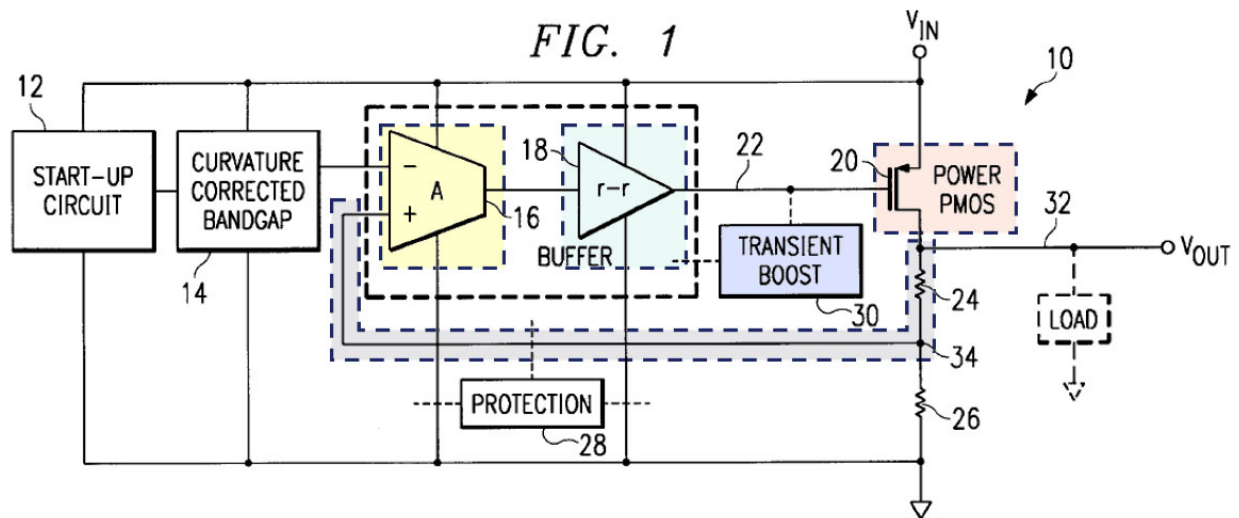
Rincon-Mora's LDO has an output power driver transistor 20, highlighted in red in the figure below. As shown, the buffer driver (green) is coupled between the output power driver and the amplifier (yellow):



(*Id.*, 3:39-47, 7:22-44, Fig. 1 (annotated); see also EX1002 ¶ 162.)

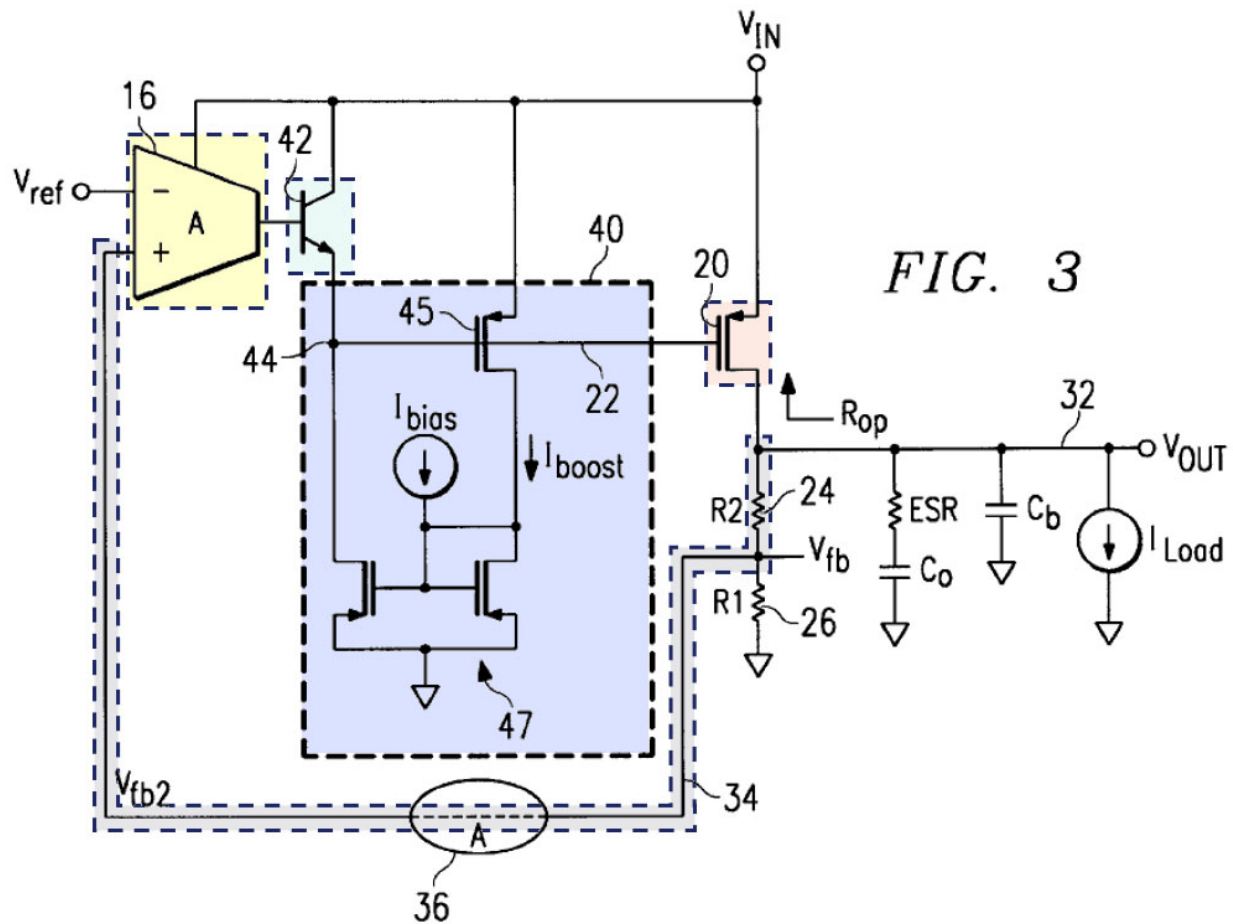
[f] a current feedback circuit coupled between the output power driver and the current buffer driver; and

As discussed above in the summary of Rincon-Mora's LDO and shown in the figure below, the LDO includes a current feedback circuit (blue) coupled between its output power driver (red) and the buffer driver (green):



(EX1013, Fig. 1 (annotated); see also EX1002 ¶ 163; Section IV.B.1, *supra*.)

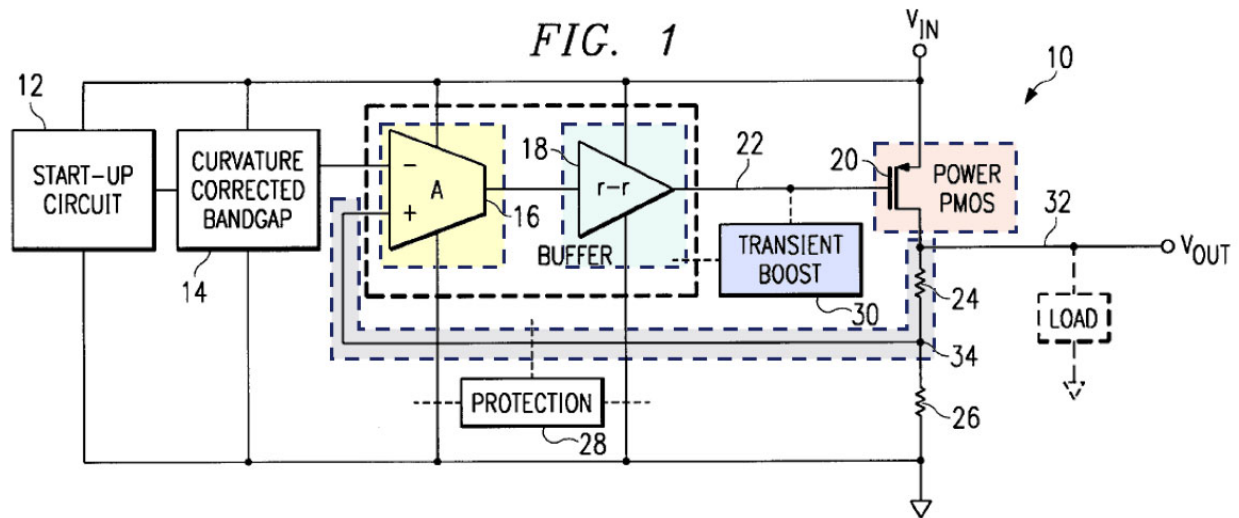
In the Rincon-Mora embodiment shown below, the current feedback circuit comprises transistor 45 and current mirror 47:



(EX1013, Fig. 3 (annotated); *see also* EX1002 ¶ 163.)

[g] a feedback loop coupled between the output power driver and the operational amplifier.

Rincon-Mora’s LDO has a feedback loop coupled between the output power driver and the error amplifier, which as discussed above under 1[a], could have been implemented as an operational amplifier. (Section IV.B.2, 1[a], *supra*.) One of the amplifier’s differential inputs is a reference voltage (EX1013, 3:26-39), while the other is a voltage provided by the output transistor that is “coupled back to . . . the error amplifier” via node 34 (*id.*, 3:58-62), as shown below:



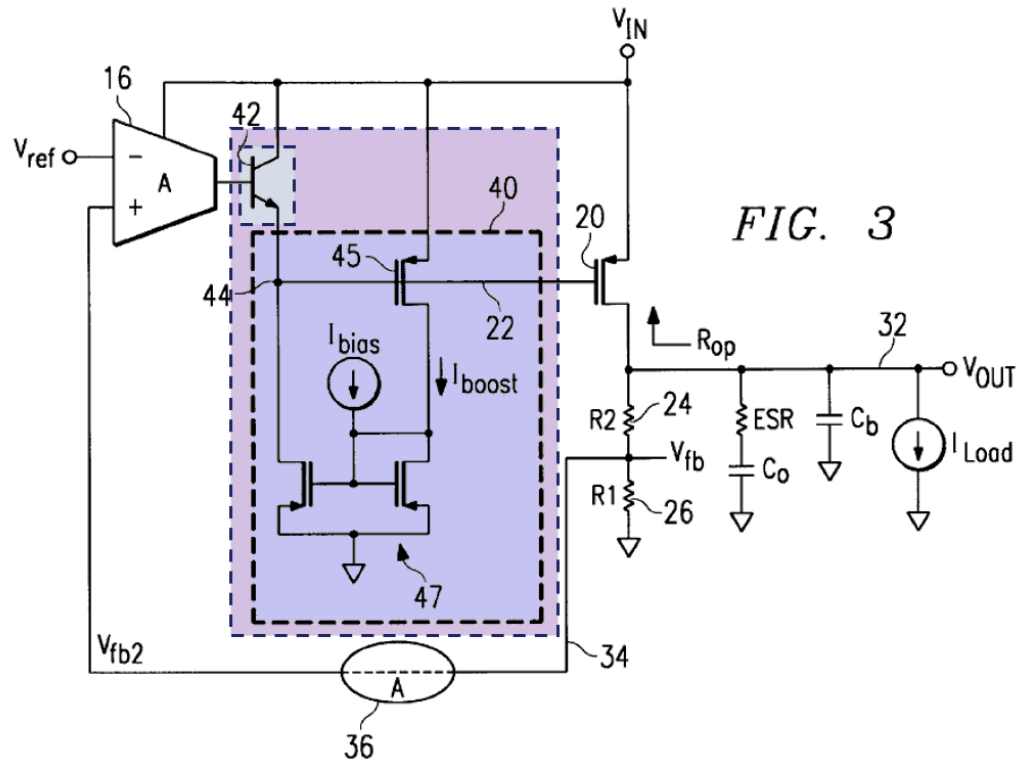
(*Id.*, Fig. 1 (annotated); *see also* EX1002 ¶ 164; Section IV.B.2, 1[a], *supra.*) Here, the feedback loop (gray) is coupled between the amplifier (yellow) and the output power driver (red), as claimed.

Claim 2 The voltage regulator according to claim 1, further comprising a gm-boost circuit coupled to the current buffer driver.

Rincon-Mora’s LDO has a gm-boost circuit in the form of a current feedback circuit coupled to the buffer driver. (EX1013, 4:62-5:21, Figs. 1, 3; *see also* EX1002 ¶¶ 165-67; Section IV.A.1, *supra.*)

As explained above under Ground 1, the ’074 patent does not define “gm-boost circuit,” but does describe a “gm-boost stage” that includes both the buffer and the current feedback circuit. (EX1001, 5:8-14; *see also* Section IV.A.2, claim 2, *supra.*) A POSITA would thus have understood that the claimed “gm-boost circuit” may include the buffer driver itself. (EX1002 ¶ 166.)

Rincon-Mora's LDO likewise includes a gm-boost circuit (shown in purple below) that includes a buffer driver (green) and a current feedback circuit (blue):



(EX1013, Fig. 3 (annotated); *see also* EX1002 ¶ 167.) As explained above, this gm-boost circuit increases the gm of the buffer driver. (See Sections IV.B.1, IV.B.2, 1[b], 1[c], *supra*.)

Claim 3 The voltage regulator according to claim 2, wherein the gm-boost circuit increases the current buffer driver input impedance.

To the extent “wherein the gm-boost circuit increases the current buffer driver input impedance” means that because of the current feedback provided by the gm-boost circuit, a transistor with relatively higher input impedance may be chosen as the current buffer driver, a POSITA would have found claim 3 to be obvious in an

implementation of the Rincon-Mora LDO that uses an operational amplifier and an NMOS as the error amplifier and buffer driver, respectively. (EX1002 ¶¶ 168-70.) By reducing the quiescent current that the buffer must supply, Rincon-Mora’s gm-boost circuit, as a POSITA would have recognized, would have allowed for a smaller NMOS—with low input capacitance and high input impedance—to be used. (*Id.*)

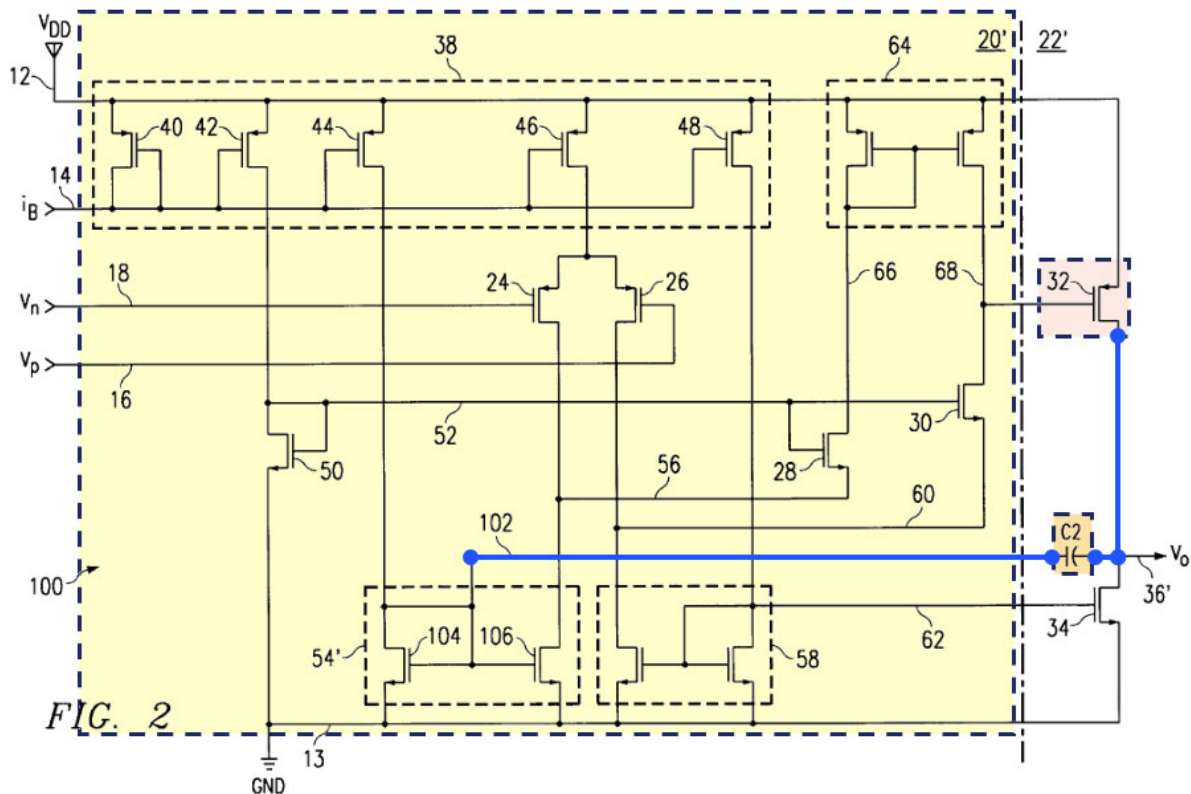
Claim 4 The voltage regulator according to claim 2, wherein the gm-boost circuit enables the current buffer driver to have a large gm value.

The ’074 patent does not explain what “large” means in claim 4. To the extent Patent Owner contends that “enables the current buffer driver to have a large gm value” should be read to mean “increases the gm value of the current buffer driver,” Rincon-Mora discloses claim 4. The gm-boost circuit in Rincon-Mora’s LDO increases the gm value of the buffer driver (transistor 42) by increasing its current using the transient response boost circuit that comprises transistor 45 and current mirror 47. (EX1002 ¶¶ 126-36, 142-48, 171; EX1013, 4:62-5:21; *see also* Sections IV.B.1, IV.B.2, 1[b], 1[c], *supra*.)

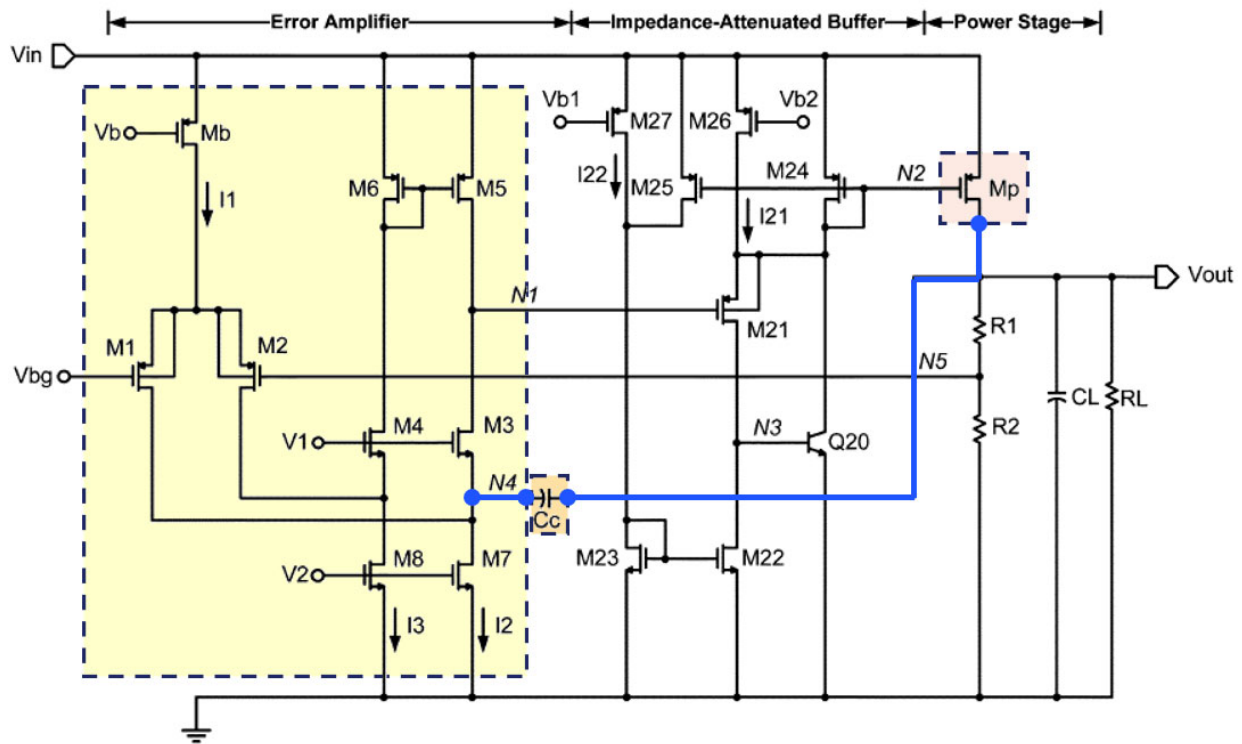
Claim 5 The voltage regulator according to claim 1, further comprising a compensation capacitor coupled between the output power driver and a cascode node of the operational amplifier.

It would have been obvious to include a compensation capacitor between the output power driver and a cascode node of the error amplifier when implementing Rincon-Mora’s LDO. Compensation capacitors, *e.g.*, Miller capacitors, were well-

known and used conventionally to improve the frequency response of a circuit by increasing the phase margin. (EX1002 ¶¶ 172-76.) The Rincon-Mora Dissertation, for example, discloses using such a capacitor, C_c , in an LDO's curvature corrected bandgap reference to provide stability. (EX1015, 109.) Rincon-Mora '475 likewise teaches that "a Miller-compensating capacitance" was a "well known technique for improving phase margin" and improving stability of a circuit "having feedback," and discloses a circuit with such a capacitor (shown in orange below) between an output PMOS (red) and a cascode node of an amplifier (yellow) in Figure 2:



(EX1016, 1:11-16, 3:1-9, Fig. 2 (annotated); *see also* EX1002 ¶ 174.) Furthermore, as discussed above for this claim under Ground 1, Al-Shyoukh also uses a Miller capacitor to “achieve stability in the full range of the load current”:



(EX1004, 1735, Fig. 8 (annotated); *see also* EX1002 ¶ 175; Section IV.A.2, claim 5, *supra*.) These examples confirm that placing a capacitor between the output driver and a cascode node of the error amplifier for Miller compensation was a well-known and widely used solution in the art. (EX1002 ¶ 176.)

As one of the stated goals of Rincon-Mora’s voltage regulator is to keep the system stable, such as by keeping the phase margin at or above 45° (EX1013, 4:27-29), a POSITA would have been motivated to place a Miller capacitor between its

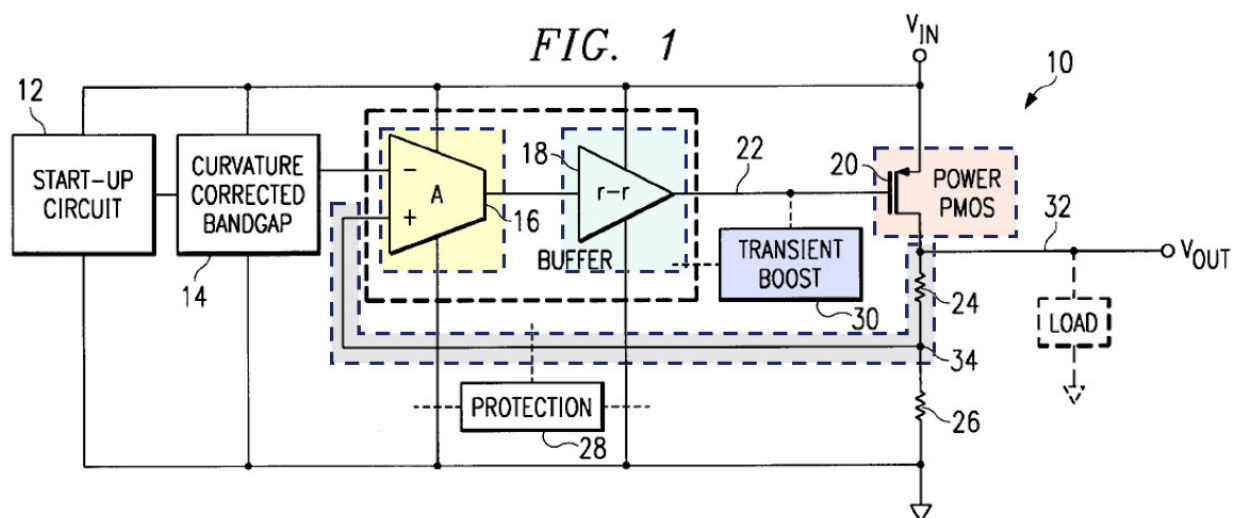
output transistor 20 and a cascode node of the error amplifier. (EX1002 ¶ 176.) And because this technique was conventional, a POSITA would have implemented it with a reasonable expectation of success and without undue experimentation. (*Id.*)

Claim 6 The voltage regulator according to claim 1, wherein the voltage regulator is a low drop out (LDO) voltage regulator.

Rincon-Mora's voltage regulator is an LDO. (EX1013, Abstract.)

Claim 7 The voltage regulator according to claim 1, wherein the operational amplifier has a first input adapted for coupling to a voltage reference, and a second input coupled to the feedback loop.

Rincon-Mora’s error amplifier (highlighted in yellow below) has a first input adapted for coupling to a voltage reference (*i.e.*, from a “curvature corrected bandgap circuit”) and a second input coupled to the feedback loop discussed above under 1[g] (gray):



(EX1013, 3:35-39, 7:19-21, Fig. 1 (annotated); EX1002 ¶ 178.)

Claim 8 The voltage regulator according to claim 1, wherein the operational amplifier is a low gain and high bandwidth amplifier.

The '074 patent does not explain what “low” or “high” means in claim 8. To the extent Patent Owner contends that “a low gain and high bandwidth amplifier” is “optimized for high bandwidth with a commensurate reduction of gain,” it would have been obvious to use such an amplifier with the Rincon-Mora LDO. (EX1002 ¶¶ 179-85.)

As discussed above under Ground 1, a POSITA would have understood that (1) trading off gain and bandwidth was a basic design step when implementing an operational amplifier, and (2) a high-bandwidth amplifier would be advantageous in an LDO to improve power efficiency and allow the LDO to respond faster to changes in input and power supply. (Section IV.A.2, claim 8, *supra*; EX1002 ¶¶ 180-84; *see also* EX1007, 8; EX1008, 96-97.) Thus, a POSITA would not only have found it to be a simple matter of design choice to use an amplifier with relatively higher bandwidth and commensurately lower gain, but would also have been motivated to do so in order to apply such an amplifier’s known benefits toward Rincon-Mora’s goals of improving power efficiency and transient response (*see, e.g.*, EX1013, 1:10-59; EX1014, 36-38). (EX1002 ¶¶ 182-84.)

Alternatively, from the parallel district court proceeding, Aptiv understands Patent Owner to argue that a folded cascode operational amplifier with a single stage

of gain (comprising a differential input and a cascode load) is necessarily a low gain and high bandwidth amplifier under claim 8. Under such a reading of the claim, the Rincon-Mora LDO as modified to use Al-Shyoukh's error amplifier (as discussed under claim 9 below) would have rendered claim 8 obvious because Al-Shyoukh's amplifier has a single-stage folded-cascode structure. (EX1002 ¶ 185.)

Claim 9 The voltage regulator according to claim 8, wherein the low gain and high bandwidth amplifier is a folded-cascode amplifier.

Rincon-Mora renders claim 9 obvious in view of Al-Shyoukh. As explained above under Ground 1, Al-Shyoukh discloses an LDO with an operational amplifier that has a single-stage folded-cascode structure. (Section IV.A.2, claim 9, *supra*; *see also* EX1004, 1735, Fig. 8.) A POSITA would have found it obvious to use the same folded-cascode amplifier in Rincon-Mora. (EX1002 ¶¶ 186-89.)

First, Rincon-Mora does not limit its error amplifier to a specific architecture, as discussed above under 1[a]. (*See* Section IV.B.2, 1[a], *supra*; *see also* EX1013, 7:19-44 (claiming “an error amplifier having first and second inputs and a reference output thereof,” but not specifying its internal structure).) Thus, a POSITA would have had a reasonable expectation of success when using a readily available error amplifier like Al-Shyoukh's to implement Rincon-Mora's LDO. (EX1002 ¶¶ 187-88.) Both of Al-Shyoukh's and Rincon-Mora's error amplifiers have the same connections—an input from a voltage reference, an input from feedback, an output

to a buffer driver, and a connection to the supply voltage—all conventional in an LDO. (*Id.*)

Second, a POSITA would have found Al-Shyoukh’s error amplifier especially suitable for Rincon-Mora because their respective LDOs are highly analogous. Not only do they have the same basic structure, but they also address the same goals of power efficiency and improved transient response, and seek to achieve them with the same general approach (using feedback mechanisms to boost current at the buffer driver). (*Id.* ¶ 189.) Al-Shyoukh’s first citation, in fact, is to the Rincon-Mora Paper, which it uses to explain the motivations behind its proposed LDO. (EX1004, 1732.) A POSITA would also have understood that a single-stage folded cascode structure is easier to stabilize and more power efficient than a multi-stage design. (EX1002 ¶ 189.) Thus, a POSITA would not just have seen Al-Shyoukh’s structure as readily available, but also have looked to it ahead of many equally available solutions. (*Id.*)

Claim 10 The voltage regulator according to claim 9, wherein the operational amplifier comprises diode connected PMOS transistors for lowering an output impedance of the folded-cascode amplifier.

As explained above under claim 9, it would have been obvious to implement the error amplifier in Rincon-Mora’s voltage regulator as Al-Shyoukh’s single-stage folded-cascode amplifier. That folded-cascode amplifier includes “a simple diode-connected active load using transistors M₅ and M₆,” resulting in “a smaller output resistance of the error amplifier r_{o1}.” (EX1004, 1738.) The advantages of including

these diode-connected transistors to reduce the amplifier's output resistance would have been obvious to a POSITA. (EX1002 ¶ 190.) For example, the Rincon-Mora Paper notes that as the maximum load-current specification increases, so does the size of the pass device, meaning higher load capacitance for the amplifier. (EX1014, 37.) It then explains that to keep the phase margin from degrading and the regulator becoming unstable, the amplifier's output impedance should be reduced. (*Id.*) A POSITA would therefore have been motivated to include Al-Shyoukh's diode-connected transistors when using Al-Shyoukh's amplifier for Rincon-Mora's LDO, rendering claim 10 obvious. (EX1002 ¶ 190; Section IV.A.2, claim 10, *supra.*)

Claim 11 The voltage regulator according to claim 1, wherein the current buffer driver is an operational transconductance amplifier (OTA).

Rincon-Mora as modified by Stanescu includes a current buffer driver that is an operational transconductance amplifier. As discussed under Ground 1, Stanescu discloses an LDO that uses an OTA as the buffer driving the output power stage:

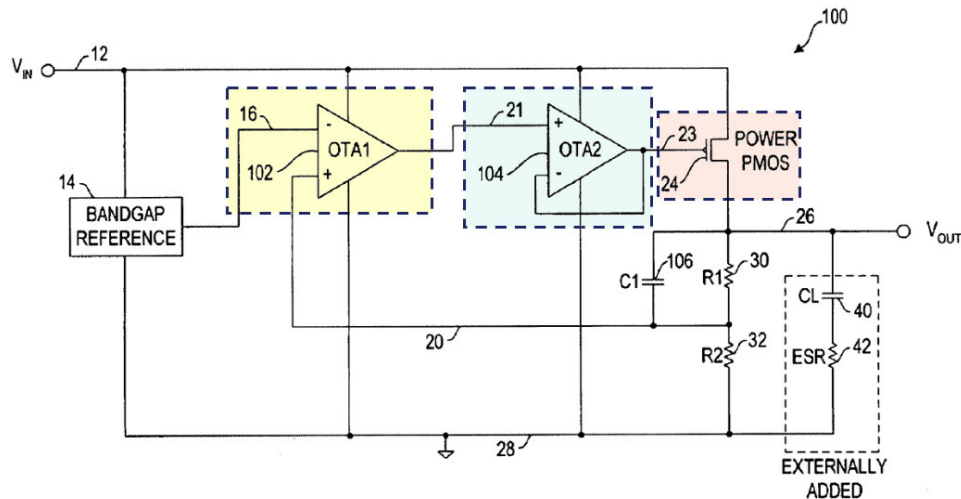


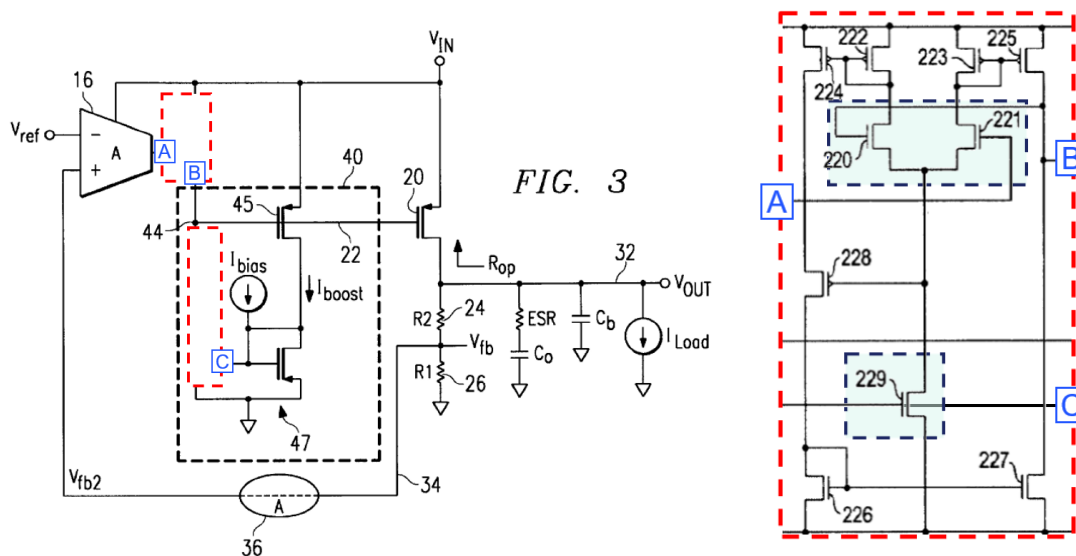
FIG. 2

(EX1006, Fig. 2 (annotated to show amplifier in yellow, buffer in green, and output power stage in red); Section IV.A.2, claim 11, *supra*.) Among the benefits of this OTA, Stanescu explains, are cost savings and improvements to bandwidth and the transient response of the LDO. (*Id.*, 2:44-53; EX1002 ¶ 192.) In addition, a POSITA would have recognized that, as a voltage follower, Stanescu’s OTA provides unity gain, and that unity gain is advantageous in an LDO because it has low output impedance and helps to keep the output voltage constant. (EX1002 ¶ 192.)

A POSITA would have been motivated by Stanescu to modify Rincon-Mora’s LDO to use an OTA as its buffer driver. (EX1002 ¶ 193.) First, Rincon-Mora does not limit its “buffer circuit” to any specific device. (*See* EX1013, 7:19-21.) Second, Stanescu is highly analogous art to Rincon-Mora because it is directed to an LDO for portable battery-powered devices (*see* EX1006, 1:17-28) that saves power by lowering the quiescent current (*see id.*, 7:64-8:3). A POSITA would have found the

advantages of Stanescu's OTA readily applicable to Rincon-Mora's LDO. (EX1002 ¶ 193.) The low output impedance of an OTA with unity gain feedback, for example, would have been helpful toward Rincon-Mora's goal of pushing the parasitic pole to higher frequencies and helping the LDO to maintain the desired output voltage. (*Id.*; EX1013, 4:13-29, 4:41-61; EX1014, 37-38.) And third, Stanescu specifically identifies Rincon-Mora's LDO as prior-art on which it improves, noting that Rincon-Mora's "biCMOS process" could be expensive. (EX1006, 2:18-21, 2:42-44; *see also* EX1002 ¶ 193.)

An exemplary combined circuit using Stanescu's OTA is shown below:



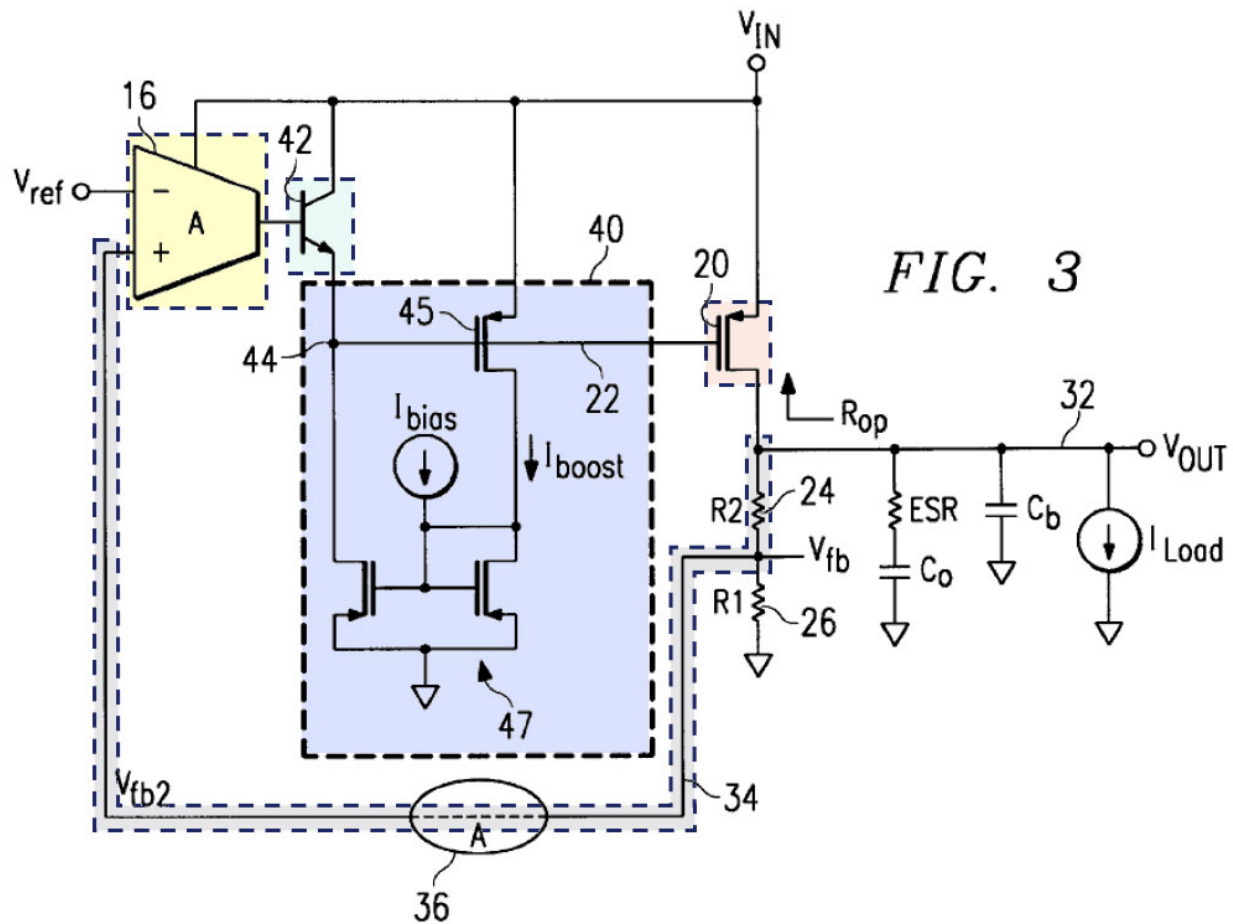
The figure on the left shows Rincon-Mora's LDO, modified to show how the OTA would fit in. The figure on the right is Stanescu's OTA, with the connection points to the Rincon-Mora circuit shown in blue. In the combined circuit, transistor 221 would receive an input from the error amplifier at A; the output of the OTA would

couple to Rincon-Mora's node 44 at B; and transistor 229 would form the left side of Rincon-Mora's current mirror 47 across C. (EX1002 ¶ 194.)

This circuit preserves Rincon-Mora's feedback mechanism because transistor 45 still senses a current change at the output transistor via node 22, generating the feedback current I_{boost} that is mirrored across current mirror 47 to transistor 229 from Stanescu, which then pulls further current from transistors 220 and 221, boosting the gm of the OTA/buffer. (*Id.* ¶ 195.) A POSITA would have arrived at the above circuit or an equivalent one without undue experimentation. (*Id.*)

Claim 12 The voltage regulator according to claim 1, wherein the current feedback circuit senses a current change at the output power driver.

Rincon-Mora's current feedback circuit senses a current change at its output power driver. As explained above under 1[f], the current feedback circuit (shown in blue below) comprises transistor 45 and current mirror 47, and transistor 20 is the output power driver (red):



(EX1013, Fig. 3 (annotated).) Transistor 45 senses a change in current at transistor 20 by receiving the corresponding voltage change on node 22. (EX1002 ¶ 196; *see also* EX1014, 37 (explaining that the boost circuit operates by “sensing the output current of the regulator and feeding back a ratio of the current to the slew-rate limited node of the circuit”).) Thus, Rincon-Mora discloses claim 12.

Claim 13 The voltage regulator according to claim 1, wherein the current feedback circuit provides transient enhancement for improved load regulation.

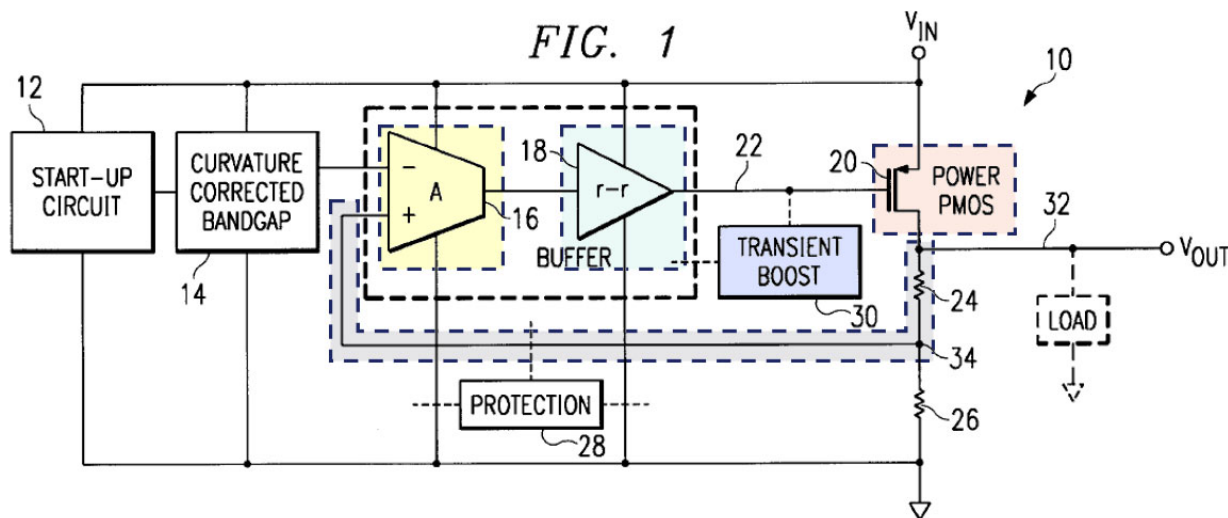
The current feedback circuit of Rincon-Mora’s LDO improve the “transient response” of the LDO to changes in load. (EX1013, 1:31-49; *see also id.*, Title.) It

does so by “selectively apply[ing] current to a slew-rate limited node,” while at the same time minimizing “standby current during zero output current load conditions.” (*Id.*, 1:12-17; EX 1002 ¶ 197.) A POSITA would have considered this improved transient response—discussed in detail above (*see* Section IV.B.1, *supra*)—to be a “transient enhancement for improved load regulation.” (EX1002 ¶ 197.)

Claim 14 The voltage regulator according to claim 1, wherein the current feedback circuit provides a feedback voltage from an output voltage node.

The '074 patent does not explain what “feedback voltage” or “output voltage node” means in claim 14. As discussed under Ground 1 above, the only way that a POSITA could have made sense of this claim in view of the rest of the specification would have been by assuming that the applicant meant to refer to 1[g]’s “feedback loop” rather than “the current feedback circuit.” (Section IV.A.2, claim 14, *supra*; *see also* EX1002 ¶¶ 198-99.)

Under this interpretation, Rincon-Mora discloses claim 14 because its feedback loop (in gray below) provides a feedback voltage (the voltage at node 34, which is the output voltage V_{OUT} less the drop across resistor 24) from the output voltage node 32 to the error amplifier (yellow):



(EX1013, Fig. 1 (annotated); EX1002 ¶ 200.)

To the extent Patent Owner contends that the claim actually was meant to refer to the “current feedback circuit,” a POSITA reviewing the rest of the specification would have understood “an output voltage node” to mean any node that provides a feedback voltage, because the ’074 patent does not identify any specific output node associated with the current feedback circuit. (EX1002 ¶ 201.) Under such a reading, Rincon-Mora discloses claim 14 because its current feedback circuit provides a voltage at node 22 to sensor transistor 45, that voltage being a “feedback voltage” because it responds to changes in the current of the output power driver 20. (*Id.*; see also Section IV.B.2, claim 12, *supra*.)

Claim 15 The voltage regulator according to claim 1, wherein the current buffer driver has a low output impedance.

The buffer driver in Rincon-Mora’s LDO has low output impedance. In fact, “[t]he idea of the buffer is to isolate the large capacitor associated with the gate of

the power PMOS transistor from the large resistance of the output of [the amplifier]’s gain stage,” which requires the buffer to have “low input capacitance and low output impedance.” (EX1014, 42.) Thus, a POSITA would have understood to implement Rincon-Mora using a buffer with those properties, and that the design of the LDO further lowers the output impedance of the buffer through the gm boost discussed above. (EX1002 ¶ 202; *see also id.* ¶ 144; Section IV.B.2, 1[b], *supra.*)

Claim 16 The voltage regulator according to claim 1, further comprising capacitors in the biasing circuit for improving noise immunity thereof.

It would have been obvious to use capacitors in the bias circuit for Rincon-Mora’s LDO to improve noise immunity. (EX1002 ¶¶ 203-06.)

dAs noted above under Ground 1, “decoupling” or “bypass” capacitors were well-known in the art and routinely used to insulate a circuit from noise. (EX1002 ¶¶ 204-05; *see also* Section IV.A.3, claim 16, *supra*; EX1009, 12 & 217 (teaching that decoupling capacitors can alleviate “power and signal integrity problems” caused by noise); EX1010, 2:64-3:1 (using a bypass capacitor to hold voltage constant “despite fluctuations” from an RF signal); EX1011, 10 (recommending decoupling capacitors to keep noise out of a bias circuit).) The Rincon-Mora Dissertation discloses such a use of capacitors in a curvature corrected bandgap circuit that supplies a reference voltage to the error amplifier of an LDO, to limit “noise bandwidth of the reference circuit” and thus “enhanc[e] noise performance.”

(EX1015, 109.) Thus, a POSITA would have recognized that decoupling capacitors were a conventional solution for reducing noise, especially in bias circuits that must reliably output a fixed voltage. (EX1002 ¶ 206.) Using these capacitors in the bias circuit for generating I_{bias} in the Rincon-Mora LDO was therefore obvious.

Claim 17 The voltage regulator according to claim 1, wherein the voltage regulator is a USB voltage regulator.

It would have been obvious to use Rincon-Mora's voltage regulator as a USB voltage regulator. (*Id.* ¶ 207.) Rincon-Mora explains that its LDO was suited for “portable, battery powered applications” where “standby and quiescent current flow [were] major concerns.” (EX1013, 1:18-25; EX1014, 36.) A POSITA would have recognized that USBs were such an application because they typically required the host device to supply power, raising power management concerns. (EX1002 ¶ 207; *see also* EX1012, 2:29-33 (identifying a method to conserve power in a USB capable device that includes providing “a USB voltage regulator”).) A POSITA would thus have found USBs to be an obvious application for Rincon-Mora's LDO.

Claim 18 The voltage regulator according to claim 1, wherein the current buffer driver has low input impedance and provides a high frequency pole that does not substantially affect the voltage regulator dominant pole.

The buffer driver in Rincon-Mora's LDO discloses claim 18. The Rincon-Mora Paper gives the system's dominant pole P_1 as:

$$P_1 \approx \frac{1}{2\pi C_o R_{o\text{-pass}}} \approx \frac{\lambda I_{\text{Load}}}{2\pi C_o}$$

where C_o is the output capacitance, $R_{o\text{-pass}}$ is the output resistance of the pass device (*i.e.*, output power driver), λ is the channel length modulation parameter, and I_{Load} is the load current. (EX1014, 37.) In addition, the parasitic pole P_3 is given by:

$$P_3 \approx \frac{g_{m\text{NPN}}}{2\pi C_{\text{par}}} = \frac{I_{\text{bias}} + I_{\text{boost}}}{2\pi V_t C_{\text{par}}} \approx \frac{I_{\text{bias}} + kI_{\text{Load}}}{2\pi V_t C_{\text{par}}}$$

where C_{par} is the parasitic capacitance at the output of buffer (node 22/44 in Figure 3 of Rincon-Mora), $g_{m(\text{npn})}$ is the transconductance of the buffer transistor, I_{bias} is the bias current, I_{boost} is the boost current, V_t is the thermal voltage, and k is the constant mirror ratio between the output driver and the transistor of the transient boost circuit that mirrors the output driver. (*Id.*, 37-38, Fig. 2; EX1013, Fig. 3 (k is ratio between transistors 20 and 45); *see also* EX1002 ¶ 208.)

Thus, the circuit “can be designed such that P_3 increases at a faster rate than the UGF with respect to load-current.” (EX1014, 38; *see also* EX1002 ¶ 209.) Thus, a POSITA would have understood that Rincon-Mora’s buffer driver provides a high frequency pole that does not substantially affect the dominant pole. (EX1002 ¶ 209; *see also* EX1013, 4:10-61 (explaining that the parasitic pole is moved to higher frequencies by the transient boost circuit, keeping it well above the dominant pole and the unity gain frequency).)

The '074 patent does not explain what it means for the current buffer driver to have “low input impedance” under claim 18. But as noted under Ground 1 with respect to claim 3, Patent Owner has interpreted (in the district court proceeding) “current buffer driver input impedance” to mean the input impedance at the point where the operational amplifier connects to the current buffer driver. Applying this same understanding to claim 18, a POSITA would have found that Rincon-Mora renders it obvious. (EX1002 ¶¶ 210-11.) This is because, when implemented as an op-amp (*see* Section IV.B.2, 1[a], *supra*), Rincon-Mora’s error amplifier would have low output impedance. (EX1002 ¶ 211.) It would therefore have been obvious to a POSITA to implement Rincon-Mora’s LDO such that the output impedance of the operational amplifier, *i.e.*, the impedance at the point where the operational amplifier connects to the buffer driver—is relatively low. (*Id.*) Claim 18 is thus obvious.

V. NOTICES AND STATEMENTS

Pursuant to 37 C.F.R. § 42.8(b)(1), Aptiv Services US, LLC, Aptiv Technologies AG, and Aptiv Technologies Limited are the real parties-in-interest for Petitioner.

Pursuant to 37 C.F.R. § 42.8(b)(2), Petitioner identifies the following related matter: the '074 patent is asserted in *Microchip Technology Inc. v. Aptiv Services US, LLC*, No. 23-cv-778-JDW (DED).

Pursuant to 37 C.F.R. § 42.8(b)(3), Petitioner identifies the following counsel (and a power of attorney accompanies this Petition).

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Pursuant to 37 C.F.R. § 42.8(b)(4), service information for lead and back-up counsel is provided above. Petitioner consents to electronic service by email to Microchip-Aptiv-PTAB@mofo.com.

Pursuant to 37 C.F.R. § 42.104(a), Petitioner certifies that the '074 patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting an *inter partes* review challenging the patent claims on the grounds identified in this Petition.

The USPTO is authorized to charge any required fees, including the fee as set forth in 37 C.F.R. § 42.15(a) and any excess claim fees, to Deposit Account No. 03-01952 referencing Docket No. 28640-00000.06.

Inter Partes Review of U.S. Patent No. 9,471,074

Dated: March 8, 2024

Respectfully submitted,

By /Alex Yap/

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Certification of Word Count (37 C.F.R. § 42.24)

I hereby certify that this Petition for *Inter Partes* Review has 13,999 words (as counted by the “Word Count” feature of the Microsoft Word™ word-processing system), exclusive of “a table of contents, a table of authorities, mandatory notices under § 42.8, a certificate of service or word count, or appendix of exhibits or claim listing.”

Dated: March 8, 2024

/Alex Yap/
Alex S. Yap

Certificate of Service (37 C.F.R. § 42.6(e)(4))

I hereby certify that the attached Petition for *Inter Partes* Review and supporting materials were served as of the below date by UPS, which is a means at least as fast and reliable as U.S. Express Mail, on the Patent Owner at the correspondence address indicated for U.S. Patent No. 9,471,074.

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Dated: March 8, 2024

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