

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

MICROCHIP TECHNOLOGY INC.,

Plaintiff,

v.

APTIV SERVICES US, LLC

Defendant.

Civil Action No. 1:23-cv-00778 (JDW)

JURY TRIAL DEMANDED

APTIV'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

TABLE OF CONTENTS

	Page
I. INTRODUCTION	1
II. THE ASSERTED PATENTS	2
A. The '665 Patent	2
III. ARGUMENT	3
A. Term 1: “second voltage rail”	3
B. Term 3: “an enable/disable function to enable/disable the biasing circuit for reducing standby current”	8
1. Means-plus-function rules apply here because the term is not a sufficiently definite name for a structure or class of structures.	9
2. The claim is indefinite because the '074 patent fails to disclose adequate structure to perform the recited functions of “enabl[ing]/disabl[ing] the biasing circuit for reducing standby current.”	11
C. Term 4: “wherein the gm-boost circuit enables the current buffer driver to have a large gm value”	12
D. Term 5: “low gain and high bandwidth amplifier”	15

TABLE OF AUTHORITIES

	Page(s)
Cases	
<i>3M Innovative Props. Co. v. Avery Dennison Corp.</i> , 350 F.3d 1365 (Fed. Cir. 2003).....	4
<i>Acera Surgical, Inc. v. Nanofiber Sols., LLC</i> , C.A. No. 20-980-CFC-JLH, 2022 WL 6948855 (D. Del. Oct. 12, 2022)	4
<i>August Tech. Corp. v. Camtek, Ltd.</i> , 655 F.3d 1278 (Fed. Cir. 2011).....	7
<i>Baran v. Med. Device Techs., Inc.</i> , 616 F.3d 1309 (Fed. Cir. 2010).....	7
<i>CAE Screenplates, Inc. v. Heinrich Fiedler Gmbh & Co. Kg</i> , 224 F.3d 1308 (Fed. Cir. 2000).....	14
<i>Diebold Nixdorf, Inc. v. Int’l Trade Comm’n</i> , 899 F.3d 1291 (Fed. Cir. 2018).....	9
<i>Dow Chem. Co. v. Nova Chems. Corp. (Canada)</i> , 803 F.3d 620 (Fed. Cir. 2015).....	16
<i>Gillette Co. v. Energizer Holdings, Inc.</i> , 405 F.3d 1367 (Fed. Cir. 2005).....	4
<i>Google LLC v. EcoFactor, Inc.</i> , 92 F.4th 1049 (Fed. Cir. 2024)	4, 5
<i>Helmsderfer v. Bobrick Washroom Equip., Inc.</i> , 527 F.3d 1379 (Fed. Cir. 2008).....	7
<i>Intell. Ventures I LLC v. AT&T Mobility LLC</i> , No. CV 13-1668-LPS, 2016 WL 4363485 (D. Del. Aug. 12, 2016), <i>rev’d in-</i> <i>part on other grounds, sub nom. Intell. Ventures I LLC v. T-Mobile USA, Inc.</i> , 902 F.3d 1372 (Fed. Cir. 2018).....	14
<i>Interval Licensing LLC v. AOL, Inc.</i> , 766 F.3d 1364 (Fed. Cir. 2014).....	13
<i>Linear Technology Corporation v. International Trade Commission</i> , 566 F.3d 1049 (Fed. Cir. 2009).....	5
<i>Nautilus, Inc. v. Biosig Inst., Inc.</i> , 572 U.S. 898 (2014).....	13, 15

<i>Nobel Biocare Servs. AG v. Intradent USA, Inc.</i> , 903 F.3d 1365 (Fed. Cir. 2018).....	7
<i>Powell v. Home Depot USA, Inc.</i> , 663 F.3d 1221 (Fed. Cir. 2011).....	5, 8
<i>PPC Broadband, Inc. v. Corning Optical Comms. RF, LLC</i> , 815 F.3d 747 (Fed. Cir. 2016).....	7
<i>PSN Illinois, LLC v. Ivoclar Vivadent, Inc.</i> , 525 F.3d 1159 (Fed. Cir. 2008).....	7
<i>Renishaw PLC v. Marposs Societa'</i> <i>per Azioni</i> , 158 F.3d 1243, 1248 (Fed. Cir. 1998).....	4
<i>Skedco, Inc. v. Statagic Ops., Inc.</i> , 685 F. App'x 956 (Fed. Cir. 2017)	5, 8
<i>Square D Company v. E.I. Electronics, Inc.</i> , 685 F. Supp. 2d 864 (N.D. Ill. 2010)	5
<i>Teleflex, Inc. v. Ficoso N. Am. Corp.</i> , 299 F.3d 1313 (Fed. Cir. 2002).....	4
<i>Williamson v. Citrix Online, LLC</i> , 792 F.3d 1339 (Fed. Cir. 2015).....	8, 9, 11

I. INTRODUCTION

The constructions proposed by Microchip Technology, Inc. (“Microchip”) for the disputed terms in the two patents it asserts against Aptiv Services US, LLC (“Aptiv”) disregard the express language of the patents’ claims and gloss over the specification in the ’074 patent, suggesting the description teaches more than it discloses to a person of skill in the art.

’665 Patent: Microchip’s proposed construction of the first term, “second voltage rail,” as used in claim 1 of the ’665 patent, conflates two distinct structures identified in the claim. The claim language unambiguously refers to three separate voltage rails, each with distinct functions and relationships. Microchip’s reliance on a portion of the specification that identifies alternate embodiments with a single power rail is misplaced, as the claim in question is specifically directed to the dual power rail embodiment. Accordingly, the “second voltage rail” is distinct from the “first voltage rail,” contrary to Microchip’s proposed construction.

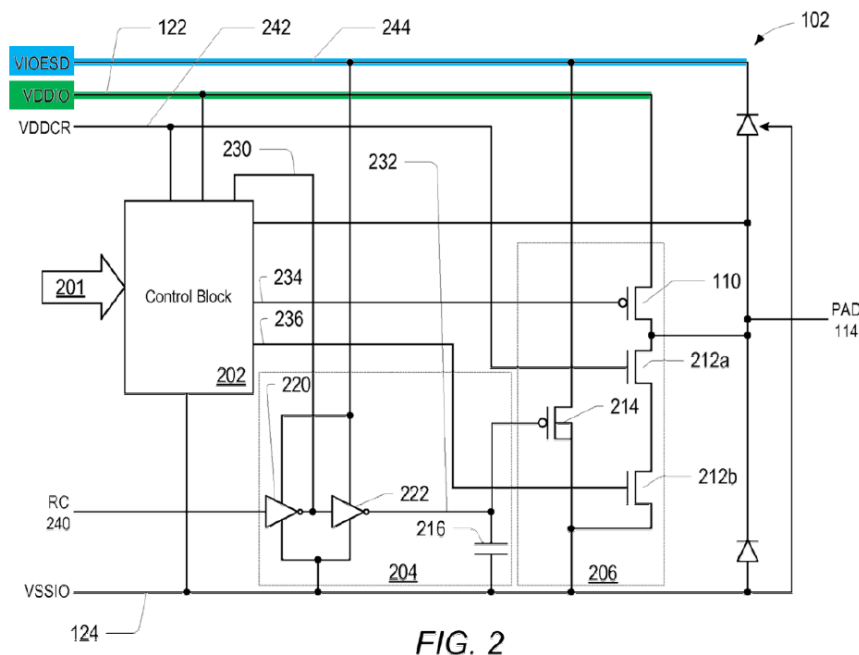
’074 Patent: The disputed term “an enable/disable function to enable/disable the biasing circuit for reducing standby current,” as used in sole independent claim 1 of the ’074 patent, is subject to the rules of mean-plus-function claiming under 35 U.S.C. 112, paragraph 6, because a person of skill in the art would not understand the term as a name for structure. Additionally, Microchip’s identification of a bare input line as the corresponding structure is insufficient. Because the patent does not disclose structure that a POSITA would recognize as adequate to achieve the claimed function—even as Microchip improperly seeks to limit it—the claim is further invalid for indefiniteness. Claim 4 and claims 8 and 9 of the ’074 patent require a “large gm value” and “low gain and high bandwidth amplifier,” respectively, which are terms of degree. These claims are indefinite because they lack objective boundaries. Microchip’s proposed constructions for these terms fail to clarify their scope. Nor could they: neither the

language of the claims nor the specification provides sufficient guidance to inform a person of ordinary skill in the art with reasonable certainty of the scope of these limitations.

II. THE ASSERTED PATENTS

A. The '665 Patent

The '665 patent is directed generally to “the design of protection circuitry for providing protection against damaging effects of Electrostatic Discharge (ESD).” The specification describes several different ways in which such a circuit can be designed. Figure 2 shows one particular embodiment, annotated below:



Only a portion of the circuit described is intended to provide ESD protection. (Declaration of Stanley Shanfield, PhD (“Shanfield Decl.”) ¶¶ 33-35.) The remainder of the circuit is what the ESD portion is protecting—sensitive input/output (“I/O”) circuitry used to send or receive a signal using a physical pad. (*Id.*)

One aspect of the circuit discussed in the specification is the way in which voltage is provided to the ESD and non-ESD (i.e., I/O) portions of the circuit. In the circuit shown in

Figure 2, this is accomplished using two separate voltage rails—VIOESD and VDDIO. The specification explains that the VIOESD (blue) rail effectively allows the system to detect an ESD event and, in such an event, to activate the clamp control circuit in an effort to protect the more sensitive I/O components. (’665 patent at 5:9-11; Shanfield Decl. ¶ 36.) (“When an ESD event occurs, the fast ramp rate of a voltage spike on VIOESD rail 244 may result in VIOESD rail 244 providing increased power to clamp control circuit 204...”)

The VDDIO (green) rail, on the other hand, is the more general “I/O supply/voltage pad rail” that provides power to the I/O components that are active during normal operation. (’665 patent at 4:3-7; Shanfield Decl. ¶ 36)

In addition to the separate VIOESD and VDDIO rails shown in Figure 2, the specification explains that “alternate embodiments may be configured with a single power rail providing power to the circuit and/or system components that are powered by VIOESD 244 and VDDIO 122 in the embodiment shown in FIG. 2.” (’665 patent at 5:58-62) (emphasis added).

III. ARGUMENT

A. Term 1: “second voltage rail”

No.	Claim Term	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
1	“second voltage rail” ’665 patent, claim 1	Plain and Ordinary Meaning Alternatively, “a second voltage rail that is distinct from the third voltage rail but may or may not be distinct from the first voltage rail”	“a second voltage rail that is distinct from the first voltage rail”

Microchip’s proposed construction for “second voltage rail” improperly elides two structures expressly and distinctly identified in claim 1 of the ’665 patent. In doing so, it relies upon a portion of the specification that identifies two alternate embodiments—one in which a single voltage rail is used to supply power and another in which two distinct rails are used to do so. While elsewhere in the ’665 patent Microchip elected to claim the single-power-rail embodiment, claim 1 is directed specifically to the dual-power-rail structure.

Claim construction begins, as always, with the actual words of the claim. *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1324 (Fed. Cir. 2002) (quoting *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1248 (Fed. Cir. 1998)) (“[T]he claims define the scope of the rights to exclude; the claim construction inquiry, therefore, begins and ends in all cases with the actual words of the claims.”). As Microchip itself recognizes, “there is a ‘presumption’ that separately listed claim limitations may indicate separate and distinct physical structure...” *Google LLC v. EcoFactor, Inc.*, 92 F.4th 1049, 1058 (Fed. Cir. 2024). Here, the words of claim 1 are unambiguous and refer to a first, a second, and a third voltage rail. The claims further describe the relationship among these three voltage rails. The first voltage rail must have “a value” above the third voltage rail and must have an “associated capacitance” capable of sharing a charge developed in the system in response to an ESD event. (See ‘665 patent at claims 1 and 2.) The second voltage rail must be configured to provide power to the enable circuitry and must be coupled to the third voltage rail via a clamp device configured to reduce, when turned on, the maximum voltage developed in the system as a result of an ESD event. (See *id.* at claim 1.)

The decision to use ordinal numbering for the rails in the system—“first voltage rail,” “second voltage rail,” and “third voltage rail”—bolsters the presumption that these are separate and distinct claim elements. See *3M Innovative Props. Co. v. Avery Dennison Corp.*, 350 F.3d 1365, 1371 (Fed. Cir. 2003) (“use of the terms ‘first’ and ‘second’ is common patent-law convention to distinguish between repeated instances of an element”); *Gillette Co. v. Energizer Holdings, Inc.*, 405 F.3d 1367, 1373 (Fed. Cir. 2005) (finding that “the terms ‘first, second, and third,’ are terms to distinguish different elements of the claim”); *Acera Surgical, Inc. v. Nanofiber Sols., LLC*, C.A. No. 20-980-CFC-JLH, 2022 WL 6948855, at *6 (D. Del. Oct. 12, 2022) (finding that a claim requiring a “first layer,” “second layer,” and “third

layer” must be “distinct and separately deposited”). This contrasts with the functional or descriptive language used to distinguish claim elements in the Federal Circuit cases relied upon by Microchip. See e.g., *Powell v. Home Depot USA, Inc.*, 663 F.3d 1221, 1231-32 (Fed. Cir. 2011) (finding that a single structure could serve as both the “cutting box” and “dust collection structure”); *Skedco, Inc. v. Statagic Ops., Inc.*, 685 F. App’x 956, 959-60 (Fed. Cir. 2017) (a claim requiring both a pump and a valve may be satisfied by a pump with an internal valve); *Google*, 92 F.4th at 1059 (finding that one claimed data input could potentially be used to calculate the other four claimed data inputs). While *Linear Technology Corporation v. International Trade Commission* involved claim elements with ordinal numbering, the Federal Circuit was not asked to determine whether the same exact circuit could satisfy both elements. 566 F.3d 1049, 1055-56 (Fed. Cir. 2009). Instead, the Court was asked merely to determine whether some overlap between the circuits was permissible. *Id.* Here, Microchip argues that the same precise structure should be read as the entirety of both the first and second voltage rail. The sole case cited by Microchip in which a single structure was found to satisfy multiple limitations with ordinal descriptors is *Square D Company v. E.I. Electronics, Inc.*, a district court decision from the Northern District of Illinois in which the specification and figures exclusively described the use of a single power supply and the only mention of a “second power supply” was found in the claims. 685 F. Supp. 2d 864, 875-76 (N.D. Ill. 2010).

In arguing that the specification rebuts the presumption of separate and distinct structures, Microchip relies extensively on a statement in the specification that:

VIOESD 244 and VDDIO 122 may in fact be the same power/supply rail, and ***alternate embodiments*** may be configured with a single power rail providing power to the circuit and/or system components that are powered by VIOESD 244 and VDDIO 122 in the embodiment shown in FIG. 2. In general, the ESD rail and the power supply rail can be the same supply rail, and separate supply rails (e.g. VIOESD 244 and a distinct VDDIO 122) may not be required.

'665 Patent at 5:57-65 (emphasis added). As this passage recognizes, the basic function of VIOESD and VDDIO rails—providing power to the ESD-specific components in addition to the more general I/O components—*may* generally be accomplished by a single rail. However, the solutions are not identical and there are technical reasons why a POSITA might elect a circuit with separate VDDIO and VIOESD rails. (Shanfield Decl. ¶ 51.) For example, a system with separate rails would avoid dissipating ESD charge within any transistor, allowing for the use of smaller and less expensive transistors. (*Id.* ¶ 52.) In contrast, a system in which a single rail serves the purposes of both the VDDIO and VIOESD rails would dissipate charge through at least one transistor, requiring larger (and more costly) transistors to effectively do so without causing permanent damage. (*Id.* ¶ 53.) It is for this reason that the passage discusses the two-rail versus three-rail configurations as distinct alternate embodiments—one “configured with a single power rail providing power to the circuit and/or system components” and the other as described in Fig. 2 and the preceding paragraphs in which the VIOESD and VDDIO voltage rails are distinct.

Aptiv agrees with Microchip that Fig. 2 of the '665 patent shows the separate-rail embodiment and that VDDIO corresponds to the “first voltage rail” and VIOESD to the “second voltage rail” in claim 1. Fig. 2 appears, in fact, to correlate directly to the embodiment claimed in claim 1. (Shanfield Decl. ¶ 50.) But claim 1 is not the only independent claim of the '665 patent; one of those other independent claims, claim 6, is directed to the “alternate embodiment” described in the specification and requires only a single power supply rail. (*Id.* ¶ 54.)

The question for the Court, then, is whether to give effect to the applicant’s decision to claim these alternate embodiments separately, or whether to read both embodiments into a single claim. Fortunately, the Federal Circuit has provided ample guidance on this topic, explaining

that it is “often the case that different claims are directed to and cover different disclosed embodiments. The patentee chooses the language and accordingly the scope of his claims.” *Helmsderfer v. Bobrick Washroom Equip., Inc.*, 527 F.3d 1379, 1383 (Fed. Cir. 2008); *accord Nobel Biocare Servs. AG v. Intradent USA, Inc.*, 903 F.3d 1365, 1381 (Fed. Cir. 2018). For this reason, “[i]t is not necessary that each claim read on every embodiment.” *Baran v. Med. Device Techs., Inc.*, 616 F.3d 1309, 1316 (Fed. Cir. 2010); *PPC Broadband, Inc. v. Corning Optical Comms. RF, LLC*, 815 F.3d 747, 755 (Fed. Cir. 2016) (rejecting, even under the more generous broadest reasonable interpretation standard, the proposition that “each and every claim ought to be interpreted to cover each and every embodiment”). And “courts must recognize that disclosed embodiments may be within the scope of other allowed but unasserted claims.” *PSN Illinois, LLC v. Ivoclar Vivadent, Inc.*, 525 F.3d 1159, 1166 (Fed. Cir. 2008). Even had the applicant not chosen to claim the alternate embodiment in claim 6, it would be improper to read that embodiment into claim 1. *See August Tech. Corp. v. Camtek, Ltd.*, 655 F.3d 1278, 1285 (Fed. Cir. 2011) (“The mere fact that there is an alternative embodiment disclosed in the asserted patent that is not encompassed by our claim construction does not outweigh the language of the claim, especially when the court’s construction is supported by the intrinsic evidence.”).

The cases Microchip relies upon are distinguishable because they are directed to situations in which a court has found that a single structure (or some part of that structure) may satisfy more than one limitation. As those cases acknowledge, though, this is only true when the specification provides no contrary indication. Here, the specification makes clear that in one of the embodiments expressly disclosed in the specification, the structures of the VDDIO and VIOESD rails are separate and distinct from one another. None of the cases cited by Microchip address a situation in which the specification provides two separate embodiments, each mapping

onto the language of separate claims. *See e.g., Powell*, 663 F.3d at 1231-32 (specification disclosed only a single embodiment); *Skedco*, 685 F. App’x at 959 (all embodiments contained the same valve configuration).

B. Term 3: “an enable/disable function to enable/disable the biasing circuit for reducing standby current”

No.	Claim Term	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
3	“an enable/disable function to enable/disable the biasing circuit for reducing standby current” ’074 patent, claim 1	Not subject to 35 U.S.C. § 112 ¶ 6. To the extent the court determines that § 112 ¶ 6 applies: Function: to enable/disable the biasing circuit for reducing standby current Structure: enable/disable signal input line (Node M)	Indefinite; Subject to 35 U.S.C. § 112 ¶ 6 without any corresponding structure

Microchip and its expert rely on four technical specifications and a digital circuit design textbook, none of which uses the term “an enable/disable function to enable/disable the biasing circuit for reducing standby current” as a name for a class of structures to perform the recited function. The varied uses of *related* terms in these sources instead support that the disputed term itself does not have a sufficiently definite meaning as the name for structure to perform the claimed function, such that the requires of mean-plus-function claiming under § 112 ¶ 6 apply. Moreover, the structure that Microchip identifies is no more than an input line (Node M), which is inadequate to perform the claimed function. And because the patent fails to disclose structure that *is* adequate to perform the function, this renders the indefinite.

To resolve the parties’ dispute, the court must first determine whether a claim limitation is drafted in means-plus-function format. *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1349 (Fed. Cir. 2015). This “inquiry is not merely the presence or absence of the word ‘means’ but

whether the words of the claim are understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the name for structure.” *Id.* at 1348. If the court determines that it does, § 112 ¶ 6 does not apply. If, on the other hand, the court concludes that the claim term “fails to ‘recite sufficiently definite structure’ or else recites ‘function without reciting sufficient structure for performing that function,’” *Diebold Nixdorf, Inc. v. Int’l Trade Comm’n*, 899 F.3d 1291, 1298 (Fed. Cir. 2018), then the limitation is in means-plus-function format and the court proceeds to step two: determining “what structure, if any, disclosed in the specification corresponds to the claimed function,” *Williamson*, 792 F.3d at 1351. A term is indefinite if the specification fails to disclose a structure that a POSITA would recognize as (1) clearly linked or associated with performance of the corresponding claimed function and (2) adequate to achieve that function. *Id.* at 1352.

1. Means-plus-function rules apply here because the term is not a sufficiently definite name for a structure or class of structures.

The ’074 patent discloses the technique of “disabling/power[ing] down operation” of the bias circuit “to make sure this circuit will consume substantially no DC current” when it is disabled. (’074 patent at 4:45-46.) Microchip attempts to demonstrate that the rules of means-plus-function claiming do not apply to the term by instead relying on the use of the term “enable”—either alone or in combination with other modifiers—to refer to a variety of different signals and structures. The evidence in fact demonstrates that the disputed term that is used by the claims would not be understood as a sufficiently definite name for class of structure by a POSITA in the context of the ’074 patent.

Exhibits 1-4 to the Taylor Declaration are technical documentation for various voltage regulators. These exhibits use one or more of the terms “enable,” “enable pin,” “enable input,” “EN,” or “EN pin” to refer solely to a *physical pin and/or wire* through which a signal may be

sent to some logic circuit on the regulator that acts to turn circuitry on or off based on the voltage of the signal. (*See* Shanfield Decl. ¶ 60.) None of the exhibits use the term “enable/disable function” to refer to such an input line. *Id.* Exhibit 1 instead uses the terms “smart enable,” “smart enable circuit,” and “smart enable input circuit”—and Exhibit 3 uses the terms “enable logic control function,” “enable function” and the label “Enable” on Figure 1—to refer instead to **circuitry that implements logic** to turn on or off some other circuitry on the regulator, based on receipt of an input signal. (*Id.*) In a third category of usage, Taylor Exhibit 5 is a digital logic textbook uses the letter “e” and the phrases “enable signal” and “enable signal e” to refer to various voltage **signals**. (*Id.*) Rather than illustrating the use of the disputed language of the claim, these examples show that other terms—which are at best substantial **variants** of the disputed term—refer **either** to signals or different structures that may be used in techniques that accomplish “enabling/disabling the flow of current in a circuit.” (*See* Taylor Decl. ¶¶ 57, 59.)

Notably, none of the signals or structures described in the cited documents perform the function of “enabl[ing]” a circuit to reduce standby current—all of them relate only to **disabling** some circuit to reduce current. (*See* Shanfield Decl. ¶ 60.) Dr. Taylor argues that “the labels ‘ENABLE’ and ‘ENABLE/DISABLE’ are interchangeable, and refer to the same structure,” but Dr. Shanfield explains that not all “enable” circuitry implies the capability to perform “disabling,” nor vice versa. (*See id.* ¶¶ 61-62.) And neither Dr. Taylor nor Microchip offers any explanation as to how an “enable/disable function” could **enable** the biasing circuit to **reduce** current, much less that the ’074 patent claims and discloses structure that could perform such a function. The evidence therefore demonstrates that the claim term “an enable/disable function to enable/disable the biasing circuit for reducing standby current” would not be understood to have

a sufficiently definite meaning as the name for a class of structure, such that the claim limitation must be construed as a means-plus-function term under § 112 ¶ 6.

2. The claim is indefinite because the '074 patent fails to disclose adequate structure to perform the recited functions of “enabl[ing]/disabl[ing] the biasing circuit for reducing standby current.”

“Where there are multiple claimed functions, as we have here, the patentee must disclose adequate corresponding structure to perform all of the claimed functions.” *Williamson*, 792 F.3d at 1351-52. The term at issue here recites at least two functions: enabling and disabling the biasing circuit for reducing standby current. As Dr. Taylor’s declaration demonstrates, the ’074 patent discloses structures that are related only to *disabling* the bias circuit to reduce standby current. (See Taylor Decl. ¶ 63 (quoting ’074 at 4:44-5 (explaining that bias circuit “[t]ransistors 320, 330, 334 and 336 may be shut off during disabling/power down operation to make sure this circuit will consume substantially no DC current.”)).) Because there is apparently no dispute that the ’074 patent fails to disclose any structure for the claimed function of “enabl[ing]... the bias circuit for reducing standby current,” this alone renders the term indefinite. See *Williamson*, 792 F.3d at 1354 (affirming invalidity of a means-plus-function term where the specification failed to disclose adequate corresponding structure for one of three claimed functions).

But with respect to the “disabl[ing]” function of the claim term, the ’074 patent fails to disclose adequate structure for that claimed function. Microchip contends that if the Court finds that the requirements of means-plus-function claiming apply, the “enable/disable signal input line (Node M)” is the structure that corresponds to the claimed function. (Op. Br. at 16-17; Taylor Decl. ¶¶ 62-63.) As Dr. Shanfield explains, the term “node” is “well-understood by a POSITA to be a region of constant voltage or, equivalently, a section of uninterrupted, highly conductive wire. In circuit design, the term “node” thus refers to a connection from one portion

of a circuit to another, or refers to a region of constant voltage on such a connective wire.”

(Shanfield Decl. ¶ 64.) As set forth below, Node M connects one section of circuitry to another, carrying signals between them, and the sets of circuitry on both sides of Node M are required to perform the function of turning the bias circuit on and off. Microchip’s expert admits that there is a group of transistors—connected after Node M in a specific arrangement depicted by Figure 3—that must be shut on or off based on a signal received through Node M to “thereby eliminat[e] the power drawn by both the bias circuits in Figure 3 of the ’074 patent.” (See Taylor Decl. ¶ 63.) The structure that is disclosed in the ’074 patent thus requires *at least* these transistors, arranged as disclosed in Figure 3, to perform the claimed function of “disabl[ing] the bias circuit for reducing standby current.” However, even the combination of these transistors with signal input line Node M is insufficient to perform the function of enabling/disabling the bias circuit: there must also be some structure, which is not disclosed anywhere in the ’074 patent, on the other side of Node M for creating and switching on/off the signal carried by Node M. (See Shanfield Decl. ¶ 65.) The patent does not disclose any such structure. (*Id.*) Because the ’074 patent therefore lacks adequate corresponding structure to perform the claimed functions of “enabl[ing]/disabl[ing] the biasing circuit for reducing standby current,” the term should be found invalid for indefiniteness.

C. Term 4: “wherein the gm-boost circuit enables the current buffer driver to have a large gm value”

No.	Claim Term	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
4	“wherein the gm-boost circuit enables the current buffer driver to have a large gm value”	Not Indefinite. Plain and Ordinary Meaning. Alternatively, “wherein the gm-boost circuit increases the gm value of the current buffer driver”	Indefinite

	'074 patent, claim 4		
--	-------------------------	--	--

The term “large gm value” is indefinite because it fails to inform a POSITA with reasonable certainty of the scope of the invention. *See Nautilus, Inc. v. Biosig Inst., Inc.*, 572 U.S. 898, 901 (2014). Even after reading the claims, specification, and prosecution history, a POSITA is left to wonder what constitutes a “large” gm value¹, as opposed to a “fairly large” gm value, or some other amount of transconductance.

Microchip concedes that “large gm value” is a term of degree. (Op. Br. at 17.) As such, it is indefinite unless the intrinsic record “provide[s] objective boundaries for those of skill in the art” to determine the scope of the claims. *Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1371 (Fed. Cir. 2014). Here, though, neither the specification nor the prosecution history provide any such boundaries. On the contrary, the U.S. prosecution history includes the findings of the International Searching Authority (“ISA”) which determined the term “large gm value” to be “vague and indefinite” because it was “not clear how large a gm value needs to be to be considered ‘large’.” (D.I. 66-7 at MCHP_00004159-60.) The ISA encouraged Microchip to amend the term to allow a “skilled person to objectively establish whether a certain gm value is large enough to fall within the scope of the claim.” (*Id.* at MCHP_00004159-60.) Microchip, however, made no such amendment.

The ISA was correct: the term lacks an objective boundary even in view of the intrinsic record. The term “large” appears only in claim 4, and the surrounding claims do not provide any insight into its meaning. Nor is the specification illuminating; the phrase “large gm value” appears only twice and is not defined. (*See* '074 patent at 2:6, 4:15.)

¹ gm is the common shorthand for transconductance—the ratio of current coming out of a component to the voltage going into that component. (Shanfield Decl. ¶ 45.)

In an attempt to invent an objective boundary, Microchip improperly conflates “large gm value” with a gm value sufficient to create a pole-splitting effect. There is, however, no support for this interpretation in the specification. In its opening brief, Microchip relies on a passage stating that “the current buffer driver 204 pushes this pole to a high frequency beyond unity-gain frequency due to its low-impedance characteristics in order to get the pole splitting effect. To achieve this, it is necessary to provide a fairly large gm value of the current buffer driver 204.” (’074 patent at 4:11-4:15.) Rather than clarifying the scope of the claim, this passage creates more confusion. As Microchip notes, the specification says that pole-splitting cannot be achieved without a “*fairly* large gm value.” (Op. Br. at 18 (emphasis added).) But the specification does not explain the difference between this “fairly large gm value” and the claimed “large gm value.” *See Intell. Ventures I LLC v. AT&T Mobility LLC*, No. CV 13-1668-LPS, 2016 WL 4363485, at *17 (D. Del. Aug. 12, 2016), *rev’d in-part on other grounds, sub nom. Intell. Ventures I LLC v. T-Mobile USA, Inc.*, 902 F.3d 1372 (Fed. Cir. 2018) (finding the claim term “large” indefinite where the specification’s use of “relatively large” caused confusion). And if a *fairly* large gm value may be sufficient to create pole-splitting, it is unclear if the ability to create pole-splitting can be the defining characteristic of a “**large** gm value.” *See CAE Screenplates, Inc. v. Heinrich Fiedler GmbH & Co. Kg*, 224 F.3d 1308, 1317 (Fed. Cir. 2000) (noting that in claim construction, different claim terms generally have different meanings).

Nor could the ability to generate pole-splitting serve as a reasonable metric for the required measure of the gm value. The amount of transconductance required to generate a pole-splitting effect depends on the operational frequency of the amplifier—a value that changes depending on the load being driven by the voltage regulator. (Shanfield Decl. ¶ 70.) Because the entire purpose of a voltage regulator is to provide a constant voltage in spite of changing loads, a

POSITA would understand that the frequency of the amplifier—and therefore the amount of transconductance required to generate a pole-splitting effect—would be expected to change regularly. Thus, in Microchip’s attempt to provide stability for the scope of its claims it actually pins the claim scope to a moving target, making it impossible for a POSITA to determine with reasonable certainty whether a given gm value is sufficiently large to fall within the scope of the claim. (*Id.*)

Microchip’s alternative proposed construction—“wherein the gm-boost circuit increases the gm value of the current buffer driver”—is equally problematic. First, it omits the very pole-splitting effect that purportedly defines the term “large gm value.” Second, Microchip seeks to improperly broaden the claim by requiring only an “increase” in gm value as opposed to a gm value exceeding a certain threshold. Under such a construction, a “large gm value” would include a trivially small gm value insufficient to generate pole-splitting so long as that gm value were in some way increased by the gm-boost circuit. Thus, far from defining the term “large gm value,” Microchip’s proposed construction reads the limitation out of the claim entirely.

D. Term 5: “low gain and high bandwidth amplifier”

No.	Claim Term	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
5	“low gain and high bandwidth amplifier” '074 patent, claims 8, 9	Not Indefinite. Plain and Ordinary Meaning. Alternatively, “amplifier optimized for high bandwidth with a commensurate reduction of gain”	Indefinite

The '074 patent’s requirement of a “low gain and high bandwidth amplifier” provides insufficient guidance to inform a POSITA, with reasonable certainty, of the scope of the claimed invention. *Nautilus, Inc. v. Biosig Inst., Inc.*, 572 U.S. 898, 901 (2014). Here, neither the claims nor the specification give context that would allow a POSITA to know when an amplifier is

sufficiently “low gain” or sufficiently “high bandwidth” to satisfy the claims’ limitations.

Without such guidance, it is impossible to determine with reasonable certainty whether a given product falls within the scope of the claim.

In the context of an amplifier, gain is a measurement of the increase in the voltage of a signal from the input of the amplifier to the output. (Shanfield Decl. ¶ 40.) Gain is measured in decibels (dB), with 0 dB indicating no change in voltage across the amplifier (known as “unity gain”), positive measurements indicating an increase in voltage across the amplifier and negative measurements indicating a decrease in voltage. (*Id.*) The problem presented by the ’074 patent’s reference to “low gain” is that it is unclear at what point an amplifier may be considered “low gain”—unity gain? 5dB? 10 dB? 40 dB?—because the specification provides no objective metric by which to make this determination. *See Dow Chem. Co. v. Nova Chems. Corp. (Canada)*, 803 F.3d 620, 635 (Fed. Cir. 2015) (finding a term indefinite for failing to disclose a method by which to determine whether a claim parameter was met). Without guidance from the specification, a POSITA is left “to consult the unpredictable vagaries of any one person’s opinion.” *Id.*

Microchip’s argument that this term refers to an Op Amp configured at “the opposite end” of the gain-bandwidth spectrum from a “traditional” Op Amp provides no useful guidance. This formulation merely swaps one undefined term (“low” or “high”) with another undefined term (“the opposite end”), and does nothing to inform a POSITA when gain is sufficiently low or bandwidth is sufficiently high to fall within the claims’ scope. (Shanfield Decl. ¶ 76.) Compounding this problem is the fact that all Op Amps have an inherent gain-bandwidth product (GBP) which can differ by orders of magnitude from one Op Amp design to another. (*Id.* ¶ 77.) As a result, two Op Amps configured to provide identical gain could produce wildly different

bandwidths, and two Op Amps configured to provide identical bandwidths could produce wildly different gain. (*Id.* ¶ 78.)

Microchip’s contention that this limitation sets a **base** for the amount of gain required, not a ceiling as would ordinarily be understood by the use of the term “low” only adds further to this ambiguity. In its brief, Microchip points to a portion of the specification stating that an amplifier may provide “good driving capability” and on this basis argues that claims 8 and 9 require an operational amplifier that balances “(1) having sufficient bandwidth such that it forms only a single pole; but (2) still offering sufficient gain to drive the current buffer.” (Op. Br. at 21.) Far from clarifying the scope of the claims, the requirement of **sufficient** gain creates yet another ambiguous boundary—this time on the **lower** end of the scale. (Shanfield Decl. ¶ 80.) Under this interpretation, a POSITA would have to determine not only when an amplifier is sufficiently “low gain,” but also whether it offers “sufficient gain” to drive the current buffer. (*Id.*) Because nothing in the intrinsic record offers guidance as to either boundary, the term “low gain and high bandwidth amplifier” is indefinite for failing to provide a POSITA with “reasonable certainty” regarding the scope of the claim.

POTTER ANDERSON & CORROON LLP

OF COUNSEL:

Daralyn J. Durie
Timothy Saulsbury
Eric C. Wiener
Andrew L. Perito
Joyce C. Li
Tannyr Pasvantis
MORRISON & FOERSTER LLP
425 Market Street

By: /s/ Philip A. Rovner

Philip A. Rovner (#3215)
POTTER ANDERSON & CORROON LLP
Hercules Plaza
P.O. Box 951
Wilmington, DE 19899
(302) 984-6000
provner@potteranderson.com

*Attorneys for Defendant
Aptiv Technologies Limited*

San Francisco, CA 94105
(415) 268-7000

Andrew T. Jones
MORRISON & FOERSTER LLP
2100 L St., NW
Suite 900
Washington, D.C., 20037
(202) 887-1500

W. Henry Huttinger
MORRISON & FOERSTER LLP
707 Wilshire Blvd.
Los Angeles, CA 90017
(213) 892-5200

Dated: March 22, 2024

CERTIFICATE OF SERVICE

I, Andrew T. Jones, hereby certify that on March 22, 2024, I served copies of the foregoing document by electronic transmission to the email addresses listed below:

BY EMAIL

Jack B. Blumenfeld
Brian P. Egan
Travis J. Murray
Morris, Nichols, Arsht & Tunnell LLP
1201 North Market Street
P.O. Box 1347
Wilmington, DE 19899
(302) 658-9200
jblumenfeld@mnat.com
began@mnat.com
tmurray@morrisnichols.com

John M. Neukom
Barbara N. Barath
Yuqing Cui
Alexander H. Lee
DEBEVOISE & PLIMPTON LLP
650 California Street, Floor 31
San Francisco, CA 94108
Telephone: (415) 738-5700
jneukom@debevoise.com
bnbarath@debevoise.com
ycui@debevoise.com
ahlee@debevoise.com
ajkuang@debevoise.com
Microchip-All@debevoise.com

Andrew Gish
Edward Tulin
GISH PLLC
41 Madison Avenue, Floor 31
New York, NY 10010
Telephone: (212) 518-2000
andrew@gishpllc.com
edward@gishpllc.com

Ryan K. Iwahashi
GISH PLLC
50 California Street, Suite 1500
San Francisco, CA 94111
(415) 630-8960
ryan@gishpllc.com

Attorneys for Plaintiff
MICROCHIP TECHNOLOGY INC.

/s/ Andrew T. Jones

Andrew T. Jones

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

MICROCHIP TECHNOLOGY INC.,

Plaintiff,

v.

APTIV TECHNOLOGIES LTD.,

Defendant.

Civil Action No. 1:23-cv-00778 (JDW)

JURY TRIAL DEMANDED

DECLARATION OF STANLEY SHANFIELD, PHD

I. INTRODUCTION

1. I have been retained on behalf of Defendant Aptiv Technologies Limited (“Aptiv”) in this case and have been asked to offer an opinion on the disputed claim terms in U.S. Patent Nos. 7,564,665 (the “’665 patent”) and 9,471,074 (the “’074 patent”) and how they would be understood by a person of ordinary skill in the art (“POSITA”).

2. All of the opinions in this report are based on my personal knowledge and professional judgment. If called as a witness, I am prepared to testify competently about them.

3. I am being compensated for my time spent on this matter at by standard consulting rate. My compensation is in no way dependent upon the substance of my opinions, my testimony, or the outcome of this litigation, nor do I have a personal interest in the outcome of this litigation.

4. My opinions are based on the information I have received and reviewed and the analysis I have carried out to date. I reserve the right to supplement, clarify, modify and/or change my testimony as additional facts, questions, or issues come to my attention.

II. MATERIALS CONSIDERED

5. In connection with the preparation of this declaration, I have reviewed the ’665 and ’074 patents, their respective prosecution histories, the parties’ respective preliminary claim constructions and the evidence identified in the Joint Claim Construction Statement (D.I. 65) and accompanying appendix (D.I. 66), Microchip’s Opening Claim Construction Brief, and the declaration of Dr. Greg Taylor in support of Microchip’s Opening Claim Construction Brief (including exhibits).

III. EXPERIENCE AND QUALIFICATIONS

6. I have four decades of professional experience as a practicing engineer in the field of semiconductor fabrication, circuit design, and electronic module design and fabrication. My

professional qualifications, experience, publications, presentations, the patents on which I am a named inventor, and a list of previous cases in which I have provided expert testimony are set forth in my curriculum vitae, attached as **Exhibit A**.

7. I received my Bachelor of Science degree in Physics from the University of California, Irvine, in 1977. I received my Ph.D. from the Massachusetts Institute of Technology (“MIT”) in 1981, with a dissertation on high field superconductors. During my doctoral program at MIT, I received a four-year scholarship from the Energy Research and Development Administration (now part of the United States Department of Energy)

8. After earning my Ph.D. in 1981, I began work as a Staff Scientist, then later as a Senior Staff Scientist, at Spire Corporation in Bedford, Massachusetts. At Spire Corporation, I developed new methods for low temperature deposition of plasma-assisted chemical vapor deposition (“CVD”) epitaxial silicon. I also built, operated, and characterized an ion-assisted deposition system for making coatings for semiconductors.

9. In 1985, I joined Raytheon Corporation, located in Lexington/Andover, Massachusetts, as a Section Manager in Semiconductors & Integrated Circuits. My work focused on developing processes for the fabrication of high power, high frequency multifunction integrated circuits. In 1992, I was promoted to Research Laboratory Manager, where I led a 90-person team developing high performance semiconductor devices and circuits, including measurement, assembly, and wafer fabrication processes. My work then focused on the design, fabrication, and measurement of state-of-the-art complimentary metal-oxide semiconductor (“CMOS”) devices of the time, primarily for digital and mixed signal applications.

10. I have had several years of experience in the design, fabrication, and testing of LDO regulators in various development programs at Raytheon Research Division during the 1990s.

This experience initially involved a focus on design issues like maintaining low noise supply voltages, maximal conversion efficiency, and stability over temperature. As higher performance regulator ICs became commercially available, I supervised their evaluation and employed them in numerous module designs.

11. In 1996, I was promoted to Manager of Semiconductor Operations. In this capacity, I was involved in all aspects of CMOS-based IC fabrication. I was also responsible for a custom silicon application-specific integrated circuit (“ASIC”) design and development group and the associated layout and simulation facilities. I was directly involved in the design of certain commercial products produced in the facility, including flip-chip modules for an AT&T wireless base station, and the transmit/receive modules for Iridium satellite handsets using chip-on-board (COB).

12. After 14 years at Raytheon, I became part of the founding team for AXSUN Technologies, located in Bedford/Billerica, Massachusetts, as a Vice President of Operations in 1999. In this capacity, I designed a complete facility for semiconductor processing, including establishing a fabrication facility in Belfast, North Ireland for producing thick oxide silicon-on-insulator material.

13. In 2003, I joined Draper Laboratory at MIT (“Draper”), located in Cambridge, Massachusetts, where I am still employed. Currently, I am the Division Leader of Advanced Hardware Development and am a Distinguished Member of Technical Staff and Technical Director. In my time at Draper, I have been responsible for in-house module and electronic system designs and have been involved in CMOS foundry implementation for multiple ASIC designs.

14. I have been a member of many professional societies and electrical engineering industry groups over the years, such as the Institute of Electrical and Electronics Engineers (IEEE) and the American Physical Society (APS).

15. I have received a number of academic awards and honors over the years, including awards and honors for the best Draper patent and most successful Draper development project.

16. I have also authored or co-authored over 25 technical papers covering various aspects of semiconductor devices and advanced semiconductor manufacturing.

17. I am a named inventor or co-inventor on multiple patents covering aspects of semiconductor devices, system and circuit design, and semiconductor manufacturing.

IV. LEGAL PRINCIPLES

18. I have been informed of the following legal principles, which I applied in conducting the analyses expressed in this declaration.

A. General Principles of Claim Construction

19. I understand that the purpose of claim construction is to give claim terms the meaning understood by a POSITA at the time of the claimed invention, when considered in the context of the patent.

20. I understand that claim terms are interpreted in the context of not only the claim in which the disputed term appears, but in the context of the entire patent, including the specification. I also understand that history of that patent's prosecution before the U.S. Patent & Trademark Office is relevant to the meaning of the claims.

21. To that end, I understand that that claims are not to be interpreted in a vacuum and must be considered within the context of this intrinsic evidence. I understand that this "intrinsic evidence" includes the subject patent itself, the history of that patent's prosecution before the U.S. Patent & Trademark Office, patents (or other materials) incorporated by reference into the

subject patent, and patents (or other materials) cited to or by the PTO during the prosecution of the subject patent.

22. I further understand that dictionary definitions and other extrinsic evidence may be considered in understanding claim terms but may not be used to vary the meaning given to a claim term in the intrinsic evidence.

B. Construing Claims Written According to 35 U.S.C. § 112 ¶ 6 (pre-AIA)

23. I understand that, according to 35 U.S.C. §112 ¶ 6, an element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such a claim must be construed to cover only the corresponding structure, material, or acts described in the specification and equivalents thereof.

24. I understand that, with this provision, Congress struck a balance in allowing patentees to express a claim limitation by reciting a function to be performed rather than by reciting structure for performing that function, while placing specific constraints on how such a limitation is to be construed, namely, by restricting the scope of coverage to only the structure, material, or acts described in the specification corresponding to the claimed function, and equivalents thereof.

25. When a claim term lacks the word “means,” there is a presumption that that term is not subject to §112 ¶ 6. I understand, however, that that presumption is not a strong presumption and can be overcome. I further understand that the “essential inquiry” is whether the words of the claim are understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the name for structure. Where the words of the claim fail to recite sufficiently definite structure or else recites function without reciting sufficient structure for performing that

function, I understand that the presumption is overcome and the corresponding claim term must be construed according to §112 ¶ 6.

26. I understand when a limitation is to be construed according to §112 ¶ 6, a POSITA must be able to identify the corresponding structure in the specification that is adequate to perform the claimed function or all of the claimed functions in the event there are multiple claimed functions. I further understand that if a specification fails to disclose corresponding structure adequate to perform the claimed functions, the claim is indefinite.

C. Indefiniteness

27. I understand that a patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention. I understand that while absolute precision in the claim language is impossible, the patent must provide objective boundaries as to the scope of the claimed subject matter. I further understand that a patent is presumed valid, and therefore, that indefiniteness must be shown by clear and convincing evidence.

D. Person of Ordinary Skill in the Art

28. In my opinion, a person of ordinary skill in the art in the field of the '665 and '074 patents, would have had at least a Master's degree in electrical engineering, computer engineering, or a related field and three to five years of experience in integrated circuit device design. Additional education may substitute for some work experience and relevant work experience may substitute for additional formal education.

29. My educational background and my level of experience in integrated circuit device design is more than is necessary for a person of ordinary skill in the art. My opinions regarding

the meaning of claim terms are analyzed from the perspective of a person of ordinary skill in the art.

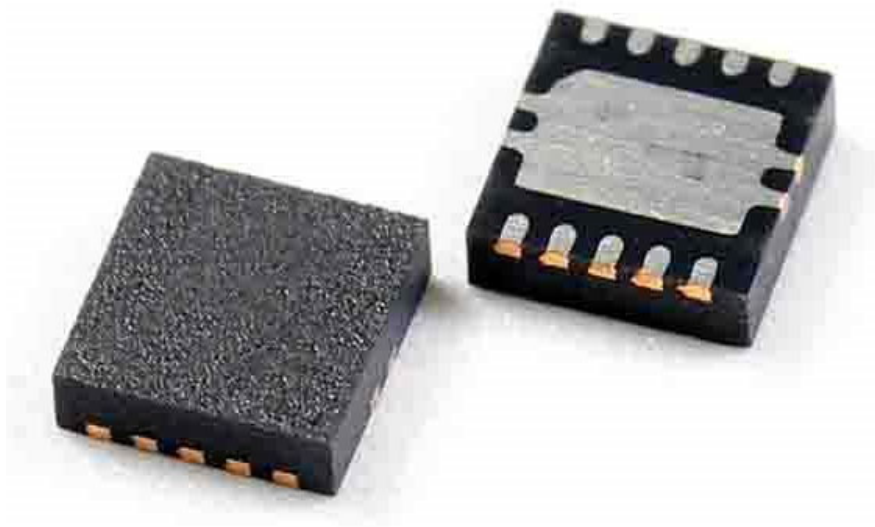
V. TECHNICAL BACKGROUND

A. Electrostatic Discharge Protection

30. The '665 patent is directed to a system for providing electrostatic discharge (“ESD”) protection to an input/output circuit. Electrostatic discharge refers to the release of static electricity when two objects with different electrical potentials come into contact with one another. It is the same phenomenon we experience when walking around the house in socks on a cold day, but in the context of sensitive electronics this discharge of electricity can be very damaging. This is especially true as electronic devices have gotten smaller and, in an effort to be more energy efficient, are designed to operate on less power. Small electrical components designed to handle small voltages may be irreparably harmed by the sudden discharge of larger amounts of electrostatic energy.

31. Because of this, nearly all integrated circuits manufactured today include some form of protection against electrostatic discharge. Some common methods include transient voltage suppressor diodes, reverse bias Zener diodes, varistors, fuses, and certain MOSFET circuit configurations. The common thread through all of these methods is to shunt the ESD away from sensitive components and either direct it out of the system in its entirety or dissipate it across components designed to handle large surges of electrical power. The '665 patent describes employing both approaches.

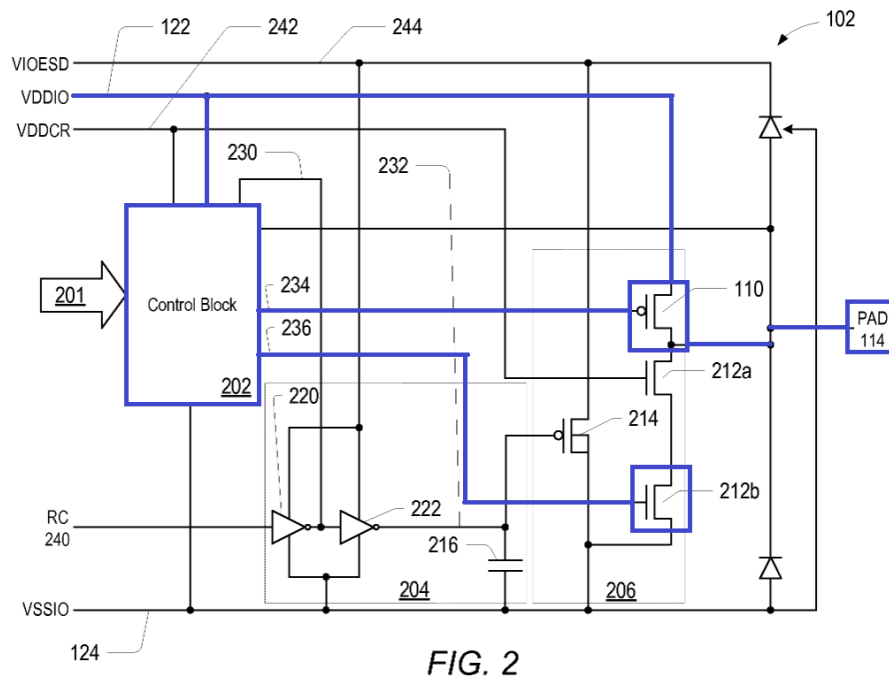
32. The circuits described in the '665 patent are only a small portion of an overall integrated circuit. They concern only the interface of the overall IC—that is, the point at which signals enter and exit the chip. This is accomplished by the use of a physical “pad”—an exposed metal contact point as can be seen in the image below:



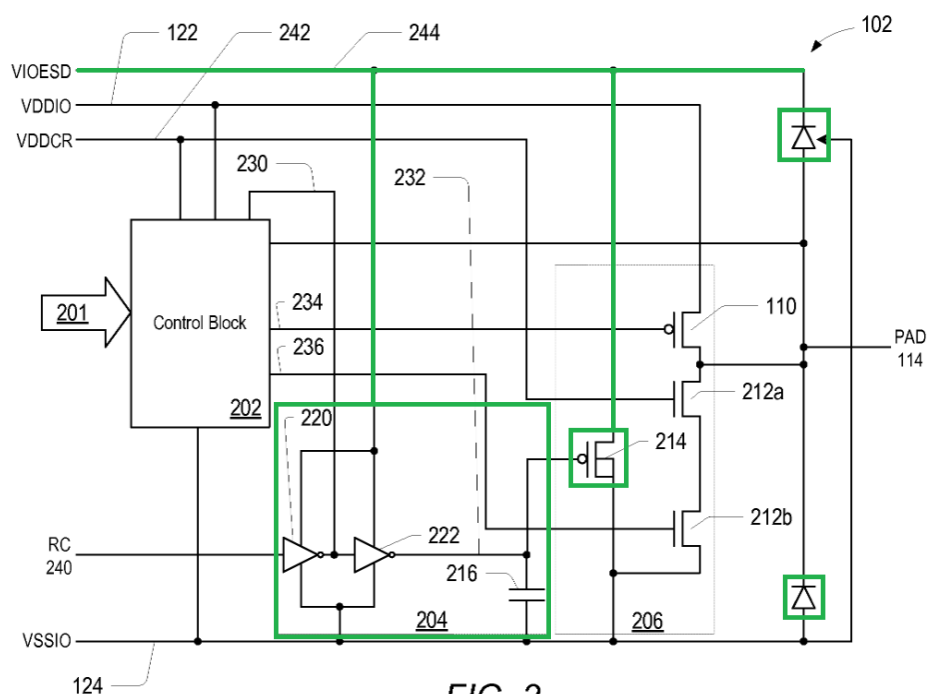
33. The circuits described in the '665 patent generally consist of two separate systems—components designed for ESD protection and components designed for normal (i.e., non-ESD) operations. In other words, the circuit describes both what is being protected and what is doing the protecting.

34. The circuit being protected is a generic input/output circuit which is designed to send and receive signals using the physical pad. There are three primary portions of the I/O system in the '665 patent: (1) a “control block”, (2) an “output buffer”, and (3) the physical pad itself. The patent explains that the control block “may contain logic circuitry to perform various functions associated with pad circuit 102, for example receiving I/O data, address information, and various system control signals 201 in order to perform I/O functions for the system.” ('665 patent at 4:39-43.) One of those functions is “the control of the output buffer 206 to drive an output signal at pad 114.” ('665 patent at 4:53-54.) An output buffer is an important component of any I/O system because it is what converts the smaller voltage signals used within the chip itself into the larger voltage signals that can be passed on beyond the chip. The final component of the I/O

system is the physical pad itself, which serves as the physical interface through which signals enter and exit the chip. *See* annotated Fig. 2:



35. The remaining components of the circuit described in the '665 patent are devoted to protecting the I/O system in the event of a ESD event. In the system shown in Figure 2, this is comprised primarily of the “enable circuitry,” the clamp device, and a pair of unlabeled diodes. *See* annotated Fig. 2:



36. In the system shown in Figure 2, the voltage supplying the I/O components is provided by a voltage rail labeled “VDDIO,” and the voltage supplying the ESD components is provided by a second, separate voltage rail labeled “VIOESD.” The patent describes that the VIOESD rail serves an additional purpose because it allows the system to detect the incidence of an ESD event and power up the clamp control circuit in response. *See* ’665 patent at 5:9-13 (“When an ESD even occurs, the fast ramp rate of a voltage spike on VIOESD rail 244 may result in VIOESD rail 244 providing increased power to clamp control circuit 204, thereby facilitating clamp control circuit 204 asserting ESD control signal 230.”)

B. Voltage Regulators

37. A voltage regulator is a standard electronic circuit that is designed to generate a fixed output voltage irrespective of the input voltage or the device that is being supplied by the regulator. Voltage regulators are exceedingly common because it is important for devices to have a reliable voltage source and avoid dips or surges that may damage components or simply

cause the device not to work in the way it was designed. There are many different voltage regulator designs ranging from something as simple as a resistor in series with a diode to far more complicated systems when higher efficiency or tighter tolerances are required.

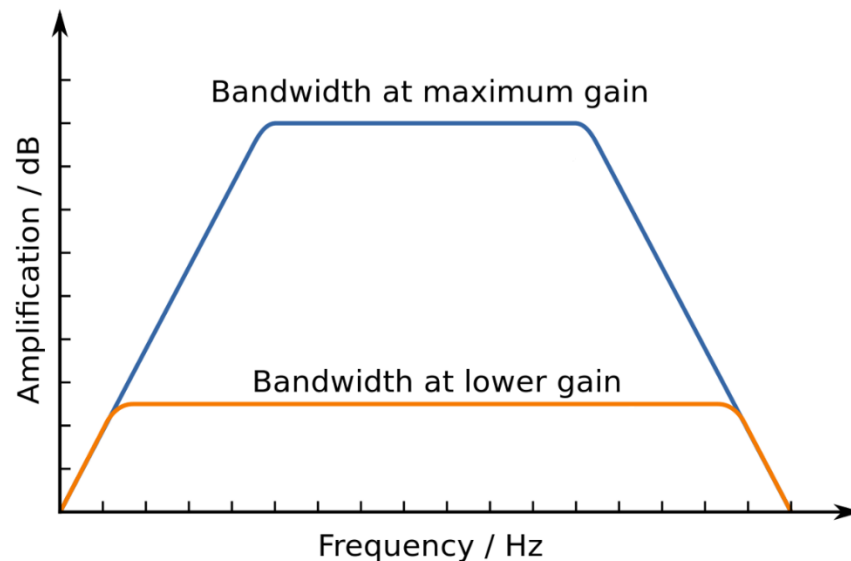
38. The particular type of regulator described in the '074 patent is a “low drop-out” or “LDO” regulator. Traditional voltage regulators are typically designed to work with a significant difference between the incoming voltage and the desired output voltage and often struggle to generate a constant voltage when the incoming voltage is close to the desired output. LDO regulators are designed to avoid this problem. Given the relatively small voltages within many modern consumer electronics, this is a highly desirable feature and LDO regulators have become the standard design choice for most consumer applications.

39. LDO voltage regulators are, at their simplest, comprised of an amplifier and some manner of feedback loop. Amplifiers are electronic devices that take an incoming signal and amplify it to make it stronger. Many are familiar with amplifiers in the context of sound systems, where they take a small signal generated by, for instance, a record player, and amplify that signal to the point that it is strong enough to drive a speaker system. Instead of sound frequencies, a typical electronic regulator amplifies a fixed DC reference voltage (the input), maintaining a stable output voltage regardless of load variability occurring at the output.

40. The amount by which an input is amplified is referred to as “gain.” The amount of gain is measured in decibels (dB). The decibel scale is a logarithmic one, with each 10 dB increase correlating to a ten-fold absolute increase in voltage. As an example, a gain of 10 dB across an amplifier would take a 0.5 V input and generate a 5V output. A 20 dB gain would take that same 0.5 V input and generate a 50V output. When there is no change in voltage from input to output, gain is equal to 0 dB and is often referred to as “unity gain.”

41. In the context of an amplifier, the term “bandwidth” refers to the range of frequencies over which an amplifier is able to generate a signal. An amplifier is unable to generate a signal at a frequency beyond the range of its bandwidth. This again, can be seen in the context of music—the attenuation of high or low frequency is the result of reducing the bandwidth of an amplifier to the point that it cannot amplify sound at the high and/or low end of the frequency range, resulting in distortion. Similarly, a regulator can maintain a fixed output voltage only when the frequency of variability of the load is within its bandwidth.

42. There is a largely fixed relationship between gain and bandwidth—as gain increases, bandwidth decreases and vice versa. This relationship can be seen in the figure below:



43. The combined value of these two metrics is referred to as the “gain-bandwidth product” (“GBP”) and is a set value for a given amplifier. Over the relevant frequency range, bandwidth can never exceed the gain-bandwidth product regardless of how small the gain, and gain can never exceed the gain-bandwidth product regardless of how narrow the bandwidth.

44. The specific type of amplifier discussed in the '074 patent is an “operational amplifier” or “Op Amp.” Op Amps differ from traditional amplifiers because, instead of taking

a single input and providing a single output, Op Amps take two different inputs, compare them, and use the *difference* between those inputs to determine the value of the output.

45. Another concept addressed in the '074 patent is transconductance, often shortened to “gm.” Transconductance is closely related to the type of gain discussed above, but instead of measuring the increase in *voltage* across an amplifier output, it measures the increase in output *current* in relation to the input voltage. Given a fixed input voltage, the larger the transconductance, the greater the resulting output current.

VI. PROPOSED CONSTRUCTIONS

A. '665 Patent, Claim 1 – “second voltage rail”

46. I understand that Microchip and Aptiv proposed different constructions for the term “second voltage rail,” a term that appears in claim 1 of the '665 patent. It is my understanding that the proposed constructions are:

No.	Claim Term	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
1	“second voltage rail” '665 patent, claim 1	Plain and Ordinary Meaning Alternatively, “a second voltage rail that is distinct from the third voltage rail but may or may not be distinct from the first voltage rail”	“a second voltage rail that is distinct from the first voltage rail”

47. Claim 1 provides (with relevant terms in bold):

1. A pad circuit configured to provide protection against electrostatic discharge (ESD) in a system comprising the pad circuit, the pad circuit comprising:

a first node coupled to a **first voltage rail**;

a second node coupled to a physical pad having capacitance;

one or more output transistor devices coupled between the first node and the second node, and operable to at least partially drive an output signal at the second node;

a control block configured, to turn on, when instructed, at least one of the one or more output transistor devices to charge the pad capacitance to reduce a maximum voltage developed in the system as a result of the ESD event;

a clamp device configured between a **second voltage rail** and a **third voltage rail** to reduce, when turned on, the maximum voltage developed in the system as the result of the ESD event;

enable circuitry configured to turn on the clamp device and instruct the control block to turn on the at least one of the one or more output transistor devices, in response to the ESD event;

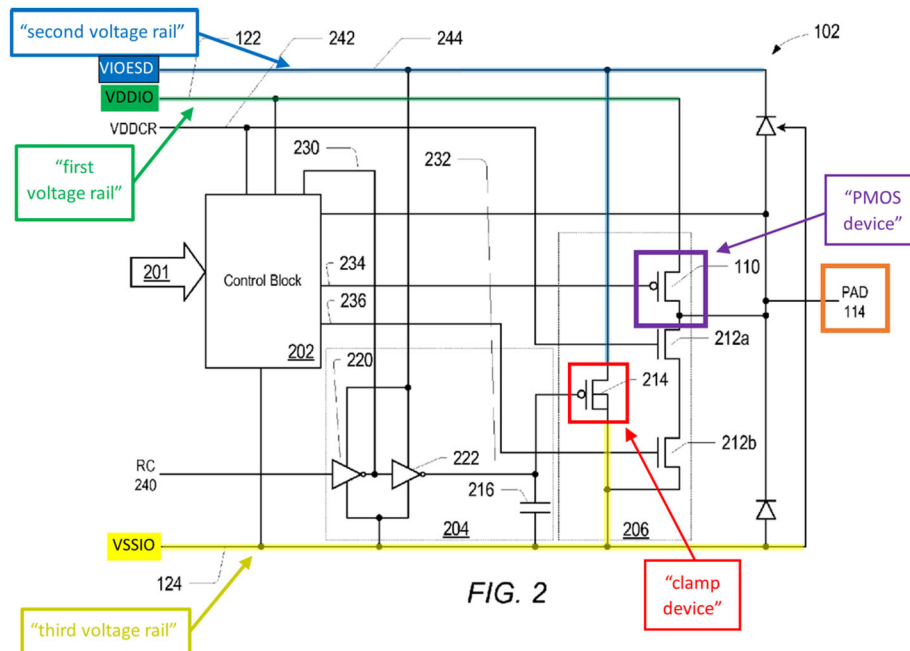
wherein the **second voltage rail** is configured to provide power to the enable circuitry, and wherein the **third voltage rail** has a value below the first voltage rail.

48. In my opinion, a POSITA would understand the term “second voltage rail” to refer to a voltage rail that is distinct from the “first voltage rail” discussed in the claim.

49. As an initial matter, the language of the claim itself clearly differentiates between the first and second voltage rails. A POSITA reading claim 1 would understand its requirement of a “first” and “second” voltage rail to require two distinct voltage rails.

50. The specification provides further support for this understanding. In describing the circuit shown in Figure 2, the specification explains that “[i]n pad circuit 102, PMOS device 110 represents one or more PMOS devices coupled between VDDIO rail 122 and PAD 114.” (’665 patent at 4:34-35.) This corresponds to the requirement in claim 1 of “one or more output transistor devices coupled between the first node [first voltage rail] and the second node [physical pad having capacitance].” (’665 patent at claim 1). The specification next explains that “[p]ad circuit 102 may also include a supply rail (VIOESD) 244 used to power up clamp control circuit 204.” (’665 patent at 5:1-3.). This corresponds to the requirement in claim 1 of a “second voltage rail [] configured to provide power to the enable circuitry” which is “configured

to turn on the clamp device...” (’665 patent at claim 1.) These structures are shown in the annotated Figure 2 provided by Microchip’s expert, Dr. Taylor.



51. The specification then describes an alternate embodiment—different from the one shown in Figure 2. It states that “VIOESD 244 and VDDIO 122 may in fact be the same power/supply rail, and alternate embodiments may be configured with a single power rail providing power to the circuit and/or system components that are powered by VIOESD 244 and VDDIO 122 in the embodiment shown in FIG. 2. In general, the ESD rail and the power supply rail can be the same supply rail, and separate supply rails (e.g., VIOESD 244 and a distinct VDDIO 122) may not be required.” (’665 patent at claim 1.) In my opinion, a POSITA would read this to be a general statement that a single rail could be used to power both the ESD protection components of circuit 102 (powered by VIOESD) and also the general I/O components of the circuit (powered by VDDIO). I do not dispute that it is possible to configure such a circuit, but a POSITA would understand, however, that the two arrangements are not

identical to one another and there are reasons that a POSITA may choose one arrangement over the other.

52. For instance, A POSITA would recognize that the electrical behavior of circuits taught in the '665 patent would be quite different with three voltage rails when compared to a two-rail design obtained by combining rails. The difference can be explained by examining Fig. 2, with the schematic having three distinct voltage rails, VIOESD, VDDIO, and VSSIO as drawn. An ESD event beginning on Pad 114 (the “second node”) would trigger activation of an output device to reduce the maximum voltage induced by the ESD. This strategy is preferred, as it avoids dissipating the unwanted ESD energy within any transistor. For added protection, the clamp device (214) is activated to minimize the voltage developed across other portions of the system, i.e., between VSSIO and VIOESD. The action of the clamp as a voltage limiter in the three-rail version would not the operation of the remainder of the circuit.

53. In contrast, a POSITA would understand the alternate embodiment where voltage rails VIOESD and VDDIO are combined as a single rail (i.e., make the first and second voltage rail the same rail) to operate differently. In this case, an ESD event at Pad 114 would similarly activate both the clamp transistor 214 and the output transistor. However, the clamp device in this case would rapidly reduce the source voltage at the output transistor. As a result, considerably more of the ESD-generated energy would be absorbed in clamp device 214, and the clamp transistor would have to become larger accordingly. In the three-rail version represented in Fig. 2, ESD energy is not primarily dissipated within transistors—this benefit is reduced with the alternate two voltage rail embodiment, and more ESD energy is dissipated within transistors.

54. This alternate two-rail embodiment correlates more closely to the embodiment in claim 6 of the '665 patent. Like claim 1, claim 6 comprises an “output buffer,” a “control

block,” and “clamp device.” But unlike claim 1, claim 6 describes only two voltage rails—a “first supply rail” and a “low supply rail.” The “low supply rail” corresponds to the “third voltage rail” from claim 1, while the first supply rail corresponds to the functions of the “second voltage rail.” No separate voltage rail for the I/O functions is discussed.

Claim 1	Claim 6
“a clamp device configured between a second voltage rail and a third voltage rail”	“a clamp device coupled between a first supply rail and a low supply rail”
“wherein the second voltage rail is configured to provide power to the enable circuitry” which is “configured to turn on the clamp device”	“wherein the first supply rail is configured to provide power to the control circuit” which is “configured to turn on the clamp device”

B. ’074 Patent, Claim 1 – “an enable/disable function to enable/disable the biasing circuit for reducing standby current”

55. I understand that Microchip and Aptiv proposed different constructions for the term “an enable/disable function to enable/disable the biasing circuit for reducing standby current,” a term that appears in claim 1 of the ’074 patent. It is my understanding that the proposed constructions are:

No.	Claim Term	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
3	“an enable/disable function to enable/disable the biasing circuit for reducing standby current” ’074 patent, claim 1	Not subject to 35 U.S.C. § 112 ¶ 6. To the extent the court determines that § 112 ¶ 6 applies: Function: to enable/disable the biasing circuit for reducing standby current Structure: enable/disable signal input line (Node M)	Indefinite; Subject to 35 U.S.C. § 112 ¶ 6 without any corresponding structure

56. Claim 1 provides (with the claim term in bold):

1. A voltage regulator, comprising:

an operational amplifier;

a gm enhanced current buffer driver;

a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver;

an enable/disable function to enable/disable the biasing circuit for reducing standby current:

an output power driver, wherein the current buffer driver is coupled between the operational amplifier and the output power driver;

a current feedback circuit coupled between the output power driver and the current buffer driver; and

a feedback loop coupled between the output power driver and the operational amplifier.

57. In Claim 1 of the '074 patent, the phrase “enable/disable function to enable/disable the biasing circuit for reducing standby current” would not be understood by a POSITA as a name for a class of structures that performs the claimed function.

58. As an initial matter, the claim language requires both “enabl[ing]” and “disable[ing]” the biasing circuit to reduce standby current. A POSITA would understand that only disabling the biasing circuit would reduce standby current; enabling a biasing circuit would not accomplish this claimed function. And the patent only discloses structures related to disabling the biasing circuit for the purpose of reducing standby current. '074 patent at 4:42-54.

59. Even setting aside this fundamental confusion in the claim language, a POSITA would not understand this term to be a name for a class of structures that performs the function of disabling a biasing circuit for reducing standby current.

60. In forming my opinion, I also reviewed the declaration of Microchip’s expert, Dr. Taylor. The examples of alleged structures from the art cited by Dr. Taylor are illustrative in that they do not support Microchip’s theory that the claim term is a name for a class of structures that can perform this function. Exhibits 1-4 to the Taylor Declaration are technical documentation for various voltage regulators. These exhibits use the terms “enable,” “enable pin,” “enable input,” “EN,” or “EN pin” to refer to a physical pin and/or wire through which a signal may be sent to some logic circuit on the regulator that acts to turn circuitry on or off based on the voltage of the signal. Taylor Ex. 1 at 1, 3-4, 24; Ex. 2 at 2, 8, 11, 13; Ex. 3 at 2, 3, 9; Ex. 4 at 1, 2, 8. Exhibit 1 uses the terms “smart enable,” “smart enable circuit,” and “smart enable input circuit” to refer to circuitry that implements logic to turn on or off some other circuitry on the regulator, based on receipt of an input signal. Taylor Decl. Ex. 1 at 1, 24. Exhibit 3 uses the terms “enable logic control function,” “enable function” and the label “Enable” on Figure 1 to refer to the same type of circuit logic. Taylor Decl. Ex. 3 at 1, 2, 9. And Taylor Exhibit 5, which is a digital logic textbook, uses the letter “e” and the phrases “enable signal” and “enable signal e” to refer to various voltage signals, not to refer to any structure. Taylor Ex. 5 at 72-74.

61. Additionally, while it is correct that there are a variety of structure classes that could accomplish the function of disabling a circuit to reduce power, there are multiple ways to accomplish this function, and the techniques of enabling and disabling circuits are not interchangeable, as Microchip’s expert Dr. Taylor states. For example, the function of reducing standby current can be performed using a logic gate or latch (combined with a “pull down” or “pull up” resistor at the output) as shown in the figure below with possible circuit elements.

62. A common “disable” or “enable” configuration (but not both) is a D-Type latch (bottom of figure), which preserves the applied state until it is reset, either through the change in

state at another input port or by interrupting the latch supply voltage. The control input in this case can create only a “disable” state, or only an “enable” state. Such a structure might be used, for example, in disabling circuitry in an error state where returning the circuitry to an enable condition might lead to damage.

63. In the voltage regulator described in the ‘074, the state of one of the gate’s outputs in the figure would be used to determine the setting of any number of possible current control components, e.g., relays, an analog current control loop, or a set of transistors like that shown in Fig. 3 of the ‘074. For the latch structure shown in the figure above, the “enable” name clearly does not imply a “disable” capability (or vice-versa), as suggested by Dr. Taylor [Par. 58] and allegedly supported by his examples. Once the “enable” (or “disable”) state is set on the latch, returning the node voltage to any earlier state will not disable (or “enable”) circuitry at the output of the latch.

64. Microchip’s proposal that “enable/disable signal input line (Node M)” is somehow the structure disclosed in the specification of the ‘074 patent that is associated with and adequate to perform the function of enabling and disabling the bias current to reduce standby current has, in my opinion, no technical basis. First, as explained above, the patent discloses only some structure that is related to disabling the bias circuit to reduce standby current. It does not refer to enabling the bias circuit to reduce standby current. Second, a “node” is well-understood by a POSITA to be a region of constant voltage or, equivalently, a section of uninterrupted, highly conductive wire. In circuit design, the term “node” thus refers to a connection from one portion of a circuit to another or refers to a region of constant voltage on such a connective wire. As explained above, there are a variety of electrical structures that might be used to enable or disable a circuit or set of circuits, but none of those structures are described by a simple node.

65. When the '074 patent discusses the process of disabling a section of circuitry to reduce standby current, it refers to structure that includes multiple transistors—numbered “320, 330, 334 and 336”—that “may be shut off during disabling/power down operation to make sure this circuit will consume substantially no DC current.” The '074 patent thus requires at least the listed transistors to perform the function of disabling the bias circuit. Additionally, there must be some structure—that is not disclosed by the '074 patent—for creating and switching on/off the “enable signal” the patent calls “Node M” and that it describes as “coming to the regulator circuit so that the module can be turned off when disabled.” '074 patent at 4:44-45.

C. '074 Patent, Claim 4 – “wherein the gm-boost circuit enables the current buffer driver to have a large gm value”

66. I understand that Microchip and Aptiv proposed different constructions for the term “wherein the gm-boost circuit enables the current buffer driver to have a large gm value,” a term that appears in claim 4 of the '074 patent. It is my understanding that the proposed constructions are:

No.	Claim Term	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
4	“wherein the gm-boost circuit enables the current buffer driver to have a large gm value” '074 patent, claim 4	Not Indefinite. Plain and Ordinary Meaning. Alternatively, “wherein the gm-boost circuit increases the gm value of the current buffer driver”	Indefinite

67. Claim 4 provides (with the claim term in bold):

1. A voltage regulator, comprising:
 - an operational amplifier;
 - a gm enhanced current buffer driver;

a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver;

an enable/disable function to enable/disable the biasing circuit for reducing standby current;

an output power driver, wherein the current buffer driver is coupled between the operational amplifier and the output power driver;

a current feedback circuit coupled between the output power driver and the current buffer driver; and

a feedback loop coupled between the output power driver and the operational amplifier.

2. The voltage regulator according to claim 1, further comprising a gm-boost circuit coupled to the current buffer driver.

4. The voltage regulator according to claim 2, **wherein the gm-boost circuit enables the current buffer driver to have a large gm value.**

68. In my opinion, a POSITA reading the '074 patent would not be able to determine with reasonable certainty whether a given current buffer driver has a sufficiently large gm value to fall within the scope of the claims. Specifically, the term “large gm value” is not defined in the intrinsic record, nor is it a term of art in the field of voltage regulator design. Thus, it would not be clear to a POSITA how to distinguish between a “large gm value” and some other amount of transconductance.

69. In forming my opinion, I also reviewed the declaration of Microchip’s expert, Dr. Taylor. Dr. Taylor opines that “a POSITA would have understood why the circuitry of the ‘074 patent includes a gm-boost circuit”, explaining that “the current buffer driver 204 pushes this pole [which would otherwise result in instability] to a high frequency beyond unity-gain frequency....”. Thus, he concludes that “the word ‘large’ in the ‘large gm value’ claim term

simply refers to boosting g_m to a value at-or-beyond which the ‘second-most-dominant pole’ will be pushed close to or beyond the unity-gain frequency...”.

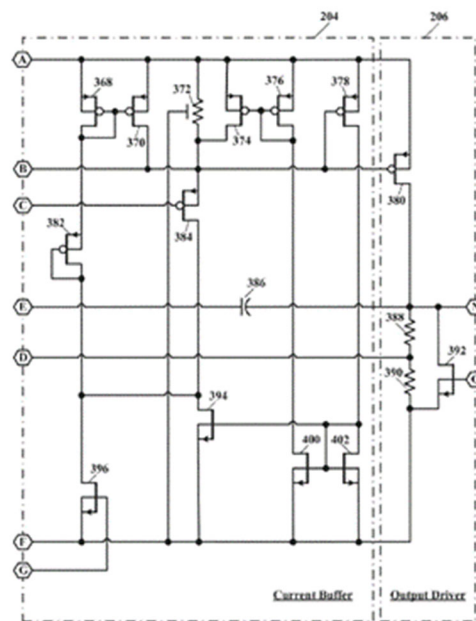


FIGURE 3B

70. Dr. Taylor omits two crucial points well understood by a POSITA which makes his definition untenable: First, the position (i.e., frequency) of the pole creating instability strongly depends on the electrical characteristics (e.g., ESR for a capacitive load) of the range of loads that could be present at the regulator output. And because the load can change during operation (e.g., a resistive heating element), so too does the operational frequency of the regulator which in turn affects the amount of transconductance required to achieve adequate pole-splitting. Second, the position of the second pole creating instability depends strongly on the specific electrical characteristics (e.g., the gate capacitance) of the transistors in output driver 206, as shown in Fig. 3B above. Thus, even under Dr. Taylor’s definition, a POSITA could not determine what constitutes a “large g_m value” without guidance from the ‘074 specification on designing for the

range of load characteristics and teachings on the allowed electrical characteristics of the output driver transistors.

D. '074 Patent, Claims 8, 9 – “low gain and high bandwidth amplifier”

71. I understand that Microchip and Aptiv proposed different constructions for the term “low gain and high bandwidth amplifier,” a term that appears in claims 8 and 9 of the '074 patent. It is my understanding that the proposed constructions are:

No.	Claim Term	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
5	“low gain and high bandwidth amplifier” '074 patent, claims 8, 9	Not Indefinite. Plain and Ordinary Meaning. Alternatively, “amplifier optimized for high bandwidth with a commensurate reduction of gain”	Indefinite

72. Claims 8 and 9 provide (with claim terms in bold):

1. A voltage regulator, comprising:

an operational amplifier;

a gm enhanced current buffer driver;

a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver;

an enable/disable function to enable/disable the biasing circuit for reducing standby current:

an output power driver, wherein the current buffer driver is coupled between the operational amplifier and the output power driver;

a current feedback circuit coupled between the output power driver and the current buffer driver; and

a feedback loop coupled between the output power driver and the operational amplifier.

8. The voltage regulator according to claim 1, wherein the operational amplifier is a **low gain and high bandwidth amplifier**.

9. The voltage regulator according to claim 8, wherein the **low gain and high bandwidth amplifier** is a folded-cascode amplifier.

73. In my opinion, a POSITA would not be able to determine with reasonable certainty whether a given amplifier is sufficiently low gain and sufficiently high bandwidth to fall within the scope of the claims.

74. The term “gain” in electrical engineering refers to a voltage or power increase between the input and output of an electrical component. In the context of a voltage amplifier like the one described in the first gain stage of the '074 patent, it refers more specifically to the increase in voltage across the amplifier.

75. Having reviewed the patent specification and intrinsic record, I do not understand how a POSITA would reasonably determine at what point an amplifier is sufficiently “low gain” to satisfy the claim limitation. The specification itself provides no metric by which to make this determination and no further explanation was provided in the prosecution history.

76. In forming my opinion, I also reviewed the declaration of Microchip’s expert, Dr. Taylor. As an initial matter, I disagree with Dr. Taylor’s assertion that the relationship between gain and bandwidth is sufficient to provide a POSITA with certainty regarding when a given amplifier is “low gain and high bandwidth.” Dr. Taylor’s position that any amplifier at “the other end” of the gain/bandwidth scale satisfies the claim limitation fails to provide a POSITA with any usable guidelines because it simply swaps one undefined term (“low” or “high”) for another undefined term (“the other end”).

77. As Dr. Taylor notes, “...a POSITA would have been aware of the sliding scale tradeoff between gain and bandwidth in an amplifier...” and “[s]ince the mathematical product of gain bandwidth is approximately constant...” [par. 71]. What Dr. Taylor does not explain is that the mathematical Gain-Bandwidth Product (“GBP”) itself must be chosen by the POSITA in

selecting an Op Amp for the '074 circuit design. A low cost, general purpose Op Amp might have a GBP of about 10^6 or 1 million (e.g., the Fairchild-designed 741 Op Amp) while much more expensive Op Amps have GBP of above 10^9 or 1 billion (e.g., Texas Instruments OPA856).

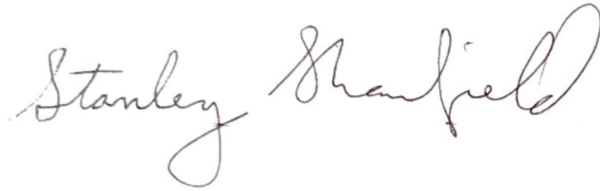
78. If a POSITA chooses the 741 Op Amp with a GBP of about 10^6 , this means that the amplifier will provide a bandwidth of 1 MHz with unity gain (i.e., a “low” gain). If the Texas Instruments OPA856 Op Amp is instead chosen, that amplifier will provide a bandwidth of 1 GHz at unity gain. Both choices are set up (using feedback elements) with “low gain” but wildly different bandwidths. The '074 patent does not make it clear whether 1 MHz is wide enough bandwidth, or if 10 MHz, or 100 MHz, or 1 GHz (1000 MHz) bandwidth is needed with the chosen “low gain”.

79. Given the choice of Op Amp products delivering orders-of-magnitude different GBP, Dr. Taylor’s prescription that “low gain and high bandwidth amplifier simply refers to an amplifier positioned at the other end of the gain-bandwidth scale from a traditional Op Amp” does not allow a POSITA to understand the meaning of “low gain and high bandwidth”. In fact, to decide on how to position the amplifier “at the other end of the gain-bandwidth scale from a traditional Op Amp”, a POSITA would need clearly explained guidance on what range of values of GBP are appropriate for the '074 patent design.

80. Dr. Taylor’s assertion that a low gain and high bandwidth amplifier is one with sufficient bandwidth to form a single pole while still providing “good driving capability” for the current buffer does not provide this guidance. The requirement of “good driving capability” sets a *floor* for the gain and does not inform a POSITA of the relevant *ceiling*—the point beneath which an amplifier is considered “low gain.” If the GBP of a chosen Op Amp product is too

low, the amplifier cannot be configured to provide “good driving capability” for the current buffer.

I declare under penalty of perjury that the foregoing is true and correct. Executed this 22nd day of March 2024 in Cambridge, Massachusetts.

A handwritten signature in cursive script, reading "Stanley Shanfield". The signature is written in dark ink and is positioned above a horizontal line.

Stanley Shanfield

Exhibit A

Stanley Shanfield



Curriculum Vitae for Stanley Shanfield

Education:

Massachusetts Institute of Technology, Ph.D., Physics, 1981

University of California, Irvine, B.S. Cum Laude, Physics, 1977

Educational Awards:

Outstanding Research Project, U.C. Regents Award, 1977

Phi Beta Kappa, 1977

Four Year Scholarship, Tuition & Research, ERDA/DOE, 1977-1981

Hands-On Professional Expertise:

Semiconductor Physics & Chemistry

Semiconductor Fabrication: Silicon and III-V Materials

Semiconductor Device & Integrated Circuit Engineering

Semiconductor Equipment: Front & Back End

Semiconductor Packaging Design and Manufacturing

Passive Component Design and Manufacturing

RF Design and Fabrication

Digital Design & Fabrication

Semiconductor Manufacturing in Silicon and III-V Materials

MEMS Design and Fabrication: Electrical, Optical, & Sensing Devices

Fiber Optic Device Design and Fabrication

Integrated Optics & Electro-Optical Devices

Plasma Physics

Specialized Training:

Global Positioning Electronics, Systems and Components

Six Sigma Semiconductor Manufacturing

Microwave Engineering

US Patent Law in Technology

Patent Application and Prosecution

Semiconductor Plasma Processing

Thin Film Physics and Technology

MEMS-based Gyroscopes and Accelerometers

Thermoelectric Materials & Technology

Phased Array Radar Engineering

Antennas and Electromagnetic Propagation

Solid State Optical Devices

Fiber Optic Communication System Operation

HALT and HAST Reliability Testing Methods

Professional Experience:

Draper Laboratory Cambridge, MA

2003 – present

Division Leader, Advanced Hardware Development Distinguished Member of Technical Staff Technical Director

Led division (about 80 staff) in re-invigorating multi-chip integrated circuit module facility, more than doubling associated revenues in two years. By most accounts, made division a viable business & technological entity again. Invented & led implementation of an ultra-miniature electronics fabrication technology which became a top laboratory priority. Led team in realization & fabrication of a newly designed precision MEMS-based gyroscope and associated ASIC. Found funding and led team in developing a miniature power source with energy density at least two orders of magnitude higher than any source previously built. Developed fabrication technology for semiconductor-based low phase noise oscillator design, allowing for receiver operation with extremely low signal strength. Many awards received, most recently, the Draper 2010 Distinguished Performance Award, and 2010 Best Patent Award. Recent work in ASIC process design and circuit design for ultra-high performance government and space systems.

Clarendon Photonics Newton, MA

2001 – 2003

Director, Packaging & Integration

30 person photonic chip startup with \$18 million 2nd round funding. Invented and productized new, low cost and reliable semiconductor processing, packaging and pig-tailing technology for optical add-drop multiplexer. Established assembly and packaging process and developed control electronics. Partner with Micron Technologies, using their R&D semiconductor facility.

AXSUN Technologies Bedford/Billerica, MA

1999 – 2001

Vice President, Operations, Co-Founder 1999 – 2000

Initially three staff members with \$6 million funding. Designed, fabricated and productized AXSUN's micro-electromechanical (MEM) Fabry-Perot optical filter. Patents granted on semiconductor processing and control electronics. Completed facility and semiconductor processing design, then completely equipped. Raised 2nd round funding for \$36 million. Established process and fabrication facility in Belfast, Northern Ireland for producing thick oxide silicon-on-insulator material.

Director, Manufacturing & Wafer Fab Technology

2000 – 2001

After 3rd round funding, led device manufacturing, creating wafer fab and assembly infrastructure; hired 70+ people, led production. Delivered first generation product for revenue to multiple customers. Converted pure technology to dominant company revenue with high yield.

Company purchased by Volcano Technologies, San Diego.

Raytheon Corporation Lexington/Andover, MA

1985 - 1999

Manager, Semiconductor Operations

1996 – 1999

Built and led a 300 employee, \$60 million revenue 24/7 semiconductor development and manufacturing operation resulting from the consolidation of a number of smaller organizations. Key player in technological development and recipient of Raytheon's 6 Sigma Leadership training. Decision maker in Texas Instrument group acquisition, providing significant expert opinion on semiconductor and design facilities. Obtained state-of-art yields using best available steppers, deep reactive ion etching, plasma assisted CVD, and ion-implantation equipment, and disciplined design-for steppers, deep reactive ion etching, plasma assisted CVD, and ion-implantation equipment, and disciplined design-for-manufacturing circuit design and layout methodology.

Research Laboratory Manager

1992 – 1996

Leader of a 90 employee development and contract research organization in high performance semiconductor devices and circuits, measurement, assembly and wafer fab. Led a team which invented and implemented a major revenue generating technology (\$.100 million) based on semiconductor device development (pseudomorphic high electron mobility transistor). Increased outside research funding by 50% in 3 years through superior technical performance relative to competitors.

Section Manager, Semiconductors & ICs

1985 – 1992

Led a MM-Wave Circuit and Module Development program over 2 years, leading to production win of a satellite terminal electronics generating \$320 million in sales. Developed processes for fabricating high power, high frequency multi-function integrated circuits, and combining high performance digital and analog devices in a single integrated circuit.

Spire Corporation Bedford, MA

1981 – 1984

**Staff Scientist
Senior Staff Scientist**

Developed new methods for low temperature deposition of plasma-assisted CVD epitaxial silicon. Wrote joint papers with MIT professor, and had process adopted by equipment manufacturers. Built, operated and characterized ion-assisted deposition system for making coating for semiconductor and machine tool industries. Process eventually purchased by Kennametal, Inc.

Publications

Restricted Publications & Reports

Process Sequence for Formation of Ultra-High Density Multi-Chip Modules:

A high yield, low cost method for creating a system-in-a-package consisting of numerous semiconductor die, passive components, and sensors. Process formed basis for new (2008) facility.

Design and Method of Fabrication of Ultra-High Density Radioisotope Power Source:

In test, a miniature power source that achieves energy density more than 1000X the best chemical battery. Method uses planar semiconductor processing of bulk thermoelectric materials.

Design and Method of Achieving Extremely Low Crystal Oscillator Phase Noise:

Method developed for very low power refrigeration of quartz or sapphire crystal resonators, resulting in extremely low phase noise oscillators. The low phase noise allows extremely high sensitivity in digital receivers, including GPS receivers, leading to use in extremely low signal conditions.

Design, Evaluation & Production of MEMS-based Fabry-Perot Interferometer:

Design and method for ultra-compact spectral analyzer made using semiconductor and optical thin film processing.

Design & Evaluation of Ultra-Fast Control Electronics for Integrated Optical Multiplexer:

Design and performance evaluation of silicon-based integrated optical multiplexer using chip-based local heating

Design and Fabrication of Q-band MILSTAR Communications Terminal Transmitter:

Record power and efficiency 44 GHz transmitter design using new transistor design, and combined waveguide

Key Publications (selected)

Process Characterization of PSG and BPSG Plasma Deposition, J. Electrochem. Soc., Volume 131, Issue 9, pp. 2202-2203

A double-recessed Al_{0.24}GaAs/In_{0.16}GaAs pseudomorphic HEMT for Ka- and Q-band power Applications, Electron Device Letters, IEEE, Volume 14, Issue 9, pp. 456 - 458

Formation of Thick Metal Structures on GaAs MMICs Using Image Reversal Lithography and Evaporated Metal Deposition, J. Electrochem. Soc., Volume 136, Issue 9, pp. 2687-2690

Contact Hole Etching in Load-Locked Hexagonal Reactive Ion Etch System, J. Electrochem. Soc., Vol. 131, No. 8, 1984

An AlGaAs/InGaAs pseudomorphic high electron mobility transistor with Improved Breakdown Voltage for X and Ku-band power applications, Microwave Theory and Techniques, IEEE Transactions on, Volume 41, Issue 5, May 1993, pp. 752 - 759

Hot-electron-induced Degradation of Metal-Semiconductor Field-Effect Transistors, Integrated Circuit Symposium, 1994. Technical Digest 1994., 16th Annual Volume , Issue , 16-19 Oct. 1994, pp. 259

Ion Beam Deposition of Cubic Boron Nitride, J. Vac. Sci. Technol. A Volume 1, Issue 2, pp. 323-325

Patents**US Patent 6504235 - Passivation layer and process for semiconductor devices**

Method of coating semiconductor devices that prevented parametric shift in electrical performance. Solved key processing problem.

US Patent 4440108 - Ion Beam Deposition Apparatus

Design of equipment for deposition of thin films in the presence of ion bombardment. System produced thin films of interest for mechanical, electrical and optical properties and was sold as an equipment product.

US Patent 6525880 - Integrated Tunable Fabry-Perot filter and Method of Making Same

Design and method for fabricating very small, very high performance variable optical filter using semiconductor fabrication technology. In current use in fiber optical networks, chemical sensors, and 3-D medical imaging applications.

US Patent 5175020 - Boron Nitride Films and Process of Making Same

Ion assisted deposition of ultra-hard cubic boron nitride films for semiconductor and machine tool applications. Significant use in both areas.

US Patent 4526673 - Coating Method

Method for deposition of thin films used in semiconductor device fabrication. Method based on direct control of the kinetics of thin film deposition.

US Patent 7727806 - Systems and Methods for High Density Multi-Component Modules

Method for fabrication of electronic modules using multiple thinned integrated circuits, patterned multi-level interconnects, passive electronic components, and sensors

US Patent Application 2009/TBD - Devices, systems, and methods for controlling the temperature of resonant elements

Devices and systems for achieving low phase noise crystal oscillators using unique low power thermoelectric structures

Expert Witness Experience:

See attachment

Expert Witness Testifying Experience (2017 to Present)

1. Samsung Electronics Co., Ltd. v. Daedalus Prime LLC, IPR2023-00868 (PTAB)
2. Samsung Electronics Co., Ltd. v. Daedalus Prime LLC, IPR2023-00841 (PTAB)
3. Samsung Electronics Co., Ltd. v. Daedalus Prime LLC, IPR2023-00562 (PTAB)
4. Samsung Electronics Co., Ltd. v. Daedalus Prime LLC, IPR2023-00563 (PTAB)
5. PDF Solutions, Inc. v. Ocean Semiconductor LLC, IPR2022-00671 (PTAB)
6. STMicroelectronics, Inc. v. Ocean Semiconductor LLC, IPR2022-00681 (PTAB)
7. STMicroelectronics, Inc. v. Ocean Semiconductor LLC, IPR2022-00680 (PTAB)
8. Trustees of Purdue Univ. v. Wolfspeed, Inc., 1:21-cv-00840-WO-LPA (NC MDC)
9. Qorvo, Inc. v. Akoustis Tech., Inc., 1:21-cv-01417-JPM (DE DC)
10. Applied Materials, Inc. v. Ocean Semiconductor LLC, IPR2021-01339 (PTAB)
11. Applied Materials, Inc. v. Ocean Semiconductor LLC, IPR2021-01342 (PTAB)
12. Applied Materials, Inc. v. Ocean Semiconductor LLC, IPR2021-01344 (PTAB)
13. Xilinx, Inc. v. FG SRC LLC, IPR2021-00633 (PTAB)
14. Kinik Company v. Chien-Min Sung, IPR2021-00638 (PTAB)
15. Taiwan Semiconductor Manufacturing Company Ltd. v. Arbor Global Strategies LLC, IPR2021-00391 (PTAB)
16. Taiwan Semiconductor Manufacturing Company Ltd. v. Arbor Global Strategies LLC, IPR2021-00393 (PTAB)
17. Taiwan Semiconductor Manufacturing Company Ltd. v. Arbor Global Strategies LLC, IPR2021-00394 (PTAB)
18. Microchip Technology Incorporated et al v. Bell Semiconductor, LLC, IPR2021-00191 (PTAB)
19. Microchip Technology Incorporated et al v. Bell Semiconductor, LLC, IPR2021-00168 (PTAB)
20. Comet Tech. v. XP Power, 5:20-cv-6408-NC (CA NDC)
21. Xilinx, Inc. v. Arbor Global Strategies LLC, IPR2020-01568 (PTAB)
22. Intel Corporation v. FG SRC LLC, IPR2020-01449 (PTAB)

Expert Witness Testifying Experience (2017 to Present)

23. Samsung Electronics Co., Ltd. v. Arbor Global Strategies LLC, IPR2020-01020 (PTAB)
24. Samsung Electronics Co., Ltd. v. Arbor Global Strategies LLC, IPR2020-01021 (PTAB)
25. Samsung Electronics Co., Ltd. v. Arbor Global Strategies LLC, IPR2020-01022 (PTAB)
26. Intel Corporation v. Tela Innovations, Inc., IPR2019-01636 (PTAB)
27. Intel Corporation v. Tela Innovations, Inc., IPR2019-01637 (PTAB)
28. Intel Corporation v. Tela Innovations, Inc., IPR2019-01513 (PTAB)
29. Intel Corporation v. Tela Innovations, Inc., IPR2019-01515 (PTAB)
30. Intel Corporation v. Tela Innovations, Inc., IPR2019-01518 (PTAB)
31. Intel Corporation v. Tela Innovations, Inc., IPR2019-01520 (PTAB)
32. Intel Corporation v. Tela Innovations, Inc., IPR2019-01521 (PTAB)
33. Intel Corporation v. Tela Innovations, Inc., IPR2019-01522 (PTAB)
34. Intel Corporation v. Tela Innovations, Inc., IPR2019-01257 (PTAB)
35. Intel Corporation v. Tela Innovations, Inc., IPR2019-01262 (PTAB)
36. Intel Corporation v. Tela Innovations, Inc., IPR2019-01255 (PTAB)
37. Intel Corporation v. Tela Innovations, Inc., IPR2019-01254 (PTAB)
38. Intel Corporation v. Tela Innovations, Inc., IPR2019-01256 (PTAB)
39. Intel Corporation v. Tela Innovations, Inc., IPR2019-01220 (PTAB)
40. Intel Corporation v. Tela Innovations, Inc., IPR2019-01221 (PTAB)
41. Intel Corporation v. Tela Innovations, Inc., IPR2019-01228 (PTAB)
42. PACT XPP Schweiz AG v. Intel Corp., 1:19-cv-01006-JDW (DE DC)
43. Greenthread LLC v. Samsung Elec. Co., Ltd, 2:19-cv-147-JRG (TX EDC)
44. Samsung Electronics Co., Ltd. et al v. ProMOS Technologies, Inc., IPR2019-00782 (PTAB)
45. Samsung Electronics Co., Ltd. et al v. ProMOS Technologies, Inc., IPR2019-00783 (PTAB)

Expert Witness Testifying Experience (2017 to Present)

46. Samsung Electronics Co., Ltd. et al v. DigitalOptics Corporation MEMS et al, IPR2018-01806 (PTAB)
47. Intel Corporation v. Godo Kaisha IP Bridge 1, IPR2018-01486 (PTAB)
48. Intel Corporation v. Godo Kaisha IP Bridge 1, IPR2018-01487 (PTAB)
49. VIZIO, Inc. v. Nichia Corporation, IPR2018-00893 (PTAB)
50. Lowe's Companies, Inc. et al v. Nichia Corporation, IPR2018-00699 (PTAB)
51. SPTS Technologies Limited et al v. Plasma-Therm LLC, IPR2018-00618 (PTAB)
52. Lowe's Companies, Inc. et al v. Nichia Corporation, IPR2018-00601 (PTAB)
53. VIZIO, Inc. v. Nichia Corporation, IPR2018-00437 (PTAB)
54. VIZIO, Inc. v. Nichia Corporation, IPR2018-00386 (PTAB)
55. Godo Kaisha IP Bridge 1 v. Intel Corp., 2:17-cv-00676-RWS-RSP (TX EDC)
56. SPTS Technologies Limited et al v. Plasma-Therm LLC, IPR2017-02164 (PTAB)
57. Lowe's Companies, Inc. et al v. Nichia Corporation, IPR2017-02011 (PTAB)
58. Lowe's Companies, Inc. et al v. Nichia Corporation, IPR2017-02014 (PTAB)
59. Taiwan Semiconductor Manufacturing Co., Ltd. v. Godo Kaisha IP Bridge 1 et al, IPR2017-01841 (PTAB)
60. Taiwan Semiconductor Manufacturing Company Limited v. Godo Kaisha IP Bridge 1, IPR2017-01842 (PTAB)
61. Taiwan Semiconductor Manufacturing Co., Ltd. v. Godo Kaisha IP Bridge 1 et al, IPR2017-01843 (PTAB)
62. Taiwan Semiconductor Manufacturing Company Limited v. Godo Kaisha IP Bridge 1, IPR2017-01844 (PTAB)
63. Orbotech Ltd. et al v. Plasma-Therm LLC, IPR2017-01792 (PTAB)
64. SPTS Technologies Limited et al v. Plasma-Therm LLC, IPR2017-01674 (PTAB)
65. VIZIO, Inc. v. Nichia Corporation, IPR2017-01608 (PTAB)
66. VIZIO, Inc. v. Nichia Corporation, IPR2017-01623 (PTAB)
67. SPTS Technologies Limited v. Plasma-Therm LLC, IPR2017-01457 (PTAB)

Expert Witness Testifying Experience (2017 to Present)

68. Samsung Electronics Co., Ltd. et al v. ProMOS Technologies, Inc., IPR2017-01419 (PTAB)
69. SPTS Technologies Ltd. v. Plasma-Therm LLC, IPR2017-01314 (PTAB)
70. Samsung Electronics Co., Ltd. et al. v. Lexington Luminance LLC, IPR2017-00539 (PTAB)
71. Samsung Electronics Co., Ltd. et al. v. Lexington Luminance LLC, IPR2017-00540 (PTAB)
72. Broadcom Corp. v. PROGRESSIVE SEMICONDUCTOR SOLUTIONS LLC, IPR2017-00090 (PTAB)
73. Samsung Electronics Co., Ltd. et al. v. Flamm, Daniel, IPR2016-01510 (PTAB)
74. Samsung Electronics Co., Ltd. et al. v. Flamm, Daniel, IPR2016-01512 (PTAB)
75. American Technical Ceramics Corp. v. Presidio Components, Inc., 2:14-cv-06544-KAM-GXB (NY EDC)
76. Home Semiconductor Corp. v. Samsung Elecs. Co., Ltd., 1:13-cv-2033-RGA (DE DC)
77. In re Certain Filament Light-Emitting Diodes and Products Containing Same, ITC 337-TA-1220 (ITC)

CERTIFICATE OF SERVICE

I, Andrew T. Jones, hereby certify that on March 22, 2024, I served copies of the foregoing document by electronic transmission to the email addresses listed below:

BY EMAIL

Jack B. Blumenfeld
Brian P. Egan
Travis J. Murray
Morris, Nichols, Arsht & Tunnell LLP
1201 North Market Street
P.O. Box 1347
Wilmington, DE 19899
(302) 658-9200
jblumenfeld@mnat.com
began@mnat.com
tmurray@morrisnichols.com

John M. Neukom
Barbara N. Barath
Yuqing Cui
Alexander H. Lee
DEBEVOISE & PLIMPTON LLP
650 California Street, Floor 31
San Francisco, CA 94108
Telephone: (415) 738-5700
jneukom@debevoise.com
bnbarath@debevoise.com
ycui@debevoise.com
ahlee@debevoise.com
ajkuang@debevoise.com
Microchip-All@debevoise.com

Andrew Gish
Edward Tulin
GISH PLLC
41 Madison Avenue, Floor 31
New York, NY 10010
Telephone: (212) 518-2000
andrew@gishpllc.com
edward@gishpllc.com

Ryan K. Iwahashi
GISH PLLC
50 California Street, Suite 1500
San Francisco, CA 94111
(415) 630-8960
ryan@gishpllc.com

Attorneys for Plaintiff
MICROCHIP TECHNOLOGY INC.

/s/ Andrew T. Jones

Andrew T. Jones