

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

MICROCHIP TECHNOLOGY INC.,

Plaintiff,

v.

APTIV SERVICES US, LLC,

Defendant.

C.A. No. 1:23-CV-00778-JDW

JURY TRIAL DEMANDED

**PLAINTIFF MICROCHIP TECHNOLOGY INC.'S
OPENING CLAIM CONSTRUCTION BRIEF**

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I. INTRODUCTION

The Parties take fundamentally different approaches to determining the meaning of the four disputed terms of U.S. Patent Nos. 7,564,665 (“’665 patent”) and 9,471,074 (“’074 patent”). Plaintiff Microchip Technology Inc. (“Microchip”) proposes constructions consistent with the plain language of the claims, the intrinsic record, legal precedent, and the knowledge of a person of ordinary skill in the art (“POSITA”). In contrast, Defendant Aptiv Services US, LLC (“Aptiv”) seeks to (1) artificially limit the claims of the ’665 patent in contravention of the express teachings of its specification; and (2) incorrectly portray one term of art and two terms of degree in the ’074 patent as indefinite by ignoring the guidance of the specification and the common knowledge of a POSITA.

Term 1, “second voltage rail,” is recited in claims 1 and 2 of the ’665 patent. Aptiv seeks to restrict this term such that the “second voltage rail” cannot be the same structure as the “first voltage rail,” in contravention of the specification’s express teaching that these two rails “may in fact be the same power/supply rail.”

Term 3,¹ “an enable/disable function to enable/disable the biasing circuit for reducing standby current,” is recited in claim 1 of the ’074 patent. Aptiv argues that the “enable/disable function” is a means-plus-function term without corresponding structure and is therefore indefinite. Not so. First, a POSITA would understand that, an “enable/disable function” simply refers to an input line for turning on and off a switch. Accordingly, this is not a means-plus-function term. Second, even if this were a means-plus-function term, the specification expressly discloses corresponding structure that undercuts Aptiv’s indefiniteness position.

¹ The parties have agreed to Aptiv’s construction of term 2 (“to charge the [respective] pad capacitance”) as stated in the Joint Clam Construction Chart (D.I. 65), so it is no longer disputed.

Term 4, “wherein the gm-boost circuit enables the current buffer driver to have a large gm value,” is recited in claim 4 of the ’074 patent. Aptiv contends that the term of degree, “large gm value,” is indefinite. But the specification’s guidance that the gm value must be sufficiently large to produce a “pole-splitting” effect stabilizing the output of the voltage regulator provides a POSITA with reasonable certainty regarding the scope of this term.

Term 5, “low gain and high bandwidth amplifier,” is recited in claims 8 and 9 of the ’074 patent. Contrary to Aptiv’s position, this is not an indefinite term of degree for two reasons. First, a POSITA would understand that this language does not refer to “low” or “high” values in the abstract. Rather, it invokes the fundamental electrical engineering principle that operational amplifiers are configured on a sliding scale between gain and bandwidth, and it directs a POSITA to configure the claimed operational amplifier on one end of that spectrum. Second, adding even more clarity, the specification again provides functional guidance that would enable a POSITA to calibrate the tradeoff between gain and bandwidth to achieve the stabilizing “pole-splitting” effect.

II. THE ASSERTED PATENTS

A. The ’665 Patent

The ’665 patent discloses and claims “circuitry for providing protection against damaging effects of Electrostatic Discharge (ESD).” (’665 patent, 1:6-9.) An electrostatic discharge occurs when a buildup of static electricity is discharged through the circuitry of a chip. (’665 patent, 1:22-28.) Typically, static charge enters the circuitry of a chip through *one* of its many conductive input/output pads. (See ’665 patent, Fig. 1, item 126.) Because this charge is concentrated in a small area, it results in a high and potentially destructive voltage. (See ’665 patent, 2:27-29, 3:50-56.) The ’665 patent solves this problem by providing circuitry that

permits “the ESD energy [to] be shared by . . . **all** the pads, thereby reducing the voltage that may develop in the system as the result of the ESD event.”² (’665 patent, 2:29-35.)

Namely, as depicted in Fig. 1 below, during an ESD event, the ’665 patent discloses enabling “PMOS devices,” *i.e.*, transistors, (110a and 110b below) to electrically connect all input/output pads to a shared voltage supply rail (VDDIO below). (’665 patent, 4:7-13.) This allows a static charge (126 below) originating at one pad (114a below) to spread to all other pads in the system (114b below) via the voltage supply rail, thereby reducing the concentration of charge in any one location and decreasing the harmful effects of ESD. (’665 patent, 4:13-21.) Although the below example depicts only two pads, the same principle applies to systems with many pads. (’665 patent, 4:13-16.)

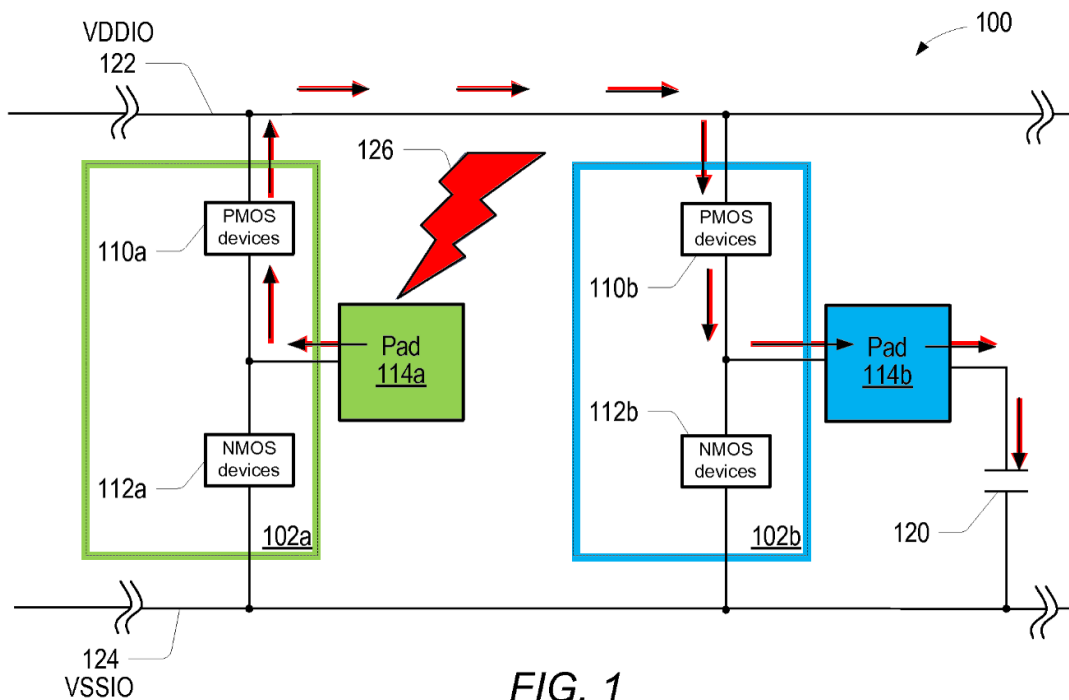


FIG. 1

(’665 Patent, FIG. 1.)

² Except where otherwise noted, all emphases herein are added, and internal quotation marks and citations are omitted.

To accomplish this charge-spreading, the '665 patent employs “pad circuitry” (102a and 102b above) attached to each pad, each instance of which is configured to recognize and react to an ESD event. (E.g., '665 patent, 3:65-67.) In one such embodiment, depicted in Fig. 2 below, the pad circuitry employs multiple voltage rails—**VDDIO** (122 below) and **VIOESD** (244 below)—that connect the pads to one another.

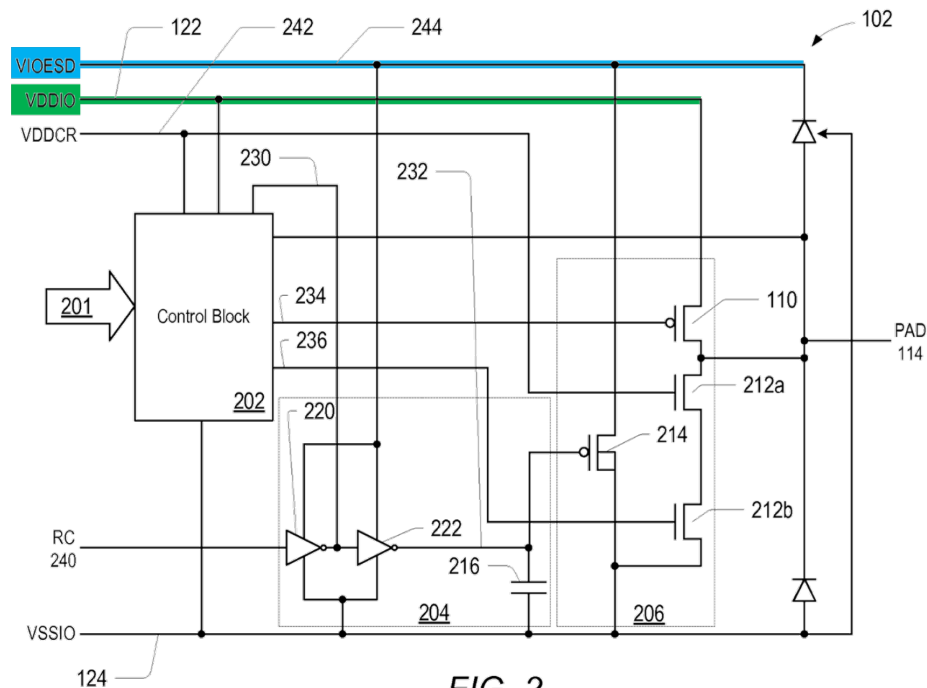


FIG. 2

But the specification makes clear that **VIOESD** and **VDDIO** may also be a single rail:

It should also be noted that **VIOESD 244 and VDDIO 122 may in fact be the same power/supply rail**, and alternate embodiments may be configured with a single power rail providing power to the circuit and/or system components that are powered by VIOESD 244 and VDDIO 122 in the embodiment shown in FIG. 2. In general, the **ESD rail and the power supply rail can be the same supply rail**, and separate supply rails (e.g. VIOESD 244 and a distinct VDDIO 122) may not be required.

('665 patent, 5:57-65.)

B. The '074 Patent

The '074 patent discloses and claims an improved voltage regulator, *i.e.*, circuitry for providing a consistent and stable voltage.

The behavior of a voltage regulator (or other circuitry) can be characterized by a mathematical “transfer function,” which describes the relationship between the circuit’s input and its output as a function of frequency. Input frequencies that result in a transfer function equaling zero are known as “zeroes,” and input frequencies that result in a transfer function equaling infinity are known as “poles.” For instance, the hypothetical transfer function

$$\frac{V_{out}}{V_{in}} = \frac{s-100}{s-5000}$$
 describes the ratio of the output voltage of a circuit (V_{out}) to the input voltage of

the circuit (V_{in}) as a function of frequency (s). It has a zero at 100 Hz, and a pole at 5000 Hz.

Roughly speaking, poles are undesirable, because they degrade the stability of a circuit. (Taylor ¶¶ 39-47, 66.)

The transfer function—and therefore performance—of a voltage regulator is dictated by the character and arrangement of components comprising the regulator. (Taylor ¶ 44.) Because voltage regulators employ an external capacitor attached to their output to provide stability, the equivalent series resistance (“ESR”) of that external capacitor affects a regulator’s transfer function. That poses a challenge, because the ESR of external capacitors can vary widely depending on the manufacturer, batch, physical orientation of the capacitor on a circuit board, the quality and length of the traces (*i.e.*, wires) that connect the external capacitor to the regulator, and other factors outside the control of a circuit designer. (*E.g.*, '074 patent, 1:25-45; Taylor ¶ 45.)

The '074 patent solves this problem with a novel architecture designed to both “reduce compensation capacitor size and provide for a wide range of external compensation capacitor

values.” (’074 patent, 1:16-20; *id.* at 1:55-59 (explaining the need to “improve the range of external capacitors with small to large ESR values . . . for stabilizing an associated voltage regulator.”).) To accomplish this, the ’074 patent prescribes at least two improvements to traditional voltage regulator circuitry.

First, the ’074 patent explains that “the key to being able to use smaller . . . external capacitances is to have a large $gm^{[3]}$ current buffer driver amplifier 204 between the first stage OpAmp 202 and the last stage power output driver 206.” (’074 patent, 3:58-62.) Provided that the current buffer has sufficient gm , this configuration “pushes [the amplifier’s] pole to a high frequency” to create a “pole-splitting effect” that stabilizes the regulator. (’074 patent, 4:11-14.)

Second, the ’074 patent prescribes using a “low gain and high bandwidth [operational] amplifier” within the regulator. There is a sliding-scale relationship between gain and bandwidth in an operational amplifier. Provided that the operational amplifier is configured with sufficiently high bandwidth and low gain, it will “form[] only one pole at the output . . . [and] provide[] a good driving capability,” which will stabilize the regulator. (’074 patent, 4:33-35.)

Separately, the ’074 patent teaches an “enable/disable function” for conserving power when the regulator is idle. Namely, ’074 patent explains that, within the chip’s “biasing” circuitry (*i.e.*, configuration circuitry), “[t]ransistors . . . may be shut off during disabling/power down operation to make sure this circuit will consume substantially no DC current.” (’074 patent, 4:44-54.) As depicted below, that is accomplished by an input line (M below), which switches on or off transistors (320, 330, 334, and 336 below) to enable or disable the flow of current in the circuitry. (Taylor ¶ 63.)

³ “ gm ” is a standard symbol used to refer to transconductance (*id.*, 3:29-30), *i.e.*, the ratio of the output current of a device to its input voltage. (Taylor ¶ 34.)

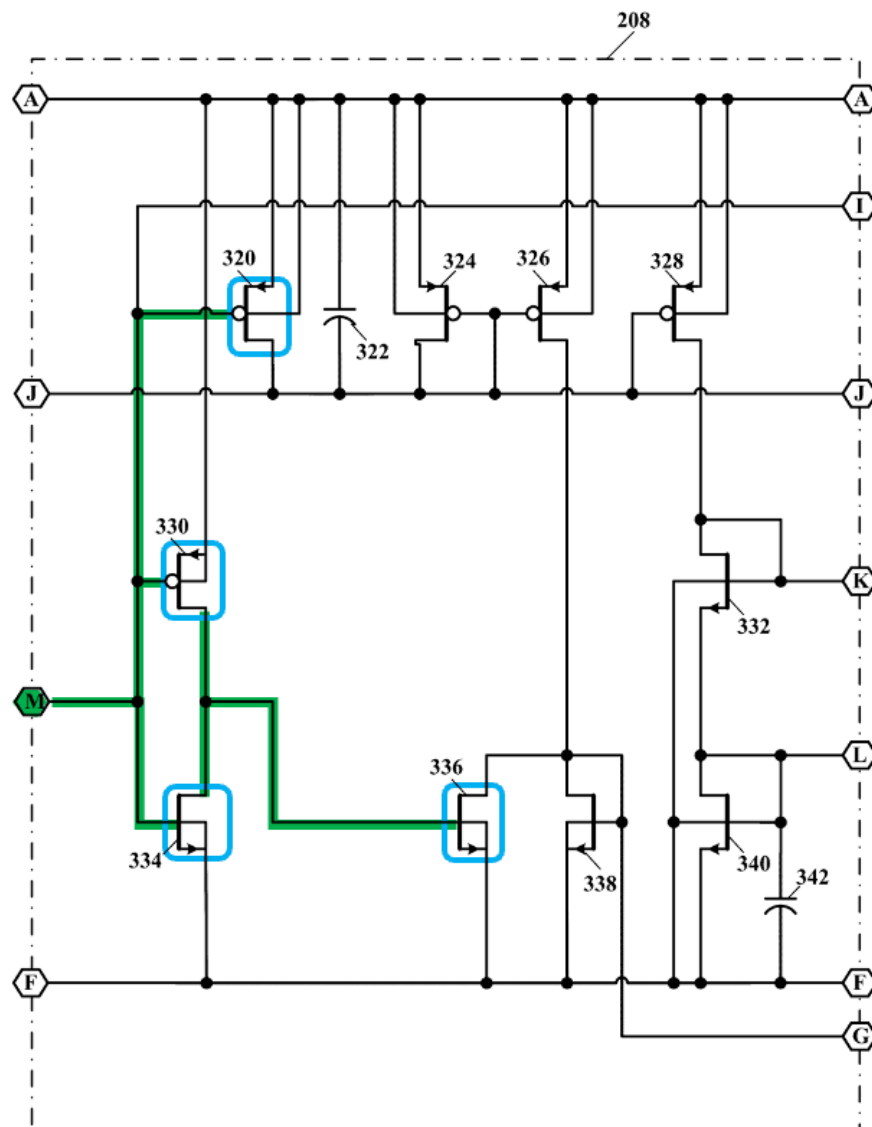


FIGURE 3

('074 patent, FIG. 3 (annotated), 4:43-44.)

III. DISPUTED '665 PATENT CONSTRUCTIONS

A. Term 1: “second voltage rail”

No.	Claim Term	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
1	“second voltage rail” '665 patent, claim 1	Plain and Ordinary Meaning Alternatively, “a second voltage rail that is distinct from the third voltage rail but may or may not be distinct from the first voltage rail”	“a second voltage rail that is distinct from the first voltage rail”

Aptiv’s proposed construction for “second voltage rail”—which seeks to preclude one structure from serving as both the “first voltage rail” and the “second voltage rail”—is contrary to the law and expressly contradicted by the specification.

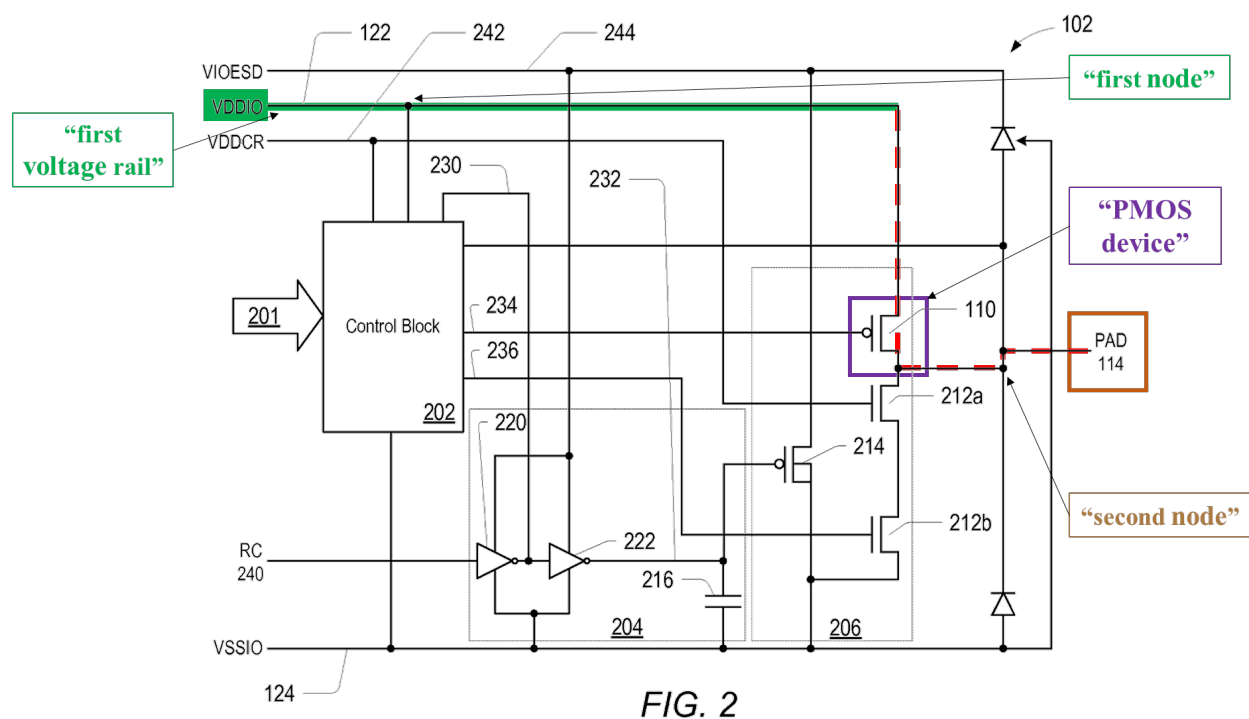
Aptiv’s construction appears to rest on the legally erroneous proposition that a single structure cannot satisfy multiple discrete claim limitations. The opposite is true. *E.g.*, *Powell v. Home Depot U.S.A., Inc.*, 663 F.3d 1221, 1231-32 (Fed. Cir. 2011) (finding that two limitations can be met by the same structure disclosed in the specification); *Skedco, Inc. v. Strategic Operations, Inc.*, 685 F. App'x 956, 959–60 (Fed. Cir. 2017) (reversing district court construction that failed to account for patent’s disclosure of a single structure meeting two limitations); *Hong Kong uCloudlink Network Tech. Ltd. v. SIMO Holdings Inc.*, 548 F. Supp. 3d 916, 928 (N.D. Cal. 2021) (“As a general matter, ‘the same structure can satisfy more than one limitation in a patent claim unless the claim specifies otherwise.’”).

Indeed, just last month the Federal Circuit reversed a PTAB claim construction that made the same mistake Aptiv urges here. *Google LLC v. Ecofactor, Inc.*, Nos. 2022-1750, 2022-1767, 2024 U.S. App. LEXIS 2795, *15-17 (Fed. Cir. Feb. 7, 2024). There, the Board had cited several “cases for the proposition that ‘[w]here a claim lists elements separately, the clear implication of the claim language is that those elements are distinct components of the patented

invention.” *Id.* at *9. The Federal Circuit rejected that analysis, explaining that, while “there is a ‘presumption’ that separately listed claim limitations may indicate separate and distinct physical structure, . . . that presumption may always be rebutted in the context of a particular patent.” *Id.* at *16; *see also Skedco*, 685 F. App’x 959-60.

That presumption is expressly rebutted here, because the ’665 patent explains that the first and second voltage rails may be the same structure. Namely, the ’665 patent (1) discloses that the claimed “first” and “second” “voltage rails” respectively are the “VDDIO” and “VIOESD” rails disclosed in the specification; and (2) instructs that “VIOESD 244 [*i.e.*, the “second voltage rail”] and VDDIO 122 [*i.e.*, the “first voltage rail”] may in fact be *the same power/supply rail*.” (’665 patent, 5:57-65.)

First, the ’665 patent makes clear that the claimed “first voltage rail” is the “VDDIO” rail disclosed in the specification, because both are described as connecting to an input/output pad via a “PMOS device” (*i.e.*, a transistor), which may be enabled to spread charge across multiple pads. Namely, as depicted in the below annotated version of Fig. 2, “**PMOS device 110** . . . [is] coupled between **VDDIO rail 122** and **PAD 114**.” (’665 patent, 4:33-35.) During an ESD event, the “**PMOS devices** turn[] on . . . resulting in the **charge** being shared across all **pads**” via the **VDDIO rail**. (’665 patent, 4:13-19; *id.* at 5:29-35.)



(*Id.*, Fig. 2.) Claim 1 recites the same relationship between the first voltage rail, the output transistor device(s), and the pad:

- a **first node** coupled to a **first voltage rail**;
- a **second node** coupled to a **physical pad** having capacitance;
- one or more **output transistor devices** [*i.e.*, PMOS devices] coupled between the **first node** and the **second node**

(*Id.*, claim 1.) And again, during an ESD event, claim 1 recites that a control block “turn[s] on the . . . one or more **output transistor devices**” to connect the **pad** to the **first voltage rail**, thereby sharing the charge. (*Id.*) Accordingly, the claimed “first voltage rail” is the “VDDIO” rail.

Similarly, the '665 patent makes clear that the claimed “second voltage rail” is the “VIOESD” rail disclosed in the specification, because both are described as connected to a low voltage rail via a clamp. Namely, as depicted in the below annotated version of Fig. 2, the

FIG. 2

(*Id.*, Fig. 2.) Again, claim 1 recites the same relationship, namely, “a **clamp device** configured between a **second voltage rail** and a **third voltage rail**.”⁴ (’665 patent, claim 1.) Accordingly, the claimed “second voltage rail” is the “VIOESD” rail.

It should also be noted that **VIOESD 244 and VDDIO 122 may in fact be the same power/supply rail**, and alternate embodiments may be configured with a single power rail providing power to the circuit and/or system components that are powered by VIOESD

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244 and VDDIO 122 in the embodiment shown in FIG. 2. In general, the **ESD rail and the power supply rail can be the same supply rail**, and separate supply rails (e.g. VIOESD 244 and a distinct VDDIO 122) may not be required.

(’665 patent, 5:57-65.) This express guidance rebuts any presumption that the first and second voltage rails must be distinct. Indeed, courts have held that “first” and “second” elements need not be distinct where a patent’s specification provides such a teaching. *See Linear Tech. Corp. v. Int’l Trade Comm’n*, 566 F.3d 1049, 1055-56 (Fed. Cir. 2009) (agreeing that “second circuit” and “third circuit” did not need to be separate and distinct); *Square D Co. v. E.I. Elecs., Inc.*, 685 F. Supp. 2d 864, 875-76 (N.D. Ill. 2010) (concluding that “a first power supply” and “a second power supply” “need not be independent”).

Moreover, the specification’s teaching that VIOESD (the “second voltage rail”) and VDDIO (the “first voltage rail”) may be the same power/supply rail is consistent with a POSITA’s understanding of real-world circuitry, which can be implemented with one or more rails. (Taylor ¶ 53; *see also id.* ¶¶ 50-52, 54-55.)

Accordingly, Aptiv’s construction should be rejected in favor of the plain meaning of the term. To the extent the Court would prefer to construe this term, it should adopt Microchip’s proposed construction, which implements the specification’s express guidance that the first and second voltage rails need not be distinct.

IV. DISPUTED '074 PATENT CONSTRUCTIONS

A. Term 3: “an enable/disable function to enable/disable the biasing circuit for reducing standby current”

No.	Claim Term	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
3	“an enable/disable function to enable/disable the biasing circuit for reducing standby current” '074 patent, claim 1	Not subject to 35 U.S.C. § 112 ¶ 6. To the extent the court determines that § 112 ¶ 6 applies: Function: to enable/disable the biasing circuit for reducing standby current Structure: enable/disable signal input line (Node M)	Indefinite; Subject to 35 U.S.C. § 112 ¶ 6 without any corresponding structure

Aptiv argues that this term is indefinite because (1) the “enable/disable function to enable/disable the biasing circuit for reducing standby current” is a means-plus-function term governed by 35 U.S.C. § 112 ¶ 6; and (2) the specification does not disclose corresponding structure.⁵ Aptiv is wrong on both accounts.

1. Means-Plus-Function Claiming Does Not Apply

Aptiv’s argument fails at the outset because the “enable disable function” is not a means-plus-function term. Because the claim language does not include the word “means,” there is a presumption that § 112 ¶ 6 does not apply. *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1348 (Fed. Cir. 2015) (en banc). Aptiv cannot rebut that presumption, because a POSITA would have understood the “enable/disable function” to refer to structure with “a reasonably well understood meaning in the art,” not a placeholder for unspecified structure. *Greenberg v. Ethicon Endo-Surgery, Inc.*, 91 F.3d 1580, 1583 (Fed. Cir. 1996).

⁵ Because the '074 patent claims priority to a provisional application filed before March 16, 2013, pre-AIA Section 112 applies. *Blue Calypso, LLC v. Groupon, Inc.*, 815 F.3d 1331, 1341 n.4 (Fed. Cir. 2016); *Solvay S.A. v. Honeywell Int’l Inc.*, 742 F.3d 998, 1000 n.1 (Fed. Cir. 2014).

Namely, a POSITA would have understood that an “enable/disable function . . . for reducing standby current” refers to an input for turning on or off the transistors that draw current, *i.e.*, a switch. (Taylor ¶ 57.) If that sounds simple, that is because it is. There is a limited menu of options in an electrical engineer’s toolkit for selectively enabling/disabling the flow of current, and by far the most common is simply applying a signal to turn off the transistors that current flows through. *Id.* This fundamental technique is used in everything from the low-power mode of a smartphone’s processor to the circuitry that disables the coils of a heater when a room has reached a desired temperature. *Id.*

Indeed, POSITAs routinely use the term “enable” to refer to an input for turning on and off the transistors that draw current. For example, technical documentation for commercially available low-dropout linear regulators often includes an “ENABLE” input line. (Taylor ¶ 58; Exs. 1-4.) Likewise, a 2012 textbook on digital circuit design describes circuitry “enable *e*” input for turning on or off transistors. (Taylor ¶ 58; Ex. 5.) (“When the enable *e* is high ($\bar{e}$ is low), the middle two transistors are on.”). Here too, a POSITA would have recognized the claimed “enable/disable function” to refer to known structure. (Taylor ¶¶ 56-61.)

Aptiv’s argument to the contrary appears to hinge on the assertion that the word “function” transforms this clear terminology into a means-plus-function placeholder. But “the mere fact that the disputed limitations incorporate functional language does not automatically convert the words into means for performing such functions.” *Zeroclick, LLC v. Apple Inc.*, 891 F.3d 1003, 1008 (Fed. Cir. 2018). Indeed, words may be “used in common parlance or by persons of skill in the pertinent art to designate structure . . . even if the term identifies the structures by their function.” *Skky, Inc. v. MindGeek, s.a.r.l.*, 859 F.3d 1014, 1019 (Fed. Cir. 2017). Accordingly, “[m]any devices take their names from the functions they perform. The examples are

innumerable, such as ‘filter,’ ‘brake,’ ‘clamp,’ ‘screwdriver,’ or ‘lock.’” *Greenberg*, 91 F.3d at 1583. That is particularly true here, in the context of integrated circuit design, where POSITAs regularly provide functional names to structural components so other engineers can easily understand their intended uses. (Taylor ¶ 60). Thus, inputs that control timing are typically called “Clock,” “CLK,” or “CK”; inputs that initialize the part are typically called “RESET”; and inputs that enable and disable circuitry are typically called “ENABLE/DISABLE,” “ENABLE” or “EN.”⁶ (Taylor ¶ 60).

2. Even if Means-Plus-Function Claiming Applied, the Specification Discloses Corresponding Structure

Even if the Court were to rule that this term is subject to § 112 ¶ 6, it is not indefinite, because the specification discloses structure corresponding to the claimed function. *Williamson*, 792 F.3d at 1351-52 (explaining that where § 112 ¶ 6 governs, “the court must determine what structure, if any, disclosed in the specification corresponds to the claimed function”).

The recited function—which Aptiv does not appear to dispute—is “to enable/disable the biasing circuit for reducing standby current.” The specification discloses exactly that. Namely, in describing the “biasing circuitry” of Fig. 3, the ’074 patent explains that “[t]ransistors 320, 330, 334 and 336 may be shut off during disabling/power down operation to make sure this circuit will consume substantially no DC current. . . . **Node M is the enable signal coming to the regulator circuit so that the module can be turned off when disabled.**” (’074 patent, 4:44-54.)

That is, as depicted below, input line M carries a signal that either (1) switches on transistors to

⁶ A POSITA would understand that the labels “enable” and “enable/disable” are interchangeable, and refer to the same structure. (Taylor ¶ 61). “Enable” is simply shorthand in which the “disable” is implied, because if an “enable” must either be on (*i.e.*, enabling transistors) or off (*i.e.*, disabling transistors). (*Id.*)

enable the necessary flow of current in the biasing circuitry; or (2) switches off transistors to disable the flow of current in the biasing circuitry. (Taylor ¶ 63.)

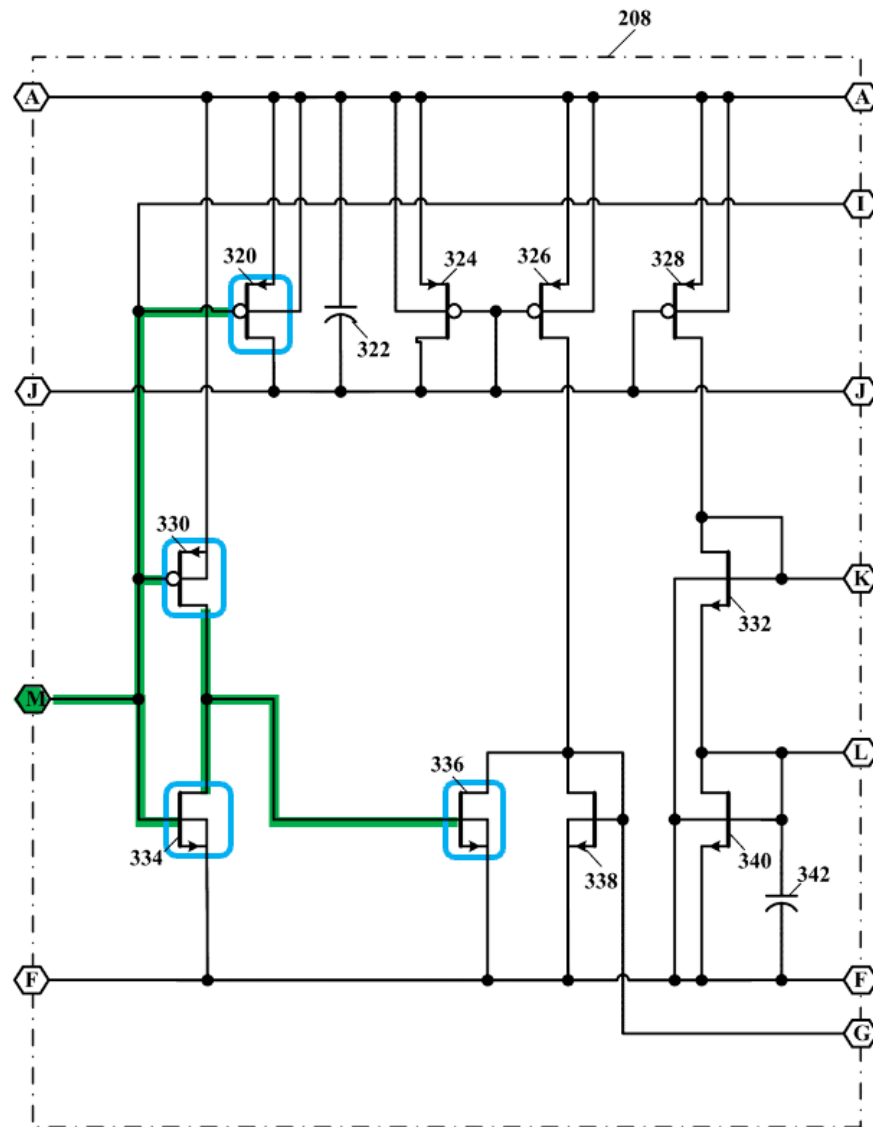


FIGURE 3

(’074 patent, FIG. 3 (annotated), 4:43-44.)

Based on this disclosure, a POSITA would have understood that the corresponding structure to “enable/disable the biasing circuit for reducing standby current” is Node M’s enable

signal input line, which permits or restricts the flow of current through biasing transistors to conserve power. (Taylor ¶¶ 62-63.)

B. Term 4: “wherein the gm-boost circuit enables the current buffer driver to have large gm value”

No.	Claim Term	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
4	“wherein the gm-boost circuit enables the current buffer driver to have a large gm value” '074 patent, claim 4	Not indefinite. Plain and Ordinary Meaning. Alternatively, “wherein the gm-boost circuit increases the gm value of the current buffer driver”	Indefinite

Contrary to Aptiv’s proposed construction, the term of degree “large gm value” does not prevent a POSITA from understanding the scope of the claims with reasonable certainty, because the specification provides guidance for assessing how large a gm value is required in the context of real-world voltage regulators.

As this Court has recognized, “[n]ot every term needs to be reduced to a numerical certainty to avoid an indefiniteness problem.” *Med-El Elektromedizinische Geräte Ges.M.B.H. v. Advanced Bionics, LLC*, 2020 U.S. Dist. LEXIS 164738, at *7-8 (D. Del. Sep. 9, 2020) (“Here, the claim term uses qualitative terms, but that does not render it indefinite.”). Rather, “[c]laim language employing terms of degree has long been found definite where it provide[s] enough certainty to one of skill in the art *when read in the context of the invention.*” *Niazi Licensing Corp. v. St. Jude Medical S.C., Inc.*, 30 F.4th 1339, 1347 (Fed. Cir. 2022) (quoting *Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1370 (Fed. Cir. 2014)) (finding terms not indefinite because “[t]he intrinsic record provides objective boundaries by which a skilled artisan could determine the scope of the claims”).

Here, the specification provides sufficient guidance for a POSITA to determine the bounds of the claims with reasonable certainty. The claimed invention seeks to enable a regulator to work with external capacitors with a wide range of ESR values. ('074 patent, 1:55-59.) One obstacle to this objective is that the regulator's output power driver must "provide very large amounts of switching current," which creates "a pole at relatively low frequency" that may undermine the stability of the regulator. (*Id.*, 4:6-11.) To solve this problem, the '074 patent prescribes coupling a "current buffer driver . . . between [an] operation amplifier and the output power driver." ('074 patent, 6:3-12.) In this configuration, "the current buffer driver 204 pushes [the amplifier's] pole to a high frequency" to create a "pole-splitting effect" between the amplifier's high frequency pole and the output driver's low frequency pole. ('074 patent, 4:11-14; *see id.* at 5:40-45 (referring to this effect as creating a "pseudo 'one-pole' system"); Taylor ¶¶ 65-67.)

But the specification explains that not just any current buffer driver will do. Rather, "[t]o achieve this, it is necessary to provide a fairly large gm value of the current buffer driver 204." ('074 patent, 4:14-15.) In other words, the specification provides a POSITA objective guidance as to the meaning of "large gm" value: it must be sufficiently large to provide a pole splitting effect that pushes the undesirable pole to a higher frequency. (Taylor ¶¶ 65-68.) Accordingly, in the context of real-world circuitry, a POSITA can readily identify the requisite gm to ensure the performance and stability of a given regulator. (Taylor ¶ 68.).

This guidance is sufficient to render the claims definite. Indeed, "all that is required is some standard for measuring the term of degree." *Exmark Mfg. Co. v. Briggs & Stratton Power Prods. Grp., LLC*, 879 F.3d 1332, 1346 (Fed. Cir. 2018). For instance, in *Exmark*, the Federal Circuit concluded that the claim term "elongated and substantially straight" was not an indefinite

term of degree because “the claims and specification provide that the elongated and straight portion of the baffle must be long enough and straight enough to at least connect these two arcuate portions of the baffle.” *Id.* at 1345. The same result applies here because the specification teaches that the gm value must be sufficiently large to achieve pole-splitting. *See Ironburg Inventions Ltd. v. Valve Corp.*, 64 F.4th 1274, 1285-1288 (Fed. Cir. 2023) (finding terms “elongate” and “substantially the full distance” not indefinite in view of the specification’s guidance because “the need to meet the purpose of the claimed invention . . . helps inform one of ordinary skill’s understanding of the scope of the claims with reasonable certainty”); *Gen. Elec. Co. v. LPP Combustion, LLC*, Case No. 22-720-GBW, 2023 U.S. Dist. LEXIS 157219, at *37-*41 (D. Del. Sept. 6, 2023) (finding the term “acceptable range” definite in view of the specification’s guidance).

Moreover, Aptiv’s insistence that the claims must recite a particular gm value with greater certainty would impose an impossible standard. The requisite gm is a context-dependent value that depends on real-world variables including the impedance of the device the regulator is driving, the amount of power the regulator must deliver, the precision of the power supply driving the regulator, the response time required of the voltage regulator, the specific semiconductor manufacturing process used to fabricate the regulator circuit, and more. (Taylor ¶¶ 69.) Accordingly, the requisite gm will vary significantly depending on context and application. *Id.* Especially given these practical constraints, numerical precision is not required; the ’074 patent need only provide guidance to enable a POSITA to evaluate the claim scope in the context of real-world circuitry. *See Ironburg*, 64 F.4th at 1285 (noting that “numerical precision is not always required, even when using a term of degree” and claims are definite so long as “the patent provides sufficient guidance to give one of ordinary skill reasonable certainty as to the scope of

the claims”); *Focus Prods. Grp. Int'l, LLC v. Kartri Sales Co.*, Case No. 14-cv-10154 (PAE), 2018 U.S. Dist. LEXIS 134661, at *24-*26 (S.D.N.Y. Aug. 9, 2018). That is exactly what it does.

C. Term 5: “low gain and high bandwidth amplifier”

No.	Claim Term	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
5	“low gain and high bandwidth amplifier” '074 patent, claims 8, 9	Not Indefinite. Plain and Ordinary Meaning. Alternatively, “amplifier optimized for high bandwidth with a commensurate reduction of gain”	Indefinite

Contrary to Aptiv’s proposed construction, the term “low gain and high bandwidth amplifier” is not indefinite. As discussed in the context of term 4 (“large gm”), both this Court and the Federal Circuit routinely find terms of degree definite, so long as a POSITA can evaluate their scope with reasonable certainty. *E.g.*, *Niazi*, 30 F.4th at 1347. That is precisely the case here, at least because (1) the well-known sliding-scale relationship between gain and bandwidth would have provided reasonable certainty to a POSITA; and (2) the specification provides *additional* guidance for assessing gain and bandwidth in the context of the claimed voltage regulator.

First, the basic scientific principle that there is a sliding-scale relationship between gain and bandwidth would have guided a POSITA with reasonable certainty. (Taylor ¶ 71.) Namely, for a given operational amplifier, a POSITA would have understood that the mathematical product of gain and bandwidth is approximately constant (*e.g.*, $\text{Gain} \times \text{Bandwidth} = 100 \text{ MHz}$). (Taylor ¶¶ 48-49.) Accordingly, a decrease in gain yields a proportionate increase in bandwidth, and vice versa. *Id.* Traditional operational amplifiers are high-gain devices with, consequently, lower bandwidth. (Taylor ¶ 71.) With this context, a POSITA would understand that the

claimed “low gain and high bandwidth amplifier” simply refers to an operational amplifier configured at the opposite end of the sliding scale from a traditional operational amplifier. *Id.* Moreover, a POSITA would know that such an operational amplifier could be achieved with a simple feedback loop, which is a standard technique for increasing bandwidth. (Taylor ¶¶ 73-75.)

Second, as with term 4 (“large gm”), the ’074 patent’s guidance regarding the desired “pole-splitting” effect provides reasonable certainty to a POSITA. (Taylor ¶¶ 70-76.) Namely, the ’074 patent explains the need to address the amplifier’s “fairly high frequency pole that would be irrelevant to interact with the system dominant pole . . . thereby having more efficient pole-splitting, and allowing easier frequency compensation.” (’074 patent, 4:57-64; *id.* at 3:25-28.) To achieve this objective, the specification employs, among other things, a “low-gain, high-bandwidth amplifier” configured so that:

(1) The architecture ***forms only one pole*** at the output of the folded stage which reduces the complexity of frequency compensation, (2) it ***provides a good driving capability*** for the source follower stage of the current buffer

(’074 patent, 4:24-42; *see id.* at 4:1-4 (explaining that the operational amplifier should have “a single pole at the output that minimizes the complexity of its compensation”).) That is, the operational amplifier must balance (1) having sufficient bandwidth such that it forms only a single pole; but (2) still offering sufficient gain to drive the current buffer. (Taylor ¶ 72.) The intersection of these two functional metrics would further assist a POSITA to identify where on the sliding scale between gain and bandwidth the claimed operational amplifier should sit. *See Ironburg*, 64 F.4th at 1285-1288; *Exmark*, 879 F.3d at 1346; *Gen. Elec. Co.*, 2023 U.S. Dist. LEXIS 157219 at *37-41. (Taylor ¶¶ 70-76.)

DATED: March 1, 2024

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CERTIFICATE OF SERVICE

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**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

MICROCHIP TECHNOLOGY INC.,

Plaintiff,

v.

APTIV SERVICES US, LLC,

Defendant

C.A. No. 1:23-CV-00778-JDW

JURY TRIAL DEMANDED

**GREG TAYLOR DECLARATION
IN SUPPORT OF MICROCHIP'S OPENING CLAIM CONSTRUCTION BRIEF**

I, Greg Taylor, do hereby declare as follows:

I. Introduction

1. I have been asked to provide my opinions regarding certain claim constructions, and the definiteness of some claims from U.S. Patent Nos. 7,564,665 (“’665 patent”) and 9,471,074 (“’074 patent”). I may refer to the patents collectively as “the Asserted Patents.”

2. I am being compensated at my usual hourly rate for my work in this case. My compensation is not based upon the outcome of the case or the Court’s determinations related to claim construction.

3. In preparing this Declaration and formulating my opinions within, I have considered the ’665 patent and its prosecution history, the ’074 patent and its prosecution history, the parties’ Joint Claim Construction Chart submission in this matter and associated exhibits, along with my personal expertise, knowledge, and experience with the relevant technology, and the materials referenced or mentioned in the body of this declaration. There are images and explanations in this Declaration included for illustrative purposes, some of which I created myself.

Images taken from patents and publications have been cited. At the time of my signing this declaration, all the hyperlinks referenced herein were publicly accessible.

II. Background and Qualifications

4. I have summarized in this section some of my educational background, career history, publications, and other relevant qualifications. My full curriculum vitae is attached as Appendix A to this declaration. During the past 5 years I submitted declarations in inter partes reviews IPR2022-00481 and IPR2022-00285, and Ex Parte Reexamination Nos. 90/019,063 and 90/019,015, but otherwise have not testified in any cases.

5. I earned a Doctor of Engineering (Ph.D.) degree in Computer and Systems Engineering from Rensselaer Polytechnic Institute in 1985. From 1986 to 1991 I worked as a Circuit Design Engineer and then Principal Design Engineer for Bipolar Integrated Technology. I started as a new hire from the Ph.D. program at RPI and ended up as the chief architect, lead product designer, lead verification engineer, and developer of the world's only formal verification tool for bipolar circuits.

6. From 1991 until 2016, I worked for Intel Corporation, starting as a Senior Staff design engineer and quickly became a team leader delivering the package, I/O, and analog circuits for the first processors on each technology generation. In 2002 I was promoted to Intel Fellow (one of the company's highest technical positions) based on both results and risk management in getting five generations of microprocessors into high volume manufacturing on schedule, including the first use of C4 packaging at Intel. From 2002 to 2016 I worked as director of numerous groups within Intel (Mixed Signal Circuit Technology, Circuit Research Lab, SoC Design Lab, Low Power Mixed Signal Lab), where I led teams that delivered three separate firsts for both Intel and the world: the first microprocessors using strained silicon, the first products using high-k metal gate transistors, and the first Trigate (FinFET) product. During this time my role expanded to

leading a new company-wide analog/mixed signal circuit review team and leading the worldwide circuit architecture teams for I/O, analog, and supply regulator design IP. I currently operate my own consulting firm (Greg Taylor Consulting, Inc.), where I provide technical consulting services on electronic product and integrated circuit development for a variety of clients.

7. Additionally, I have been an IEEE Fellow since 2009. I have published more than 60 peer reviewed papers, and I am the inventor of 67 U.S. patents on integrated circuit design and testing.

8. Throughout my career, I have been involved in the design of I/O circuits that were required to survive electrostatic discharge events. This required understanding the discharge types, the paths that current would follow in an ESD event, and then designing pad cells, clamps, pad wiring, and power supply wiring to mitigate the effects of ESD.

9. In addition to the above, I was also responsible for power distribution circuitry in several generations of microprocessors I worked on. This included not just distributing large currents at low impedances to the digital circuits on chip, but also building on-chip regulators to power the less noise-tolerant analog circuits that were also integrated on chip. Later, while I was leading the Circuit Research Lab at Intel Corporation, my team successfully developed a 100 MHz on-chip switching regulator technology that took a high voltage input supply (twice what any transistor on the chip could survive) and delivered a high efficiency, clean, low voltage output without using any board level passive components.

III. Legal Standards

10. I am not an attorney and will not provide opinions of law. I have been instructed on principles of law, as set forth below, so that I may apply those principles, as appropriate, to my analysis.

A. Claim Construction

11. I understand that claim construction is a matter of law to be decided by the Court, but the Court may use input from expert testimony to assist in its determination of the meaning of claim terms.

12. I understand that terms in patent claims are given their ordinary and customary meaning as they would be understood by a person having ordinary skill in the art at the time of the invention (“POSITA”). In determining the ordinary and customary meaning, I understand one should look to those sources available that show what one of skill in the art would have understood disputed claim language to mean. I understand that the words of the patent’s claims and the context in which the term is used in the patent’s claims can be highly instructive in ascertaining the term’s meaning. I further understand that the terms of a claim are interpreted in the context of the entire patent, including the patent’s claims, its specification, its figures, and the prosecution history, also referred to as “intrinsic evidence.”

13. I understand that “extrinsic evidence”—i.e., evidence external to the patent and the prosecution history—includes evidence concerning the relevant scientific principles, the meaning of technical terms, and the state of the art. I understand that such evidence may also be useful in interpreting patent claims when the intrinsic evidence itself is insufficient. I understand that when patents and their claims refer to or utilize terminology from industry standards, the disclosures of the industry standards may also be useful in interpreting patent claims.

14. I understand that words or terms should be given their ordinary and customary meaning to a POSITA unless it appears that the inventors were using them to mean something else. In making this determination, the claims, the patent specification, and the prosecution history are of paramount importance. Additionally, the specification and prosecution history may be consulted to confirm whether the patentee has acted as its own lexicographer (i.e., provided its

own special meaning to any disputed terms), or intentionally disclaimed, disavowed, or surrendered any claim scope.

15. I understand that in general, a term or phrase found in the introductory words of the claim—the preamble of the claim—is limiting if it recites additional structure or steps, or is necessary to give life, meaning, and vitality to the claim. Conversely, a preamble term or phrase is not limiting where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention. In making this distinction, one should review the entire patent to gain an understanding of what the inventors claim they actually invented and intended to encompass by the claims.

B. Indefiniteness

16. I understand that a patent claim must particularly point out and distinctly claim the subject matter which the applicant regards as his invention. I understand that a patent claim is invalid if, read in light of the specification and the prosecution history, the claim fails to inform, with reasonable certainty, those skilled in the art about the scope of the invention. I understand that a patent claim must be precise enough to afford clear notice of what is claimed, thereby apprising the public of what is still open to them, while recognizing that absolute precision is unobtainable.

17. I understand that the indefiniteness inquiry focuses on the understanding of a skilled artisan at the time of the patent application. To understand the meaning of a claim term as understood by persons of skill in the art, I understand that courts may look to the intrinsic record, including the specification and the prosecution history, as well as extrinsic evidence, such as expert testimony, dictionaries, and learned treatises.

18. I also understand that so-called “terms of degree” are not necessarily indefinite and numerical precision is not required. Rather, I understand that Courts look to see whether the

claims and intrinsic record provides sufficient guidance to give one of ordinary skill reasonable certainty as to the scope of the claim.

C. Means Plus Function Claims

19. I understand that a means-plus-function claim term is one that recites a placeholder referring to a function, with the corresponding structure for performing that function identified in the specification.

20. I understand that, if a claim term uses the word “means” (e.g., “means for transmitting” or “transmitting means”), it is presumed to be a means-plus-function term. If, on the other hand, a claim term does not use the word “means,” it is presumed not to be a means-plus-function term. However, this presumption may be overcome where a claim term does not use the word “means” but recites a function without reciting sufficient structure for performing that function. For example, if a term uses functional language and/or a nonce word that would have the same effect as the word “means,” and does not provide sufficient structure, the presumption against means-plus-function claiming will be overcome. By contrast, where a term is used in common parlance byPOSITAs to designate a particular structure or class of structures, it is considered to have sufficient structure, and therefore will not be considered a means-plus-function term.

21. If a claim term is a means-plus-function term, the specification must supply the corresponding structure to carry out the function. If there is no corresponding structure in the specification, the term is indefinite.

IV. Level of Ordinary Skill in the Art

22. I have been asked to consider the abilities and education of a person of ordinary skill in the art as of the priority dates that apply to each of the Asserted Patents. The application

leading to the '665 patent was filed January 10, 2007. The application leading to the '074 patent was filed March 11, 2014, but claims priority to a provisional application filed March 14, 2013.

23. In my opinion, with respect to the '074 Patent, a POSITA would have a bachelor's degree in electrical engineering, computer science, or an equivalent technical degree and substantial experience (e.g., several years) in analog mixed signal design for integrated circuits. With respect to the '665 Patent, a POSITA would have a bachelor's degree in electrical engineering, computer science, or an equivalent technical degree and substantial experience (e.g., several years) in I/O and ESD design for integrated circuits. In either case, additional education related to the hardware, architecture, and circuit design aspects of could be substituted for professional experience, and vice versa.

24. While my experience level exceeds that of a POSITA, I am familiar with POSITAs from the time frame of the priority dates of the Asserted Patents, and my opinions regarding what a POSITA would understand are based on a POSITA's perspective at those times.

V. Technology Background

A. Electrostatic Discharge (ESD) Protection and the '665 Patent

25. In integrated circuits, ESD refers to the sudden inrush of current that can happen when the chip is brought into contact with static electricity. This is typically a concern during the processes of packaging chips and assembling chips onto printed circuit boards, though ESD events can occur in other circumstances as well. In the case of assembly, chips or boards may accumulate a static charge during shipment. This charge is rapidly dissipated as the two get close enough together to breakdown the air gap that separates them.

26. Typical integrated circuits operate at only a few volts and usually cannot tolerate higher voltages for very long. ESD discharges are therefore problematic because they can

involve hundreds or thousands of volts. Sometimes these high voltages will destructively break down an oxide on a chip, but more frequently the damage is thermal: the rapid deposition of a lot of energy in a small area can melt wires. In more spectacular cases, the wire can evaporate and explode, leaving a crater on the surface of the integrated circuit. In each of these cases, the strategy for mitigating ESD is to dissipate the energy so that there isn't enough charge concentrated in any small area to cause damage.

27. Since ESD events typically occur during chip assembly, ESD protection must account for the fact that the power supplies normally used to operate the chip are not themselves active (or even installed yet). This means that any circuitry that is intended to handle ESD must be powered by the ESD itself. (See Basic ESD and I/O Design, Sanjay Dabral & Timothy Maloney, John Wiley & Sons, 1998, section 2.7.1.)

28. When evaluating ESD protection circuitry it is important to keep in mind Kirchoff's First Law, which states that the net current flowing into any node is zero, i.e. the current flowing into the node is equal to the current flowing out of the node. This means that, although the static electricity that triggers an ESD event is typically introduced to the chip on one specific pad, the current flows from that pad to other places until it finds its way back off the chip. Design for ESD tolerance largely consists of managing the flow of that current while dissipating (generating heat in resistances) and/or storing (in capacitors) its energy.

29. The '665 patent discloses an invention for mitigating the effects of ESD. Namely, the '665 patent discloses a multi-pad system wherein "pad circuitry" is connected to each pad. When a static electric charge is deposited on a pad, that static charge opens a path from the pad to a common voltage rail (or multiple voltage rails) shared by all pads. The static charge then powers portions of the pad circuitry of the other pads, which in turn enable transistors to create a

conductive path between their pads and the common voltage rail. This creates an electrical connection between the pad where a static electric charge was deposited through the common voltage rail to the other pads of the system, allowing the charge to be spread out and shared by all pads, preventing the harmful concentration of charge in any one location.

B. USB Voltage Regulators and the '074 Patent

30. An important component in modern electronics is the voltage regulator—used to ensure that an electronic device has a steady voltage supply during all operational conditions. One form of voltage regulator addressed by the '074 patent is a “low-dropout (LDO) voltage regulator.” Because an LDO voltage regulator is, generally speaking, a form of a linear amplifier with feedback, it will be helpful to understand some basic concepts in amplifier circuitry.

1. Amplifiers and Feedback

31. Amplifiers are widely used in electronic systems to magnify small signals, drive large loads, and compensate for the degradation of signals propagating from one location to another.

32. One of the simplest amplifiers is a source follower, as shown in Figure 1 below. (Analysis and Design of Analog Integrated Circuits, Fourth Edition, Gray, Hurst, Lewis, Meyer, John Wiley & Sons, 2001, section 7.2.3.2) This circuit is used to isolate signal IN from the capacitance of the load OUT it drives. The strength (current) with which it drives the load is given by the transconductance of the MOSFET, known as “*gm*.” In general, *gm* of a MOSFET is given by $gm = \frac{2I_{DS}}{V_{GS} - V_t}$, where I_{DS} is the drain to source current, V_{GS} is the gate to source voltage, and V_t is the threshold voltage of the transistor. In these source followers, *gm* is determined by the value of the load resistor and the starting voltage of IN, as well as the specific transistor.

When the voltage gain of an amplifier remains very close to 1, also known as “unity gain”—the output is a replica of the input shifted by the threshold voltage of the source follower.

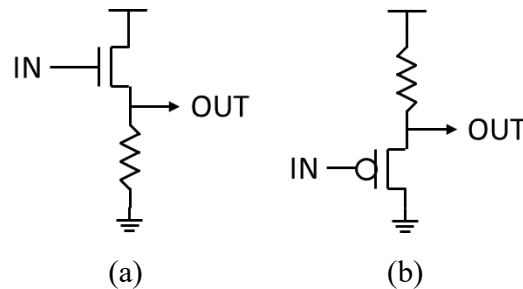


Figure 1. Source followers. (a) NMOS, (b) PMOS

33. Further, feedback techniques allow designers to create amplifiers with stable, predictable gain by leveraging negative feedback and passive components (primarily resistors and capacitors).

34. The operation of negative feedback is shown in Figure 2 below. (Analysis and Design of Analog Integrated Circuits, Fourth Edition, Gray, Hurst, Lewis, Meyer, John Wiley & Sons, 2001, section 8.7) The amplifier has a large DC gain of A and produces an output that is A times the difference in its input voltages. This information allows us to solve for the gain of the circuit, since we know the gain of the amplifier, the value of the resistors, and that no current flows into the inputs of the amplifier, yielding $\frac{OUT}{IN} = \frac{A}{1+A\beta}$, where $\beta = \frac{R2}{R1+R2}$. If the gain of the amplifier is large, then we have $\frac{OUT}{IN} = \frac{A}{1+A\beta} \cong \frac{1}{\beta} = \frac{R1+R2}{R2}$. So, the gain of the circuit is stable (controlled by the ratio of the resistors and independent of variation in the amplifier) as long as the gain of the amplifier remains large. Thus, the appropriate application of feedback overcomes the inherent variation in the transistors that provide the gain.

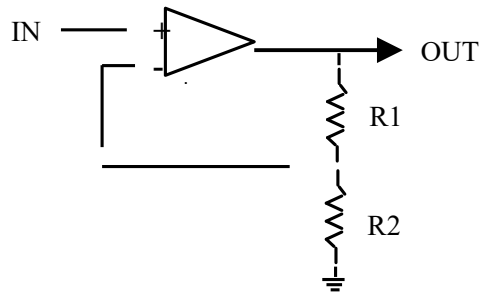


Figure 2. Negative Feedback

35. When the input signal IN is changing, the amplifier may end up amplifying the difference between the changing input and an older delayed output because not only do amplifiers have gain, but they also delay the input signal a small amount. If we input a sinusoidal signal into the amplifier and ramp up the frequency, the system will behave differently depending on the speed of the frequency. When the frequency is slow compared to the delay of the amplifier then circuit still responds as if it were a simple amplifier. But as the input changes more quickly (at a higher frequency) the amplifier is now amplifying the difference between the input and an older, delayed output. At some frequency this delay will result in the peaks of the input being compared to the troughs of the output (and vice versa) resulting in an output that swings between very large positive and negative voltages. The amplifier has become unstable.

36. Real amplifiers have a saving grace: when the input is pushed beyond some threshold frequency, the amplifier's gain starts dropping and continues to drop further as the frequency is increased. If the gain of the amplifier drops below 1 before it reaches the frequency where the peaks of the output collided with the troughs of the input, then the instability problem is resolved because that instability will be amplified by a gain of less than 1, i.e., it will be reduced.

37. Note that the output of the amplifier feeds back to the input, repeatedly passing through this gain. Accordingly, a small instability going repeatedly through a gain that amplifies it even a small amount will eventually overwhelm the amplifier response. Similarly, an

instability that repeatedly goes through a gain that shrinks it will eventually disappear. Put another way, the gain amplifies the degree of instability; if the “gain” experienced by the instability is less than 1, the “good” parts of the signal will be amplified while the instability is filtered away.

38. This leaves the problem of determining the stability of a feedback system. Mathematical “transfer functions” and Bode plots (such as those shown in Figure 1 of the ’074 patent) can help answer this.

2. Transfer Functions, Bode Plots, and “Poles and Zeroes”

39. In circuit analysis, a transfer function describes the mathematical relationship between a circuit’s input and its output as a function of frequency. (The Analysis of Linear Circuits, Charles M Close, Harcourt, Brace & World, 1966, section 6.1) Input frequencies that result in the transfer function equaling zero are known as “zeroes” and input frequencies that result in the transfer function equaling infinity are known as “poles.” “Poles” determine the “free response” or “natural behavior” of the system – how that system responds to changes. (The Analysis of Linear Circuits, Charles M Close, Harcourt, Brace & World, 1966, section 3.1) Note that the usage of “frequency” in this type of analysis is based on these frequencies being complex numbers of the form $\sigma + j\omega$, where $j = \sqrt{-1}$. Furthermore, the sinusoidal waveforms that we normally work with in the time domain are represented in the s-domain by $s = j2\pi f$, where “f” is the time domain frequency. Thus, a hypothetical transfer function $\frac{V_{out}}{V_{in}} = \frac{s-100}{s-5000}$ would describe the ratio of V_{out} (the output voltage of the circuit) to V_{in} (the input voltage of the circuit) as a function of frequency (s). This hypothetical function has a zero at 100 Hz, and a pole at 5000 Hz. Generally speaking, the number and value of those poles and zeroes dictates the stability of the circuit. In practice, the actual values of the poles and zeroes in a manufactured circuit will differ

from design intent based on the variation of real components from their target values. Thus, circuit designs should not be designed as “just barely” stable, but should include a margin of stability that will allow for these variations while maintaining stability.

40. Figure 3 below shows a Bode plot for a simple (first order or “single pole”) amplifier with 50 dB¹ of gain and a pole at 100 Hz. (The Analysis of Linear Circuits, Charles M Close, Harcourt, Brace & World, 1966, section 6.5) This plot includes two curves, a blue curve showing the gain of the amplifier and an orange curve showing the phase. The phase is a measure of the delay of the amplifier with respect to the signal frequency. When the phase is 0°, the output is aligned with the input (i.e., there is no delay). When the phase is -180° then the output peaks are aligned with the input troughs, which, as described above, leads to instability. One measurement of the stability of a system is the “phase margin”: the difference between the phase of the amplifier and -180° at the frequency where the gain drops to 0 dB (gain=1) (the “unity gain frequency”). This Bode plot shows a unity gain frequency of 30 KHz, because that is the frequency where the gain is 0 dB. At that point, the phase is -90°. Accordingly, this Bode Plot shows 90° of phase margin (-90° - -180° = 90°). Because the phase margin is significantly greater than zero at the unity gain frequency, this system is stable. That is generally true of first order systems. Unfortunately, real amplifiers (systems) are more complicated.

¹ Gain is measured in decibels (dB). When measuring the voltage of a signal the gain in decibels is given by the equation $Gain_{dB} = 20 \log_{10} H(f)$, where $H(f)$ is the linear gain of the amplifier as a function of frequency. Since the gain rolls off proportional to $1/f$ measuring gain in decibels converts this roll off to a line on a log plot such as a Bode plot.

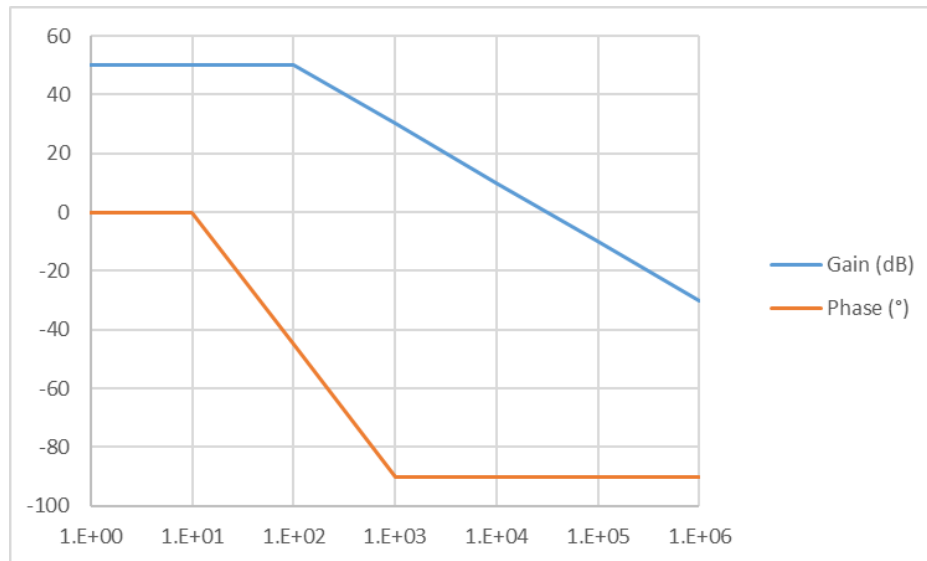


Figure 3. Bode plot for a first order amplifier

41. Bode plots are used because they can be easily constructed by hand without the use of computers once the poles and zeros of the system and the gain at a given frequency are known. Here the initial gain is 50 dB and this gain continues until the frequency of the first (and only) pole at 100 Hz. Beyond this pole the gain changes by -20 dB/decade (that is it drops by 20 dB (100x) for every 10x increase in frequency). At each additional pole the gain would drop by another -20 dB/decade when the frequency hits that pole value. In a similar manner, the phase changes by -90° as a pole is passed, with half of this change occurring a decade before the pole and half after. If there are additional poles, then the phase would accumulate an additional -90° of phase as each pole is passed. Zeros are the opposite of poles: as a zero is passed the slope of the gain is increased by 20 dB/decade and the phase is changed by $+90^\circ$.

42. Using this analysis, we can easily show what happens if the system has two poles at 100 Hz instead of a single pole, as shown in Figure 4. In this case the gain starts dropping by 40 dB/decade at 100 Hz, while the phase shifts by -180° around the same frequency. The phase hits -180° around a decade later while the gain is still 10 dB, enough to amplify the misaligned signals with the output fed back to be further amplified, ad infinitum (or at least until something

breaks). (The Analysis of Linear Circuits, Charles M Close, Harcourt, Brace & World, 1966, section 9.3.)

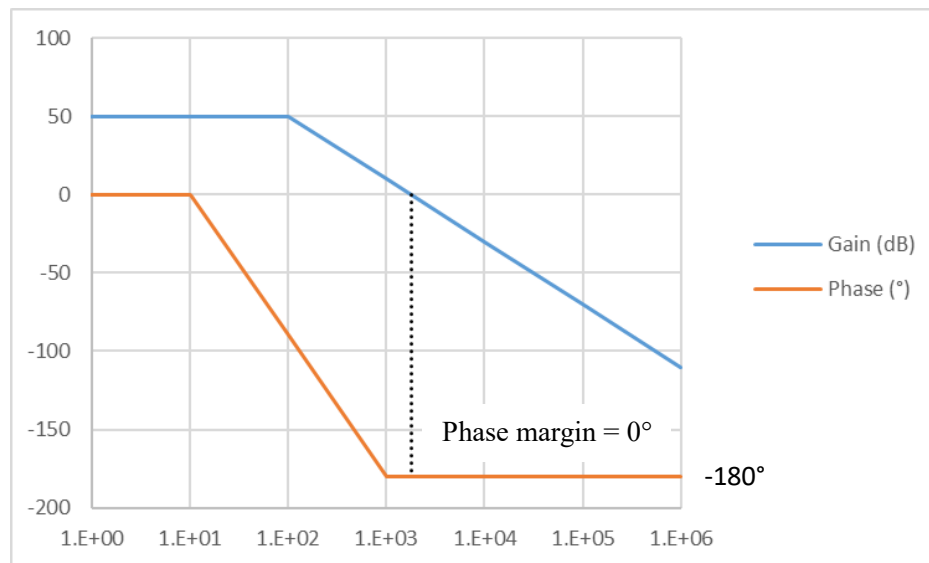


Figure 5. Bode plot with a double pole at 100 Hz

43. Figure 5 shows what the system looks like if the second pole is pushed to 100 kHz. This is beyond the frequency where the first pole has dropped the gain to zero, and as a result the system looks more like Figure 3. In this case the first pole dominates the behavior of the system, and it remains stable. Note that even though the dominant pole is three orders of magnitude lower than the added pole, the added pole still noticeably reduced the phase margin of the system.

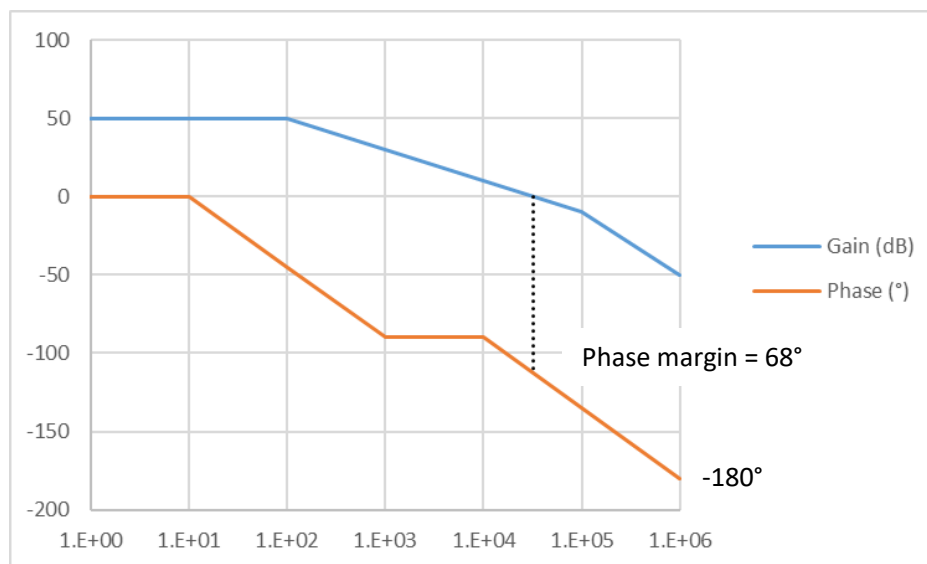


Figure 5. Bode plot with poles at 100 Hz and 100 kHz

44. The performance of a voltage regulator, reflected in its transfer function, is dictated by the type of components and arrangement of components comprising that regulator. For example, Low Dropout Regulators typically include an output capacitance to deal with high frequency changes in the load current. The series resistance (ESR or Effective Series Resistance) of the wires leading to the capacitor, shown in Figure 6, contributes a zero to the regulator. The frequency of this zero is given by $f_{zero} = \frac{1}{2\pi R_{ESR} C_{OUT}}$. As mentioned earlier, in the corresponding Bode plot, this zero adds +90° to the phase and causes the magnitude to rise at 20 dB/decade. And if the capacitor ESR varies, then the placement of this zero will shift.



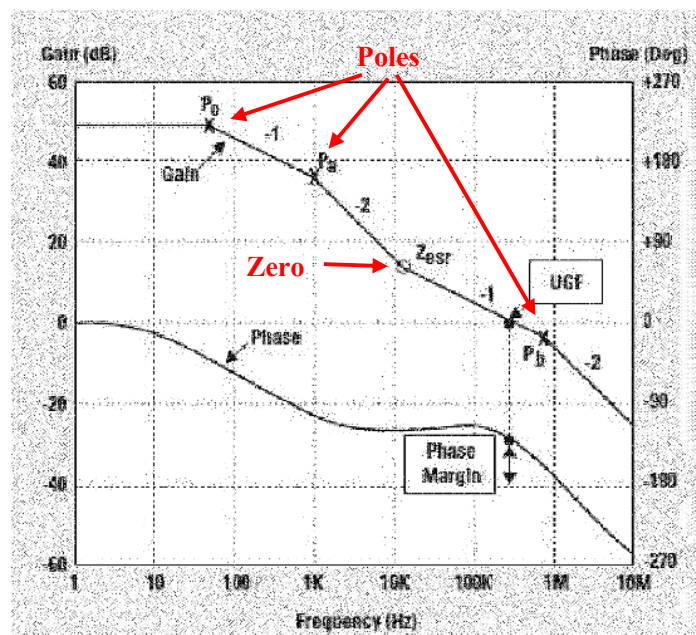
Figure 6. Capacitor and ESR model

45. And as the '074 patent explains, because the ESR of external compensation capacitors can vary widely depending on a lot of factors outside the regulator designer's control, including the capacitor manufacturer, the orientation of the capacitor on the physical board, the

quality and length of the traces (wires) connecting the capacitor to the regulator, etc., this poses a big problem for designers hoping to build a stable regulator that can handle a wide range of ESR values. '074 patent, 1:25-45.

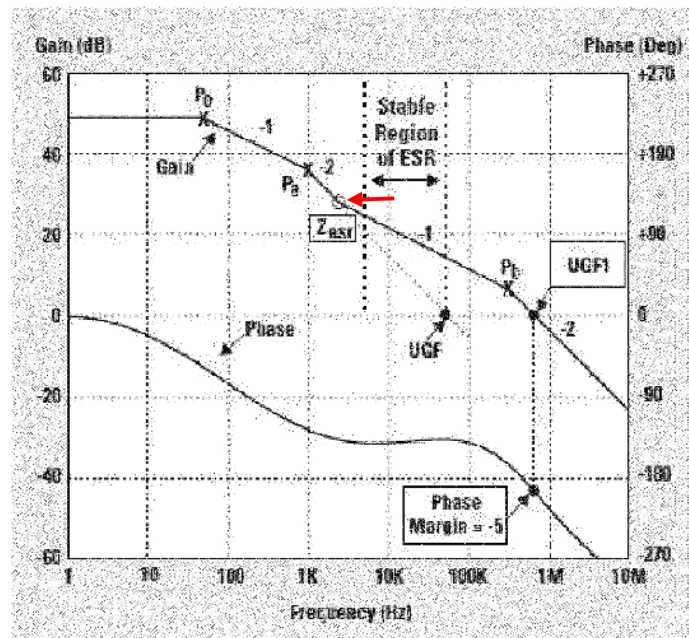
46. This problem is discussed in the context of the Bode plots in the '074 patent.

Figure 1(a) from the '074 patent is shown below and shows three poles, P_0 (~50 Hz), P_a (~1 kHz), and P_b (~800 kHz), as well as one zero provided by the ESR of the decoupling capacitor at about 10 kHz, annotated in red. The original also includes annotations between the locations of the poles and zero indicating the net number of zeros to the left of the point where the annotation is made. Thus, we see -1 between the first two poles, indicating that the slope is -20 dB/decade; followed by -2 after the second pole, indicating a slope of -40 dB/decade. This changes back to -1 after the zero and to -2 again after the third pole. Finally, the original includes annotation showing 40° of phase margin at the unity gain frequency ("UGF").



'074 Patent Figure 1(a) Normal Frequency Response with annotation
Prior Art

47. Figure 1(b) in the '074 patent shows what happens if the ESR of an external capacitor is more than doubled, shifting the zero to ~ 2 kHz. This pushes out the unity gain frequency, reducing the phase margin to -5° , driving the Bode plot well into instability. This variation could be caused by the use of a different capacitor, manufacturing variation in the capacitor, different mounting on the board, differences in the manufacturing or design of the board, or a combination of all of these factors. The original patent figure includes annotations showing the acceptable frequency range for the “zero” provided by the combination of the output capacitor and ESR (Z_{ESR}). Being either below or above this range of ESR values leads to instability. An ESR to the left of this range creates instability because a low zero frequency pushes the unity gain frequency far to the right, meaning that the phase margin will have dropped below 0° before the unity gain frequency. An ESR to the right of this range creates because it leaves the decrease in phase shift caused by the poles uncompensated until a higher frequency, meaning again that the phase shift will drop below 0° before the unity gain frequency.



'074 Patent Figure 1(b) ESR value too high with zero shift annotated
Prior Art

3. Gain-Bandwidth Tradeoff

48. A common figure used to describe amplifiers is the gain-bandwidth product. For amplifiers that are dominated by a single pole the product of the amplifier gain and its bandwidth is approximately constant as feedback is used to change the bandwidth of the amplifier. This characteristic means that the most common tradeoff when designing an amplifier circuit (including feedback) is between gain and bandwidth—increasing one invariably means compromising on the other.

49. For example, in the figure below the unity-gain bandwidth is 100 MHz. That is, the gain drops to 1 (unity-gain), at a frequency of 100 MHz. The raw amplifier (the amplifier without any feedback loop, also known as “open loop”) has a gain at low frequency of 1 million and a pole at (bandwidth of) 100 Hz. If feedback is added (“closed loop”) to decrease the gain to 100, the bandwidth (the frequency at which the gain has dropped 3 dB below its DC value) would consequently rise to 1 MHz. If the gain were decreased to 10, the bandwidth would increase to 10 MHz, etc. In all cases the product of the gain and the bandwidth is the same: 100 MHz. Note that this use of feedback can only decrease the gain of the raw amplifier, trading reduced gain for increased bandwidth. Increasing both gain and bandwidth requires increasing the gain-bandwidth of the amplifier – replacing it with a different amplifier at significant cost in area and power. This sliding scale tradeoff between gain and bandwidth would have been well-understood by POSITAs as of the priority date. (Analysis and Design of Analog Integrated Circuits, Fourth Edition, Gray, Hurst, Lewis, Meyer, John Wiley & Sons, 2001, section 9.2.)

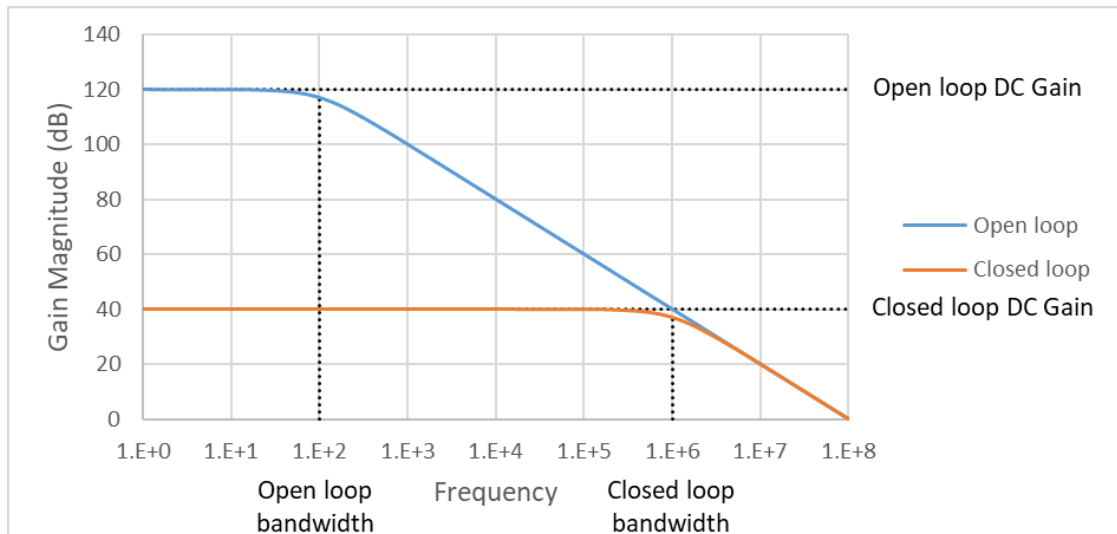


Figure 6. Gain magnitude versus frequency for basic amplifier and feedback amplifier
Adapted from Analysis and Design of Analog Integrated Circuits Figure 9.2

VI. Disputed Claim Terms

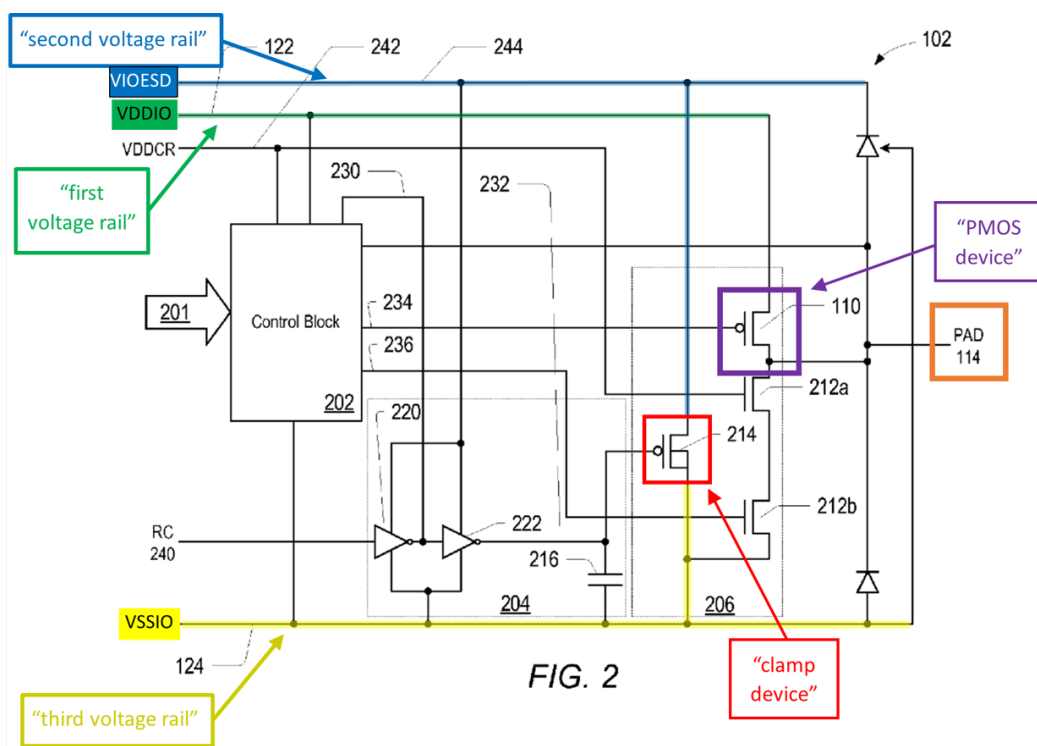
A. Term 1 – “second voltage rail” (’665 Patent, claim 1)

No.	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
1	Plain and Ordinary Meaning Alternatively, “a second voltage rail that is distinct from the third voltage rail but may or may not be distinct from the first voltage rail”	“a second voltage rail that is distinct from the first voltage rail”

50. The structure referenced in this claim is shown in Figure 2 of the ’665 patent. The “first voltage rail” is VDDIO 122, the “second voltage rail” is VIOESD 244, and the “third voltage rail” is VSSIO 124.

51. Specifically, claim 1 confirms that the “first voltage rail” is VDDIO where it specifies that the claimed PMOS device (annotated in purple below) sits between the “first node coupled to a first voltage rail” (annotated in green) and the “second node coupled to a physical pad

having capacitance” (annotated in orange). ’074 patent, claim 1. This is consistent with the specification’s description of Figure 2: “**PMOS device 110** . . . [is] coupled between **VDDIO rail 122** and **PAD 114**.” (’665 patent, 4:33-35.) Likewise, claim 1 requires that the control block “turn[s] on the . . . one or more output transistor devices [PMOS devices]” thereby connecting the pad to the first voltage rail so it may share the charge. Again, this is consistent with the specifications description: during an ESD event, the “**PMOS devices** turn[] on . . . resulting in the charge being shared across all **pads**” via the VDDIO rail. (’665 patent, 4:13-19, 5:29-35.)



52. In addition, claim 1 and the specification confirm that the “second voltage rail” refers to VIOESD in Figure 2. Specifically, claim 1 requires “a **clamp device** configured between a **second voltage rail** and a **third voltage rail**.” The specification confirms, as illustrated in annotated Figure 2 above, that the clamp 214 is situated between VIOESD (the “second” voltage

rail) and VSSIO (the “third” voltage rail). Namely, Figure 2 includes a “**clamp device 214** configured to shunt **VIOESD rail 244** and **VSSIO rail 124**.” (’665 patent, 5:13-17.)

53. The specification also explains that VIOESD and VDDIO may be the same power rail: “It should also be noted that **VIOESD 244** and **VDDIO 122** may in fact be the same power/supply rail, and alternate embodiments may be configured with a single power rail providing power to the circuit and/or system components that are powered by **VIOESD 244** and **VDDIO 122** in the embodiment shown in FIG. 2. In general, the ESD rail and the power supply rail can be the same supply rail, and separate supply rails (e.g. **VIOESD 244** and a distinct **VDDIO 122**) may not be required.” (’665 patent, 5:57-65.) Indeed, a POSITA would have education and/or experience working with systems with one, two, or more supply rails.

54. Note that VSSIO 124 (the “third voltage rail” in claim 1 of the ’665 patent) must be distinct from the other two rails. That is because it provides the negative supply to the output driver. If there were only one power rail for the output driver, then it would be able to drive only that one voltage out of the chip and thus would be unable to move any data off of the chip. Furthermore, if both ends of the clamp 214 in ’665 Figure 2 were tied to the same supply rail then the clamp would serve no purpose. Clamping a supply to itself is redundant.

55. In my opinion and for the above reasons, a POSITA would have understood “second voltage rail,” in the context of these claims, to have its plain and ordinary meaning. In particular, a POSITA would have understood that the claimed “second” voltage rail must be distinct from the “third” voltage rail but need not be distinct from the “first” voltage rail.

B. Term 2 – “an enable/disable function to enable/disable the biasing circuit for reducing standby current” (’074 Patent, claim 1)

No.	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
2	Not subject to 35 U.S.C. 112 ¶ 6. To the extent the court determines that § 112 ¶ 6 applies: Function: to enable/disable the biasing circuit for reducing standby current Structure: enable/disable signal input line (Node M)	Indefinite; Subject to 35 U.S.C. § 112 ¶ 6 without any corresponding structure

56. In my opinion, a POSITA would have understood the term “an enable/disable function to enable/disable the biasing circuit for reducing standby current” to refer to a structural input to the biasing circuit structure and not merely a functional result.

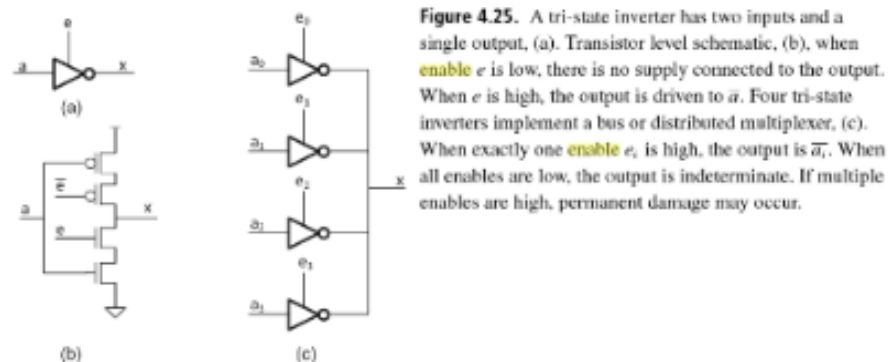
57. In particular, a POSITA would have understood the term refers to an input for turning one or more transistors on or off like a switch to enable or disable the flow of current. A POSITA would have recognized that there are only a limited number of ways for enabling/disabling the flow of current in a circuit and that by far the most common way is to turn on or off the transistor itself through which current is flowing. This is a fundamental technique that is used in all types of applications, such as disabling current in a smartphone circuit or disabling the coils in a room heater when a given temperature is reached.

58. Moreover, because engineers routinely use an input to a circuit to enable or disable it, they often use the term “enable” as the name of that structural input. For example, a review of datasheets for a number of commercially available voltage regulators confirms that “ENABLE” is a common description for a physical input line. Ex. 1 (<https://www.ti.com/lit/gpn/tps7a20>); Ex. 2 (<https://www.analog.com/media/en/technical-documentation/data-sheets/max25302a-max25302b.pdf>); Ex. 3 (<https://www.st.com/resource/en/datasheet/ld39200.pdf>);

Ex. 4 (<https://www.diodes.com/assets/Datasheets/AP7331.pdf>). Similarly, a 2012 textbook on digital circuit design describes a circuit with three physical input lines, one of which is called “enable e ” and is used for turning on or off the circuit: “When the enable e is high ($\bar{e}$ is low), the middle two transistors are on.” Ex. 5 (Digital Design, A Systems Approach, William J. Dally & R. Curtis Harting, Cambridge University Press, 2012, section 4.3.4., Figure 4.25))

4.3 CMOS gate circuits

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59. Thus, a POSITA would have understood the claimed “enable/disable function to enable/disable the biasing circuit for reducing standby current” to refer to a particular structure, or class of structures, commonly used for enabling and disabling circuit elements, as exemplified in the exhibits above.

60. It is not surprising that circuit designers use the term “enable” to refer to this structure, because many (if not most) circuit blocks and inputs are named according to their functions. This is so engineers can quickly comprehend what the block does and how to use it. Among other examples, pins that control timing are “CLOCK”, “CLK”, or “CK”; pins that initialize a part are “RESET”; power supplies that deliver a constant voltage start with “V” followed by an indicator of the type of voltage (“VSS” for the source/low voltage, “VDD” for the

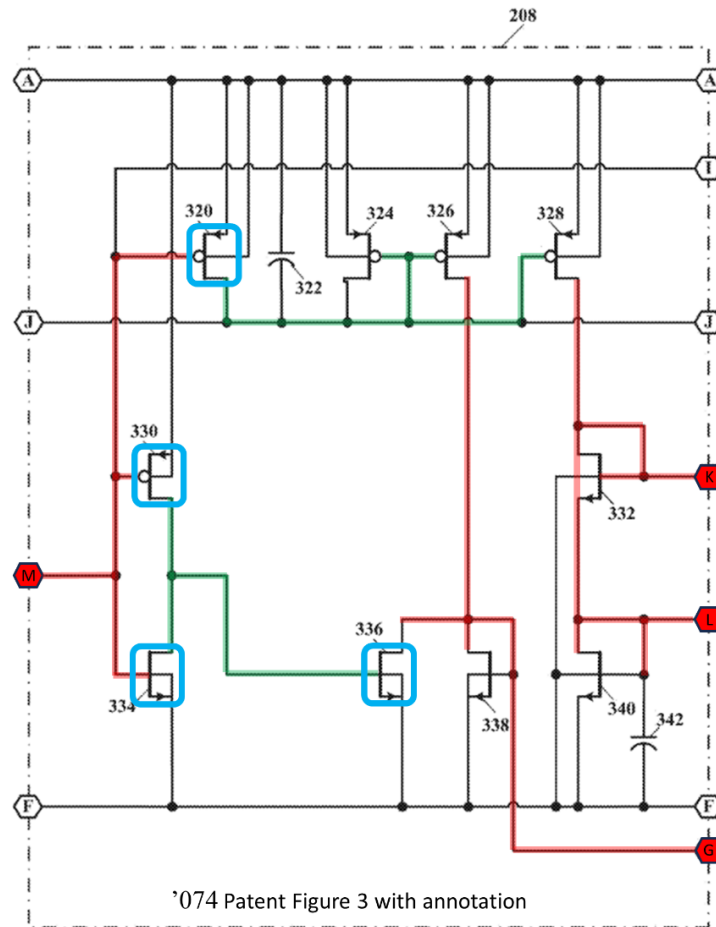
drain/high voltage, “VBIAS”, “VREF”, ...); and enables are “ENABLE”, “ENABLE/DISABLE,” “OUTPUT ENABLE”, or “CLOCK ENABLE”.

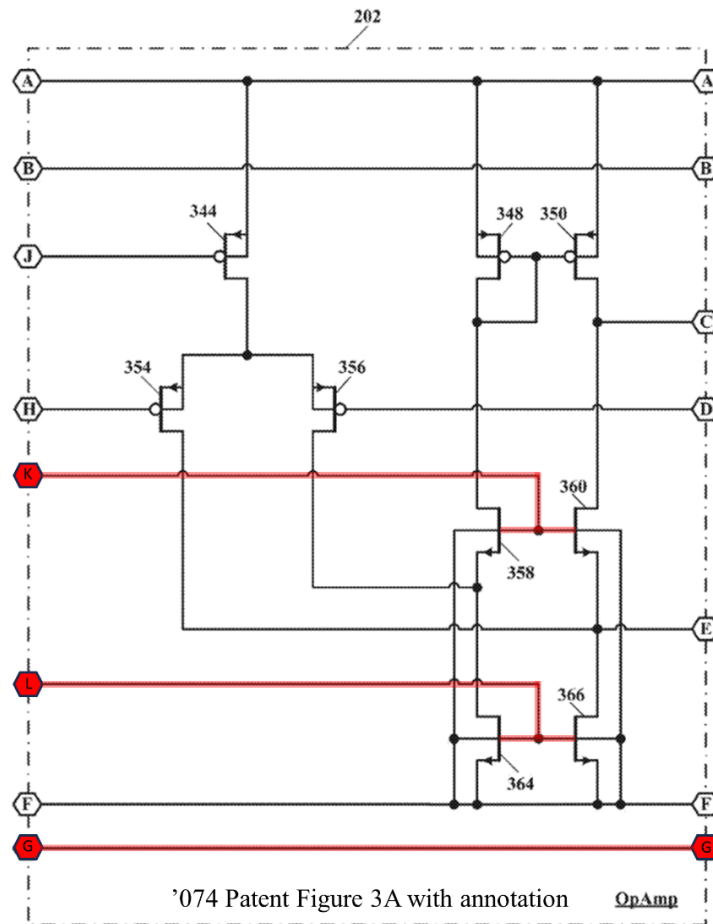
61. I note that the labels “ENABLE” and “ENABLE/DISABLE” are interchangeable, and refer to the same structure. “Enable” is simply shorthand in which the “disable” is implied, because if an “enable” must either be on (i.e., enabling transistors) or off (i.e., disabling transistors).

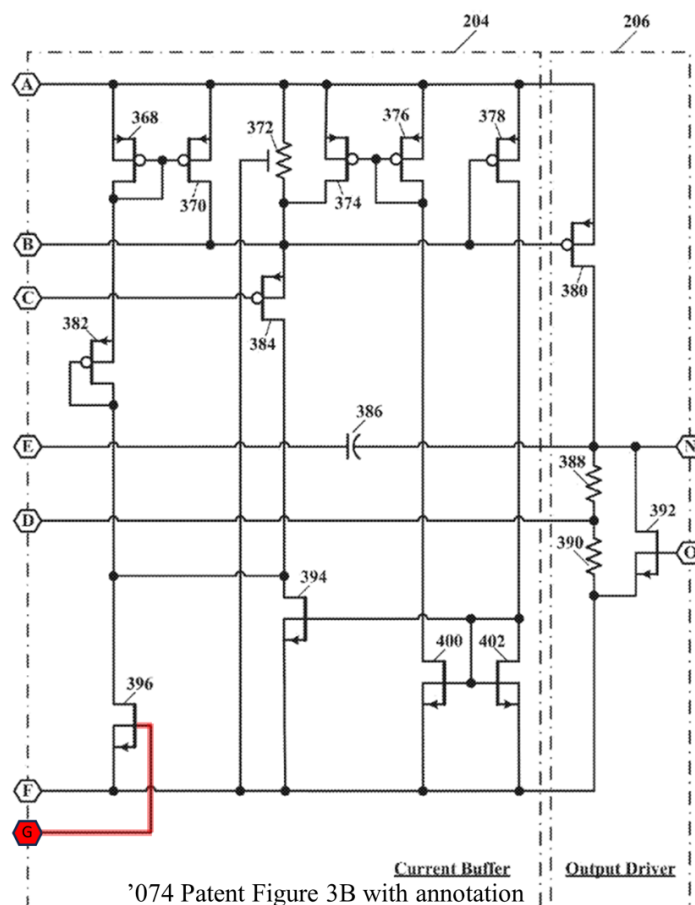
62. I understand that—because a POSITA would have understood the term “an enable/disable function to enable/disable the biasing circuit for reducing standby current” to refer to structure, and not function—so-called “mean plus function” rules do not apply. However, to the extent that the Court applies means plus function rules, in my opinion, the claimed function would be “to enable/disable the biasing circuit for reducing standby current” and the corresponding structure disclosed in the specification is the enable/disable signal input line (Node M) shown in ’074 Figure 3 and described in the specification at 4:43-46.

63. Specifically, the specification explains, in the context of ’074 Figure 3’s biasing circuit, that “[t]ransistors 320, 330, 334 and 336 may be shut off during disabling/power down operation to make sure this circuit will consume substantially no DC current. . . . **Node M is the enable signal coming to the regulator circuit so that the module can be turned off when disabled.**” (’074 patent, 4:44-54.) That is, Node M can force node J high through PMOS 320, which turns off PMOS 328. PMOS 328 provides the current that biases current source references K and L, which are shut off when this bias current is eliminated. They in turn shut off current bias NMOS devices 358, 360, 364, and 366 within the rest of OpAmp 202 thereby eliminating the power drawn by both the bias circuits in Figure 3 of the ’074 patent as well as the OpAmp power in Figure 3A of the same patent. At the same time, M can turn on NMOS 336, which pulls node G

low, shutting off bias NMOS 396 in Figure 3B, eliminating the power drawn by Current Buffer Driver 204. This is illustrated in the following 3 figures where the nodes that are **low** when node M is low are highlighted in **red** and the nodes that are **high** when node M is low are highlighted in **green**.







C. Term 4 – “wherein the gm-boost circuit enables the current buffer driver to have large gm value” ('074 Patent, claim 4)

No.	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
4	Not indefinite. Plain and Ordinary Meaning Alternatively, “wherein the gm-boost circuit increases the gm value of the current buffer driver”	Indefinite

64. In my opinion, a POSITA would have understood the term “wherein the gm-boost circuit enables the current buffer driver to have a large gm value” with reasonable certainty. In particular, the specification provides objective guidance to a POSITA to understand the scope of the claim in the context of this invention.

65. As an initial matter, I note that Aptiv does not contend that a POSITA would not have understood the concept of gm-boosting a circuit as described in the '074 patent. Rather, Aptiv appears to assert that the word “large” makes the term indefinite. But this ignores the context in which “large gm value” is used in the '074 patent specification. According to the '074 specification, “[t]he key to being able to use smaller value internal and external capacitances is to have *a large gm current driver buffer* amplifier 204 between the first stage Op Amp 202 and the last stage power output driver 206. ('074 patent, 3:58-62.) The specification further explains that “various values of ESR may be handled by separating the poles inside of the voltage regulator circuit sufficiently to create an approximate one pole system.” ('074 patent, 3:50-53.) Thus, a POSITA would have understood *why* the circuitry of the '074 patent includes a gm-boost circuit.

66. As described above, a “pole” here represents a complex frequency at which the transfer function of the circuitry goes to infinity. While a system with a single well-behaved pole is stable, adding additional poles for gain, bandwidth, or compensation purposes can lead to instability. Roughly speaking, additional poles are undesirable because they undermine stability and, when customer-selected components are part of the feedback loop, the usability of a circuit.

67. The specification explains further that “[t]he implementation of the OpAmp 202 as a folded cascode configuration is due to its unique architecture which results in a single pole at the output that minimizes the complexity of its compensation. The current buffer driver 204 acts like a low impedance driver which connects between the OpAmp 202 and the output driver 206. Since the output driver 206 may provide very large amounts of switching current during power supply operation, the gate capacitance is significantly high due to the size of the driver, thereby resulting in the generation of a pole at relatively low frequency. Thus, the current buffer driver 204 pushes this pole to a high frequency beyond unity-gain frequency due to its low-impedance characteristics

in order to get the pole splitting effect.” (’074 patent at 4:1-14.) In this context, “pole splitting” and “compensation” refer to techniques for shifting the locations of the non-dominant poles so that there will be only one (dominant) pole present within the operating frequency range of interest.

68. As a POSITA would have understood, this pole splitting could be accomplished by increasing the transconductance (gm) of the current buffer driver. As just described, gm-boosting is used as part of the pole-splitting compensation technique—which is used to clear non-dominant poles out of the frequency range of operation of the op amp circuit(s) of the ’074 patent. A POSITA would therefore understand that the word “large” in the “large gm value” claim term simply refers to boosting gm to a value at-or-beyond which the “second-most-dominant pole” will be pushed close to or beyond the unity-gain frequency and the impact of the pole is pushed above-and-beyond the unity-gain frequency.

69. Finally, a POSITA would have understood that the requisite gm is a context-dependent value. Some variables that would affect the necessary gm in a given scenario include, but are not limited to, the output voltage being delivered by the regulator, the amount of power the regulator is delivering, the power supply’s precision, the voltage regulator’s response time, the characteristics (including ESR) of the external bypass capacitor, and the manufacturing process used to fabricate the regulator circuit. But although the necessary gm varies by application and context, a POSITA would have understood based on the ’074 patent and their general background knowledge, how to calculate a gm sufficiently large in any given scenario to push the second most dominant pole above and beyond the unity gain frequency.

D. Term 5 – “low gain and high bandwidth amplifier” (’074 Patent, claim 8)

No.	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
5	Not Indefinite. Plain and Ordinary Meaning Alternatively, “amplifier optimized for high bandwidth with a commensurate reduction of gain”	Indefinite

70. In my opinion, a POSITA would have understood with reasonable certainty the term “low gain and high bandwidth amplifier” as having its plain and ordinary meaning. In particular, the specification provides objective guidance to a POSITA to understand the scope of the claim in the context of this invention.

71. As an initial matter, and as discussed above in my Technology Background, a POSITA would have been aware of the sliding scale tradeoff between gain and bandwidth in an amplifier and thus would have understood how a low gain / high bandwidth amplifier differs from a “traditional” high gain / low bandwidth amplifier. Since the mathematical product of gain and bandwidth is approximately constant, a POSITA would have understood that increasing bandwidth is the inherent result of reducing the low frequency gain of the amplifier. Put another way, a POSITA would have understood that a “low gain and high bandwidth amplifier” simply refers to an amplifier positioned at the other end of the gain/bandwidth scale from a traditional OpAmp.

72. Further, the specification explains that it achieves the object of the invention using, among other things, a “low-gain, high bandwidth amplifier” designed such that “(1) The architecture forms only one pole at the output of the folded stage which reduces the complexity of frequency compensation, [and] (2) it provides a good driving capability for the source follower stage of the current buffer.” (’074 patent, 4:24-42). Thus, a POSITA would have understood the

patent as teaching the goal of balancing sufficient bandwidth such that the amplifier forms only a single pole while still offering sufficient gain to drive the current buffer.

73. As explained below, and confirmed by the '074 specification and diagrams, a POSITA would have understood that this increase in bandwidth (and commensurate reduction in gain) could be achieved with a simple feedback loop, or by modifying an existing loop. As can be seen in Figure 6 (repeated below) extending the bandwidth of an amplifier (within the bounds of its gain-bandwidth product) is accomplished by “throwing away” the unneeded low frequency gain.

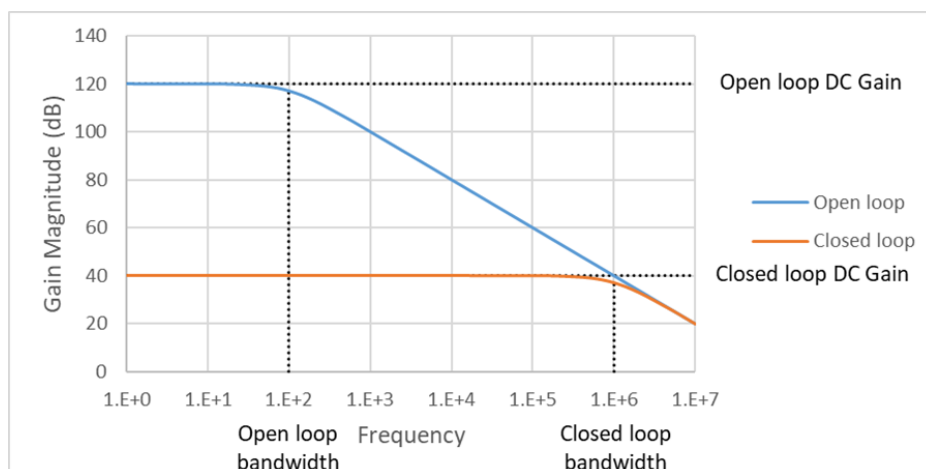


Figure 6. Gain magnitude versus frequency for basic amplifier and feedback amplifier
Adapted from Analysis and Design of Analog Integrated Circuits Figure 9.2

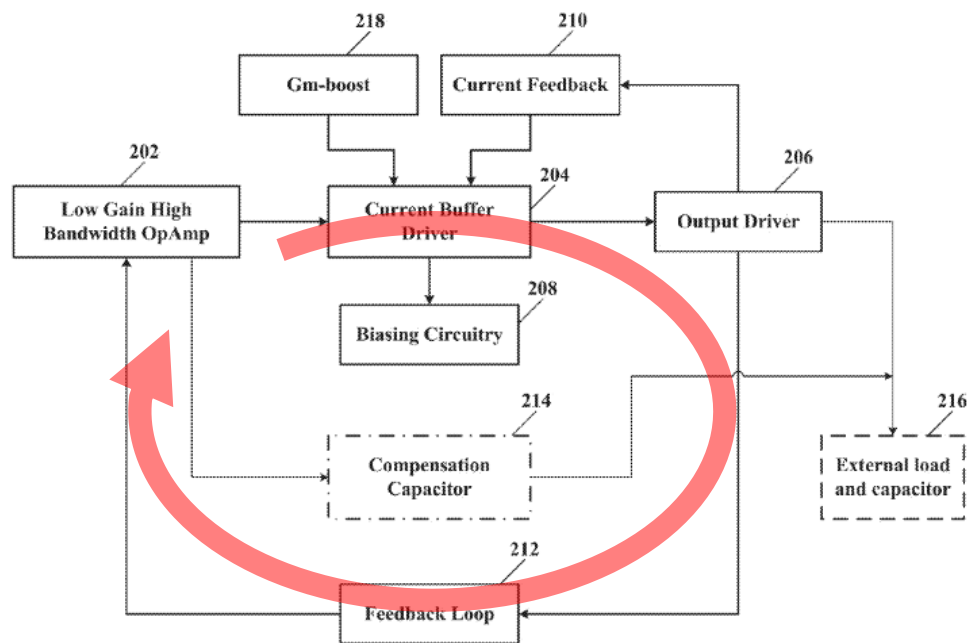
74. Figure 2 from the '074 patent shows the top-level diagram of the regulator circuit and confirms how the invention can use feedback to effect a low-gain, high-bandwidth amplifier. In particular, the pictured circuit includes multiple amplifiers and multiple loops. As pointed out in the specification:

Since the output driver 206 may provide very large amounts of switching current during power supply operation, the gate

capacitance is significantly high due to the size of the driver, thereby resulting in the generation of **a pole at relatively low frequency**.

(’074 patent 4:6-11.)

75. A POSITA would have understood that feedback loop 212 operates from Output Driver 206 to Low Gain High Bandwidth OpAmp 202 as annotated in Figure 2 from the ’074 patent below, and includes Current feedback 210, Compensation Capacitor 214, and the effects of External load and capacitor 216, the ESR of which contributes a zero to the system. Because this loop encompasses these other poles and zeroes, they will all interact with one another to create the poles and zeroes of the overall circuit’s transfer function, as was the case for the Bode plots shown in Figures 1 and 1A in the ’074 patent.



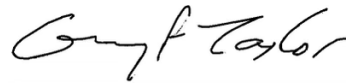
’074 Patent Figure 2 – with annotation

76. As the ’074 patent further explains, the voltage regulator should be designed so it “acts like a pseudo ‘one-pole’ system that is independent from the output pole changing so long as it falls within the bandwidth of the system” (’074 patent, 5:43-45) and a POSITA would have understood this pole-splitting results in a more stable system dominated by a single low frequency

pole. Raising the gain of Low Gain High Bandwidth OpAmp 202 would increase the overall gain of the top-level system, which would push out the unity-gain frequency and reduce the dominance of the compensated pole at the output of OpAmp 202. Given these constraints that this amplifier must meet if the overall system is to be dominated by the pole of this OpAmp while the overall system is also an effective regulator, a POSITA would have readily understood the claims' use of a "low gain and high bandwidth amplifier."

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct, and that all statements reflect my opinions based upon my knowledge and experience.

Date: March 1, 2024

A handwritten signature in black ink, appearing to read "Gregory F. Taylor". The signature is written in a cursive, flowing style.

Gregory F. Taylor

Appendix A

Gregory F. Taylor

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Experience

- 2016- **Greg Taylor Consulting, Inc.**, Portland OR
Principal. Technical consulting on electronic product and integrated circuit development with a variety of clients, as well as patent expert witness work.
- 2016-2020 **zGlue Corporation**, Hillsboro OR
zGlue Fellow. Consulted on new product planning; integrated circuit design, specification, validation, testing, and manufacturing; represented zGlue at opencompute.org's Open Domain Specific Architecture (ODSA) working group.
- 2014-2016 **Intel Corporation**, Platform Engineering Group, Hillsboro OR
Intel Fellow, Hard IP Group Chief Architect. Leading the worldwide circuit architecture teams for I/O, analog, and linear supply regulator design.
- 2008-2015 **Intel Fellow, Analog Review Committee lead.** Led an internal team driving the development of 22, 14, and 10 nm analog/mixed signal circuits across all product lines using Intel process technologies. Drove consistency and sharing of these IPs across most of the business units at Intel.
- 2013 **Intel Corporation**, Intel Labs, Hillsboro OR
Intel Fellow, Director of the Low Power Mixed Signal Lab. Started a new lab to develop analog/mixed signal circuits and design methods that will enable lower power computing and communication platforms.
- 2011-2013 **Intel Fellow, Director of the SoC Design Lab.** Led a multinational team to develop prototype Systems on Chip, including work to improve time to market and energy efficiency through improvements to chip design.
- 2008-2011 **Intel Fellow, Director of the Circuit Research Lab.** Led a team developing circuits and microarchitectures that will lead to lower power and higher performance computing platforms.
- 2004-2008 **Intel Corporation**, Logic Technology Development, Hillsboro OR
Intel Fellow, Director of Mixed Signal Circuit Technology. Led a cross organizational team coordinating the 45 nm and 32 nm collateral delivery between process technology development and multiple design projects. Technical lead for the team that developed I/O, clock generation, temperature sensing, and other analog circuits for use across all Intel microprocessors developed on 65 nm, 45 nm, and 32 nm manufacturing technologies, including the first commercial high-k metal gate based product. Started analog circuit development for what became the first commercial FinFET manufacturing process.
- 2002-2004 **Intel Fellow, Director of Mixed Signal Circuit Technology.** Managed the team responsible for the design of clock generation, clock distribution, I/O circuitry, package, power distribution and other mixed signal circuits for a pair of 90 and 65 nm Pentium® 4 processors, including the first commercial strained silicon based product.
- 1993-2002 **Principal Engineer/Component Design Manager.** Managed the team responsible for the design of clock generation, clock distribution, I/O circuitry, package, power distribution and other mixed signal circuits for Pentium, Pentium II, and Pentium III microprocessors in 0.35 through 0.13 μm technologies.
- 1991-1993 **Staff Design Engineer.** Designed a CMOS/ECL cache for the Pentium Microprocessor, Intel's first BiCMOS product, in 0.8 μm and 0.6 μm

technologies. Developed an Electrical Rules Checker to ensure the correctness of signaling between different frequency clock domains.

Bipolar Integrated Technology, Beaverton OR

- 1988-1991 **Principal Design Engineer.** Participated in all phases of the design of a second generation floating point chip. Made customer visits to determine product requirements; developed the architecture, test and validation plans; and designed the multiplier circuit. Developed an ECL Electrical Rules Checker and formal verification tool and supervised the package design. Consulted in the design, validation, and debug of Sparc® and MIPS® ECL microprocessors.
- 1986-1988 **Circuit Design Engineer.** Designed Emitter Coupled Logic floating point integrated circuits. Generated test suite and validated correctness of overall design. Developed a switch level simulator to verify the logical correctness of ECL gates. Completed debug and sustaining engineering.

Education

- 1983-1985 D.Eng. Computer and Systems Engineering, Rensselaer Polytechnic Institute (RPI), Troy, NY. Thesis topic: An Architecture for a Wafer Scale Integration Two Dimensional Fast Fourier Transform Processor.
- 1981-1983 MSEE Computer and Systems Engineering, RPI, Troy NY. Thesis topic: An ECL Floating Point Processor.
- 1977-1981 BSEE Computer and Systems Engineering, RPI, Troy, NY.

Other

- IEEE Fellow, 2009 to present.
- Fannie and John Hertz Foundation Fellowship, recipient, 1981 to 1985.
- VLSI Circuit Symposium Technical Committee, member, 1999 to 2006.
- Published more than 60 peer reviewed papers, 67 issued US patents.

Publications

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- "Designing Software Configurable Chips and SIPs using Chiplets and zGlue", Jawad Nasrullah, Zhiquan Luo, Greg Taylor, International Symposium on Microelectronics, September 2019.
- "High Capacity on-Package Physical Link Considerations", Greg Taylor, Ramin Farjadrad, Bapiraju Vinnakota, Hot Interconnects Conference, August 2019.
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