

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

MICROCHIP TECHNOLOGY INC.,

Plaintiff,

v.

APTIV SERVICES US, LLC,

Defendant.

C.A. No. 1:23-CV-00778-JDW

JURY TRIAL DEMANDED

**PLAINTIFF MICROCHIP TECHNOLOGY INC.'S
REPLY CLAIM CONSTRUCTION BRIEF**

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I. THE '665 PATENT

A. Term 1: “second voltage rail”

No.	Claim Term	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
1	“second voltage rail” '665 patent, claim 1	Plain and Ordinary Meaning Alternatively, “a second voltage rail that is distinct from the third voltage rail but may or may not be distinct from the first voltage rail”	“a second voltage rail that is distinct from the first voltage rail”

Aptiv’s argument rests on the false premise that the patentee chose to limit claim 1 to a dual power rail embodiment and that Microchip now seeks to override that choice by expanding the claim to encompass a single power rail embodiment.¹ But this is not a dispute over whether every claim must encompass every embodiment regardless of its language; the parties agree that is not the law. Rather, this is a dispute over whether the applicant imposed such a limitation at all. Because the claims are agnostic as to whether the first and second voltage rails must be physically distinct, Aptiv’s construction would inappropriately narrow the scope of this claim. *Home Diagnostics, Inc. v. LifeScan, Inc.*, 381 F.3d 1352, 1358 (Fed. Cir. 2004) (“Absent a clear disavowal or contrary definition in the specification or the prosecution history, the patentee is entitled to the full scope of its claim language.”).

If the patentee wanted to require separate first and second voltage rails, it could have done so expressly. Indeed, the patentee used claim language to distinguish the first voltage rail from the third voltage rail (“the third voltage rail *has a value below* the first voltage rail”), and the second voltage rail from the third voltage rail (“a clamp device configured *between* a second voltage rail and a third voltage rail”). ('665 patent, 6:51-52, 6:42-43.) But there is no claim

¹ In addition to one or two power rails, each configuration *additionally* includes a ground rail (i.e., the “third” rail).

language requiring physically distinct first and second voltage rails. The patentee’s choice not to include such a limitation here is particularly telling given the specification’s guidance that “[i]n general, the ESD rail and the power supply rail can be the same supply rail, and separate supply rails (e.g. VIOESD 244 and a distinct VDDIO 122) may not be required.” (’665 patent, 5:62-65.)

In this context, the best reading of the claims is that the words “first” and “second” are *labels* for components, *not quantitative requirements*. The claim language imposes no functional restrictions or relationships precluding the first and second voltage rails from being the same rail. (Taylor Reply ¶¶ 8-9.) The first and second voltage rails are not defined *relative to one another*. Accordingly, there is no logical contradiction with the two elements being met by the same voltage rail.

This case is distinct from those cited by Aptiv, which involved claim limitations that made it *illogical* for one structure to satisfy two limitations. For instance, in *Gillette*, the claimed “second blade [was] defined solely by its elevation and location between the [first] and [third] blades.” *Gillette Co. v. Energizer Holdings, Inc.*, 405 F.3d 1367, 1373 (Fed. Cir. 2005). Thus, the second and first blade could not logically be the same blade. Likewise, in *Acera*, the claims required that the “the second layer *is combined* with the first layer ... suggest[ing] that the first layer must be distinct in the sense that it was formed separately, independent from the second layer.” *Acera Surgical, Inc. v. Nanofiber Sols. LLC*, No. 20-980-CFC-JLH, 2022 WL 6948855, at *6 (D. Del. Oct. 12, 2022) (internal quotation marks omitted; emphasis in original). By contrast, the claim language here imposes no such relationship between the first and second voltage rails, and the claim should therefore be given its full scope.

Indeed, where one structure can logically satisfy the functional requirements of claimed “first” and “second” elements, courts consistently hold that elements need not be distinct. For

instance, in *Linear Tech. Corp. v. Int’l Trade Comm’n*, the Federal Circuit affirmed that “there is nothing in the claim language or specification that supports narrowly construing the terms to require a specific structural requirement or entirely distinct ‘second’ and ‘third’ circuits. Rather, the ‘second’ and ‘third’ ***circuits must only perform their stated functions.***” 566 F.3d 1049, 1055 (Fed. Cir. 2009) (emphasis added). Similarly here, because the first and second voltage rails can perform their functions whether they are two structures or one, the claim should be interpreted to encompass both options. Aptiv’s only argument to the contrary is that in *Linear Tech.* the Federal Circuit looked at whether there could be overlap between the disputed elements rather than whether they could be satisfied by the “same exact circuit.” (Opp. 5.) But that was because the Federal Circuit in *Linear Tech.* was following the specification’s guidance that “the ‘second circuit’ and ‘third circuit’ can ***share common components.***” 566 F.3d at 1055 (emphasis added). By contrast, here the specification expressly instructs that the claimed rails “***can be the same supply rail.***” (’665 patent, 5:62-65 (emphasis added).)

Likewise, Aptiv cannot reconcile its position that “first” and “second” necessarily mean distinct and separate elements with *Square D C. v. E.I. Elecs., Inc.*’s holding that “the first power supply and the second power supply ***need not be independent.***” 685 F. Supp. 2d 864, 875-76 (N.D. Ill. 2010) (emphasis added). Aptiv argues that *Square* is distinguishable because the specification there disclosed only a single power supply. (Opp. 5.) But this proves Microchip’s point. Despite the use of “first” and “second” in the claims, there was no presumption that the two elements were separate; in fact, the Court found that “the claim language is clear and unambiguous, and nothing in the claims or the specification ***limits*** this second source of power as EI seeks to limit it.” *Square*, 685 F. Supp. 2d at 875 (emphasis added). Here too, nothing in the claims or specification limits the “second voltage rail” from being the same as the “first voltage rail.”

Aptiv’s final argument is that “there are technical reasons why a POSITA might elect a circuit with separate VDDIO and VIOESD rails.” (Opp. 6.) That is entirely beside the point. The comparative technical benefits of one- and two-rail systems do not indicate one way or another whether *this claim language* encompasses both. (Taylor Reply ¶¶ 8-9.) If anything, the fact that both configurations are useful suggests that the patentee likely intended its claims to cover both.

In short, the Federal Circuit “has cautioned against interpreting a claim term in a way that excludes disclosed embodiments, when that term has multiple ordinary meanings consistent with the intrinsic record.” *Helmsderfer v. Bobrick Washroom Equip., Inc.*, 527 F.3d 1379, 1383 (Fed. Cir. 2008). The language of the claims—which can be logically satisfied by a single or dual power rail configuration—suggests that the patentee was, at most, agnostic on this point. That is consistent with the intrinsic record, which confirms that one rail can serve in place of two. And where, as here, the claims do not contain restrictions to the contrary, the case law uniformly supports a non-restrictive interpretation of ordinal numbering. Accordingly, the Court should afford this term its full scope.

II. THE '074 PATENT

A. Term 3: “an enable/disable function to enable/disable the biasing circuit for reducing standby current”

No.	Claim Term	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
3	“an enable/disable function to enable/disable the biasing circuit for reducing standby current” '074 patent, claim 1	Not subject to 35 U.S.C. § 112 ¶ 6. To the extent the court determines that § 112 ¶ 6 applies: Function: to enable/disable the biasing circuit for reducing standby current Structure: enable/disable signal input line (Node M)	Indefinite; Subject to 35 U.S.C. § 112 ¶ 6 without any corresponding structure

The claimed “enable/disable function to enable/disable the biasing circuit for reducing standby current” refers to a fundamental principle of circuit design: applying an enable/disable signal to enable the flow of current through transistors (allowing a device to function) or to disable the flow of current through transistors (turning the device off to save power). Aptiv—which bears the burden to prove indefiniteness—offers no affirmative evidence to the contrary, and now admits that Microchip’s evidence shows consistent use of “enable” terminology in the art. Aptiv’s few arguments in support of its indefiniteness position twist the claim language, mischaracterize the knowledge of a POSITA, and ultimately fail.

1. Aptiv’s Admissions Confirm That It Cannot Overcome the Presumption Against Means-Plus-Function Claiming

Because this term does not use the word “means,” it is presumptively *not* a means-plus-function term. *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1348-49 (Fed. Cir. 2015) (en banc). Aptiv offers no affirmative evidence to overcome this presumption and argues only that Microchip’s evidence fails to establish uniform usage of this term in the art. That does not begin to overcome the presumption against means-plus-function claiming. *See PACT XPP Schweiz AG*

v. Intel Corp., No. 1:19-cv-01006-JDW, 2020 WL 5821723, at *6 (D. Del. Sept. 30, 2020) (where “the wide use of the term in the literature indicates that a person skilled in the art would have understood it at the time,” Defendant expert’s mere criticism of those sources is insufficient to overcome the presumption that § 112 ¶ 6 does not apply). Moreover, in attempting to distinguish Microchip’s extrinsic evidence (*i.e.*, Taylor Exs. 1-5), Aptiv and Dr. Shanfield effectively admit that this term **does** have a reasonably well understood meaning in the art. As Aptiv explains:

Exhibits 1-4 to the Taylor Declaration are technical documentation for various voltage regulators [*i.e.*, the technology claimed in the ’074 patent]. These exhibits use one or more of the terms “enable,” “enable pin,” “enable input,” “EN,” or “EN pin” to refer solely to a **physical pin and/or wire** through which a signal may be sent to some logic circuit on the regulator that acts ***to turn circuitry on or off*** based on the voltage of the signal.

(Opp. 9-10 (emphasis added for italics; emphasis in original for underlines) (citing Shanfield ¶ 60).) This is consistent with Microchip’s position that:

a POSITA would have understood that an “enable/disable function ... for reducing standby current” refers to an ***input for turning on or off the transistors that draw current***, *i.e.*, a switch.

(Br. 14 (emphasis added) (citing Taylor ¶ 57).) Thus, the parties agree that the word “enable” signifies structure—physical wiring that controls transistors—for turning circuitry on or off.² (*See also* Taylor Reply ¶ 11.) This alone defeats Aptiv’s argument that the presumption against means-plus-function claiming does not apply. *Williamson*, 792 F.3d at 1348 (noting that the “essentially inquiry” is “whether the words of the claim are understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the name for structure”) (citing *Greenberg v. Ethicon Endo-Surgery, Inc.*, 91 F.3d 1580, 1583 (Fed. Cir. 1996) (“What is important is ... that the term, as the name for structure, has a reasonably well understood meaning in the art.”)).

² As Aptiv itself argued in the related case, “‘circuit’ itself connotes structure to a POSITA.” (C.A. No. 1:23-CV-00307-JDW, Dkt. 158, 49.)

Aptiv offers only three arguments to the contrary. All fail. **First**, Aptiv argues that *one* of Microchip’s five pieces of extrinsic evidence—Taylor Ex. 5—“uses the letter ‘e’ and the phrases ‘enable signal’ and ‘enable signal e’ to refer to various voltage *signals*” rather than *physical circuitry*. (Opp. 10 (emphasis in original).) But directly to the left of the relevant description, Taylor Ex. 5 shows “e” being applied to *physical enable/disable signal input lines* controlling transistors to enable or disable the flow of current through the circuitry. (Taylor ¶ 58.)

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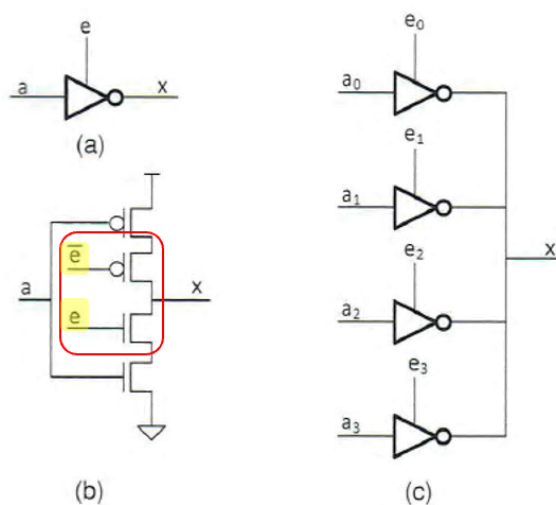


Figure 4.25. A tri-state inverter has two inputs and a single output, (a). Transistor level schematic, (b), when enable e is low, there is no supply connected to the output. When e is high, the output is driven to $\bar{a}$. Four tri-state inverters implement a bus or distributed multiplexer, (c). When exactly one enable e_i is high, the output is $\bar{a}_i$. When all enables are low, the output is indeterminate. If multiple enables are high, permanent damage may occur.

(Taylor Ex. 5, 73; Taylor Reply ¶ 12.) There is no inconsistency between Taylor Exs. 1-4 and Taylor Ex. 5; enable signals can be sent over enable/disable signal input lines.

Second, Aptiv complains that Taylor Exhibits 1-5 do not use “the term ‘an enable/disable function to enable/disable the biasing circuit for reducing standby current,’” but instead use “*related* terms” or “*variants* of the disputed term.” (Opp. 8, 10 (emphases in original).) At the outset, Aptiv’s admission that these terms are “related” “variants” confirms that neither it nor Dr. Shanfield had any difficulty recognizing their relationship. And indeed, the law does not impose a formalistic requirement that a term be used *verbatim* in the art to avoid means plus function

claiming. For instance, in *Greenberg*, the Federal Circuit found the term “detent mechanism defining the conjoint rotation of said shafts ...” was not subject to § 112 ¶ 6 because “detent” denotes a structure with a generally understood meaning in the art. *See Greenberg*, 91 F.3d at 1583. Here too, “enable” and “enable function” have a generally understood meaning in the art—as evidenced by Taylor Exhibits 1-5—and that meaning is properly applied to the full term at issue. If anything, the additional language of this claim term—which explains that the enable/disable function serves “to enable/disable the biasing circuit for reducing standby current”—provides additional guidance to direct a POSITA to a known structure in the art.

Third, Aptiv argues that Taylor Exs. 1-5 do not provide an enable/disable function because none “perform the function of ‘enabl[ing]’ a circuit to reduce standby current—all of them relate only to *disabling* some circuit to reduce standby current.” (Opp. 10 (emphasis in original).) That is, Aptiv contends that, whether the enable/disable input is set to on or off, it must turn off the biasing circuitry. This interpretation defies common sense. If the biasing circuitry were always turned off, the regulator would be permanently disabled. Indeed, the claim language makes clear that the enable/disable function serves to “enable/disable the biasing circuit *for reducing standby current*.” (Taylor Reply ¶¶ 10, 15.) That is, turning on the enable/disable input enables the regulator to function normally, and turning off the enable/disable input restricts the flow of current to save power when the regulator is not in use (*i.e.*, disabling the regulator). The specification makes this point even more expressly, explaining that “Node M is the enable signal coming to the regulator circuit *so that the module can be turned off when disabled*.” (’074 patent, 4:52-54 (emphasis added).)

This term is akin to an “ON/OFF switch for turning a light ON/OFF to save electricity when not in use.” (Taylor Reply ¶ 10.) This language plainly means a switch that either turns the

light on (in which case electricity is used) or off (in which case electricity is not used). *Id.* It does not somehow refer to a switch that turns the light off to save electricity regardless of which way it is flipped.

Aptiv’s treatment of Taylor Exhibit 3 makes clear that this confusion is contrived. There, Aptiv agrees “enable function” refers to “circuitry that implements logic *to turn on or off some other circuitry.*” (Opp. 10 (emphasis changed).) The same reasoning applies to this claim term.

2. Even If Means-Plus-Function Claiming Applies, There is Sufficient Corresponding Structure

Even if the Court finds that means-plus-function claiming applies, Aptiv has not met its burden to show by clear and convincing evidence that the specification does not disclose structure to “enable/disable the biasing circuit for reducing standby current.” *Budde v. Harley-Davidson, Inc.*, 250 F.3d 1369, 1376-77 (Fed. Cir. 2001) (“[A] challenge to a claim containing a means-plus-function limitation as lacking structural support requires a finding, by clear and convincing evidence, that the specification lacks disclosure of structure sufficient to be understood by one skilled in the art as being adequate to perform the recited function.”). Aptiv offers only two arguments, both of which fail.

First, Aptiv argues that the enable/disable function requires *enabling* the bias circuit to reduce standby current. This is a rehash of Aptiv’s argument that, whether the enable/disable function is turned on or off, it should stop the flow of current in the biasing circuit. This tortured reading of the claim language should be rejected for the reasons detailed above, in § II.A.1. The specification need not supply corresponding structure for this unclaimed function.

Second, Aptiv argues that the “enable/disable signal input line (Node M)” cannot supply sufficient structure because a “node” is mere wiring incapable of “enabl[ing]/disabl[ing] the biasing circuit.” Aptiv asserts that, to achieve its function, the corresponding structure must

additionally include (a) transistors that Node M controls; and (b) circuitry “for creating and switching on/off the signal carried by Node M.” (Opp. 11-12.)

With respect to the former, Aptiv does not dispute that at least Fig. 3 of the specification discloses transistors controlled by Node M. (Opp. 12.) Accordingly, this does not evince a lack of corresponding structure that would support Aptiv’s indefiniteness position.³

With respect to the latter, no corresponding structure is required, because this is an unclaimed function. The claim language recites only “an enable/disable function to enable/disable the biasing circuit for reducing standby current.” The disclosed structure—*i.e.*, the enable/disable signal input line of Node M, which enables or disables transistors in the biasing circuit—does exactly that. The claim language does not further recite, *e.g.*, the creation of this signal, switching this signal on and off, or logic for evaluating when to apply this signal. (Taylor Reply ¶ 15.) Accordingly, the specification need not supply corresponding structure for these unclaimed functions.

³ Aptiv also hints that, if this term is definite, it requires not only that the input line controls the flow of current through biasing transistors, but that it controls the flow of current through the “*specific arrangement*” of biasing transistors disclosed in Fig. 3. That position is meritless. The relevant “enable/disable” structure disclosed in Fig. 3 is simply an input line controlling the flow of current through biasing transistors. (Taylor Reply ¶ 14.) The “specific arrangement” of transistors is a function not of the “enable/disable function,” but of the exemplary biasing circuitry. (*Id.*) Importing the precise topology of this exemplary biasing circuitry into the construction of the “enable/disable function” would improperly narrow the scope of this term.

B. Term 4: “wherein the gm-boost circuit enables the current buffer driver to have large gm value”

No.	Claim Term	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
4	“wherein the gm-boost circuit enables the current buffer driver to have a large gm value” '074 patent, claim 4	Not indefinite. Plain and Ordinary Meaning. Alternatively, “wherein the gm-boost circuit increases the gm value of the current buffer driver”	Indefinite

The claimed “large gm value” is not indefinite because the specification provides objective guidance to determine the bounds of this term with reasonable certainty. Namely, the gm value must be sufficiently large to provide a pole-splitting effect that pushes the regulator’s undesirable pole to a frequency that will not interfere with its operation. (Taylor ¶¶ 65-68; '074 patent, 4:6-15, 5:40-45.) Aptiv does not dispute that the specification teaches the use of a “large gm” to achieve the desired “the pole-splitting effect.” (Opp. 14.) Nor does Aptiv dispute that a POSITA would have understood how gm affects a regulator’s poles. (Opp. 14-15.) Instead, Aptiv raises three arguments that this teaching does not go far enough to impart reasonable certainty. All three fail to provide clear and convincing evidence of invalidity. *BASF Corp. v. Johnson Matthey Inc.*, 875 F.3d 1360, 1365 (Fed. Cir. 2017) (“[Defendant] had the burden of proving indefiniteness by clear and convincing evidence.”) (citation omitted).

First, Aptiv argues that a report by the International Search Authority (“ISA”) expressing concern that it was “not clear how large a gm value needs to be to be considered ‘large’” indicates that this term is indefinite. Quite the opposite. The examiner expressly allowed the claims *after* the ISA issued its report, meaning that the examiner considered and rejected the ISA’s assessment. *Innogenetics, N.V. v. Abbott Labs.*, 512 F.3d 1363, 1379 (Fed. Cir. 2008) (“Given that the [] PCT application had been submitted for the patent examiner to examine herself, she was free to accept

or reject the patentee's arguments"). If anything, this strengthens the presumption of validity on this issue, and Aptiv thus has "the added burden of overcoming the deference that is due to a qualified government agency presumed to have properly done its job ... and whose duty it is to issue only valid patents." *PowerOasis, Inc. v. T-Mobile USA, Inc.*, 522 F.3d 1299, 1304 (Fed. Cir. 2008) (quoting *Am. Hoist & Derrick Co. v. Sowa & Sons*, 725 F.2d 1350, 1360 (Fed. Cir. 1984)).

Second, Aptiv argues that because the specification appends the adverb "fairly" to the phrase "large gm value" in one of four instances of this term, the scope of the term is indeterminate. But Aptiv's assertion that this usage establishes two distinct quantities—a "fairly large gm" and a "large gm"—does not withstand scrutiny. To the contrary, the specification uses these terms interchangeably to refer to the amount of gm necessary to achieve the desired pole-splitting effect, and thereby allow for a greater range of external capacitor ESR values. Namely, the specification explains that:

[1] A voltage regulator has a **large gm** current buffer driver added between a first stage of an operation amplifier and a last stage power transistor. This current buffer ***allows a significant reduction in the maximum internal and external compensation capacitances*** needed for regulator stability.

[2] [A] voltage regulator may comprise a **large gm** (transconductance) current driver (low impedance current buffer amplifier) [T]he current buffer, according to the teachings of this disclosure, ***offers the circuit designer a wider range of external capacitor sizes to choose from.***

[3] The key to being able to use ***smaller value internal and external capacitances*** is to have a **large gm** current driver buffer amplifier 204 between the first stage OpAmp 202 and the last stage power output driver 206.

[4] [T]he current buffer driver 204 ***pushes this pole to a high frequency*** beyond unity-gain frequency due to its low-impedance characteristics in order to get the pole-splitting effect. To achieve this, it is necessary to provide a ***fairly large gm*** value of the current buffer driver 204.

('074 patent, Abstract; *id.* at 3:29-41, 3:58-62, 4:11-15 (emphasis added).) In short, "fairly large gm" and "large gm" are both described as achieving the goal of the invention. Accordingly, the

most plausible interpretation is that the terms are interchangeable, and that stray usage of the term “fairly” was redundant and not definitional.

Moreover, the only two cases Aptiv cites are inapposite. In *CAE Screenplates, Inc. v. Heinrich Fiedler GmbH & Co. KG*, the Federal Circuit held that an amendment during prosecution replacing a claim reciting the term “bottom” with one reciting “bottom *plane*” to overcome prior art indicated a meaningful difference between the terms. 224 F.3d 1308, 1317 (Fed. Cir. 2000). That is not the case here. “Fairly large” is not a claim term, let alone one added in a narrowing amendment to escape prior art. Its isolated use in the specification does not somehow render the term “large” indefinite. *Id.* Likewise, in *Intell. Ventures I LLC v. AT&T Mobility LLC*, the specification’s use of the term “*relatively* large” created ambiguity because it “impl[ied] that the number ... should be compared to something else, without explaining what that is.” No. CV 13-1668-LPS, 2016 WL 4363485, at *17 (D. Del. Aug. 12, 2016) (citation omitted). By contrast, here there is no such “relative” comparison creating ambiguity.

Third, Aptiv argues that pole splitting cannot serve as a reasonable metric because the gm required to provide pole splitting “changes depending on the load being driven.”⁴ (Opp. 14.) This only proves Microchip’s point. As detailed in Microchip’s Opening Brief, “[t]he requisite gm is a context-dependent value that depends on real-world variables including the impedance of the device the regulator is driving” (Br. 19.) Accordingly, requiring numerical precision would impose an impossible standard. However, in the context of real-world circuitry, POSITAs can apply standard circuit analysis techniques—like Bode plots and Root Locus analysis—to assess the effects of practical variables on the requisite gm. (Taylor Reply ¶ 17.) Variations in load

⁴ “Load” refers to the device that is driven by the regulator. The load has electrical characteristics, such as impedance and capacitance. (Taylor Reply ¶ 17.)

during operation are no more confounding than other practical variables. Indeed, circuit designers understand the practical applications of the regulators they design, and routinely design circuits to operate over a range of expected loads. (Taylor Reply ¶ 17.) This is not particularly difficult, as load characteristics have little effect on the location of poles in a regulator. (Taylor Reply ¶¶ 18-21.) Accordingly, the '074 patent's objective to use a large gm to achieve pole splitting would provide reasonable certainty to a POSITA. *Ironburg Inventions Ltd. v. Valve Corp.*, 64 F.4th 1274, 1288 (Fed. Cir. 2023) (stating that “[t]he need to meet the purpose of the claimed invention ... helps inform one of ordinary skill’s understanding of the scope of the claims with reasonable certainty”).

Separately, Aptiv complains that Microchip’s alternative proposed construction—“wherein the gm-boost circuit increases the gm value of the current buffer driver”—does not expressly require a sufficiently large gm value to provide a pole-splitting effect. To avoid any ambiguity, Microchip is willing to clarify its alternative proposed construction to read “wherein the gm-boost circuit increases the gm value of the buffer driver *to be sufficiently large to provide pole-splitting*.”

C. Term 5: “low gain and high bandwidth amplifier”

No.	Claim Term	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
5	“low gain and high bandwidth amplifier” '074 patent, claims 8, 9	Not Indefinite. Plain and Ordinary Meaning. Alternatively, “amplifier optimized for high bandwidth with a commensurate reduction of gain”	Indefinite

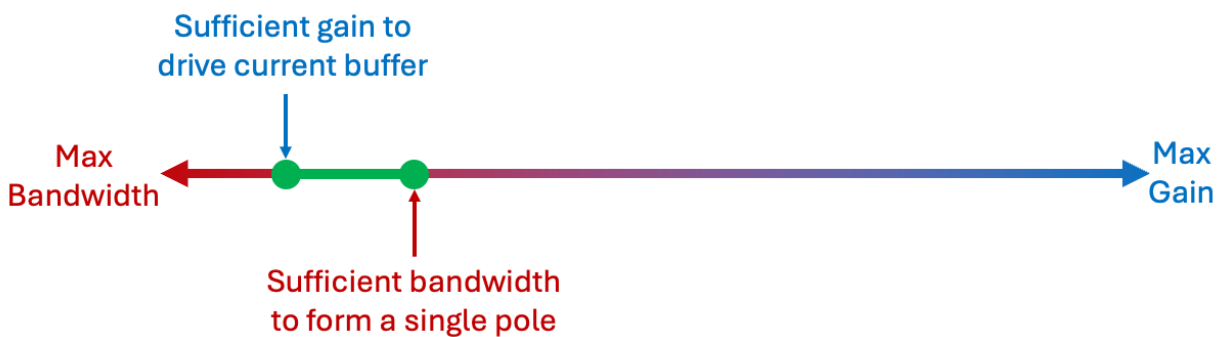
When read in the context of the specification, “low gain and high bandwidth amplifier” is sufficiently definite to allow a POSITA to understand the bounds of the claims at issue. Aptiv’s

argument that the words “low” and “high” are so subjective as to render the claims indefinite fails on the law and the facts.

First, Aptiv argues that without an explicit numerical boundary—e.g., “5dB,” “10dB,” or “40dB”—this term is indefinite. (Opp. 16.) That is not the law. To the contrary, “[n]ot every term needs to be reduced to a numerical certainty in order to avoid an indefiniteness problem.” *Med-El Elektromedizinische Geräte Ges.m.b.H. v. Advanced Bionics, LLC*, No. 1:18-cv-01530-JDW, 2020 WL 5994181, at *3 (D. Del. Oct. 9, 2020). Rather, “claim language employing terms of degree has long been found definite where it provide[s] enough certainty to one of skill in the art when ***read in the context of the invention.***” *Niazi Licensing Corp. v. St. Jude Med. S.C., Inc.*, 30 F.4th 1339, 1347 (Fed. Cir. 2022) (internal quotation marks and citation omitted). As detailed above and below, a POSITA would understand the scope of this term with reasonable certainty in the context of voltage regulator circuitry.

Second, Aptiv argues that this supposed quantification problem is “compound[ed] ... by the fact that all Op Amps have an inherent gain-bandwidth product (GBP) which can differ by orders of magnitude from one Op Amp to another.” (Opp. 16.) This only proves Microchip’s point. Because requisite “low gain” and “high bandwidth” are context-dependent values that depend on the specific circuitry employed—including the choice of Op Amp—it is not possible to quantitatively specify these values in the abstract. But the numerical precision Aptiv insists upon is not required because, as detailed above and below, the patent provides a POSITA with objective guidelines for evaluating the claim scope in the context of real-world circuitry. *Ironburg*, 64 F.4th at 1285 (explaining that “numerical precision is not always required, even when using a term of degree” and claims are definite so long as “the patent provides sufficient guidance to give one of ordinary skill reasonable certainty as to the scope of the claims”) (citations omitted).

Third, Aptiv argues that the '074 patent's provision of multiple items of objective guidance—that the Op Amp must balance (1) having sufficient bandwidth such that it forms only a single pole; but (2) still offering sufficient gain to drive the current buffer—somehow multiplies the uncertainty. (Opp. 17.) But this only heightens the precision. Namely, these criteria define a limited range (green below) on the gain/bandwidth sliding scale where the Op Amp provides (1) enough gain to drive the system's current buffer, but (2) enough bandwidth to form a single pole:



(Taylor ¶¶ 71-76; Taylor Reply ¶¶ 23, 25).

Nor does the word “sufficient” undermine the reasonable certainty of the claims, as Aptiv implies. Indeed, although Aptiv complains that a POSITA “*would have to* determine not only when an amplifier is sufficiently “low gain,” but also whether it offers “sufficient gain” to drive the current buffer” (Opp. 17 (emphasis added)), neither Aptiv nor Dr. Shanfield argue that a POSITA *could not* do so. And indeed, a POSITA could apply rudimentary circuit analysis techniques to make these assessments in the context of real-world circuitry. (Taylor Reply ¶¶ 23-25.)

Once again, Aptiv has not met its burden to show this term is indefinite, let alone by clear and convincing evidence.

DATED: April 17, 2024

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CERTIFICATE OF SERVICE

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**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

MICROCHIP TECHNOLOGY INC.,

Plaintiff,

v.

APTIV SERVICES US, LLC,

Defendant

C.A. No. 1:23-CV-00778-JDW

JURY TRIAL DEMANDED

**GREG TAYLOR DECLARATION
IN SUPPORT OF MICROCHIP'S REPLY CLAIM CONSTRUCTION BRIEF**

I, Greg Taylor, declare as follows:

I. Introduction

1. I have been asked to provide my opinions regarding Aptiv's Responsive Claim Construction Brief and Dr. Shanfield's Declaration.

2. All the opinions in this report are based on my personal knowledge and professional judgement. If called as a witness, I am prepared to testify competently about them.

3. I am being compensated for my time spent on this matter at my standard consulting rate. My compensation is in no way dependent upon the substance of my opinions, my testimony, or the outcome of this litigation, nor do I have a personal interest in the outcome of this litigation.

4. My opinions are based on the information I have received and reviewed and the analysis I have carried out to date. I reserve the right to supplement, clarify, modify and/or change my testimony as additional facts, questions, or issues come to my attention.

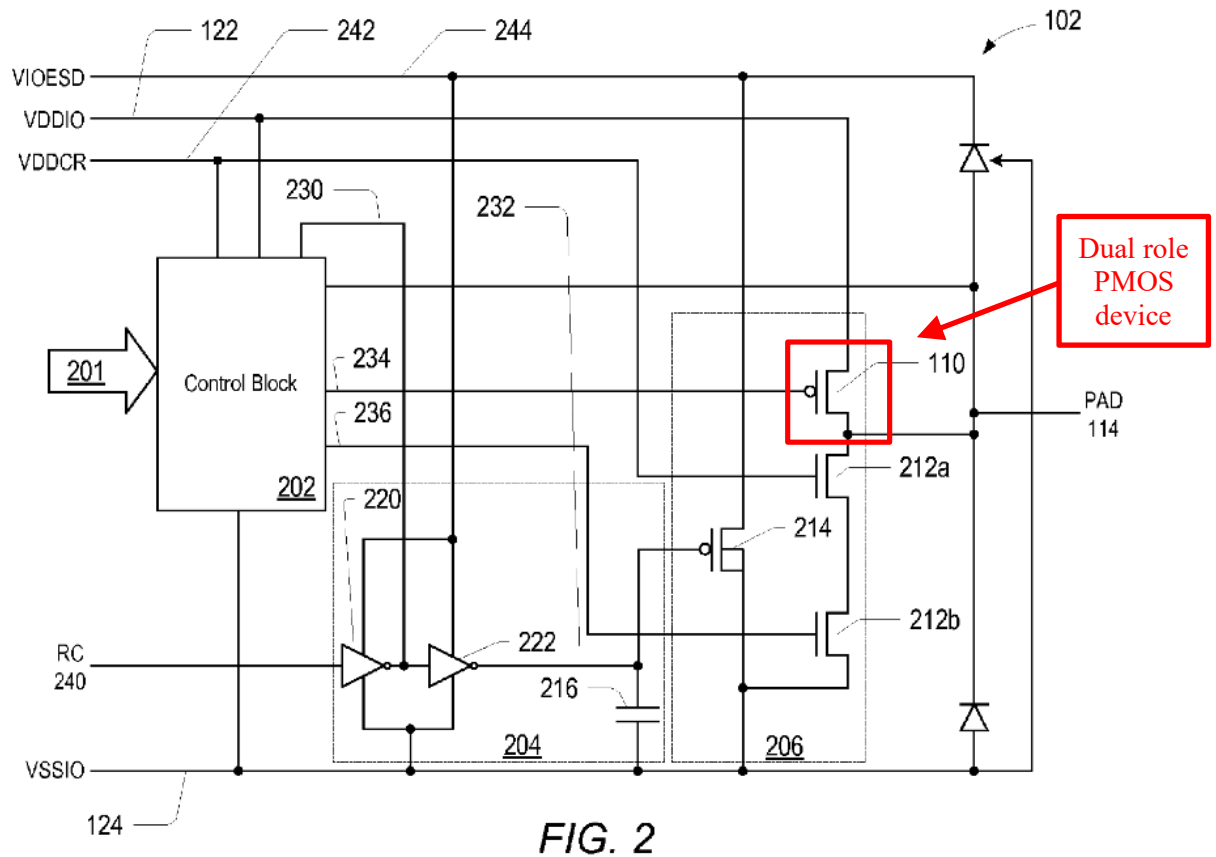
5. My experience and qualifications are detailed in my March 1, 2024 Declaration in Support of Microchip's Opening Claim Construction Brief.

II. Materials Considered

6. I incorporate by reference any materials considered that were mentioned in my opening declaration. I have also considered Aptiv’s Responsive Claim Construction Brief and Dr. Shanfield’s Declaration.

III. Electrostatic Discharge (ESD) Protection and the ’665 Patent

7. In his declaration Dr. Shanfield says: “The circuits described in the ’665 patent generally consist of **two separate systems**—components designed for ESD protection and components designed for normal (i.e., non-ESD) operations. In other words, the circuit describes both what is being protected and what is doing the protecting.” (Shanfield Declaration, ¶33 (emphasis added).) This is not entirely true. Although some of the components shown in Figure 2 of the ’665 patent have other functions, all of them serve a role in ESD protection. One example of this is provided by PMOS transistor 110 which during normal operation serves to drive pad 114 high in response to system control signals, but during ESD events is turned on to share the energy of the ESD zap to any single pad 114 across the capacitance of all the pads sharing the VDDIO power supply. This dual use is articulated in the specification of the ’665 patent. (’665 patent, 2:51-65.)



A. '665 Patent, Claim 1 – “second voltage rail”

No.	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
1	<p>Plain and Ordinary Meaning</p> <p>Alternatively, “a second voltage rail that is distinct from the third voltage rail but may or may not be distinct from the first voltage rail”</p>	<p>“a second voltage rail that is distinct from the first voltage rail”</p>

8. In support of his opinion regarding this claim term, Dr. Shanfield quotes the '665 patent specification’s explanation that “VIOESD 244 and VDDIO 122 may in fact be the same power/supply rail, and alternate embodiments may be configured with a single power rail providing power to the circuit and/or system components that are powered by VIOESD 244 and VDDIO 122 in the embodiment shown in FIG. 2. In general, the ESD rail and the power supply rail can be the same supply rail, and separate supply rails (e.g., VIOESD 244 and a distinct VDDIO

122) may not be required.” (’665 patent, 5:57-65.)¹ Dr. Shanfield then opines that “a POSITA would read this to be a general statement that a single rail could be used to power both the ESD protection components of circuit 102 (powered by VIOESD) and also the general I/O components of the circuit (powered by VDDIO). I do not dispute that it is possible to configure such a circuit, but a POSITA would understand, however, that the two arrangements are not identical to one another and there are reasons that a POSITA may choose one arrangement over the other.” (Shanfield Declaration, ¶51.) I agree that a POSITA would understand that single power rail configurations and dual power rail configurations are both possible, and that a POSITA would understand the differences between them. But no such functional or structural differences are reflected in or required by the language of claim 1 and neither Dr. Shanfield nor Aptiv have identified any claim language requiring the two voltage rails to be separate.

9. Indeed, the fundamentals of the response to the ESD event are the same in single power rail and dual power rail configurations of the ’665 patent. Namely, the electrostatic charge will be both (1) shared with other I/O pad cells; and (2) shunted to ground through a clamp. A POSITA will understand that there is no fundamental difference between split and joined power rails, that both are appropriate to use in different circumstances, and would choose between these implementations based on other needs of the system being delivered. However, claim 1 of the ’665 patent does not implicate those tradeoffs, and would not indicate to a POSITA that it is restricted to either a single power rail or dual power rail configuration.

¹ Dr. Shanfield’s declaration cites claim 1 of the ’665 patent as the source for this quotation, but I understand that this was an error. I cite the correct portion of the specification here.

IV. USB Voltage Regulators and the '074 Patent

A. Term 2 – “an enable/disable function to enable/disable the biasing circuit for reducing standby current” ('074 Patent, claim 1)

No.	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
2	Not subject to 35 U.S.C. 112 ¶ 6. To the extent the court determines that § 112 ¶ 6 applies: Function: to enable/disable the biasing circuit for reducing standby current Structure: enable/disable signal input line (Node M)	Indefinite; Subject to 35 U.S.C. § 112 ¶ 6 without any corresponding structure

10. I disagree with Dr. Shanfield’s claims that a POSITA would not understand the usage of “enable/disable function” because it “requires both enabl[ing] and disable[ing] the biasing circuit to reduce standby current.” (Shanfield Declaration, ¶58 (quotation marks omitted).) Functional descriptions of switches with a binary pair of choices are common and not confusing. Two household examples are “on/off” switches and the “heat/cool” setting on a thermostat. These are recognized as an enumeration of two different possible outcomes to be chosen between. The claim term is similar to an “ON/OFF switch for turning a light ON/OFF to save electricity when not in use.” The light switch is either on (and using electricity) or it is off (and not using electricity); there is no confusion that electricity is saved only when the switch is off. “Enable/disable” is of the same nature and a POSITA’s common sense would eliminate any confusion. In this case the “enable” state enables some function allowing it to be used, while the “disable” state disables the function, and thereby saves the power that capability would normally consume. Moreover, Dr. Shanfield’s interpretation is incorrect because if both enabling and disabling the circuit required turning the circuit off to reduce standby current, the regulator would be permanently disabled and would be pointless. Rather, the claim language and specification make clear that the enable/disable “enable[s]/disable[s] the biasing circuit for reducing standby current” such that, when the circuit

is enabled, it functions normally, and when it is disabled, the flow of current is restricted so as to save power when not in use. For example, the specification explains that “Node M is the enable signal coming to the regulator circuitry **so that the module can be turned off when disabled.**” (’074 patent, 4:44-45 (emphasis added).)

11. Dr. Shanfield’s subsequent review of the product data sheets that were referenced in my earlier declaration (as Exhibits 1-5) supports my opinion that the term is understood to be structural. He states: “These exhibits use the terms ‘enable,’ ‘enable pin,’ ‘enable input,’ ‘EN,’ or ‘EN pin’ to **refer to a physical pin and/or wire** through which a signal may be sent to some logic circuit on the regulator that acts to turn circuitry on or off based on the voltage of the signal. Exhibit 1 uses the terms ‘smart enable,’ ‘smart enable circuit,’ and ‘smart enable input circuit’ to **refer to circuitry** that implements logic to turn on or off some other circuitry on the regulator, based on receipt of an input signal. Exhibit 3 uses the terms ‘enable logic control function,’ ‘enable function’ and the label ‘Enable’ on Figure 1 to **refer to the same type of circuit logic.**” (Shanfield Declaration, ¶60) (citations omitted; emphasis added).) Because the quoted terms refer to physical pins and/or circuitry, clearly they are referring to real structural elements and not to abstract functions.

12. I also disagree with Dr. Shanfield’s characterization of my Exhibit 5, the digital logic textbook. Dr. Shanfield argues that book merely “uses the letter ‘e’ and the phrases ‘enable signal’ and ‘enable signal e’ to refer to various voltage signals, not to refer to any structure.” (Shanfield Declaration, ¶60.) But the textbook expressly depicts these enable inputs as controlling transistors to enable or disable the flow of current through the circuitry using physical inputs to the transistors. (Exhibit 5, 73.)

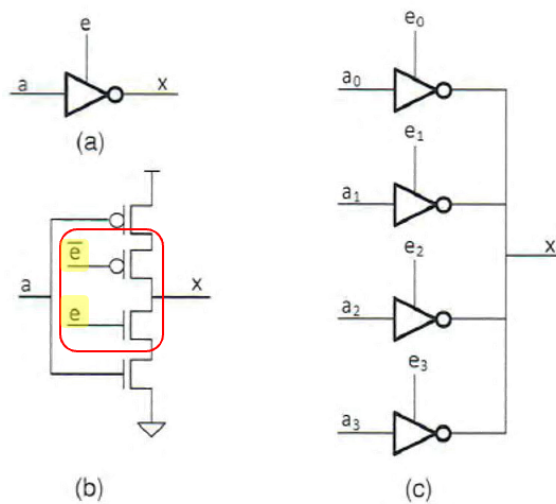


Figure 4.25. A tri-state inverter has two inputs and a single output, (a). Transistor level schematic, (b), when enable e is low, there is no supply connected to the output. When e is high, the output is driven to $\bar{a}$. Four tri-state inverters implement a bus or distributed multiplexer, (c). When exactly one enable e_i is high, the output is $\bar{a}_i$. When all enables are low, the output is indeterminate. If multiple enables are high, permanent damage may occur.

13. In his declaration Dr. Shanfield refers to a figure that is “below” ¶61 and “above” ¶63, but there is no figure in or between these paragraphs. Dr. Shanfield’s incomplete declaration with reference to non-existent figures makes his declaration unreliable and without basis to respond fully. To the extent Dr. Shanfield supplements this declaration with new information that should have been in his opening declaration, I reserve the right to respond.

14. Dr. Shanfield acknowledges that the '074 patent discusses the process of disabling a section of circuitry to reduce standby current [by] refer[ring] to structure that includes multiple transistors—numbered ‘320, 330, 334 and 336.’” (Shanfield Declaration, ¶65.) Thus, Dr. Shanfield and I agree that there is disclosed structure for disabling the biasing circuit to reduce standby current. I disagree, however, that the exact arrangement of transistors is required for the disclosed function. Rather, a POSITA would have understood that the disclosed “enable/disable function” is an input line controlling the flow of current through biasing transistors. It is a fundamental principle of circuit design that an enable signal input line may be fed into any appropriate set of transistors to disable a portion of the circuit. The structure necessary to accomplish the function is,

at most, the enable signal input line controlling the flow of current through a set of one or more transistors. By contrast, a POSITA would understand that the *specific arrangement* of biasing transistors is a function of the particular biasing circuitry used in a regulator.

15. At the end of this section Dr. Shanfield complains that the '074 patent is incomplete: “Additionally, there must be some structure—that is not disclosed by the '074 patent—for creating and switching on/off the enable signal the patent calls Node M and that it describes as coming to the regulator circuit so that the module can be turned off when disabled.” (Shanfield Declaration, ¶65 (quotation marks omitted).) But that argument is beside the point because the recited function is enabling/disabling the biasing circuit to reduce current; it is not the creation of this signal, or logic evaluating when to apply this signal. Rather, the claim is silent on those functions and the specification therefore need not disclose them for means-plus-function purposes.

B. Term 4 – “wherein the gm-boost circuit enables the current buffer driver to have large gm value” ('074 Patent, claim 4)

No.	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
4	Not indefinite. Plain and ordinary Meaning Alternatively, “wherein the gm-boost circuit increases the gm value of the current buffer driver”	Indefinite

16. I disagree with Dr. Shanfield’s conclusion that the claim term “wherein the gm-boost circuit enables the current buffer driver to have large gm value” cannot be understood with reasonable certainty. As explained in my prior declaration, and as discussed further below, a POSITA would have understood the claim term with reasonable certainty. A POSITA would have understood that “large gm value” is context dependent, and in view of the specification’s teachings, would have had the means and understanding to account for various factors to design a system

with a large gm value to achieve the pole splitting effect that is discussed in the '074 specification. A POSITA would have understood that “large gm value” would need to be large enough to push the output pole to or beyond the unity gain frequency of the regulator, resulting in the op-amp pole dominating the behavior of the regulator.

17. A POSITA would have several tools to understand and analyze voltage regulator circuits, pole splitting, and gm values. For example, and as discussed in my prior declaration, one common tool is Bode plots, which may include considering the Phase Margin and Gain Margin (both of which can be derived from Bode plots). A POSITA also would have understood that Root Locus analysis can be used to evaluate and select appropriate parameter values for a regulator circuit. Generally, a Root Locus analysis allows a POSITA to consider the effects of various parameters on poles and zeroes and their impact on the stability of the system. When designing a regulator circuit, a POSITA would have relied on these exemplary tools and analysis, as well as others, to account for real-world variables, such as load (i.e., the device that is driven by the regulator) characteristics. Unsurprisingly, voltage regulators are typically designed to support varying loads because a voltage regulator that supports only a single load (or a limited range of loads) would have limited practical use.

18. While load is a variable that is considered when designing a circuit, a POSITA would have understood that load ultimately has negligible effect on the location of poles. As described in the '074 specification, the purpose of the invention is to push all but one of the poles in the system to a high frequency so we are left with only a dominant pole at the output of the op-amp. As the specification explains:

The output stage (transistors 350, 360 and 366) from the OpAmp 202 (FIG. 3A, node C) then connects to the gate of the PMOS second stage transistor 384. The low impedance looking into the amplifier function of the current buffer 204 and source of transistor 384 **creates a fairly high frequency pole that would be**

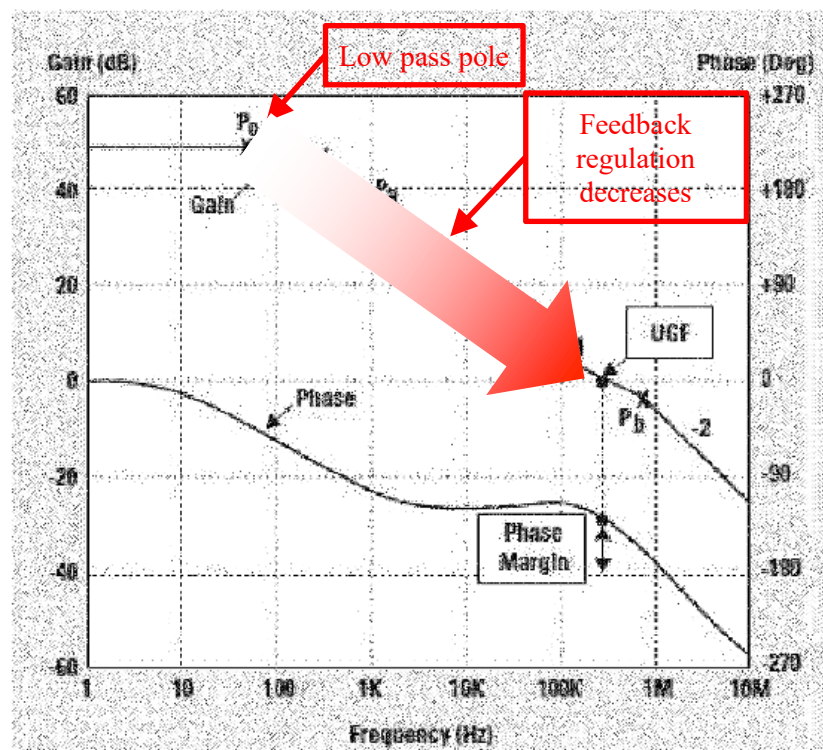
irrelevant to interact with the system dominant pole, which connects to the power PMOS transistor 380 in the power output driver 206, thereby having more efficient pole-splitting, and allowing easier frequency compensation. The current driver stage transistor 384 (in the current buffer 204) of the regulator circuit shown in FIG. 3B creates a low impedance environment using the current buffer (transistors 384 and 394, and resistor 372) **to separate the poles seen on the big power output driver 206** comprising transistor 380 and the internal stages of the regulator (OpAmp 202, FIG. 3A, node C). **By literally pushing the pole at the gate of transistor 380 to a high frequency domain, effectively leaves the only dominant pole at the output (node C) of the OpAmp 202 during full-load conditions.** To achieve such operation, a gm-boost stage may be used.

(’074 Patent, 4:55-5:7.)

19. As the specification further explains: “With the simple current buffer 204 comprising transistors 368, 370, 374, 376, 378, 382, 396, 394, 400, 402, 384 and resistor 372, the voltage regulator acts like a pseudo ‘one-pole’ system that is independent from the output pole changing so long as it falls within the bandwidth of the system. Thus, the range of ESR is extended along with the output capacitance. Therefore a wider range of external capacitors may be effectively used, according to the teachings of this disclosure.” (’074 Patent, 5:40-49.) This disclosure is consistent with a POSITA’s understanding that it is immaterial whether the load on the circuit changes because by splitting the poles, the design of the circuit is specifically intended to handle those changes. In particular, a POSITA would have understood that once the output pole is pushed to or beyond the unity gain frequency of the regulator, the output pole will not be materially impacted by changes in the load. In fact, as Figure 4 of the specification demonstrates, the circuit remains stable even when the ESR values of the external capacitor vary by a factor of 200 and/or when the capacitance is varied by a factor of 10.

20. In contrast, Dr. Shanfield appears to misunderstand the structure of the regulator. He states “the position (i.e., frequency) of the pole creating instability strongly depends on the electrical characteristics (e.g., **ESR for a capacitive load**) of the range of loads that could be

present at the regulator output.” (Shanfield Declaration, ¶70 (emphasis added).) But the external capacitor is not part of the load placed upon the regulator, it is an element of the regulator itself. The regulator feedback loop is a “low pass” filter – at frequencies below that of the lowest frequency pole (P_0 in Figure 1(a) of the '074 Patent, shown below) it corrects changes to the output voltage to maintain regulation of the output voltage. At frequencies above P_0 this control response gets progressively weaker and at very high frequencies, the regulator feedback loop provides less correction but the external capacitor compensates.



'074 Patent Figure 1(a) Normal Frequency Response (with annotation)

21. For example, if the output voltage of the regulator is to remain within 5% of its target value and the reference generated internally to the regulator has an accuracy of $\pm 1\%$, then the output of the regulator can change by at most 4% when the output current switches between its minimum and maximum values. Dividing 4% of the typical output voltage by the change in current

between minimum and maximum yields a “load line” resistance. The magnitude of the output impedance of the regulator must be smaller than this value to maintain regulation as the load changes. To deliver this low output impedance at high frequencies, the output capacitance must be large enough that the magnitude of its impedance ($ESR + \frac{1}{j2\pi fC}$) is below the required “load line” resistance before the frequency (f) becomes high enough that the regulator feedback loop starts to lose control of the output. As a POSITA would have known, this ESR requirement is in addition to the stability concerns that the patent addresses. It is addressed here because it shows that the external capacitor is not part of the load even though in this embodiment of the invention, it is external to the chip containing the rest of the regulator. Accordingly, the regulator is not sensitive to variations in the load, which is why designs are commonly broken up into separate “regulators” and “loads.” As such, a POSITA would have been able to determine if gm is large enough to deliver pole splitting despite reasonable variations in load characteristics.

C. Term 5 – “low gain and high bandwidth amplifier” (’074 Patent, claim 8)

No.	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
5	Not Indefinite. Plain and Ordinary Meaning Alternatively, “amplifier optimized for high bandwidth with a commensurate reduction of gain”	Indefinite

22. I disagree with Dr. Shanfield’s opinion that a POSITA “would not be able to determine with reasonable certainty when a given operational amplifier is sufficiently low gain and sufficiently high bandwidth to fall within the scope of the claims.” (Shanfield Declaration, ¶73.) Rather, as I explained in my opening declaration, a POSITA would have understood the boundaries of the claim given the specification’s guidance.

23. Dr. Shanfield complains that different op-amps have different gain-bandwidth products (Shanfield Declaration, ¶¶76-79), but this is irrelevant in view of the patent's teachings to create a dominant pole. As a POSITA would recognize, the design of a regulator requires balancing many factors including both performance and cost. The op-amp and the input of the regulator is no exception. Figure 3 from my original declaration appears below with additional annotations. This Bode plot for a first order system is a reasonable approximation for the Bode plot of a system with a dominant pole. Here we see the (dominant) pole appears at 100 Hz with a gain of 50 dB. The gain then rolls off at -20 dB/decade until it reaches unity gain at a frequency of about 31 kHz. Importantly, a POSITA would have understood that to achieve the necessary pole splitting and, consequently, stability for the regulator, the non-dominant poles need to be pushed beyond unity gain. In other words, the higher unity gain is from the dominant pole frequency, the harder it will be to split the poles effectively. Thus, a POSITA would have understood to keep gain low to simplify effective and efficient pole splitting.

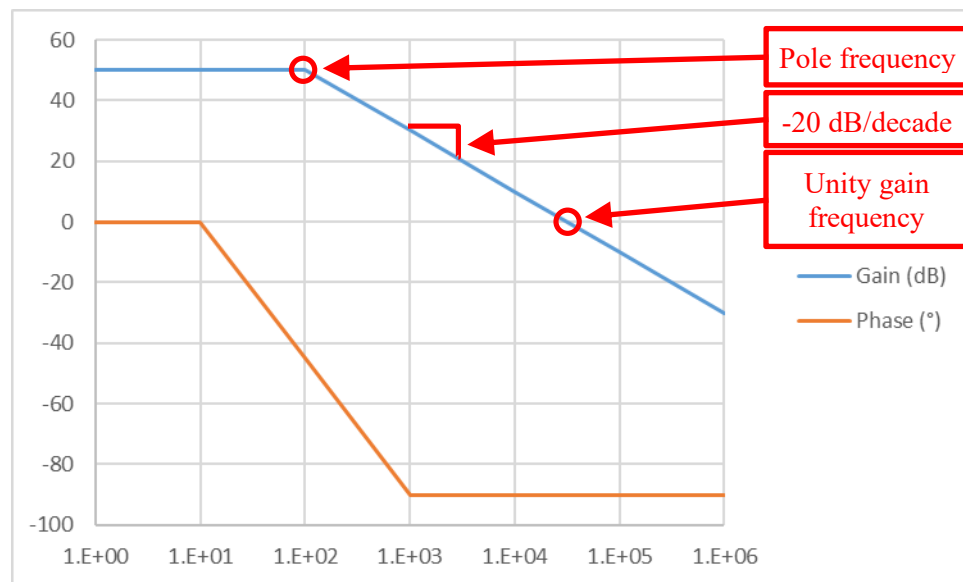


Figure 3. Bode plot for a first order amplifier

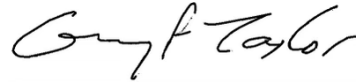
24. Once the dominant pole's frequency and the low frequency gain are chosen, there are no more degrees of freedom. That is, the gain of a first order system always rolls off at -20 dB/decade, so, for example, a gain of 50 dB means the unity gain frequency will be 2.5 decades above the pole frequency.

25. Most important, a POSITA would have understood these concepts and, based on the guidance in the specification, would have understood how to build a given voltage regulator circuit to be low gain, and consequently high bandwidth, in order to meet the specified guidance of stability through pole-splitting. For example, a POSITA would have understood how to take a given set of design constraints—e.g., expected load of a circuit, expected temperatures, target voltages, necessary currents, etc.—and calculate the appropriate low gain, high bandwidth op-amp to ensure effective pole-splitting. While the metrics would change depending on the particulars of a given regulator, the fundamental concepts do not change and provide sufficient guidance to a POSITA.

26. I disagree with certain other opinions rendered by Dr. Shanfield in his report regarding the technical disclosures of the '665 and '074 patents. However, because Aptiv has not relied on those opinions in the present claim construction dispute, I have not been asked to address them here. Should Aptiv rely on those opinions in the future, I reserve the right to supplement my reports.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct, and that all statements reflect my opinions based upon my knowledge and experience.

Date: April 17, 2024

A handwritten signature in black ink, appearing to read "Gregory F. Taylor". The signature is written in a cursive, flowing style.

Gregory F. Taylor