

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APTIV SERVICES US, LLC,
Petitioner,

v.

MICROCHIP TECHNOLOGY INC,
Patent Owner.

Case No. IPR2024-00646
U.S. Patent No. 9,471,074

PATENT OWNER'S RESPONSE

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LISTING OF EXHIBITS

Exhibit	Description
2001	U.S. Pat. 7,312,598 (“Huang”)
2002	Aptiv’s Responsive Claim Construction Brief and supporting Declaration of Stanley Shanfield, Ph.D. (March 22, 2024)
2003	Aptiv’s Sur-reply Claim Construction Brief and supporting Declaration of Stanley Shanfield, Ph.D. (May 3, 2024)
2004	U.S. Pat. 6,246,22 (“Xi”)
2005	Chronological File History for U.S. Pat. 9,471,074
2006	Aptiv’s District Court Invalidity Contentions (December 8, 2023)
2007	Microchip’s Opening Claim Construction Brief and supporting Declaration of Greg Taylor (March 1, 2024)
2008	Microchip’s Reply Claim Construction Brief and supporting Declaration of Greg Taylor (April 17, 2024)
2009	Docket in <i>Microchip Technology Inc. v. Aptiv Services US, LLC</i> , Case No. 1:23-cv-00778-JDW (D. Del.)
2010	<i>Aptiv Services US, LLC v. Microchip Technology Inc.</i> , IPR2024-00803, Paper 10 (Institution Decision) (P.T.A.B., November 7, 2024)
2011	Texas Instruments datasheet for LM2990 Negative Low Dropout [Voltage] Regulator, April, 2013
2012	ST Micro datasheet for L78MxxAB/C voltage regulator, May 2012 (from Dr. Chen deposition)
2013	’074 patent claim 1 (from Dr. Chen deposition)
2014	Rincon-Mora Biasing Circuit (Fig. 3) (from Dr. Chen deposition)
2015	Al-Shyoukh Biasing Circuit (Fig. 8) (from Dr. Chen deposition)

Exhibit	Description
2016	Texas Instruments datasheet for LM1117/LM1117I Low-Dropout Linear [Voltage] Regulator, 2012
2017	Excerpts from the Laplante Electrical Engineering Dictionary (CRC Press LLC, 2000)
2018	December 4, 2024 Deposition Transcript of Dr. Michael Chen.
2019	Microchip 300 mA CMOS LDO with Shutdown, Bypass and Independent Delayed Reset Function, 2012
2020	Fairchild KA78RXXC-Series 1A Output Low Dropout Voltage Regulators datasheet
2021	Declaration of Dr. Greg Taylor in Support of Patent Owner's Response
2022	<i>Universal Serial Bus 3.0 Specification</i> , Revision 1.0, November 12, 2008 ("USB 3.0 Specification")

I. INTRODUCTION

Patent Owner Microchip Technology Inc. (“PO”) submits this Patent Owner Response (“POR”) to Aptiv Services US, LLC’s Petition for *Inter Partes* Review (Paper 1, the “Petition”) of U.S. Pat. 9,471,074 (the “’074 patent”). The Board should find all challenged claims not unpatentable for three independent reasons.

First, Petitioner erroneously conflates two separate claim requirements (gm enhance[ment]¹ (element 1[b]) and gm-boost (element 1[c])). While related in some respects, they are separate limitations that employ distinct circuit techniques. Petitioner points to the same circuitry in Rincon-Mora and Al-Shyoukh to satisfy both limitations. In doing so, Petitioner fails to establish that either Rincon-Mora or Al-Shyoukh disclose gm enhance[ment].

Second, claim 1 requires a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver. See element 1[c]. But Petitioner points to **currents** for element 1[c]. And the only bias circuit Petitioner’s expert could identify at deposition has nothing to do with set[ting] a biasing ratio for gm-boost of the current buffer driver.

Third, Petitioner fails to show a motivation to combine the Ivanov reference, relying instead on impermissible hindsight reasoning. Petitioner fundamentally

¹ Claim language is setoff in **red italics**.

misapprehends the Rincon-Mora and Al-Shyoukh references, believing they express a need for enable/disable functionality when in fact they teach the opposite. Absent Petitioner’s mistaken premise, there is no motivation to combine at all. Even if Rincon-Mora or Al-Shyoukh suggested a need for further power reduction (which they do not), Petitioner fails to consider any drawbacks or trade-offs that would be involved in deciding whether to combine Ivanov. In doing so, Petitioner erroneously focuses on what a POSITA ***could have*** done, not what a POSITA ***would have*** done.

II. LEVEL OF SKILL IN THE ART

Petitioner asserts that “[a] POSITA in the field of the ’074 patent in 2013 would have had at least a Master’s Degree in Electrical Engineering, or alternatively a Bachelor’s Degree in Electrical Engineering and two years of experience working on analog circuit design.” Pet., 9. Petitioner’s expert parrots the same sentence, without any discussion or analysis of why it is appropriate, or even mentioning what factors he considered in arriving at that definition. *See* EX1002, ¶38.

At Institution, PO had no reason to address Petitioner’s definition, and the Board “preliminarily” adopted it because it was “uncontested” at that time. ID (Paper 11), 9. PO submits a POSITA in 2013 would have a bachelor’s degree in electrical engineering, computer science, or equivalent technical degree and substantial experience (e.g., several years) in analog/mixed-signal IC design. Additional education related to the hardware, architecture, and circuit design aspects

could be substituted for professional experience, and vice versa. EX2021 (“Taylor”), ¶¶30-36.

PO explains in the analysis sections that follow (and the accompanying Taylor Declaration) the specific points it relies on regarding a POSITA’s knowledge as it relates to the state of the art, the interpretation and application of Petitioner’s prior art, and why Petitioner’s references and proposed combinations fail to establish obviousness.

To the extent Petitioner believes there are any substantive differences in the level of skill in the art—and concomitantly the knowledge of a POSITA—PO believes its assertions are correct and supported by substantial evidence, including the testimony of Dr. Taylor. Regardless, PO submits the IPR outcome should result in a determination that no challenged claim is obvious under either party’s articulation.

III. TECHNOLOGY BACKGROUND

The ’074 patent pertains to voltage regulator design, including a class of regulators called “low-dropout (LDO) voltage regulator[s].” *See, e.g.*, EX1001, 2:14-16. Accordingly, it is helpful to understand some basic concepts in voltage regulator design and analog circuits, voltage regulator performance parameters, and related regulator design considerations.

A. Voltage Regulators

A common component in many electronic systems is the voltage regulator, which provides a relatively steady/reliable supply voltage to one or more other components in the electronic system across a specified set of operating conditions (*e.g.*, within a specified temperature range, across a given range of load impedances, etc.). *See, e.g.*, EX1013 (“Rincon-Mora”), 1:18-21.

In the voltage regulator context, the descriptor “low drop out” refers to the fact that the regulator can supply an output voltage nearly equal to the supply voltage that powers the regulator. *Id.* So, for example, if the regulator supply voltage was 2V, the output voltage could almost equal 2V as well. This contrasts with other types of voltage regulators which often have a significant voltage “drop” between the supply voltage and the output voltage. Taylor, ¶¶53-65.

B. Common Voltage Regulator Components and Concepts

Voltage regulators typically include analog circuitry which can be categorized into two buckets: (1) the “active” circuitry (*viz.*, transistors) that lie in the path from input to output; and (2) the “bias” circuitry (*viz.*, transistors) that exists to ensure the “active” devices are set (*i.e.*, “biased”) to the appropriate steady state (*i.e.*, nominal or DC) current and/or voltage levels.

Biasing. The Laplante Electrical Engineering Dictionary (CRC Press LLC, 2000) provides the following definition of “biasing” which is applicable here:

“**biasing**: the technique of applying a direct-current voltage to a transistor or an active network to establish the desired operating point.” EX2017, 5; *see also id.*, 3-5 (definitions of “active device,” “bias current,” and “bias voltage or current”). This is consistent with how a POSITA would understand that term and concept in the context of LDO voltage regulators. Taylor, ¶¶46-52.

Active Circuitry. The active circuitry in a linear voltage regulator typically includes an amplifier and an output drive transistor (sometimes called a pass gate). Taylor, ¶¶46, 55. The amplifier receives a reference voltage input (*e.g.*, voltage desired to be reproduced on the output). The reference voltage is typically a stable voltage that does not vary (or varies very little) with temperature, other environmental conditions, or manufacturing. One may wonder why a voltage regulator is needed at all if there is already a stable voltage available on the input. The answer to that question lies with an understanding of the output “load.”

Output Load. The voltage regulator output drive transistor connects to a “load” on the output. The load simply refers to the component(s) that consumes the power (voltage and current) supplied by the voltage regulator. The nature of voltage regulators is to hold the output voltage constant, regardless of how much current is needed to do so. Taylor, ¶54. The amount of current necessary is a function of the size of the load being driven, which may frequently change. *Id.*

For example, in a USB voltage regulator, the load current depends on whether the USB device is actively sending and/or receiving signals. If the USB data lines are in “listening” mode, little load current is required. If the USB data lines are transmitting signals, the load current will be higher, which would typically lower the voltage according to well-understood laws of physics and engineering. Taylor, ¶¶64. The voltage regulator’s purpose is to hold the voltage steady even as the amount of current necessary to do so rapidly changes. It is difficult for the reference voltage on the input of the voltage regulator to do this because it is typically supplied by a special circuit custom-tuned to adjust for environment conditions like temperature change, not changes in output load. *Id.*, ¶¶50-53.

Example Voltage Regulator. Annotated Fig. 2 below from Rincon-Mora shows “a partial, simplified schematic illustration of selected portions of the output section of a conventional LDO voltage regulator.” Rincon-Mora, 2:54-56. One way Fig. 2 is simplified is that it does not show the bias circuitry.

voltage regulator design is transconductance. This is a well-known engineering concept which refers to a “quantity used to specify a field-effect transistor, defined as the differential change in drain current upon a differential change in gate voltage.” EX2017, 7. In simpler terms, transconductance measures how much the output current of a device changes as a function of input voltage change. The notation g_m is a universally recognized symbol for transconductance. See EX2017, 6 (“ g_m common notation for DC transconductance.”). The equation for determining transconductance is $g_m = \frac{\Delta i_{OUT}}{\Delta v_{IN}}$, where i_{out} refers to the output current, v_{in} refers to input voltage, and the triangle symbol Δ (called “delta”) reflects you are measuring a *change* in output current relative to a *change* in input voltage. The units of transconductance are called Siemens.

Generally speaking, higher transconductance is desirable in certain voltage regulator components. Taylor, ¶¶66-71. This is because higher transconductance generally means a voltage regulator can react more quickly and robustly to varying output current needs because only a small change between the reference and feedback voltages results in a large output current change. *Id.* The mechanisms used for “gm-enhancement” and “gm-boost” are discussed *infra* §§IV.A, VII.A.

Additional concepts regarding voltage regulator components and design principles are discussed throughout the Petition and the accompanying Taylor

declaration where relevant. *See, e.g.*, Taylor, ¶¶39-71 (Technology Background).

C. Voltage Regulator Performance Metrics

Al-Shyoukh identifies several “major performance requirements of [an] LDO [voltage regulator].” EX1004 (“Al-Shyoukh”), 1. These include: “low dropout voltage, high output current, low no-load quiescent current, and small output transient undershoots and overshoots.” *Id.* We briefly discuss each in turn.

Low Dropout Voltage. First, Al-Shyoukh observes “low dropout voltage across the pass device of the LDO is required [to] provide high power efficiency.” *Id.* As Dr. Chen admitted, “low dropout voltage” refers to “the output voltage that is produced versus the input voltage of this regulator[.]. We would like that voltage difference to be small, as small as possible.” EX2018 (Chen Tr.), 131:9-18. Power efficiency refers to the ratio of power provided by the regulator at its output relative to the total power the regulator consumes. Taylor, ¶32; *see also* EX1014, 1-2 (“[current efficiency is] the ratio of the load-current to the total battery drain current, which is comprised of load-current (I_{Load}) and the quiescent current (I_q) of the regulator: $\text{Efficiency}_{current} = \frac{I_{Load}}{I_{Load} + I_q}$ ”). The importance of power efficiency is highly application dependent and often negligible. Taylor, ¶¶58-60.

High Output Current. High output current is perhaps the most straightforward performance metric Al-Shyoukh identifies. Output current (sometimes called load current I_L) simply refers to the maximum current the voltage

regulator can provide while maintaining its output voltage within a specified voltage range. The maximum load current is commonly reported on commercial voltage regulator datasheets as it is of high practical importance when selecting (or designing) a voltage regulator. Taylor, ¶59.

It bears noting that Al-Shyoukh's proposed design could supply a maximum output load current of 200mA, which it presumably considered as "high" output current. Al-Shyoukh, Table II. But no matter how much current Al-Shyoukh meant by the term "high," it is self-evident that not all applications require the same output current. Regardless, the impact voltage regulator design choices have on output current should always be considered.

Low Quiescent Current. The third LDO performance metric Al-Shyoukh identifies is "low no-load quiescent current." Al-Shyoukh, 1. The no-load quiescent current may be described more than one way. Dr. Chen described it as follows: "'Quiescent current' typically means the nominal current that this circuit would need to run" when it is not driving a load on the output. EX2018 (Chen Tr.), 130:4-131:8. In lay terms, it can be thought of as the current needed to keep a circuit ready for use. Taylor, ¶60.

The 2013 datasheet for the LM2990 Low Dropout Regulator from Texas Instruments defines "quiescent current" as "[t]hat part of the positive input current that does not contribute to the positive load current. The regulator ground lead

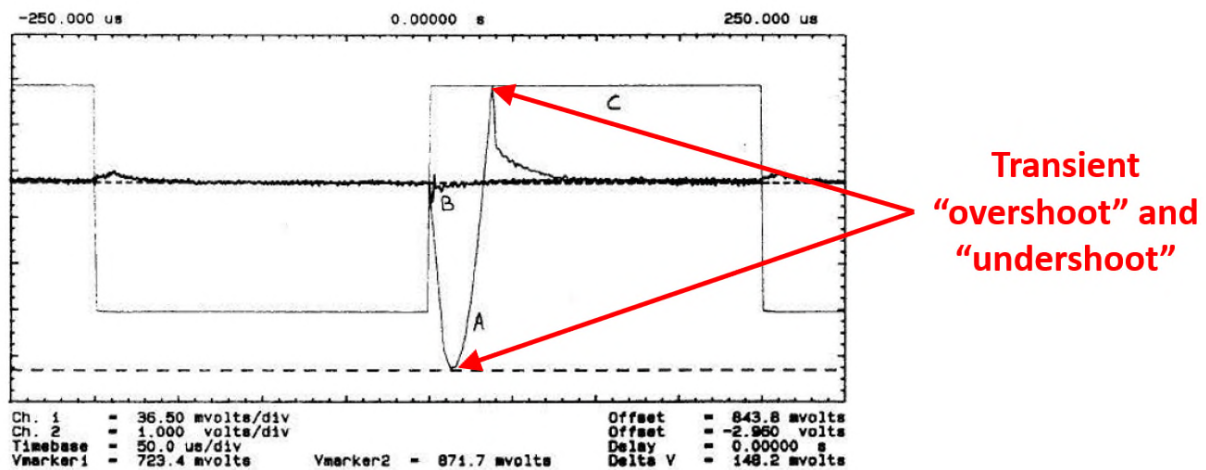
current.” EX2011, 5. Quiescent current can be determined under both no/low load conditions and fully loaded conditions. This is consistent with Al-Shyoukh Fig. 10 which reports quiescent current “under different load currents I_L . Al-Shyoukh, 8; *see also id.*, Tables I and II.

The qualifier “low” is necessarily subjective, but Al-Shyoukh repeatedly describes its regulator (which dissipates only 20 μ A of quiescent current) as achieving sufficiently low quiescent current for battery-powered applications. Al-Shyoukh, 1-4, 9-10. Similarly, the Rincon-Mora paper is titled “A Low-Voltage, **Low Quiescent Current**, Low Drop-Out Regulator.”² EX1014, Title. The Rincon-Mora paper reports its low quiescent current of only 23 μ A. EX1014, 1. Likewise, the LM2990 voltage regulator datasheet “uses new circuit design techniques to provide low dropout and low quiescent current ... The quiescent current is typically 1 mA with 1A load current.” EX2011, 1. And it shows a low-load quiescent current of 1-2mA. *See id.*, Fig. 8; *see also* EX2019, 1 (showing regulator “supply current is reduced to 30 μ A (typical)” when in shutdown mode).

Small Transients. The final performance criterion Al-Shyoukh mentions is “small output transient undershoots and overshoots.” Al-Shyoukh, 1. Al-Shyoukh explains “[g]ood load transient response with small output-voltage variation

² All emphasis added unless otherwise noted.

including overshoots and undershoots upon load switching is critical to prevent an accidental turn off or resetting of the portable device.” *Id.* The Rincon-Mora paper provides a helpful graphic (Fig. 13) illustrating this concept. EX1014, 8, Fig. 13. Curve “C” shows a load current swing on the output. Curves “A” and “B” (with and without transient boost, respectively) show output voltage variations of the voltage regulator in response to the changed load current.



EX1014, Fig. 13 (annotated). Fig. 13 shows a “large overshoot o[n] trace A” which results in an “appreciably longer” settling time compared to trace B. *Id.*, 8. Al-Shyouxh Figs. 11-13 shows similar transient waveform settling results for undershoots/overshoots under various operating conditions and loads.

Another (and perhaps more intuitive) way to think about transient over/undershoot is simply the time it takes for the voltage output to stabilize. Other things being equal, smaller undershoots/overshoots generally correlate with increased regulator operation speed responsive to changing load conditions. Taylor,

¶¶61-63.

D. Regulator System Design and Tradeoffs

As any POSITA would attest, engineering is full of trade-offs. And voltage regulator design is no exception. Indeed, Al-Shyoukh expressly recognizes you cannot analyze one performance metric in isolation without considering its impact on overall regulator/system operation. Al-Shyoukh, 1 (“These four major performance requirements of the LDO ... are, however, difficult to achieve simultaneously.”). Simply put, there are competing engineering and performance trade-offs that must be considered when designing a voltage regulator or implementing one in a larger system. Taylor, ¶¶43, 62-65.

Al-Shyoukh develops its own so-called “figure of merit,” which is an omnibus measurement that tries to capture a variety of metrics in a single number for comparing different regulators. Al-Shyoukh, 9. Indeed, his goal is to “compare the transient response of different LDOs by *evaluating the tradeoffs* between the response time Tr , the quiescent current I_q and the maximum load current $I_{L,max}$.” *Id.* The Rincon-Mora paper explains another tradeoff: “Further limits to low quiescent current arise from the transient requirements of the regulator, namely, the permissible output voltage variation in response to a maximum load-current step swing.” EX1014, 2.

At deposition, Dr. Chen testified that “when you decide the circuiting [sic]

system, there are just so many consideration[s] to consider, right. It's not just in one single angle on this biasing of the regulators or whatever the circuit that you provide. Also, there's also part of the SOC that you need to consider. So typically that would need to be considered jointly.” EX2018, 263:6-16.

In addition to impacts on the metrics Al-Shyoukh lists, when deciding on a voltage regulator implementation/architecture (or even selecting a commercial part), a POSITA would need to consider circuit size, speed, power consumption, application usage, cost, longevity, operating environment and conditions, part lifetime, development time and complexity, and other factors too numerous to mention. Taylor, ¶63; EX1014, 1 (“financial considerations also require” consideration). For example, a USB voltage regulator must comply with USB industry standards regarding operating speeds and specific power supply voltage levels and current requirements. Taylor, ¶64. In summary, one cannot simply pick one performance criterion and myopically focus on that parameter without considering its impact on the overall regulator/system in which it will be used. *Id.*, ¶63.

IV. THE '074 PATENT

A. '074 Patent Summary (Taylor, ¶¶72-81)

The '074 patent is titled “USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of

External Capacitor.” EX1001, Title. The application resulting in the ’074 patent was filed March 11, 2014, and claims priority to a provisional application filed March 14, 2013. *Id.*

The ’074 patent “relates to USB voltage regulators, and, more particularly, to a USB voltage regulator having a current buffer to reduce compensation capacitor size.” *Id.*, 1:17-19. This allows for “a wide range of external compensation capacitor ESR [equivalent series resistance] values” on the voltage regulator output. *Id.*, 1:20-21. The specification explains that “[t]he external capacitor may have very different ESR (equivalent series resistance) values ranging from a few milliohms to tens of ohms” in USB applications. *Id.*, 3:22-28.

To support a wide range of load impedances (*e.g.*, in USB applications), the ’074 patent explains “a need exists to push the gate pole of the last stage PMOS power transistor to a higher frequency.” *Id.* To achieve this, the ’074 patent discloses a voltage regulator with a “large gm (transconductance) current driver (low impedance current buffer amplifier) added between a first stage operation amplifier (OpAmp) and a last stage power transistor.” *Id.*, 3:29-34. This approach broadens “the working range of the external load capacitance from about 0.4 microfarads to about 4.7 microfarads.” *Id.*, 3:34-41.

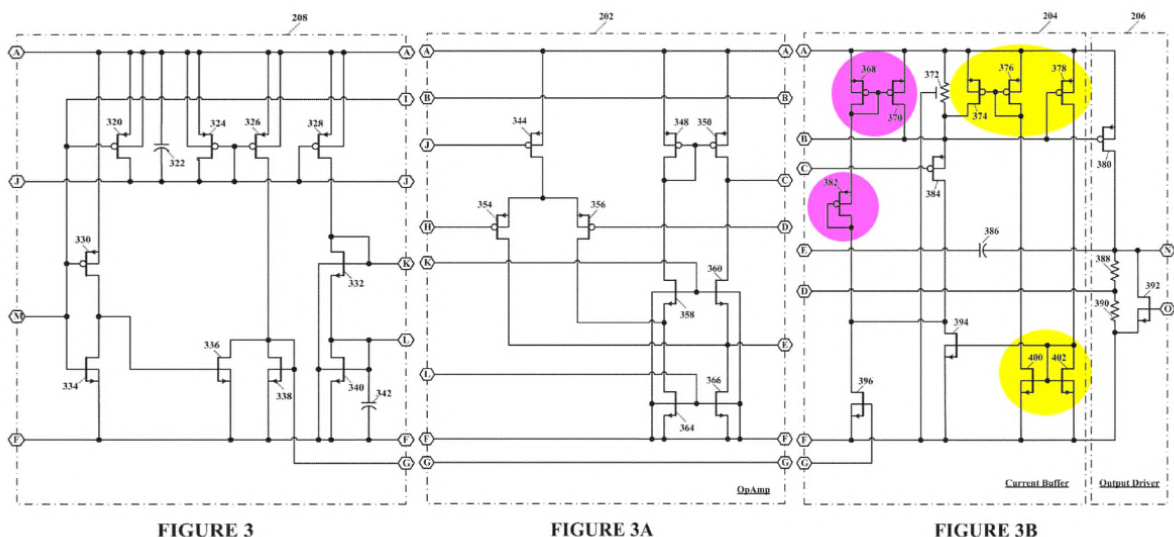
As noted above, increasing transconductance (*viz.*, current output as a function of changing input voltage) is key to enabling a wider range of capacitors on the

output load because increased transconductance allows the voltage regulator to respond more quickly and easily to changing load conditions. The '074 patent discloses two different ways of increasing transconductance. One way is what the patent refers to as “gm-boost.” *See, e.g. id.*, 3:64-65, 2;1-9 (“a gm-boost circuit may be coupled to the current buffer driver. ... the gm-boost circuit increases the current buffer driver input impedance. ... [T]he gm-boost circuit enables the current buffer driver to have a large gm value.”). The gm-boost circuit “provide[s] a gm-boost technique that will increase the impedance value of the current buffer driver 204 with the help of the current feedback 210 which may sense the current change at the output of the output driver 206.” *Id.*, 4:15-20. The gm-boost technique relies exclusively on output current feedback. *Id.* Notably, Rincon-Mora uses a similar term to describe its operation in this regard. Rincon-Mora, Title (“Low-dropout Voltage Regulator Incorporating a Current Efficient ***Transient Response Boost Circuit***”).

The second mechanism the '074 patent discloses for increasing transconductance is what claim 1 and the specification call gm-enhancement, a technique that does ***not*** rely on output current feedback. *See* EX1001, 1:60-62 (“[A] voltage regulator may comprise: an operational amplifier; a ***gm enhanced*** current buffer driver”). This is a different and independent approach from gm-boost (recited separately in claim 1) and is discussed at col. 5:8-49. The '074 patent’s gm-boost

and gm-enhancement techniques are complementary to one another and additive. Taylor, ¶¶75, 87, 66-71. As such, employing both circuits beneficially increases the transconductance more than either technique alone could. *Id.*

The separate gm-boost and gm-enhancement circuits are most easily seen in Figs. 3, 3A, and 3B. These figures collectively illustrate “a schematic diagram of a folded-cascode amplifier having bias, gm-boost, current driver and current feedback circuits.” *Id.*, 2:57-60. Because the figures are intended to be viewed “in combination” (*id.*), they will be referred to hereafter as “Fig. 3,” unless necessary to be more specific. The gm-boost circuitry is highlighted in yellow, and the gm-enhancement circuitry in pink. As shown, the gm-boost circuitry relies on current feedback from output buffer 380. In contrast, the gm-enhancement circuitry in pink does not. While both techniques serve to increase the gm of transistor 384, they do so in fundamentally different ways. One (gm-boost) acts to increase gm by adding current through transistor 384, while the other (gm-enhancement) increases gm by steering current around transistor 384. Taylor, ¶¶75, 87, 66-71.



EX1001, Figs. 3, 3A, and 3B (annotated).³

Another aspect of the '074 patent has to do with power consumption and efficiency. “[A]ccording to various embodiments, the voltage regulator, e.g., USB voltage regulator, may consume less power by, for example but is not limited to, using low-drop out (LDO) voltage regulator circuit designs.” *Id.*, 3:44-49. In this regard, for example, the '074 patent discloses that “an enable/disable function may be provided to enable/disable the biasing circuit for reducing standby current.” *Id.*, 2:9-11.

³ One point that bears noting in Fig. 3 is that block 208 is identified as biasing circuitry. EX1001, 4:43-44. This is correct, but is only part of the claimed **biasing circuit** in claim 1, which the claim specifies performs a particular function.

B. '074 File History

The '074 patent underwent a relatively typical prosecution, with two IDS submissions and two Office Actions. In an August 31, 2015 Office Action, the Examiner rejected claims 1-4, 7-17, and 19-20 as anticipated by or obvious over U.S. Pat. 6,246,221 (Xi, EX2004) and U.S. Pub. 2013/0241505 (Chang). EX2005, 67-75. But the examiner indicated original dependent claims 5, 6, and 18 would be allowable if rewritten in independent form. *Id.*, 74.

In a November 24, 2015 Office Action Response, the applicant traversed the rejection, distinguishing Xi because it lacked the claimed “current buffer driver” limitation. *Id.*, 90-99 (emphasis is original). The Examiner did not maintain the Xi rejection. *Id.*, 105-114. Instead, in a second Office Action dated March 4, 2016, the Examiner rejected claims 1-5, 7-17, and 20 as anticipated (and claim 19 as obvious) over Al-Shyoukh. *Id.*, 107-111. The Examiner also stated claims 6 and 18 would be allowable if rewritten in independent form. *Id.*, 112. In particular, regarding claim 6, the Examiner stated the prior art lacks “***an enable/disable function to enable/disable the biasing circuit for reducing standby current.***” *Id.* Thus, the “enable/disable ...” limitation for the “biasing circuitry” was the reason for allowance. *See id.*, 140.

Without conceding the propriety of the Al-Shyoukh rejections, in a June 6, 2016 Office Action Response, the applicant amended claim 1 to include the

limitations of claim 6 (and intervening claim 5). *Id.*, 126-131.

During prosecution, the applicant submitted two IDS statements identifying various prior art references, both of which the Examiner considered and signed. *See id.*, 45 (IDS submission), 69 (Examiner consideration), 78 (Examiner signature), 164 (IDS submission), 220 (Examiner signature). The '074 patent issued October 18, 2016.

V. CLAIM CONSTRUCTION

In an IPR, claim terms are construed under *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc) and its progeny. The Board, however, only construes claim terms when necessary (and to the extent necessary) to resolve the controversy. *See, e.g., Toyota Motor Corp. v. Cellport Sys., Inc.*, No. IPR2015-00633, Paper No. 11 at 16 (P.T.A.B. Aug. 14, 2015).

On July 25, 2024, the Delaware federal court issued a *Markman* order construing three terms from the '074 patent. *See* EX3001. For purposes of this IPR proceeding, PO applies the district court's ruling that element 1[d] (**an enable/disable function to enable/disable the biasing circuit for reducing standby current**) is not a means-plus-function term. EX3001, 9. The remaining two terms construed by the district court (which affect only dependent claims 4, 8, and 9) are not at issue in this POR. *Id.* 12-17.

The **gm-boost** and **gm-enhanced** limitations (elements 1[c] and 1[d],

respectively) are presumed to be different requirements and don't require explicit construction. *See, e.g., CAE Screenplates, Inc. v. Heinrich Fiedler GmbH & Co. KG*, 224 F.3d 1308, 1317 (Fed. Cir. 2000) ("we must presume that the use of these different terms in the claims connotes different meanings"); *Chi. Bd. Options Exch., Inc. v. Int'l Sec. Exch., LLC*, 677 F.3d 1361, 1369 (Fed. Cir. 2012) (similar).

But to the extent Petitioner disputes the former point, the specification confirms they are distinct requirements achieved through different circuit techniques. *See* EX1001, Fig. 3; §IV.A (showing different transistors for each technique); Taylor, ¶¶84-87, 66-71.

Gm-boost. As noted previously, the '074 patent uses similar "boost" terminology as Rincon-Mora to describe dynamically controlling the current through the source follower buffer so that g_m is proportional to the voltage regulator's output current. Taylor, ¶¶70, 84-86. Rincon-Mora refers to this circuit technique as both a "transient response boost circuit" and a "transient boost circuit." Rincon-Mora, Fig. 3, 1:10-17, 2:57-64. In like manner the '074 patent uses calls this approach " g_m -boost," stating: "The **gm-boost circuit 218** may provide a **gm-boost technique** that will increase the impedance value of the current buffer driver 204 with the help of the current feedback 210 which may sense the current change at the output of the output driver 206." Ex., 1001, 4:15-20.

Gm-enhancement. As discussed in §IV.A, the '074 patent discloses multiple

different circuit techniques for raising the effective g_m of a source follower. See also Taylor, ¶¶66-71, 75-81. Fig. 3 of the '074 patent—which Petitioner repeatedly relies on throughout its analysis to show claim elements are met—shows two different circuit techniques are used: one for *gm-boost* and another for *gm-enhance[ment]*. In particular, as shown in Fig. 3B below, a current buffer 204 that provides a g_m greater than that provided by source follower 384, around which the current buffer is based. Taylor, ¶¶75, 78, 81, 85-86.

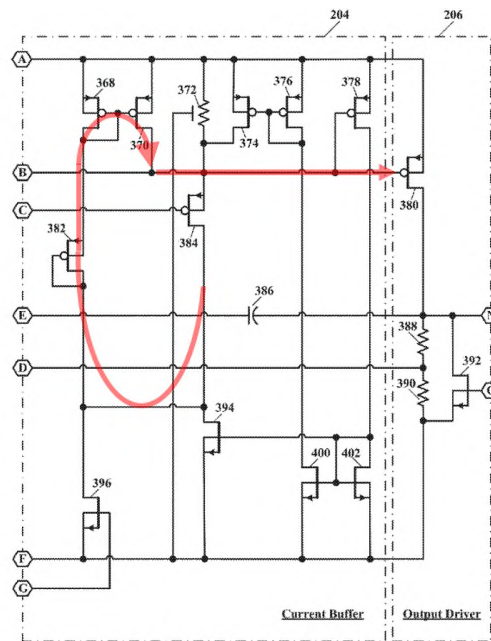


FIGURE 3B

EX1001, Fig. 3B (annotated to show g_m -enhancement).

If the voltage on node C rises, the current through source follower 384 is reduced (because it is a PMOS transistor), causing the excess bias current to be redirected through current mirror 368/370 into node B (viz., the gate capacitance of the power output transistor 380). Taylor, ¶86. Where PMOS transistors 368 and

370 are the same size, the redirected current provides additional gm equal to that of source follower 384, doubling the overall gm of the circuit. *Id.* Sizing PMOS transistor 370 to be larger than transistor 368 will cause the gm to be further enhanced. *Id.* If the voltage on node C drops, transistor 384 sources more current because it is a PMOS device and its Vgs increased. *Id.* This, in turn, enhances gm because some current previously flowing through transistor 368 now flows through 384 to account for the increased current through transistor 384. *Id.* This is “gm enhancement” to which element 1[b] refers, and is not the same as “gm-boost” (which employs a different mechanism). *Id.*, ¶¶83-87, 75-81, 66-71. In other words, gm-boost changes the overall *magnitude* of the standing current, whereas gm-enhancement changes the *allocation* of where the current is deployed. *See, e.g., Id.*, ¶86.

As Dr. Taylor explains, the combined effects of *gm-boost* and *gm-enhance[ment]* are cumulatively greater than the effect either could achieve alone. Taylor, ¶41. Equating “gm enhancement” with “gm-boost” would negate this cumulative effect, and improperly conflates the analysis of elements 1[b] and 1[c] into a singular requirement. *Id.*, ¶¶87, 109. But that is precisely what Petitioner and its expert do. *See* §§VII.A.1 (Rincon-Mora analysis) and VII.A.2 (Al-Shyoukh analysis).

VI. ASSERTED PRIOR ART REFERENCES

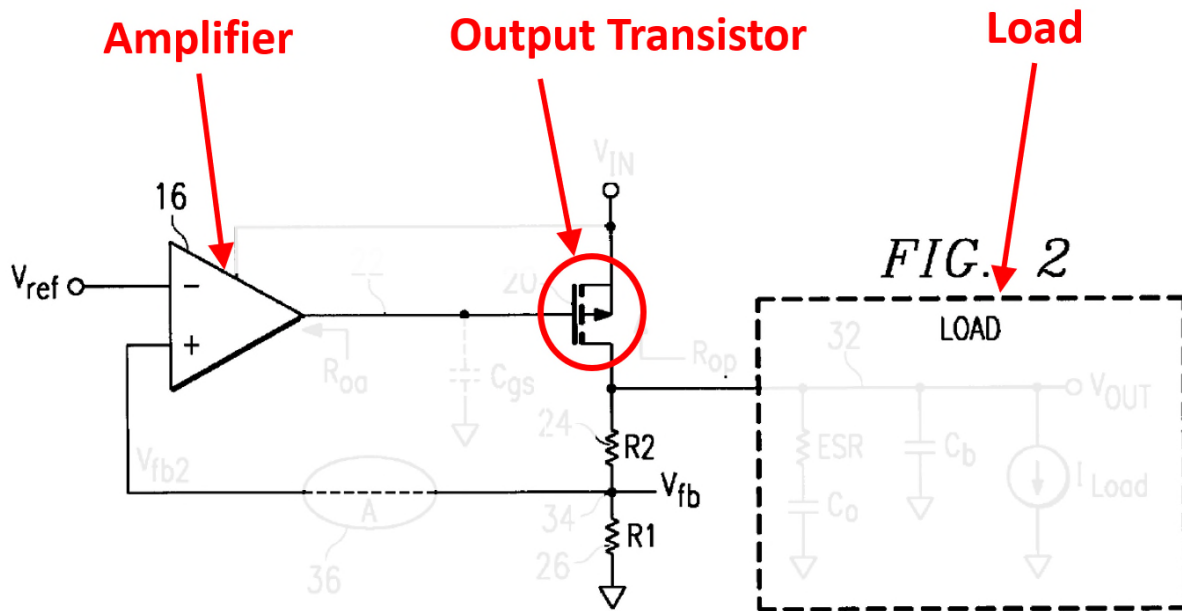
Petitioner relies on several references. For example, in Ground 2, Petitioner relies on combining the Rincon-Mora patent (EX1013), the Rincon-Mora paper (EX1014), Al-Shyoukh (EX1004), Ivanov (EX1005), and Stanescu (EX1006). *See* Pet., 53. Only the main references at issue are summarized here.

A. Rincon-Mora References (Taylor, ¶¶88-91)

1. Rincon-Mora Patent

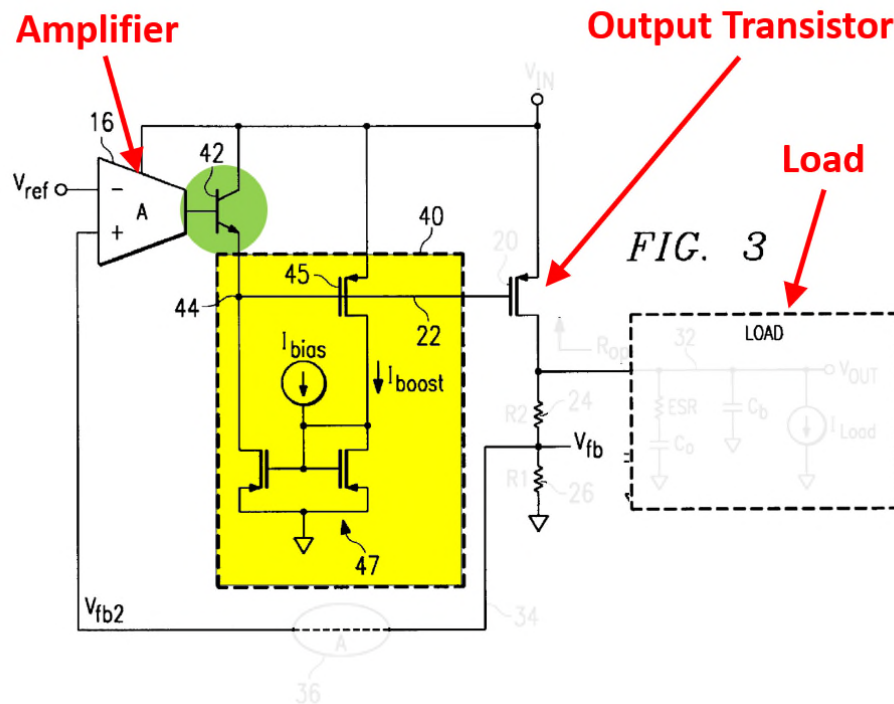
The Rincon-Mora patent (EX1013) is titled “Low-dropout Voltage Regulator Incorporating a Current Efficient Transient Response Boost Circuit.” Rincon-Mora, 1. The abstract describes Rincon-Mora as disclosing “[a]n improved low-dropout (‘LDO’) voltage regulator [that] incorporates a transient response boost circuit which is added to the slew-rate limited node at the control terminal of the LDO voltage regulator output transistor and provides improved transient response performance to the application of various load current step stimuli while requiring no standby or quiescent current during zero output current load conditions.” This is an apt description.

Rincon-Mora provides “a partial, simplified schematic illustration of selected portions of the output section of a conventional LDO voltage regulator” in Fig. 2, reproduced with annotations below. Rincon-Mora, 2:54-56.



Id., Fig. 2 (annotated). This circuit operates in the conventional manner described in §III.B.

Rincon-Mora’s improvement is illustrated in Fig. 3, which shows “a partial, simplified schematic illustration of the output section of an LDO voltage regulator in accordance with the present invention including one particular embodiment of a transient boost circuit.” Rincon-Mora, 2:57-60. It includes a similar amplifier, output transistor, and load as Fig. 2. But Fig. 3 adds “transient boost circuit 40” (highlighted in yellow) and “buffer 42” (highlighted in green). *Id.*, 4:30-40.



Id., Fig. 3 (annotated). Nothing more (including enable/disable functionality) is added. Notably, there is no mechanism for gm-enhancement. Rather, the transient **boost circuit 40** and buffer 42 work together to “improve[] transient response performance.” *Id.*, Abstract.

Rincon-Mora explains the “transient boost circuit ... **is operative to supply current to the control terminal of the output switching device** in response to a current load placed on the voltage output of the LDO voltage regulator.” Rincon-Mora, 2:33-39. In other words, the transient boost circuit can quickly turn on/off output transistor 20 (which provides current to the load) by rapidly charging/discharging the output transistor gate capacitance.

Rincon-Mora’s abstract further states the transient boost circuit not only

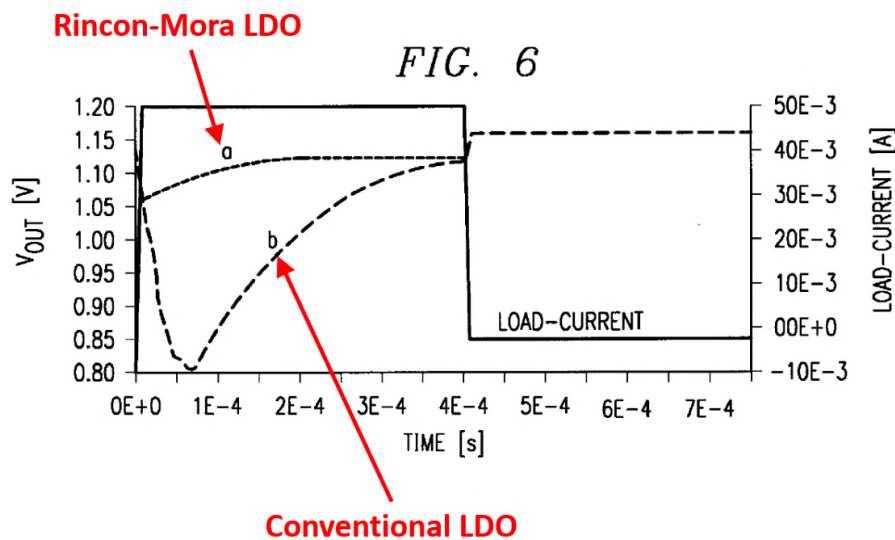
“provides improved transient response performance,” but does so “while requiring ***no standby or quiescent current*** during zero output current load conditions.”

Rincon-Mora, Abstract. This concept is reiterated throughout the reference, including the title: “Low-Dropout Voltage Regulator Incorporating a ***Current Efficient*** Transient Response Boost Circuit.” And the specification’s first paragraph repeats: “[T]he present invention relates to a ***current efficient LDO*** voltage regulator ... [that] ***requires no standby current during zero output current load conditions.***” *Id.*, 1:12-17.

Rincon-Mora readily acknowledges “***some LDO voltage regulators incorporate a separate enable terminal*** to switch the device into a standby mode of operation to minimize power consumption.” Rincon-Mora, 1:24-29. But the reason Rincon-Mora’s LDO does not include an enable/disable feature is because it is “current efficient” and “requires no standby current during zero output current load conditions.” *Id.*, 1:12-17; *see also id.*, 1:48-52 (criticizing “known techniques result in circuit designs that ... require more quiescent current flow than is desired during zero load current conditions.”); 1:66-2:3 (describing “current efficient design”), 2:4-9 (“requires no standby current during zero output current load conditions.”). Rincon-Mora explains its embodiments “supply current to the slew-rate limited node only upon demand.” *Id.* Rincon-Mora explains how its design achieves these results: “at $I_{Load}=0$ Amps, ... I_{boost} is zero because the aspect ratio of the PMOS

transistor 45 forming a portion of the transient boost circuit 40 is much less than that of the output PMOS transistor 20, ***thus yielding low quiescent current.*** *Id.*, 4:41-48. Additionally, “due to the provision of a relatively high mirror ratio, the current sourced by transistor 45 is negligible and it consumes no power.” *Id.*, 5:9-11. In other words, Rincon-Mora unequivocally declared victory over the prior art problem of excessive quiescent current, and thus had no need for an enable/disable feature.

Rincon-Mora also touts its fast operation. Rincon-Mora, 6:43-49 (“This time can be on the order of 1 to 8 μ seconds which is lower than in the case of a similarly biased embodiment without a transient boost circuit (50 μ s) thereby achieving a factor improvement of 6 to 10.”). Rincon-Mora illustrates this improvement in Fig. 6, comparing the settling time for a conventional voltage regulator (curve “b”) with Rincon-Mora’s voltage regulator (curve “a”). *Id.*, Fig. 6, 6:15-49.



Id., Fig. 6 (annotated). The Rincon-Mora regulator stabilizes at the desired output

voltage far more quickly than the conventional LDO, while simultaneously exhibiting smaller voltage transients.

2. Rincon-Mora Paper

The Rincon-Mora paper (EX1014), by the same author, is titled “A Low-Voltage, Low Quiescent Current, Low Drop-Out Regulator.” EX1014, 1. Petitioner asserts the Rincon-Mora patent and Rincon-Mora paper “discloses substantially the same LDO,” and thus would have been combined. Pet., 56; EX1002, ¶137.

Like the Rincon-Mora patent, the Rincon-Mora paper touts its LDO regulator’s “low quiescent current” and “current efficien[cy].” See EX1014, 1. Indeed, the title is “A Low-Voltage, **Low Quiescent Current**, Low Drop-Out Regulator.” The abstract explains “[t]his paper discusses some techniques that enable the practical realizations of **low quiescent current LDO’s** at low voltages.” *Id.* The Rincon-Mora paper explains that “[d]uring low load-current conditions, the current fed back (I_{boost}) is negligible, thereby yielding high overall current efficiency and not aggravating battery life.” *Id.*, 2. It further highlights “the biasing conditions for the case of zero load-current can be designed to utilize a minimum amount of current, which yields maximum current efficiency and prolonged battery life.” *Id.*

The Rincon-Mora paper recognizes “[l]ow quiescent current flow is especially important in portable products where the total current drain determines battery life.” EX1014, 8. But continues to say its improvements “do[] not come at the expense of

additional quiescent current flow during zero load-current conditions. Consequently, current efficiency and battery life are maximized.” *Id.*, 4; *see also id.*, 8 (“Two significant contributions, current efficient buffer and current boosted pass device, made the low-voltage design viable for battery powered circuits.”); *id.* (design has “low component count and low overall ground current.”).

Thus, like the Rincon-Mora patent, the Rincon-Mora paper discourages anyone from adding enable/disable functionality, even for battery powered applications. Taylor, ¶¶89, 130-138. Unlike the Rincon-Mora patent which does not quantify its quiescent current, the Rincon-Mora paper does provide quantitative data, stating it has “zero-load quiescent current flow of 23μA.” EX1014, 1; *see also id.*, Fig. 11, Table 1, 9 (showing 23μA quiescent current). Thus, the references collectively teach that 23μA of quiescent current is tantamount to “no standby or quiescent current during zero output current load conditions.” Rincon-Mora patent, Abstract. Indeed, Dr. Chen testified the Rincon-Mora patent disclosure applies to the Rincon-Mora paper. *See* EX2018,124:17-22 (“Would it be fair to say that in your view the disclosure in the Rincon-Mora patent applies to the Rincon-Mora paper as well? A. Yes. That’s why I see them as one unit or one group.”).

The Rincon-Mora paper also explains that “[t]he settling time of the LDO response without M_{ps} [*i.e.*, a conventional LDO] is appreciably longer, [as] illustrated by the large overshoot of trace A.” EX1014, 8.

B. Al-Shyoukh (Taylor, ¶¶92-97)

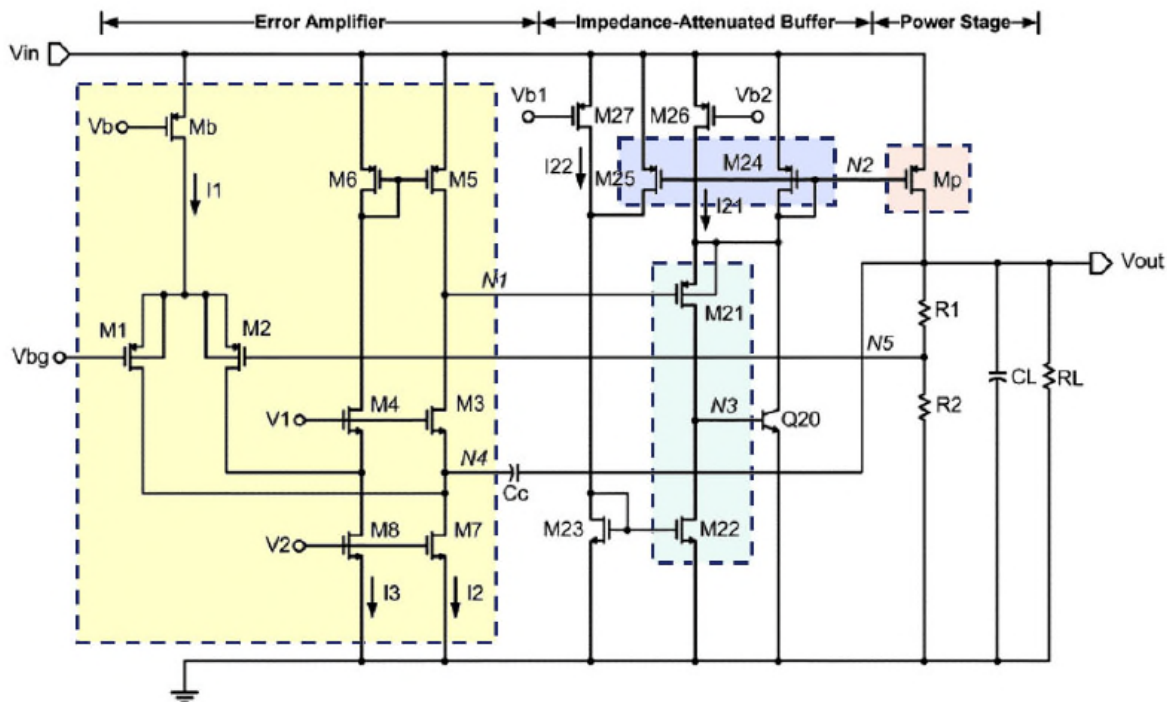
Al-Shyoukh (EX1004) is titled “A Transient-Enhanced Low-Quiescent Current Low-Dropout Regulator With Buffer Impedance Attenuation.” Al-Shyoukh, 1. This is the same Al-Shyoukh reference overcome during prosecution by adding the enable/disable limitation to claim 1. *See* §IV.B. As with the Rincon-Mora paper, Al-Shyoukh’s title touts its “Low Quiescent Current.” Al-Shyoukh, Title. By comparison, Al-Shyoukh’s quiescent current is 20μA (*see, e.g., id.*, Table II) compared to 23μA for Rincon-Mora (*see* §VI.A.2). Given that the Rincon-Mora patent describes this as “no standby or quiescent current” (EX1013, Abstract), it is unsurprising that Al-Shyoukh does **not** disclose an enable/disable function.

Indeed, there is a close linkage between Rincon-Mora and Al-Shyoukh. The first reference Al-Shyoukh cites and discusses is the Rincon-Mora paper. Al-Shyoukh, 1, 10 (citing reference [1]). And the first thing it is cited for is the proposition of minimizing “no-load quiescent current of the LDO.” *Id.*, 1. Al-Shyoukh notes that “[Rincon-Mora’s] reported LDO dissipates low quiescent current.” *Id.* Al-Shyoukh critiques Rincon-Mora’s regulator for its limited 50mA maximum current output, but **not** for its quiescent current. *Id.*

Al-Shyoukh then describes its voltage regulator design, culminating in Fig. 8 (relied on throughout the Petition) which sources 200mA of current. Al-SHYoukh, Fig. 8, 7 (“The schematic of the proposed LDO is shown in Fig. 8.”), Table II

(reporting 200mA current). As Petitioner admits, “Al-Shyoukh discloses an LDO suitable for ‘battery-powered portable devices such as cellular phones and PDAs in order to reduce the standby power and prolong the battery runtime.’” Pet., 10 (quoting Al-Shyoukh, 1). Much of Al-Shyoukh’s improved output current is attributable to a 0.35µm technology process instead of 2µm technology used by Rincon-Mora. Al-Shyoukh, Table II (row 1); Taylor, ¶95.

Petitioner provides a color-coded version of Fig. 8 to show key components. Pet., 11. As Petitioner explains, “[t]his shows in yellow a single-stage folded cascode error amplifier,” and “the output of the pass device [M_p] that supplies the output voltage ([is] in red).” *Id.*, 12. Petitioner notes that Al-Shyoukh has a “buffer[] driver, which is shown in green.” *Id.* Petitioner further states “[t]he voltage regulator further includes a current feedback circuit comprising transistors M₂₄ and M₂₅,” which Petitioner highlighted in blue. *Id.*; see also *id.*, 30 (“current feedback circuit (blue)”).



Id., 11 (reproducing Al-Shyoukh Fig. 8, annotated by Petitioner).

Regarding the “buffer[] driver” (in green above), Al-Shyoukh explains that “to further improve LDO performances, buffer impedance attenuation technique (BIA) is first proposed to realize an intermediate stage for driving the pMOS pass device.” Al-Shyoukh, 2. This circuit operates similarly to Rincon-Mora’s “boost” circuit, and achieves the same effect. Taylor, ¶92. As Al-Shyoukh explains, “[t]he BIA technique thus allows the LDO to dissipate low quiescent current.” Al-Shyoukh, 2; *see also id.*, 3 (similar).

Al-Shyoukh explains “the use of a pMOS transistor [for M₂₁] to implement the source-follower in the proposed buffer is extremely critical to minimize the quiescent current at no-load condition.” Al-Shyoukh, 7. “Under no-load condition,

the pass device M_p is almost turned off.” *Id.* Al-Shyoukh provides measured results, touting that its “LDO consumes small quiescent current of 20 μ A under no-load conditions.” *Id.*, 10; *see also id.*, Table I. Al-Shyoukh compares its regulator with others in Table II.

TABLE II
PERFORMANCE COMPARISON WITH PREVIOUSLY REPORTED LDOs

	1998 [1]	2000 [3]	2003 [4]	2004 [5]	2005 [17]	This Work
Technology (μ m)	2.0	1.0	0.6	0.5	0.09	0.35
V_{do} (V)	0.3	N.A.	0.2	N.A.	0.3	0.2
$I_{L,max}$ (mA)	50	200	100	160	100	200
I_q (mA)	0.023	0.03	0.038	0.025	6	0.02
Current Efficiency at $I_{L,max}$ (%)	99.5	N.A.	N.A.	N.A.	94.3	99.8
ΔV_{out} (mV)	19	220	130	200	90	54
T_r (μ s)	1.8	1.1	2	2.75	0.00054	0.27
C_L (μ F)	4.7	1	10	2.2	0.00060	1
ESR Zero Required	No	Yes	Yes	No	No	No
FOM (ns)	8.2	0.165	4.9	0.43	0.032	0.027

Rincon-Mora

Al-Shyoukh

Id., Table II (annotated). Al-Shyoukh has the lowest I_q (quiescent current) of 20 μ A (*i.e.*, 0.02mA), followed closely by Rincon-Mora with 23 μ A (*i.e.*, 0.023mA).

Al-Shyoukh also touts that its full-load quiescent current is so low that its regulator design has “worst-case current efficiency of 99.8%.” Al-Shyoukh., 8. Because “[c]urrent efficiency above 99% is critical if the LDO is designed for

portable applications as the current efficiency determines the battery lifetime,” Al-Shyoukh’s design is well-suited for portable battery powered applications. *Id.*, 9; *see also id.*, 1 (“This paper present a low-dropout regulator (LDO) for portable applications ... without dissipating large quiescent current.”). Consistent with these results and assertions, Al-Shyoukh does not disclose enable/disable functionality.

Like Rincon-Mora, Al-Shyoukh touts its “good transient settling behavior and small output-voltage variation even if a small output capacitor is used.” Al-Shyoukh, 2; *see also id.*, 9-10. In other words, Al-Shyoukh is concerned with how quickly the voltage undershoots/overshoots on its output settle within required performance parameters. Taylor, ¶¶96-97. With a 1 μ F capacitive output load, Al-Shyoukh reports “[t]he total output undershoots and overshoots are less than 15 mV above and below the steady-state V_{out} , which amounts to less than 1% of the output voltage.” Al-Shyoukh, 8. In other words, Al-Shyoukh’s regulator is intended to be fast. Taylor, ¶¶96-97.

C. Ivanov (Taylor, ¶¶98-103)

Ivanov (EX1005) “relates to a quick turn-on disable/enable bias control circuit for use in conjunction with high speed CMOS amplifiers, particularly CMOS amplifiers used in high speed video multiplexing applications.” EX1005, 1:8-11. The Petition relies on Ivanov Fig. 1 (*see, e.g.*, Pet., 24), which includes substantial overhead circuitry. Indeed, in some ways, Ivanov requires more circuitry than the

active components in the Rincon-Mora and Al-Shyoukh voltage regulators. Nevertheless, Ivanov's core function is quite straightforward—it turns on/off biasing transistor M22. EX1005, 2:15-19. But it has nothing to do with—and is completely silent on—*set[ting] a biasing ratio for gm-boost of the current buffer driver*, as required by '074 patent claim 1. Taylor, ¶¶98, 103. In other words, Ivanov exclusively concerns “reference generation” (*i.e.*, generating a reference current/voltage to place active circuitry in a ready state), not with the functionality, design, transconductance, or operation of the active circuitry itself. Taylor, ¶¶98-103.

“ordinarily would simply be a buffer circuit or a Schmitt trigger circuit having its output connected to conductor 8 and its input connected to an external conductor 80 on which ***a user applies an external control signal to disable/enable bias control circuit.***” EX1005, 4:20-25; *see also id.*, 2:59-62; 3:45-49. Ivanov leaves the “user” the task of determining when/whether to actually enable/disable the circuit. Taylor, ¶98.

Ivanov explains how Fig. 1 operates to turn off M22 (*i.e.*, disabled state, EX1005, 5:18-6:6) and turn on M22 (*id.*, 6:7-27). Notably, the $V_{SHUTDOWN}$ control signal on node 8 is active high, meaning that when $V_{SHUTDOWN}$ is driven high, M22 will be enabled (*i.e.*, turned on). *Id.*, 6:7-11. And when $V_{SHUTDOWN}$ is driven low, M22 will be disabled (*i.e.*, turned off). *Id.*, 5:19-25. When $V_{SHUTDOWN}$ is low, PMOS transistor M11 is on which passes a high voltage to the gate of NMOS transistor M17. *Id.*, 5:24-30. This turns M17 on, which dissipates “approximately 0.1 to 5 microamperes” of current. *Id.*, 5:39-41.

While Ivanov purports to provide a “quick turn-on disable/enable bias control circuit” (*id.*, Title), no matter how fast it operates it still introduces additional delay into any circuit that would otherwise be enabled. Taylor, ¶98. The techniques Ivanov employs (*e.g.*, trickle charge circuit) to reduce delay requires extra circuitry and power consumption. *Id.*, ¶¶100-103. A POSITA would understand the time required for Ivanov’s circuit to supply the desired bias voltage depends on how long

Ivanov’s circuit has been in standby—the longer Ivanov has been in standby, the more time is required to exit standby. *Id.*, ¶101. This is because the voltage on the compensation capacitor C_{ϕ} in standby mode is determined by the trickle charge circuit design which is set irrespective of the desired voltage for a particular application. *Id.* Other factors (like temperature, etc.) also impact turn-on time. *Id.*

VII. THE PETITION FAILS TO ESTABLISH ANY CLAIM IS OBVIOUS

The ’074 patent has 18 claims, but only 1 independent claim. See EX1001, cls. 1-18. Petitioner fails to establish independent claim 1 is unpatentable for at least three independent reasons. For the same reasons, Petitioner has failed to establish that any dependent claims are unpatentable. See, e.g., *Callaway Golf Co. v. Acushnet Co.*, 576 F.3d 1331, 1344 (Fed. Cir. 2009).

A. Petitioner Fails to Show the “gm-enhance[ment]” Limitation (Taylor, ¶¶104-111)

Element 1[b] requires ***a gm enhanced current buffer driver***. Element 1[c] separately requires ***a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver***. These are distinct claim limitations which must both be satisfied. See §§V, IV.A. Petitioner and its expert fail to show that Rincon-Mora or Al-Shyoukh satisfy the ***gm enhance[ment]*** limitation of element 1[b] (*viz.*, current *allocation* as opposed to *magnitude*). Petitioner’s fundamental problem is that it conflates two separate and distinct claim limitations.

While the Petition recites the claim elements under separate headings, the substance of its analysis (and the underlying circuitry it points to) is substantially the same for both elements, essentially collapsing the two requirements into one. This is true for both the Rincon-Mora and Al-Shyoukh grounds. See Pet., 16-21 (for Al-Shyoukh) and 58-62 (for Rincon-Mora).

1. Rincon-Mora

As discussed in §§V.A.1 and V.A.2, Rincon-Mora discloses a gm-boost circuit in Fig. 3. In summary, Rincon-Mora builds on a conventional LDO regulator (shown in Fig. 2) by adding “transient boost circuit 40” (and buffer 42) in Fig. 3 (highlight in yellow and green, respectively). See Rincon-Mora, 4:30-40.

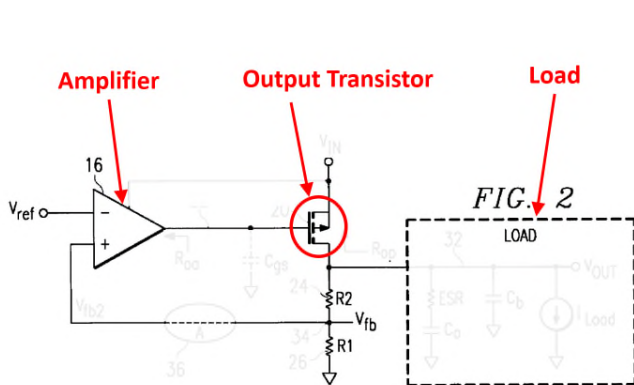


Fig. 2 (annotated)

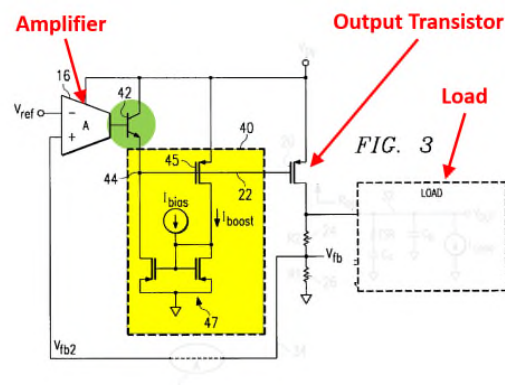


Fig. 3 (annotated)

When Petitioner analyzes element 1[c], this is what Petitioner and its expert discuss. See, e.g., Pet., 61 (citing Rincon-Mora at 3:55-62, 4:30-65, and 7:35-41, all of which discuss the “transient boost circuit”); EX1002, ¶¶145-149. For example, Petitioner’s expert states “[Rincon-Mora’s] transient response boost circuit provides a gm-boost

to the buffer driver.” EX1002, ¶145.

Rincon-Mora’s Fig. 3 contains no additional circuitry or mechanism for gm-enhancement—it simply is not there. Taylor, ¶¶105-110, 88-91. As a result, when confronted with the requirement of element 1[b] (*a gm enhanced current buffer driver*), Petitioner and its expert have no recourse other than to point back to the same thing they rely on for *gm-boost* in element 1[c], which performs no *allocation* of current. Pet., 59-62 (Rincon-Mora); *see also* EX1002, ¶¶142-144 (similar for Dr. Chen). In particular, when analyzing element 1[c], Petitioner’s argument is that “Rincon-Mora’s buffer driver is ‘gm enhanced’ because the transient boost circuit, comprising transistor 45 and current mirror 47, increases its gm.” Pet., 58. Likewise, Dr. Chen states that “[Rincon Mora] includes a current feedback system (shown in blue below) that enhances the gm of the buffer driver (green).” EX1002, ¶142. Everything Petitioner and its expert identify is part of the highlighted transient-boost circuitry above in Rincon-Mora Fig. 3. Notably, Petitioner makes no obviousness argument for element 1[c], either by way of a combination with, or modification of, Rincon-Mora.

Petitioner’s failure is perhaps nowhere more apparent than from Dr. Chen’s deposition, where he testified as follows:

Q. How is the claim[ed] gm-boost different from the claim[ed] gm enhancement? A. As I mentioned exactly on page 25, you -- because you have this feedback circuits, you have gm-boost, right, and as a

result you increase the current for that for the buffer transistors. So you enhance that gm and that's how I understand a gm enhanced. So you almost think that as outcome of that gm-boost.

EX2018, 251:9-19. In substance, Dr. Chen testified that anytime “you have gm-boost,” you necessarily also “enhance that gm.” *Id.* In his view, they are the same thing. Given another chance to explain, Dr. Chen confirmed he didn't recall any distinction between gm-boost and gm-enhancement in the '074 patent, but that it did not matter because if you have gm-boost, you also satisfy the gm-enhancement limitation:

Q. [L]ooking at claim 1 are gm enhancement and gm-boost the same thing or are they different? ... A. Sitting here, I don't recall that the '074 actually defined gm enhanced or gm-boost separately. But it's my understanding that I show in the report because you do the gm-boost, you increase the current, you know, particularly to the transistor M21, and hence you increase the gm. That's how I understand this enhanced -- or sorry, the gm enhanced buffer.

EX2018, 249:8-22. This is fatal to Petitioner's argument. Dr. Chen's testimony is equally applicable to Rincon-Mora and Al-Shyoukh, but PO separately addresses Al-Shyoukh below.

2. Al-Shyoukh

Petitioner's Al-Shyoukh analysis suffers from the same defect described above for Rincon-Mora—improperly conflating the separate **gm-boost** and **gm-**

enhance[ment] claim limitations.

When analyzing element 1[c], Petitioner asserts “Al-Shyoukh’s LDO uses a biasing circuit coupled to the buffer driver to set a voltage V_{b1} at the gate of transistor M_{27} , providing a bias current I_{22} that is mirrored across transistors M_{23} and M_{22} to set a biasing ratio for gm-boost of the current buffer driver.” Pet., 17. Similarly, Dr. Chen states “[Al-Shyoukh] boosts the gm of the buffer driver transistor M_{21} is by increasing the current at transistor M_{22} (which pulls current from M_{21}), which is in turn done by increasing current at M_{23} , which mirrors to M_{22} .” EX1002, ¶56. This is the same gm-boost technique employed by Rincon-Mora, which does not *allocate* current. Taylor, ¶¶111, 92-97.

But when analyzing the **gm-enhance[ment]** limitation of element 1[b], Petitioner and its expert again point to **gm-boost** in element 1[c]. Pet., 16-17; EX1002, ¶¶53-55 (similar for Dr. Chen). In particular, Petitioner states that “[c]entered on the driver transistor M_{21} , Al-Shyoukh’s buffer is ‘**gm enhanced**’ **because it receives a gm boost** from a current feedback circuit comprising M_{24} and M_{25} , as detailed above.” Pet., 16 (Al-Shyoukh). Likewise, for element 1[b], Dr. Chen states: “I have explained above in my summary of Al-Shyoukh how its circuit includes a current feedback system that enhances the gm of transistor M_{21} , which is the core component of the buffer driver shown in green.” EX1002, ¶53. Notably, Petitioner makes no obviousness argument for element 1[c], either by way of a

combination with, or modification of, Al-Shyoukh.

When specifically questioned about **gm-enhance[ment]** for Al-Shyoukh, Dr. Chen responded by explaining how Al-Shyoukh Fig. 8 “provide[d] the **gm-boost** to the buffer driver.” EX2018, 251:20-252:14. To make sure Dr. Chen had not misheard the question, the questioner clarified that the question was about gm-enhancement, not gm-boost:

Q. My question was not about gm-boost. It was about gm enhancement. What transistor in Al-Shyoukh Figure 8 performs gm enhancement?

A. So counsel, as I mentioned before, *the way I understand the gm enhance is the outcome of the gm-boost* because you increase the current through this M21. That’s why the gm increase, that’s why you are gm enhanced. So gm enhanced is outcome of the circuit that we built. That’s the way I understand it.

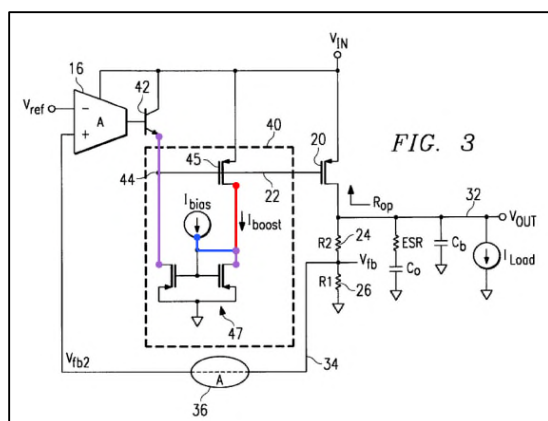
EX2018, 252:15-253:2. Dr. Chen’s response again confirms Petitioner’s mistaken premise that gm-boost and gm-enhancement are one and the same thing accomplished through the same mechanism of transistor M21 in Al-Shyoukh Fig. 8. *See id.*, 253:3-18.

As explained above, **gm-boost** and **gm-enhance[ment]** are different requirements implemented by different (but complementary) circuit techniques. Because Petitioner conflates the requirements and points to Al-Shyoukh’s gm-boost circuitry for both, Petitioner fails to show Al-Shyoukh meets element 1[c].

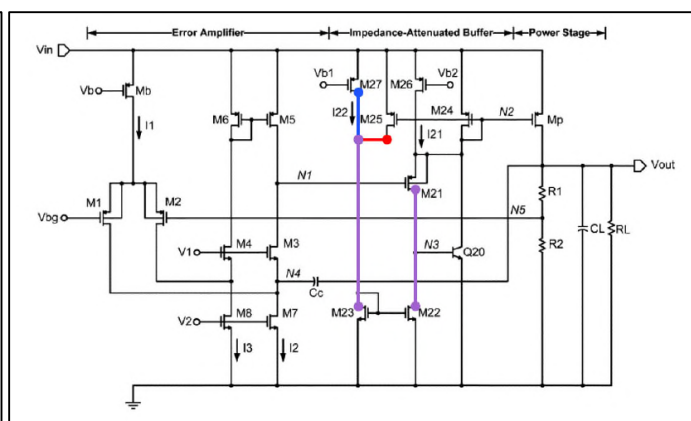
B. Petitioner Fails to Show the Claimed “biasing circuit ... [that] sets a biasing ratio for gm-boost” (Taylor, ¶¶112-124)

Claim element 1[c] requires *a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver*. Petitioner fails to establish that either Rincon-Mora or Al-Shyoukh meets this limitation. Petitioner’s error is similar for both grounds—it conflates bias circuitry (like that in Ivanov used for reference generation) that merely places the voltage regulator circuit in a state ready for operation with the claimed *biasing circuit* that must *set a biasing ratio for gm-boost of the current buffer driver*.

To begin, the claim requires a *biasing circuit*. Courts (and the Board) have repeatedly held that the term “circuit” requires actual circuitry. *See, e.g., Mass. Inst. of Tech. v. Abacus Software*, 462 F.3d 1344, 1357 (Fed. Cir. 2006) (“We conclude that the term ‘circuitry’ in claim 1 is limited to hardware.”). Rather than identify any actual circuits (*viz.*, transistors), the Petition highlights and discusses various *currents* for element 1[c], as illustrated below. *See* Pet., 59-62 (Rincon-Mora), 17-21 (Al-Shyoukh).



**Pet., 61 (Rincon-Mora)
(annotated by Petitioner)**



**Pet., 19 (Al-Shyoukh)
(annotated by Petitioner)**

This stands in contrast to other claim elements (*e.g.*, element 1[e]) where Petitioner actually highlights the circuitry it contends map to the claim element.

Another aspect of element 1[c] requires ***set[ting] a biasing ratio for gm-boost of the current buffer driver***. Dr. Chen admits that a ratio refers to the quotient between two values. EX2018, 242:24-243:23. Here, the claim itself specifies that the ratio sets ***gm-boost***. In the context of the claimed voltage regulator and the '074 patent specification, a POSITA would understand that this ratio refers to the ratio of current in the output transistor to the buffer driver. Taylor, ¶¶80, 118. Petitioner's expert (Dr. Chen) acknowledges as much. See EX1002, ¶¶145-146 (discussing the "ratio between [Rincon-Mora] transistors 20 [the output driver] and 45 [the buffer driver]"). Petitioner's problem is that the ***biasing circuit*** Petitioner relies on (for both Rincon-Mora and Al-Shyoukh) does not ***set a biasing ratio for gm-boost of the current buffer driver***.

At the outset, it is helpful to understand another flaw with Petitioner's treatment of the claimed **biasing circuit**. That term is introduced in element 1[c] (as quoted above), but is referenced again in element 1[d]: **an enable/disable function to enable/disable the biasing circuit for reducing standby current**. It is clear from the antecedent basis (**the biasing circuit**) in element 1[d], that the term is referring to the same **biasing circuit** introduced in element 1[c] (**a biasing circuit ...**).

Petitioner does not argue obviousness of element 1[c] (for either Rincon-Mora or Al-Shyoukh), but does argue obviousness for element 1[d] by combining Ivanov. See Pet., 22 (“Al-Shyoukh with Ivanov discloses 1[d].”), 62 (“Rincon-Mora’s LDO in combination with Ivanov discloses 1[d].”). Petitioner plays fast-and-loose with the **biasing circuit** requirements by invoking Ivanov for the **biasing circuit** limitation in 1[d], but not element 1[c]. See Pet., 22 (Al-Shyoukh element 1[d]), 62 (Rincon-Mora element 1[d]). Petition cannot have its cake and eat it too, by mixing-and-matching what circuitry it contends is the claimed **biasing circuit** depending on what claim element it is analyzing. Petitioner’s inconsistent positions cannot establish unpatentability.

Regardless of whether the not-shown **bias[] circuit** comes from Ivanov or not, it makes no difference since such circuitry would simply generate a reference voltage for the Rincon-Mora and Al-Shyoukh regulator circuits, which is not what the claims require. Taylor, ¶¶114, 120.

1. Rincon-Mora Ground (Taylor, ¶¶119-124)

Against this backdrop, Petitioner asked Dr. Chen at deposition to identify the claimed ***biasing circuit*** in Rincon-Mora. Dr. Chen testified as follows:

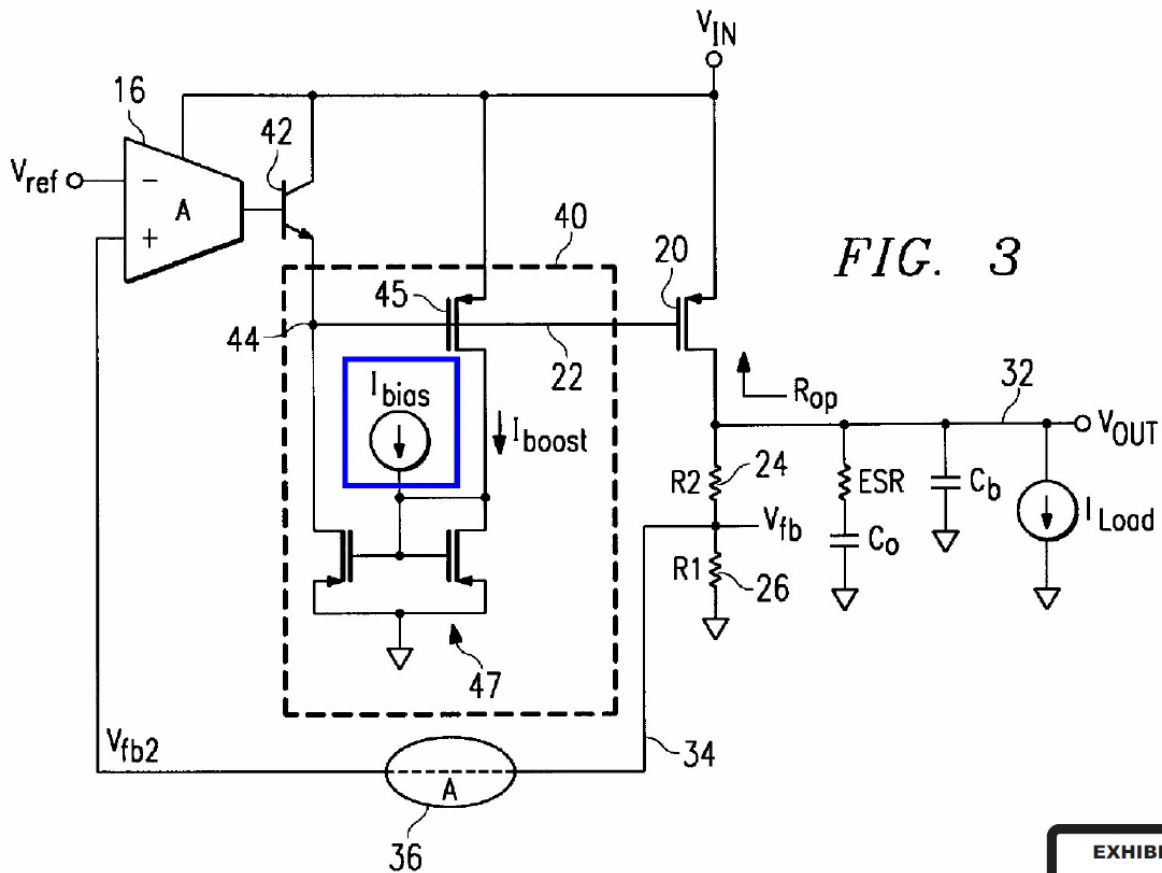
Q. What do you identify, if anything, in Rincon-Mora Figure 3 as the claimed biasing circuit that is recited in Claim Element 1C?

A. So that would be the blue box that you highlight earlier. Because you can see that bias current eventually will be coupled to the buffer driver 42. Yes.

Q. Okay. So I've placed a blue box around the I-Bias that you referenced, correct?

A. Correct.

EX2018, 213:3-14; *see also id.*, 226:1-6, 210:18-211:1, 254:1-6 (“I believe I mentioned that before. Because they do not show the biasing circuits, both Rincon-Mora and Al-Shyoukh, and that’s why I cannot make that decision or judgment to even look for those enable and disable signals.”); EX1002, ¶145 (discussing “a biasing circuit that is external to the LDO (and thus not shown in the figure”); Pet., 64 (“POSITA could have integrated *Ivanov’s biasing circuit* and its enable/disable function with Rincon-Mora’s LDO”). The blue box Dr. Chen referenced is shown in EX2014 (reproduced below) from his deposition and is simply a current source. *See* EX2018, 214:1-9.



EX2014 (annotated version for Rincon-Mora Fig. 3 from Dr. Chen deposition). This I_{bias} block has nothing to do with *set[ting] a biasing ratio for gm-boost of the current buffer driver*. Taylor, ¶¶120-122. Rather, it merely performs the generic function of placing the circuit at a desired operating point or condition, as described in Technology Background, §III.B. See also Taylor, ¶¶46-52.

Dr. Chen admits in his declaration (see ¶¶145-146), that the biasing ratio in Rincon-Mora Fig. 3 is the “ratio between transistors 20 and 45,” which are the output driver (20), and buffer driver (45) transistors, respectively. But this is divorced from the function of I_{bias} which simply places the circuit in a “ready” state. Taylor, ¶¶120-

122. Thus, the “bias circuit” (viz., the I_{bias} block) is completely independent of the bias ratio between Rincon-Mora’s transistors 20 and 45. At most, Petitioner posits a circuit coupled to another/different circuit that **set[s] a biasing ratio**, but which does not itself participate in set[ting] a bias ratio. *Id.* Thus, Petitioner has failed to show Ground I satisfies element 1[c].

Petitioner contends “a bias current I_{bias} [] is mirrored in current mirror 47 to set a biasing ratio for gm-boost.” Pet., 59; *see also id.*, 61 (“This sum current is ‘ratio’ed’ in current mirror 47”). To the extent Petitioner and Dr. Chen rely on comparing Rincon-Mora’s current mirror 47 transistors to the purportedly “ratio’ed in transistors 368 and 370” (*see* Pet., 59) in Fig. 3 of the ’074 patent, they draw a false comparison as those transistors are not what **set[s] a biasing ratio for gm-boost of the current buffer driver**. Taylor, ¶¶120-122. Accordingly, this argument fails for the same reason above.

Petitioner’s alternative argument spanning one paragraph (regurgitated word-for-word in the expert declaration) generically recites what “a POSITA would have understood” and is not sufficiently well-developed for PO to adequately understand it. *See* Pet., 61-62. In any event, it relies on “adjusting the biasing circuit to set the value of I_{bias} ” (*id.*), which has already been explained is barking up the wrong tree entirely. Taylor, ¶¶123-124.

2. Al-Shyoukh Ground (Taylor, ¶¶113-118)

Petitioner's analysis for Al-Shyoukh is likewise flawed. Once again, we begin with what Petitioner and its expert identify as the claimed **biasing circuit**. And, once again, they dodge by discussing various **currents** rather than circuits. See Pet., 19, 21 (highlighting currents but no circuits); see also EX1002, ¶¶145-149 (similar). So Petitioner asked Dr. Chen at deposition to identify the claimed **biasing circuit**. He testified that, at most, one transistor (M27) in Al-Shyoukh Fig. 8 was "part of" the biasing circuit, but everything else was not shown:

Q. Under the first interpretation that you offer, what transistors do you map to the biasing circuit in Al-Shyoukh Figure 8? A. Again, in the first interpretation, right, the biasing circuits is consists of Vb1 because that drive the gate of M27. ...

Q. And under that interpretation, are you saying that transistor M27 is also part of the biasing circuit? A. The bias voltage come to that particular transistors. So a POSITA could understand that as also part of the biasing circuits, that is correct. ***And that's, you know, because the figure unfortunately they do not show how the generate Vb1, right. So that could be why I could not circle a box to show you what transistors.*** So instead, you know, I have to use the text to say that, which is in paragraph 56, right, so you can see that voltage Vb1.

EX2018, 222:7-223:7. Because this was an important issue (and massive shortcoming in the Petition), Petitioner asked a similar question again:

Q. Is Vb1 a transistor? A. No, Vb1 is the voltage that come into this

transistor.

Q. So my question is, what transistors are you identifying as the biasing circuit in Al-Shyoukh Figure 8? ... A. So that would entail ***M27 as well as whatever that circuitry would generate, the Vb1.***

EX2018, 215:10-216:11.

At deposition, Dr. Chen confirmed that what he identified in the blue box below (and external circuitry providing the Vb1 voltage) is the ***bias circuitry.***

EX2018, 227:6-228:15.

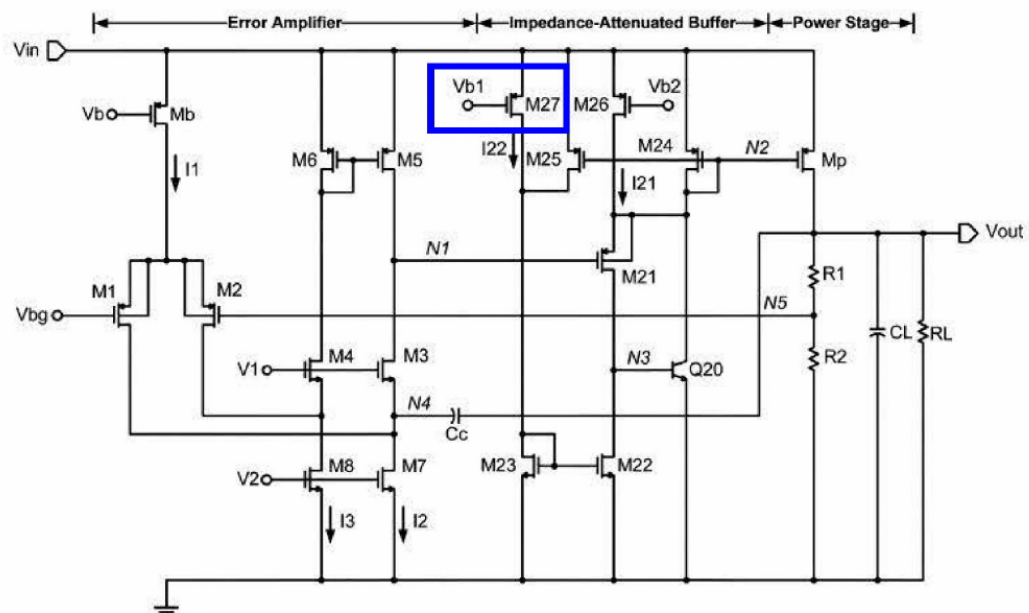


Fig. 8. Schematic of the proposed LDO.



EX2015 (annotated version of Al-Shyoukh Fig. 8 from Dr. Chen deposition).

As with Rincon-Mora, this is fatal to Petitioner's case because the external bias circuitry that turns on M27 to ready the circuit for operation has nothing to do with *set[ting] a biasing ratio for gm-boost of the current buffer driver* as required by element 1[c]. Taylor, ¶¶113-118. Because Petitioner's theory relied on currents instead of circuitry to try and explain how Al-Shyoukh *set a biasing ratio*, Petitioner asked Dr. Chen for clarification:

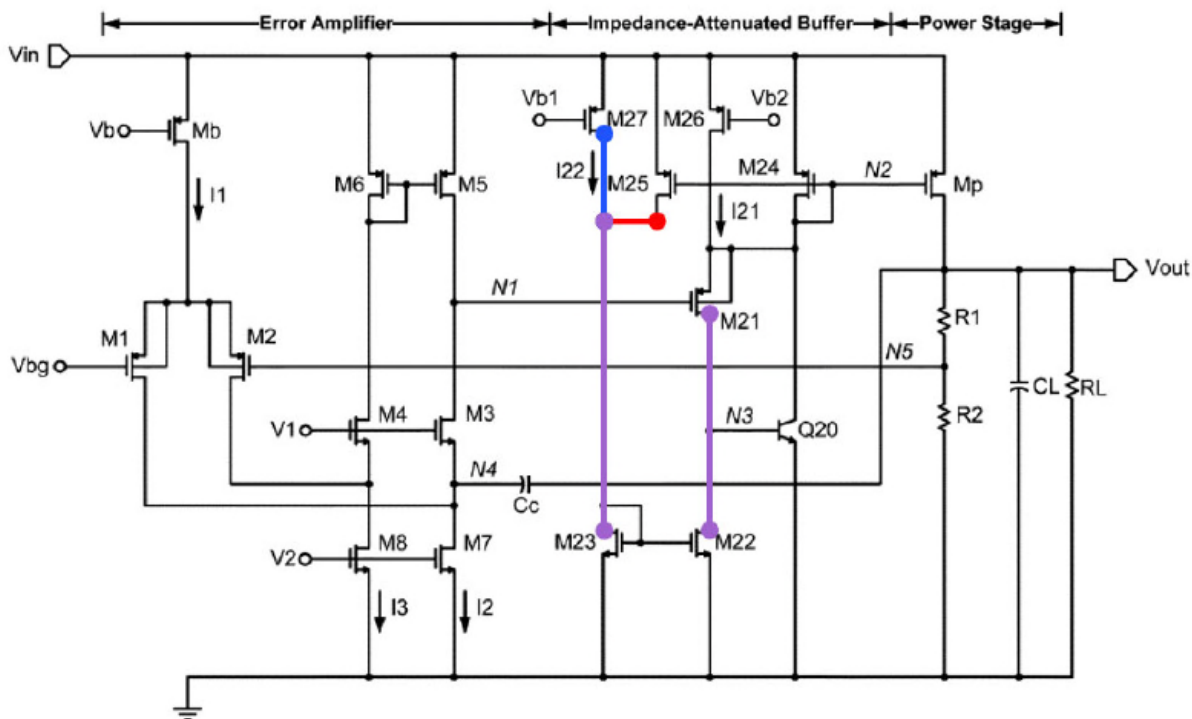
Q. And which two currents in Al-Shyoukh Figure 8 set the claimed biasing ratio under your first interpretation? A. Counsel, that's what I mentioned earlier. In the first interpretation, *the transistor M23, M22, now we're determining the current ratio.*

Q. And those are the two transistors that form the current mirror? A. That is correct.

EX2018, 247:21-248:5. Dr. Chen's answer was further fatal to Petitioner's case for another reason—not only was he identifying a current mirror (which does not *set a biasing ratio*), but he was now pointing to something that was not even part of the alleged *bias circuit*.

Further analysis confirms the flaws with Petitioner's analysis. Dr. Chen opines that “[a] POSITA reading Al-Shyoukh would have understood that, although not shown, the voltage V_{b1} at the gate of M₂₇ is provided by a biasing circuit.” EX1002, ¶56. He proceeds to assert that his annotated version of Al-Shyoukh Fig. 8 (reproduced below) “shows the feedback current from M₂₅ in red, and the summed

current flowing into M₂₃, and mirrored to M₂₂, in purple.” *Id.*; see also Pet., 19 (similar).



Pet., 19 (Al-Shyoukh annotated by Petitioner); EX1002, ¶56 (same).

The alleged biasing circuit identified by Petitioner determines the current provided by PMOS transistor M27, which does not set the claimed **biasing ratio**. Taylor, ¶¶114, 118. Instead, it merely provides a constant current that biases the circuit at its operating point. *Id.* A POSITA would recognize that in Al-Shyoukh Fig. 8 the gm-boost is supplied by the current from M25, and the gm-boost ratio (the quotient of the output driver current that biases the source follower) is given by the size ratio: $\frac{M25 \times M22}{Mp \times M23}$, which is ratio of currents between Mp and M21 (*i. e.*, M21/Mp).

Id. The design of the identified bias circuit and the size of M27 do not appear in this ratio because M27 and its bias circuit do not set the biasing ratio for gm-boost of the current buffer driver. At most, Petitioner posits a circuit coupled to another/different circuit that ***set[s] a biasing ratio***, but which does not itself participate in set[ting] a bias ratio. *Id.* Thus, Petitioner has failed to show Ground II satisfies element 1[c].

Petitioner and Dr. Chen provide a single-paragraph “[a]lternative[.]” argument. See Pet., 20; EX1002, ¶59. While the Board should dismiss this argument as underdeveloped, PO addresses it anyway (to the extent it can be understood) because it suffers from the same flaws as Petitioner’s primary theory. Petitioner’s alternative theory merely extends its analysis from the bias circuit encompassing Vb1 (and the external circuitry that provides that voltage) to also encompass Vb2 (and the external circuitry that provides that voltage). *Id.* This does nothing to address the fundamental problems that none of this circuitry ***set[s] a biasing ratio for gm-boost of the current buffer driver***.

C. Petitioner Fails to Give a Non-Hindsight Motivation for Combining Ivanov and Misunderstands/Ignores the Express Teachings of the References (Taylor, ¶¶125-138)

Petitioner raises no anticipation grounds. See Pet., 9. Petitioner and its expert admit that neither primary reference (Rincon-Mora or Al-Shyoukh) discloses element 1[d]: ***an enable/disable function to enable/disable the biasing circuit for reducing standby current***. See, e.g., EX2018, 128:17-129:6. Instead, for both

Grounds, Petitioner relies on Ivanov to supply the missing element 1[d].⁴ *See* Pet., 22 (“Al-Shyoukh with Ivanov discloses 1[d]”), 62 (“Rincon-Mora’s LDO in combination with Ivanov discloses 1[d].”); EX2018, 225:6-20, 231:13-20 (“I mainly show Ivanov, you know, how they can use that transistors in 11 and that sh[u]tdown circuits to perform the enable and disable function.”). Petitioner applies the same flawed rationale for combining Ivanov with Rincon-Mora and Al-Shyoukh. *Compare* Pet., 62-66 (Rincon-Mora) *with* 22-26 (Al-Shyoukh); EX2018, 238:7-15.

Petitioner’s entire analysis for why a POSITA would be motivated to combine Ivanov with Rincon-Mora is as follows: “A POSITA would have been motivated to use Ivanov’s disable/enable control mechanism for the biasing circuit for Rincon-Mora’s LDO. Both Rincon-Mora and Ivanov are highly concerned with power efficiency, and Ivanov’s mechanism saves power by shutting off unused circuitry. [cites to Ivanov and Rincon-Mora] In addition, Ivanov specifically states that voltage regulators were an intended application for its circuit.” Pet., 64. That’s it. Petitioner motivation analysis for the Al-Shyoukh ground is substantially identical. Pet., 25. Dr. Chen’s declaration is equally conclusory. *See* EX1002, ¶157 (Rincon-

⁴ Petitioner identifies no single-reference obviousness ground. *See* Pet., 9. To the extent Petitioner generically relies on POSITA knowledge to supply element 1[d] (*see* EX1002, ¶¶70, 161), that argument fails for the same reasons.

Mora ground) and ¶67 (Al-Shyoukh ground).

Petitioner’s argument fails because it (1) rests on a false premise rebutted by the art itself; and (2) is conclusory and fails to account for countervailing factors and trade-offs. In summary, Petitioner’s bare bones assertion is nothing more than a hindsight-driven results-oriented approach that uses the claim as a roadmap.

Claim element 1[d] requires **an enable/disable function to enable/disable the biasing circuit for reducing standby current**. As explained below, Petitioner admits neither Rincon-Mora nor Al-Shyoukh disclose the requisite **biasing circuit**. Further, Rincon-Mora expressly teaches its LDO voltage regulator “require[es] no standby or quiescent current during zero output current load conditions.” Rincon-Mora, Abstract. Against this backdrop, Petitioner proposes adding/modifying not-shown biasing circuitry to enable/disable voltage regulator circuitry which already draws “no standby or quiescent current.” This is the epitome of hindsight reasoning.

Nor is this the first time the Board found Aptiv and Dr. Chen to have engaged in improper hindsight bias. *See Aptiv Services US, LLC, v. Microchip Technology Inc.*, IPR2024-00803, Paper 10 (Order Denying Institution), 28 (P.T.A.B., Nov. 7, 2024) (“[N]either Petitioner nor Dr. Chen explains what reason or motivation one of ordinary skill in the art would have had to combine those embodiments. [cite omitted] Dr. Chen’s conclusory analysis here suffers from hindsight bias.”), *id.*, 26 (“We also agree with Patent Owner that the corresponding obviousness rationale is

conclusory.”), *id.*, 28 (“Dr. Chen’s declaration merely repeats the Petition’s argument. [cite omitted]. Thus, Dr. Chen’s assertions (EX1002 ¶ 206) are entitled to little weight.”).

1. Petitioner Fundamentally Misunderstands the Prior Art and Its Logic Rests on a False Premise

The first link in Petitioner’s logical reasoning chain rests on a false premise—*viz.*, that Rincon-Mora and Al-Shyoukh require further power reduction. Pet., 25, 64. This is fatal to Petitioner’s purported motivation to combine. In other words, Petitioner’s motivation does not even cross the start line.

a. Rincon-Mora

Petitioner cites Rincon-Mora for its statement that “standby and quiescent current flow are major concerns” in LDO design as support for the notion that a POSITA would be motivated to add a disable function to reduce Rincon-Mora’s power consumption. Pet. 64 (quoting Rincon-Mora, 1:18-30). But the context for this statement is to contrast previous LDO voltage regulator designs (which failed to achieve adequately low standby/quiescent currents) with Rincon-Mora’s regulator design which satisfied those needs. Rincon-Mora, 1:18-30 (contrasting “LDO voltage regulators [that] incorporate a separate enable terminal to switch the device into a standby mode of operation to minimize power consumption when the associated device is disabled”). In particular, Rincon-Mora touts right in its Abstract that its regulator design “require[s] no standby or quiescent current during zero

output current load conditions.”

This theme is repeated throughout Rincon-Mora. See §VI.A.1. The title emphasizes the “Current Efficient” nature of Rincon-Mora’s LDO. The first paragraph of the specification states “the present invention relates to a **current efficient LDO** voltage regulator ... [that] **requires no standby current during zero output current load conditions.**” Rincon-Mora, 1:12-18. This benefit of Rincon-Mora’s design is repeated throughout the specification. See, e.g., *id.*, 1:48-52 (criticizing “known techniques [which] result in circuit designs that ... require more quiescent current flow than is desired during zero load current conditions.”); 1:66-2:2 (describing its “current efficient design”); 2:4-9 (Rincon-Mora’s regulator “requires no standby current during zero output current load conditions.”). Section IV.A.1 explains how Rincon-Mora supplies current only upon demand.

Tellingly, even Petitioner (and its expert) recognize as much, stating that “if [Rincon-Mora’s] transistor 45 is sufficiently small, its quiescent current in a no-load state **is negligible and thus power-efficient.**” Pet., 56; see also EX1002, ¶136 (same). In other words, Rincon-Mora unequivocally declared victory over the prior art problem of too much quiescent current, and thus taught away from an enable/disable feature. Taylor, ¶¶89-91, 127-130.

The only other Rincon-Mora passage Petitioner (or its expert) cite actually cuts in PO’s favor as well. Petitioner cites Rincon-Mora col. 5:18-21 for the

proposition that “a benefit of [Rincon-Mora’s] proposed transient response boost circuit is that it is ‘power efficient’ because ‘it only sinks current upon demand.’” Pet., 64. That makes PO’s point—a key benefit of Rincon-Mora’s regulator design is that it is already “power efficient” and “only sinks current upon demand,” negating any need or motivation to add an enable/disable function (which would cost more, incur startup delays, and increase circuit complexity). Taylor, ¶¶89-91, 127-130, 136-138. Thus, Petitioner fundamentally misapprehends the teachings of the prior art, and Petitioner’s analysis backfires by citing the benefit Rincon-Mora’s voltage regulator design achieved, not something that remained to be accomplished.

The Rincon-Mora paper is in accord. Petitioner’s sole reason for combining the Rincon-Mora patent and Rincon-Mora paper was “to understand [Rincon-Mora’s] invention, including the transient boost circuit, fully.” Pet., 56. And Dr. Chen admitted at deposition that the Rincon-Mora patent disclosure applies to the Rincon-Mora paper. EX2018,124:17-22. Thus, the Rincon-Mora paper provides further context for the Rincon-Mora patent statements that its voltage regulator “requires no standby current during zero output current load conditions.” Rincon-Mora, Abstract. In particular, as summarized in §VI.A.2, the Rincon-Mora paper provides quantitative quiescent current data, reporting that the regulator has “a zero-load quiescent current flow of 23µA.” EX1014, 1; *see also id.*, Fig. 11, Table 1. Thus, the references collectively teach that 23µA of quiescent current is tantamount

to “no standby or quiescent current during zero output current load conditions.” Rincon-Mora, Abstract. That is the understanding a POSITA would take from reading the two references. Taylor, ¶89, fn.5.

And, as summarized in §VI.A.2, the Rincon-Mora paper touts that its “low quiescent current” and “current efficient” design “utilize a minimum amount of current” for “maximum current efficiency and prolonged battery life.” EX1014, 1-2, 4. Thus, Rincon-Mora is already well-suited for low-power battery applications. *Id.* This plainly teaches away from adding enable/disable functionality. Taylor, ¶¶89-91, 129-130; *see also* Rincon-Mora, 1:12-30 (contrasting Rincon-Mora’s low quiescent current design with previous regulators that needed a disable function).

b. Al-Shyoukh

To begin, it should be kept in mind that the enable/disable limitation is what overcame Al-Shyoukh during prosecution. *See* §IV.B. Petitioner admits that Al-Shyoukh does not teach an enable/disable function. *See, e.g.*, EX2018, 128:17-25. And Petitioner’s rationale for combining Al-Shyoukh with Ivanov is substantially the same (and equally cursory) as its reason for combining Ivanov with Rincon-Mora, and fails for the same reason. Pet., 25.

Petitioner cites Al-Shyoukh for its vanilla assertion that LDO voltage regulators are “critical power management modules,” and that “low no-load quiescent current” is a performance requirement. Pet., 25 (citing Al-Shyoukh, 1).

But these statements simply set the stage for Al-Shyoukh to discuss its voltage regulator design, which Al-Shyoukh goes on to tout “minimize[s] the quiescent current at no-load condition,” “consumes small quiescent current of 20 μ A,” has “low quiescent current,” and achieves “worst-case current efficiency of 99.8%.” See §VI.B (quoting and summarizing Al-Shyoukh).

Notably, Al-Shyoukh compares its voltage regulator to the Rincon-Mora regulator (and four others) in Table II. Notably, Al-Shyoukh’s 20 μ A of I_q (quiescent current) is the lowest of all the regulators.

TABLE II
PERFORMANCE COMPARISON WITH PREVIOUSLY REPORTED LDOs

	1998 [1]	2000 [3]	2003 [4]	2004 [5]	2005 [17]	This Work
Technology (μ m)	2.0	1.0	0.6	0.5	0.09	0.35
V_{do} (V)	0.3	N.A.	0.2	N.A.	0.3	0.2
$I_{L,max}$ (mA)	50	200	100	160	100	200
I_q (mA)	0.023	0.03	0.038	0.025	6	0.02
Current Efficiency at $I_{L,max}$ (%)	99.5	N.A.	N.A.	N.A.	94.3	99.8
ΔV_{out} (mV)	19	220	130	200	90	54
T_r (μ s)	1.8	1.1	2	2.75	0.00054	0.27
C_L (μ F)	4.7	1	10	2.2	0.00060	1
ESR Zero Required	No	Yes	Yes	No	No	No
FOM (ns)	8.2	0.165	4.9	0.43	0.032	0.027

Rincon-Mora

Al-Shyoukh

Al-Shyoukh, Table II (annotated). While Al-Shyoukh criticizes Rincon-Mora for only sourcing 50mA of output current, Al-Shyoukh raises no concern with Rincon-

Mora's 23 μ A quiescent current. Al-Shyoukh, 1. Especially considering Rincon-Mora's express teachings that its quiescent current obviates the need for extra enable/disable circuitry, a POSITA would understand Al-Shyoukh (which has even lower quiescent current) and its comparison to Rincon-Mora to suggest the same. Taylor, ¶¶131-138, 92-97. In other words, if a POSITA would not add enable/disable functionality to a regulator with 23 μ A of quiescent current (as Rincon-Mora teaches), a POSITA would not view Al-Shyoukh's even lower 20 μ A of quiescent current as a motivation to add enable/disable functionality. Taylor, ¶¶133-136.

Thus, once again, far from providing a motivation to combine with Ivanov, Al-Shyoukh's reported results (touted as more than sufficient for battery powered applications) teach away from adding unnecessary enable/disable circuitry that would slow the regulator down and increase design complexity. Taylor, ¶¶131-138, 92-97. A POSITA would understand that the reason Al-Shyoukh does not discuss the possibility of an enable/disable circuit is because, like Rincon-Mora, Al-Shyoukh believes its low-quiescent current regulator design has sufficiently addressed the issue. *Id.* Al-Shyoukh goes on to explain that its "LDO is designed for portable applications" and has an overall "figure of merit" (FOM) score better than regulators "[1], [3]-[5] by at least one order of magnitude." Al-Shyoukh, 9. This would not lead a POSITA to conclude there was any need for a disable feature.

Even assuming a POSITA wished to improve upon Al-Shyoukh's design they would look to parameters where other designs out-performed Al-Shyoukh. For example, Rincon-Mora [1] has lower ΔV_{out} (*i.e.*, the maximum transient output-voltage variation). And the 2005 [17] design has substantially faster transient response time. Al-Shyoukh, Table II. Quiescent current, however, is not one of those parameters as Al-Shyoukh has the best performance in that metric. Again, this teaches away from where a POSITA would look to devote engineering time and energy to achieve performance improvements. Taylor, ¶¶127, 131-138.

In summary, Petitioner fails to proffer any legitimate reason why a POSITA would view Al-Shyoukh (or Rincon-Mora) in the first instance as raising a concern that lower quiescent current is needed. To the contrary, the references suggest just the opposite. This is consistent with additional datapoints as well. For example, the MIC59300 LDO voltage regulator datasheet that Petitioner cites includes an enable pin that “allows on-off control of the regulator. Current drain reduces to ‘zero’ when the device is shutdown, with only microamperes of leakage current.” EX1011, 11; *see also* EX2019, 2 (Datasheet for TC1300 300 mA CMOS LDO with shutdown where “[d]uring shutdown, regulator output voltage falls to zero, RESET output remains valid and supply current is reduced to 30 μA (typ.).”); EX2020, 3 (Fairchild KA78RXXC-Series regulator datasheet showing disable bias current of 20 μA); EX2012, 7 (STMicro Precision 500 mA regulators datasheet showing 6mA

quiescent current); EX2016, 6 (TI 800mA Low-Dropout Linear Regulator with 10mA quiescent current); EX2011, 1, 3 (TI LM2990 Negative Low Dropout Regulator with “quiescent current [of] typically 1 mA”).

2. Petitioner Fails to Analyze Any of the Trade-Offs Involved to Add Enable/Disable Functionality.

Even if a POSITA had some reason to consider adding enable/disable functionality to Rincon-Mora or Al-Shyoukh’s voltage regulators, a POSITA would have needed to evaluate the trade-offs and drawbacks of doing so. Taylor, ¶¶43, 59, 62-63, 130-138. Petitioner’s failure to consider this is fatal to its obviousness case.

As discussed in §III.D, voltage regulator design is full of trade-offs. Power consumption is just one consideration; others include circuit size, speed, complexity, cost, regulator stability, drop-out voltage, system-level considerations, intended applications, etc. *Id.* In short, no engineer (*viz.*, POSITA) would analyze one performance metric in isolation without considering its impact on other aspects of the design. *Id.*; §III.D. Indeed, Al-Shyoukh expressly states the “four major [LDO] performance requirements” it identifies “are, however, difficult to achieve simultaneously.” Al-Shyoukh, 1; *see also id.*, 9 (discussing “evaluating the tradeoffs between the response time T_r , the quiescent current I_q and the maximum load current I_{Lmax} .”).

At deposition, Dr. Chen admitted “when you decide the circuiting [sic] system, there are just so many consideration[s] to consider, right. It’s not just in one

single angle on this biasing of the regulators or whatever the circuit that you provide. Also, there's also part of the SOC that you need to consider. So typically that would need to be considered jointly.” EX2018, 263:6-16; *see also id.*, 260:24-261:21 (designer would consider cost of enable/disable circuitry), 261:22-262:12 (“when POSITA design the circuits, you always need to concern about the size that you use, right, the size that you use for all these devices, you know, will affect the circuit performance.”), 262:13-23; Al-Shyoukh, 8 (touting its “low component count.”).

It is self-evident that adding enable/disable functionality requires additional circuitry, which increases circuit complexity, takes up extra area, and adds cost. Taylor, ¶¶43, 59, 62-63, 130-138; EX2018, 255:13-20. And no matter how quickly this extra circuitry can re-enable the regulator, a delay penalty that must be paid to do so. Taylor, ¶¶43-44, 98, 134. Any POSITA would need to analyze these tradeoffs before concluding it was “obvious” to add such functionality. *Id.* But Petitioner failed to do so. *See* Pet., 25, 64. Determining/sensing when and whether to disable a voltage regulator also requires additional circuitry and is not a trivial exercise, largely because it can be difficult to detect when a regulator has an idle load and when it affirmatively needs to drive a low voltage (*e.g.*, 0V) on the output. Taylor, ¶63. Speed and stabilization time must also be considered as many applications have specific timing requirements. Taylor, ¶¶52, 63-64, 91, 96; EX2022.

Both Rincon-Mora and Al-Shyoukh expressly identify speed/timing as a key

consideration and principle of operation of their respective designs. See §VI.A and VI.B (discussing transient overshoots/undershoots and improved settling/stabilization times). No matter how fast an enable/disable signal may operate, it still slows down overall regulator operation by requiring it to come out of standby. Taylor, ¶¶43-44, 98, 134. This runs contrary to Al-Shyoukh and Rincon-Mora's goal of fast transient response (*viz.*, when the LDO output swings rail-to-rail from a low voltage quiescent state). Taylor, ¶¶91, 96-97. Thus, adding an enable/disable feature runs contrary to this operational principle. But Petitioner and its expert ignore this. EX2018, 256:6-25, 257:4-13 ("Q. Did you do any analysis in your report regarding how adding an enable/disable function would impact the speed of the Rincon-Mora or Al-Shyoukh voltage regulators? ... A. I don't remember that, that I did analysis of that enable and disable and how that impact the regulator speed of Rincon-Mora and Al-Shyoukh.").

The enable/disable circuitry itself consumes power, which also must be taken into account. Taylor, ¶¶100-103, 127, 130, 137-138. And there are alternatives to enable/disable functionality, such as powering down the regulator altogether. Taylor, ¶¶41-44. This option is attractive where there are expected to be long periods of inactivity. Petitioner did not consider any of these factors or alternatives in its single-paragraph conclusion that it would be obvious to add Ivanov's enable/disable circuitry to Rincon-Mora and Al-Shyoukh. See Pet., 25, 64; EX1002, ¶¶67, 157.

With respect to Ivanov, Petitioner did not account for the 5 μ A “trickle charge” current for the compensation capacitor C_{ϕ} . Pet., 25, 64; §VI.C. Nor did Petitioner address why a POSITA would focus on enable/disable for the voltage regulator instead of other aspects of system design with greater impact on overall power consumption. Taylor, ¶¶94, 100-102.

When asked at deposition about this, Dr. Chen confirmed he performed no such analysis:

Q. And you didn’t analyze any of those considerations in your report, did you? ...

A. I don’t recall that, but counsel let me quickly check this. So, counsel, the most relevant ones regarding to our discussions is on page 38, paragraph 70, and that's the power efficiency that we just talk about -- or I just talk about. ***I don’t see other considerations that I’ve analyzed in my report.***

EX2018, 264:23-265:10.

Dr. Chen further confirmed he did not analyze any drawbacks associated with implementing Ivanov’s enable/disable function—he only looked at whether Ivanov had an enable/disable function:

Q. What are the drawbacks to using an enable/disable circuit?

A. I suppose that were related to some system design concerns. As I mentioned earlier, I did not perform system analysis in this particular case at this point. So I’m not ready to offer that opinions by sitting here

today.

Q. And you didn't render any such opinions in your report, correct?

A. I don't recall that. I don't recall that I offered that kind of opinions other than showing that Ivanov circuit examples, you know, has this enable/disable signals.

EX2018, 254:13-255:4; *see also id.*, 255:21-24, 257:14-258:1 ("I don't think I can offer that opinions or analysis, you know, as to, you know, what cost that is adding.").

In summary, one cannot simply pick one performance criterion and myopically focus on it without considering the impact on the overall regulator or system in which it will be used. Any engineer who did so would likely not be employed for long. Yet that is precisely the analytic approach Dr. Chen took to his motivation to combine analysis.

3. Petitioner Mistakenly Focuses on What "Could" Have Been Done, Instead of What a POSITA "Would" Have Been Motivated To Do.

Petitioner fundamentally misunderstands obviousness law in another way—mistakenly believing that merely showing something *could* been done is equivalent to showing a POSITA *would* have been motivated to do it. But the Federal Circuit has repeatedly held "obviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or

modifications of prior art to arrive at the claimed invention.” *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (emphasis in original); *see also, e.g., Personal Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993-94 (Fed. Cir. 2017) (whether two references “*could be* combined ... is not enough: it does not imply a motivation to pick out those two references and combine them to arrive at the claimed invention.” (emphasis in original); *Polaris Indus., Inc. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1068-69 (Fed. Cir. 2018). This problem is pervasive throughout the Petition and its expert declaration.

Petitioner proposes various changes/modifications for multiple claim elements and claims. Starting with element 1[a] which requires an **operational amplifier**, Petitioner asserts “Rincon-Mora’s LDO comprises an error amplifier, which a POSITA would have understood **could be** an operational amplifier.” Pet., 57; *see also id.*, (“a POSITA would have understood that **it could just as well be implemented** as an operational amplifier.”); 68.

Continuing with element 1[b], Petitioner contends “[a] POSITA would also have understood that the buffer [in Rincon-Mora] **could be implemented** as an NMOS source follower.” *Id.*, 58. Next, for element 1[c] (which requires **a biasing circuit ... to set a biasing ratio for gm-boost of the current buffer driver**), Petitioner states “the biasing circuit **could be implemented** according to conventional, well-understood methods.” *Id.*, 62.

Next, for element 1[c], “[a] POSITA would have known that the biasing circuit **could be adjusted** to set V_{b1} and V_{b2} .” *Id.*, 21.

Continuing with element 1[d] (which requires **an enable/disable function to enable/disable the biasing circuit for reducing standby current**), Petitioner again invokes what *could* be done: “[A] POSITA **could have integrated** Ivanov’s biasing circuit” *Id.*, 64; *see also id.* (“Ivanov’s components **could be chosen** so that I_{BIAS+} is set to the desired value.”); *id.*, 64-65 (“[T]his logic block **could alternatively serve** as Ivanov’s external shutdown.”), 22 (“the biasing circuit **could be implemented** using conventional, well-understood methods.”), 25 (“a POSITA **could have integrated** Ivanov’s enable/disable function into Al-Shyoukh”).

Even where Petitioner invoked “would have” language, it did so to express that a POSITA “would have understood [or recognized]” what “**could be**” done, not what a POSITA **would have been motivated** to do. This is insufficient. *See Belden*, 805 F.3d at 1073; *Personal Web*, 848 F.3d at 993-94; *Polaris*, 882 F.3d at 1068-69.

Petitioner’s expert declaration—which largely copies the Petition—suffers the same defect. *See* EX1002, ¶140 (Rincon-Mora element 1[a]: “the error amplifier **could just as easily have been implemented** as an operational amplifier.”); ¶144 (Rincon-Mora element 1[b]: “Rincon-Mora’s buffer **could also be implemented as an NMOS source follower**”), ¶59 (Al-Shyoukh element 1[c]: “a circuit designer **could set bias voltages** V_{b1} and V_{b2} ...”), ¶60 (Al-Shyoukh element 1[d]: “it **could**

be implemented using any of a variety of conventional and well-understood methods”), ¶150 (Rincon-Mora element 1[d]: “[I]t *could be implemented* using any of a variety of conventional and well-understood methods.”); ¶158 (Rincon-Mora element 1[d]: “a POSITA *could simply have used* Ivanov’s circuit.”), ¶68 (same for Al-Shyoukh), ¶159 (Rincon-Mora element 1[d]: “This logic block *could, as a POSITA would have recognized, be* Ivanov’s external shutdown.”). These examples are from claim 1, but the same problem infects the dependent claims too. See *id.*, ¶195 (Rincon-Mora claim 11: “This circuit is one example of many variants that a POSTIA [sic] *could have arrived at* without undue experimentation.”), ¶101 (same for Al-Shyoukh), ¶203 (Rincon-Mora claim 16: “[T]he biasing circuit for the Rincon-Mora LDO *could be implemented* using conventional and well-understood methods.”), ¶112 (same for Al-Shyoukh).

Even where Petitioner proffered a purported motivation (*e.g.*, for element 1[d]), its argument fails for the reasons discussed in §§VII.C.1 and VII.C.2.

VIII. SECONDARY CONSIDERATIONS

Because Petitioner presents such a weak case of obviousness (*e.g.*, one that does not even support a *prima facie* showing of obviousness), secondary considerations are unnecessary to rebut it. Regardless, any secondary considerations would only further support the non-obviousness of the claims.

IX. CONCLUSION

For the foregoing reasons, PO respectfully requests that the Board find the challenged claims not unpatentable.

Respectfully submitted,

Dated: January 8, 2025

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PATENT OWNER'S RESPONSE complies with the type volume limitation in 37 C.F.R. § 42.24(a). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 13,975 words.

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CERTIFICATE OF SERVICE

The undersigned certifies that on January 8, 2025, a copy of the following was served in its entirety via electronic mail, upon the following attorneys of record for Petitioner:

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