

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APTIV SERVICES US, LLC,
Petitioner,

v.

MICROCHIP TECHNOLOGY INC,
Patent Owner.

Case No. IPR2024-00646
U.S. Patent No. 9,471,074

**DECLARATION OF DR. GREG TAYLOR
IN SUPPORT OF PATENT OWNER'S RESPONSE**

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I, Greg Taylor, do hereby declare as follows:

I. INTRODUCTION

1. I have been retained by counsel for Microchip Technology Inc. (“Microchip” or “Patent Owner”) in the above-captioned matter as an independent consultant. I have been asked consider whether the Petition’s prior art in Ground 1 (the Al-Shyoukh ground) or Ground 2 (the Rincon-Mora ground), when considered in light of the knowledge of a person of ordinary skill in the art (“POSITA”), show that claims 1-18 in U.S. Pat. 9,471,074 (“the ’074 patent” or “the challenged patent”) are obvious.

2. I have confined my analysis to the materials available at the time of the preparation of this Declaration - supplemented with my own knowledge and experience in the field. Should new materials, analyses, or opinions be introduced subsequent to the filing of this Declaration, I reserve the right to provide supplementary declarations to the extent necessary to address any such newly-introduced items.

II. BACKGROUND AND QUALIFICATIONS

3. I summarize in this section some of my educational background, career history, publications, and other relevant qualifications. My full *curriculum vitae* is attached as Appendix A to this Declaration. During the past 5 years I submitted declarations in the following matters, but otherwise have not testified in any cases.

- The co-pending district court litigation between the same parties;
- IPR2021-01531;
- IPR2022-00481;
- IPR2022-00285;
- IPR2023-00453;
- *Ex Parte* Reexamination No. 90/019,063;
- *Ex Parte* Reexamination No. 90/019,015; and
- *Ex Parte* Reexamination No. 90/019,117.

4. I earned a Doctor of Engineering (Ph.D.) degree in Computer and Systems Engineering from Rensselaer Polytechnic Institute (RPI) in 1985. From 1986 to 1991 I worked as a Circuit Design Engineer and then Principal Design Engineer for Bipolar Integrated Technology. I started as a new hire from the Ph.D. program at RPI and ended up as the chief architect, lead product designer, lead verification engineer, and developer of the world's only formal verification tool for bipolar circuits.

5. From 1991 until 2016, I worked for Intel Corporation, starting as a Senior Staff design engineer and quickly became a team leader delivering the package, I/O, and analog circuits for the first processors on each technology generation. In 2002 I was promoted to Intel Fellow (one of the company's highest technical positions) based on both results and risk management in getting five

generations of microprocessors into high volume manufacturing on schedule, including the first use of C4 packaging at Intel. From 2002 to 2016 I worked as director of numerous groups within Intel (Mixed Signal Circuit Technology, Circuit Research Lab, SoC Design Lab, Low Power Mixed Signal Lab), where I led teams that delivered three separate firsts for both Intel and the world: the first microprocessors using strained silicon, the first products using high-k metal gate transistors, and the first Trigate (FinFET) product. During this time my role expanded to leading a new company-wide analog/mixed signal circuit review team and leading the worldwide circuit architecture teams for I/O, analog, and supply regulator design IP. I currently operate my own consulting firm (Greg Taylor Consulting, Inc.), where I provide technical consulting services on electronic product and integrated circuit development for a variety of clients.

6. In addition to the above, I was also responsible for power distribution circuitry in several generations of microprocessors I worked on. This included not just distributing large currents at low impedances to the digital circuits on chip, but also building on-chip LDO voltage regulators to power the less noise-tolerant analog circuits that were integrated on chip. Later, while I was leading the Circuit Research Lab at Intel, my team successfully developed a 100 MHz on-chip switching regulator technology that took a high voltage input supply (twice what any transistor on the chip could survive) and delivered a high efficiency, clean, low voltage output

without using any board level passive components. My team also worked on LDO regulators, producing reference 17 of Al-Shyoukh, his only reference with a “Figure of Merit” close to his own. [EX1004, Table II] This regulator was also notable for requiring an output capacitor more than 1000 times smaller than Al-Shyoukh or any of the other regulators referenced by him.

7. Additionally, I have been an IEEE Fellow since 2009. I have published more than 60 peer reviewed papers, and I am the inventor of 68 U.S. patents on integrated circuit design and testing.

III. COMPENSATION

8. I am being compensated at my usual hourly rate for my work in this case. My compensation is not based upon the content of my opinions or the outcome of the matter.

IV. MATERIALS CONSIDERED

9. In preparing this Declaration and formulating my opinions within, I have considered the '074 patent and its prosecution history, along with my personal expertise, knowledge, and experience with the relevant technology, and the materials referenced or mentioned in the body of this Declaration. I have also considered the following materials:

Exhibit	Description
1001	U.S. Patent No. 9,471,074

Exhibit	Description
1002	Declaration of Dr. Michael S. Chen
1003	Prosecution History of U.S. Patent No. 9,471,074
1004	Mohammad Al-Shyoukh, et al., “A Transient-Enhanced Low-Quiescent Current Low-Dropout Regulator with Buffer Impedance Attenuation,” <i>IEEE Journal of Solid-State Circuits</i> , Vol. 42, No. 8 (Aug. 2007) (“Al-Shyoukh”)
1005	U.S. Patent No. 6,400,207 (“Ivanov”)
1006	U.S. Patent No. 6,710,583 (“Stanescu”)
1011	Micrel Inc., MIC59300 Datasheet (Jan. 2009) (“MIC59300”)
1013	U.S. Patent No. 6,046,577 (“Rincon-Mora”)
1014	Gabriel A. Rincon-Mora, “A Low-Voltage, Low Quiescent Current, Low Drop-Out Regulator,” <i>IEEE Journal of Solid-State Circuits</i> , Vol. 33, No. 1 (Jan. 1998) (“Rincon-Mora Paper”)
1015	Gabriel A. Rincon-Mora, “Current Efficient, Low Voltage, Low Dropout Regulators” (Nov. 1996) (“Rincon-Mora Dissertation”)
1016	U.S. Patent No. 6,084,475 (“Rincon-Mora ’475”)
1017	Michael Day, “Understanding Low Drop Out (LDO) Regulators,” <i>2006 Texas Instruments Portable Power Design Seminar</i> (2006) (“Day”)
1018	Chester Simpson, “Linear and Switching Voltage Regulator Fundamental Part I” (2011) (“Simpson”)
1019	U.S. Provisional Patent Application No. 61/780,985
2001	U.S. Pat. 7,312,598 (“Huang”)
2002	Aptiv’s Responsive Claim Construction Brief and supporting Declaration of Stanley Shanfield, Ph.D. (March 22, 2024)

Exhibit	Description
2003	Aptiv's Sur-reply Claim Construction Brief and supporting Declaration of Stanley Shanfield, Ph.D. (May 3, 2024)
2004	U.S. Pat. 6,246,22 ("Xi")
2005	Chronological File History for U.S. Pat. 9,471,074
2006	Aptiv's District Court Invalidity Contentions (December 8, 2023)
2007	Microchip's Opening Claim Construction Brief and supporting Declaration of Greg Taylor (March 1, 2024)
2008	Microchip's Reply Claim Construction Brief and supporting Declaration of Greg Taylor (April 17, 2024)
2011	Texas Instruments datasheet for LM2990 Negative Low Dropout [Voltage] Regulator, April, 2013
2012	ST Micro datasheet for L78MxxAB/C voltage regulator, May 2012 (from Dr. Chen deposition)
2013	'074 patent claim 1 (from Dr. Chen deposition)
2014	Rincon-Mora Biasing Circuit (Fig. 3) (from Dr. Chen deposition)
2015	Al-Shyoukh Biasing Circuit (Fig. 8) (from Dr. Chen deposition)
2016	Texas Instruments datasheet for LM1117/LM1117I Low-Dropout Linear [Voltage] Regulator, 2012
2017	Excerpts from the Laplante Electrical Engineering Dictionary (CRC Press LLC, 2000)
2018	December 4, 2024 Deposition Transcript of Dr. Michael Chen.
2019	Microchip TC1300 CMOS LDO with Shutdown, Bypass and Independent Delayed Reset Function, 2012
2020	Fairchild KA78RXXC-Series 1A Output Low Dropout Voltage Regulators datasheet

Exhibit	Description
2022	<i>Universal Serial Bus 3.0 Specification</i> , Revision 1.0, November 12, 2008 (“USB 3.0 Specification”)

10. There are images and explanations in this Declaration included for illustrative purposes, some of which I created myself for explanatory purposes. Images taken from patents and publications have been cited. At the time of my signing this Declaration, all the hyperlinks referenced herein were publicly accessible.

V. LEGAL STANDARDS

11. I am not an attorney and will not provide opinions of law. I have been instructed on principles of law, as set forth below. I applied these principles, as appropriate, to my analysis. I have been informed that each patent claim is considered separately for purposes of patentability and that a dependent claim that depends from another claim includes all of the limitations of the claim it depends from. I have been informed and understand that if a prior art reference (or references) does not render an independent claim unpatentable, then it necessarily fails to render any dependent claims unpatentable as well.

A. Claim Construction

12. I have been informed that the claims in this proceeding are to be construed using the same claim construction standard applied in district court. I have been informed that the claim construction analysis begins with the ordinary meaning

of a claim term, and there is a presumption that the term carries its plain and ordinary meaning to persons of ordinary skill in the art as of the effective filing date of the patent. I have also been informed that the most important sources for determining the meaning of a claim term are the claims, the specification, and the prosecution history of the patent at issue, which collectively is called “intrinsic evidence.” I have been further informed that the meaning of a claim term may also be guided by “extrinsic evidence,” such as contemporaneous dictionaries and treatises, as well as the testimony of technically-skilled witnesses such as myself.

B. Burden of Proof

13. I have been informed that the petitioner in an *inter partes* review bears the burden of establishing unpatentability by “a preponderance of the evidence.” I have been further informed and understand that, to prove an assertion by “a preponderance of the evidence,” the party with the burden of proof must demonstrate that it is more likely than not that the assertion is true.

C. Anticipation

14. I have been informed that a patent claim is unpatentable if it is “anticipated” by prior art. I have been informed that a reference anticipates a claim if the reference discloses each limitation of the claim at issue, either expressly or inherently. I have been informed that a prior art reference may anticipate a claim without disclosing a feature of the claimed invention if that missing characteristic is

necessarily present, or inherent, in the single anticipating reference as would have been understood by one of ordinary skill in the art. I have been informed that material not explicitly contained in a single prior art document may still be considered for purposes of anticipation if that material is incorporated by reference into the document.

D. Obviousness

15. I have been informed that a patent claim is unpatentable if it would have been obvious to a person of ordinary skill in the art (“POSITA”) at the time of the claimed invention. I have been further informed that a claimed invention is not patentable if differences between it and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. I have been informed that factors relevant to the determination of obviousness include the scope and content of the prior art, the level of ordinary skill in the art at the time of the invention, differences between the claimed invention and the prior art, and “secondary considerations” (also called objective indicia) of non-obviousness.

16. I have been informed that a single reference alone can render a patent claim obvious, if any differences between the reference and the claim would have been known or obvious to a POSITA at the time of the invention. That is, if the POSITA could have and would have adapted the reference to meet the claims of the

patent by applying known concepts to achieve expected results, then the patent claims are rendered obvious by that reference.

17. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I have been further informed and understand that when a patent claim simply arranges old elements with each performing the same function it had been known to perform, and yields no more than one of ordinary skill would expect from such an arrangement, the combination is obvious.

18. I have been informed that a patent claim composed of several limitations is not obvious merely because each limitation was independently known in the prior art. Hindsight reasoning is not an appropriate basis for combining references to form an obviousness combination. I have been further informed that it is important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine multiple prior art references, or multiple teachings of the same prior art reference.

19. I have been informed that various “secondary considerations” (sometimes referred to as objective indicia of non-obviousness) may support a determination of non-obviousness and that such secondary considerations (if available) should be considered as part of an obviousness analysis. I have been informed that the patentee bears the burden of showing the existence and effect of

secondary considerations of non-obviousness, after which the burden of coming forward with rebuttal evidence shifts to the party arguing obviousness. I have been informed that the following secondary considerations may indicate non-obviousness:

20. ***Copying***: evidence that others, including the accused infringer, copied the patented invention.

21. ***Long-standing problem or need***: evidence of a persistent problem or need in the art that was resolved by the patented invention.

22. ***Prior failure***: evidence that others have tried and failed to solve the problem or failed to provide the need resolved by the claimed invention.

23. ***Commercial acquiescence of competitors***: the willingness of industry to license the patent at issue.

24. ***Skepticism***: evidence that those of ordinary skill in the art were skeptical as to the merits of the invention.

25. ***Praise***: evidence of praise directed to an invention by others in the field.

26. ***Unexpected results***: evidence that those of ordinary skill in the art were surprised by the capabilities of the claimed invention.

27. I have also been informed that the near-simultaneous invention by others can be evidence that a claimed invention is obvious. I have further been informed that the patentee bears the burden of showing a “nexus” between the claimed invention and the evidence proffered on secondary considerations (e.g.,

proof of commercial success of a product that practices the claimed invention is not enough; there must be evidence that the commercial success resulted, at least in part, from the claimed invention).

E. Priority Date

28. I have been informed that a U.S. patent may claim “priority” to the filing date of one or more earlier filed applications. I have been informed that the priority date, also called the “effective filing date,” is the earliest filing date to which a claim is entitled – and that such date is relevant for determining what qualifies as prior art. I understand that a claim must have written description support in the application(s) to which it claims priority to be entitled to an earlier effective filing date. I have been informed that the priority date determination is done on a claim-by-claim basis, and that claims in the same patent may have different priority dates.

29. The '074 patent application was filed March 11, 2014 and claims priority through a provisional application to March 14, 2013. My opinions in this Declaration would not change regardless of which date is used as the priority date. Accordingly, I render no opinion regarding the '074 patent priority date, but reserve the right to do so.

F. Level of Ordinary Skill in the Art

30. I have been informed that the level of ordinary skill in the relevant art at the time of the invention (*i.e.*, the priority date) is pertinent to inquiries such as

the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons one of ordinary skill in the art (“POSITA”) may have for combining references. I have been asked to consider the abilities and education of a POSITA as of the priority date.

31. I have been informed that factors that may be considered in determining the level of ordinary skill include: (1) the type of problems encountered in the art; (2) prior art solutions to those problems; (3) rapidity with which innovations are made; (4) sophistication of the technology; and (5) education level of active workers in the relevant field. I have been further informed that a POSITA is also a person of ordinary creativity.

32. In my opinion, a POSITA would have a bachelor’s degree in electrical engineering, computer science, or an equivalent technical degree and substantial experience (e.g., several years) in analog mixed signal design for integrated circuits.

33. I was at the time of the alleged invention at least a POSITA in the art relevant to the challenged patent. Further, based on my experience and education, I understand and know of the capabilities of a POSITA at the relevant time - and I am familiar with how a POSITA would have understood and used the terminology found in the prior art and the challenged patent at the time of its filing, and with the state of the art at that time.

34. From reviewing the Petition, it is my understanding that Petitioner proposes the following definition for a POSITA: “A POSITA in the field of the ’074 patent in 2013 would have had at least a Master’s Degree in Electrical Engineering, or alternatively a Bachelor’s Degree in Electrical Engineering and two years of experience working on analog circuit design.” [Pet., 9.]

35. While I disagree that a Master’s degree is necessary, this proposed standard is actually relatively close to the standard that I have proposed above. I also qualify as a POSITA under Petitioner’s definition. Regardless of which POSITA definition is used, my analysis and opinions that follow would not in any way be changed or affected.

36. While my experience level exceeds that of a POSITA, I am familiar with POSITAs from the time frame of the priority date, and my opinions regarding what a POSITA would understand are based on a POSITA’s perspective at that time.

VI. SUMMARY OF OPINIONS

37. The Petition asserts two Grounds of unpatentability challenging claims 1-18 of the ’074 patent (the “Challenged Claims”). [See Pet., 9] Both Grounds are obviousness challenges. I have been asked to evaluate if either of Petitioner’s Grounds (and the references cited therein) establish obviousness of the Challenged Claims. The primary reference for Ground 1 is Al-Shyoukh, and the primary reference for Ground 2 is Rincon-Mora. [Id.] Both grounds combine the Ivanov

reference as a secondary reference for claim 1. Certain dependent claims combine additional prior art references.

38. Based on my evaluation and analysis, it is my opinion that Petitioner has failed to meet its burden to show that claim 1 (and thus any dependent claim) is rendered obvious by either Ground.

VII. TECHNOLOGY BACKGROUND

A. Design Hierarchy and Organization

39. Modern integrated circuits (also known as “chips”) contain large numbers (potentially billions) of transistors. Consequently, the designs of these chips depend upon being well organized. Initial design typically starts by breaking the specified functionality of the chip down into pieces that can be designed separately, and those pieces are similarly partitioned into their components. This “top down design” repeats until the pieces are small enough to be implemented and verified as a single component (a building block). The implementation then proceeds “bottom up” assembling the blocks that were partitioned in the “top down” phase.

40. Implementing separate building blocks as separate elements serves (at least) two functions: (1) each building block can be built and verified, ensuring it meets its target specifications, before it is built into a higher-level component; and (2) maintaining blocks (either fixing bugs or making late improvements) can be done

with minimal impact to the other pieces of the chip. Somewhat more complex blocks will then be assembled from several basic blocks, from which yet more complex blocks will be created. By building up the complexity of the system gradually designers are better able to verify that each component has been built correctly and less likely to fail to discover an interaction because they added too many elements together at once.

B. Power Management

41. From a user point of view, many electronic systems have only two power states: “on” and “off.” When a system is on, it is capable of immediately carrying out tasks for the user but is dissipating power. When a system is off it does not dissipate any power but must be turned on (a process that can consume significant amounts of time and power) before it can be used.

42. For some systems “on” and “off” are the only power states, but as energy efficiency and the use of batteries to power systems have become more common, additional power states have been added to systems. Sometimes these are explicitly visible to the user (e.g. the “sleep” and “hibernate” states supported by many computers), more often they are present but invisible to the user. An example of the latter is the “autohalt” capability that was integrated into Intel® processors in the early 1990s – the CPU clock would stop whenever the CPU became idle (often between keystrokes while the user typed) but be capable of restarting in a small

fraction of a microsecond. This introduction was driven by the EPA's original Energy Star program in 1992 (<https://www.energystar.gov/about/how-energy-star-works/history>).

43. The commonality of these power states is that each offers a unique tradeoff between power dissipation and usability, with power savings being traded off for increased delay until the system becomes usable. For example, the “autohalt” capability mentioned above turned off the clock distribution of the processor but didn’t shut off any power supplies or even the clock source itself, it just prevented the clock from going to most of the chip. This reduced the power dissipation by perhaps 90% while costing only a handful of clock cycles to “wake up,” a short enough delay that the operating system didn’t need any modification to support. Responding to external events (the user typing on the keyboard, a device needing attention to input or output data) were significantly slower than the operating system and could be handled without needing to make the user or device aware that “autohalt” was saving power.

44. As system designers have worked to reduce power they have turned off more clocks and power supplies, but have always been limited by the maximum delay that other parts of a system (or other connected systems) can tolerate without failing. By comparing the externally needed response time to the startup requirements of each impacted subsystem a decision about the needed power state

(thus power dissipation) can be made for each part of a system, reducing overall system power to a minimum while maintaining expected functionality.

C. Conductance and Transconductance

45. In electronics conductance describes the relationship between changes in current and changes in voltage. For a resistor, current (i) and voltage (v) are proportional to one another, following $i = gv^1$, and conductance (g) is the constant of proportionality. When a voltage in one part of a circuit (e.g. an amplifier input) controls the current that appears in another part (e.g. an amplifier output) we refer to this relationship as “transconductance” because it follows a similar equation: $\Delta i = g_m \Delta v$.

D. Bias Circuits

46. Analog circuits can generally be divided into two portions: the “active” devices that are in the signal path from input to output and the “bias” devices that are present to ensure that the “active” devices are biased with appropriate DC current

¹ If $i = gv$, and g is constant then it is also true that $\Delta i = g\Delta v$. In the general case where g is not constant engineers apply the latter relationship. Note that this relationship is alternatively written as $di/dt = g dv/dt$ (differential calculus) or $\delta i/\delta t = g \delta v/\delta t$ (partial differential calculus). The nuances implied by these different forms are not relevant here.

and/or voltage levels. The Laplante Electrical Engineering Dictionary (CRC Press LLC, 2000) provides a relevant definition for the term “biasing”:

Biasing: the technique of applying a direct-current voltage to a transistor or an active network to establish the desired operating point. [EX2017, 5]

This is consistent with how a POSITA would understand that term and concept in the context of LDO voltage regulators.

47. Transistors are non-linear devices, if you double the input the output does not necessarily also double. In the case of the saturation current through an ideal MOSFET, there is a square law relationship: $I_{DS} = k(V_{GS} - V_t)^2$, where I_{DS} is the current flowing from the drain to source, V_{GS} is the voltage from the gate to the source, V_t is the threshold voltage of the transistor, and k is a constant. A graph of this relationship is shown in Figure 1. When analyzing and designing a circuit it's easier to consider linear operation, so engineers will consider an “operating point” (the orange dot in Figure 1) and “linearize” the system – assume that it is operating along the orange line rather than the blue curve. For small changes in $V_{GS} - V_t$, this results in a good approximation of the actual I_{DS} vs $V_{GS} - V_t$ curve. The procedure of ensuring that the transistor is operating near the selected operating point is called “biasing” the device.

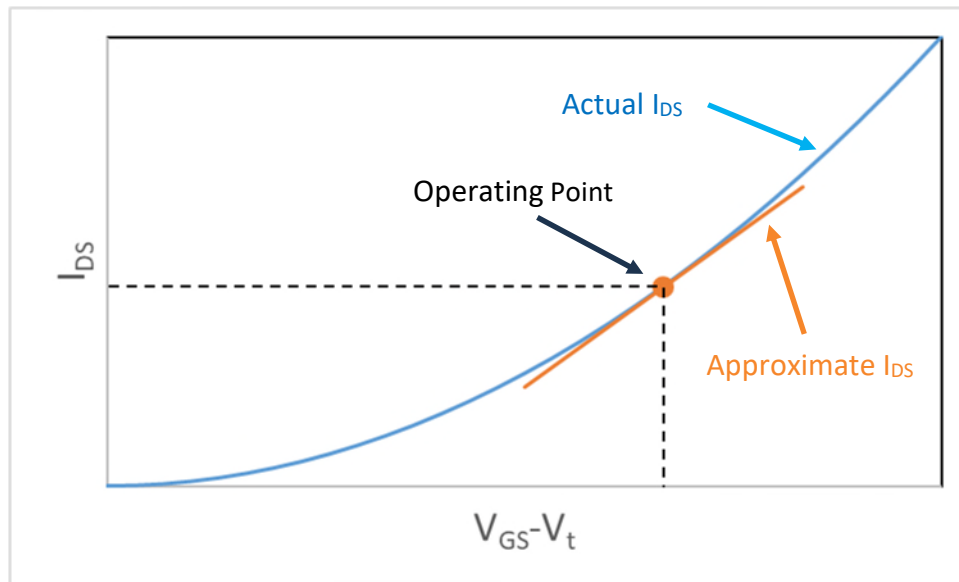


Figure 1. Plot of I_{DS} versus $V_{GS}-V_t$ and a selected operating point

48. Figure 2 shows an example of an NMOS source follower (a simple transconductance amplifier) biased by a current source connected to the transistor's source terminal. Here the NMOS transistor provides the path from input IN to output OUT, while the current source ensures that the DC current flowing through the source follower is at an appropriate level. This is important because the transconductance, g_m , of the source follower is proportional to the current flowing through it. If this current source is removed from the circuit and IN is stable (not changing) then voltage OUT will rise until the current in the source follow shuts off, reducing g_m to zero, almost certainly not the intended transconductance.

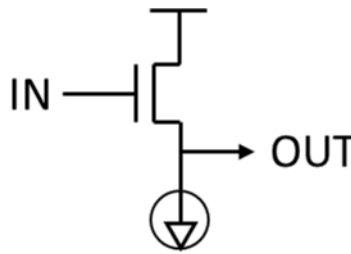


Figure 2. NMOS source follower

49. By drawing a current source in Figure 2 we're both emphasizing the "active" signal path and hiding the details of the bias circuit. More details of the bias circuit are shown in Figure 3, illustrating another level of granularity (and complexity) in the bias circuits: bias circuits typically consist of transistors (such as the output of the current mirror shown here) that directly apply the bias to the active network in the signal path from input to output, as well as reference generation circuitry that in this case delivers the constant reference current I_b . The transistors that directly apply the bias current to the active network are unique to each instance of an analog circuit and thus are drawn within the schematic of that analog circuit. The reference generation circuits, for example the circuit providing I_b here, is typically a single copy of a circuit that is shared between many individual analog circuits. Since the references are shared, they are most often not drawn inside the schematics for each amplifier or other analog block. The diode connected transistor in the current mirror may appear in either the amplifier or in the reference generation block, with the "correct" location depending upon the locality of the two circuits and

the potential for currents generated in other unrelated circuits to induce a shift in the ground level between the reference generator and the amplifier.

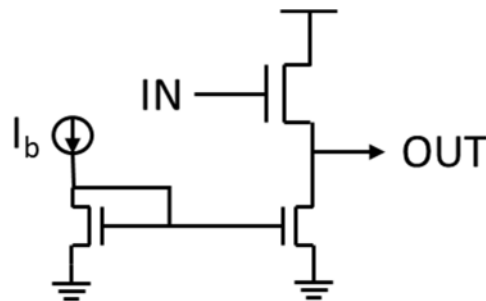


Figure 3. NMOS source follower with explicit current source biasing

50. The “reference” terminology and the concept that reference generation often happens in a unique block is shared with the Petitioner’s Rincon-Mora thesis as highlighted in Figure 6.1 from EX1015 (Figure 4 below).

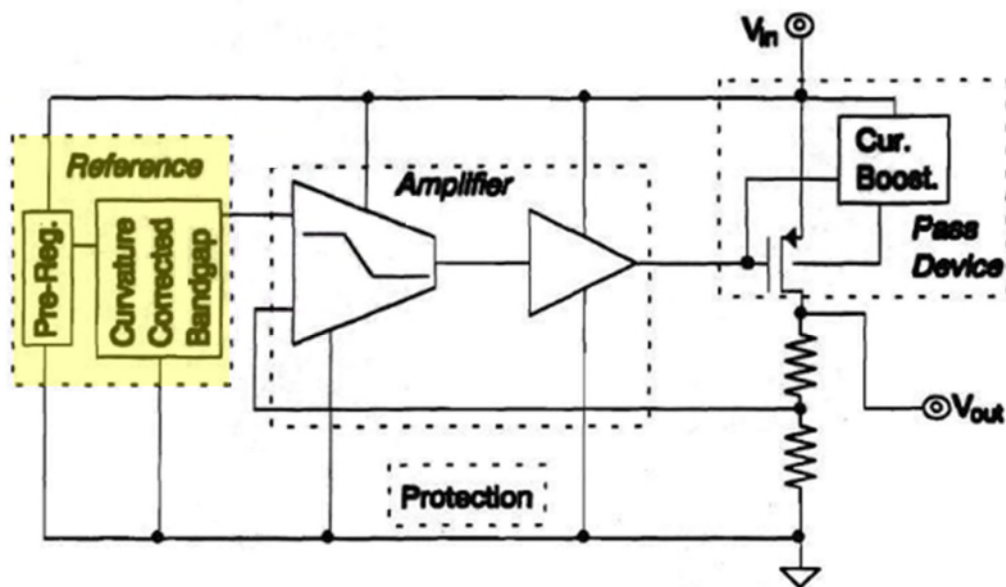


Figure 6.1. Block level diagram of the system.

Figure 4. Rincon-Mora Thesis, Fig. 6.1 (annotation added) [EX1015, 114]

51. Labeling a node as a reference implies that the voltage or current being carried by the node is precise. Reference nodes also tend to have limited drive capability: if a significant amount of current is drawn from a reference voltage then the voltage will “droop” out of specification. Circuits like regulators that use a reference voltage need to be designed to limit the load that they place upon this voltage. Similarly, reference currents can only be provided to a single load. In both cases the wires that are routed next to a reference node should be power supplies or “shields” to protect the reference from noise coupled from nearby wires.

52. Another important aspect of biasing is that reference generation circuits typically “turn on” more slowly than the bias distribution circuits that apply the bias levels to the active devices. Systems are typically very concerned with the time required to enable a circuit that has been disabled so that they can ensure that they are able to meet critical timing requirements to respond to events that may occur. Shutting off a reference generation circuit is not the same thing as shutting off the bias distribution within an amplifier both because the reference generation circuit turns on more slowly than the bias distribution and because it is often shared with other (possibly not disabled) amplifiers.

E. Voltage Regulators

53. The design of many systems requires the use of multiple power supply voltages. Rather than require the user to provide each one individually, systems are

usually built with a single, master power supply from which they derive the other voltages that they need using voltage regulators. Each voltage regulator takes an input power supply voltage² and a reference voltage and uses these to generate a new output voltage. The regulator does not significantly load³ the reference voltage, it just uses it to determine the target voltage for the output. The use of an external reference voltage allows the design of regulators that have variable (controllable) outputs and also allows a single reference generator to drive multiple voltage regulators.

54. The most widely used type of voltage regulator is known as a linear regulator. These regulators can only produce output voltages that are smaller than their input supply voltage. The excess voltage (the amount that the power supply voltage exceeds the output voltage) is “dropped” in the regulator, with this excess power being wasted as heat. These regulators are used both to filter noise in the

² The “input power supply voltage” is simply the power supply to the regulator, and is not to be confused with either of the voltages on the inputs of the error amplifier.

³ As a verb “load” means to draw current from. In this case the regulator draws essentially no current from the reference voltage input, but the output of the regulator can supply significant current to the circuit(s) which form its load. As a noun a “load” is a circuit which draws current from another circuit.

input supply from the output supply and to respond to changes in the output load current before they can lead to significant changes in the output supply voltage. For example, the regulator should be able to keep its output voltage within specifications in response to the output load switching from minimum current to maximum current very rapidly.

55. A simplified example of a linear regulator is shown below in Fig. 2 from Rincon-Mora. An amplifier (also known as the error amplifier) amplifies the difference between the reference voltage V_{ref} and the feedback voltage V_{fb} . Its output drives the output transistor which in turn drives the output voltage and the (external) load that is driven by the regulator. Finally, resistors R1 and R2 generate V_{fb} , which is provided to the error amplifier. Feedback of this sort is widely used in analog circuits: the output is “fed back” to the input, compensating for any variation (within design limits) that may occur in the amplifier, input voltage, or load by changing the control voltage applied to the output transistor.

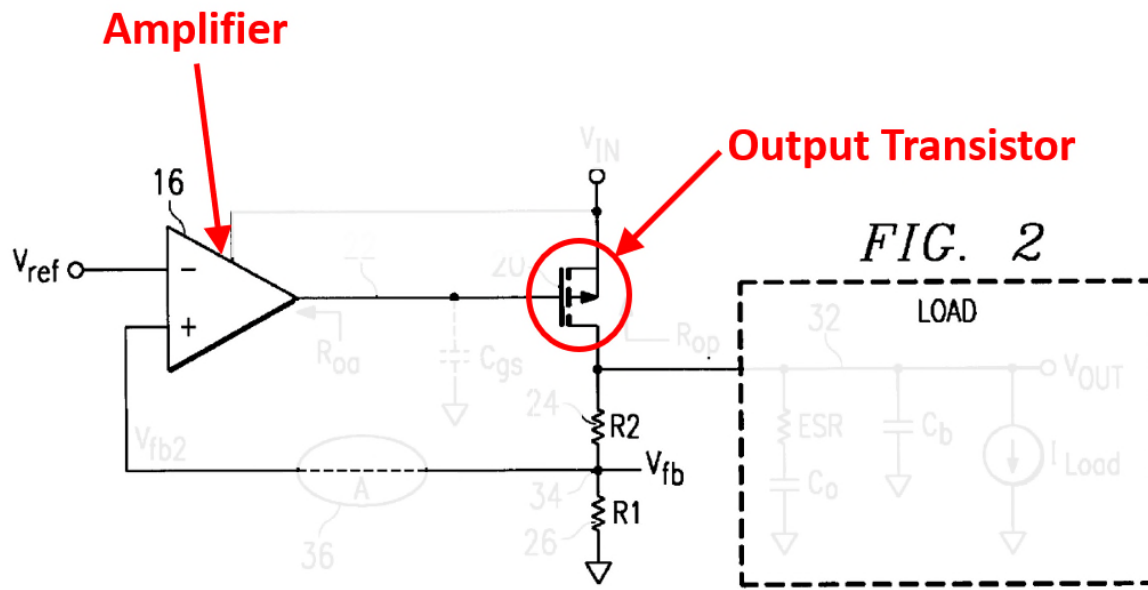


Figure 5. Rincon-Mora, Fig. 2 (annotation added) [EX1013]

F. Low Dropout (LDO) Voltage Regulators

56. When a linear regulator is capable of delivering a high-quality output voltage with only a small difference between the input and output voltages it is termed a “low dropout” (LDO) voltage regulator. To deliver a large current with only a small voltage difference the output transistor that connects the input voltage to the output voltage must have a large transconductance, and consequently a large size. The capacitance of these large transistors is difficult to drive rapidly, demanding higher transconductance from the earlier stages of the LDO and thus complicating the design of LDOs. Because the dropout voltage is small, the power wasted in an LDO is minimized.

57. Al-Shyoukh defines the key performance metrics of an LDO as low dropout voltage, high output current, low quiescent current, low transient over/undershoot. [EX1004, Introduction]

58. The power efficiency of a regulator is defined as the power delivered to the load divided by the total power dissipated in the load and the regulator. Ideally no power would be dissipated in the regulator and the efficiency would be 100%, but the efficiency of an LDO can be no higher than $\frac{V_{input}-V_{dropout}}{V_{input}}$. Minimizing the dropout voltage is thus key to keeping the power efficiency high.

59. The purpose of an LDO is to deliver current to a load at a regulated voltage. The more current it can deliver, the larger the loads it can deliver. The capability to drive larger loads comes at a cost in terms of size and other parameters, and an excessively large LDO is not desirable. Maximum load current is thus one of the key specifications reported on datasheets for regulators. Some LDOs cannot operate without a load, but instead specify a minimum load current that is only a fraction of the maximum load. In those situations the designer may need to avoid an output minimum current that is too high.

60. The other term that matters to the efficiency of the LDO is quiescent current: the current drawn by the regulator when there is no load (*e.g.*, while idling but ready for use). This is most relevant in battery power systems. I note, however,

that the relative importance of power efficiency highly depends on the application and was frequently not a significant design consideration.

61. Al-Shyoukh's final performance metric is output transient undershoots and overshoots: the quality of the voltage regulation. Figure 6 shows the undershoot and overshoot of the voltage output by a Micrel 59300 LDO when the output load current switches from very low to maximum and back. Ideally these transients would approach 0V in size, but 50mV on a 1V output (5% variation) is typical. To rapidly respond to small changes in output voltage with large changes in output current the overall voltage regulator needs high transconductance. Raising the transconductance of components of the regulator helps in delivering this overall transconductance and in making the response of the regulator faster.

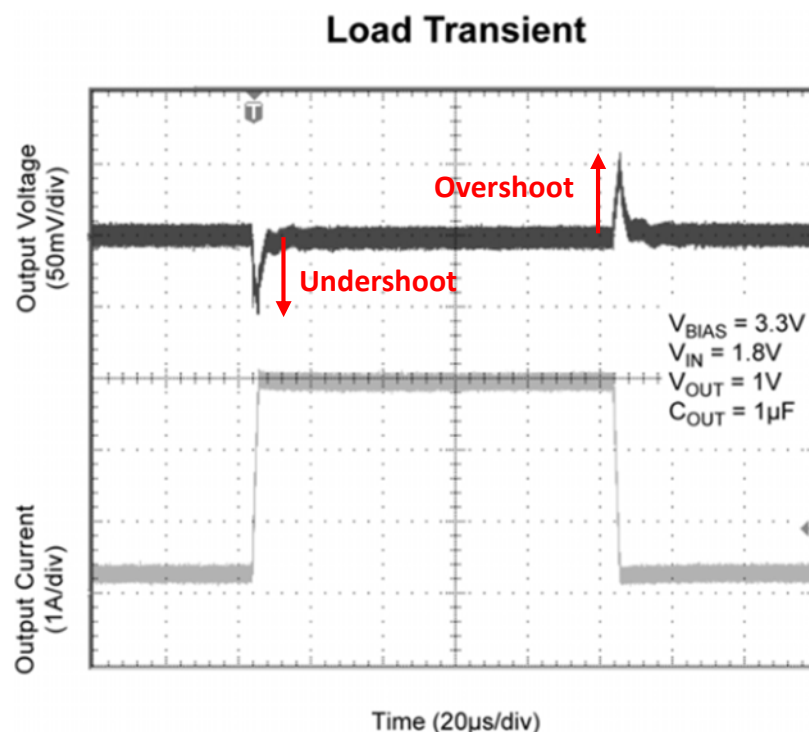


Figure 6. Load Transient (annotation added) [EX1011, 8]

62. If quiescent current is high, then it may also be desirable to have an enable/disable pin on the LDO. When the load is known to be inactive (a potentially hard question to answer in some systems) the regulator can be disabled. When disabled a low standby current is still drawn and the user would like this to be as small as possible. One tradeoff is turn-on time. A disabled regulator typically must bring its output all the way from 0V, probably 20 or more times larger than the voltage difference than is seen in the largest transient and will need much more time to get close to its target voltage than is needed during a transient. The larger this turn-on time becomes, the more likely it is that a system will not be able to utilize the enable capability, complicating the system level use of the regulator.

63. All Al-Shyoukh's parameters trade off against one another and other considerations such as cost, product lifetime, speed of operation, circuit size, operating temperature, development and validation complexity, and more. A low dropout voltage requires a large output transistor. Raising the output current will increase the dropout voltage, again leading to a larger output transistor. In either case a larger output transistor requires either more power to drive it, impacting quiescent current, or slows down the regulator increasing transient undershoots and overshoots. Decreasing quiescent current slows down the regulator, again increasing transient deviations of the output voltage. Engineering is the practice of determining how a product should be implemented to deliver an appropriate balance between all

these factors, focusing on only a single attribute to the exclusion of everything else is simply not reasonable and not something a POSITA would do. That is not to say every possible trade-off must be considered for every design, but no POSITA would design for one criterion alone to the exclusion of all others. I note that deciding when/whether to disable a voltage regulator is often a challenging exercise (which requires additional circuitry) because of the need to distinguish an idle load from the absence of a load.

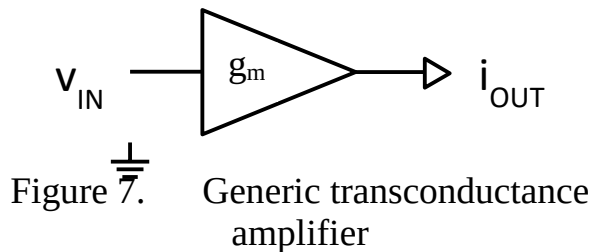
64. If the LDO is to be used with a USB port, all of these can lead to significant constraints. A notable one is that USB defines a “U1” low power state that can be used when the port is idle. Shutting a regulator down while it is idle is tempting, but the USB specification requires that the USB port complete “U1 exit” (return to normal operation – turn the regulator on and carry out any necessary logic) within 900ns, a very short time. [EX2022 (Universal Serial Bus 3.0 Specification, Revision 1.0), Table 6-21] By contrast, the Micrel MIC59300 LDO referenced by Dr. Chen in his declaration requires 300 μ s turn-on time, which would be followed by any needed logic delay to complete the USB response [EX1002, ¶114; EX1011, 5]. A simpler answer is to avoid disabling the regulator and design for very low quiescent current.

65. Voltage regulators have been around for many years, including in the 2013 timeframe (and much earlier). Various companies manufactured and sold

voltage regulators. Some companies I was personally aware of circa 2013 included Texas Instruments, ST Microelectronics, Fairchild, and Microchip. These companies adhered to the common practice of publishing public datasheets describing their product offerings, including voltage regulators. These companies made datasheets and product descriptions readily available, e.g., on their websites and via distributor websites, for the obvious reason that the companies were attempting to sell their products, including to POSITAs doing design work. The availability of electronic parts information and datasheets was so widespread that, before 2013 it was possible to use common internet search engines (such as Google and Bing) to locate electronic components and datasheets. It was also common practice for engineers to go to manufacturer websites (or distributor websites) to locate datasheets for components when designing products. I have reviewed Exhibit Nos. 2011-2012, 2016, and 2019-2020, and they are precisely the types of documents and information I was accustomed to seeing—and would expected to have seen—in voltage regulator data sheets circa 2013 (and earlier).

G. Transconductance (Gm)

66. Amplifiers that receive a voltage as an input and output a current are characterized by their transconductance, gm. A generic transconductance amplifier is shown in Figure 7 and gm is defined as the change in output current Δi_{OUT} that is caused by a given change in input voltage Δv_{IN} : $g_m = \frac{\Delta i_{OUT}}{\Delta v_{IN}}$.



67. The simplest transconductance amplifier is a single transistor source follower where the input voltage is applied to the gate and the output current is delivered by the source. The transistor drain is typically (but not necessarily) connected to a power supply. Figure 8 shows both NMOS and PMOS source followers. Note that V_{GS} is negative in the case of a PMOS source follower.

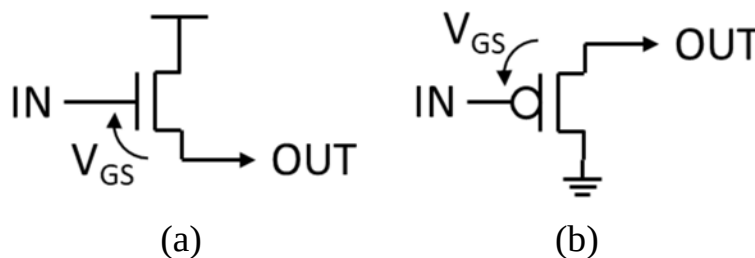


Figure 8. Source followers (a) NMOS and (b) PMOS

68. In general, g_m of a MOSFET is given by $g_m = \frac{2I_{DS}}{V_{GS} - V_t}$, where I_{DS} is the drain to source current (the output current in Figure 8), V_{GS} is the gate to source voltage, and V_t is the threshold voltage of the transistor. If a source follower is biased with a current source as seen in Figure 9, then the g_m of the combined circuit is the g_m of the source follower because the current provided from the current source doesn't change as the output voltage changes and g_m is determined by the changes in output current and input voltage and not by their absolute values. Given this information there are three different ways that the g_m of a source follower can be

raised: (1) the source follower transistor can be made bigger (e.g., a wider channel width), (2) more current can be drawn through the source follower, or (3) additional transistors can be used. These three techniques are independent of one another so it's possible to use combinations of them in the same circuit to deliver a higher overall transconductance than any single one of them delivers.

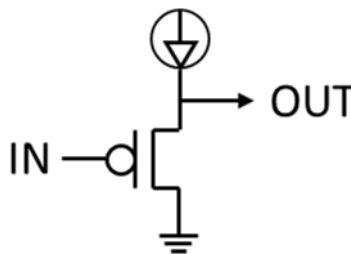


Figure 9. PMOS source follower with current source load

69. First, making the source follower transistor wider without changing the current through it reduces the current density in the transistor which in turn reduces $V_{GS}-V_t$. This reduces the denominator of $g_m = \frac{2I_{DS}}{V_{GS}-V_t}$, raising g_m . On the other hand, the wider transistor also raises the input capacitance of the source follower. If the goal is to reduce loading on the stage that is driving the gate of the source follower, this approach will raise the input capacitance (loading) faster than it improves g_m often making it an unattractive solution.

70. Second, raising the current through the source follower increases the numerator of $g_m = \frac{2I_{DS}}{V_{GS}-V_t}$, increasing g_m . This raises the power drawn by the circuit, but it increases g_m without increasing the loading upon the stage driving the source

follower. Furthermore, the bias current can be changed dynamically, allowing the circuit to have a high g_m at critical times and low power when low g_m is acceptable. This is the approach used by Rincon-Mora in his “transient response boost circuit,” which he also called a “transient boost circuit.” [EX1013, Fig. 3, 1:10-17, 2:57-64] The '074 patent refers to this approach as gm-boost. [EX1001, 4:15-23]

71. The third approach to raising g_m is to use a different circuit topology. The simplest modification to raise the g_m of a source follower is shown below in Figure 10. Here current sources are used to bias both the source and drain of the source follower. Notice that this doesn't increase the power of the circuit because the same current I_b is flowing through both current sources. If signal IN rises, this will reduce the magnitude of V_{GS} , which in turn reduces the magnitude of I_{DS} - the (negative) current flowing through the PMOS transistor. Since I_b remains unchanged, the reduction in I_{DS} is now delivered into node OUT, which raises the voltage by charging the capacitance on this node. This charging stops when OUT rises enough to return V_{GS} to its original value. While node OUT is charging up, the same amount of current also discharges the drain capacitance of the PMOS because the lower I_b current source is also unchanged, leaving a portion of this current to discharge the drain voltage. An additional amplifier is then used to amplify the drain voltage to further drive node OUT without placing any additional loading on node IN. Note that the same amount of charge is available to charge up node OUT and to

discharge the drain of the PMOS device. In the common case where node OUT is driving a large capacitance while the drain is more lightly loaded, the drain voltage will be an amplified and inverted version of the change on node OUT, allowing a simple amplifier to substantially add to the g_m driving node OUT.

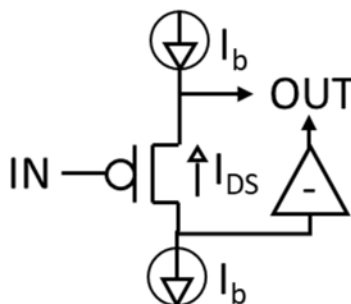


Figure 10. PMOS source follower with enhanced g_m

VIII. SUMMARY OF THE '074 PATENT

72. The '074 patent, “USB Regulator with Current Buffer to Reduce Compensation Capacitor Size and Provide for Wide Range of ESR Values of External Capacitor,” relates to USB voltage regulators, particularly the use of a current buffer to reduce compensation capacitor size and increase tolerance to a wide range of external compensation capacitor ESR (equivalent series resistance) values. [EX1001, 1:17-21]

73. USB regulators typically have very low ESR, e.g. $\sim 10\text{m}\Omega$. Capacitor manufacturers rarely specify ESR values, and minimum ESR values even more rarely. Furthermore, the actual ESR can depend upon how the circuit board is laid out and assembled. This variation can be significant when compared to the stability

requirements of prior art regulator designs, leading to unstable operation when seemingly innocuous changes are made in manufacturing. By adding a current buffer between the error amplifier and the output transistor, the inventors have found a way to make a USB regulator that tolerates significant variation in the external compensation capacitor while maintaining the performance and stability of the regulator.

74. This tolerance to external compensation capacitor variation is delivered by pushing the pole at the gate of the output transistor to a high frequency, leaving the voltage regulator dominated by the low frequency pole at the output of the first stage (error) amplifier. The dominance of this pole causes the regulator to act like a single pole system, which is unconditionally stable. Because the output transistor is large (in order to drive the large output load), pushing this pole to high frequency requires the addition of a large g_m (high transconductance) current buffer between the error amplifier and this output transistor, as shown in Figure 2 of the '074 patent (Figure 11 below, where the added current buffer driver and supporting blocks are highlighted).

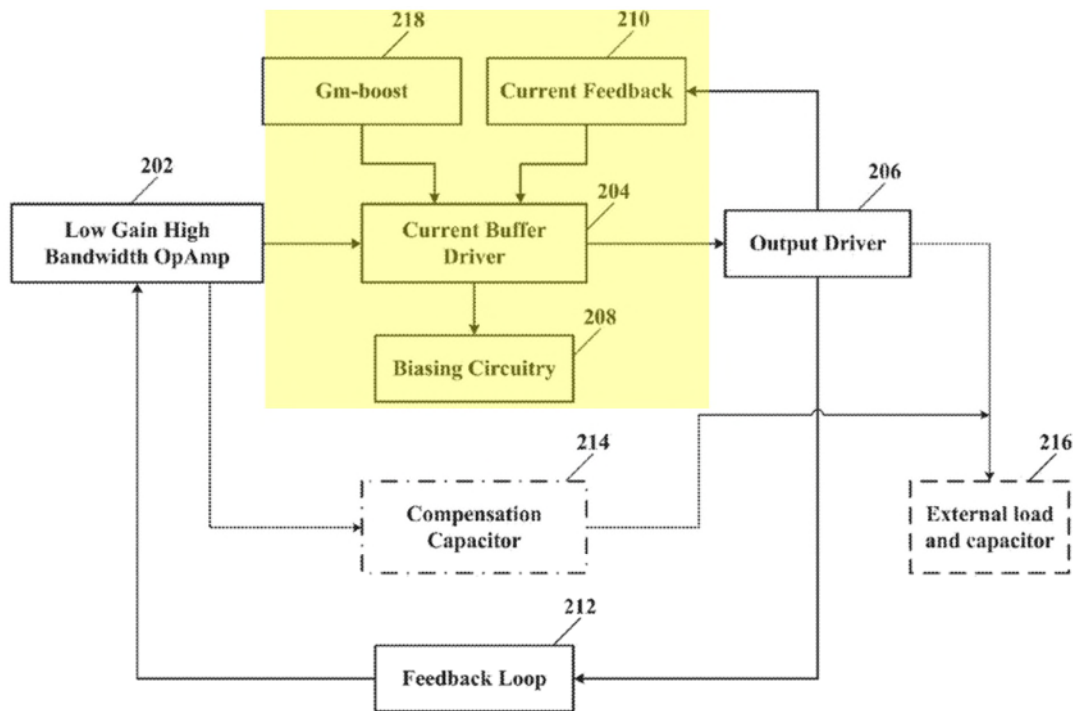


FIGURE 2

Figure 11. '074, Fig. 2 (with annotation) [EX1001]

75. ***Gm-boost***⁴ controls the g_m of source follower 384 by biasing it with a current that is proportional to the output driver current. Unlike ***gm-boost[ing]***, ***gm-enhance[ment]*** steers the bias currents (i_{bias} , i_{sf} , and i_{mirror}) that are already flowing in Figure 3B of the '074 patent (Figure 12 below) in the steady state. I note that because ***gm-boost*** and ***gm-enhancement*** (discussed below) are achieved using different circuits and techniques their respective benefits are additive to one another.

76. When the input voltage and the load current are stable for a long time the voltage regulator is in “steady state” – the voltages inside the regulator are not

⁴ Claim language is shown in ***red italics***.

changing but current continues to flow. If we focus on the gate of PMOS 380, the output transistor, in Figure 3B there are currents flowing both into and out of node B but they are of equal magnitude so the voltage on node B doesn't change.

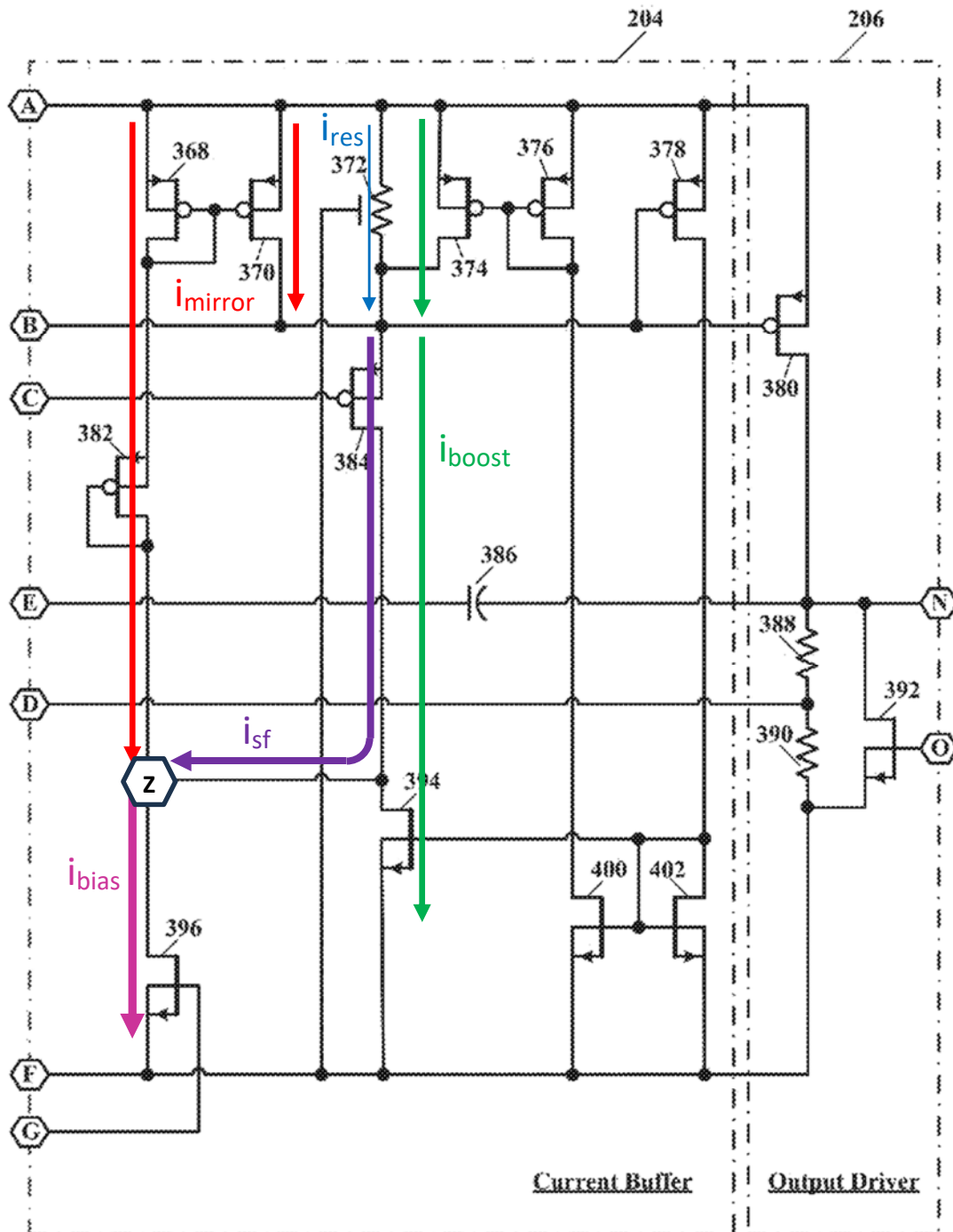


FIGURE 3B

Figure 12. '074, Fig. 3B (annotation added) [EX1001]

77. **Gm-boost** controls the **i_{boost}** current marked in green in Figure 3B. In the steady state **i_{boost}** is delivered to node B by PMOS 374, pulling it up, and drained

from node B through the source follower and current source 384, equally pulling node B down. This current flowing through source follower 384 boosts its g_m , because the g_m of a source follower is proportional to the current flowing through it.

78. ***Gm enhance[ment]*** controls the other currents annotated on Figure 3B. Current source 396 delivers i_{bias} (in magenta) to the current buffer driver at the node labeled “Z” above. There it divides into two parts, i_{mirror} (in red) which flows to PMOS devices 382 and 368, and i_{sf} in purple, which flows through source follower 384, pulling down on Node B. Because PMOS 368 and 370 form a current mirror, i_{mirror} also flows through PMOS 370 into node B, pulling it up. Finally, there is a current i_{res} (in blue) through resistor 372 that also flows into node B pulling it up. In the steady state the voltage on node B doesn’t change, so i_{sf} must equal $i_{mirror} + i_{res}$. The voltage on node Z controls how i_{bias} is split into i_{mirror} and i_{sf} , shifting current from i_{mirror} to i_{sf} when node Z rises and from i_{sf} to i_{mirror} when it falls. Knowing how i_{bias} flows when nothing is changing, we’re prepared to see how ***gm enhance[ment]*** works.

79. If the load current increases, it pulls the output N of the regulator down. The error amplifier responds to this change by dropping node C. This increases the V_{gs} of PMOS 384, increasing the current through it and pulling nodes B and Z closer together. Because B has a lot of capacitance due to the large size of driver 380, it

moves more slowly. But when node Z rises, it shifts current from i_{mirror} to i_{sf} which results in i_{mirror} through PMOS 370 pulling up less strongly on node B, helping source follower 384 pull node B down. If the transistors in current mirror 368/370 are the same size as each other then this action doubles the g_m contribution made by the diverted current. If transistor 370 is larger than transistor 368, then the diverted current makes an even larger g_m contribution to current buffer driver 204. As a result, current buffer driver 204 has a g_m that is larger than the g_m of just source follower 384. If the load current decreases, the same reactions occur but in the opposite direction and again the g_m of current buffer driver 204 is larger than the g_m of just source follower 384.

80. The arrow sizes do not imply anything about the relative sizes of i_{bias} and i_{boost} . Since i_{boost} changes dynamically there is no fixed ratio between the two currents.

81. Phrasing this explanation differently, gm-boost controls the g_m of source follower 384 by changing the current that flows through it, biasing it with a current that is proportional to the output driver current. When output current is high, *gm-boost[ing]* delivers a high current into node B through PMOS 374 and then out of node B through source follower 384. When output current is low, these same currents into and out of node B are lowered together. Unlike *gm-boosting*, *gm*

enhance[ment] steers the bias currents that are already flowing in Figure 3B in the steady state.

IX. CLAIM CONSTRUCTION

82. For purposes of my Declaration, I have applied the district court’s ruling that element 1[d] (**an enable/disable function to enable/disable the biasing circuit for reducing standby current**) is not a means-plus-function term. [EX3001, 9] The other two terms that the district court construed (for claim 4, 8, and 9) do not affect my analysis. [*Id.*, 12-17]

83. I have been asked to opine on how a POSITA would understand the **gm-boost** and **gm enhanced** limitations (elements 1[c] and 1[b], respectively) in view of the intrinsic and extrinsic evidence. I have been informed by counsel that claim terms using different language are presumed to have different meanings.

84. **Gm-boost.** As noted in ¶**Error! Reference source not found.**, Rincon-Mora described his circuit development as both a “transient response boost circuit” and a “transient boost circuit.” [EX1013, Fig. 3, 1:10-17, 2:57-64] The ’074 patent continues the use of “boost” terminology to describe dynamically controlling the current through the source follower buffer so that g_m is proportional to the voltage regulator’s output current as **“gm-boost[ing],”** stating: “The **gm-boost circuit 218** may provide a **gm-boost technique** that will increase the impedance value of the current buffer driver 204 with the help of the current feedback 210 which may sense

the current change at the output of the output driver 206.” [EX1001, 4:15-20] **Gm-boost** can thus be summarized as raising the overall/total current through the source follower using output current feedback to raise its g_m when high g_m is needed.

85. **Gm enhance[ment]**. The '074 patent discloses multiple different circuit techniques for raising the effective g_m of a source follower circuit, techniques described in ¶¶**Error! Reference source not found.**-71. Fig. 3B of the '074 patent shows two different circuit techniques are used: both **gm-boost** and **gm enhance[ment]**. **Gm enhance[ment]** is illustrated in Fig. 3B below, yielding a current buffer 204 that provides a g_m greater than that provided by just source follower 384.

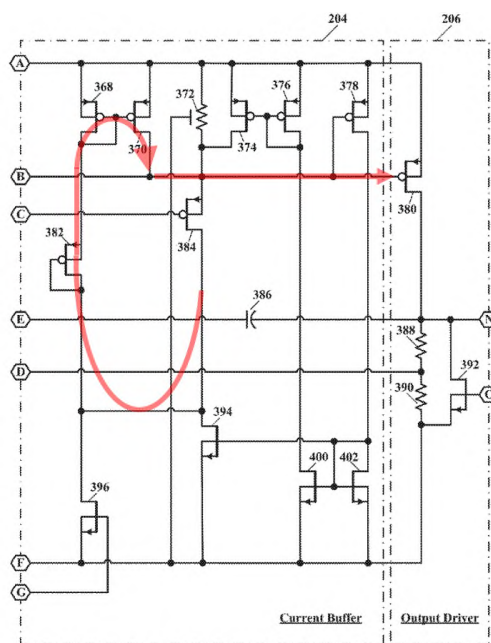


FIGURE 3B

Figure 13. '074, Fig. 3B (annotated to show **gm enhance[ment]**) [EX1001]

86. As annotated in Fig. 3B, if the voltage on node C rises, the current through source follower 384 is reduced (because it is a PMOS transistor), causing the excess bias current to be redirected through current mirror 368/370 into node B (viz., the gate capacitance of the power output transistor 380) (indicated by the red arrows in the figure). If PMOS transistors 368 and 370 are the same size, the redirected current provides additional g_m equal to that of source follower 384, doubling the overall g_m of the circuit. Sizing PMOS transistor 370 to be larger than transistor 368 will cause the g_m to be further enhanced. If instead the voltage on node C drops, transistor 384 sources more current because it is a PMOS device and its V_{gs} is increased. This, in turn, enhances g_m because some current previously flowing through transistor 368 now flows through 384 to account for the increased current through transistor 384. This is ***gm enhance[ment]*** to which element 1[b] refers and is not the same as ***gm-boost*** (which employs a different mechanism). In other words, g_m -boost changes the overall **magnitude** of the standing (bias) current, whereas ***gm enhance[ment]*** changes the **allocation** of where the bias current is deployed. Furthermore, ***gm-boost*** is implemented in Figure 3B using transistors 374, 376, 378, 394, 400, and 402 while ***gm-enhance[ment]*** is implemented by transistors 368, 370, and 382, a separate set of transistors.

87. It is significant (especially from an engineering/POSITA perspective) that the combined effects of ***gm-boost*** and ***gm-enhance[ment]*** are cumulatively

greater than the effect either achieves by itself. Equating **gm enhance[ment]** with **gm-boost** would negate this cumulative effect. This interpretation means that any system that meets 1[c] will necessarily meet 1[b], rendering 1[b] meaningless. This is not how a POSITA would understand the two related, but distinct, concepts. But that is what Petitioner and its expert, Dr. Chen, do. [Pet. 16-17, 58-59; EX1002 ¶¶53-55, 142-144]

X. SUMMARY OF THE PRIOR ART

A. Rincon-Mora

88. According to the Petitioner, Rincon-Mora is a set of two (and sometimes three) references, a patent, a technical paper, and a thesis. The patent [EX1013] lists Nicolas Salamina as a co-inventor, the paper [EX1014] lists Phillip E Allen as co-author, and the thesis [EX1015] is authored by Gabriel Rincon-Mora. The technical paper emphasizes that the regulator has “made the low-voltage design viable for battery powered circuits.” [EX1014, 8 (VI. Conclusion)] The thesis concludes “Circuit techniques have been developed and verified that permit the practical realization of low drop-out regulators in a single, low-voltage battery cell environment to be feasible in current existing technologies.” [EX1015, 175 (8.4 Conclusion and Recommendations)]

89. Focusing on the Rincon-Mora patent [EX1013] the invention claims to deliver “[a]n improved low-dropout (‘LDO’) voltage regulator incorporat[ing] a

transient response boost circuit which is added to the slew-rate limited node at the control terminal of the LDO voltage regulator output transistor and provides improved transient response performance to the application of various load current step stimuli while **requiring no standby or quiescent current during zero output current load conditions.**” [EX1013, Abstract (emphasis added)] The patent further states “the present invention relates to a current efficient LDO voltage regulator ... and yet **requires no standby current during zero output current load conditions**” [EX1013, 1:13-17 (emphasis added)] and “[i]n a preferred embodiment disclosed herein, a transient boost circuit is added to the slew-rate limited node and **requires no standby current during zero output current load conditions.**” [EX 1013, 2:4-7 (emphasis added)]⁵

90. This objective is delivered through the introduction of a gain stage between the error amplifier and the output PMOS transistor as shown in Fig. 5A (see Figure 14 below). Rincon-Mora Fig. 3 is similar and provides more detail.

⁵ The Rincon-Mora paper says its LDO regulator has 23 μA of quiescent current. [EX1014, Abstract] A POSITA reading the Rincon-Mora patent and Rincon-Mora paper together would understand that he is saying 23 μA of quiescent current is tantamount to “no” quiescent current such that it need not be considered further, including for battery applications.

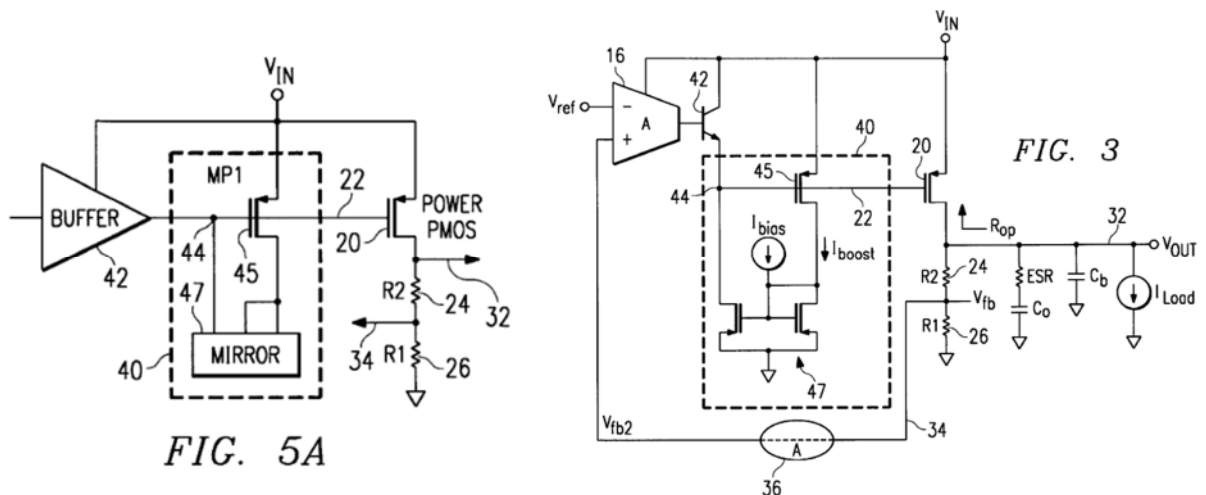


Figure 14. Rincon-Mora, Fig. 5A, Fig. 3 [EX1013]

91. Notable in Fig. 5A is that the current that is used to bias buffer 42 is proportional to the output current supplied to the load by power PMOS 20. If the load current is zero, then this bias current will also be zero, leading to the repeated statement that the LDO requires no quiescent current during zero output load current conditions. [EX1013, Abstract, 1:13-17, 2:4-7] Despite this very low quiescent current, the bias supplied to buffer 42 rapidly increases as the output current increases, raising the speed of the regulator, allowing it to control the gate of power PMOS 20 more quickly, and improving the regulator's transient response. This can be seen in Figure 15 below, where waveform "a" shows the step response (the response to a sudden change in load current) of an LDO according to Rincon-Mora and waveform "b" shows that of a "conventional LDO voltage regulator used similarly biased conditions." [EX1013, 3:19-21] Here it is readily observed that the initial portions of the a and b waveforms appear to match, but Rincon-Mora's LDO

generates a response much more rapidly than the conventional LDO that generates

b. This more rapid response results in a much smaller deviation of the voltage waveform from its final value (blue dashed line) for waveform a (in green) than for waveform b (in red).

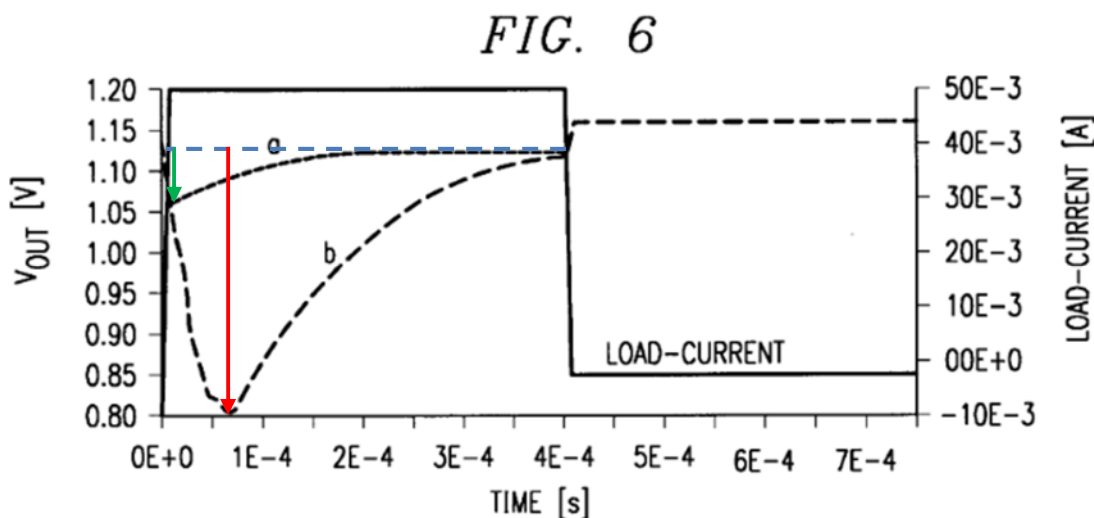


Figure 15. Rincon-Mora, Fig. 6 (annotation added) [EX1013]

B. Al-Shyoukh

92. Mohammad Al-Shyoukh, along with co-authors Hoi Lee, and Raul Perez, wrote “A Transient-Enhanced Low-Quiescent Current Low-Dropout Regulator With Buffer Impedance Attenuation.” [EX1004] This paper (hereafter “Al-Shyoukh”) presents an LDO with many similarities to Rincon-Mora (including a transient boost circuit), but also provides shunt feedback to the source follower (BJT Q20 in Figure 16 below). And it includes a much more rigorous analysis of the stability of the resulting regulator than is present in the Rincon-Mora patent. Al-Shyoukh achieves a quiescent current of 20- μ A [EX1004, Abstract] (an even lower

quiescent current than Rincon-Mora) and states “[t]he LDO is able to achieve low dropout voltage of 200 mV and deliver 200-mA load current for portable power management applications with lithium-ion batteries.” [EX1004, 10 (V. Conclusion)]

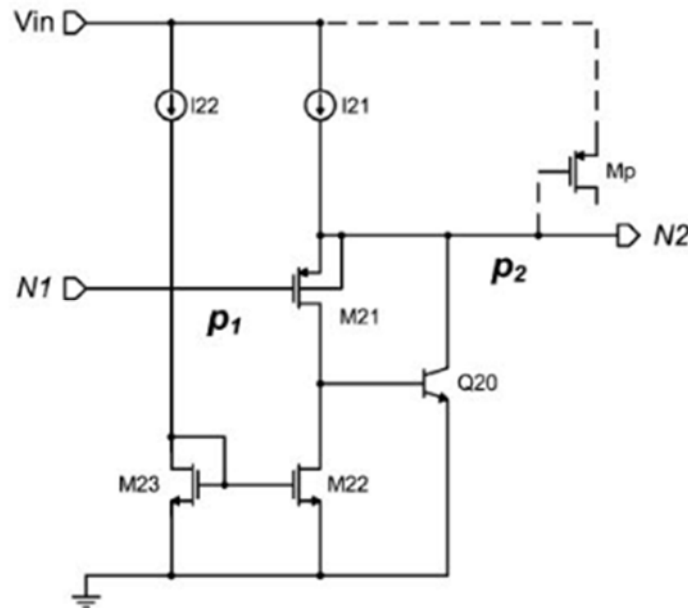


Figure 16. Al-Shyoukh, Fig. 3a, Source-follower with shunt feedback
[EX1004, 3]

93. The LDO regulator that Al-Shyoukh proposes is shown in Figure 17 below. Like Rincon-Mora, Al-Shyoukh includes an intermediate stage amplifier (“Impedance Attenuated Buffer”), but a PMOS source follow instead of an NPN emitter follower. This Impedance attenuated buffer is also dynamically biased using feedback from the output PMOS transistor M_p but using a different circuit topology than Rincon-Mora, and in addition it includes shunt feedback.

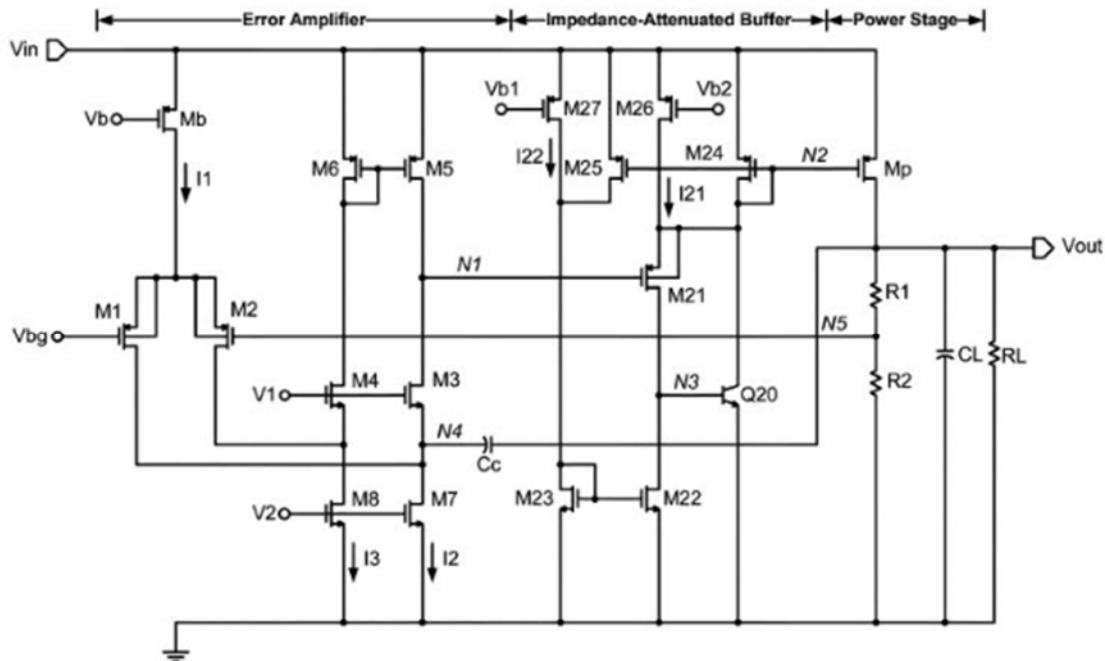


Figure 17. Al-Shyoukh Fig. 8 [EX1004, 7]

94. The replacement of the NPN emitter follower used in Rincon-Mora with a PMOS source follower is significant in that the output of an NPN emitter follower is approximately 0.7V lower than its input, while the output of a PMOS source follower is higher than its input. This higher output value makes it easier to turn off output transistor M_p under zero output current conditions.

95. Al-Shyoukh includes a thorough stability analysis of his circuit, which resulted in phase margin varying from 69° (good) to $>85^\circ$ (better) across more than 5 orders of magnitude variation in load current, as shown in Figure 18 below. At the same time, he delivers four times the load current supported by Rincon-Mora (200mA versus 50mA) at a slightly lower quiescent current. It's unclear how much of this improvement is due to the higher g_m available in the $0.35\mu\text{m}$ technology used

by Al-Shyoukh versus the 2 μ m technology used by Rincon-Mora (5 generations of technology). [EX1004, Table II]

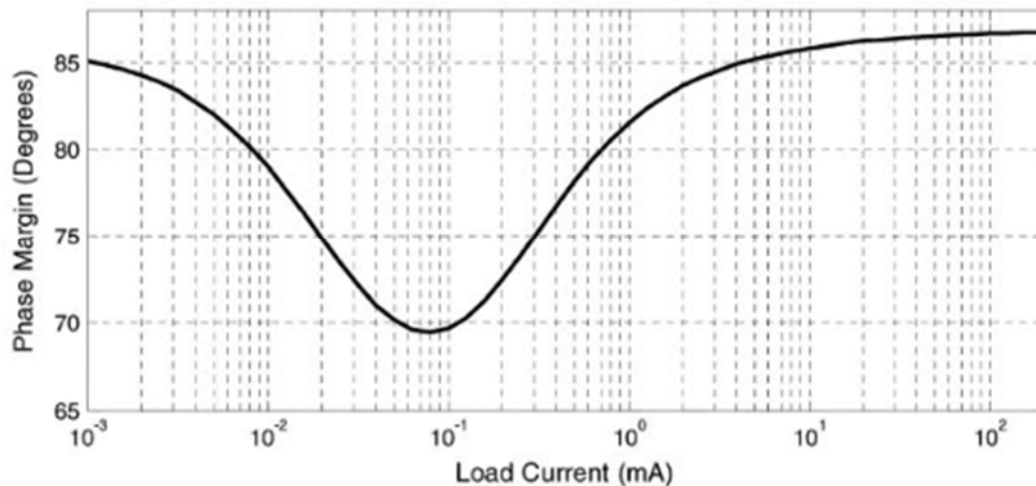
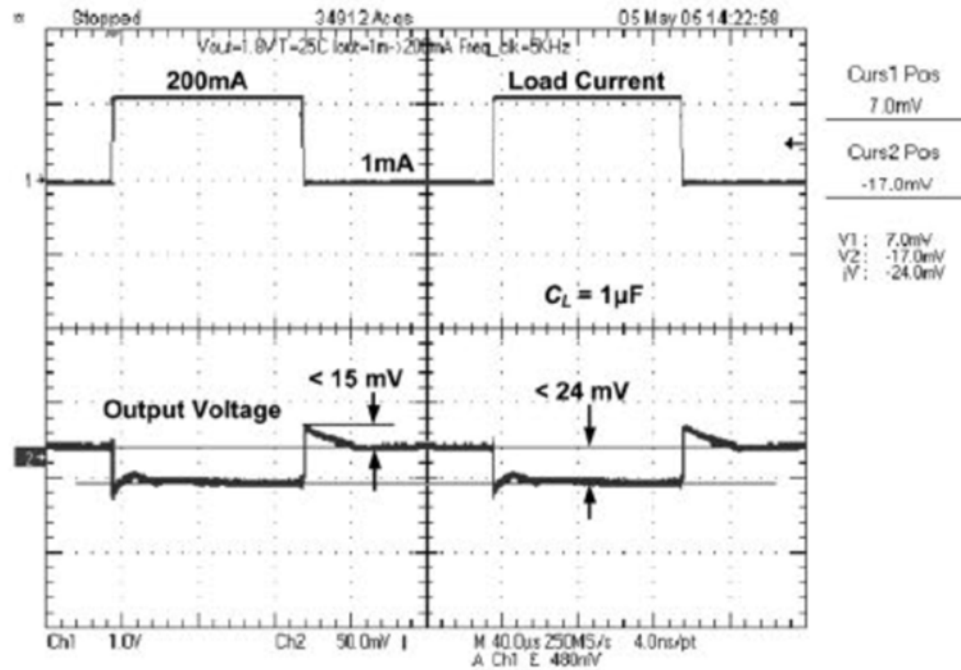
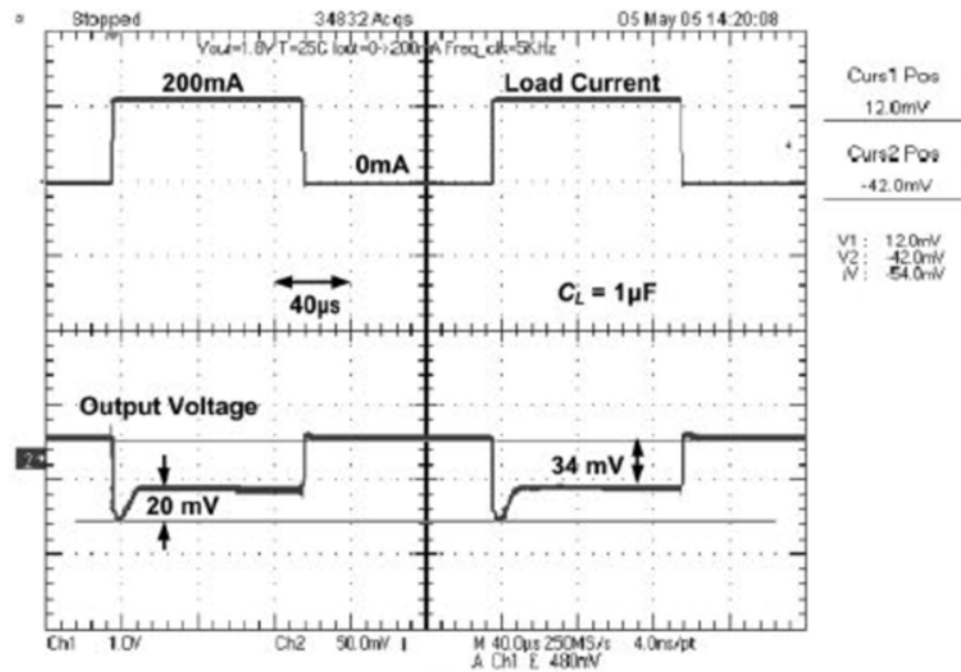


Figure 18. Al-Shyoukh, Fig. 7 [EX1004, 7]

96. As seen in Figure 19 below, Al-Shyoukh's LDO has approximately 1% undershoot (20mV on a 1.8V supply) for a 0 to 200mA output load current transition and under 1% overshoot for a 200 to 1mA output load current reduction (this is worse than the 200 to 0mA transition). There is about 1.5% DC variation in the output voltage between 1mA and peak load. There is an additional 10mV of DC droop when the low load is dropped to 0mA, an anomalously large value, but still overall the regulation is very good due to the high speed and high gm of the regulator.



(a)



(b)

Figure 19. Al-Shyoukh, Fig. 11, Measured load transient response [EX1004, 9]

97. Figure 20 shows a summary of Al-Shyoukh's results compared with 5 prior papers. Compared to Rincon-Mora (which is reference [1] in Al-Shyoukh), Al-Shyoukh delivers four times the load current at a slightly lower quiescent current. Al-Shyoukh does not say how much of this improvement is due to the higher gm available in the 0.35 μ m technology used by Al-Shyoukh versus the 2 μ m technology used by Rincon-Mora (5 generations of technology). [EX1004, Table II]

TABLE II
PERFORMANCE COMPARISON WITH PREVIOUSLY REPORTED LDOS

	1998 [1]	2000 [3]	2003 [4]	2004 [5]	2005 [17]	This Work
Technology (μ m)	2.0	1.0	0.6	0.5	0.09	0.35
V_{do} (V)	0.3	N.A.	0.2	N.A.	0.3	0.2
$I_{L,max}$ (mA)	50	200	100	160	100	200
I_q (mA)	0.023	0.03	0.038	0.025	6	0.02
Current Efficiency at $I_{L,max}$ (%)	99.5	N.A.	N.A.	N.A.	94.3	99.8
ΔV_{out} (mV)	19	220	130	200	90	54
T_r (μ s)	1.8	1.1	2	2.75	0.00054	0.27
C_L (μ F)	4.7	1	10	2.2	0.00060	1
ESR Zero Required	No	Yes	Yes	No	No	No
FOM (ns)	8.2	0.165	4.9	0.43	0.032	0.027

Figure 20. Al-Shyoukh, Table II [EX1004, 10]

C. Ivanov

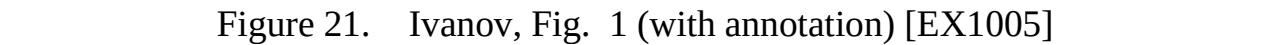
98. Ivanov (U.S. Pat. 6,400,207) is a patent entitled "Quick Turn-On Disable/Enable Bias Control Circuit for High Speed CMOS Opamp," and lists Vadim Ivanov and Shilong Zhang as the inventors. "[It] relates generally to start-

up circuits for integrated circuit applications. More particularly, [it] relates to a quick turn-on disable/enable bias control circuit for use in conjunction with high speed CMOS amplifiers, particularly CMOS amplifiers used in high speed video multiplexing applications.” [EX1005, 1:6-11] Being focused on the enable/disable circuit, the specification is silent on the question of *set[ting] a biasing ratio for gm-boost of the current buffer driver* and provides essentially no information on how reference generation circuits are to be built. Instead, it responds to a user supplied “shutdown” signal to enable or disable the reference voltage output. While Ivanov’s title has the word “Quick Turn-On” in it, a POSITA would understand that any circuit which can be enabled/disabled (including Ivanov’s) incurs some amount of a delay penalty when coming out of the disabled state.

99. Ivanov offers embodiments based on several variants of bandgap circuits. [EX1005, Figs. 1, 3, and 4] This class of circuits offers the generation of currents that are proportional to absolute temperature (PTAT) and voltages that are robust in the face of process, supply voltage, and temperature variations. One challenge of bandgap circuits is that they have two potential operating states: a metastable state where they draw no current and do not deliver a usable output, and a stable, nonzero current state where they deliver well-regulated outputs. As a result of this characteristic, there are a wide variety of “start-up circuits” that yank the

bandgap out of the zero current state without significantly impacting the normal operating state of the circuit.

100. Looking at Ivanov's Fig. 1 (Figure 21 below), the capacitor C0 provides noise immunity on a high impedance node when the circuit is operating. The reference generator turns off when $V_{SHUTDOWN}$ is low, turning on M_{11} and turning off M_3 (yellow highlighting). If the voltage on capacitor C0 were to drop to zero volts when the reference generator is operating, then M_6 would stop carrying current, the rest of the reference generation circuit 2 would completely shut down and start up only very slowly. Ivanov includes trickle charge circuit 3 to avoid the occurrence of this situation.



operating again and stabilize in about 100 to 150 ns. [EX1005, 6:28-36] The precise time will depend upon the difference in voltage between the trickle charge output and the operating voltage of C0, with the former being dependent upon how long the circuit has been in “shutdown” (viz., with longer standby time resulting in longer startup time) and the latter depending upon temperature. And additional time will be needed to distribute the reference voltage to all of its receivers and for them to turn on in response to its arrival.

102. Importantly, the trickle circuit charge works continuously, even when V_{SHUTDOWN} is high. This adds an offset to the circuit, which under normal operating conditions applies the same voltage to the gates of M_0 and M_{11} and the same currents to their drains. The trickle current will thus result in the output voltage/current being both off target and increasing its temperature sensitivity.

103. Understanding the impact of this trickle charge current requires some understanding of how bandgap circuits work, but none of this information is included in the Ivanov patent. To summarize, Ivanov presents a method to enable and disable a *reference generation* circuit. It includes essentially no information on how to build a reference generation circuit. And Ivanov says nothing whatsoever about **set[ting] a biasing ratio for gm-boost of the current buffer driver**. It appears Ivanov was included purely because the words “enable/disable bias control circuit”

are present in the title of the patent and, in hindsight, match some of the language in claim 1[d].

XI. RESPONSE TO THE PETITIONER’S ARGUMENTS AND DR. CHEN’S DECLARATION

A. Petitioner Conflates Gm Boosting With Gm Enhancement and Fails to Show Gm Enhancement in Either Ground

104. Claim 1 of the '074 patent is:

1.	A voltage regulator, comprising:
1[a]	an operational amplifier
1[b]	a gm enhanced current buffer driver;
1[c]	a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver;
1[d]	an enable/disable function to enable/disable the biasing circuit for reducing standby current;
1[e]	an output power driver, wherein the current buffer driver is coupled between the operational amplifier and the output power driver;
1[f]	a current feedback circuit coupled between the output power driver and the current buffer driver; and
1[g]	a feedback loop coupled between the output power driver and the operational amplifier.

105. As noted in ¶¶68-71, there are multiple circuit techniques that can be used to raise the effective g_m of a source follower. Rincon-Mora dynamically controls the current through the source follower being used as a buffer so that g_m is proportional to the output current being delivered by the voltage regulator and refers

to this technique as both a “transient response boost circuit” and a “transient boost circuit.” [EX1013, Fig. 3, 1:10-17, 2:57-64] The ’074 patent uses similar terminology, calling this approach “ g_m -boost”:

The g_m -boost circuit 218 may provide a g_m -boost technique that will increase the impedance value of the current buffer driver 204 with the help of the current feedback 210 which may sense the current change at the output of the output driver 206.” [EX1001, 4:15-20]

106. As explained in ¶¶84-87 above, equating ***gm-boost*** with Rincon-Mora’s “Transient (Response) Boost” matches what is recited in claim 1[c]: this boost technique forces the g_m of the source follower to be proportional (ratioed) to a current elsewhere in the circuit, in Rincon-Mora’s case to the current in the output PMOS 20 of the voltage regulator (see Rincon-Mora Fig. 3 below).

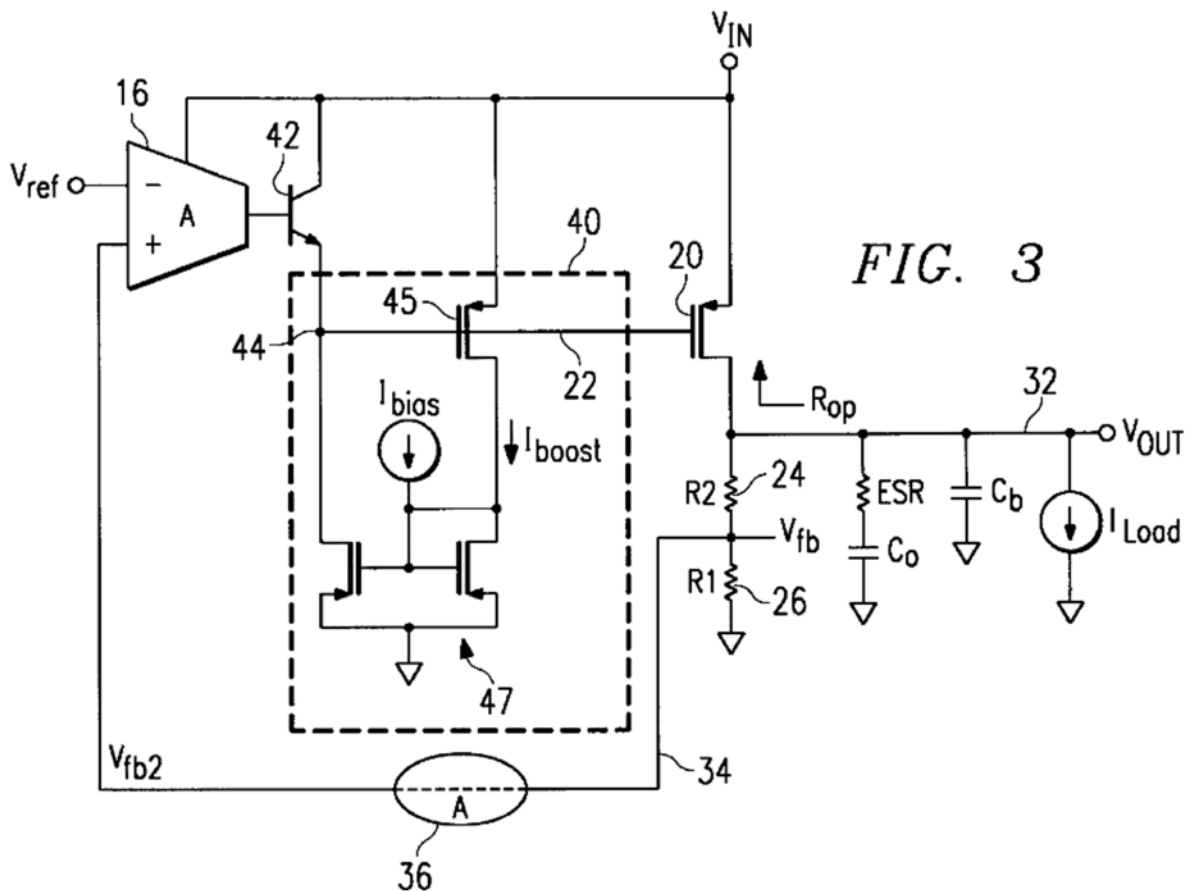


Figure 22. Rincon-Mora, Fig. 3, showing transient boost circuit 40 [EX1013, 4:32]

107. On the other hand, **gm enhancement** is a different method to increase the g_m of the circuit, one that offers benefits that are additional to those offered by **gm-boost**. [¶¶Error! Reference source not found.-Error! Reference source not found.] Treating the two different terms as synonyms ignores the improvement in g_m offered by employing both techniques together.

108. Petitioner contends that “Rincon-Mora’s buffer driver is **gm enhanced** because the transient boost circuit, comprising transistor 45 and current mirror 47,

Figure 23. Rincon-Mora, Fig. 3, including annotations by Dr. Chen [EX1013, EX1002, ¶142]

109. Equating **gm enhance[ment]** with **gm-boost** would mean that any system that meets claim 1[c] will necessarily also meet claim 1[b], and improperly

conflates the two different claim limitations, contrary to how a POSITA would understand them. The difference between the two is confirmed by the '074 patent specification, which shows a current buffer 204 that delivers a g_m that is greater than that provided just by source follower 384, around which the current buffer is based, in Figure 3B (seen below). Here we can see that if the voltage on node C rises, the current through source follower 384 is reduced, with that reduction the bias current is redirected through current mirror 368/370 into node B (viz., the gate capacitance of the power output transistor 380). If PMOS devices 368 and 370 are the same size, then this redirected current will provide an additional g_m equal to that of source follower 384, doubling the overall g_m of the circuit. If PMOS device 370 is larger than 368, then the g_m will be further enhanced. On the other hand, if the voltage on node C falls, then the opposite set of changes occur, again enhancing the overall g_m of the circuit. This is the ***gm enhancement*** to which claim 1[b] refers, and it is not the same as ***gm-boost*** (which employs a totally different mechanism as described in ¶¶70-71). The techniques are different, with ***gm enhance[ment]*** reallocating bias current while ***gm-boost*** dynamically raises bias current. Together the combined g_m is superior to what either technique offers by itself.

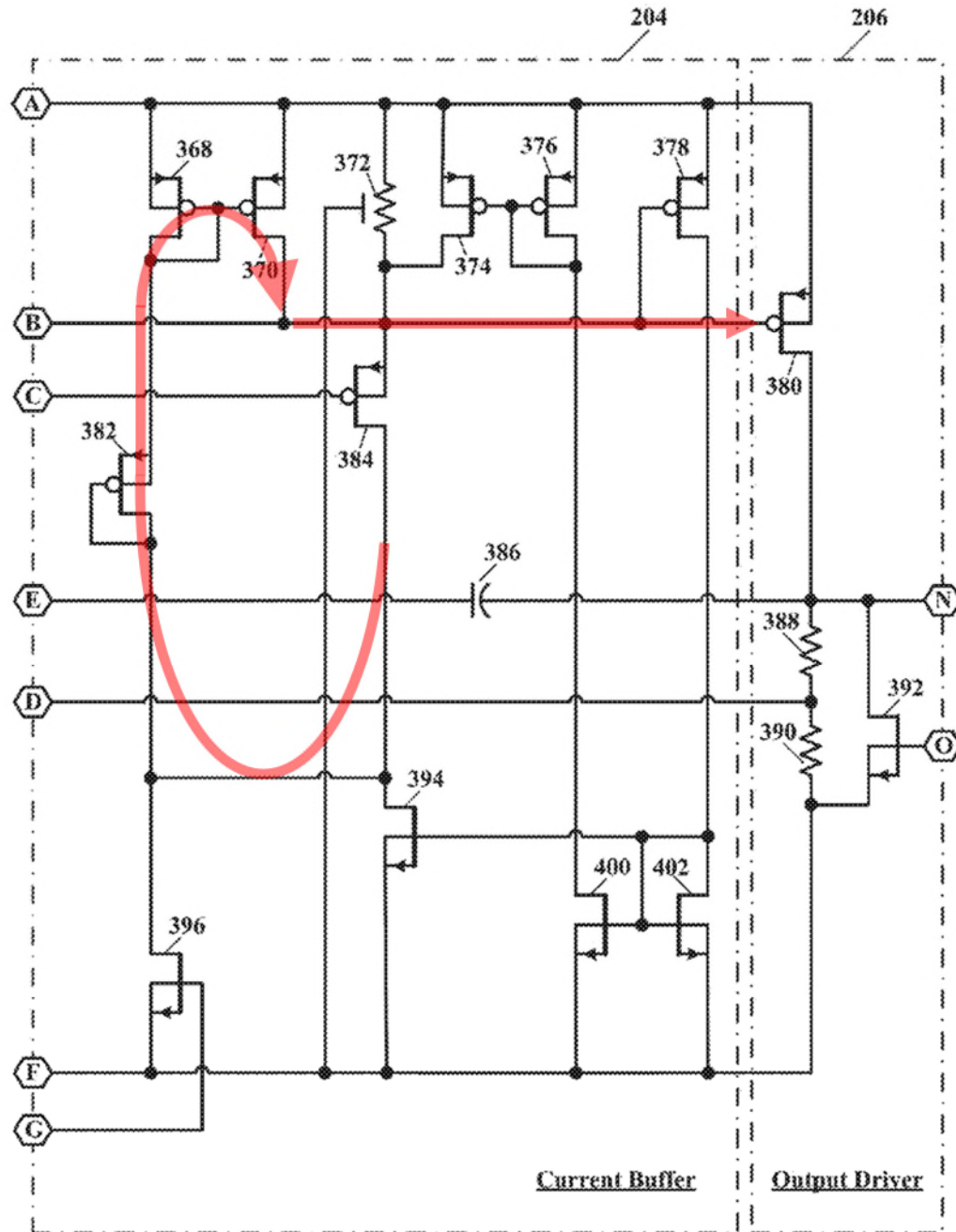


FIGURE 3B

Figure 24. '074, Fig. 3B with annotation showing *gm enhance[ment]* [EX1001]

110. Dr. Chen states “I have explained above in my summary of Rincon-Mora how its circuit includes a current feedback system (shown in blue below) that

enhances the gm of the buffer driver (green)...” [EX1002, ¶142] and then two paragraphs later concludes with “Given that Rincon-Mora’s buffer and the ’074 patent’s buffer are both structurally and functionally similar, a POSITA would have understood Rincon-Mora’s buffer to be a current buffer to the same extent that the ’074 patent’s buffer is a current buffer.” [EX1002, ¶144 (quotation marks omitted)] Nowhere does Dr. Chen describe Rincon-Mora demonstrating *gm enhance[ment]* (reallocation of existing bias current), only *gm-boost[ing]* (changing the total amount of bias current). Without *gm enhance[ment]*, clearly there is no *gm enhanced current buffer driver*.

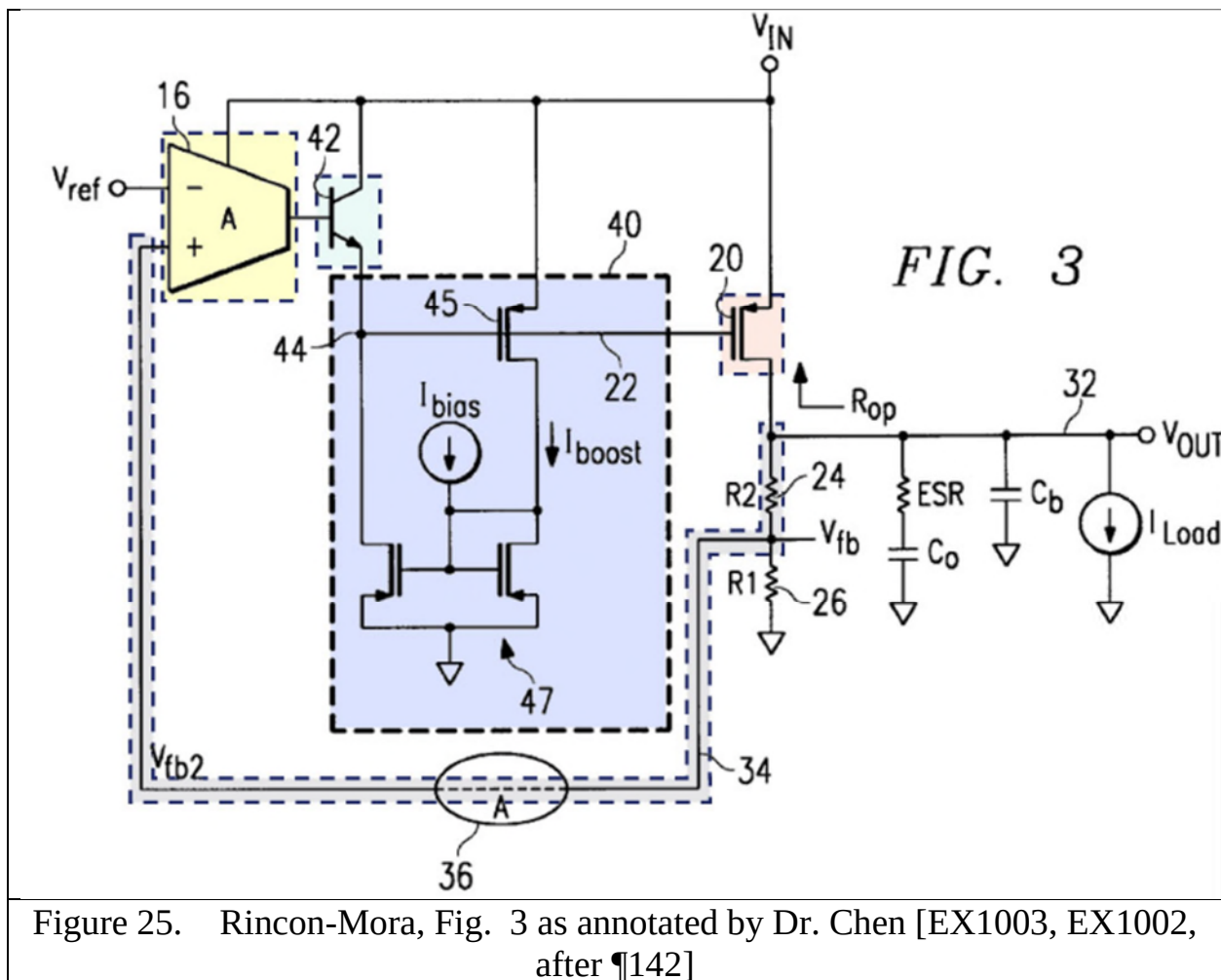


Figure 25. Rincon-Mora, Fig. 3 as annotated by Dr. Chen [EX1003, EX1002, after ¶142]

111. The same flawed arguments are presented with respect to Al-Shyoukh. Petitioner states that “Al-Shyoukh’s buffer is ‘**gm enhanced**’ because it receives a **gm boost**.” [Pet., 16] Dr. Chen states “I have explained above in my summary of Al-Shyoukh how its circuit includes a current feedback system that enhances the gm of transistor M_{21} ...” [EX1002, ¶53] and then two paragraphs later concludes with “Thus, it is my view that regardless of what precisely is meant by current buffer driver, Al-Shyoukh discloses the same current buffer driver that the ’074 patent discloses.” [EX1002, ¶55 (quotation marks omitted)] Nowhere do Petitioner or Dr.

Chen describe Al-Shyoukh demonstrating *gm enhance[ment]* (reallocation of existing bias current), only *gm-boosting* (changing the amount of bias current). Without *gm enhance[ment]*, clearly there is no *gm enhanced current buffer driver*.

B. Petitioner Fails to Show the Claimed “Biasing Circuit ...” in Either Ground

112. Claim element 1[c] recites *a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver*.

Petitioner fails to show that either Al-Shyoukh or Rincon Mora meet this requirement.

113. The Petitioner proposes the argument:

Al-Shyoukh’s LDO uses a biasing circuit coupled to the buffer driver to set a voltage V_{b1} at the gate of transistor M_{27} , providing a bias current I_{22} that is mirrored across transistors M_{23} and M_{22} to set a biasing ratio for gm-boost of the current buffer driver. (EX1002 ¶¶ 56-58; EX1004, Fig. 8.) [Pet., 17]

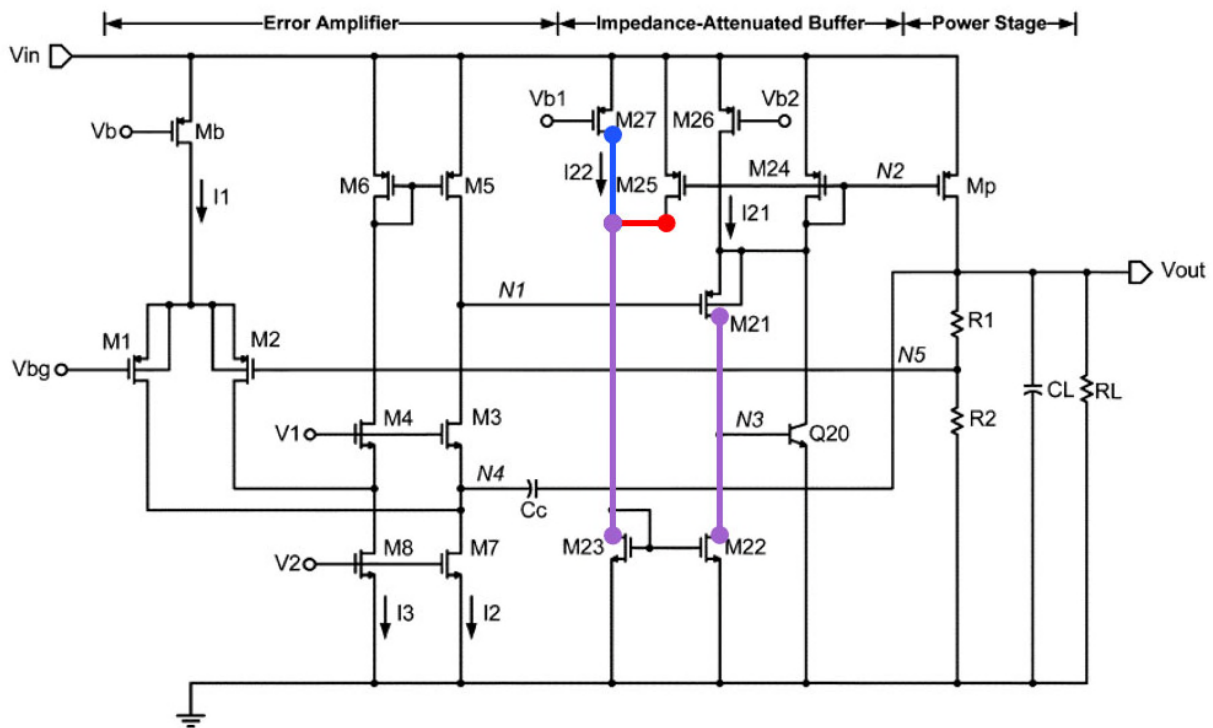


Figure 26. Al-Shyoukh, Fig. 8 (as annotated in Petition) [Pet., 19, EX1004]

114. In the Petitioner’s argument the biasing circuit (not shown) determines the current provided by M27. This current is added to the **gm-boost** current provided by M25 and the total current is then mirrored by M23/M22 where it biases the drain of source follower M21. Rather than **a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver**, at most there is “a biasing circuit coupled to the circuit that **set[s] a biasing ratio for gm-boost of the current buffer driver.**” In the former the **biasing circuit** participates in **set[ing] a bias ratio** while in the latter the **biasing circuit** is merely coupled to the circuit that **set[s] a biasing ratio.**

115. The Petitioner then compounds this error in the next paragraph:

This matches the patent's description of a bias network "fixed by transistor 396" such that the current from the network is "ratio'ed in transistors 368 and 370" with a feedback current. (EX1001, 5:15-24.) [Pet., 17-18]

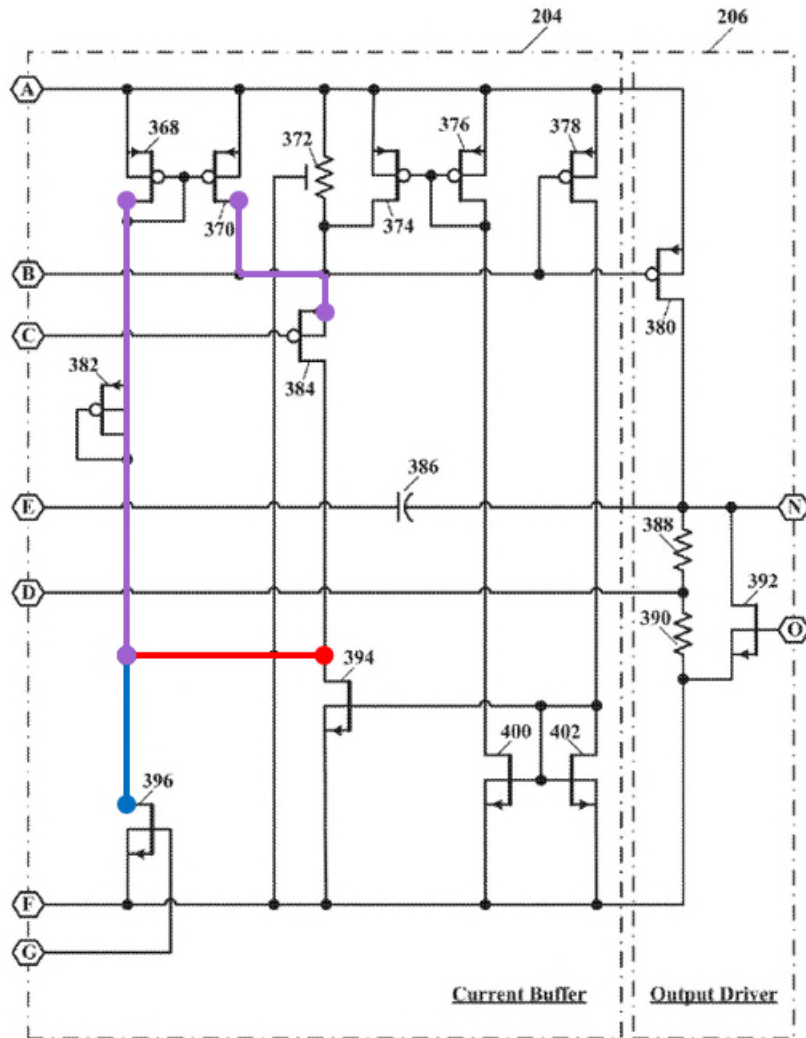


FIGURE 3B

Figure 27. '074, Fig. 3B (as annotated in Petition) [Pet., 18, EX1001]

116. The Petitioner has matched portions of the *gm-boost* circuit in Al-Shyoukh and the *gm enhancement* circuit in the '074 patent in the hope that this will hide the fact that no *biasing circuit[ry] ... to set a biasing ratio for gm-boost*

of the current buffer driver has been identified. Both happen to use current mirrors which have ratios, but the transistors identified in the '074 patent are not part of the *gm-boost* circuitry.

117. Similarly, in ¶¶56-59 of his declaration, Dr. Chen shows (see Figure 28 below) that there is a bias circuit coupled to the current buffer driver (“A POSITA reading Al-Shyoukh would have understood that, although not shown, the voltage V_{b1} at the gate of M_{27} is provided by a biasing circuit” [EX1002, ¶56]) and he shows that there is a circuit to set a biasing ratio for gm-boost of the current buffer driver (“In addition, the figure above shows the feedback current from M_{25} in red, and the summed current, flowing into M_{23} , and mirrored to M_{22} , in purple.” [EX1002, ¶56]).

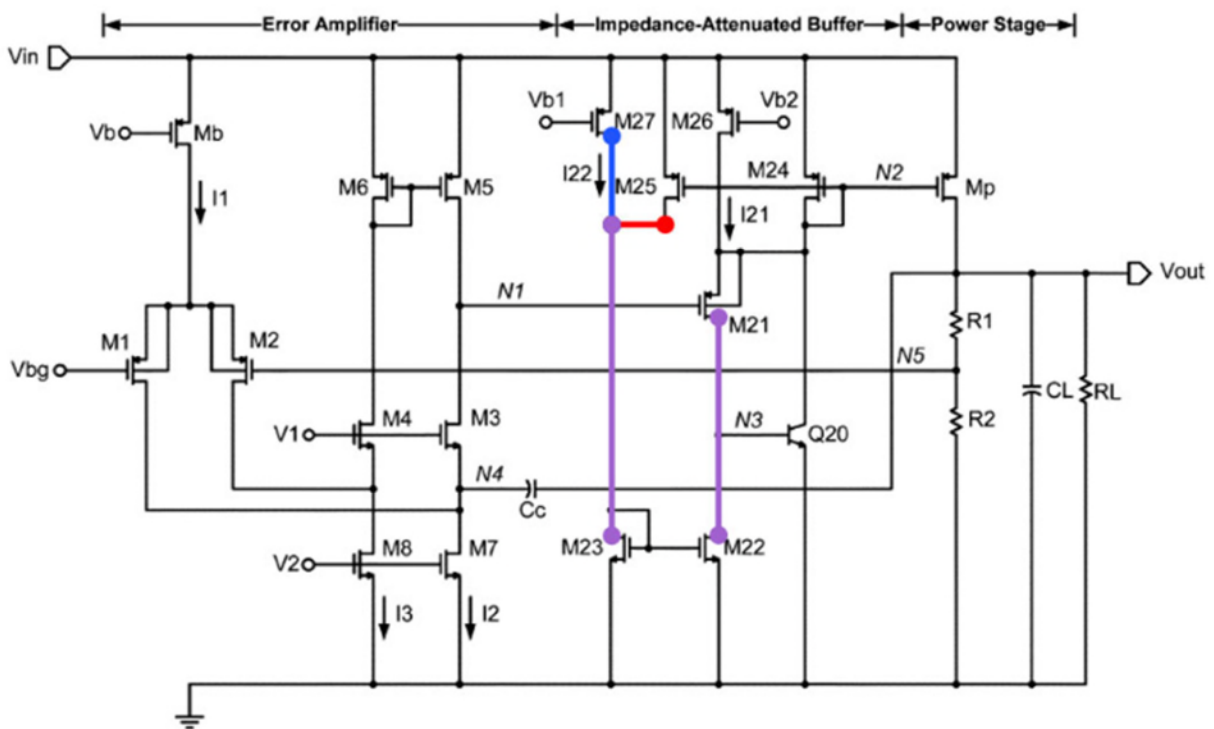
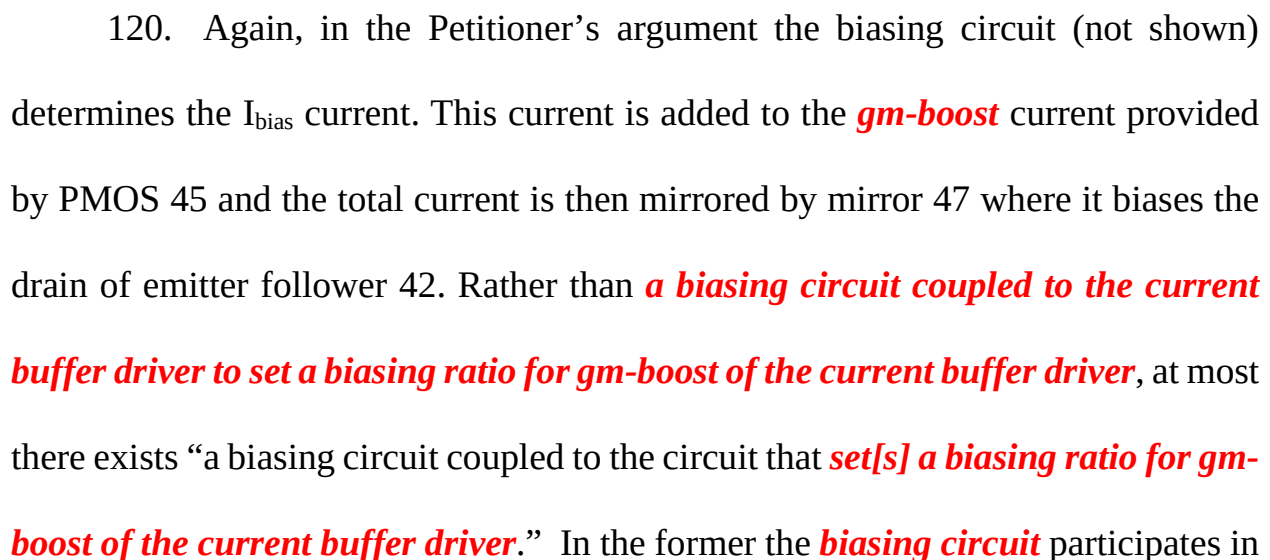


Figure 28. Al-Shyoukh, Fig. 8 as annotated by Dr. Chen [EX1002, ¶56]

118. The biasing circuit that Dr. Chen identifies determines the current provided by PMOS M27. This circuit does not **set a biasing ratio**, it merely provides a portion of the current going to the circuit that sets the bias ratio, M22 and M23 in his depiction. A POSITA would recognize that in this schematic the **gm-boost** is supplied by the current provided by M25, and the **biasing ratio for gm-boost** (the fraction of the output driver current that biases the source follower) is given by the size ratio: $\frac{M25 \times M22}{M27 \times M23}$. The design of the identified bias circuit and the size of M27 do not appear in this ratio because M27 and its bias circuit do not set the biasing ratio for gm-boost of the current buffer driver, instead M27 provides a constant bias current.

119. When discussing Rincon-Mora, the Petitioner's argument suffers from similar flaws, starting with:

Rincon-Mora's LDO uses a biasing circuit coupled to the buffer driver to set a bias current I_{bias} that is mirrored in current mirror 47 to set a biasing ratio for gm-boost of the buffer driver. (EX1013, 3:55-62, 4:30-65, 7:35-41, Figs. 1, 3; EX1002 ¶¶ 145-49.) [Pet., 59]



set[ting] a bias ratio while in the latter the *biasing circuit* is merely coupled to the circuit that *set[s] a biasing ratio*.

121. In the following paragraph the Petitioner again compares a portion of the *gm-boost* circuit in Rincon-Mora to the *gm enhancement* circuit in the '074 patent because both happen to contain current mirrors, ignoring the fact that no *biasing circuit[ry] ... to set a biasing ratio for gm-boost of the current buffer driver* has been identified.

122. Dr. Chen repeats this same mistaken analysis in ¶¶145-146 of his declaration for the Rincon-Mora ground. Here the current provided by the identified bias circuit is shown in blue in his Fig. 3 (Figure 30 below), while the independent boost current I_{boost} is shown in red. He correctly identifies the bias ratio: “As the Rincon-Mora Paper explains, this boost increases the slew-rate current of the error amplifier as $I_{\text{sr}} = I_{\text{bias}} + I_{\text{boost}} = I_{\text{bias}} + kI_{\text{load}}$, where I_{load} is the load current and **k is the mirror ratio between transistors 20 and 45.** (EX1014, 38.)” [EX1002, ¶146 (emphasis added)]. However, the bias circuit Dr. Chen relies on does not “set” the bias ratio, instead it provides the quiescent current that keeps the regulator operating when there is no output current and is completely independent of the identified [bias] ratio between transistors 20 and 45.

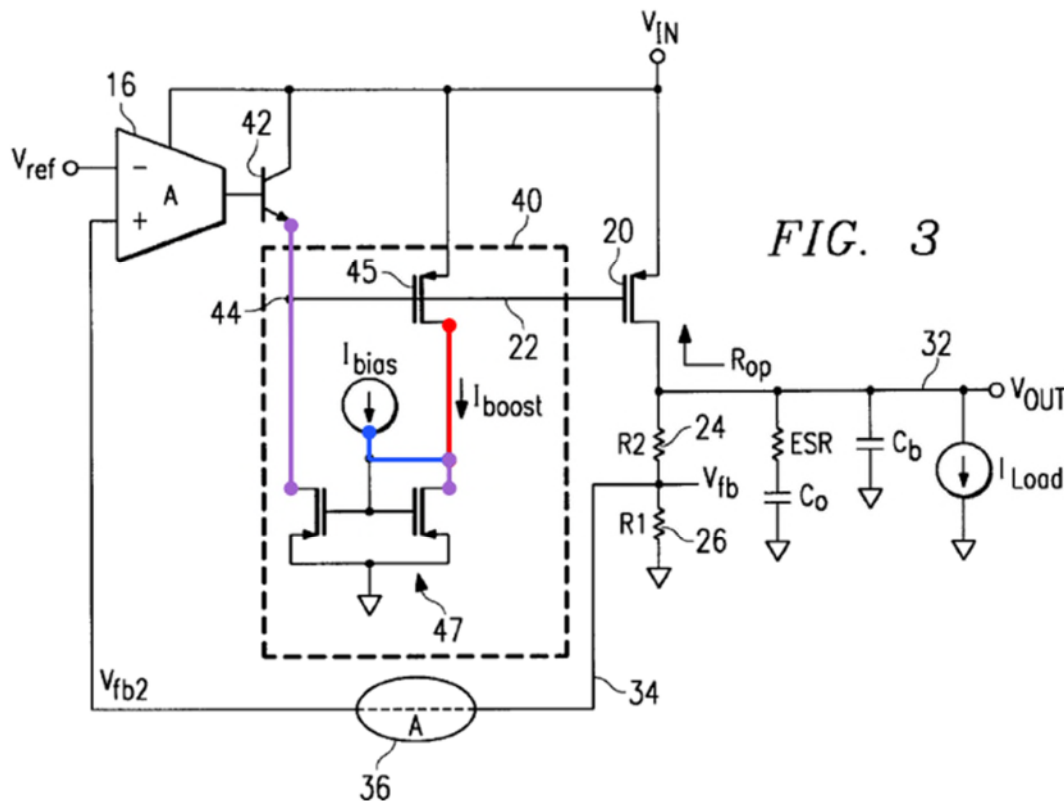


Figure 30. Rincon-Mora, Fig. 3 (as annotated by Dr. Chen) [EX1002, ¶145; EX1013]

123. In ¶149 Dr. Chen asserts that even if **biasing ratio** is understood to mean a ratio of current that the current buffer draws from DC relative to the current feedback circuit then Rincon-Mora LDO's biasing circuit (which he never identifies) would still meet 1[c]. The Petition says the same thing. [Pet., 20] The only basis provided for this interpretation is "Patent Owner's expected claim constructions." [Id., fn. 2] Patent Owner pursued no such claim construction. In any event, the assertion makes no sense, especially without further context. Dr. Chen says "The Rincon-Mora LDO's biasing circuit provides a bias current I_{bias} , and a POSITA would have understood that adjusting the biasing circuit to set I_{bias} would have

allowed the circuit designer to set a ratio of current drawn from DC and current drawn from the feedback circuit (I_{boost}). (EX1013, Fig. 3.)” [EX1002, ¶149] But I_{bias} is a constant current while I_{boost} varies dynamically. How is the designer to set a ratio between a fixed quantity and a varying quantity? The ratio will continuously vary as the output current changes, it is never “set.”

124. The Petition makes a slightly different argument, that Rincon-Mora’s current mirror 47 is somehow analogous to “a current that is ratio’ed in transistors 368 and 370 with a current provided by the feedback circuit.” [Pet., 59 (quotations marks omitted)] But current mirror 47 is part of Rincon-Mora’s gm-boost circuit, while the ’074 patent’s transistors 368 and 370 are part of the *gm enhancement* circuit and do not *set a biasing ratio for gm-boost of the current buffer driver*.

C. Petitioner Fails to Establish a Legitimate, Non-Hindsight Motivation to Combine Ivanov with Either Rincon-Mora or Al-Shyoukh

125. Petitioner and Dr. Chen employ the same inadequate rationale to combine Ivanov with Rincon-Mora (Ground 2) or Al-Shyoukh (Ground 1). Both admit that neither Rincon-Mora nor Al-Shyoukh meet claim element 1[d], “*an enable/disable function to enable/disable the biasing circuit for reducing standby current*.” [EX2018, 128:17-129:6 (“Q. What claim elements in Claim 1 are missing from the Al-Shyoukh reference? A. ... So Al-Shyoukh satisfies most of these claims, except for the 1D, the enable/disable function. Q. What elements of Claim 1 are

missing from the Rincon-Mora reference? A. Yeah, so counsel, the combination for Rincon-Mora is Claim 1D, the enable/disable function.”)].

126. Citing power efficiency, Petitioner combines Ivanov with Rincon-Mora and Al-Shyoukh in an attempt to meet claim 1[d]:

- Both Rincon-Mora and Ivanov are highly concerned with power efficiency, and Ivanov’s mechanism saves power by shutting off unused circuitry. [Pet., 64]
- Rincon-Mora’s LDO in combination with Ivanov discloses 1[d]. [Pet. 62]
- POSITA “would have recognized Ivanov’s bias circuit model, including its disable/enable control mechanism, to be useful and suitable for Rincon-Mora’s LDO. One of Rincon-Mora’s main objectives is to improve power efficiency and reduce quiescent current.” [EX1002, ¶157]
- Al-Shyoukh is highly concerned with power efficiency, and Ivanov’s mechanism saves power by shutting off circuitry when it is not needed. [Pet., 25]
- Al-Shyoukh with Ivanov discloses 1[d]. [Pet., 22]
- POSITA “would have recognized Ivanov’s bias circuit model, including its disable/enable control mechanism, to be useful

and suitable for Al-Shyoukh's LDO. One of Al-Shyoukh's primary overall objectives is to improve power efficiency and reduce quiescent current." [EX1002, ¶67]

- "I mainly show Ivanov, you know, how they can use that transistors in 11 and that sh[u]tdown circuits to perform the enable and disable function." [EX2018, 225:6-20, 231:13-20].

127. Nowhere do the Petitioner or Dr. Chen address the fact that power management is a system level problem, that the system designer will focus on the big sources of power first, and that system level solutions have implications beyond the block in which a change (such as the addition of enable/disable functionality) is made. Instead, they propose the addition of an enable/disable circuit as a simple, painless solution to an insignificant problem. In doing so they ignore the significant impact of Ivanov's "charging reference current" of 0.1 to 5 μA and "trickle charging current" of 1 to 2 μA circuit on the existing 20 or 23 μA quiescent current. [EX1005, 5:39-41, 5:54-58] These are examples of using hindsight to justify the combination of references that fail to explain why POSITA would be motivated to do so.

128. Rincon-Mora and Al-Shyoukh were motivated by power efficiency to develop their own circuits, but they did not casually forget to think about enable. Instead, they actively teach away from it, starting with Rincon-Mora's abstract:

An improved low-dropout (“LDO”) voltage regulator incorporates a transient response boost circuit which is added to the slew-rate limited node at the control terminal of the LDO voltage regulator output transistor and provides improved transient response performance to the application of various load current step stimuli **while requiring no standby or quiescent current during zero output current load conditions.** [EX1013, Abstract (emphasis added)]

More particularly, the present invention relates to a current efficient LDO voltage regulator incorporating a transient response boost circuit which may be added to selectively apply current to a slew-rate limited node and **yet requires no standby current during zero output current load conditions of the LDO voltage regulator.** [EX1013, 1:12-18 (emphasis added)]

In a preferred embodiment disclosed herein, a transient boost circuit is added to the slew-rate limited node and **requires no standby current during zero output current load conditions.** [EX1013, 2:4-7 (emphasis added)]

129. Since Rincon-Mora in his own words has delivered a voltage regulator that has no standby or quiescent current, there is simply no reason for a POSITA to deal with the complexity of deciding when to enable and when to disable the regulator. When the load is not active the regulator will automatically draw no current yet be ready to immediately deal with subsequent increases in load current.

Clearly no disable is needed, so why include one? The only answer is hindsight. No POSITA would add complexity and effort to deal with a non-problem.

130. Moreover, even if a POSITA were to try and solve a problem the reference itself said does not exist, Petitioner fails to consider the trade-offs involved in doing so. For example, according to Ivanov, the trickle charge circuit draws up to 5 μ A, not including the 1-2 μ A of current that is trickled onto capacitor C0. [EX1005, 5:39-41, 5:59-65] 7 μ A is a lot of current to add to save 23 μ A of quiescent current, especially when it will also require the addition of a new analog circuit that can detrimentally impact reference generation and logic to determine when the regulator should be turned on and off. It would be simpler to just leave the regulator enabled and letting the load decide whether it wants to draw current or not, avoiding potential bugs in both the enable of the reference generation and the enable/disable decision. Contrast this with the Micrel MIC59300 regulator that Dr. Chen provided as an example of a commercial LDO: the MIC59300 has a quiescent current of 7.5 mA (more than 300x Rincon-Mora) and clearly benefits from the addition of a “shutdown” circuit. [EX1011, 4 (V_{BIAS} supply current)] But this shutdown circuit comes with the penalty of a 300 μ s turn-on time, making it potentially unusable in many systems. [EX1011, 5 (Turn-on Time)]

131. Turning to Al-Shyoukh, a similar analysis leads to the same result. A POSITA reading the Rincon-Mora paper (discussed in Al-Shyoukh) and the Rincon-

Mora patent together would understand Rincon-Mora to be equating 23 μ A of quiescent current to be sufficiently low as to be negligible. In this regard, I note that even the Petitioner and Dr. Chen recognize as much, stating that “if [Rincon-Mora’s] transistor 45 is sufficiently small, its quiescent current in a no-load state is negligible and thus power-efficient.” [Pet., 56; EX1002, ¶136 (same)]

132. When reviewing Rincon-Mora’s results, Al-Shyoukh points only to the use of an emitter follower driving the output PMOS device and the low output current limit of 50 mA:

In [Rincon-Mora], an emitter-follower has been adopted as a voltage buffer to drive the pMOS pass device. The low output resistance of the emitter-follower allows the pole at the gate of the pass device to be pushed beyond the unity-gain frequency of the LDO regulation loop. The reported LDO dissipates low quiescent current, while sourcing the maximum load current of 50 mA. [EX1004, 1]

133. Notably, Al-Shyoukh does not point to inadequate power savings in Rincon-Mora. The changes made by Al-Shyoukh addressed these same two issues, eliminating the emitter follower and quadrupling the maximum output current, while offering only incremental gains in quiescent current himself: 20 μ A compared to the 23 μ A that he references in the Rincon-Mora paper.

134. Al-Shyoukh’s Table II Performance Comparison with Previously Reported LDOs is shown below, to which I have added an addition column/product

on the right which is the Micrel MIC59300 regulator submitted by Petitioner. This addition is highlighted in **green** and quiescent current in **yellow**. The Micrel MIC59300 is competitive using Al-Shyoukh's figure of merit (possibly even better considering the MIC59300 is a high yielding product and not a cherry picked laboratory curiosity), but has a high I_q even allowing for its 15x higher $I_{L,max}$ than Al-Shyoukh. Al-Shyoukh's quiescent current of 20 μA (even lower than Rincon-Mora's 23 μA) is much closer to the Micrel disable current of "microamperes" than it is to 7.5 mA. Where is the motivation to add an enable capability to Al-Shyoukh when Al-Shyoukh automatically delivers such a low quiescent current whenever the load is inactive and is constantly ready to deliver a larger current when the load demands it? Adding an enable/disable capability would not only add circuit complexity and area it would also require the system designer to answer complex questions about when it is possible to survive a long startup delay to shut down the regulator. On the other hand, there are multiple other parameters ($I_{L,max}$, ΔV_{out} , and T_r) where there is clearly room to improve on Al-Shyoukh's results.

	1998	2000	2003	2004	2005	2007 Al- Shyoukh	2009
	[1]	[3]	[4]	[5]	[17]		MIC59300
Technology (μm)	2	1	0.6	0.5	0.09	0.35	N.A.
V_{do} (V)	0.3	N.A.	0.2	N.A.	0.3	0.2	0.205
$I_{\text{L,max}}$ (mA)	50	200	100	160	100	200	3000
I_{q} (mA)	0.023	0.03	0.038	0.025	6	0.02	7.5
Current Efficiency at $I_{\text{L,max}}$ (%)	99.5	N.A.	N.A.	N.A.	94.3	99.8	95.2
ΔV_{out} (mV)	19	220	130	200	90	54	60
T_{r} (μs)	1.8	1.1	2	2.75	0.00054	0.27	0.02
C_{L} (μF)	4.7	1	10	2.2	0.00060	1	1
ESR Zero Required	No	Yes	Yes	No	No	No	No
FOM (ns)	8.2	0.165	4.9	0.43	0.032	0.027	0.05

Figure 31. Al-Shyoukh, Table II (highlighting and MIC59300 added)
[EX1004]

135. Comparing Al-Shyoukh's results with the commercial LDO that Dr. Chen referenced, the Micrel MIC59300 shows that Al-Shyoukh has delivered a regulator with a quiescent current of 20 μA [EX1004, Table II, I_{q} is 0.02 mA]. In comparison the MIC59300 draws 7.5 mA when $I_{\text{L}} = 100$ mA (the closest the Micrel datasheet comes to specifying a quiescent current). [EX1011, 4 (V_{BIAS} supply current)] The Micrel 59300 also offers a shutdown (enable/disable) mode:

Enable

An active high enable input (EN) allows on-off control of the regulator. Current drain reduces to “zero” when the device is shutdown, **with only microamperes of leakage current**. The EN input has CMOS compatible thresholds for simple logic interfacing. EN may be directly tied to V_{BIAS} and pulled up to the maximum supply voltage. [EX1011, 11 (emphasis added)]

This comes at the cost of a 300 μs turn-on time. [EX1011, 5] Compare this to the Load Transient response shown in Figure 32. Here we see that the current ramps approximately 2.75 A (90% of full load current) in approximately 3 μs , 100 times faster than the “turn-on time.” Clearly there is a significant time penalty involved with disabling the regulator.

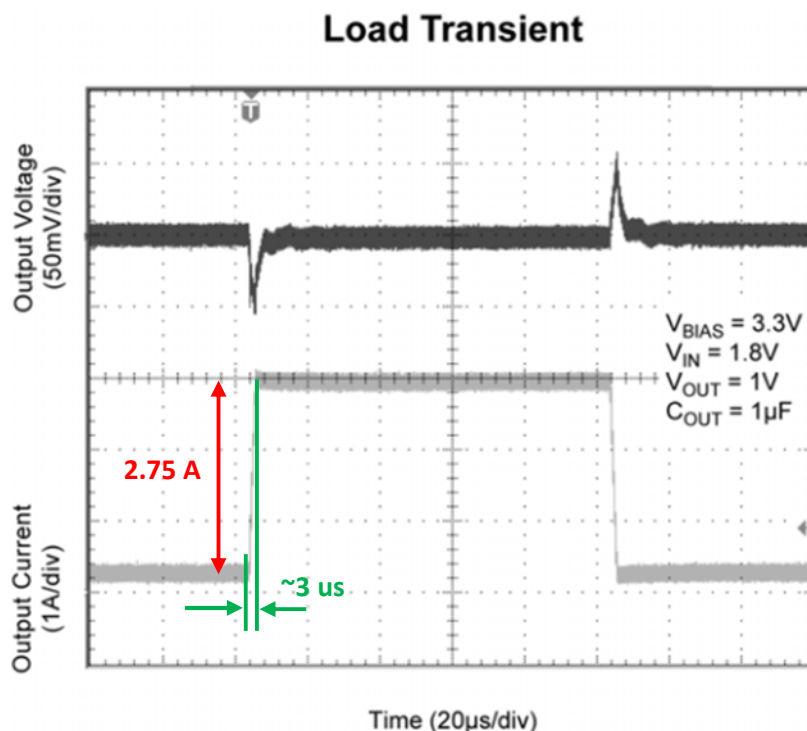


Figure 32. Load Transient (annotation added) [EX1011, 8]

136. Comparing Rincon-Mora, Al-Shyoukh, and an additional 5 commercial voltage regulators using Al-Shyoukh’s metrics plus the shutdown/disable current yields the table shown below (Figure 33). Al-Shyoukh and Rincon-Mora deliver the lowest quiescent current by a factor of 7 to more than 400. Their quiescent current is comparable to or lower than the shutdown current of two of the three alternative regulators that support shutdown (the Micrel MIC59300 only says “Current drain

reduces to ‘zero’ when the device is in shutdown, with only microamperes of leakage” [EX1011, 11]). Note that even when disabled, regulators still have leakage and still dissipate power. There is no reason Rincon-Mora or Al-Shyoukh would be any different. If Ivanov’s enable/disable circuitry were added to these regulators, then their quiescent current would increase by Ivanov’s 5-7 μA and their shutdown/disable current might not reduce significantly from the present 20 to 23 μA of quiescent current. Neither the Petitioner nor Dr. Chen has shown why POSITA would increase the quiescent current by 30 to 35% to obtain a shutdown current that is at best a minor improvement (and possibly a small step backwards) over their existing quiescent current.

	1998 EX1013	2009 EX1004	2009 EX1011	2013 EX2011	2012 EX2012	2012 EX2016	2012 EX2019	2003 EX2020
Technology (μm)	2	0.35	N.A.	N.A.	N.A.	N.A.	N.A.	N.A.
V_{do} (V)	0.3	0.2	0.205	<1	2	1.2	0.39	<0.5
$I_{\text{L,max}}$ (mA)	50	200	3000	1000	500	1500	300	3000
I_{q} (mA)	0.023	0.02	7.5	5	6	10	0.16	10
I_{SHUTDOWN} (mA)	N.A.	N.A.	<0.01	N.A.	N.A.	N.A.	0.06	0.02
Current Efficiency at $I_{\text{L,max}}$ (%)	99.5	99.8	95.2	95.2	98.8	98.8	99.9	99.7
ΔV_{out} (mV)	19	54	60	40	500	130	100	N.A.
T_{r} (μs)	1.8	0.27	0.02	0.04	0.1	1.63	0.33	N.A.
C_{L} (μF)	4.7	1	1	1	0.1	10	1	47
ESR Zero Required	No	No	No	Yes	No	Yes	Yes	No
FOM (ns)	8.2	0.027	0.05	0.2	1.2	20.3	0.18	N.A.

Figure 33. Comparison of Rincon-Mora [EX1013], Al-Shyoukh [EX1004], MIC59300 [EX1011], LM2990 [EX2011], L78Mxx [EX2012], LM1117 [EX2016], TC1300 [EX2019], and KA78Rxx [EX2020]

137. Aside from quiescent current, the $I_{\text{L,max}}$ offered by Rincon-Mora and Al-Shyoukh consistently falls short of the alternatives, some of which offer better T_{r} ,

and/or C_L in spite of have a worse FOM than Al-Shyoukh. And both Rincon-Mora and the LM2990 [EX2011] offer better ΔV_{out} than Al-Shyoukh. With all these deficiencies, why would POSITA focus on improving what is already the best quiescent current? Al-Shyoukh has already delivered a regulator suitable for lithium-ion battery powered systems without using an enable/disable capability, so why add Ivanov's trickle charge/disable circuit and increase the quiescent current by 35%? [EX1004, V. Conclusion]

138. Like Rincon-Mora, Al-Shyoukh delivered a quiescent current that was close enough to zero that the system level problems involved with enabling and disabling regulators could be avoided entirely. The Petitioner and Dr. Chen have failed to explain why POSITA would want to open Pandora's Box by raising the quiescent current of the regulator (by adding Ivanov's trickle charge/disable circuit), and increasing system design complexity by requiring a decision about when the regulator can be disabled and when it must be enabled, without addressing whether further regulator power savings are even needed or if the shutdown/disabled current of the regulator plus Ivanov's trickle charge/disable circuit is below the quiescent current of the existing design.

XII. CONCLUSION

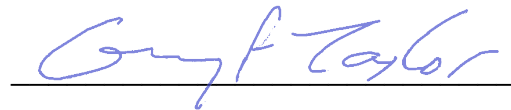
139. I am aware that this declaration will be filed as evidence in an *inter partes* review ("IPR") proceeding before the Patent Trial and Appeal Board. I am

Decl. of Dr. Greg Taylor

aware that making willfully false statements in my declaration are punishable by fine or imprisonment, or both (under 18 U.S.C. §1001), and thus such actions may compromise the validity of the IPR proceeding. All statements herein made by me of my own knowledge are true, and all statements made on information and belief are believed to be true.

140. I declare under penalty of perjury that the foregoing is true and correct.

Executed this 7th day of January, 2025.



Gregory F. Taylor

APPENDIX A

Gregory F. Taylor

2894 NW 127th Avenue
Portland, OR 97229-8386
(503) 880-9254
Greg@GregTaylorConsulting.com

Experience

- 2016- **Greg Taylor Consulting, Inc.**, Portland OR
Principal. Technical consulting on electronic product and integrated circuit development with a variety of clients, as well as patent expert witness work.
- 2016-2020 **zGlue Corporation**, Hillsboro OR
zGlue Fellow. Consulted on new product planning; integrated circuit design, specification, validation, testing, and manufacturing; represented zGlue at opencompute.org's Open Domain Specific Architecture (ODSA) working group.
- 2014-2016 **Intel Corporation**, Platform Engineering Group, Hillsboro OR
Intel Fellow, Hard IP Group Chief Architect. Leading the worldwide circuit architecture teams for I/O, analog, and linear supply regulator design.
- 2008-2015 **Intel Fellow, Analog Review Committee lead.** Led an internal team driving the development of 22, 14, and 10 nm analog/mixed signal circuits across all product lines using Intel process technologies. Drove consistency and sharing of these IPs across most of the business units at Intel.
- 2013 **Intel Corporation**, Intel Labs, Hillsboro OR
Intel Fellow, Director of the Low Power Mixed Signal Lab. Started a new lab to develop analog/mixed signal circuits and design methods that will enable lower power computing and communication platforms.
- 2011-2013 **Intel Fellow, Director of the SoC Design Lab.** Led a multinational team to develop prototype Systems on Chip, including work to improve time to market and energy efficiency through improvements to chip design.
- 2008-2011 **Intel Fellow, Director of the Circuit Research Lab.** Led a team developing circuits and microarchitectures that will lead to lower power and higher performance computing platforms.
- 2004-2008 **Intel Corporation**, Logic Technology Development, Hillsboro OR
Intel Fellow, Director of Mixed Signal Circuit Technology. Led a cross organizational team coordinating the 45 nm and 32 nm collateral delivery between process technology development and multiple design projects. Technical lead for the team that developed I/O, clock generation, temperature sensing, and other analog circuits for use across all Intel microprocessors developed on 65 nm, 45 nm, and 32 nm manufacturing technologies, including the first commercial high-k metal gate based product. Started analog circuit development for what became the first commercial FinFET manufacturing process.
- 2002-2004 **Intel Fellow, Director of Mixed Signal Circuit Technology.** Managed the team responsible for the design of clock generation, clock distribution, I/O circuitry, package, power distribution and other mixed signal circuits for a pair of 90 and 65 nm Pentium® 4 processors, including the first commercial strained silicon based product.
- 1993-2002 **Principal Engineer/Component Design Manager.** Managed the team responsible for the design of clock generation, clock distribution, I/O circuitry, package, power distribution and other mixed signal circuits for Pentium, Pentium II, and Pentium III microprocessors in 0.35 through 0.13 μm technologies.
- 1991-1993 **Staff Design Engineer.** Designed a CMOS/ECL cache for the Pentium Microprocessor, Intel's first BiCMOS product, in 0.8 μm and 0.6 μm

technologies. Developed an Electrical Rules Checker to ensure the correctness of signaling between different frequency clock domains.

Bipolar Integrated Technology, Beaverton OR

- 1988-1991 **Principal Design Engineer.** Participated in all phases of the design of a second generation floating point chip. Made customer visits to determine product requirements; developed the architecture, test and validation plans; and designed the multiplier circuit. Developed an ECL Electrical Rules Checker and formal verification tool and supervised the package design. Consulted in the design, validation, and debug of Sparc® and MIPS® ECL microprocessors.
- 1986-1988 **Circuit Design Engineer.** Designed Emitter Coupled Logic floating point integrated circuits. Generated test suite and validated correctness of overall design. Developed a switch level simulator to verify the logical correctness of ECL gates. Completed debug and sustaining engineering.

Education

- 1983-1985 D.Eng. Computer and Systems Engineering, Rensselaer Polytechnic Institute (RPI), Troy, NY. Thesis topic: An Architecture for a Wafer Scale Integration Two Dimensional Fast Fourier Transform Processor.
- 1981-1983 MSEE Computer and Systems Engineering, RPI, Troy NY. Thesis topic: An ECL Floating Point Processor.
- 1977-1981 BSEE Computer and Systems Engineering, RPI, Troy, NY.

Other

- IEEE Fellow, 2009 to present.
- Fannie and John Hertz Foundation Fellowship, recipient, 1981 to 1985.
- VLSI Circuit Symposium Technical Committee, member, 1999 to 2006.
- Published more than 60 peer reviewed papers, 68 issued US patents.

Publications

"A 1–2 GHz Computational-Locking ADPLL With Sub-20-Cycle Locktime Across PVT Variation", Fahim ur Rahman, Greg Taylor, Visvesh Sathe, IEEE Journal of Solid-State Circuits, September 2019.

"Designing Software Configurable Chips and SIPs using Chiplets and zGlue", Jawad Nasrullah, Zhiquan Luo, Greg Taylor, International Symposium on Microelectronics, September 2019.

"High Capacity on-Package Physical Link Considerations", Greg Taylor, Ramin Farjadrad, Bapiraju Vinnakota, Hot Interconnects Conference, August 2019.

"Smart Silicon Substrate for Quick Time to Market Chip-Stacks and Systems-in-Package", Omar Alnaggar, Rakesh Kumar, Jawad Nasrullah, Greg Taylor, IEEE System on Chip Conference, September 2018.

"Computational Locking: Accelerating Lock-Times in All-Digital PLLs", Fahim ur Rahman, Greg Taylor, Visvesh Sathe, VLSI Circuits Symposium, June 2017.

"Product Scaling in the System on Chip Era", Greg Taylor, International Electron Devices Meeting, December 2013.

"How to Reduce Power in 3D IC Designs- A Case Study with OpenSPARC T2 Core", Moongon Jung, Taigon Song, Yang Wan, Young-Joon Lee, Debabrata Mohapatra, Hong Wang, Greg Taylor, Devang Jariwala, Vijay Pitchumani, Patrick Morrow, Clair Webb, Paul Fischer, and Sung Kyu Lim, IEEE Custom Integrated Circuits Conference, September 2013.

"A Novel Digital Loop Filter Architecture for Bang-Bang ADPLL", Moataz Abdelfattah, Maged Ghoneima, Yehea I Ismail, Amr Lotfy, Mohamed Abdel-moneum, Nasser A. Kurd, Greg Taylor, International System on Chip Conference, September 2012.

"Modeling the Response of Bang-Bang Digital PLLs to Phase Error Perturbations", Moataz Abdelfattah, Maged Ghoneima, Yehea I Ismail, Amr Lotfy, Mohamed Abdelsalem, Mohamed Abdel-moneum, Nasser A. Kurd, Greg Taylor, IEEE Custom Integrated Circuits Conference, September 2012.

"The Next Decade of Computing", Greg Taylor, Theory and Applications of Computational Chemistry, September 2012.

"Digital Randomness", Greg Taylor and George Cox, IEEE Spectrum, September 2011.

"Analog Mixed Signal Design: The Technology Scaling Rate Limiter", Greg Taylor, Frontiers in Analog CAD, July 2011.

"SiP, SOC, and TSV: Issues in Getting from Technologies to Systems", Greg Taylor, GIT 3D System Workshop, June 2011.

"HVM Performance Validation and DFM Techniques used in a 32nm CMOS Thermal Sensor System", D. Duarte, P. Zepeda, S. Hsu, A. Maheshwari and G. Taylor, IEEE Sensors, November 2010.

"A Wide Dynamic Range Self-Biased Fully Differential Operational Amplifier for Micro Mechanical Sensors and Actuators Circuitry", Mohamed Abdel-moneum, David Duarte, Greg Taylor, IEEE Sensors, November 2010.

"HVM Performance Validation and DFM Techniques used in a 32nm CMOS Thermal Sensor System", D. Duarte, P. Zepeda, S. Hsu, A. Maheshwari and G. Taylor, IEEE Custom Integrated Circuits Conference, September 2010.

"2.4GHz 7mW All-Digital PVT-Variation Tolerant True Random Number Generator in 45nm CMOS", S. Srinivasan, S. Mathew, R. Ramanarayanan, F. Sheikh, M. Anders, H. Kaul, V. Erraguntla, R. Krishnamurthy, G. Taylor, VLSI Circuit Symposium, June 2010.

"A 1.05 V 1.6 mW, 0.45 °C 3 σ Resolution SD Based Temperature Sensor With Parasitic Resistance Compensation in 32 nm Digital CMOS Process", Hasnain Lakdawala, Y. William

Li, Arijit Raychowdhury, Greg Taylor, and Krishnamurthy Soumyanath, IEEE Journal of Solid State Circuits, December 2009, pp. 3621-3630.

"A 1.05 V 1.6 mW, 0.45 °C 3 σ Resolution SD Based Temperature Sensor With Parasitic Resistance Compensation in 32 nm Digital CMOS Process", Hasnain Lakdawala, Y. William Li, Arijit Raychowdhury, Greg Taylor, and Krishnamurthy Soumyanath, International Solid State Circuits Conference, February 2009.

"Managing Process Variation in Intel's 45nm CMOS Technology", Kelin Kuhn, Chris Kenyon, Avner Kornfeld, Mark Liu, Atul Maheshwari, Wei-Kai Shih, Sam Sivakumar, Greg Taylor, Peter VanDerVoorn, Keith Zawadski, Intel Technology Journal, June 2008, pp. 93-110.

"A Band-Limited Active Damping Circuit With 13 dB Power Supply Resonance Reduction", Jianping Xu, Zuoguo Wu, Peter Hazucha, Paolo Aseron, Mingwei Huang, Fabrice Paillet, Gerhard Schrom, James Tschanz, Vivek De, Tanay Karnik, Greg Taylor, IEEE Journal of Solid State Circuits, January 2008, pp. 61-68.

"On-Die Supply-Resonance Suppression Using Band-Limited Active Damping", Jianping Xu, Peter Hazucha, Mingwei Huang, Paolo Aseron, Fabrice Paillet, Gerhard Schrom, James Tschanz, Cangsang Zhao, Vivek De, Tanay Karnik, Greg Taylor, International Solid State Circuits Conference, February 2007.

"Designing for Low Power", Tawfik Rahal-Arabi, Ali Muhtaroglu, and Greg Taylor, Electrical Performance of Electronic Packaging, October 2006.

"The Impact of Leakage to the Power Supply Impedance of a Microprocessor", Ananda Sarangi, Greg Taylor, Signal Propagation on Interconnects, May 2006, pp. 43-46.

"Enhancing Microprocessor Immunity to Power Supply Noise with Clock/Data Compensation", Keng L Wong, Tawfik Rahal-Arabi, Matthew Ma, Greg Taylor, IEEE Journal of Solid State Circuit Design, April 2006, pp. 749-758.

"Reducing the Impact of Power Supply Noise on Microprocessor Performance", T. Rahal-Arabi, K.L. Wong, M. Ma, J. Barkatullah, G. Taylor, Electrical Performance of Electronic Packaging, October 2005, pp. 307-310.

"Design and Validation of a Power Supply Noise Reduction Technique", Gang Ji, Tawfik R Arabi, Greg Taylor, IEEE Transactions on Advanced Packaging, August 2005, pp. 445-448.

"Enhancing Microprocessor Immunity to Power Supply Noise with Clock/Data Compensation", Tawfik Rahal-Arabi, Greg Taylor, Javed Barkatullah, Keng L Wong, Matthew Ma, 2005 Symposium on VLSI Circuits, June 2005, pp. 16-19.

"Impact of On-Die Decoupling on the Core and IO Supplies of High Performance Microprocessors", Tawfik Rahal-Arabi, Gang Ji, Greg Taylor, Signal Propagation on Interconnects, May 2005, pp. 31-34.

"I/O Self-Leakage Test", Ali Muhtaroglu, Benoit Provost, Tawfik Rahal-Arabi, Greg Taylor, International Test Conference, October 2004, pp. 903-906.

"Computational Electromagnetics for High-Frequency IC Design", Dan Liao, Changhong Dai, Shihuh-Wuu Lee, Tawfik Rahal-Arabi, Greg Taylor, Antennas and Propagation Society Symposium, Jun 2004, pp. 3317-3320.

"Development and Validation of an Electromagnetic Distributed Power Grid Model for High Frequency Microprocessors", Tawfik Rahal-Arabi, Gang Ji, Matthew Ma, Ali Muhtaroglu, Greg Taylor, 2004 Symposium on VLSI Circuits, June 2004, pp. 110-113.

"Dampening High Frequency Noise in High Performance Microprocessor Packaging", Tawfik Rahal-Arabi, Gang Ji, Greg Taylor, Signal Propagation on Interconnects, May 2005, pp. 53-56.

"On-Die Droop Detector for Analog Sensing of Power Supply Noise", Ali Muhtaroglu, Greg Taylor, Tawfik Rahal-Arabi, IEEE Journal of Solid State Circuit Design, April 2004, pp. 651-660.

"Maintaining Microprocessor Compatibility across Process Generations", Ananda Sarangi, Sean R. Babcock, Jeff R. Jones, Gregory F. Taylor, Electrical Performance of Electronic Packaging, October 2003.

"Design and Validation of a Power Supply Noise Reduction Technique", Gang Ji, Tawfik Arabi, Greg Taylor, Electrical Performance of Electronic Packaging, October 2003, pp. 137-140.

"On-Die Droop Detector for Analog Sensing of Power Supply Noise", Ali Muhtaroglu, Greg Taylor, Tawfik Rahal-Arabi, Kent Callahan, 2003 Symposium on VLSI Circuits, June 2003, pp. 193-196.

"A Design Methodology for The I/O Power Supply of Next Generation Packaging", Gang Ji, Tawfik Arabi, Greg Taylor, Mark Beiley, Electrical Performance of Electronic Packaging, October 2002, pp. 253-256.

"Design and Validation of the Core and IOs Decoupling of the Pentium® III and Pentium® 4 Processors", Tawfik Rahal-Arabi, Greg Taylor, Matthew Ma, Jeff Jones and Clair Webb, Electrical Performance of Electronic Packaging, October 2002, pp. 249-252.

"Power Level Management in an IA32 Microprocessor", Ananda Sarangi, Gregory F. Taylor, Rachael J. Parker, Edward P. Osburn, Patrick J. Ott, Electrical Performance of Electronic Packaging, October 2002, pp. 235-238.

"Design & Validation of the Pentium® III and Pentium® 4 Processors Power Delivery", Tawfik Rahal-Arabi, Greg Taylor, Matthew Ma, and Clair Webb, 2002 Symposium on VLSI Circuits, June 2002, pp. 220-223.

"An Approach to Measuring the Power Supply Impedance of Microprocessors", Greg Taylor, Craig Deutschle, Tawfik Arabi, Brian Owens, Electrical Performance of Electronic Packaging, October 2001, pp. 211-214.

"Design and Performance Evaluation of Pentium® III Microprocessor Packaging", Ananda Sarangi, Gang Ji, Tawfik Arabi, Gregory F. Taylor, Electrical Performance of Electronic Packaging, October 2001, pp. 291-294.

"A JTAG Based AC Leakage Self Test", Tawfik Rahal-Arabi, Greg Taylor, 2001 Symposium on VLSI Circuits, June 2001, pp. 205-206.

"On-die Clock Jitter Detector for High Speed Microprocessors", Ravi Kuppaswamy, Kent Callahan, Keng Wong, Dan Ratchen, Greg Taylor, 2001 Symposium on VLSI Circuits, June 2001, pp. 187-190.

"High Performance Package Designs for a 1 GHz Microprocessor", Altaf Hasan, Ananda Sarangi, Christopher S Baldwin, Robert L Sankman, Gregory F Taylor, Electronic Components and Technology Conference, August 2000, pp. 1178-1184.

"Reliability and Performance Tradeoffs in the Design of On-Chip Power Delivery and Interconnects", Greg Taylor, Tawfik Arabi, Hans Greub, Richard Muyschondt, Alicia Manthe, and Payman Aminzadeh, Electrical Performance of Electronic Packaging, October 1999, pp. 49-52.

"Modeling, Simulation, and Design Methodology of the Interconnect and Packaging of an Ultra-High Speed Source Synchronous Bus", Tawfik Arabi, Jeff Jones, Greg Taylor, and Dave Riendeau, Electrical Performance of Electronic Packaging, October 1998, pp. 8-11.

"A 2MB, 3.6GB/s Back-side Bus Cache for an IA32 450 MHz Microprocessor", Greg Taylor, Tawfik Arabi, Ken Hose, Jeff Jones, Songmin Kim, Ravi Kuppaswamy, Randy Mooney, Jack Price, Ananda Sarangi, 2001 Symposium on VLSI Circuits, June 1998, pp. 184-185.

"Power-On Contention Elimination", Greg Taylor, Keng Wong, 1996 Symposium on VLSI Circuits, June 1996, pp. 22-23.

"Microprocessor Clock Distribution", Greg Taylor, George Geannopoulos, Electrical Performance of Electronic Packaging, October 1996, pp. 29.

"High Fan-in Circuit Design", Lawrence T. Clark and Gregory F. Taylor, IEEE Journal of Solid State Circuit Design, January 1996, pp. 91-96.

"High Fan-in Circuit Design", Lawrence T. Clark and Gregory F. Taylor, Bipolar Circuits and Technology Meeting, October 1994, pp. 27-32.

"Building the world's fastest floating point processor", G. Sanguinetti, G. Taylor, and D. Clinkenbeard, ASIC Technology & News, January 1991, pp. 12-13.

"An Approach to 150K Gate Low Power ECL Cell Based Integrated Circuits", G. Taylor, G. Sanguinetti, and R Lane, International Conference on Computer Design, September 1990, pp. 263-268.

"A 100 MHz Floating Point/Integer Processor", Greg Taylor, Hot Chips, August 1990.

"A 100 MHz Floating Point/Integer Processor", Greg Taylor, Alex Rekow, Jory Radke, Greg Thompson, Custom Integrated Circuits Conference, May 1990, pp. 24.5.1-4.

"An Architecture for a Video Rate Two-Dimensional Fast Fourier Transform Processor", G. F. Taylor, R. H. Steinvorth, and J. F. McDonald, IEEE Transactions on Computers, September 1988.

"A Sub 10 ns Bipolar 64 Bit Integer/Floating Point Processor Implemented on Two Circuits", Bob Elkind, Jay Lessert, Jim Peterson, and Greg Taylor, Bipolar Circuits and Technology Meeting, September 1987, pp. 101-104.

"ECL gains ground in battle against CMOS", Bob Leibowitz and Greg Taylor, Computer Design, April 1987, pp. 91-95.

"Wafer Scale Integration Using Discretionary Microtransmission Line Interconnections", B. J. Donlan, G. F. Taylor, R. H. Steinvorth, A. S. Bergendahl, J. F. McDonald, chapter 2.3 of Wafer Scale Integration, edited by Chris Jesshope and Will Moore, Adam Hilger, Boston, © 1996, pp. 31-45.

"Thick Film Stripline Micro Transmission Line Interconnections for Wafer Scale Integration", A. S. Bergendahl, J. F. McDonald, R. H. Steinvorth, G. F. Taylor, VLSI Science and Technology/1985, pp. 175-184.

"Wafer Scale Integration of a Video Rate Fuzzy Golay Processor", R. H. Steinvorth, G. F. Taylor, J. F. McDonald, A. S. Bergendahl, International Conference on Computer Design, October 1985, pp. 672-677.

"Fabrication and Performance Considerations for Gallium Arsenide Wafer Scale Integration", J. F. McDonald, R. H. Steinvorth, A. S. Bergendahl, G. F. Taylor, International Conference on Computer Design, October 1985, pp. 400-405.

"An Architecture for a Video Rate Fuzzy Golay Processor", R. H. Steinvorth, G. F. Taylor, J. F. McDonald, T. Hunter, International Conference on Parallel Processing, 1985.

"A Thick Film Lift-Off Technique for High Frequency Interconnection in Wafer Scale Integration", A. S. Bergendahl, B. J. Donlan, J. F. McDonald, R. H. Steinvorth, G. F. Taylor, VLSI Multilevel Interconnect Conference, 1985.

"Thick Film Stripline Micro Transmission Line Interconnections for Wafer Scale Integration", A. S. Bergendahl, J. F. McDonald, R. H. Steinvorth, G. F. Taylor, Electrochemical Society Spring Meeting, May 1985, pp. 311-312.

"The Wafer Transmission Module - Wafer Scale Integration Packaging", G. F. Taylor, Lt. B. J. Donlan, J. F. McDonald, A. S. Bergendahl, R. H. Steinvorth, Custom Integrated Circuits Conference, May 1985, pp. 55-58.

"Computer-Aided Design and Fabrication for Wafer Scale Integration", Lt. B. J. Donlan, J. F. McDonald, G. F. Taylor, R. H. Steinvorth, A. S. Bergendahl, VLSI Design magazine, April 1985.

"An Architecture for a Wafer Scale Integration Video Rate Two Dimensional Fast Fourier Transform Processor", G. F. Taylor, R. H. Steinvorth, J. F. McDonald, International Conference on Computer Design, October 1984, pp. 623-628.

US Patents

Number	Issue Date	Title	Inventors
4,972,362	11/20/1990	Method and apparatus for implementing binary multiplication using Booth type multiplication	Bob Elkind, Jay D. Lessert, James R. Peterson, Gregory F. Taylor
4,982,352	1/1/1991	Methods and apparatus for determining the absolute value of the difference between binary operands	Gregory F. Taylor
5,153,848	10/6/1992	Floating point processor with internal free-running clock	Gregory F. Taylor
5,306,964	4/26/1994	Reference generator circuit for BiCMOS ECL gate employing PMOS load devices	Gregory F. Taylor, Lawrence T. Clark
5,345,120	9/6/1994	Swing limiting circuit for BiCMOS sense amplifiers	Gregory F. Taylor, Jeffrey E. Smith
5,399,918	3/21/1995	Large fan-in, dynamic, BiCMOS logic gate	Gregory F. Taylor
5,539,337	7/23/1996	Clock noise filter for integrated circuits	Golnaz Kaveh, Gregory F. Taylor, Jeffrey E. Smith
5,801,561	9/1/1998	Power-on initializing circuit	Keng L. Wong, Gregory F. Taylor, Roshan J. Fernando, Jeffrey E. Smith
6,075,285	6/13/2000	Semiconductor package substrate with power die	Gregory F. Taylor, George L. Geannopoulos, Larry E. Mosley
6,075,832	6/13/2000	Method and apparatus for deskewing clock signals	George Geannopoulos, Keng L. Wong, Greg F. Taylor, Xia Dai
6,085,345	7/4/2000	Timing control for input/output testability	Gregory F. Taylor
6,124,755	9/26/2000	Method and apparatus for biasing a charge pump	Douglas R. Parker, Gregory F. Taylor
6,157,206	12/5/2000	On-chip termination	Gregory F. Taylor, Jack A. Price, Chee How Lim
6,208,169	3/27/2001	Internal clock jitter detector	Keng L. Wong, Gregory F. Taylor, Ravishankar Kuppuswamy, Douglas R. Parker, Hung-Piao Ma, Kent R. Callahan, Xia Dai
6,236,695	5/22/2001	Output buffer with timing feedback	Gregory F. Taylor
6,298,105	10/2/2001	Method and apparatus for a low skew, low standby power clock network	Xia Dai, George Geannopoulos, John Orton, Keng Wong, Greg F. Taylor
6,326,802	12/4/2001	On-die adaptive arrangements for continuous process, voltage and temperature compensation	Paul F. Newman, Jeff R Jones, Greg Taylor, Chee How Lim, Gerald Pasdast

Number	Issue Date	Title	Inventors
6,396,309	5/28/2002	Clocked sense amplifier flip flop with keepers to prevent floating nodes	Cangsang Zhao, Chi-Yeu Chao, Gregory F. Taylor
6,410,990	6/25/2002	Integrated circuit device having C4 and wire bond connections	Gregory F. Taylor, George L. Geannopoulos
6,452,502	9/17/2002	Method and apparatus for early detection of reliability degradation of electronic devices	Terrance J. Dishongh, David H. Pullen, Gregory F. Taylor
6,453,421	9/17/2002	Processor System with Power Supply Selection Mechanism	Gregory F. Taylor
6,535,047	3/18/2003	Apparatus and Method to Use a Single Reference Component in a Master-Slave Configuration for Multiple Circuit Compensation	Usman A. Mughal, Razi Uddin, Chee How Lim, Songmin Kim, Gregory F. Taylor
6,552,570	4/22/2003	Input circuit with non-delayed time blanking	Gregory F. Taylor, Chi-Yeu Chao
6,573,764	6/3/2003	Method and apparatus for voltage-mode differential simultaneous bi-directional signaling	Gregory F. Taylor
6,584,591	6/24/2003	Timing control for input/output testability	Gregory F. Taylor
6,628,157	9/30/2003	Variable Delay Element for Use in Delay Tuning of Integrated Circuits	Ravishankar Kuppaswamy, Gregory Taylor
6,671,847	12/30/2003	I/O Device Testing Method and Apparatus	Chi-Yeu Chao, Tawfik R. Arabi, Thomas D. Barrett, Gregory F. Taylor
6,691,241	2/10/2004	Delay tuning to improve timing in multi-load systems	Gregory F. Taylor
6,717,455	4/6/2004	Apparatus and Method to Use a Single Reference Component in a Master-Slave Configuration for Multiple Circuit Compensation	Usman A. Mughal, Razi Uddin, Chee How Lim, Songmin Kim, Gregory F. Taylor
6,727,597	4/27/2004	Integrated circuit device having C4 and wire bond connections	Gregory F. Taylor, George L. Geannopoulos
6,747,470	6/8/2004	Method and apparatus for on die voltage fluctuation detection	Ali Muhtaroglu, Kent Callahan, Tawfik Arabi, Gregory F. Taylor
6,748,549	6/8/2004	Clocking an I/O buffer, having a selectable phase difference from the system clock, to and from a remote I/O buffer clocked in phase with the system clock	Chi-Yeu Chao, Chee How Lim, Keng L. Wong, Songmin Kim, Gregory F. Taylor
6,771,134	8/3/2004	Frequency control for clock generating circuit	Keng L. Wong, Hong-Piao Ma, Greg F. Taylor, Chee How Lim, Edward A. Burton

Number	Issue Date	Title	Inventors
6,777,970	8/17/2004	AC testing of leakage current in integrated circuits using RC time constant	Tawfik R. Arabi, Gregory F. Taylor, Srirama Pedarla, Patrick Elwer, Dan Murray
6,778,033	8/17/2004	Voltage control for clock generating circuit	Keng L. Wong, Hong-Piao Ma, Greg F. Taylor
6,781,428	8/24/2004	Input circuit with switched reference signals	Chi-Yeu Chao, Gregory F. Taylor
6,792,489	9/14/2004	Multistage configuration and power setting	Edward P. Osburn, Gregory F. Taylor, Ananda Sarangi
6,809,606	10/26/2004	Voltage ID based frequency control for clock generating circuit	Keng L. Wong, Hong-Piao Ma, Greg F. Taylor, Chee How Lim, Robert Greiner, Edward A. Burton, Douglas R. Huard
6,874,083	3/29/2005	Method and apparatus to ensure proper voltage and frequency configuration signals are defined before applying power to processor	Ananda Sarangi, Rachael Jade Parker, Edward P. Osburn, Gregory F. Taylor
6,885,231	4/26/2005	Variable delay element for use in delay tuning of integrated circuits	Ravishankar Kuppaswamy, Gregory Taylor
6,924,710	8/2/2005	Voltage ID Based Frequency Control for Clock Generating Circuit	Keng L. Wong, Hong-Piao Ma, Greg F. Taylor, Chee How Lim, Robert Greiner, Edward A. Burton, Douglas R. Huard
6,967,496	11/22/2005	AC testing of leakage current in integrated circuits using RC time constant	Tawfik R. Arabi, Gregory F. Taylor, Srirama Pedarla, Patrick Elwer, Dan Murray
6,985,041	1/10/2006	Clock generating circuit and method	Keng L. Wong, Niraj Bindal, Hong-Piao Ma, George Geannopoulos, Greg F. Taylor, Edward A. Burton
7,038,512	5/2/2006	Closed-loop independent DLL-controlled rise/fall time control circuit	Timothy M Wilson, Michael C. Rifani, Songmin Kim, Greg Taylor
7,038,513	5/2/2006	Closed-loop independent DLL-controlled rise/fall time control circuit	Timothy M Wilson, Michael C. Rifani, Songmin Kim, Greg Taylor, Navindra Navaratnam

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7,049,865	5/23/2006	Power-on detect circuit for use with multiple voltage domains	Rachael J Parker, Mark L Neidengard, Patrick J Ott, Gregory F Taylor
7,109,737	9/19/2006	Arrangements having IC voltage and thermal resistance designated on a per IC basis	Tawfik Arabi, Hung-Piao Ma, Gregory M Iovino, Shai Rotem, Avner Kornfeld, Gregory F Taylor
7,112,979	9/26/2006	Arrangements having IC voltage and thermal resistance designated on a per IC basis	Tawfik Arabi, Hung-Piao Ma, Gregory M Iovino, Shai Rotem, Avner Kornfeld, Gregory F Taylor
7,143,381	11/28/2006	Resonance reduction arrangements	Cangsang Zhao, Greg Taylor
7,157,924	1/2/2007	Method and apparatus for on die voltage fluctuation detection	Ali Muhtaroglu, Kent Callahan, Tawfik Arabi, Gregory F. Taylor
7,199,624	4/3/2007	Phase locked loop system capable of deskewing	Keng L Wong, Gregory F Taylor, Chee How Lim
7,233,162	6/19/2007	Arrangements having IC voltage and thermal resistance designated on a per IC basis	Tawfik Arabi, Hung-Piao Ma, Gregory M. Iovino, Shai Rotem, Avner Kornfeld, Gregory F. Taylor
7,242,261	7/10/2007	Voltage control for clock generating circuit	Keng L. Wong, Hong-Piao Ma, Greg F. Taylor
7,282,937	10/16/2007	On-Chip Frequency Degradation Compensation	Ravisangar Muniandy, Gregory F Taylor, Payman Aminzadeh
7,348,790	3/25/2008	AC testing of leakage current in integrated circuits using RC time constant	Tawfik R. Arabi, Gregory F. Taylor, Srirama Pedarla, Patrick Elwer, Dan Murray
7,394,274	7/1/2008	On-chip frequency degradation compensation	Ravisangar Muniandy, Gregory F Taylor, Payman Aminzadeh
7,417,459	8/26/2008	On-die offset reference circuit block	Timothy M Wilson, Songmin Kim, Gregory F Taylor
7,471,102	12/30/2008	Measuring threshold voltage of transistors in a circuit	Atul Maheshwari, Greg Taylor

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7,501,845	3/10/2009	On-chip frequency degradation compensation	Ravisangar Muniandy, Gregory F Taylor, Payman Aminzadeh
7,602,663	10/13/2009	Fuse cell array with redundancy features	Zhanping Chen, Jonathan P Douglas, Praveen Mosalikanti, Kevin Zhang, Gregory F Taylor
7,889,587	2/15/2011	Fuse Programming Schemes for Robust Yield	Jun He, Zhanping Chen, Jeffrey Hicks, Gregory F Taylor
8,096,707	1/17/2012	Thermal Sensor Device	Arajit Raychowdhury, Hasnain Lakdawala, Yee (William) Li, Greg Taylor, Soumyanath Krishnamurthy
8,314,725	11/20/2012	On-die digital-to-analog conversion testing	Paola Zepeda, David E. Duarte, Gregory F. Taylor, Atul Maheshwari
8,589,706	11/19/2013	Data inversion based approaches for reducing memory Power Consumption	Ming Zhang, Chris Wilkerson, Greg Taylor, Randy J. Aksamit, James Tschanz
8,827,550	9/9/2014	Thermal Sensor using a vibrating MEMS resonator of a chip interconnect layer	Mohamed A. Abdelmoneum, Tawfik M. Rahal-Arabi, Gregory F. Taylor, Kevin J. Fischer, Andrew Yeoh
9,702,769	7/11/2017	Self-Calibrated Thermal Sensors of an Integrated Circuit Die	Mohamed A. Abdelmoneum, David Duarte, Gregory F. Taylor