

Patent No. 9,471,074
Petition For *Inter Partes* Review

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APTIV SERVICES US, LLC,
Petitioner,

v.

MICROCHIP TECHNOLOGY, INC.,
Patent Owner.

Patent No. 9,471,074

Case No. IPR2024-00646

SECOND SUPPLEMENTAL DECLARATION OF DR. MICHAEL S. CHEN

I, Dr. Michael S. Chen, make this declaration in connection with the proceeding identified above.

1. I have been retained by counsel for Aptiv Services US, LLC (“Aptiv”) as a technical expert in connection with the proceeding identified above. I submit this second supplemental declaration in support of Aptiv’s Petition for *Inter Partes* Review of United States Patent No. 9,471,074 (the “’074 patent”) and its Reply.

I. Dr. Taylor’s Declaration (EX2021)

2. I have been asked to consider certain of Dr. Taylor’s opinions submitted in support of the Patent Owner’s Response.

A. “a gm enhanced current buffer driver”

3. I disagree with Dr. Taylor’s analysis of an alleged technique that he provides “gm enhancement,” as reflected in the claim term “gm enhanced current buffer driver.” Dr. Taylor states that what he calls “gm enhancement” can increase the gm of the current buffer driver by double or more. That conclusion is incorrect.

4. While Dr. Taylor makes numerous errors in his analysis, I highlight an especially significant error here—his assumption that as the load current of the ’074 patent’s voltage regulator rises, node B (located at the output of the current buffer driver and the gate of the output driver) responds slowly. (EX2021 ¶ 79.) This is important to Dr. Taylor’s analysis because he uses it to assume that the V_{gs} (or gate-

to-source voltage) of the buffer driver transistor 384 changes, leading to a change in current through transistor 384, which produces a change in current through transistor 370, which helps transistor 384 charge or discharge node B. (*Id.*)

5. Dr. Taylor's assumption is incorrect because the '074 patent's circuit is specifically designed to make node B fast. The '074 patent explains that it places a current buffer driver between its operational amplifier and the output driver in order to push the pole at the gate of the output transistor "to a high frequency domain, effectively leav[ing] the only dominant pole at the output (node C) of the OpAmp 202 during full-load conditions." (EX1001, 5:3-6.) The patent also explains that "to achieve this, it is necessary to provide a fairly large gm value of the current buffer driver." (*Id.*, 4:14-15.) It then explains that the large gm value is achieved using "a gm-boost technique." (*Id.*, 4:15-16.) I note that Dr. Taylor acknowledged this in his Declaration in Support of Microchip's Opening Claim Construction Brief in district court, where he stated that "separating the poles inside of the voltage regulator circuit sufficiently to create an approximate one pole system" is "*why* the circuitry of the '074 patent includes a gm-boost circuit." (EX2007 ¶ 65.)

6. The benefit of this pole-splitting is that node B responds quickly to any changes in the much slower node C. This occurs because the pole-splitting ensures that the frequency pole associated with node B is much higher than the frequency

pole associated with node C. The frequency pole associated with a circuit node is the inverse of its RC time constant, *i.e.*, the product of equivalent resistance R and capacitance C at that particular node. A smaller RC time constant means a faster transient response—the node waveform would follow its input signal closer. Here, since node C has a very large RC time constant, the signal on node C would change very slowly because it cannot follow any fast voltage change at the error amplifier input. Meanwhile, the voltage on node B (the output of the current buffer) would follow closely with node C (the input of the current buffer) due to a much smaller RC time constant.

7. Because node B responds quickly and follows node C closely, increases in V_{gs} caused by a drop in the voltage of node C would be negligible. Thus, the “gm enhancement” effect described by Dr. Taylor would also be negligible, because it depends on V_{gs} increasing.

B. “biasing ratio”

8. I disagree with Dr. Taylor’s interpretation of the term “biasing ratio” as “the fraction of the output driver current that biases the source follower.” (EX2021 ¶ 118.) To begin, I note that Dr. Taylor does not provide an explanation as to why he interprets “biasing ratio” in this way. In addition, I believe he is incorrect.

9. Dr. Taylor explains that his definition of “biasing ratio” is ultimately a ratio of transistor sizes, including the size of the output driver transistor. (EX2021 ¶ 118.) Although he does not explain what the “biasing ratio” would be in the circuit shown in Figure 3B of the ’074 patent, he provides a formula for the ratio for Al-Shyoukh’s circuit that makes clear that the ratio involves only transistor sizes. (*Id.*) The reasoning behind this formula appears to be based on tracing how the current in the output transistor would affect the current in the source follower based on pairs of transistors whose currents would have a fixed ratio based on their sizes.

10. The ’074 patent’s claims recite “a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver.” Based on my review of the ’074 patent, I understand the biasing circuit in the embodiment described in the specification and shown in Figures 3, 3A, and 3B to be circuit 208. The patent repeatedly refers to this circuit as “biasing circuits,” “the bias circuit,” or “biasing circuitry.” (EX1001, 3:63, 4:43, Fig. 1.) Bias circuit 208 contributes to the current buffer driver 204 by providing a bias voltage to transistor 396. (*Id.*, Figs. 3, 3B.) It is not connected to the output driver, transistor 380. (*Id.*)

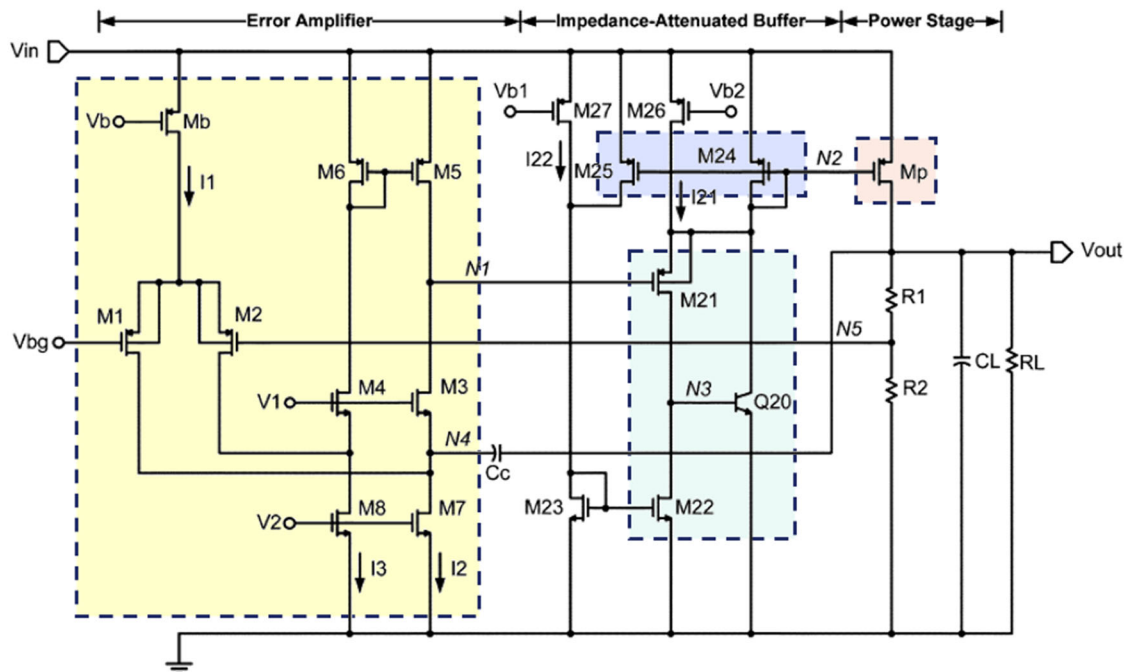
11. Thus, applying Dr. Taylor’s logic to the ’074 patent would result in a mathematical expression for “biasing ratio” that has nothing to do with bias circuit 208 or transistor 396. An expression analogous to Dr. Taylor’s for the Al-Shyoukh

circuit would involve only transistors of the current feedback circuit 210, through which changes in the current of the output driver transistor 380 are made to affect the current of the source follower transistor 384. In other words, Dr. Taylor's view of the term "biasing ratio" is inconsistent with the '074 patent.

II. Ground 1 Under Patent Owner's Construction of "Gm Enhanced"

12. While I disagree with Patent Owner and Dr. Taylor as to the meaning of "gm enhanced," I have been asked to consider whether Al-Shyoukh discloses a "gm enhanced current buffer driver" under Patent Owner's proposed meaning. It is my opinion that it does.

13. Shown in the figure below is an alternative mapping of the '074 patent to Al-Shyoukh's voltage regulator circuit:



(EX1004, Fig. 8 (annotated).) I note that this mapping is the same as the one that I analyzed in my original declaration, except for one small change, which is that the green portion representing the buffer driver has been expanded to include transistor Q₂₀. Al-Shyouxh explains that Q₂₀ is an npn transistor in parallel to the output of the source-follower M₂₁. (*Id.*, 1734.) When connected in this way, Q₂₀ helps improve the slew behavior of the circuit. For example, Al-Shyouxh explains that “[d]uring the transition from no load to full load, the decrease in the voltage at N₁ causes an increase in the transient current through M₂₁, which flows through the base of Q₂₀. The collector current of Q₂₀ then increases to discharge the large gate capacitance of the pass device C_p and the voltage at N₂ decreases with a faster slewing.” (*Id.*, 1734.)

14. In my opinion, Q₂₀ “enhances” the gm of Al-Shyoukh’s current buffer driver in an analogous way to the technique that Dr. Taylor describes for the ’074 patent. (EX2021 ¶ 79.) Dr. Taylor says that when load current increases, the error amplifier responds by “dropping node C,” which is the node at the output of the error amplifier and the gate of the buffer driver transistor. (*Id.*) Similarly, Al-Shyoukh describes a decrease in the voltage at node N₁, which is also at the output of the error amplifier and the gate of the buffer driver transistor, M₂₁. Next, Dr. Taylor says that transistor 370 adjusts its current to “pull[] up less strongly on node B,” which is at the gate of the output driver transistor, to help the latter “pull node B down.” (*Id.*) Similarly, Q₂₀ helps M₂₁ decrease the voltage at node N₂, which is the node at the gate of output driver M_p.

15. Whether Al-Shyoukh’s buffer driver is defined to include Q₂₀, as above, or not, as in the opinions in my original declaration, my opinions as to the remaining claims and claim limitations would not change.

III. Voltage Regulator Datasheets

16. I have reviewed two datasheets for purposes of this declaration.

17. The first is a datasheet dated May 2010 for a Micrel Inc. regulator called MIC3385. I obtained the copy of this datasheet submitted as EX1030 from the URL https://web.archive.org/web/20101225002117/http://www.micrel.com/_PDF/mic3

[385.pdf](#). From reviewing this datasheet, it is my understanding that the MIC3385 device may operate in an LDO mode that has a maximum reported 29 μA quiescent current and a 5 μA shutdown current (which the datasheet explains is the quiescent current when the “Enable” input has a logic low). (EX1030, 2-3.) In addition, based on the “Typical Characteristics – LDO Mode” section of the datasheet, I understand the expected typical turn-on time to be on the order of 60 μs .

18. The second datasheet appears to be dated January 2011 for a part called AP7331 made by Diodes Incorporated. It is my understanding that this datasheet was submitted by Dr. Taylor in related district court claim construction proceedings. Based on my review of this datasheet, I understand it to report a maximum quiescent current at no-load of 75 μA , a maximum shutdown current of 1 μA , and a typical start-up time of 80 μs . (EX1031, 151.)

* * *

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code.

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Dated: April 3, 2025

A handwritten signature in black ink, appearing to read "Jna", positioned above a horizontal line.

Dr. Michael S. Chen