

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

MICROCHIP TECHNOLOGY INC.,

Plaintiff,

v.

APTIV SERVICES US, LLC,

Defendant

C.A. No. 1:23-CV-00778-JDW

JURY TRIAL DEMANDED

**GREG TAYLOR DECLARATION
IN SUPPORT OF MICROCHIP'S OPENING CLAIM CONSTRUCTION BRIEF**

I, Greg Taylor, do hereby declare as follows:

I. Introduction

1. I have been asked to provide my opinions regarding certain claim constructions, and the definiteness of some claims from U.S. Patent Nos. 7,564,665 (“’665 patent”) and 9,471,074 (“’074 patent”). I may refer to the patents collectively as “the Asserted Patents.”

2. I am being compensated at my usual hourly rate for my work in this case. My compensation is not based upon the outcome of the case or the Court’s determinations related to claim construction.

3. In preparing this Declaration and formulating my opinions within, I have considered the ’665 patent and its prosecution history, the ’074 patent and its prosecution history, the parties’ Joint Claim Construction Chart submission in this matter and associated exhibits, along with my personal expertise, knowledge, and experience with the relevant technology, and the materials referenced or mentioned in the body of this declaration. There are images and explanations in this Declaration included for illustrative purposes, some of which I created myself.

Images taken from patents and publications have been cited. At the time of my signing this declaration, all the hyperlinks referenced herein were publicly accessible.

II. Background and Qualifications

4. I have summarized in this section some of my educational background, career history, publications, and other relevant qualifications. My full curriculum vitae is attached as Appendix A to this declaration. During the past 5 years I submitted declarations in inter partes reviews IPR2022-00481 and IPR2022-00285, and Ex Parte Reexamination Nos. 90/019,063 and 90/019,015, but otherwise have not testified in any cases.

5. I earned a Doctor of Engineering (Ph.D.) degree in Computer and Systems Engineering from Rensselaer Polytechnic Institute in 1985. From 1986 to 1991 I worked as a Circuit Design Engineer and then Principal Design Engineer for Bipolar Integrated Technology. I started as a new hire from the Ph.D. program at RPI and ended up as the chief architect, lead product designer, lead verification engineer, and developer of the world's only formal verification tool for bipolar circuits.

6. From 1991 until 2016, I worked for Intel Corporation, starting as a Senior Staff design engineer and quickly became a team leader delivering the package, I/O, and analog circuits for the first processors on each technology generation. In 2002 I was promoted to Intel Fellow (one of the company's highest technical positions) based on both results and risk management in getting five generations of microprocessors into high volume manufacturing on schedule, including the first use of C4 packaging at Intel. From 2002 to 2016 I worked as director of numerous groups within Intel (Mixed Signal Circuit Technology, Circuit Research Lab, SoC Design Lab, Low Power Mixed Signal Lab), where I led teams that delivered three separate firsts for both Intel and the world: the first microprocessors using strained silicon, the first products using high-k metal gate transistors, and the first Trigate (FinFET) product. During this time my role expanded to

leading a new company-wide analog/mixed signal circuit review team and leading the worldwide circuit architecture teams for I/O, analog, and supply regulator design IP. I currently operate my own consulting firm (Greg Taylor Consulting, Inc.), where I provide technical consulting services on electronic product and integrated circuit development for a variety of clients.

7. Additionally, I have been an IEEE Fellow since 2009. I have published more than 60 peer reviewed papers, and I am the inventor of 67 U.S. patents on integrated circuit design and testing.

8. Throughout my career, I have been involved in the design of I/O circuits that were required to survive electrostatic discharge events. This required understanding the discharge types, the paths that current would follow in an ESD event, and then designing pad cells, clamps, pad wiring, and power supply wiring to mitigate the effects of ESD.

9. In addition to the above, I was also responsible for power distribution circuitry in several generations of microprocessors I worked on. This included not just distributing large currents at low impedances to the digital circuits on chip, but also building on-chip regulators to power the less noise-tolerant analog circuits that were also integrated on chip. Later, while I was leading the Circuit Research Lab at Intel Corporation, my team successfully developed a 100 MHz on-chip switching regulator technology that took a high voltage input supply (twice what any transistor on the chip could survive) and delivered a high efficiency, clean, low voltage output without using any board level passive components.

III. Legal Standards

10. I am not an attorney and will not provide opinions of law. I have been instructed on principles of law, as set forth below, so that I may apply those principles, as appropriate, to my analysis.

A. Claim Construction

11. I understand that claim construction is a matter of law to be decided by the Court, but the Court may use input from expert testimony to assist in its determination of the meaning of claim terms.

12. I understand that terms in patent claims are given their ordinary and customary meaning as they would be understood by a person having ordinary skill in the art at the time of the invention (“POSITA”). In determining the ordinary and customary meaning, I understand one should look to those sources available that show what one of skill in the art would have understood disputed claim language to mean. I understand that the words of the patent’s claims and the context in which the term is used in the patent’s claims can be highly instructive in ascertaining the term’s meaning. I further understand that the terms of a claim are interpreted in the context of the entire patent, including the patent’s claims, its specification, its figures, and the prosecution history, also referred to as “intrinsic evidence.”

13. I understand that “extrinsic evidence”—i.e., evidence external to the patent and the prosecution history—includes evidence concerning the relevant scientific principles, the meaning of technical terms, and the state of the art. I understand that such evidence may also be useful in interpreting patent claims when the intrinsic evidence itself is insufficient. I understand that when patents and their claims refer to or utilize terminology from industry standards, the disclosures of the industry standards may also be useful in interpreting patent claims.

14. I understand that words or terms should be given their ordinary and customary meaning to a POSITA unless it appears that the inventors were using them to mean something else. In making this determination, the claims, the patent specification, and the prosecution history are of paramount importance. Additionally, the specification and prosecution history may be consulted to confirm whether the patentee has acted as its own lexicographer (i.e., provided its

own special meaning to any disputed terms), or intentionally disclaimed, disavowed, or surrendered any claim scope.

15. I understand that in general, a term or phrase found in the introductory words of the claim—the preamble of the claim—is limiting if it recites additional structure or steps, or is necessary to give life, meaning, and vitality to the claim. Conversely, a preamble term or phrase is not limiting where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention. In making this distinction, one should review the entire patent to gain an understanding of what the inventors claim they actually invented and intended to encompass by the claims.

B. Indefiniteness

16. I understand that a patent claim must particularly point out and distinctly claim the subject matter which the applicant regards as his invention. I understand that a patent claim is invalid if, read in light of the specification and the prosecution history, the claim fails to inform, with reasonable certainty, those skilled in the art about the scope of the invention. I understand that a patent claim must be precise enough to afford clear notice of what is claimed, thereby apprising the public of what is still open to them, while recognizing that absolute precision is unobtainable.

17. I understand that the indefiniteness inquiry focuses on the understanding of a skilled artisan at the time of the patent application. To understand the meaning of a claim term as understood by persons of skill in the art, I understand that courts may look to the intrinsic record, including the specification and the prosecution history, as well as extrinsic evidence, such as expert testimony, dictionaries, and learned treatises.

18. I also understand that so-called “terms of degree” are not necessarily indefinite and numerical precision is not required. Rather, I understand that Courts look to see whether the

claims and intrinsic record provides sufficient guidance to give one of ordinary skill reasonable certainty as to the scope of the claim.

C. Means Plus Function Claims

19. I understand that a means-plus-function claim term is one that recites a placeholder referring to a function, with the corresponding structure for performing that function identified in the specification.

20. I understand that, if a claim term uses the word “means” (e.g., “means for transmitting” or “transmitting means”), it is presumed to be a means-plus-function term. If, on the other hand, a claim term does not use the word “means,” it is presumed not to be a means-plus-function term. However, this presumption may be overcome where a claim term does not use the word “means” but recites a function without reciting sufficient structure for performing that function. For example, if a term uses functional language and/or a nonce word that would have the same effect as the word “means,” and does not provide sufficient structure, the presumption against means-plus-function claiming will be overcome. By contrast, where a term is used in common parlance byPOSITAs to designate a particular structure or class of structures, it is considered to have sufficient structure, and therefore will not be considered a means-plus-function term.

21. If a claim term is a means-plus-function term, the specification must supply the corresponding structure to carry out the function. If there is no corresponding structure in the specification, the term is indefinite.

IV. Level of Ordinary Skill in the Art

22. I have been asked to consider the abilities and education of a person of ordinary skill in the art as of the priority dates that apply to each of the Asserted Patents. The application

leading to the '665 patent was filed January 10, 2007. The application leading to the '074 patent was filed March 11, 2014, but claims priority to a provisional application filed March 14, 2013.

23. In my opinion, with respect to the '074 Patent, a POSITA would have a bachelor's degree in electrical engineering, computer science, or an equivalent technical degree and substantial experience (e.g., several years) in analog mixed signal design for integrated circuits. With respect to the '665 Patent, a POSITA would have a bachelor's degree in electrical engineering, computer science, or an equivalent technical degree and substantial experience (e.g., several years) in I/O and ESD design for integrated circuits. In either case, additional education related to the hardware, architecture, and circuit design aspects of could be substituted for professional experience, and vice versa.

24. While my experience level exceeds that of a POSITA, I am familiar with POSITAs from the time frame of the priority dates of the Asserted Patents, and my opinions regarding what a POSITA would understand are based on a POSITA's perspective at those times.

V. Technology Background

A. Electrostatic Discharge (ESD) Protection and the '665 Patent

25. In integrated circuits, ESD refers to the sudden inrush of current that can happen when the chip is brought into contact with static electricity. This is typically a concern during the processes of packaging chips and assembling chips onto printed circuit boards, though ESD events can occur in other circumstances as well. In the case of assembly, chips or boards may accumulate a static charge during shipment. This charge is rapidly dissipated as the two get close enough together to breakdown the air gap that separates them.

26. Typical integrated circuits operate at only a few volts and usually cannot tolerate higher voltages for very long. ESD discharges are therefore problematic because they can

involve hundreds or thousands of volts. Sometimes these high voltages will destructively break down an oxide on a chip, but more frequently the damage is thermal: the rapid deposition of a lot of energy in a small area can melt wires. In more spectacular cases, the wire can evaporate and explode, leaving a crater on the surface of the integrated circuit. In each of these cases, the strategy for mitigating ESD is to dissipate the energy so that there isn't enough charge concentrated in any small area to cause damage.

27. Since ESD events typically occur during chip assembly, ESD protection must account for the fact that the power supplies normally used to operate the chip are not themselves active (or even installed yet). This means that any circuitry that is intended to handle ESD must be powered by the ESD itself. (See Basic ESD and I/O Design, Sanjay Dabral & Timothy Maloney, John Wiley & Sons, 1998, section 2.7.1.)

28. When evaluating ESD protection circuitry it is important to keep in mind Kirchoff's First Law, which states that the net current flowing into any node is zero, i.e. the current flowing into the node is equal to the current flowing out of the node. This means that, although the static electricity that triggers an ESD event is typically introduced to the chip on one specific pad, the current flows from that pad to other places until it finds its way back off the chip. Design for ESD tolerance largely consists of managing the flow of that current while dissipating (generating heat in resistances) and/or storing (in capacitors) its energy.

29. The '665 patent discloses an invention for mitigating the effects of ESD. Namely, the '665 patent discloses a multi-pad system wherein "pad circuitry" is connected to each pad. When a static electric charge is deposited on a pad, that static charge opens a path from the pad to a common voltage rail (or multiple voltage rails) shared by all pads. The static charge then powers portions of the pad circuitry of the other pads, which in turn enable transistors to create a

conductive path between their pads and the common voltage rail. This creates an electrical connection between the pad where a static electric charge was deposited through the common voltage rail to the other pads of the system, allowing the charge to be spread out and shared by all pads, preventing the harmful concentration of charge in any one location.

B. USB Voltage Regulators and the '074 Patent

30. An important component in modern electronics is the voltage regulator—used to ensure that an electronic device has a steady voltage supply during all operational conditions. One form of voltage regulator addressed by the '074 patent is a “low-dropout (LDO) voltage regulator.” Because an LDO voltage regulator is, generally speaking, a form of a linear amplifier with feedback, it will be helpful to understand some basic concepts in amplifier circuitry.

1. Amplifiers and Feedback

31. Amplifiers are widely used in electronic systems to magnify small signals, drive large loads, and compensate for the degradation of signals propagating from one location to another.

32. One of the simplest amplifiers is a source follower, as shown in Figure 1 below. (Analysis and Design of Analog Integrated Circuits, Fourth Edition, Gray, Hurst, Lewis, Meyer, John Wiley & Sons, 2001, section 7.2.3.2) This circuit is used to isolate signal IN from the capacitance of the load OUT it drives. The strength (current) with which it drives the load is given by the transconductance of the MOSFET, known as “*gm*.” In general, *gm* of a MOSFET is given by $gm = \frac{2I_{DS}}{V_{GS}-V_t}$, where I_{DS} is the drain to source current, V_{GS} is the gate to source voltage, and V_t is the threshold voltage of the transistor. In these source followers, *gm* is determined by the value of the load resistor and the starting voltage of IN, as well as the specific transistor.

When the voltage gain of an amplifier remains very close to 1, also known as “unity gain”— the output is a replica of the input shifted by the threshold voltage of the source follower.

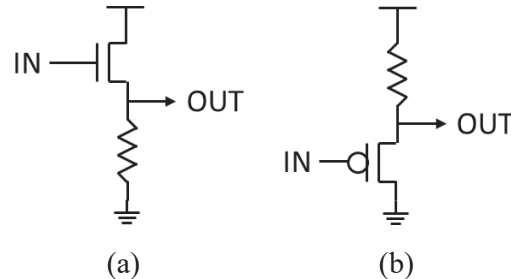


Figure 1. Source followers. (a) NMOS, (b) PMOS

33. Further, feedback techniques allow designers to create amplifiers with stable, predictable gain by leveraging negative feedback and passive components (primarily resistors and capacitors).

34. The operation of negative feedback is shown in Figure 2 below. (Analysis and Design of Analog Integrated Circuits, Fourth Edition, Gray, Hurst, Lewis, Meyer, John Wiley & Sons, 2001, section 8.7) The amplifier has a large DC gain of A and produces an output that is A times the difference in its input voltages. This information allows us to solve for the gain of the circuit, since we know the gain of the amplifier, the value of the resistors, and that no current flows into the inputs of the amplifier, yielding $\frac{OUT}{IN} = \frac{A}{1+A\beta}$, where $\beta = \frac{R2}{R1+R2}$. If the gain of the amplifier is large, then we have $\frac{OUT}{IN} = \frac{A}{1+A\beta} \cong \frac{1}{\beta} = \frac{R1+R2}{R2}$. So, the gain of the circuit is stable (controlled by the ratio of the resistors and independent of variation in the amplifier) as long as the gain of the amplifier remains large. Thus, the appropriate application of feedback overcomes the inherent variation in the transistors that provide the gain.

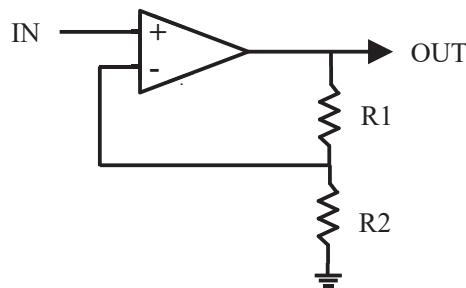


Figure 2. Negative Feedback

35. When the input signal IN is changing, the amplifier may end up amplifying the difference between the changing input and an older delayed output because not only do amplifiers have gain, but they also delay the input signal a small amount. If we input a sinusoidal signal into the amplifier and ramp up the frequency, the system will behave differently depending on the speed of the frequency. When the frequency is slow compared to the delay of the amplifier then circuit still responds as if it were a simple amplifier. But as the input changes more quickly (at a higher frequency) the amplifier is now amplifying the difference between the input and an older, delayed output. At some frequency this delay will result in the peaks of the input being compared to the troughs of the output (and vice versa) resulting in an output that swings between very large positive and negative voltages. The amplifier has become unstable.

36. Real amplifiers have a saving grace: when the input is pushed beyond some threshold frequency, the amplifier's gain starts dropping and continues to drop further as the frequency is increased. If the gain of the amplifier drops below 1 before it reaches the frequency where the peaks of the output collided with the troughs of the input, then the instability problem is resolved because that instability will be amplified by a gain of less than 1, i.e., it will be reduced.

37. Note that the output of the amplifier feeds back to the input, repeatedly passing through this gain. Accordingly, a small instability going repeatedly through a gain that amplifies it even a small amount will eventually overwhelm the amplifier response. Similarly, an

instability that repeatedly goes through a gain that shrinks it will eventually disappear. Put another way, the gain amplifies the degree of instability; if the “gain” experienced by the instability is less than 1, the “good” parts of the signal will be amplified while the instability is filtered away.

38. This leaves the problem of determining the stability of a feedback system. Mathematical “transfer functions” and Bode plots (such as those shown in Figure 1 of the ’074 patent) can help answer this.

2. Transfer Functions, Bode Plots, and “Poles and Zeroes”

39. In circuit analysis, a transfer function describes the mathematical relationship between a circuit’s input and its output as a function of frequency. (The Analysis of Linear Circuits, Charles M Close, Harcourt, Brace & World, 1966, section 6.1) Input frequencies that result in the transfer function equaling zero are known as “zeroes” and input frequencies that result in the transfer function equaling infinity are known as “poles.” “Poles” determine the “free response” or “natural behavior” of the system – how that system responds to changes. (The Analysis of Linear Circuits, Charles M Close, Harcourt, Brace & World, 1966, section 3.1) Note that the usage of “frequency” in this type of analysis is based on these frequencies being complex numbers of the form $\sigma + j\omega$, where $j = \sqrt{-1}$. Furthermore, the sinusoidal waveforms that we normally work with in the time domain are represented in the s-domain by $s = j2\pi f$, where “f” is the time domain frequency. Thus, a hypothetical transfer function $\frac{V_{out}}{V_{in}} = \frac{s-100}{s-5000}$ would describe the ratio of V_{out} (the output voltage of the circuit) to V_{in} (the input voltage of the circuit) as a function of frequency (s). This hypothetical function has a zero at 100 Hz, and a pole at 5000 Hz. Generally speaking, the number and value of those poles and zeroes dictates the stability of the circuit. In practice, the actual values of the poles and zeroes in a manufactured circuit will differ

from design intent based on the variation of real components from their target values. Thus, circuit designs should not be designed as “just barely” stable, but should include a margin of stability that will allow for these variations while maintaining stability.

40. Figure 3 below shows a Bode plot for a simple (first order or “single pole”) amplifier with 50 dB¹ of gain and a pole at 100 Hz. (The Analysis of Linear Circuits, Charles M Close, Harcourt, Brace & World, 1966, section 6.5) This plot includes two curves, a blue curve showing the gain of the amplifier and an orange curve showing the phase. The phase is a measure of the delay of the amplifier with respect to the signal frequency. When the phase is 0°, the output is aligned with the input (i.e., there is no delay). When the phase is -180° then the output peaks are aligned with the input troughs, which, as described above, leads to instability. One measurement of the stability of a system is the “phase margin”: the difference between the phase of the amplifier and -180° at the frequency where the gain drops to 0 dB (gain=1) (the “unity gain frequency”). This Bode plot shows a unity gain frequency of 30 KHz, because that is the frequency where the gain is 0 dB. At that point, the phase is -90°. Accordingly, this Bode Plot shows 90° of phase margin (-90° - -180° = 90°). Because the phase margin is significantly greater than zero at the unity gain frequency, this system is stable. That is generally true of first order systems. Unfortunately, real amplifiers (systems) are more complicated.

¹ Gain is measured in decibels (dB). When measuring the voltage of a signal the gain in decibels is given by the equation $Gain_{dB} = 20 \log_{10} H(f)$, where $H(f)$ is the linear gain of the amplifier as a function of frequency. Since the gain rolls off proportional to $1/f$ measuring gain in decibels converts this roll off to a line on a log plot such as a Bode plot.

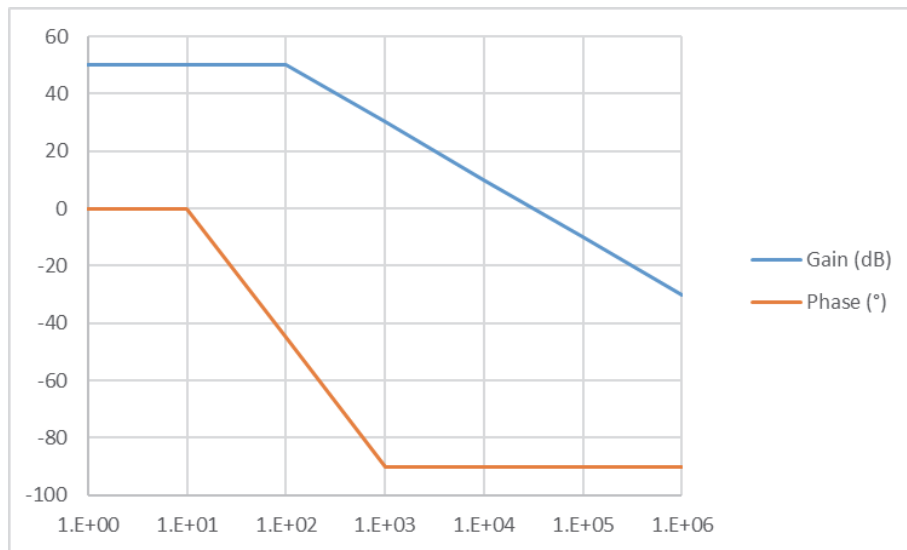


Figure 3. Bode plot for a first order amplifier

41. Bode plots are used because they can be easily constructed by hand without the use of computers once the poles and zeros of the system and the gain at a given frequency are known. Here the initial gain is 50 dB and this gain continues until the frequency of the first (and only) pole at 100 Hz. Beyond this pole the gain changes by -20 dB/decade (that is it drops by 20 dB (100x) for every 10x increase in frequency). At each additional pole the gain would drop by another -20 dB/decade when the frequency hits that pole value. In a similar manner, the phase changes by -90° as a pole is passed, with half of this change occurring a decade before the pole and half after. If there are additional poles, then the phase would accumulate an additional -90° of phase as each pole is passed. Zeros are the opposite of poles: as a zero is passed the slope of the gain is increased by 20 dB/decade and the phase is changed by $+90^\circ$.

42. Using this analysis, we can easily show what happens if the system has two poles at 100 Hz instead of a single pole, as shown in Figure 4. In this case the gain starts dropping by 40 dB/decade at 100 Hz, while the phase shifts by -180° around the same frequency. The phase hits -180° around a decade later while the gain is still 10 dB, enough to amplify the misaligned signals with the output fed back to be further amplified, ad infinitum (or at least until something

breaks). (The Analysis of Linear Circuits, Charles M Close, Harcourt, Brace & World, 1966, section 9.3.)

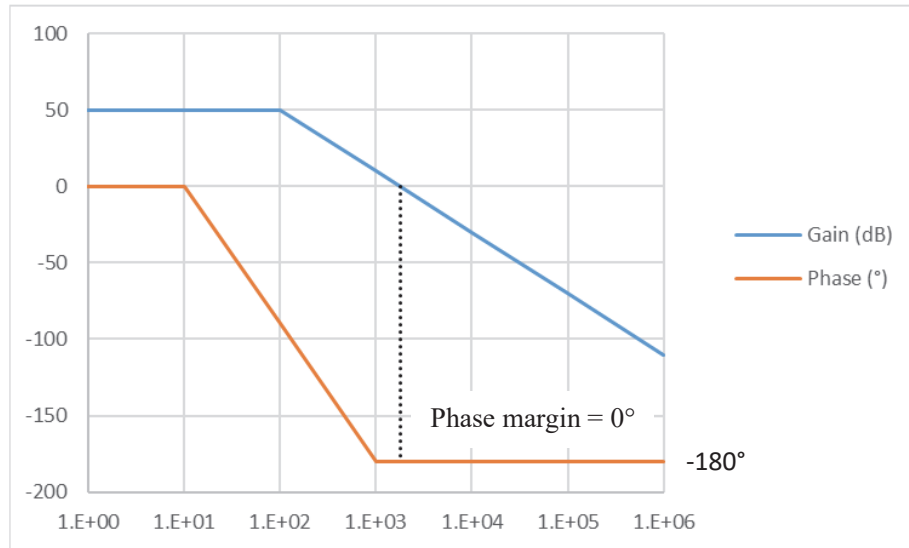


Figure 5. Bode plot with a double pole at 100 Hz

43. Figure 5 shows what the system looks like if the second pole is pushed to 100 kHz. This is beyond the frequency where the first pole has dropped the gain to zero, and as a result the system looks more like Figure 3. In this case the first pole dominates the behavior of the system, and it remains stable. Note that even though the dominant pole is three orders of magnitude lower than the added pole, the added pole still noticeably reduced the phase margin of the system.

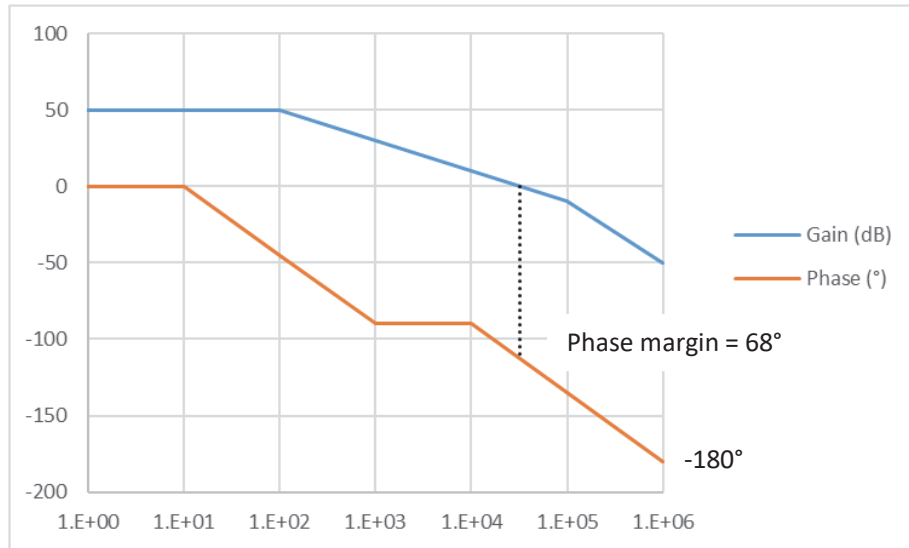


Figure 5. Bode plot with poles at 100 Hz and 100 kHz

44. The performance of a voltage regulator, reflected in its transfer function, is dictated by the type of components and arrangement of components comprising that regulator. For example, Low Dropout Regulators typically include an output capacitance to deal with high frequency changes in the load current. The series resistance (ESR or Effective Series Resistance) of the wires leading to the capacitor, shown in Figure 6, contributes a zero to the regulator. The frequency of this zero is given by $f_{zero} = \frac{1}{2\pi R_{ESR} C_{OUT}}$. As mentioned earlier, in the corresponding Bode plot, this zero adds +90° to the phase and causes the magnitude to rise at 20 dB/decade. And if the capacitor ESR varies, then the placement of this zero will shift.

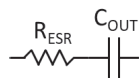


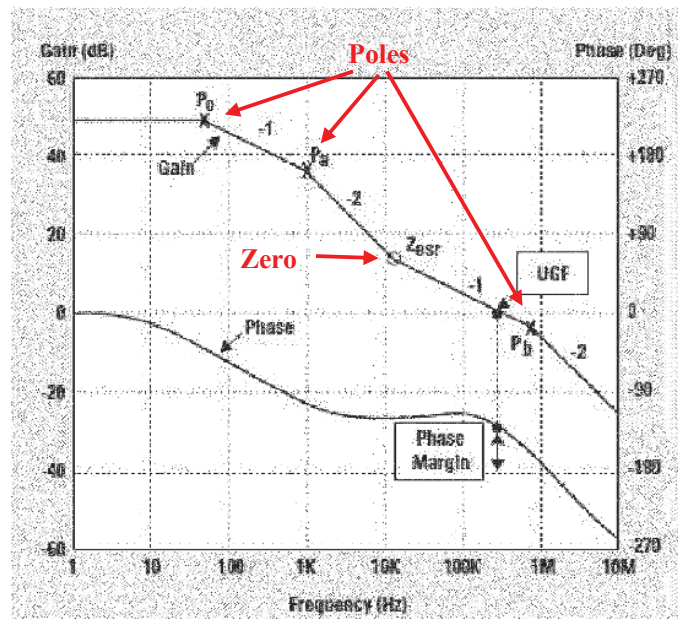
Figure 6. Capacitor and ESR model

45. And as the '074 patent explains, because the ESR of external compensation capacitors can vary widely depending on a lot of factors outside the regulator designer's control, including the capacitor manufacturer, the orientation of the capacitor on the physical board, the

quality and length of the traces (wires) connecting the capacitor to the regulator, etc., this poses a big problem for designers hoping to build a stable regulator that can handle a wide range of ESR values. '074 patent, 1:25-45.

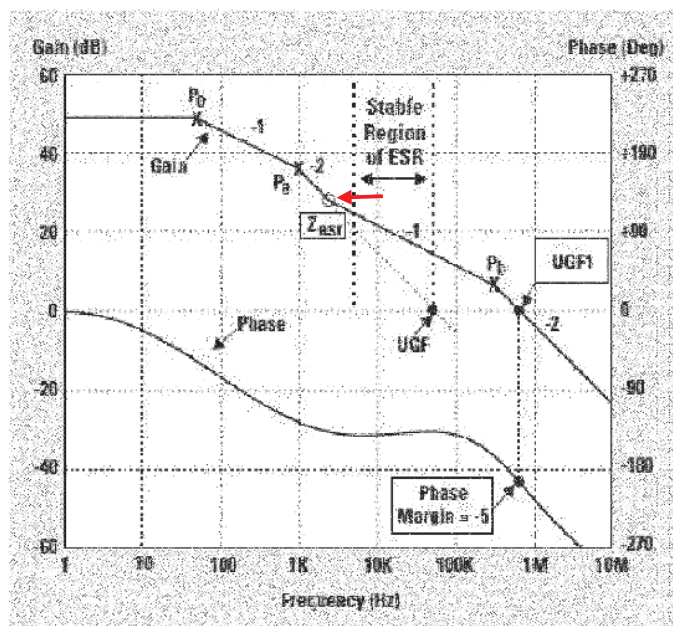
46. This problem is discussed in the context of the Bode plots in the '074 patent.

Figure 1(a) from the '074 patent is shown below and shows three poles, P_0 (~50 Hz), P_a (~1 kHz), and P_b (~800 kHz), as well as one zero provided by the ESR of the decoupling capacitor at about 10 kHz, annotated in red. The original also includes annotations between the locations of the poles and zero indicating the net number of zeros to the left of the point where the annotation is made. Thus, we see -1 between the first two poles, indicating that the slope is -20 dB/decade; followed by -2 after the second pole, indicating a slope of -40 dB/decade. This changes back to -1 after the zero and to -2 again after the third pole. Finally, the original includes annotation showing 40° of phase margin at the unity gain frequency ("UGF").



'074 Patent Figure 1(a) Normal Frequency Response with annotation
Prior Art

47. Figure 1(b) in the '074 patent shows what happens if the ESR of an external capacitor is more than doubled, shifting the zero to ~ 2 kHz. This pushes out the unity gain frequency, reducing the phase margin to -5° , driving the Bode plot well into instability. This variation could be caused by the use of a different capacitor, manufacturing variation in the capacitor, different mounting on the board, differences in the manufacturing or design of the board, or a combination of all of these factors. The original patent figure includes annotations showing the acceptable frequency range for the “zero” provided by the combination of the output capacitor and ESR (“ Z_{ESR} ”). Being either below or above this range of ESR values leads to instability. An ESR to the left of this range creates instability because a low zero frequency pushes the unity gain frequency far to the right, meaning that the phase margin will have dropped below 0° before the unity gain frequency. An ESR to the right of this range creates because it leaves the decrease in phase shift caused by the poles uncompensated until a higher frequency, meaning again that the phase shift will drop below 0° before the unity gain frequency.



'074 Patent Figure 1(b) ESR value too high with zero shift annotated
Prior Art

3. Gain-Bandwidth Tradeoff

48. A common figure used to describe amplifiers is the gain-bandwidth product. For amplifiers that are dominated by a single pole the product of the amplifier gain and its bandwidth is approximately constant as feedback is used to change the bandwidth of the amplifier. This characteristic means that the most common tradeoff when designing an amplifier circuit (including feedback) is between gain and bandwidth—increasing one invariably means compromising on the other.

49. For example, in the figure below the unity-gain bandwidth is 100 MHz. That is, the gain drops to 1 (unity-gain), at a frequency of 100 MHz. The raw amplifier (the amplifier without any feedback loop, also known as “open loop”) has a gain at low frequency of 1 million and a pole at (bandwidth of) 100 Hz. If feedback is added (“closed loop”) to decrease the gain to 100, the bandwidth (the frequency at which the gain has dropped 3 dB below its DC value) would consequently rise to 1 MHz. If the gain were decreased to 10, the bandwidth would increase to 10 MHz, etc. In all cases the product of the gain and the bandwidth is the same: 100 MHz. Note that this use of feedback can only decrease the gain of the raw amplifier, trading reduced gain for increased bandwidth. Increasing both gain and bandwidth requires increasing the gain-bandwidth of the amplifier – replacing it with a different amplifier at significant cost in area and power. This sliding scale tradeoff between gain and bandwidth would have been well-understood by POSITAs as of the priority date. (Analysis and Design of Analog Integrated Circuits, Fourth Edition, Gray, Hurst, Lewis, Meyer, John Wiley & Sons, 2001, section 9.2.)

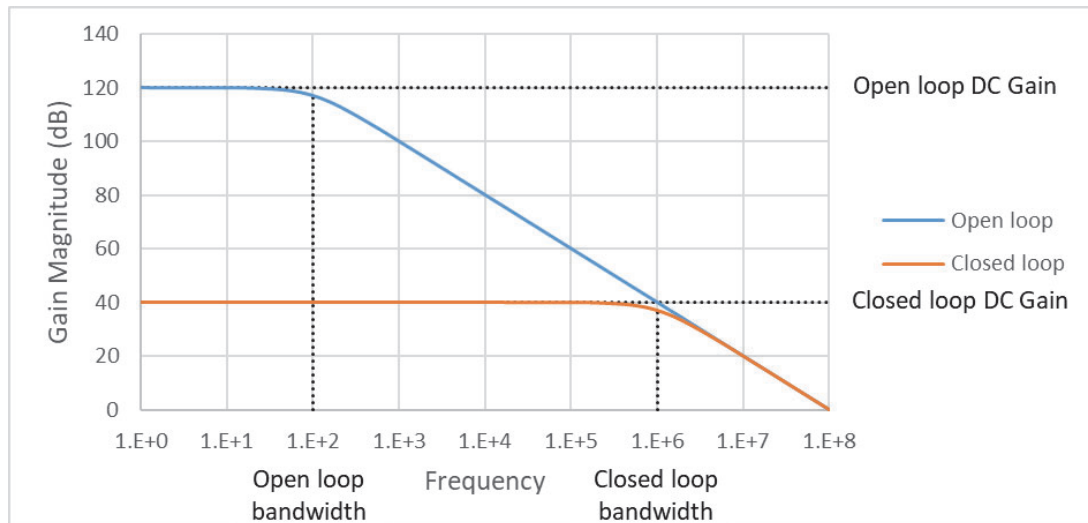


Figure 6. Gain magnitude versus frequency for basic amplifier and feedback amplifier
Adapted from Analysis and Design of Analog Integrated Circuits Figure 9.2

VI. Disputed Claim Terms

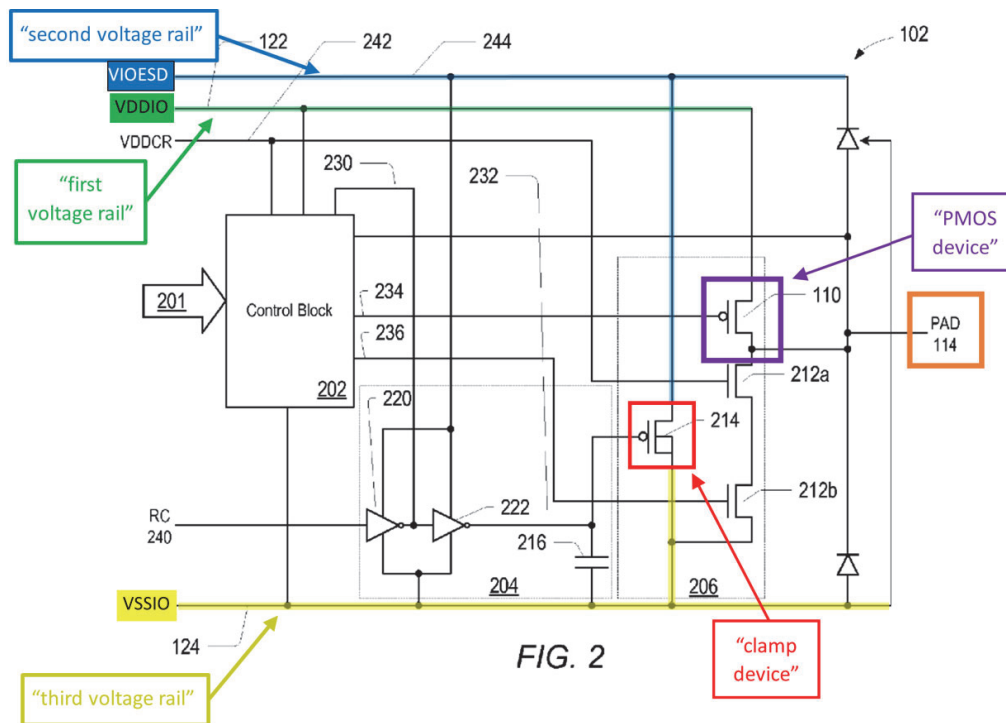
A. Term 1 – “second voltage rail” (’665 Patent, claim 1)

No.	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
1	Plain and Ordinary Meaning Alternatively, “a second voltage rail that is distinct from the third voltage rail but may or may not be distinct from the first voltage rail”	“a second voltage rail that is distinct from the first voltage rail”

50. The structure referenced in this claim is shown in Figure 2 of the ’665 patent. The “first voltage rail” is VDDIO 122, the “second voltage rail” is VIOESD 244, and the “third voltage rail” is VSSIO 124.

51. Specifically, claim 1 confirms that the “first voltage rail” is VDDIO where it specifies that the claimed PMOS device (annotated in purple below) sits between the “first node coupled to a first voltage rail” (annotated in green) and the “second node coupled to a physical pad

having capacitance” (annotated in orange). ’074 patent, claim 1. This is consistent with the specification’s description of Figure 2: “**PMOS device 110** . . . [is] coupled between **VDDIO rail 122** and **PAD 114**.” (’665 patent, 4:33-35.) Likewise, claim 1 requires that the control block “turn[s] on the . . . one or more output transistor devices [PMOS devices]” thereby connecting the pad to the first voltage rail so it may share the charge. Again, this is consistent with the specifications description: during an ESD event, the “**PMOS devices** turn[] on . . . resulting in the charge being shared across all **pads**” via the VDDIO rail. (’665 patent, 4:13-19, 5:29-35.)



52. In addition, claim 1 and the specification confirm that the “second voltage rail” refers to VIOESD in Figure 2. Specifically, claim 1 requires “a **clamp device** configured between a **second voltage rail** and a **third voltage rail**.” The specification confirms, as illustrated in annotated Figure 2 above, that the clamp 214 is situated between VIOESD (the “second” voltage

rail) and VSSIO (the “third” voltage rail). Namely, Figure 2 includes a “**clamp device 214** configured to shunt **VIOESD rail 244** and **VSSIO rail 124**.” (’665 patent, 5:13-17.)

53. The specification also explains that VIOESD and VDDIO may be the same power rail: “It should also be noted that **VIOESD 244** and **VDDIO 122** may in fact be the same power/supply rail, and alternate embodiments may be configured with a single power rail providing power to the circuit and/or system components that are powered by **VIOESD 244** and **VDDIO 122** in the embodiment shown in FIG. 2. In general, the ESD rail and the power supply rail can be the same supply rail, and separate supply rails (e.g. **VIOESD 244** and a distinct **VDDIO 122**) may not be required.” (’665 patent, 5:57-65.) Indeed, a POSITA would have education and/or experience working with systems with one, two, or more supply rails.

54. Note that VSSIO 124 (the “third voltage rail” in claim 1 of the ’665 patent) must be distinct from the other two rails. That is because it provides the negative supply to the output driver. If there were only one power rail for the output driver, then it would be able to drive only that one voltage out of the chip and thus would be unable to move any data off of the chip. Furthermore, if both ends of the clamp 214 in ’665 Figure 2 were tied to the same supply rail then the clamp would serve no purpose. Clamping a supply to itself is redundant.

55. In my opinion and for the above reasons, a POSITA would have understood “second voltage rail,” in the context of these claims, to have its plain and ordinary meaning. In particular, a POSITA would have understood that the claimed “second” voltage rail must be distinct from the “third” voltage rail but need not be distinct from the “first” voltage rail.

B. Term 2 – “an enable/disable function to enable/disable the biasing circuit for reducing standby current” (’074 Patent, claim 1)

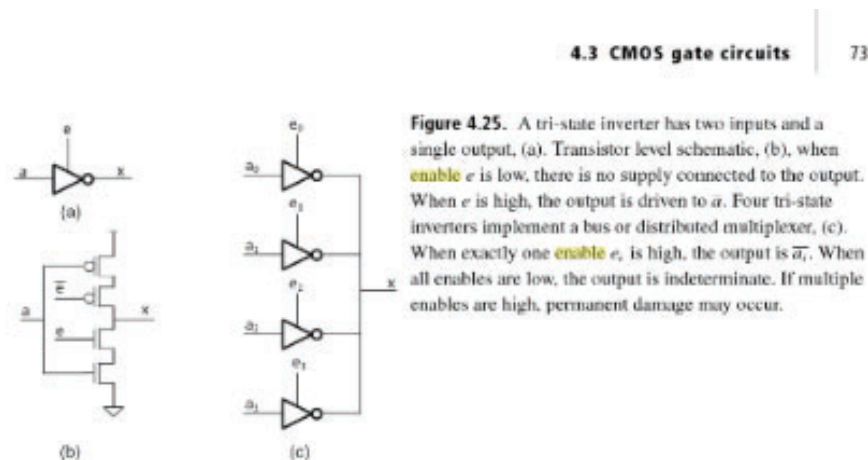
No.	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
2	Not subject to 35 U.S.C. 112 ¶ 6. To the extent the court determines that § 112 ¶ 6 applies: Function: to enable/disable the biasing circuit for reducing standby current Structure: enable/disable signal input line (Node M)	Indefinite; Subject to 35 U.S.C. § 112 ¶ 6 without any corresponding structure

56. In my opinion, a POSITA would have understood the term “an enable/disable function to enable/disable the biasing circuit for reducing standby current” to refer to a structural input to the biasing circuit structure and not merely a functional result.

57. In particular, a POSITA would have understood the term refers to an input for turning one or more transistors on or off like a switch to enable or disable the flow of current. A POSITA would have recognized that there are only a limited number of ways for enabling/disabling the flow of current in a circuit and that by far the most common way is to turn on or off the transistor itself through which current is flowing. This is a fundamental technique that is used in all types of applications, such as disabling current in a smartphone circuit or disabling the coils in a room heater when a given temperature is reached.

58. Moreover, because engineers routinely use an input to a circuit to enable or disable it, they often use the term “enable” as the name of that structural input. For example, a review of datasheets for a number of commercially available voltage regulators confirms that “ENABLE” is a common description for a physical input line. Ex. 1 (<https://www.ti.com/lit/gpn/tps7a20>); Ex. 2 (<https://www.analog.com/media/en/technical-documentation/data-sheets/max25302a-max25302b.pdf>); Ex. 3 (<https://www.st.com/resource/en/datasheet/ld39200.pdf>);

Ex. 4 (<https://www.diodes.com/assets/Datasheets/AP7331.pdf>). Similarly, a 2012 textbook on digital circuit design describes a circuit with three physical input lines, one of which is called “enable e ” and is used for turning on or off the circuit: “When the enable e is high ($\bar{e}$ is low), the middle two transistors are on.” Ex. 5 (Digital Design, A Systems Approach, William J. Dally & R. Curtis Harting, Cambridge University Press, 2012, section 4.3.4., Figure 4.25))



59. Thus, a POSITA would have understood the claimed “enable/disable function to enable/disable the biasing circuit for reducing standby current” to refer to a particular structure, or class of structures, commonly used for enabling and disabling circuit elements, as exemplified in the exhibits above.

60. It is not surprising that circuit designers use the term “enable” to refer to this structure, because many (if not most) circuit blocks and inputs are named according to their functions. This is so engineers can quickly comprehend what the block does and how to use it. Among other examples, pins that control timing are “CLOCK”, “CLK”, or “CK”; pins that initialize a part are “RESET”; power supplies that deliver a constant voltage start with “V” followed by an indicator of the type of voltage (“VSS” for the source/low voltage, “VDD” for the

drain/high voltage, “VBIAS”, “VREF”, ...); and enables are “ENABLE”, “ENABLE/DISABLE,” “OUTPUT ENABLE”, or “CLOCK ENABLE”.

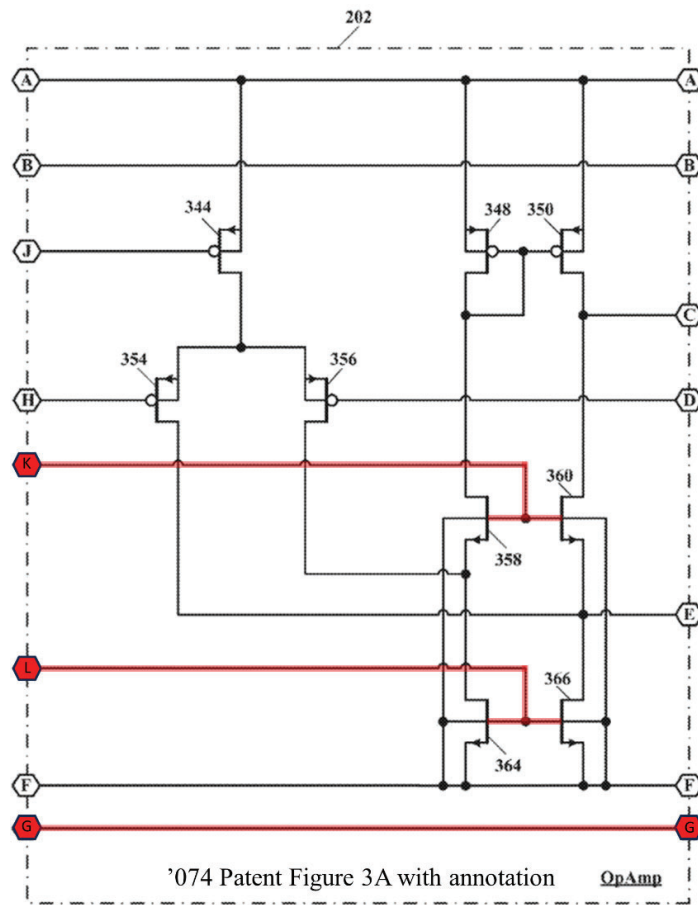
61. I note that the labels “ENABLE” and “ENABLE/DISABLE” are interchangeable, and refer to the same structure. “Enable” is simply shorthand in which the “disable” is implied, because if an “enable” must either be on (i.e., enabling transistors) or off (i.e., disabling transistors).

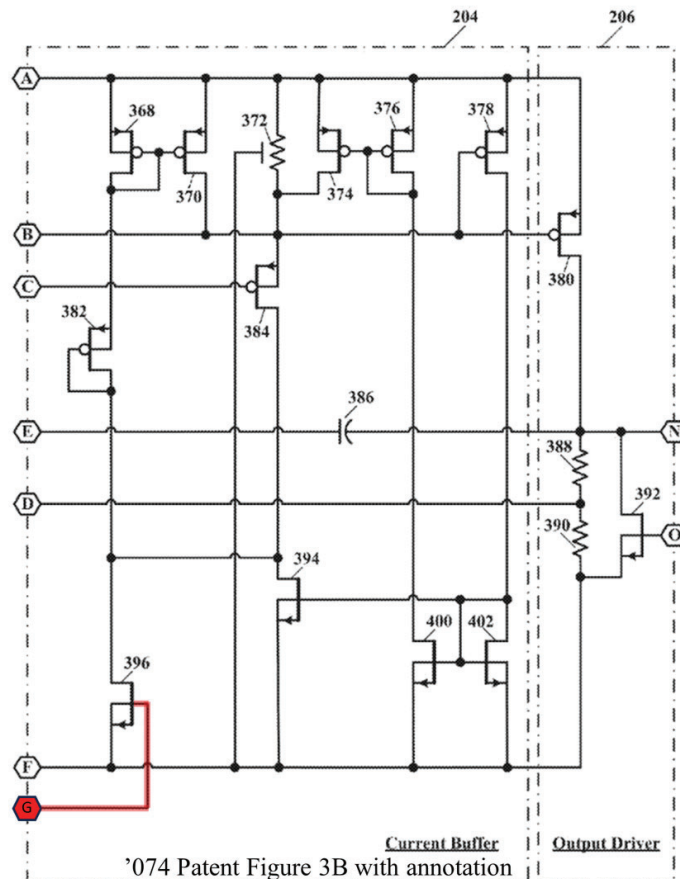
62. I understand that—because a POSITA would have understood the term “an enable/disable function to enable/disable the biasing circuit for reducing standby current” to refer to structure, and not function—so-called “mean plus function” rules do not apply. However, to the extent that the Court applies means plus function rules, in my opinion, the claimed function would be “to enable/disable the biasing circuit for reducing standby current” and the corresponding structure disclosed in the specification is the enable/disable signal input line (Node M) shown in ’074 Figure 3 and described in the specification at 4:43-46.

63. Specifically, the specification explains, in the context of ’074 Figure 3’s biasing circuit, that “[t]ransistors 320, 330, 334 and 336 may be shut off during disabling/power down operation to make sure this circuit will consume substantially no DC current. . . . **Node M is the enable signal coming to the regulator circuit so that the module can be turned off when disabled.**” (’074 patent, 4:44-54.) That is, Node M can force node J high through PMOS 320, which turns off PMOS 328. PMOS 328 provides the current that biases current source references K and L, which are shut off when this bias current is eliminated. They in turn shut off current bias NMOS devices 358, 360, 364, and 366 within the rest of OpAmp 202 thereby eliminating the power drawn by both the bias circuits in Figure 3 of the ’074 patent as well as the OpAmp power in Figure 3A of the same patent. At the same time, M can turn on NMOS 336, which pulls node G

in **green**.







C. Term 4 – “wherein the gm-boost circuit enables the current buffer driver to have large gm value” (’074 Patent, claim 4)

No.	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
4	Not indefinite. Plain and Ordinary Meaning Alternatively, “wherein the gm-boost circuit increases the gm value of the current buffer driver”	Indefinite

64. In my opinion, a POSITA would have understood the term “wherein the gm-boost circuit enables the current buffer driver to have a large gm value” with reasonable certainty. In particular, the specification provides objective guidance to a POSITA to understand the scope of the claim in the context of this invention.

65. As an initial matter, I note that Aptiv does not contend that a POSITA would not have understood the concept of gm-boosting a circuit as described in the '074 patent. Rather, Aptiv appears to assert that the word “large” makes the term indefinite. But this ignores the context in which “large gm value” is used in the '074 patent specification. According to the '074 specification, “[t]he key to being able to use smaller value internal and external capacitances is to have *a large gm current driver buffer* amplifier 204 between the first stage Op Amp 202 and the last stage power output driver 206. (’074 patent, 3:58-62.) The specification further explains that “various values of ESR may be handled by separating the poles inside of the voltage regulator circuit sufficiently to create an approximate one pole system.” (’074 patent, 3:50-53.) Thus, a POSITA would have understood *why* the circuitry of the '074 patent includes a gm-boost circuit.

66. As described above, a “pole” here represents a complex frequency at which the transfer function of the circuitry goes to infinity. While a system with a single well-behaved pole is stable, adding additional poles for gain, bandwidth, or compensation purposes can lead to instability. Roughly speaking, additional poles are undesirable because they undermine stability and, when customer-selected components are part of the feedback loop, the usability of a circuit.

67. The specification explains further that “[t]he implementation of the OpAmp 202 as a folded cascode configuration is due to its unique architecture which results in a single pole at the output that minimizes the complexity of its compensation. The current buffer driver 204 acts like a low impedance driver which connects between the OpAmp 202 and the output driver 206. Since the output driver 206 may provide very large amounts of switching current during power supply operation, the gate capacitance is significantly high due to the size of the driver, thereby resulting in the generation of a pole at relatively low frequency. Thus, the current buffer driver 204 pushes this pole to a high frequency beyond unity-gain frequency due to its low-impedance characteristics

in order to get the pole splitting effect.” (’074 patent at 4:1-14.) In this context, “pole splitting” and “compensation” refer to techniques for shifting the locations of the non-dominant poles so that there will be only one (dominant) pole present within the operating frequency range of interest.

68. As a POSITA would have understood, this pole splitting could be accomplished by increasing the transconductance (gm) of the current buffer driver. As just described, gm-boosting is used as part of the pole-splitting compensation technique—which is used to clear non-dominant poles out of the frequency range of operation of the op amp circuit(s) of the ’074 patent. A POSITA would therefore understand that the word “large” in the “large gm value” claim term simply refers to boosting gm to a value at-or-beyond which the “second-most-dominant pole” will be pushed close to or beyond the unity-gain frequency and the impact of the pole is pushed above-and-beyond the unity-gain frequency.

69. Finally, a POSITA would have understood that the requisite gm is a context-dependent value. Some variables that would affect the necessary gm in a given scenario include, but are not limited to, the output voltage being delivered by the regulator, the amount of power the regulator is delivering, the power supply’s precision, the voltage regulator’s response time, the characteristics (including ESR) of the external bypass capacitor, and the manufacturing process used to fabricate the regulator circuit. But although the necessary gm varies by application and context, a POSITA would have understood based on the ’074 patent and their general background knowledge, how to calculate a gm sufficiently large in any given scenario to push the second most dominant pole above and beyond the unity gain frequency.

D. Term 5 – “low gain and high bandwidth amplifier” (’074 Patent, claim 8)

No.	Microchip’s Proposed Construction	Aptiv’s Proposed Construction
5	Not Indefinite. Plain and Ordinary Meaning Alternatively, “amplifier optimized for high bandwidth with a commensurate reduction of gain”	Indefinite

70. In my opinion, a POSITA would have understood with reasonable certainty the term “low gain and high bandwidth amplifier” as having its plain and ordinary meaning. In particular, the specification provides objective guidance to a POSITA to understand the scope of the claim in the context of this invention.

71. As an initial matter, and as discussed above in my Technology Background, a POSITA would have been aware of the sliding scale tradeoff between gain and bandwidth in an amplifier and thus would have understood how a low gain / high bandwidth amplifier differs from a “traditional” high gain / low bandwidth amplifier. Since the mathematical product of gain and bandwidth is approximately constant, a POSITA would have understood that increasing bandwidth is the inherent result of reducing the low frequency gain of the amplifier. Put another way, a POSITA would have understood that a “low gain and high bandwidth amplifier” simply refers to an amplifier positioned at the other end of the gain/bandwidth scale from a traditional OpAmp.

72. Further, the specification explains that it achieves the object of the invention using, among other things, a “low-gain, high bandwidth amplifier” designed such that “(1) The architecture forms only one pole at the output of the folded stage which reduces the complexity of frequency compensation, [and] (2) it provides a good driving capability for the source follower stage of the current buffer.” (’074 patent, 4:24-42). Thus, a POSITA would have understood the

patent as teaching the goal of balancing sufficient bandwidth such that the amplifier forms only a single pole while still offering sufficient gain to drive the current buffer.

73. As explained below, and confirmed by the '074 specification and diagrams, a POSITA would have understood that this increase in bandwidth (and commensurate reduction in gain) could be achieved with a simple feedback loop, or by modifying an existing loop. As can be seen in Figure 6 (repeated below) extending the bandwidth of an amplifier (within the bounds of its gain-bandwidth product) is accomplished by “throwing away” the unneeded low frequency gain.

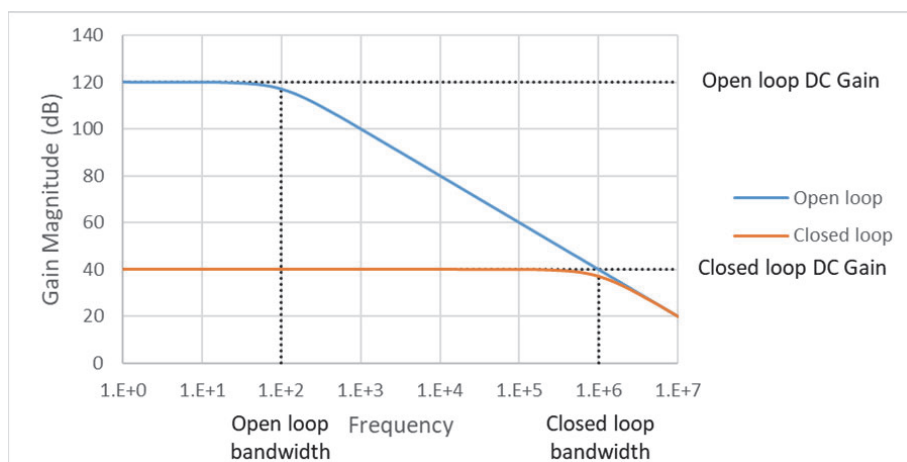


Figure 6. Gain magnitude versus frequency for basic amplifier and feedback amplifier
Adapted from Analysis and Design of Analog Integrated Circuits Figure 9.2

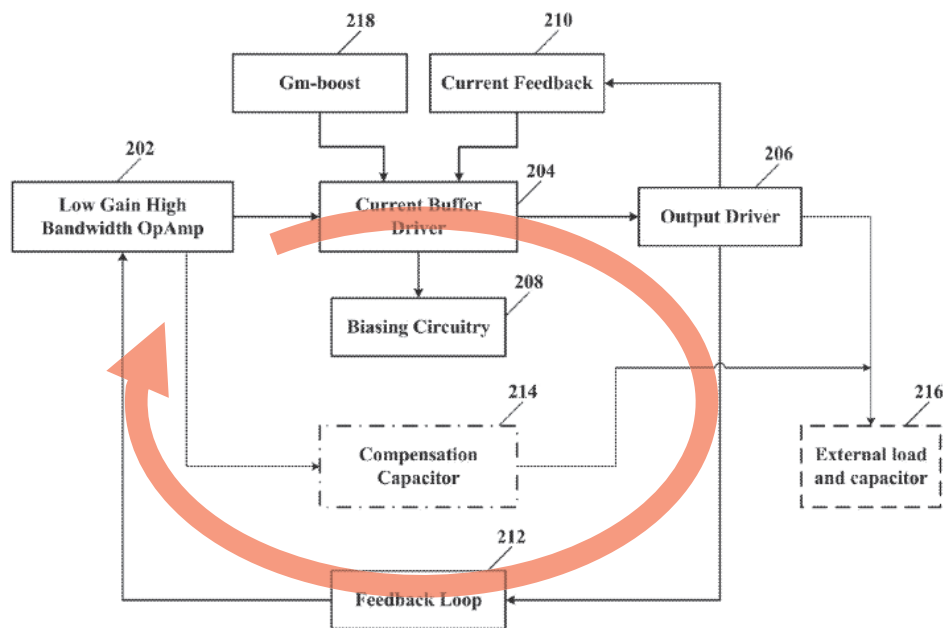
74. Figure 2 from the '074 patent shows the top-level diagram of the regulator circuit and confirms how the invention can use feedback to effect a low-gain, high-bandwidth amplifier. In particular, the pictured circuit includes multiple amplifiers and multiple loops. As pointed out in the specification:

Since the output driver 206 may provide very large amounts of switching current during power supply operation, the gate

capacitance is significantly high due to the size of the driver, thereby resulting in the generation of a **pole at relatively low frequency**.

(’074 patent 4:6-11.)

75. A POSITA would have understood that feedback loop 212 operates from Output Driver 206 to Low Gain High Bandwidth OpAmp 202 as annotated in Figure 2 from the ’074 patent below, and includes Current feedback 210, Compensation Capacitor 214, and the effects of External load and capacitor 216, the ESR of which contributes a zero to the system. Because this loop encompasses these other poles and zeroes, they will all interact with one another to create the poles and zeroes of the overall circuit’s transfer function, as was the case for the Bode plots shown in Figures 1 and 1A in the ’074 patent.



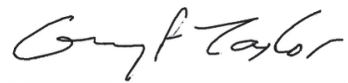
’074 Patent Figure 2 – with annotation

76. As the ’074 patent further explains, the voltage regulator should be designed so it “acts like a pseudo ‘one-pole’ system that is independent from the output pole changing so long as it falls within the bandwidth of the system” (’074 patent, 5:43-45) and a POSITA would have understood this pole-splitting results in a more stable system dominated by a single low frequency

pole. Raising the gain of Low Gain High Bandwidth OpAmp 202 would increase the overall gain of the top-level system, which would push out the unity-gain frequency and reduce the dominance of the compensated pole at the output of OpAmp 202. Given these constraints that this amplifier must meet if the overall system is to be dominated by the pole of this OpAmp while the overall system is also an effective regulator, a POSITA would have readily understood the claims' use of a "low gain and high bandwidth amplifier."

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct, and that all statements reflect my opinions based upon my knowledge and experience.

Date: March 1, 2024

A handwritten signature in cursive script, reading "Gregory F. Taylor".

Gregory F. Taylor

Appendix A

Gregory F. Taylor

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Experience

- Greg Taylor Consulting, Inc.**, Portland OR
- 2016- **Principal.** Technical consulting on electronic product and integrated circuit development with a variety of clients, as well as patent expert witness work.
- 2016-2020 **zGlue Corporation**, Hillsboro OR
zGlue Fellow. Consulted on new product planning; integrated circuit design, specification, validation, testing, and manufacturing; represented zGlue at opencompute.org's Open Domain Specific Architecture (ODSA) working group.
- Intel Corporation**, Platform Engineering Group, Hillsboro OR
- 2014-2016 **Intel Fellow, Hard IP Group Chief Architect.** Leading the worldwide circuit architecture teams for I/O, analog, and linear supply regulator design.
- 2008-2015 **Intel Fellow, Analog Review Committee lead.** Led an internal team driving the development of 22, 14, and 10 nm analog/mixed signal circuits across all product lines using Intel process technologies. Drove consistency and sharing of these IPs across most of the business units at Intel.
- Intel Corporation**, Intel Labs, Hillsboro OR
- 2013 **Intel Fellow, Director of the Low Power Mixed Signal Lab.** Started a new lab to develop analog/mixed signal circuits and design methods that will enable lower power computing and communication platforms.
- 2011-2013 **Intel Fellow, Director of the SoC Design Lab.** Led a multinational team to develop prototype Systems on Chip, including work to improve time to market and energy efficiency through improvements to chip design.
- 2008-2011 **Intel Fellow, Director of the Circuit Research Lab.** Led a team developing circuits and microarchitectures that will lead to lower power and higher performance computing platforms.
- Intel Corporation**, Logic Technology Development, Hillsboro OR
- 2004-2008 **Intel Fellow, Director of Mixed Signal Circuit Technology.** Led a cross organizational team coordinating the 45 nm and 32 nm collateral delivery between process technology development and multiple design projects. Technical lead for the team that developed I/O, clock generation, temperature sensing, and other analog circuits for use across all Intel microprocessors developed on 65 nm, 45 nm, and 32 nm manufacturing technologies, including the first commercial high-k metal gate based product. Started analog circuit development for what became the first commercial FinFET manufacturing process.
- 2002-2004 **Intel Fellow, Director of Mixed Signal Circuit Technology.** Managed the team responsible for the design of clock generation, clock distribution, I/O circuitry, package, power distribution and other mixed signal circuits for a pair of 90 and 65 nm Pentium® 4 processors, including the first commercial strained silicon based product.
- 1993-2002 **Principal Engineer/Component Design Manager.** Managed the team responsible for the design of clock generation, clock distribution, I/O circuitry, package, power distribution and other mixed signal circuits for Pentium, Pentium II, and Pentium III microprocessors in 0.35 through 0.13 μm technologies.
- 1991-1993 **Staff Design Engineer.** Designed a CMOS/ECL cache for the Pentium Microprocessor, Intel's first BiCMOS product, in 0.8 μm and 0.6 μm

technologies. Developed an Electrical Rules Checker to ensure the correctness of signaling between different frequency clock domains.

Bipolar Integrated Technology, Beaverton OR

1988-1991 **Principal Design Engineer.** Participated in all phases of the design of a second generation floating point chip. Made customer visits to determine product requirements; developed the architecture, test and validation plans; and designed the multiplier circuit. Developed an ECL Electrical Rules Checker and formal verification tool and supervised the package design. Consulted in the design, validation, and debug of Sparc® and MIPS® ECL microprocessors.

1986-1988 **Circuit Design Engineer.** Designed Emitter Coupled Logic floating point integrated circuits. Generated test suite and validated correctness of overall design. Developed a switch level simulator to verify the logical correctness of ECL gates. Completed debug and sustaining engineering.

Education

1983-1985 D.Eng. Computer and Systems Engineering, Rensselaer Polytechnic Institute (RPI), Troy, NY. Thesis topic: An Architecture for a Wafer Scale Integration Two Dimensional Fast Fourier Transform Processor.

1981-1983 MSEE Computer and Systems Engineering, RPI, Troy NY. Thesis topic: An ECL Floating Point Processor.

1977-1981 BSEE Computer and Systems Engineering, RPI, Troy, NY.

Other

- IEEE Fellow, 2009 to present.
- Fannie and John Hertz Foundation Fellowship, recipient, 1981 to 1985.
- VLSI Circuit Symposium Technical Committee, member, 1999 to 2006.
- Published more than 60 peer reviewed papers, 67 issued US patents.

Publications

"A 1–2 GHz Computational-Locking ADPLL With Sub-20-Cycle Locktime Across PVT Variation", Fahim ur Rahman, Greg Taylor, Visvesh Sathe, IEEE Journal of Solid-State Circuits, September 2019.

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"Analog Mixed Signal Design: The Technology Scaling Rate Limiter", Greg Taylor, Frontiers in Analog CAD, July 2011.

"SiP, SOC, and TSV: Issues in Getting from Technologies to Systems", Greg Taylor, GIT 3D System Workshop, June 2011.

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"A Wide Dynamic Range Self-Biased Fully Differential Operational Amplifier for Micro Mechanical Sensors and Actuators Circuitry", Mohamed Abdel-moneum, David Duarte, Greg Taylor, IEEE Sensors, November 2010.

"HVM Performance Validation and DFM Techniques used in a 32nm CMOS Thermal Sensor System", D. Duarte, P. Zepeda, S. Hsu, A. Maheshwari and G. Taylor, IEEE Custom Integrated Circuits Conference, September 2010.

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"A 1.05 V 1.6 mW, 0.45 °C 3 σ Resolution SD Based Temperature Sensor With Parasitic Resistance Compensation in 32 nm Digital CMOS Process", Hasnain Lakdawala, Y. William

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"Designing for Low Power", Tawfik Rahal-Arabi, Ali Muhtaroglu, and Greg Taylor, Electrical Performance of Electronic Packaging, October 2006.

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"Reducing the Impact of Power Supply Noise on Microprocessor Performance", T. Rahal-Arabi, K.L. Wong, M. Ma, J. Barkatullah, G. Taylor, Electrical Performance of Electronic Packaging, October 2005, pp. 307-310.

"Design and Validation of a Power Supply Noise Reduction Technique", Gang Ji, Tawfik R Arabi, Greg Taylor, IEEE Transactions on Advanced Packaging, August 2005, pp. 445-448.

"Enhancing Microprocessor Immunity to Power Supply Noise with Clock/Data Compensation", Tawfik Rahal-Arabi, Greg Taylor, Javed Barkatullah, Keng L Wong, Matthew Ma, 2005 Symposium on VLSI Circuits, June 2005, pp. 16-19.

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"On-Die Droop Detector for Analog Sensing of Power Supply Noise", Ali Muhtaroglu, Greg Taylor, Tawfik Rahal-Arabi, IEEE Journal of Solid State Circuit Design, April 2004, pp. 651-660.

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Exhibit 1

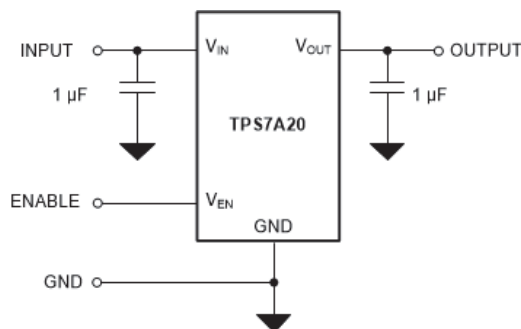
TPS7A20 300-mA, Ultra-Low-Noise, Low- I_Q , High PSRR LDO

1 Features

- Low output voltage noise: 7 μV_{RMS}
 - No noise-bypass capacitor required
- High PSRR: 95 dB at 1 kHz
- Very low I_Q : 6.5 μA
- Input voltage range: 1.6 V to 6.0 V
- Output voltage range: 0.8 V to 5.5 V
- Output voltage tolerance: $\pm 1.5\%$ (max)
- Very low dropout:
 - 140 mV (max) at 300 mA ($V_{\text{OUT}} = 3.3 \text{ V}$)
 - 145 mV (max) at 300 mA ($V_{\text{OUT}} = 3.3 \text{ V, DBV}$)
- Low inrush current
- Smart enable pulldown
- Stable with 1- μF minimum ceramic output capacitor
- Packages:
 - 1-mm $\times$ 1-mm X2SON
 - 0.616-mm $\times$ 0.616-mm DSBGA
 - 2.90-mm $\times$ 1.60-mm SOT23-5

2 Applications

- [Smartphones](#) and [tablets](#)
- [IP network cameras](#)
- [Portable medical equipment](#)
- [Smart meters](#) and [field transmitters](#)
- [Motor drives](#)
- [Wearables](#)



Simplified Schematic

3 Description

The TPS7A20 is an ultra-small, low-dropout (LDO) linear regulator that can source 300 mA of output current. The TPS7A20 is designed to provide low noise, high PSRR, and excellent load and line transient performance that can meet the requirements of RF and other sensitive analog circuits. Using innovative design techniques, the TPS7A20 offers an ultra-low noise performance without the addition of a noise bypass capacitor. The TPS7A20 also provides the advantage of low quiescent current, which can be ideal for battery-powered applications. With an input voltage range of 1.6 V to 6.0 V and an output range of 0.8 V to 5.5 V, the TPS7A20 can be used for a wide variety of applications. The device uses a precision reference circuit to provide a maximum accuracy of 1.5% over load, line, and temperature variations.

The TPS7A20 features an internal soft-start to lower the inrush current, thus minimizing the input voltage drop during start up. The device is stable with small ceramic capacitors, allowing for a small overall solution size.

The TPS7A20 has a smart enable input circuit with an internally controlled pulldown resistor that keeps the LDO disabled even when the EN pin is left floating and helps eliminate the external components used to pulldown the EN pin.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A20	X2SON (4)	1.00 mm $\times$ 1.00 mm
	DSBGA (4)	0.616 mm $\times$ 0.616 mm
	SOT-23 (5)	2.90 mm $\times$ 1.60 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (April 2022) to Revision G (May 2022)	Page
• Changed UVLO condition from rising to falling for YCJ and YCK packages.....	6

Changes from Revision E (December 2021) to Revision F (April 2022)	Page
• Changed DSBGA dimensions from 0.603 mm × 0.603 mm to 0.616 mm × 0.616 mm in <i>Features and Description</i> sections.....	1

5 Pin Configuration and Functions

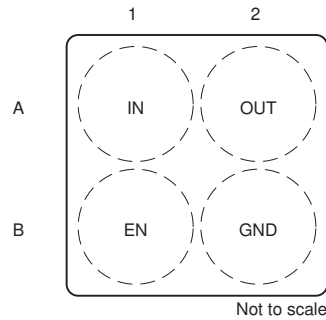


Figure 5-1. YCJ and YCK Packages, 4-Pin DSBGA (Top View)

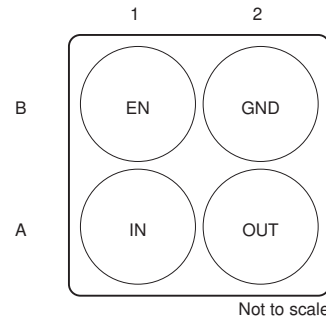


Figure 5-2. YCJ and YCK Packages, 4-Pin DSBGA (Bottom View)

Pin Functions: DSBGA

PIN		I/O	DESCRIPTION
NO.	NAME		
A1	IN	I	Input voltage supply. For best transient response and to minimize input impedance, use the nominal value or larger capacitor from IN to ground as listed in the <i>Recommended Operating Conditions</i> table. Place the input capacitor as close to the IN and GND pins of the device as possible.
A2	OUT	O	Regulated output voltage. A low equivalent series resistance (ESR) capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger capacitor listed in the <i>Recommended Operating Conditions</i> table. Place the output capacitor as close to the OUT and GND pins of the device as possible. An internal 150-Ω (typical) pulldown resistor prevents a charge from remaining on V_{OUT} when the regulator is in shutdown mode ($V_{EN} < V_{EN(LOW)}$).
B1	EN	I	Enable input. A low voltage ($< V_{EN(LOW)}$) on this input turns the regulator off and discharges the output pin to GND. A high voltage ($> V_{EN(HI)}$) on this pin enables the regulator output. This pin has an internal 500-kΩ pulldown resistor to hold the regulator off by default. When $V_{EN} > V_{EN(HI)}$, the 500-kΩ pulldown is disconnected to reduce input current.
B2	GND	—	Common ground.

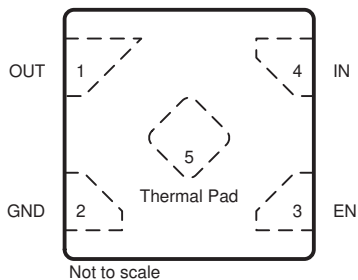


Figure 5-3. DQN Package, 4-Pin X2SON (Top View)

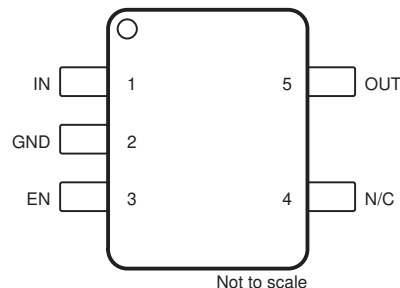


Figure 5-4. DBV Package, 5-Pin SOT-23 (Top View)

Pin Functions: X2SON, SOT-23

NAME	PIN		I/O	DESCRIPTION
	X2SON	SOT-23		
IN	4	1	I	Input voltage supply. For best transient response and to minimize input impedance, use the nominal value or larger capacitor from IN to ground as listed in the <i>Recommended Operating Conditions</i> table. Place the input capacitor as close to the IN and GND pins of the device as possible.
OUT	1	5	O	Regulated output voltage. A low equivalent series resistance (ESR) capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger capacitor listed in the <i>Recommended Operating Conditions</i> table. Place the output capacitor as close to the OUT and GND pins of the device as possible. An internal 150-Ω (typical) pulldown resistor prevents a charge from remaining on V_{OUT} when the regulator is in shutdown mode ($V_{EN} < V_{EN(LOW)}$).
EN	3	3	I	Enable input. A low voltage ($< V_{EN(LOW)}$) on this pin turns the regulator off and discharges the output pin to GND. A high voltage ($> V_{EN(HI)}$) on this pin enables the regulator output. This pin has an internal 500-kΩ pulldown resistor to hold the regulator off by default. When $V_{EN} > V_{EN(HI)}$, the 500-kΩ pulldown is disconnected to reduce input current.
GND	2	2	—	Common ground.
N/C	—	4	—	No internal electrical connection.
Thermal Pad	5	—	—	Thermal pad for the X2SON package. Connect this pad to GND or leave floating. Do not connect to any potential other than GND. Connect the thermal pad to a large-area ground plane for best thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (3)}

		MIN	MAX	UNIT
Voltage	V _{IN}	−0.3	6.5	V
	V _{OUT}	−0.3	6.5 or V _{IN} + 0.3 ⁽²⁾	
	V _{EN}	−0.3	6.5	
Current	Maximum output ⁽⁴⁾	Internally limited		A
Temperature	Operating junction, T _J	−40	150	°C
	Storage, T _{stg}	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The maximum value of V_{OUT} is the lesser of 6.5 V or (V_{IN} + 0.3 V).
- (3) All voltages are with respect to the GND pin.
- (4) Internal thermal shutdown circuitry protects the device from permanent damage.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	NOM	MAX	UNIT
V _{IN}	Input supply voltage	1.6		6.0	V
V _{EN}	Enable input voltage	0		6.0	V
V _{OUT}	Nominal output voltage range	0.8		5.5	V
I _{OUT}	Output current	0		300	mA
C _{IN}	Input capacitor ⁽²⁾		1		μF
C _{OUT}	Output capacitor ⁽³⁾	1		200	μF
ESR	Output capacitor effective series resistance			100	mΩ
T _J	Operating junction temperature	−40		125	°C

- (1) All voltages are with respect to GND.
- (2) An input capacitor is not required for LDO stability. However, an input capacitor with an effective value of 0.47 μF minimum is recommended to counteract the effect of source resistance and inductance, which may in some cases cause symptoms of system-level instability such as ringing or oscillation, especially in the presence of load transients.
- (3) Effective output capacitance of 0.47 μF minimum and 200 μF maximum is required for stability.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS7A20				UNIT
		DBV (SOT-23)	DQN (X2SON)	YCJ (DSBGA)	YCK (DSBGA)	
		5 PINS	4 PINS	4 PINS	4 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	187.1	166.1	199.6	201.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	85.5	103.6	2.8	2.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	54.4	110.6	67.5	69.3	°C/W
ψ _{JT}	Junction-to-top characterization parameter	27.1	3.0	1.4	1.4	°C/W
ψ _{JB}	Junction-to-board characterization parameter	54.1	103.3	67.4	69.2	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	98.8	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

at operating temperature range ($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$), $V_{IN} = V_{OUT(NOM)} + 0.3\text{ V}$ or 1.6 V , whichever is greater, $V_{EN} = 1.0\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$ (unless otherwise noted); all typical values are at $T_J = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ΔV_{OUT}	Output voltage tolerance	$V_{IN} = (V_{OUT(NOM)} + 0.3\text{ V})$ to 6.0 V , $I_{OUT} = 1\text{ mA}$ to 300 mA , $V_{OUT} \geq 1.85\text{ V}$ (DQN, YCJ, YCK packages)		-1.5		1.5	%
		$V_{IN} = (V_{OUT(NOM)} + 0.3\text{ V})$ to 6.0 V , $I_{OUT} = 1\text{ mA}$ to 300 mA , $V_{OUT} \geq 2.8\text{ V}$ (DBV package)		-1.5		1.5	
		$V_{IN} = (V_{OUT(NOM)} + 0.5\text{ V})$ to 6.0 V , $I_{OUT} = 1\text{ mA}$ to 300 mA , $V_{OUT} < 1.85\text{ V}$ (DQN, YCJ, YCK packages)		-30		30	mV
		$V_{IN} = (V_{OUT(NOM)} + 0.3\text{ V})$ to 6.0 V , $I_{OUT} = 1\text{ mA}$ to 300 mA , $V_{OUT} < 2.8\text{ V}$ (DBV package)		-40		40	
ΔV_{OUT}	Line regulation	$V_{IN} = (V_{OUT(NOM)} + 0.3\text{ V})$ to 6.0 V , $I_{OUT} = 1\text{ mA}$			0.03		%/V
ΔV_{OUT}	Load regulation	$I_{OUT} = 1\text{ mA}$ to 300 mA (DQN, YCJ, YCK packages)			13		mV
		$I_{OUT} = 1\text{ mA}$ to 300 mA (DBV package)			19		
I _{GND}	Quiescent ground current	$V_{EN} = V_{IN} = 6\text{ V}$, $I_{OUT} = 0\text{ mA}$	$T_J = 25^{\circ}\text{C}$		6.5	8.5	μA
			$T_J = -40^{\circ}\text{C}$ to 85°C			10	
			$T_J = -40^{\circ}\text{C}$ to 125°C			15	
		$V_{EN} = V_{IN} = 6\text{ V}$, $I_{OUT} = 300\text{ mA}$			2000		
I _{SHDN}	Shutdown ground current	$V_{EN} = 0\text{ V}$ (disabled), $V_{IN} = 6.0\text{ V}$, $T_J = 25^{\circ}\text{C}$			0.07	0.2	μA
I _{GND(DO)}	I _{GND} in dropout	$V_{IN} \leq V_{OUT(NOM)}$, $I_{OUT} = 0\text{ mA}$, $V_{EN} = V_{IN}$			6.5	15	μA
V _{DO}	Dropout voltage	$I_{OUT} = 300\text{ mA}$, $V_{OUT} = 95\% \times V_{OUT(NOM)}$, (DQN, YCJ, YCK packages unless otherwise noted)	$0.8\text{ V} \leq V_{OUT} < 1.0\text{ V}^{(1)}$			690	mV
			$1.0\text{ V} \leq V_{OUT} < 1.2\text{ V}^{(1)}$			490	
			$1.2\text{ V} \leq V_{OUT} < 1.5\text{ V}^{(1)}$			355	
			$1.5\text{ V} \leq V_{OUT} < 2.5\text{ V}$			200	
			$1.5\text{ V} \leq V_{OUT} < 2.5\text{ V}$ (DBV)			205	
			$2.5\text{ V} \leq V_{OUT} < 5.5\text{ V}$			140	
			$2.5\text{ V} \leq V_{OUT} < 5.5\text{ V}$ (DBV)			145	

6.5 Electrical Characteristics (continued)

at operating temperature range ($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$), $V_{IN} = V_{OUT(NOM)} + 0.3\text{ V}$ or 1.6 V , whichever is greater, $V_{EN} = 1.0\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$ (unless otherwise noted); all typical values are at $T_J = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I _{CL}	Output current limit	V _{OUT} = 0.9 x V _{OUT(NOM)} , V _{IN} = V _{OUT(NOM)} + 0.5 V	V _{OUT} < 1.5 V (YCK, YCK packages)	360	520	770	mA
		V _{OUT} = 0.9 x V _{OUT(NOM)} , V _{IN} = V _{OUT(NOM)} + 0.5 V	V _{OUT} < 1.5 V (DQN package)	360	520	730	
		V _{OUT} = V _{OUT(NOM)} - 150 mV, V _{IN} = V _{OUT(NOM)} + 0.5 V	V _{OUT} < 1.5 V (DBV package)	360	520	730	
		V _{OUT} = 0.9 x V _{OUT(NOM)} , V _{IN} = V _{OUT(NOM)} + 0.3 V	V _{OUT} ≥ 1.5 V (YCK, YCK packages)	360	520	770	
		V _{OUT} = 0.9 x V _{OUT(NOM)} , V _{IN} = V _{OUT(NOM)} + 0.3 V	V _{OUT} ≥ 1.5 V (DQN package)	360	520	730	
I _{SC}	Short-circuit current limit	V _{OUT} = 0 V		160			mA
PSRR	Power-supply rejection ratio	I _{OUT} = 20 mA, V _{IN} = V _{OUT} + 1.0 V	f = 100 Hz	95			dB
			f = 1 kHz	95			
			f = 10 kHz	75			
			f = 100 kHz	75			
			f = 1 MHz	45			
		I _{OUT} = 300 mA, V _{IN} = V _{OUT} + 1.0 V	f = 100 Hz	65			
			f = 1 kHz	92			
			f = 10 kHz	75			
			f = 100 kHz	60			
			f = 1 MHz	40			
V _N	Output noise voltage	BW = 10 Hz to 100 kHz, V _{OUT} = 2.8 V	I _{OUT} = 300 mA	7			μV _{RMS}
			I _{OUT} = 1 mA	10			
R _{PULLDOWN}	Output automatic discharge pulldown resistance	V _{EN} < V _{EN(LOW)} (output disabled), V _{IN} = 3.1 V		150			Ω
T _{SD}	Thermal shutdown	T _J rising		165			°C
		T _J falling		140			
V _{EN(LOW)}	Low input threshold	V _{IN} = 1.6 V to 6.0 V, V _{EN} falling until the output is disabled		0.3			V
V _{EN(HI)}	High input threshold	V _{IN} = 1.6 V to 6.0 V V _{EN} rising until the output is enabled		0.9			V
V _{UVLO}	UVLO threshold	V _{IN} rising (YCKJ and YCK packages)		1.11	1.35	1.59	V
		V _{IN} rising (DBV and DQN packages)		1.17	1.35	1.59	
		V _{IN} falling (YCKJ and YCK packages)		1.05	1.3	1.55	
		V _{IN} falling (DBV and DQN packages)		1.11	1.3	1.55	
V _{UVLO(HYST)}	UVLO hysteresis			50			mV
I _{EN}	EN input leakage current	V _{EN} = 6.0 V and V _{IN} = 6.0 V		90 250			nA
R _{EN(PULL-DOWN)}	Smart enable pulldown resistor	V _{EN} = 0.25 V		500			KΩ

(1) Design simulation data only

6.6 Switching Characteristics

at operating temperature range ($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$), $V_{IN} = V_{OUT(NOM)} + 0.3\text{ V}$ or 1.6 V , whichever is greater, $V_{EN} = 1.0\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$ (unless otherwise noted); all typical values are at $T_J = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
tSTR	Start-up time	From VEN > VEN(HI) to VOUT = 95% of VOUT(NOM),		750	1150	μs

6.7 Typical Characteristics

$V_{IN} = V_{OUT(NOM)} + 0.3 \text{ V}$ or 1.6 V (whichever is greater), $V_{OUT} = 2.8 \text{ V}$, $I_{OUT} = 1 \text{ mA}$, $C_{IN} = 1 \mu\text{F}$, $C_{OUT} = 1 \mu\text{F}$, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

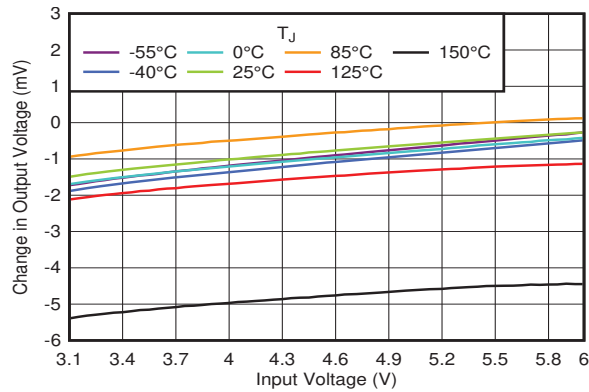


Figure 6-1. Line Regulation vs V_{IN}

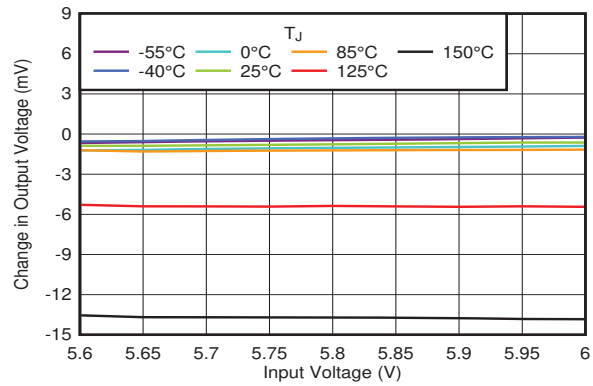


Figure 6-2. Line Regulation vs V_{IN}

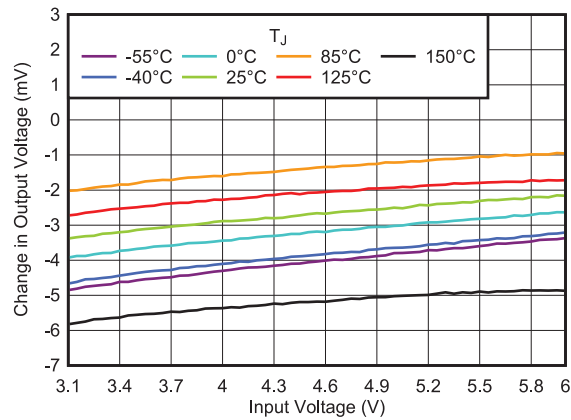


Figure 6-3. Line Regulation vs V_{IN}

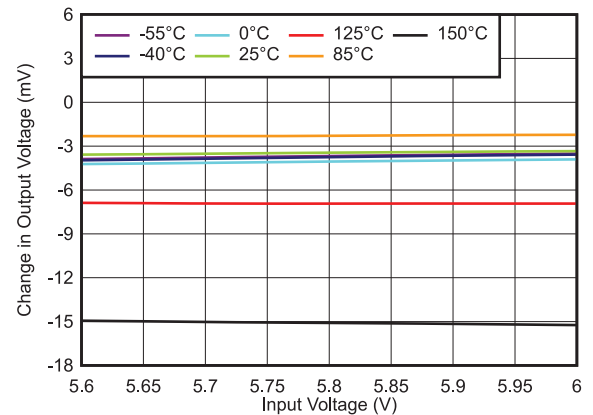


Figure 6-4. Line Regulation vs V_{IN}

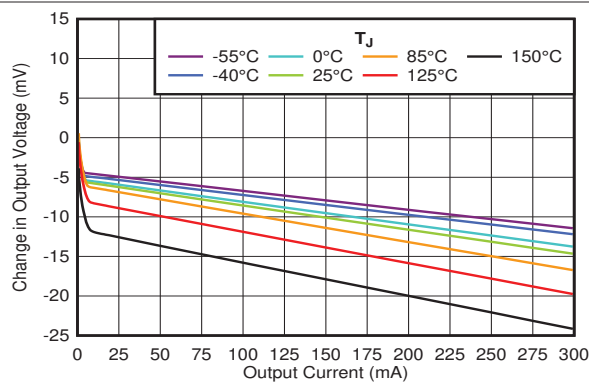


Figure 6-5. Load Regulation vs I_{OUT}

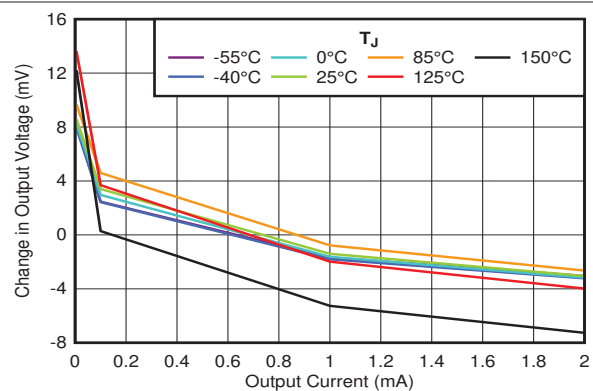


Figure 6-6. Load Regulation vs I_{OUT}

6.7 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.3 \text{ V}$ or 1.6 V (whichever is greater), $V_{OUT} = 2.8 \text{ V}$, $I_{OUT} = 1 \text{ mA}$, $C_{IN} = 1 \mu\text{F}$, $C_{OUT} = 1 \mu\text{F}$, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

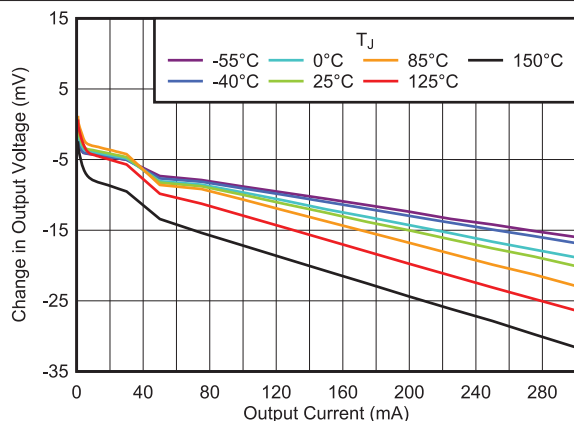


Figure 6-7. Load Regulation vs I_{OUT}
 $V_{IN} = 2.8 \text{ V}$, $V_{EN} = 1 \text{ V}$, DBV package

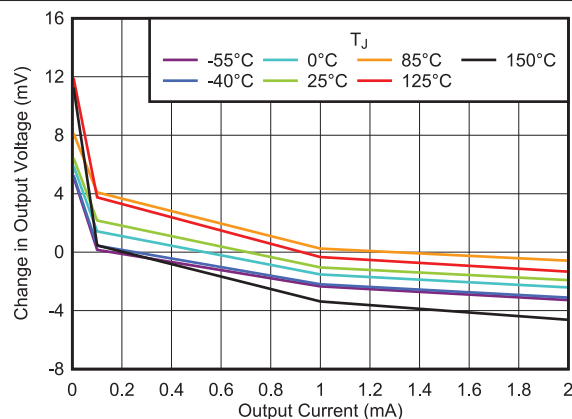


Figure 6-8. Load Regulation vs I_{OUT}
 $V_{IN} = 2.8 \text{ V}$, $V_{EN} = 1 \text{ V}$, DBV package

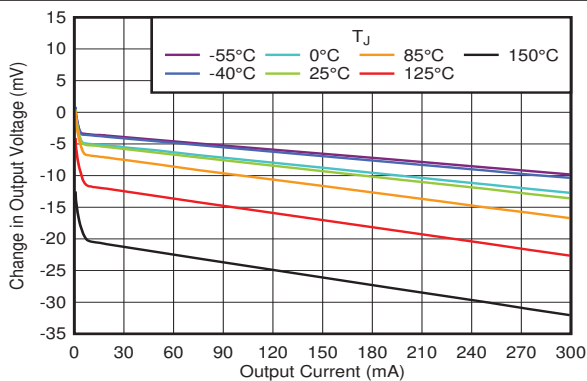


Figure 6-9. Load Regulation vs I_{OUT}
 $V_{OUT} = 5.5 \text{ V}$, $V_{EN} = 1 \text{ V}$, DQN, YCJ, and YCK packages

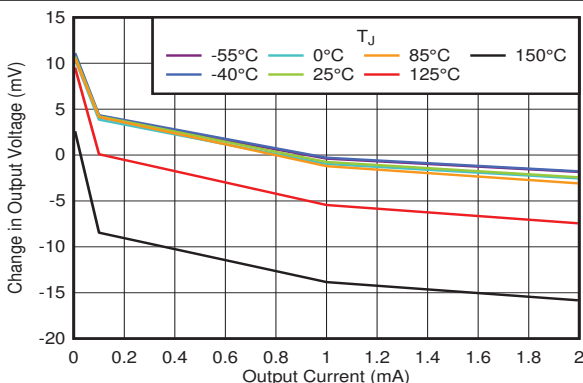


Figure 6-10. Load Regulation vs I_{OUT}
 $V_{OUT} = 5.5 \text{ V}$, $V_{EN} = 1 \text{ V}$, DQN, YCJ, and YCK packages

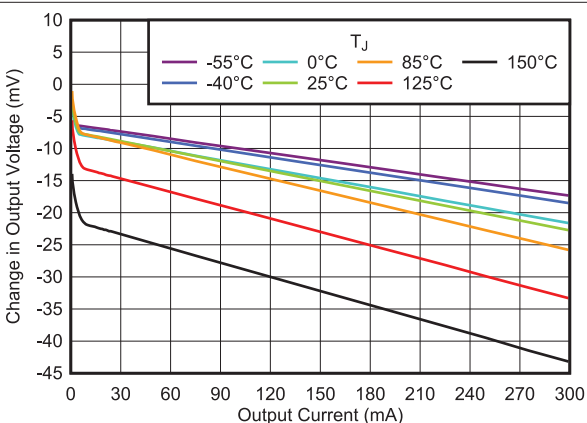


Figure 6-11. Load Regulation vs I_{OUT}
 $V_{OUT} = 5.5 \text{ V}$, $V_{EN} = 1 \text{ V}$, DBV package

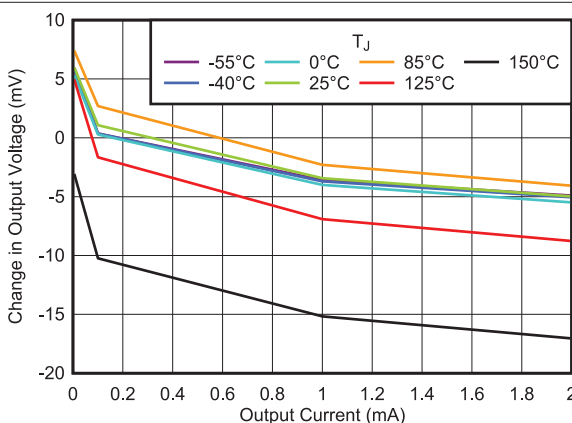


Figure 6-12. Load Regulation vs I_{OUT}
 $V_{OUT} = 5.5 \text{ V}$, $V_{EN} = 1 \text{ V}$, DBV package

6.7 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.3 \text{ V}$ or 1.6 V (whichever is greater), $V_{OUT} = 2.8 \text{ V}$, $I_{OUT} = 1 \text{ mA}$, $C_{IN} = 1 \mu\text{F}$, $C_{OUT} = 1 \mu\text{F}$, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

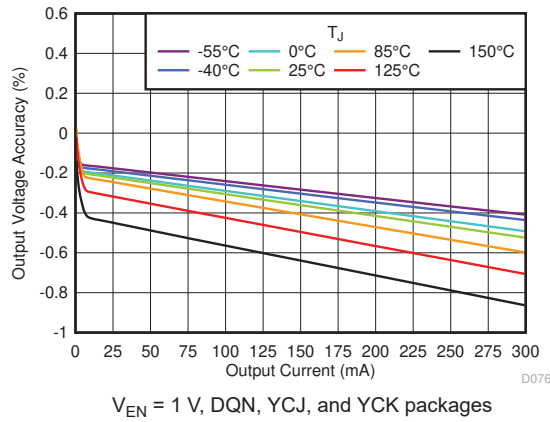


Figure 6-13. Output Voltage Accuracy vs I_{OUT}

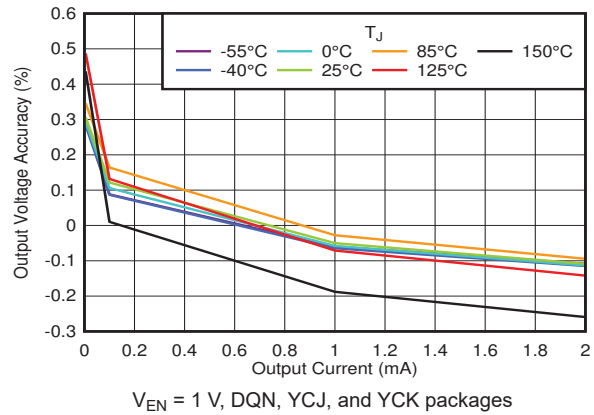


Figure 6-14. Output Voltage Accuracy vs I_{OUT}

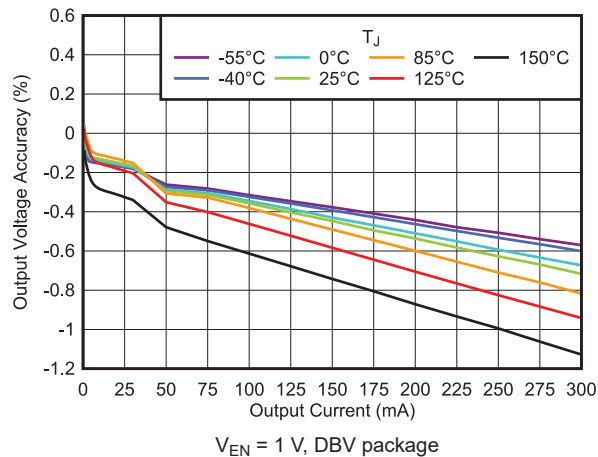


Figure 6-15. Output Voltage Accuracy vs I_{OUT}

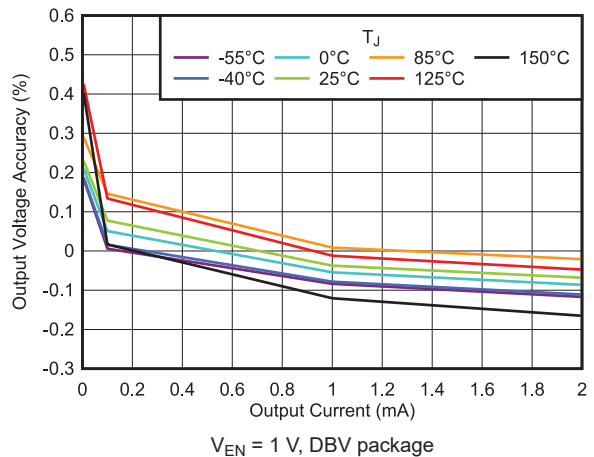


Figure 6-16. Output Voltage Accuracy vs I_{OUT}

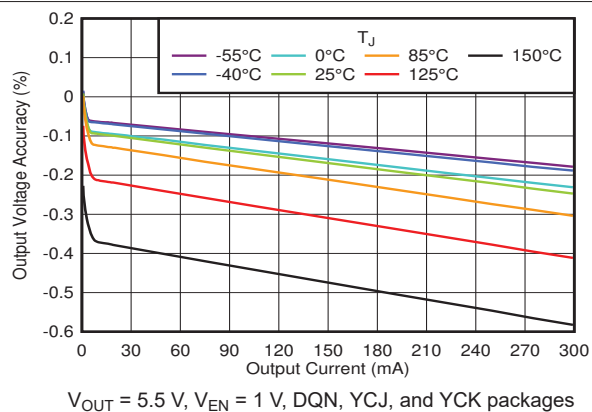


Figure 6-17. Output Voltage Accuracy vs I_{OUT}

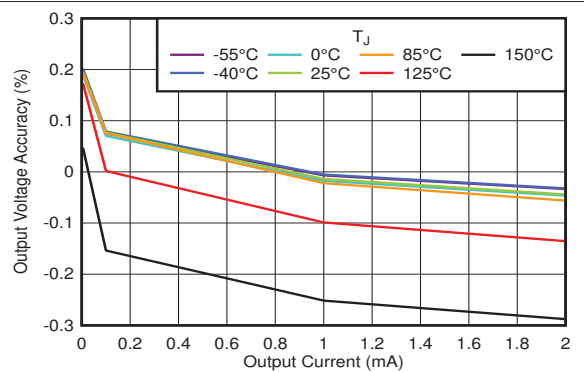
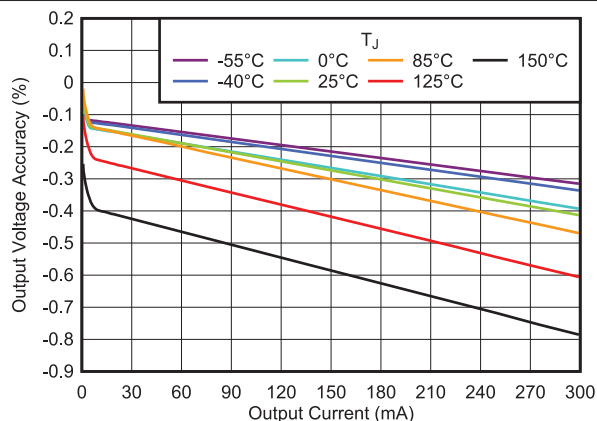


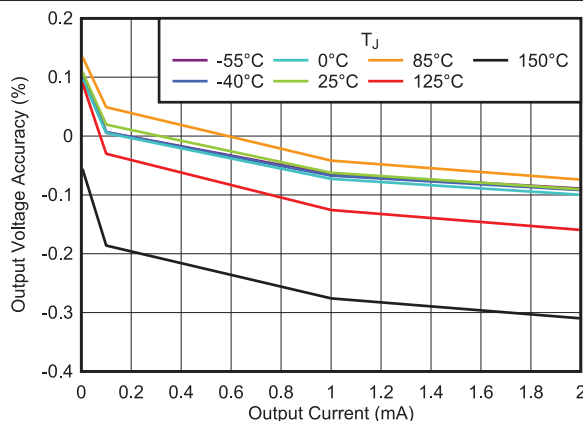
Figure 6-18. Output Voltage Accuracy vs I_{OUT}

6.7 Typical Characteristics (continued)

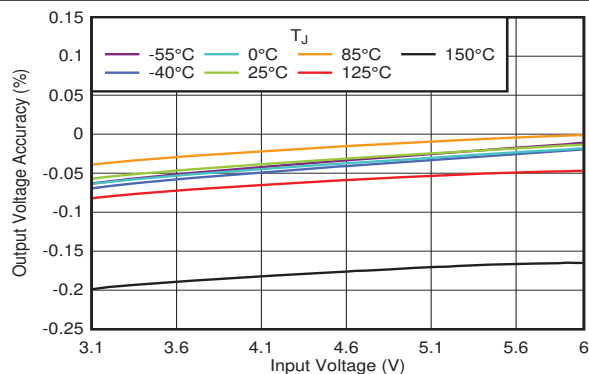
$V_{IN} = V_{OUT(NOM)} + 0.3 \text{ V}$ or 1.6 V (whichever is greater), $V_{OUT} = 2.8 \text{ V}$, $I_{OUT} = 1 \text{ mA}$, $C_{IN} = 1 \mu\text{F}$, $C_{OUT} = 1 \mu\text{F}$, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)



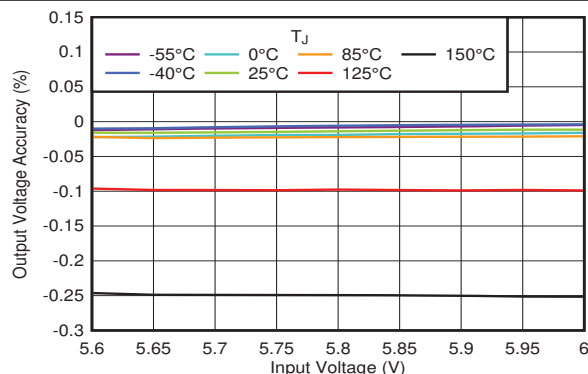
$V_{OUT} = 5.5 \text{ V}$, $V_{EN} = 1 \text{ V}$, DBV package
Figure 6-19. Output Voltage Accuracy vs I_{OUT}



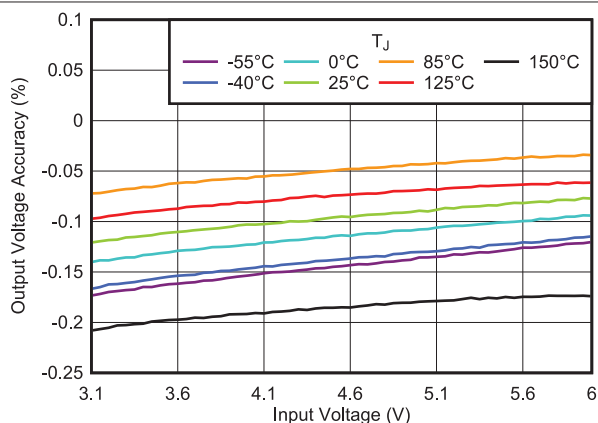
$V_{OUT} = 5.5 \text{ V}$, $V_{EN} = 1 \text{ V}$, DBV package
Figure 6-20. Output Voltage Accuracy vs I_{OUT}



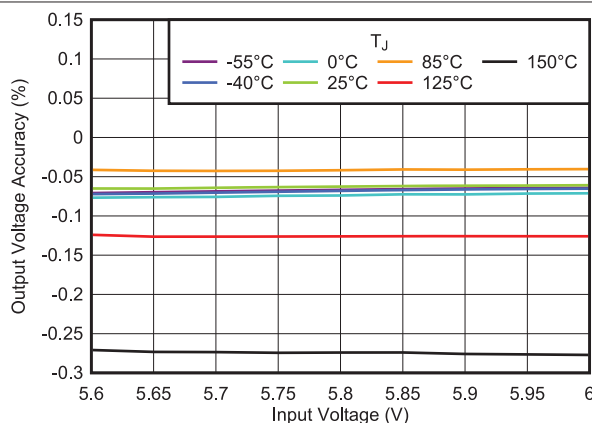
$V_{EN} = 1 \text{ V}$, $I_{OUT} = 1 \text{ mA}$, DQN, YCJ, and YCK packages
Figure 6-21. Output Voltage Accuracy vs V_{IN}



$V_{OUT} = 5.5 \text{ V}$, $V_{EN} = 1 \text{ V}$, DQN, YCJ, and YCK packages
Figure 6-22. Output Voltage Accuracy vs V_{IN}



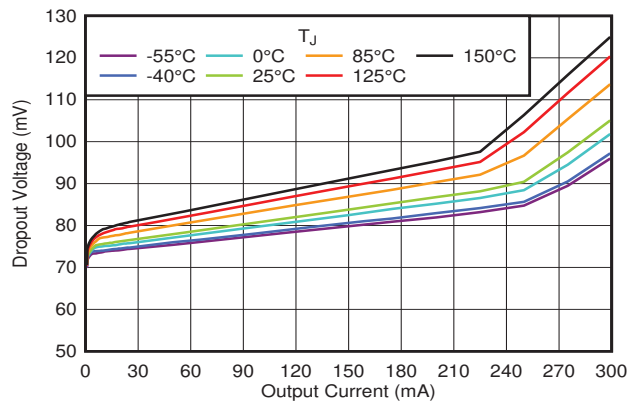
$V_{EN} = 1 \text{ V}$, $I_{OUT} = 1 \text{ mA}$, DBV package
Figure 6-23. Output Voltage Accuracy vs V_{IN}



$V_{OUT} = 5.5 \text{ V}$, $V_{EN} = 1 \text{ V}$, DBV package
Figure 6-24. Output Voltage Accuracy vs V_{IN}

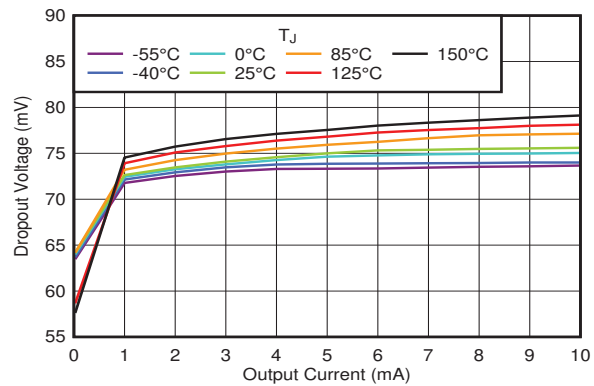
6.7 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.3 \text{ V}$ or 1.6 V (whichever is greater), $V_{OUT} = 2.8 \text{ V}$, $I_{OUT} = 1 \text{ mA}$, $C_{IN} = 1 \mu\text{F}$, $C_{OUT} = 1 \mu\text{F}$, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)



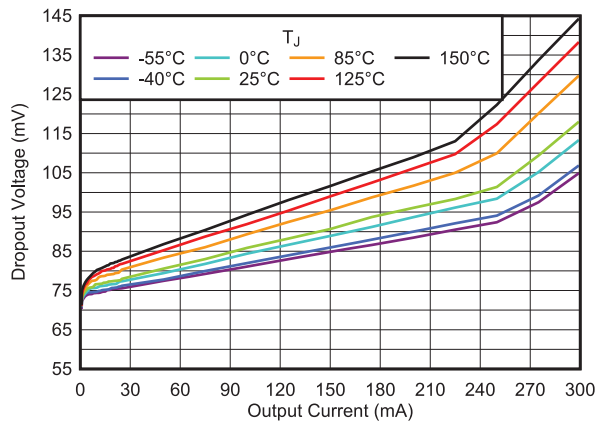
$V_{EN} = 1 \text{ V}$, DQN, YCJ, and YCK packages

Figure 6-25. Dropout Voltage vs I_{OUT}



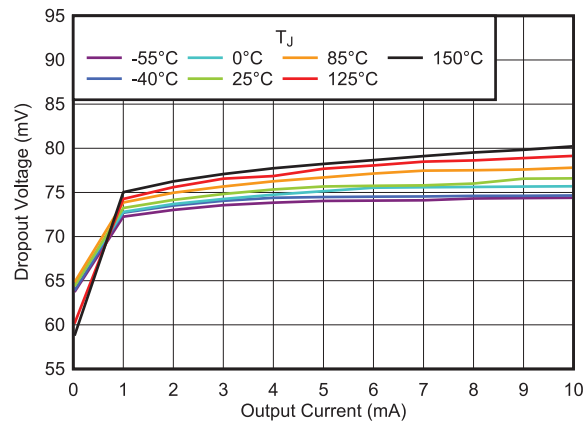
$V_{EN} = 1 \text{ V}$, DQN, YCJ, and YCK packages

Figure 6-26. Dropout Voltage vs I_{OUT}



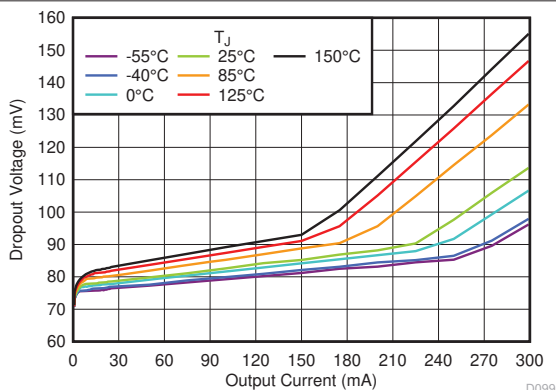
$V_{EN} = 1 \text{ V}$, DBV package

Figure 6-27. Dropout Voltage vs I_{OUT}



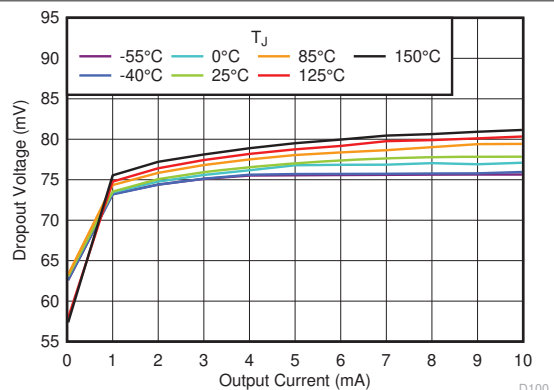
$V_{EN} = 1 \text{ V}$, DBV package

Figure 6-28. Dropout Voltage vs I_{OUT}



$V_{OUT} = 1.8 \text{ V}$, $V_{EN} = 1 \text{ V}$, DQN, YCJ, and YCK packages

Figure 6-29. Dropout Voltage vs I_{OUT}



$V_{OUT} = 1.8 \text{ V}$, $V_{EN} = 1 \text{ V}$, DQN, YCJ, and YCK packages

Figure 6-30. Dropout Voltage vs I_{OUT}

6.7 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.3 \text{ V}$ or 1.6 V (whichever is greater), $V_{OUT} = 2.8 \text{ V}$, $I_{OUT} = 1 \text{ mA}$, $C_{IN} = 1 \mu\text{F}$, $C_{OUT} = 1 \mu\text{F}$, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

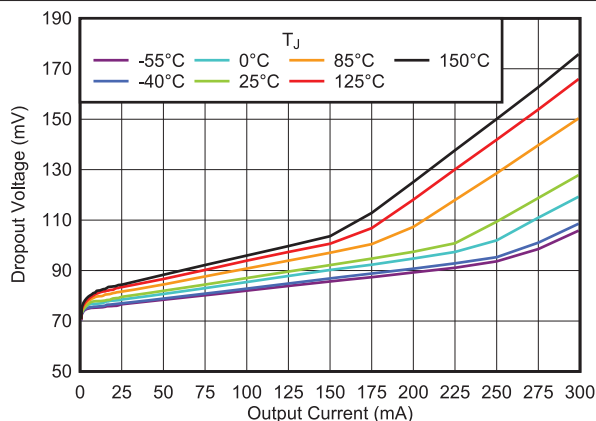


Figure 6-31. Dropout Voltage vs I_{OUT}

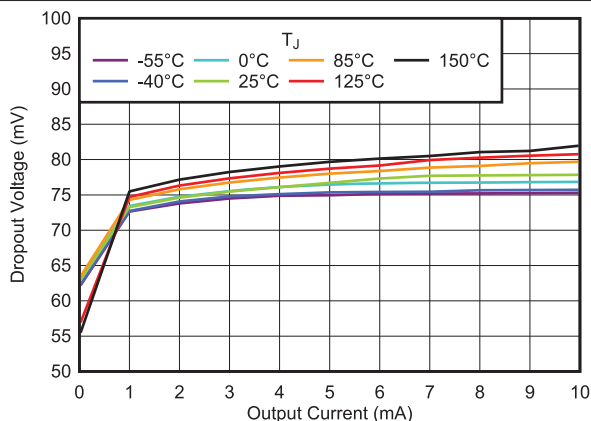


Figure 6-32. Dropout Voltage vs I_{OUT}

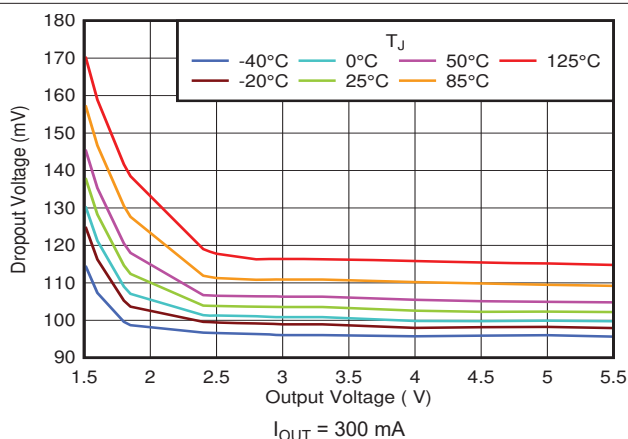


Figure 6-33. Dropout Voltage vs V_{OUT}

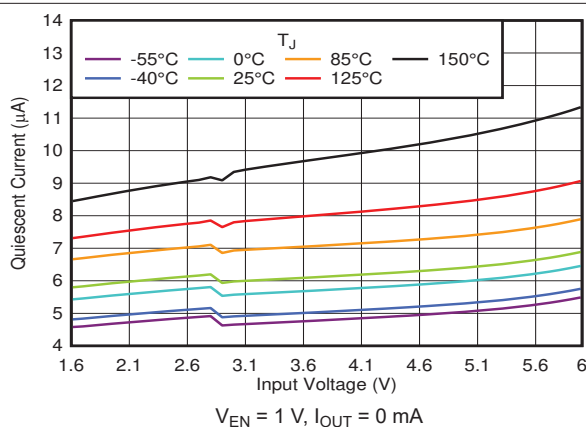


Figure 6-34. I_{GND} vs V_{IN}

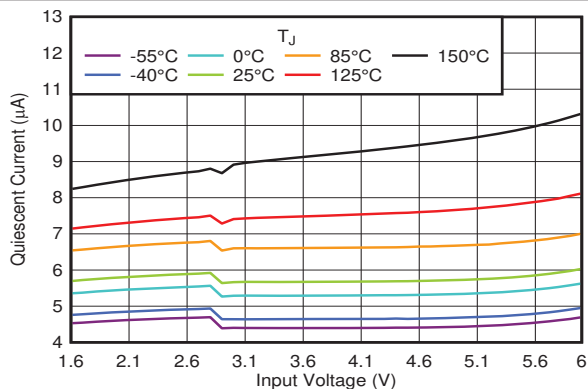


Figure 6-35. I_{GND} vs V_{IN}

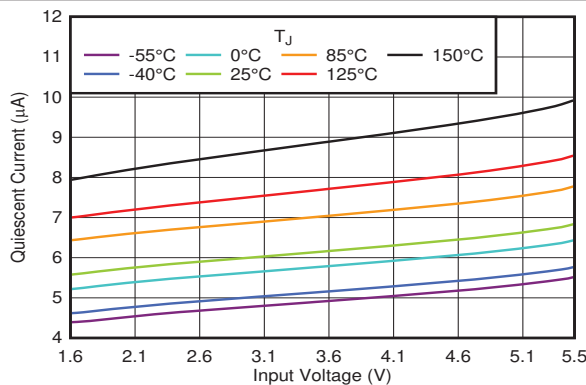


Figure 6-36. I_{GND} vs V_{IN} in the Dropout Region

6.7 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.3 \text{ V}$ or 1.6 V (whichever is greater), $V_{OUT} = 2.8 \text{ V}$, $I_{OUT} = 1 \text{ mA}$, $C_{IN} = 1 \mu\text{F}$, $C_{OUT} = 1 \mu\text{F}$, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

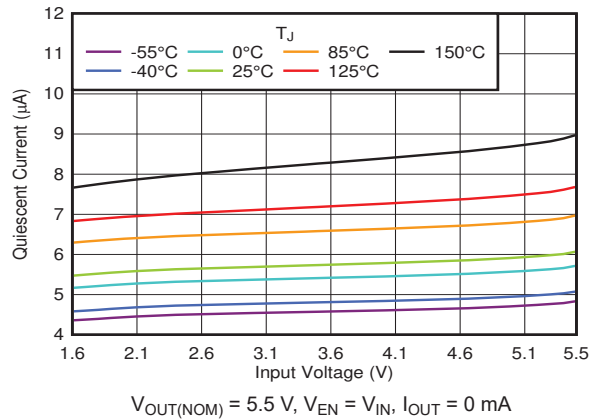


Figure 6-37. I_{GND} vs V_{IN} in the Dropout Region

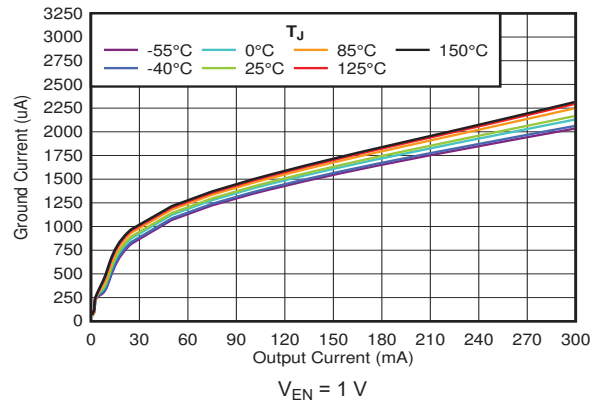


Figure 6-38. I_{GND} vs I_{OUT}

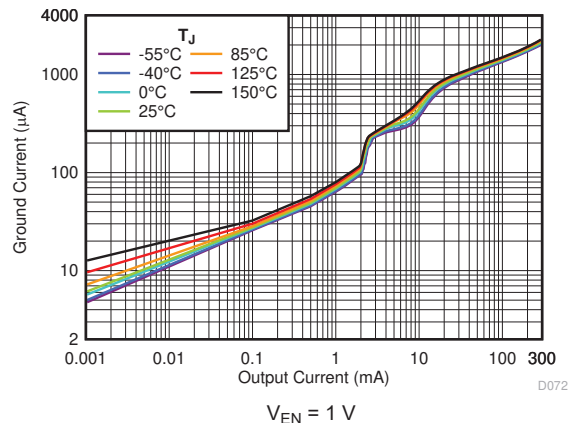


Figure 6-39. I_{GND} vs I_{OUT}

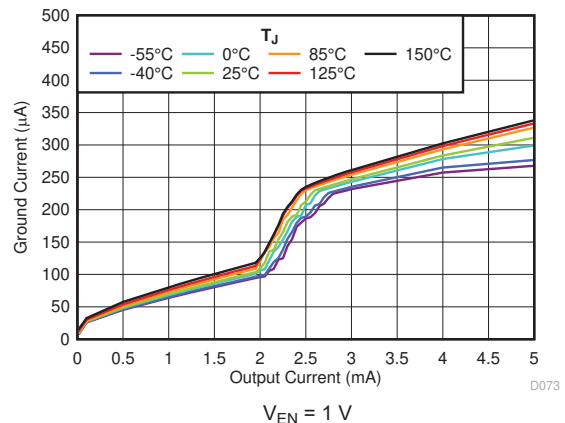


Figure 6-40. I_{GND} vs I_{OUT}

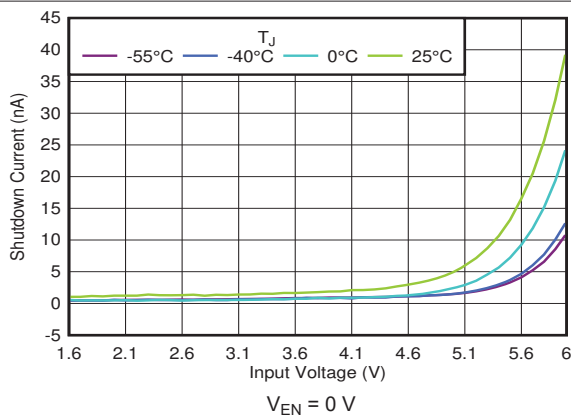


Figure 6-41. Shutdown Current vs V_{IN}

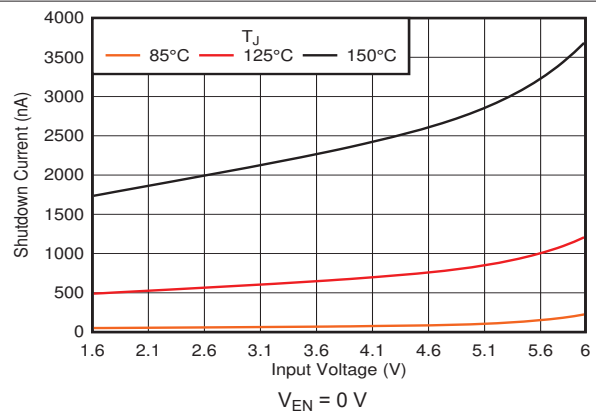
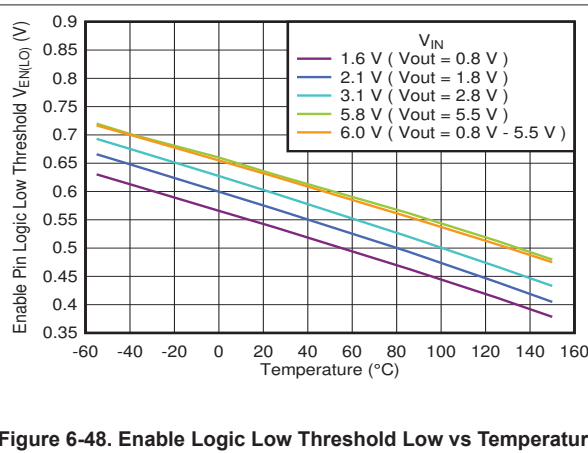
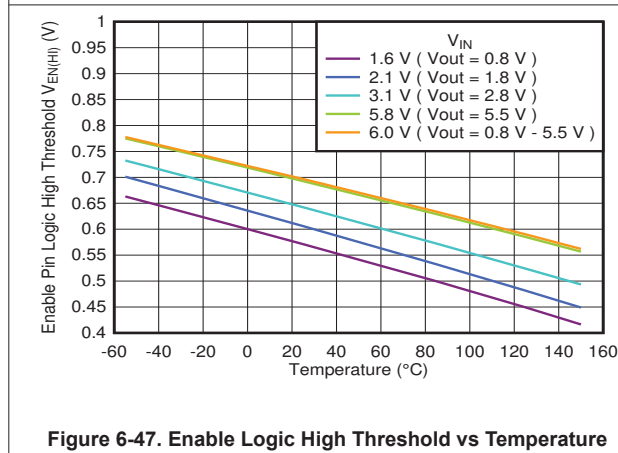
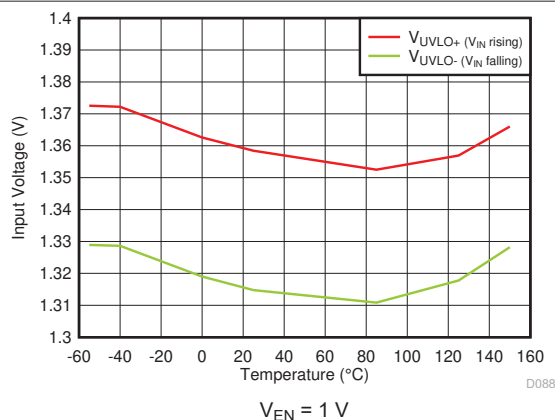
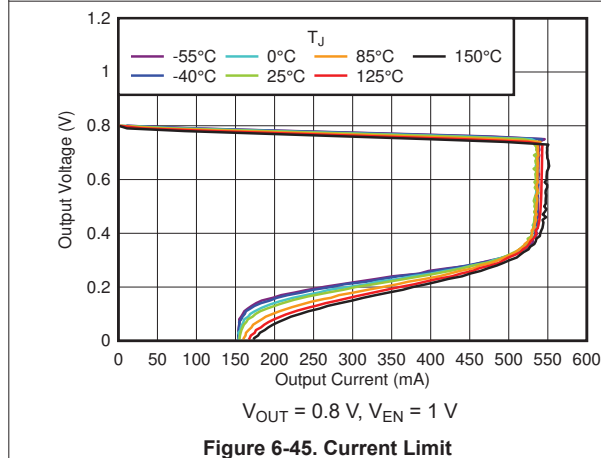
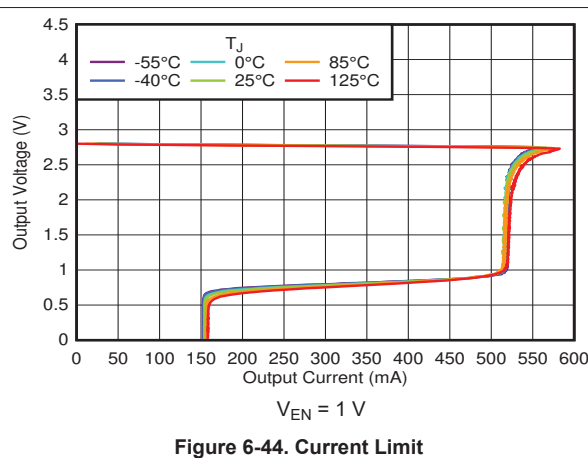
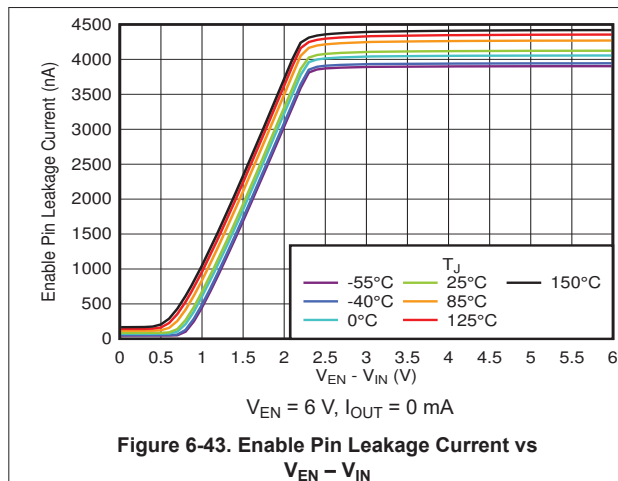


Figure 6-42. Shutdown Current vs V_{IN}

6.7 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.3\text{ V}$ or 1.6 V (whichever is greater), $V_{OUT} = 2.8\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)



6.7 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.3 \text{ V}$ or 1.6 V (whichever is greater), $V_{OUT} = 2.8 \text{ V}$, $I_{OUT} = 1 \text{ mA}$, $C_{IN} = 1 \mu\text{F}$, $C_{OUT} = 1 \mu\text{F}$, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

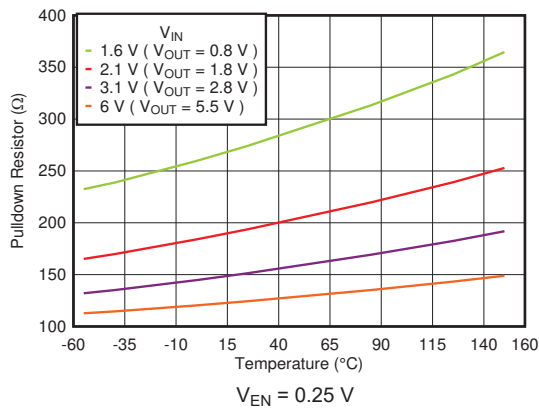


Figure 6-49. Output Pulldown Resistor vs Temperature

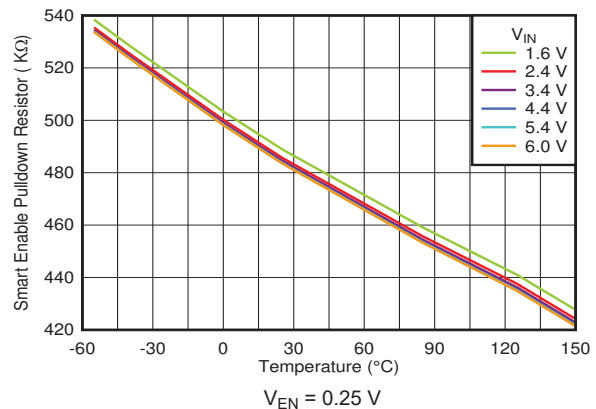
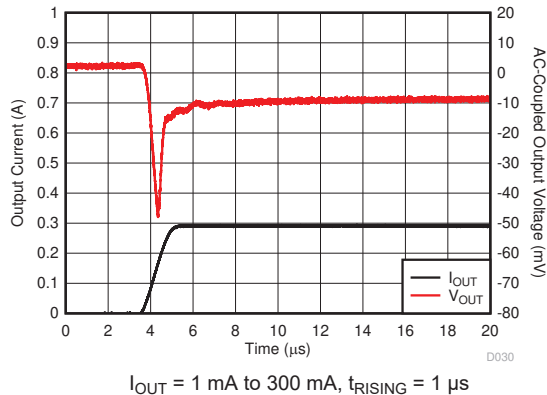
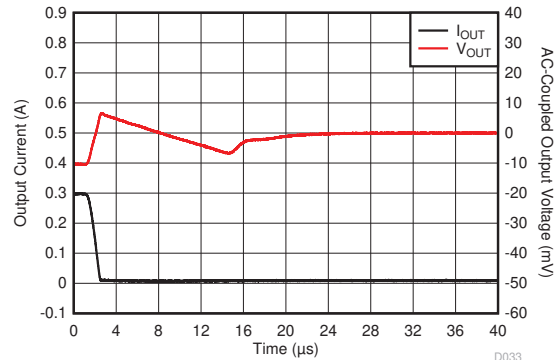


Figure 6-50. Smart Enable Pulldown Resistor vs Temperature and V_{IN}



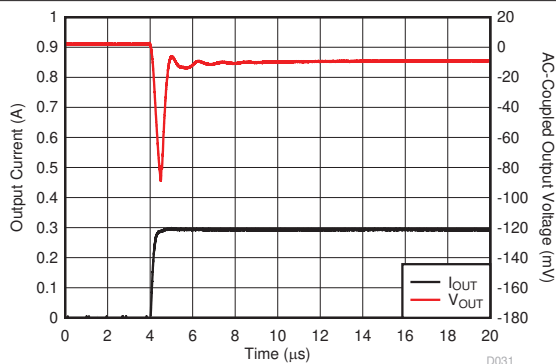
$I_{OUT} = 1 \text{ mA to } 300 \text{ mA}$, $t_{RISING} = 1 \mu\text{s}$

Figure 6-51. Load Transient



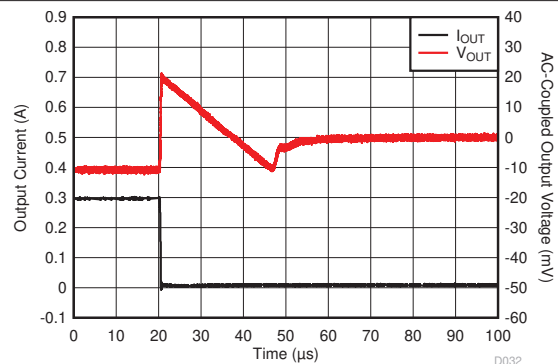
$I_{OUT} = 300 \text{ mA to } 1 \text{ mA}$, $t_{FALLING} = 1 \mu\text{s}$

Figure 6-52. Load Transient



$I_{OUT} = 1 \text{ mA to } 300 \text{ mA}$, $t_{RISING} = 200 \text{ ns}$

Figure 6-53. Load Transient



$I_{OUT} = 300 \text{ mA to } 1 \text{ mA}$, $t_{FALLING} = 200 \text{ ns}$

Figure 6-54. Load Transient

6.7 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.3 \text{ V}$ or 1.6 V (whichever is greater), $V_{OUT} = 2.8 \text{ V}$, $I_{OUT} = 1 \text{ mA}$, $C_{IN} = 1 \mu\text{F}$, $C_{OUT} = 1 \mu\text{F}$, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

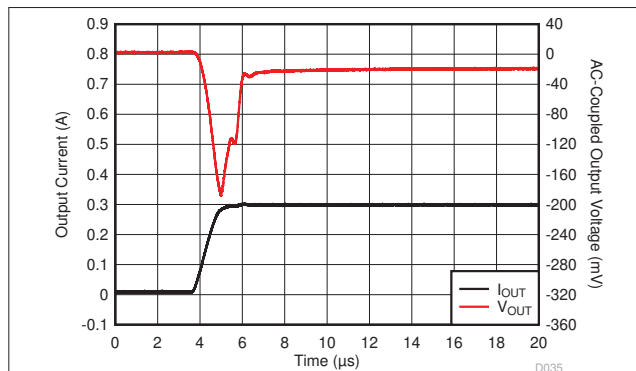


Figure 6-55. Load Transient

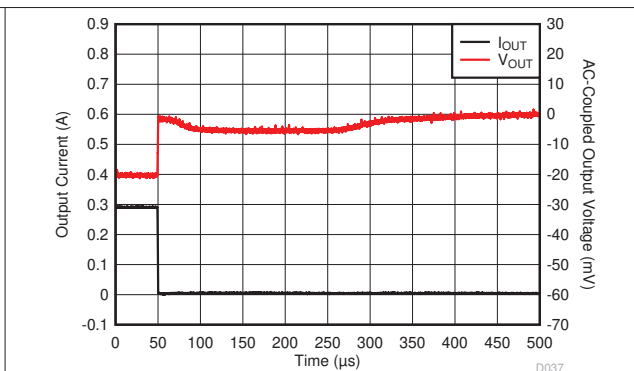


Figure 6-56. Load Transient

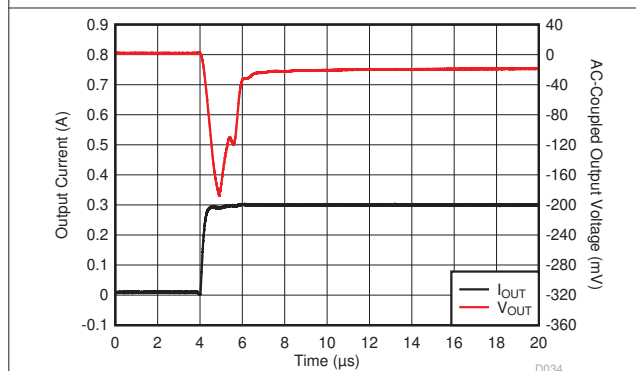


Figure 6-57. Load Transient

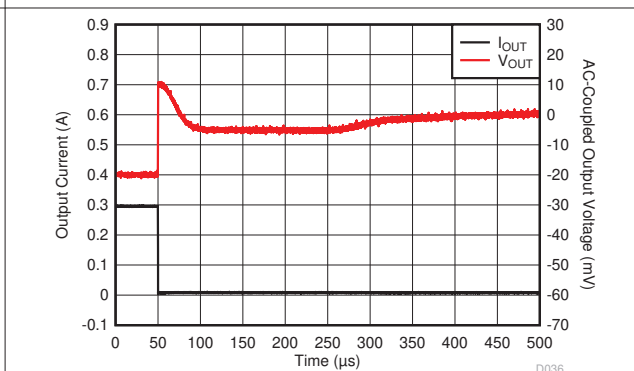


Figure 6-58. Load Transient

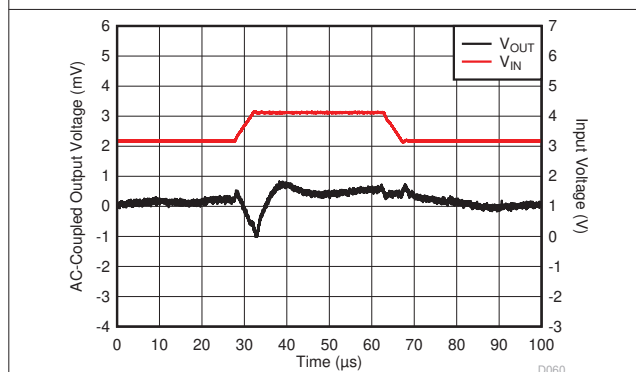


Figure 6-59. Line Transient

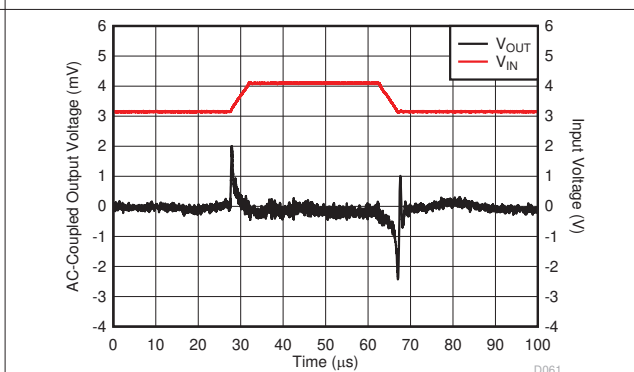


Figure 6-60. Line Transient

6.7 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.3 \text{ V}$ or 1.6 V (whichever is greater), $V_{OUT} = 2.8 \text{ V}$, $I_{OUT} = 1 \text{ mA}$, $C_{IN} = 1 \mu\text{F}$, $C_{OUT} = 1 \mu\text{F}$, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

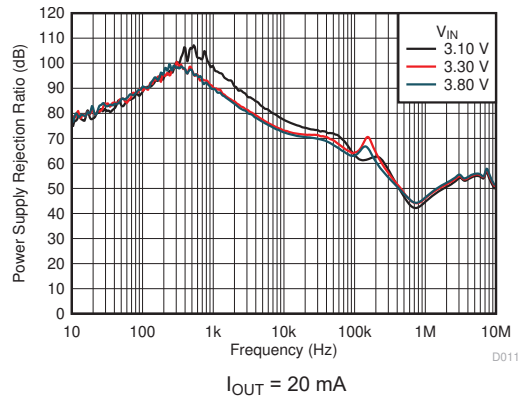


Figure 6-61. PSRR vs V_{IN} vs Frequency and V_{IN}

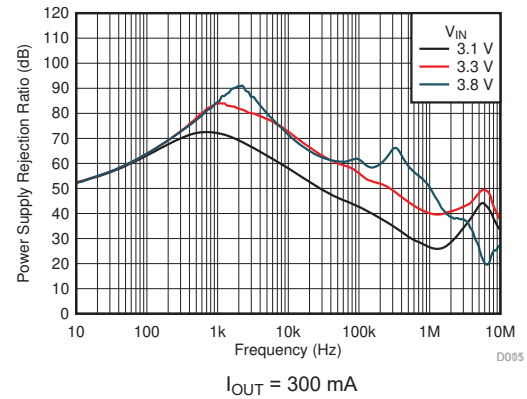


Figure 6-62. PSRR vs Frequency and V_{IN}

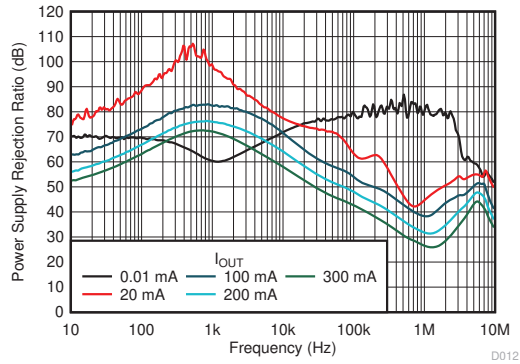


Figure 6-63. PSRR vs Frequency and I_{OUT}

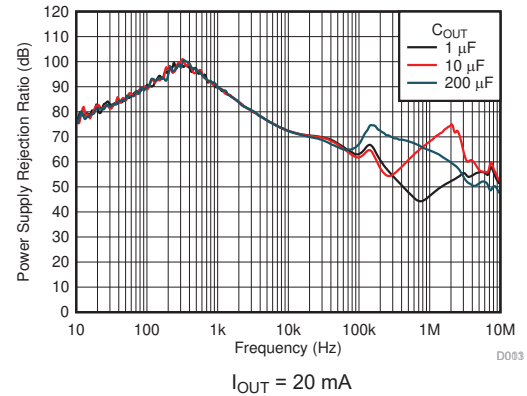


Figure 6-64. PSRR vs Frequency and C_{OUT}

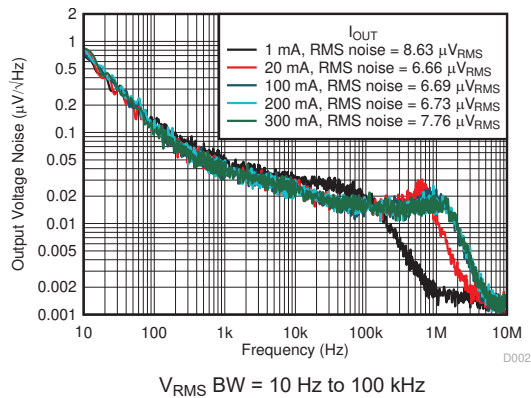


Figure 6-65. Noise vs Frequency and I_{OUT}

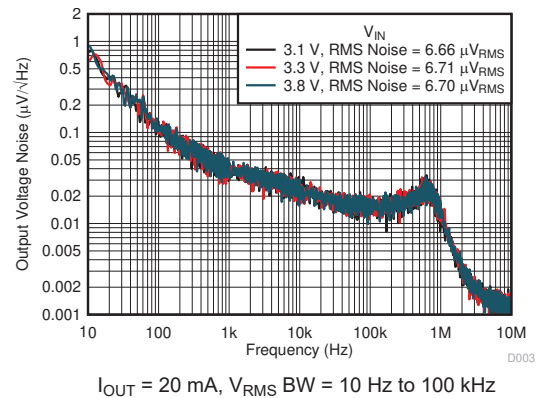
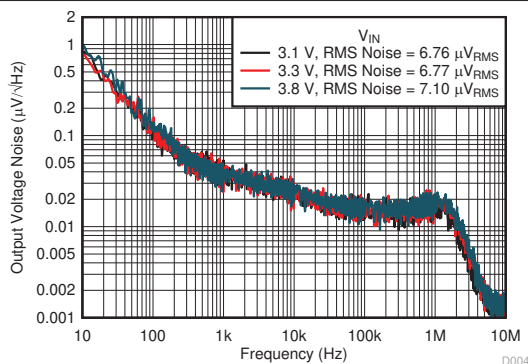


Figure 6-66. Noise vs Frequency and V_{IN}

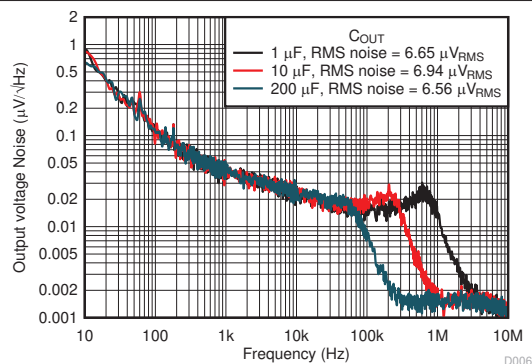
6.7 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.3 \text{ V}$ or 1.6 V (whichever is greater), $V_{OUT} = 2.8 \text{ V}$, $I_{OUT} = 1 \text{ mA}$, $C_{IN} = 1 \mu\text{F}$, $C_{OUT} = 1 \mu\text{F}$, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)



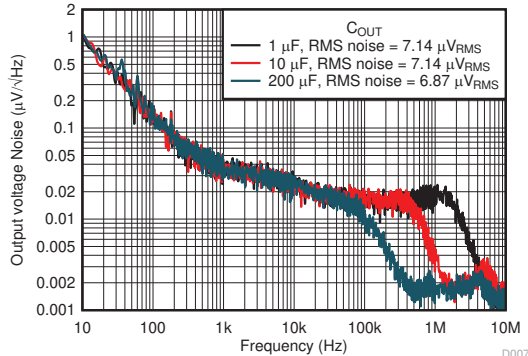
$I_{OUT} = 300 \text{ mA}$, $V_{RMS} \text{ BW} = 10 \text{ Hz to } 100 \text{ kHz}$

Figure 6-67. Noise vs Frequency and V_{IN}



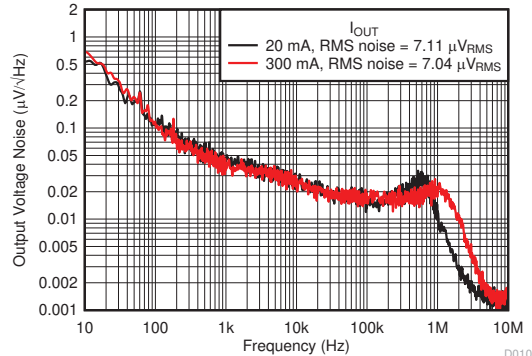
$V_{IN} = 3.8 \text{ V}$, $I_{OUT} = 20 \text{ mA}$, $V_{RMS} \text{ BW} = 10 \text{ Hz to } 100 \text{ kHz}$

Figure 6-68. Noise vs Frequency and C_{OUT}



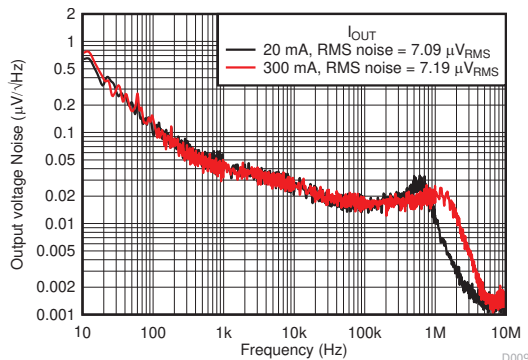
$V_{IN} = 3.8 \text{ V}$, $I_{OUT} = 300 \text{ mA}$, $V_{RMS} \text{ BW} = 10 \text{ Hz to } 100 \text{ kHz}$

Figure 6-69. Noise vs Frequency and C_{OUT}



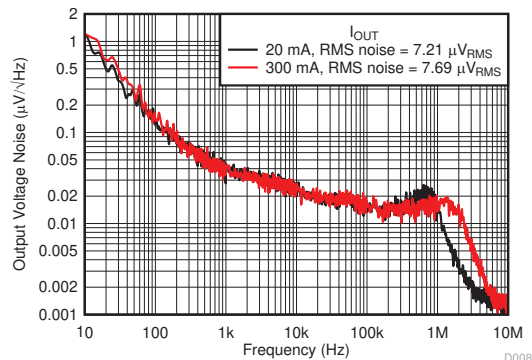
$V_{OUT} = 0.8 \text{ V}$, $V_{RMS} \text{ BW} = 10 \text{ Hz to } 100 \text{ kHz}$

Figure 6-70. Noise vs Frequency and I_{OUT}



$V_{OUT} = 0.8 \text{ V}$, $V_{IN} = 1.8 \text{ V}$, $V_{RMS} \text{ BW} = 10 \text{ Hz to } 100 \text{ kHz}$

Figure 6-71. Noise vs Frequency and I_{OUT}

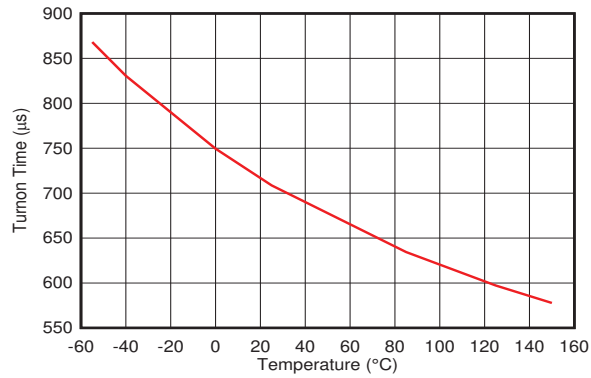


$V_{OUT} = 5.5 \text{ V}$, $V_{IN} = 6 \text{ V}$, $V_{RMS} \text{ BW} = 10 \text{ Hz to } 100 \text{ kHz}$

Figure 6-72. Noise vs Frequency and I_{OUT}

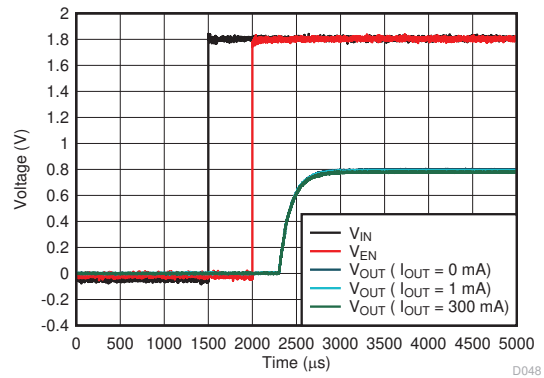
6.7 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.3 \text{ V}$ or 1.6 V (whichever is greater), $V_{OUT} = 2.8 \text{ V}$, $I_{OUT} = 1 \text{ mA}$, $C_{IN} = 1 \mu\text{F}$, $C_{OUT} = 1 \mu\text{F}$, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)



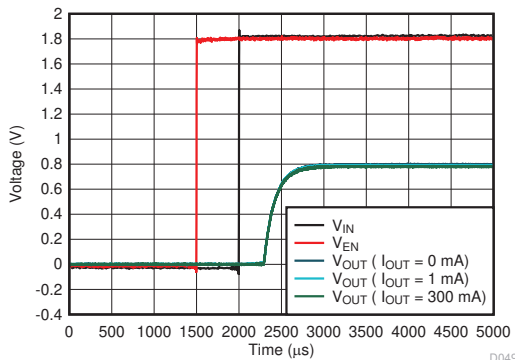
From $V_{EN} = V_{EN(HI)}$ to $V_{OUT} = 95\%$ of $V_{OUT(NOM)}$, $I_{OUT} = 0 \text{ mA}$

Figure 6-73. Start-Up Turn-On Time



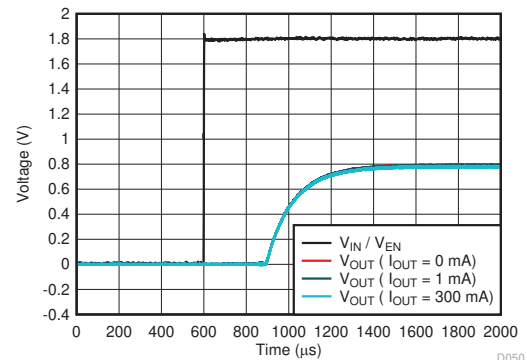
$V_{OUT} = 0.8 \text{ V}$, $V_{IN} = 0 \text{ V}$ to 1.8 V , $V_{EN} = 0 \text{ V}$ to 1.8 V , V_{EN} rises $500 \mu\text{s}$ behind V_{IN} , V_{IN} and V_{EN} slew rate = $1 \text{ V}/\mu\text{s}$

Figure 6-74. Start-Up



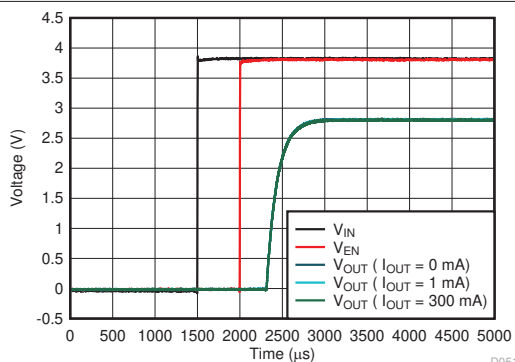
$V_{OUT} = 0.8 \text{ V}$, $V_{IN} = 0 \text{ V}$ to 1.8 V , $V_{EN} = 0 \text{ V}$ to 1.8 V , V_{EN} rises $500 \mu\text{s}$ ahead of V_{IN} , V_{IN} and V_{EN} slew rate = $1 \text{ V}/\mu\text{s}$

Figure 6-75. Start-Up



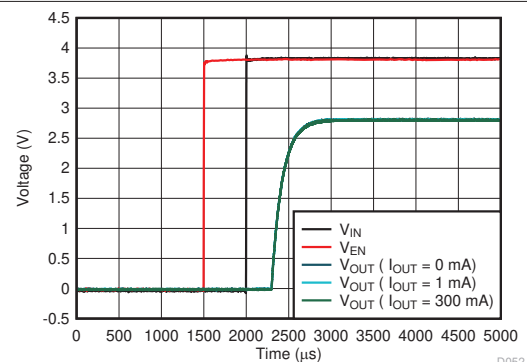
$V_{OUT} = 0.8 \text{ V}$, $V_{IN} = 0 \text{ V}$ to 1.8 V , $V_{EN} = V_{IN}$, V_{IN} slew rate = $1 \text{ V}/\mu\text{s}$

Figure 6-76. Start-Up



$V_{IN} = 0 \text{ V}$ to 3.8 V , $V_{EN} = 0 \text{ V}$ to 3.8 V , V_{EN} rises $500 \mu\text{s}$ behind V_{IN} , V_{IN} and V_{EN} slew rate = $1 \text{ V}/\mu\text{s}$

Figure 6-77. Start-Up

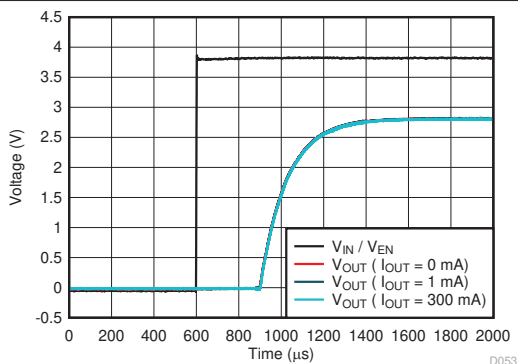


$V_{IN} = 0 \text{ V}$ to 3.8 V , $V_{EN} = 0 \text{ V}$ to 3.8 V , V_{EN} rises $500 \mu\text{s}$ ahead of V_{IN} , V_{IN} and V_{EN} slew rate = $1 \text{ V}/\mu\text{s}$

Figure 6-78. Start-Up

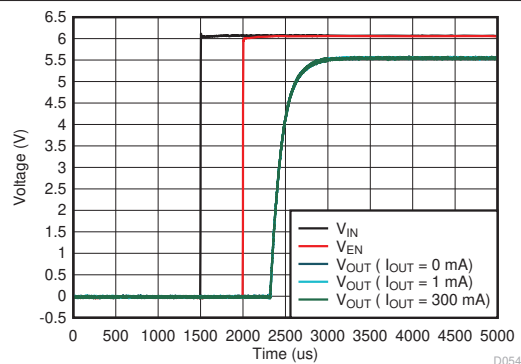
6.7 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.3\text{ V}$ or 1.6 V (whichever is greater), $V_{OUT} = 2.8\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)



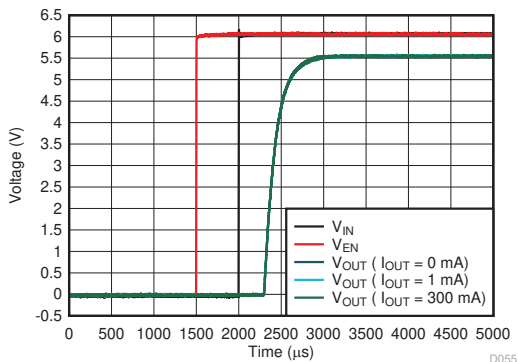
$V_{IN} = 0\text{ V}$ to 3.8 V , $V_{EN} = 0\text{ V}$ to 3.8 V , $V_{EN} = V_{IN}$, V_{IN} and slew rate = $1\text{ V}/\mu\text{s}$

Figure 6-79. Start-Up



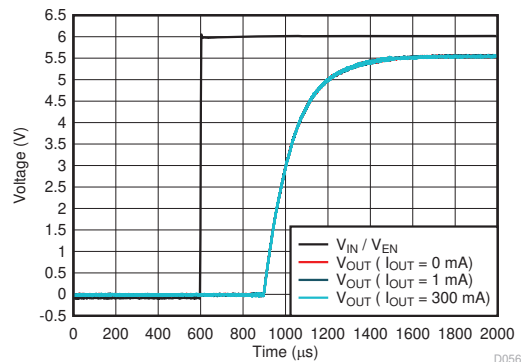
$V_{OUT} = 5.5\text{ V}$, $V_{IN} = 0\text{ V}$ to 6.0 V , $V_{EN} = 0\text{ V}$ to 6.0 V , V_{EN} rises $500\text{ }\mu\text{s}$ behind V_{IN} , V_{IN} and V_{EN} slew rate = $1\text{ V}/\mu\text{s}$

Figure 6-80. Start-Up



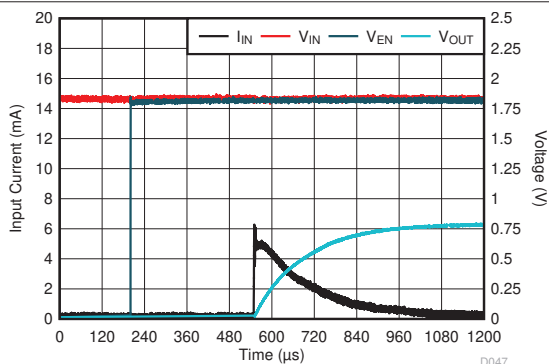
$V_{OUT} = 5.5\text{ V}$, $V_{IN} = 0\text{ V}$ to 6.0 V , $V_{EN} = 0\text{ V}$ to 6.0 V , V_{EN} rises $500\text{ }\mu\text{s}$ ahead of V_{IN} , V_{IN} and V_{EN} slew rate = $1\text{ V}/\mu\text{s}$

Figure 6-81. Start-Up



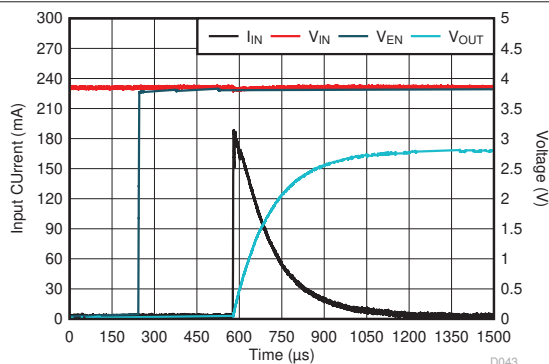
$V_{OUT} = 5.5\text{ V}$, $V_{IN} = 0\text{ V}$ to 6 V , $V_{EN} = V_{IN}$, V_{IN} slew rate = $1\text{ V}/\mu\text{s}$

Figure 6-82. Start-Up



$V_{OUT} = 0.8\text{ V}$, $V_{IN} = 1.8\text{ V}$, $V_{EN} = 0\text{ V}$ to 1.8 V , V_{EN} slew rate = $1\text{ V}/\mu\text{s}$, $C_{OUT} = 10\text{ }\mu\text{F}$

Figure 6-83. Inrush Current

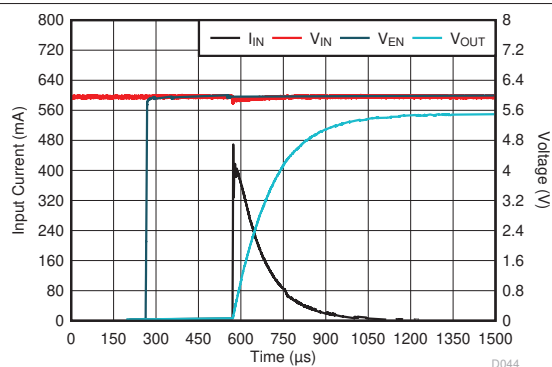


$V_{IN} = 3.8\text{ V}$, $V_{EN} = 0\text{ V}$ to 3.8 V , V_{EN} slew rate = $1\text{ V}/\mu\text{s}$, $C_{OUT} = 10\text{ }\mu\text{F}$

Figure 6-84. Inrush Current

6.7 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.3 \text{ V}$ or 1.6 V (whichever is greater), $V_{OUT} = 2.8 \text{ V}$, $I_{OUT} = 1 \text{ mA}$, $C_{IN} = 1 \mu\text{F}$, $C_{OUT} = 1 \mu\text{F}$, and $T_A = 25^\circ\text{C}$ (unless otherwise noted)



$V_{OUT} = 5.5 \text{ V}$, $V_{IN} = 6.0 \text{ V}$, $V_{EN} = 0 \text{ V to } 6.0 \text{ V}$,
 V_{EN} slew rate = $1 \text{ V}/\mu\text{s}$, $C_{OUT} = 10 \mu\text{F}$

Figure 6-85. Inrush Current

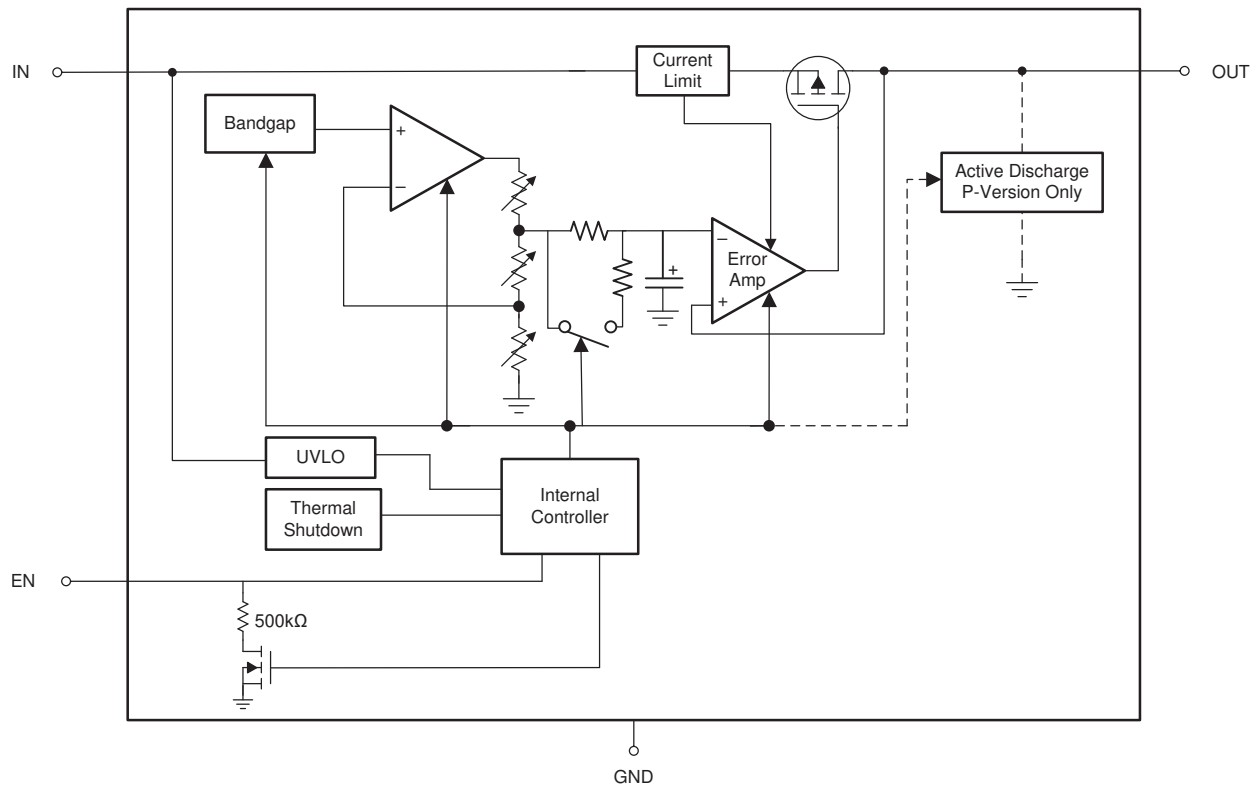
7 Detailed Description

7.1 Overview

Designed to meet the needs of sensitive RF and analog circuits, the TPS7A20 provides low noise, high PSRR, low quiescent current, as well as low line and load transient response figures. Using innovative design techniques, the TPS7A20 offers class-leading noise performance without the need for a separate noise filter capacitor.

The TPS7A20 is designed to operate with a single 1- μ F input capacitor and a single 1- μ F ceramic output capacitor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Low Output Noise

Any internal noise at the TPS7A20 reference voltage is reduced by a first-order, low-pass RC filter before being passed to the output buffer stage. The low-pass RC filter has a –3-dB cut-off frequency of approximately 0.1 Hz.

During start-up, the filter resistor is bypassed to reduce output rise time; the filter begins normal operation after the output voltage reaches the correct value.

7.3.2 Smart Enable

The enable (EN) input polarity is active high. The output voltage is enabled when the voltage of the enable input is greater than $V_{EN(HI)}$ and disabled when the enable input voltage is less than $V_{EN(LOW)}$. If independent control of the output voltage is not needed, connect EN to IN.

This device has a smart enable circuit to reduce quiescent current. When the voltage on the enable pin is driven above $V_{EN(HI)}$, as listed in the *Electrical Characteristics* table, the device is enabled and the smart enable internal pulldown resistor ($R_{EN(PULLDOWN)}$) is disconnected. When the enable pin is floating, the $R_{EN(PULLDOWN)}$ is connected and pulls the enable pin low to disable the device. The $R_{EN(PULLDOWN)}$ value is listed in the *Electrical Characteristics* table.

7.3.3 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} - V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the value required to maintain output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

7.3.4 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brickwall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brickwall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power $[(V_{IN} - V_{OUT}) \times I_{CL}]$. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power $[(V_{IN} - V_{OUT}) \times I_{SC}]$. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the [Know Your Limits application report](#).

Figure 7-1 shows a diagram of the foldback current limit.

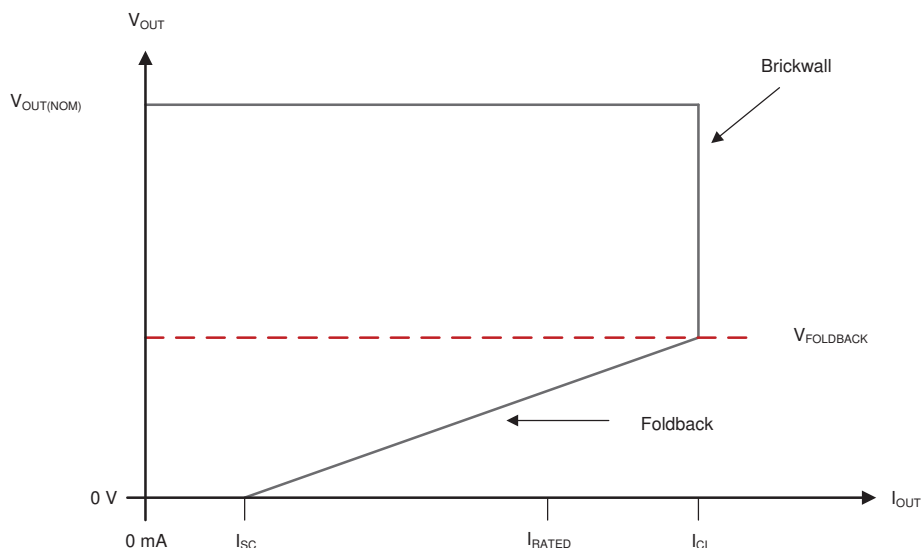


Figure 7-1. Foldback Current Limit

7.3.5 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

7.3.6 Thermal Shutdown

A thermal shutdown protection circuit disables the LDO when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during startup can be high from large $V_{IN} - V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before startup completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7.3.7 Active Discharge

An internal pulldown MOSFET connects a resistor from OUT to ground when the device is disabled to actively discharge the output capacitance. The active discharge circuit is activated by driving EN low or by the voltage on IN falling below the undervoltage lockout (UVLO) threshold.

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can possibly flow from the output to the input. This reverse current flow can cause damage to the device. Limit reverse current to no more than 5% of the device rated current for a short period of time.

7.4 Device Functional Modes

7.4.1 Device Functional Mode Comparison

Table 7-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

7.4.4 Disabled

The output of the LDO can be shut down by driving EN to less than $V_{EN(LOW)}$ (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shut down, and the output voltage is actively discharged to ground by an internal discharge circuit between OUT and ground.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a rule of thumb, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

8.1.2 Input and Output Capacitor Requirements

Although the LDO itself is stable without an input capacitor, good analog design practice is to connect a capacitor from IN to GND, with a value at least equal to the nominal value specified in the *Recommended Operating Conditions* table. The input capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR, and is recommended if the source impedance is greater than 0.5 Ω . When the source resistance and inductance are sufficiently high, especially in the presence of load transients, the overall system may be susceptible to instability (including ringing and sustained oscillation) and other performance degradation if there is insufficient capacitance between IN and GND. A capacitor with a value greater than the minimum may be necessary if large, fast-rise-time load or line transients are anticipated or if the device is located more than a few centimeters from the input power source.

An output capacitor of an appropriate value helps ensure stability and improve dynamic performance. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table.

8.1.3 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response: the transition from a light to a heavy load and the transition from a heavy to a light load. The regions shown in [Figure 8-1](#) are broken down as follows. Regions A, E, and H are where the output voltage is in steady-state.

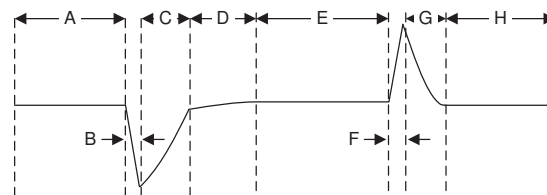


Figure 8-1. Load Transient Waveform

During transitions from a light load to a heavy load, the:

- Initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)

- Recovery from the dip results from the LDO increasing its sourcing current, and leads to output voltage regulation (region C)

During transitions from a heavy load to a light load, the:

- Initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)
- Recovery from the rise results from the LDO decreasing its sourcing current in combination with the load discharging the output capacitor (region G)

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger DC load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

8.1.4 Undervoltage Lockout (UVLO) Operation

The UVLO circuit ensures that the device stays disabled before its input supply reaches the minimum operational voltage range, and ensures that the device shuts down when the input supply collapses. [Figure 8-2](#) shows the UVLO circuit response to various input voltage events. The diagram can be separated into the following parts:

- Region A: The device does not start until the input reaches the UVLO rising threshold.
- Region B: Normal operation, regulating device.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output may fall out of regulation but the device remains enabled.
- Region D: Normal operation, regulating device.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is re-enabled when the UVLO rising threshold is reached by the input voltage and a normal start-up follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.
- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0 V. The output falls because of the load and active discharge circuit.

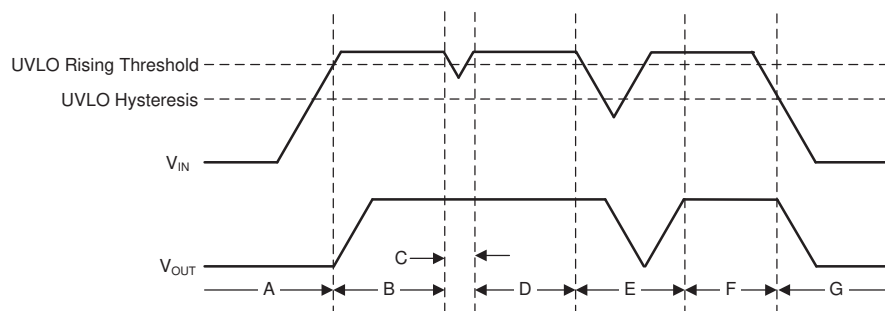


Figure 8-2. Typical UVLO Operation

8.1.5 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use [Equation 2](#) to approximate P_D :

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TPS7A20 allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. According to Equation 3, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A). Equation 4 rearranges Equation 3 for output current.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (3)$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \quad (4)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the X2SON package junction-to-case (bottom) thermal resistance ($R_{\theta JC(bot)}$) plus the thermal resistance contribution by the PCB copper.

8.1.5.1 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with Equation 5 and are given in the *Thermal Information* table.

$$\Psi_{JT} : T_J = T_T + \Psi_{JT} \times P_D \text{ and } \Psi_{JB} : T_J = T_B + \Psi_{JB} \times P_D \quad (5)$$

where:

- P_D is the power dissipated as explained in Equation 2
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

8.1.5.2 Recommended Area for Continuous Operation

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. The recommended area for continuous operation for a linear regulator is given in Figure 8-3 and can be separated into the following parts:

- Dropout voltage limits the minimum differential voltage between the input and the output ($V_{IN} - V_{OUT}$) at a given output current level. See the *Dropout Operation* section for more details.
- The rated output currents limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- The rated junction temperature limits the maximum junction temperature of the device. Exceeding this rating causes the device to fall out of specification and reduces long-term reliability.
 - The shape of the slope is given by Equation 4. The slope is nonlinear because the maximum-rated junction temperature of the LDO is controlled by the power dissipation across the LDO; thus when $V_{IN} - V_{OUT}$ increases the output current must decrease.
- The rated input voltage range governs both the minimum and maximum of $V_{IN} - V_{OUT}$.

Figure 8-3 shows the recommended area of operation for this device on a JEDEC-standard high-K board with a $R_{\theta JA}$ as given in the *Thermal Information* table.

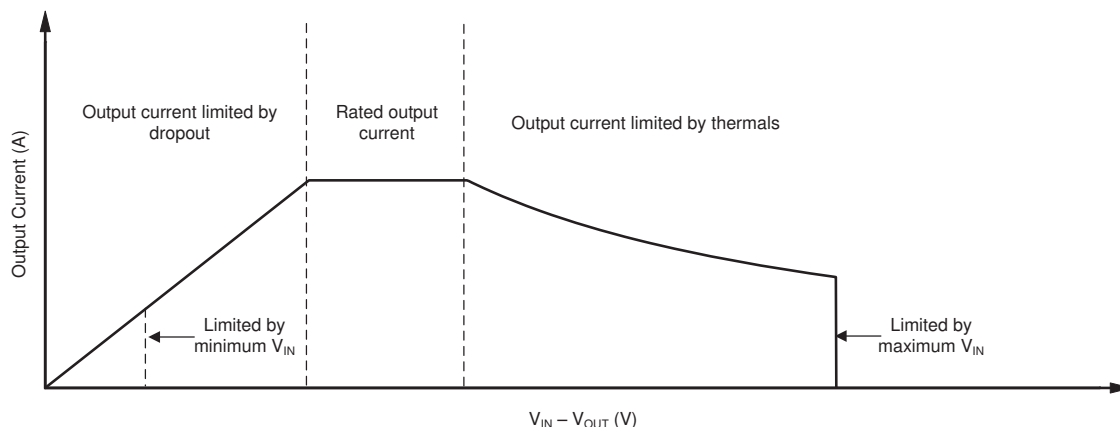
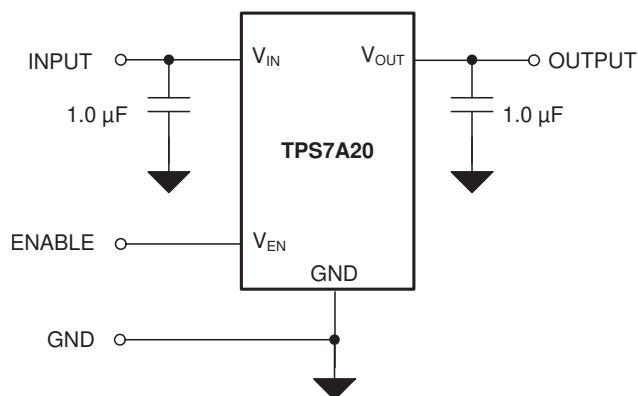


Figure 8-3. Region Description of Continuous Operation Regime

8.2 Typical Application

Figure 8-4 shows the typical application circuit for the TPS7A20. Input and output capacitances may need to be increased above the 1 μ F minimum for some applications.



SVA-30180501

Figure 8-4. TPS7A20 Typical Application

8.2.1 Design Requirements

Table 8-1 summarizes the design requirements for Figure 8-4.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	3.1 V to 3.6 V
Output voltage	2.8 V
Output current	200 mA
Maximum ambient temperature	85°C

8.2.2 Detailed Design Procedure

For this design example, the 2.8-V output version (TPS7A2028) is selected. A nominal 3.3-V input supply is assumed. A minimum 1.0- μ F input capacitor is recommended to minimize the effect of resistance and inductance between the 3.3-V source and the LDO input. A minimum 1.0- μ F output capacitor is also

recommended for stability and good load transient response. The dropout voltage (V_{DO}) is less than 140 mV maximum at a 2.8-V output voltage and 300-mA output current, so there are no dropout issues with a minimum input voltage of 3.0 V and a maximum output current of 200 mA.

8.2.3 Application Curves

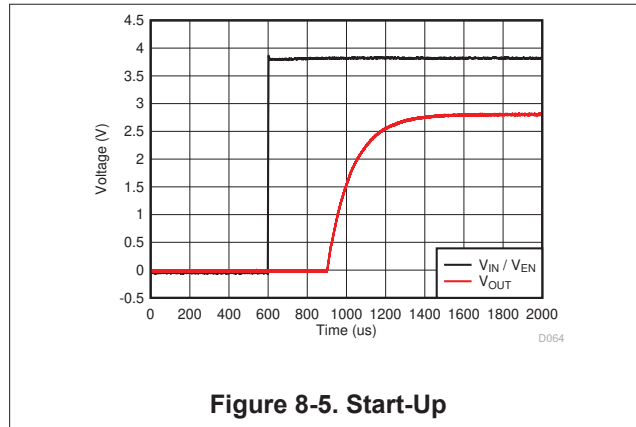


Figure 8-5. Start-Up

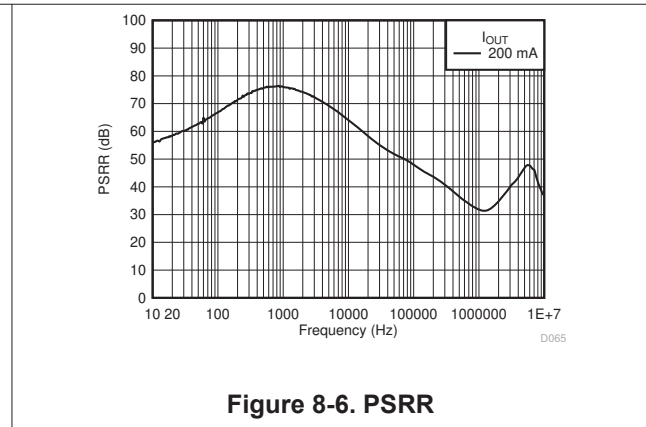


Figure 8-6. PSRR

9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.6 V to 6.0 V. The input supply must be well regulated and free of spurious noise. To ensure that the output voltage is well regulated and dynamic performance is optimum, the input supply must be at least $V_{OUT(nom)} + 0.3 \text{ V}$ or 1.6 V, whichever is greater. TI highly recommends using a 1- μF or greater input capacitor to reduce the impedance of the input supply, especially during transients.

10 Layout

10.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- Do not place a thermal via directly beneath the thermal pad of the DQN package. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

10.2 Layout Examples

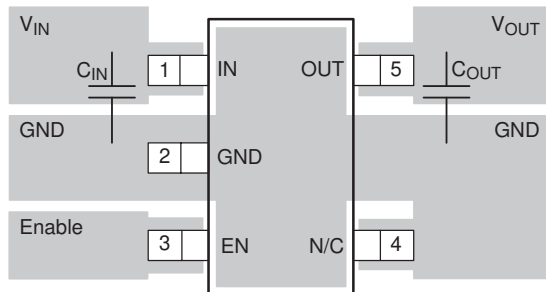


Figure 10-1. DBV Package (SOT-23) Typical Layout

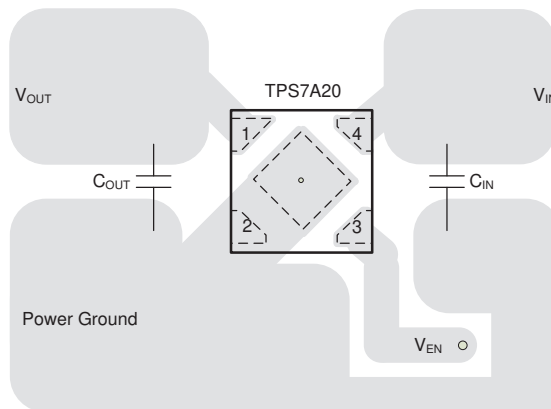


Figure 10-2. DQN Package (X2SON) Typical Layout

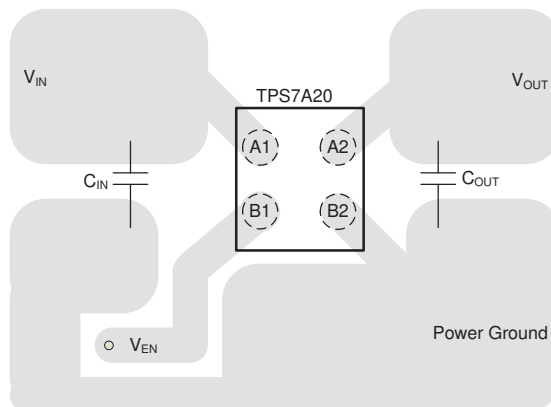


Figure 10-3. YCJ and YCK Package (DSBGA) Typical Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

Table 11-1. Device Nomenclature

PRODUCT ^{(1) (2)}	V _{OUT}
TPS7A20xx(x)Pyyyz	xx(x) is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V). P indicates an active output discharge feature. All members of the TPS7A20 family actively discharge the output when the device is disabled. yyy is the package designator. z is the package quantity. R is for reel (3000 pieces for DQN and DBV; 12000 pieces for YCJ and YCK).

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
- (2) Output voltages from 0.8 V to 5.5 V in 25-mV increments are available. Contact the factory for details and availability.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Mechanical Data

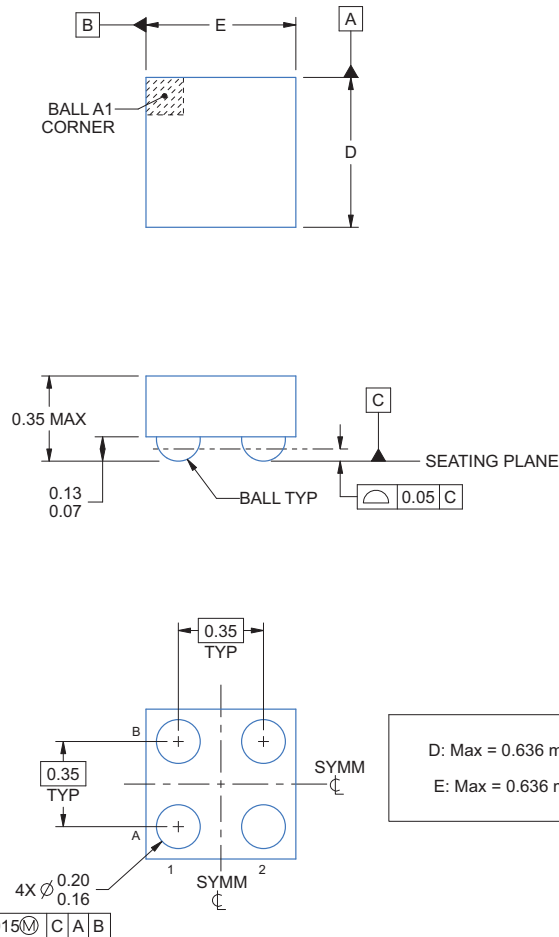


PACKAGE OUTLINE

YCJ0004-C02

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



4226216/A 09/2020

NOTES:

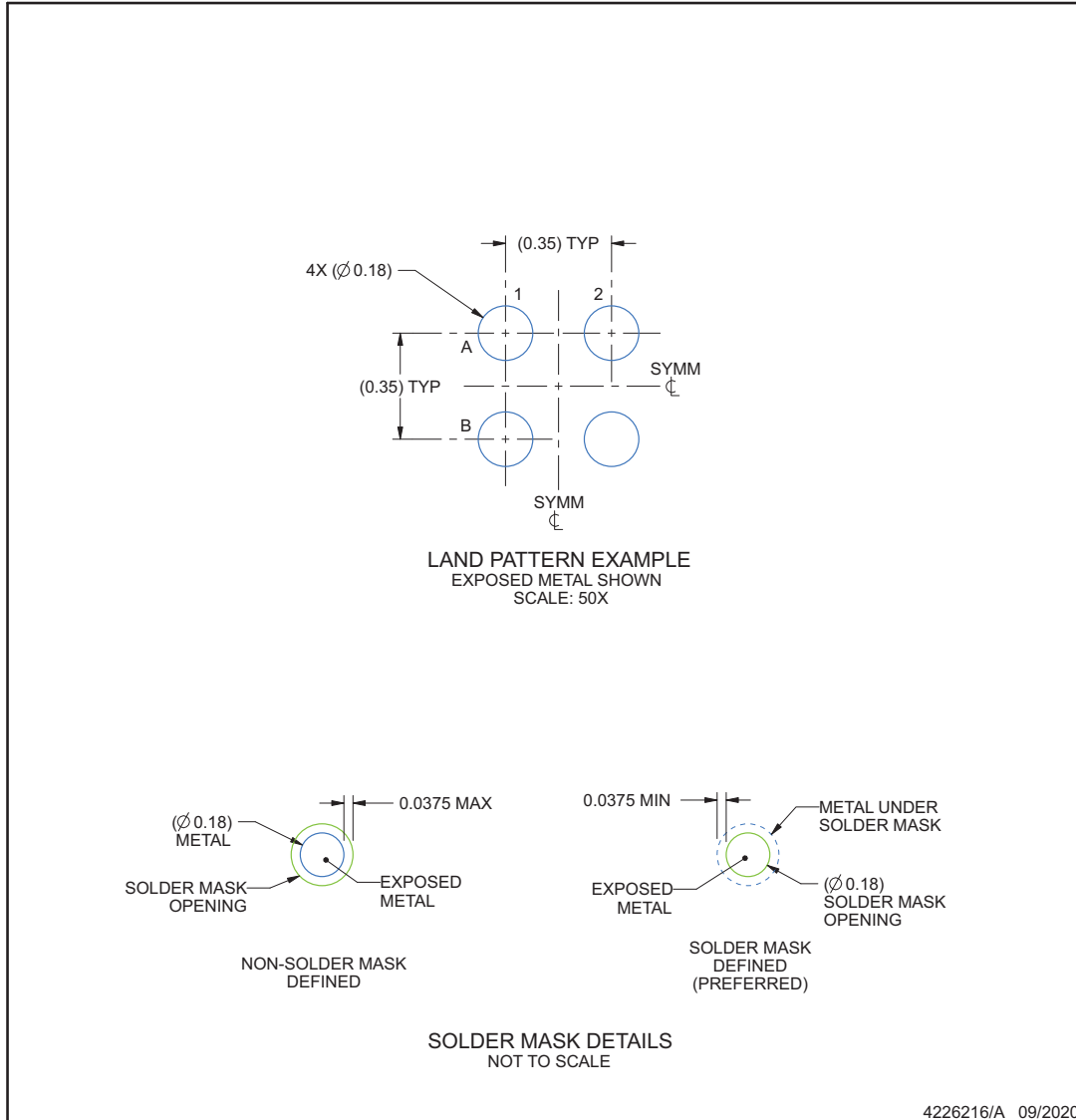
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YCJ0004-C02

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY

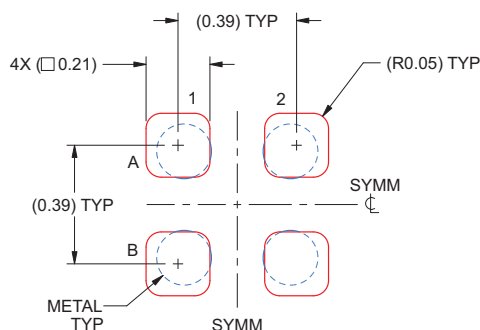


NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN**YCJ0004-C02****DSBGA - 0.35 mm max height**

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
 BASED ON 0.075 mm THICK STENCIL
 SCALE: 50X

4226216/A 09/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

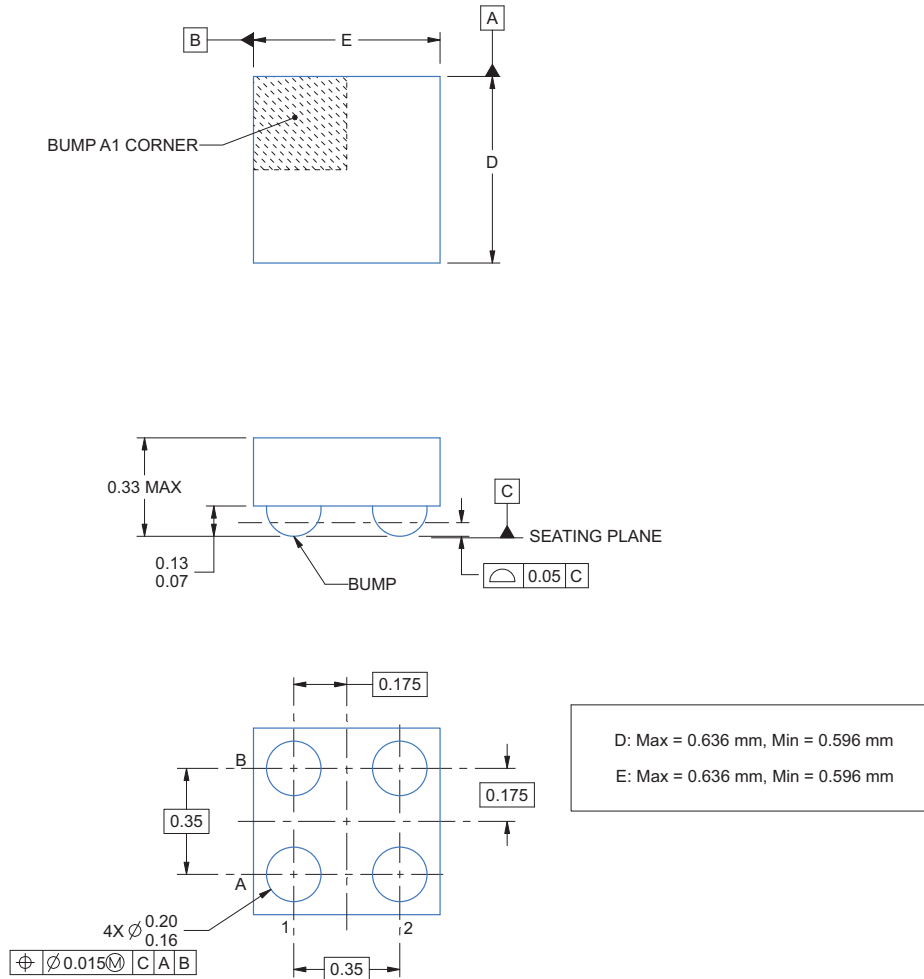


PACKAGE OUTLINE

YCK0004-C01

DSBGA - 0.33mm MAX HEIGHT

DIE SIZE BALL GRID ARRAY



4228575/A 03/2022

NOTES:

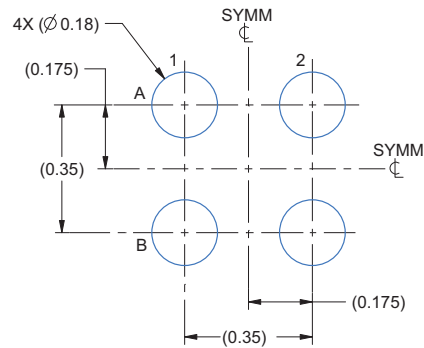
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



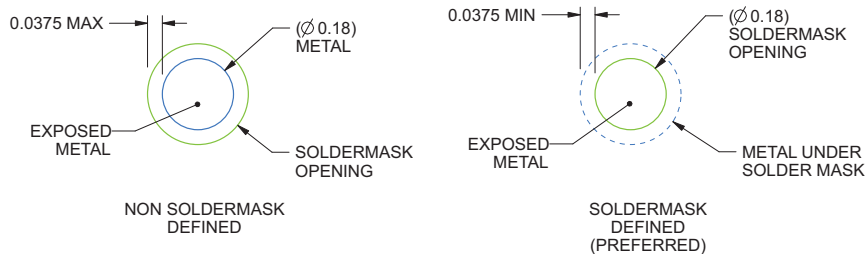
TEXAS
INSTRUMENTS
www.ti.com

EXAMPLE BOARD LAYOUT**YCK0004-C01****DSBGA - 0.33mm MAX HEIGHT**

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



SOLDERMASK DETAILS
NOT TO SCALE

4228575/A 03/2022

NOTES: (continued)

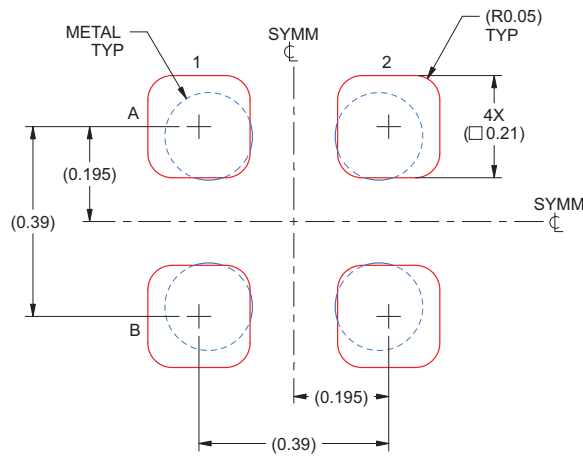
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YCK0004-C01

DSBGA - 0.33mm MAX HEIGHT

DIE SIZE BALL GRID ARRAY



4228575/A 03/2022

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS7A2025PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS7A2045PDQNR	ACTIVE	X2SON	DQN	4	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TPS7A2009PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2GBF	Samples
TPS7A2009PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KT	Samples
TPS7A20105PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KS	Samples
TPS7A2011PYCKR	ACTIVE	DSBGA	YCK	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	Q	Samples
TPS7A2012PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2ATF	Samples
TPS7A2012PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JC	Samples
TPS7A2012PYCJR	ACTIVE	DSBGA	YCJ	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	M	Samples
TPS7A2015PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2DTF	Samples
TPS7A2015PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	JD	Samples
TPS7A201825PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	IQ	Samples
TPS7A20185PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2CBF	Samples
TPS7A20185PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	JE	Samples
TPS7A20185PYCKR	ACTIVE	DSBGA	YCK	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	T	Samples
TPS7A2018PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2AUF	Samples
TPS7A2018PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	JF	Samples
TPS7A2018PDQNRM3	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JF	Samples
TPS7A2018PYCKR	ACTIVE	DSBGA	YCK	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D	Samples
TPS7A2020PYCKR	ACTIVE	DSBGA	YCK	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	S	Samples

PACKAGE OPTION ADDENDUM

4-Aug-2023

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A2022PYCKR	ACTIVE	DSBGA	YCK	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	K	Samples
TPS7A2024PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2CCF	Samples
TPS7A2025PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2AVF	Samples
TPS7A2025PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JG	Samples
TPS7A2025PYCJR	ACTIVE	DSBGA	YCJ	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	L	Samples
TPS7A2027PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KO	Samples
TPS7A2027PYCJR	ACTIVE	DSBGA	YCJ	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	N	Samples
TPS7A20285PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2GCF	Samples
TPS7A20285PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KN	Samples
TPS7A20285PYCKR	ACTIVE	DSBGA	YCK	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	P	Samples
TPS7A2028PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2AWF	Samples
TPS7A2028PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	JH	Samples
TPS7A2028PDQNRM3	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JH	Samples
TPS7A2028PYCJR	ACTIVE	DSBGA	YCJ	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	E	Samples
TPS7A2028PYCKR	ACTIVE	DSBGA	YCK	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	E	Samples
TPS7A2029PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JI	Samples
TPS7A2030PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2AXF	Samples
TPS7A2030PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JJ	Samples
TPS7A2031PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2GDF	Samples
TPS7A2032PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2GEF	Samples
TPS7A2033PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2AZF	Samples

PACKAGE OPTION ADDENDUM

4-Aug-2023

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A2033PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	JA	Samples
TPS7A2033PDQNRM3	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JA	Samples
TPS7A2033PYCJR	ACTIVE	DSBGA	YCJ	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	O	Samples
TPS7A2036PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2GIF	Samples
TPS7A2036PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KP	Samples
TPS7A2040PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KQ	Samples
TPS7A2042PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2GFF	Samples
TPS7A2042PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KV	Samples
TPS7A2045PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2GGF	Samples
TPS7A2045PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	JB	Samples
TPS7A2050PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2B1F	Samples
TPS7A2050PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KR	Samples
TPS7A2050PDQNRM3	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KR	Samples
TPS7A2050PYCKR	ACTIVE	DSBGA	YCK	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	H	Samples
TPS7A2055PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	2GHF	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

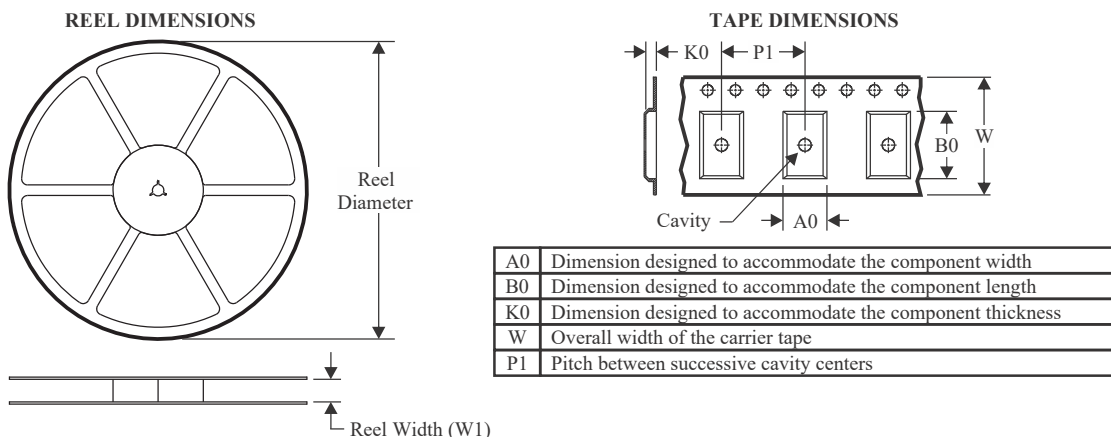
⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

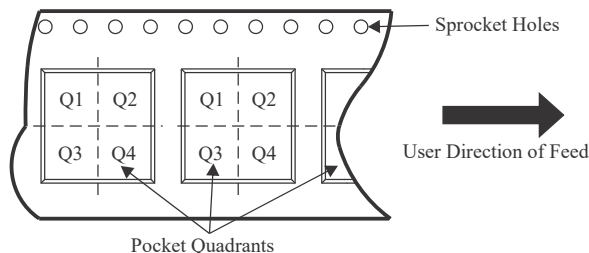
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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



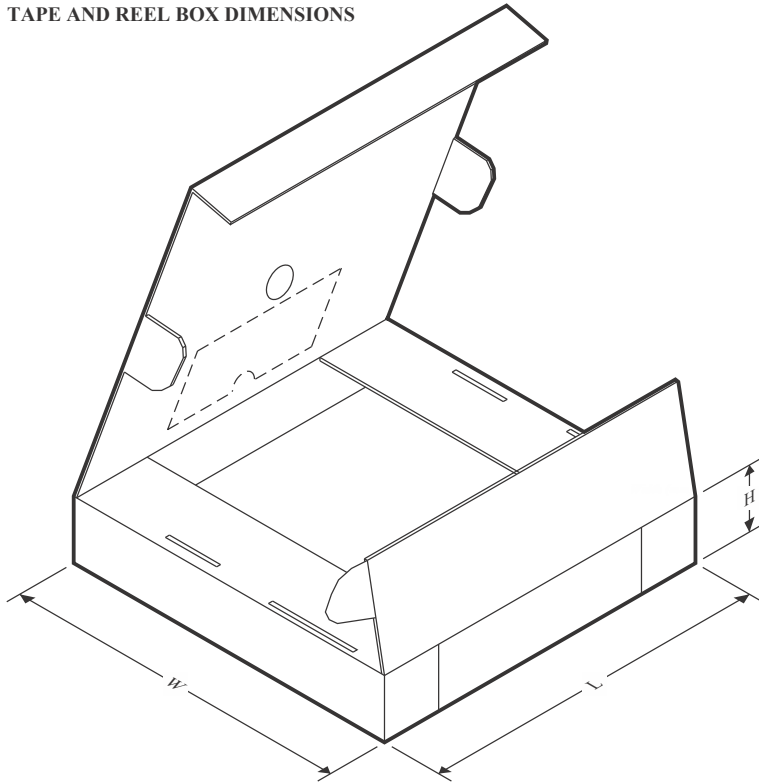
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A2009PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2009PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A20105PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2011PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2011PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2012PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2012PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2012PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2012PYCJR	DSBGA	YCJ	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2012PYCJR	DSBGA	YCJ	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2015PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2015PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2015PDQNR	X2SON	DQN	4	3000	178.0	8.4	1.13	1.13	0.53	4.0	8.0	Q2
TPS7A201825PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A201825PDQNR	X2SON	DQN	4	3000	178.0	8.4	1.13	1.13	0.53	4.0	8.0	Q2
TPS7A20185PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A20185PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A20185PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A20185PDQNR	X2SON	DQN	4	3000	178.0	8.4	1.13	1.13	0.53	4.0	8.0	Q2
TPS7A20185PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2018PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2018PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2018PDQNR	X2SON	DQN	4	3000	178.0	8.4	1.13	1.13	0.53	4.0	8.0	Q2
TPS7A2018PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2018PDQNRM3	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2018PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2018PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2020PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2020PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2022PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2022PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2024PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2024PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2025PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2025PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2025PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2025PYCJR	DSBGA	YCJ	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2025PYCJR	DSBGA	YCJ	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2027PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2027PYCJR	DSBGA	YCJ	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2027PYCJR	DSBGA	YCJ	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A20285PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A20285PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A20285PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2028PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2028PDQNR	X2SON	DQN	4	3000	178.0	8.4	1.13	1.13	0.53	4.0	8.0	Q2
TPS7A2028PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2028PDQNRM3	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2028PYCJR	DSBGA	YCJ	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2028PYCJR	DSBGA	YCJ	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2028PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2028PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2029PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2030PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2030PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2030PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2031PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A2031PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A2032PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2032PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A2033PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2033PDQNR	X2SON	DQN	4	3000	178.0	8.4	1.13	1.13	0.53	4.0	8.0	Q2
TPS7A2033PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2033PDQNRM3	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2033PYCJR	DSBGA	YCJ	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2033PYCJR	DSBGA	YCJ	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2036PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A2036PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2036PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2040PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2042PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A2042PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2042PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2045PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2045PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2050PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2050PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2050PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2050PDQNRM3	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A2050PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2050PYCKR	DSBGA	YCK	4	12000	180.0	8.4	0.71	0.71	0.42	2.0	8.0	Q1
TPS7A2055PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A2055PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

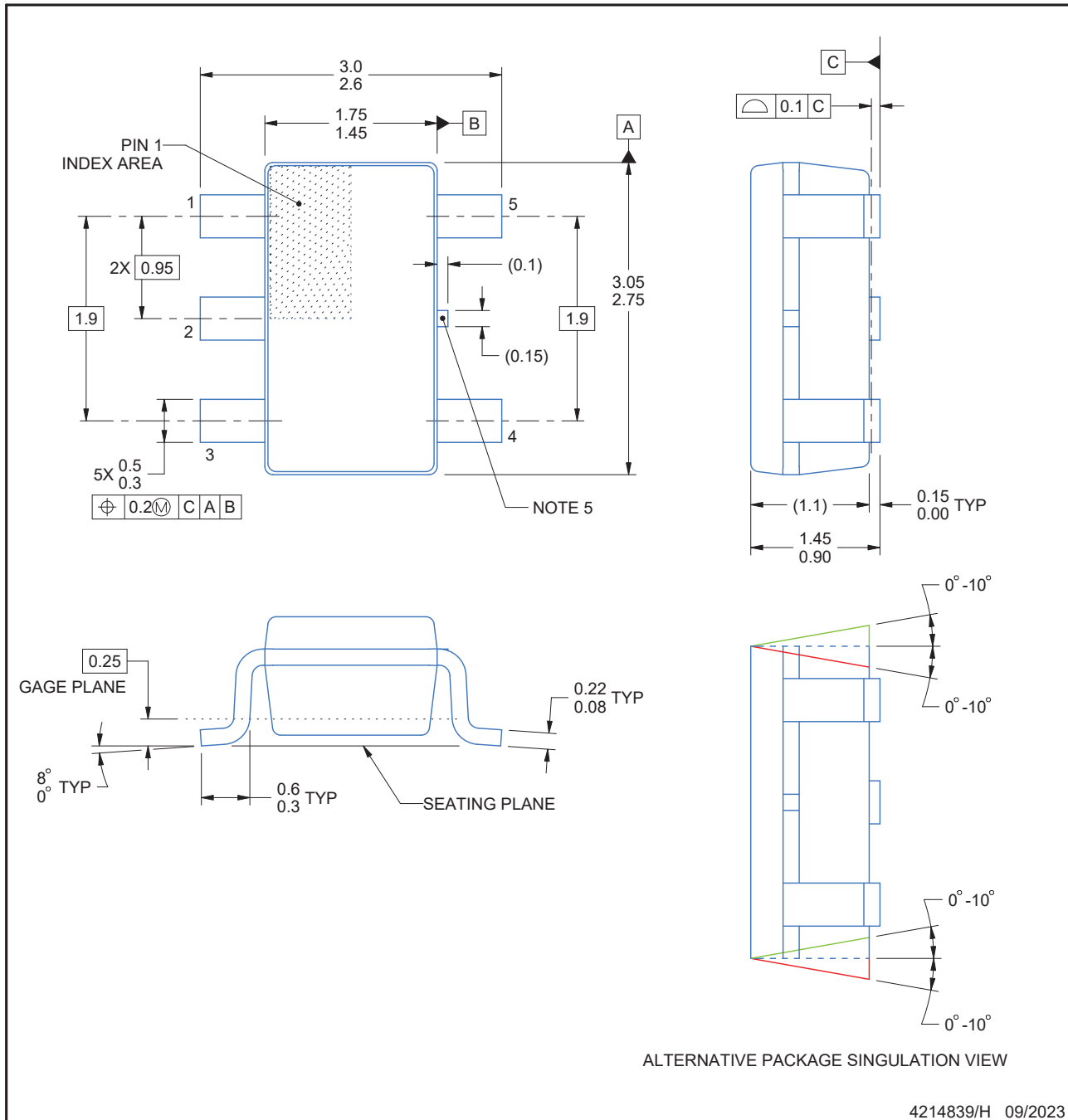


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A2009PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2009PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A20105PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A2011PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2011PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2012PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2012PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2012PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A2012PYCJR	DSBGA	YCJ	4	12000	182.0	182.0	20.0
TPS7A2012PYCJR	DSBGA	YCJ	4	12000	210.0	185.0	35.0
TPS7A2015PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2015PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A2015PDQNR	X2SON	DQN	4	3000	205.0	200.0	33.0
TPS7A201825PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A201825PDQNR	X2SON	DQN	4	3000	205.0	200.0	33.0
TPS7A20185PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A20185PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A20185PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A20185PDQNR	X2SON	DQN	4	3000	205.0	200.0	33.0
TPS7A20185PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2018PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2018PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2018PDQNR	X2SON	DQN	4	3000	205.0	200.0	33.0
TPS7A2018PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A2018PDQNRM3	X2SON	DQN	4	3000	210.0	185.0	35.0
TPS7A2018PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2018PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2020PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2020PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2022PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2022PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2024PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2024PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2025PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2025PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2025PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A2025PYCJR	DSBGA	YCJ	4	12000	182.0	182.0	20.0
TPS7A2025PYCJR	DSBGA	YCJ	4	12000	210.0	185.0	35.0
TPS7A2027PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A2027PYCJR	DSBGA	YCJ	4	12000	210.0	185.0	35.0
TPS7A2027PYCJR	DSBGA	YCJ	4	12000	182.0	182.0	20.0
TPS7A20285PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A20285PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A20285PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2028PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2028PDQNR	X2SON	DQN	4	3000	205.0	200.0	33.0
TPS7A2028PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A2028PDQNRM3	X2SON	DQN	4	3000	210.0	185.0	35.0
TPS7A2028PYCJR	DSBGA	YCJ	4	12000	182.0	182.0	20.0
TPS7A2028PYCJR	DSBGA	YCJ	4	12000	210.0	185.0	35.0
TPS7A2028PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2028PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2029PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A2030PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2030PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2030PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A2031PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2031PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A2032PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2032PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A2033PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A2033PDQNR	X2SON	DQN	4	3000	205.0	200.0	33.0
TPS7A2033PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A2033PDQNRM3	X2SON	DQN	4	3000	210.0	185.0	35.0
TPS7A2033PYCJR	DSBGA	YCJ	4	12000	210.0	185.0	35.0
TPS7A2033PYCJR	DSBGA	YCJ	4	12000	182.0	182.0	20.0
TPS7A2036PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A2036PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2036PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A2040PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A2042PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A2042PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2042PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A2045PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2045PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A2050PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2050PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2050PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A2050PDQNRM3	X2SON	DQN	4	3000	210.0	185.0	35.0
TPS7A2050PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2050PYCKR	DSBGA	YCK	4	12000	182.0	182.0	20.0
TPS7A2055PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A2055PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0



4214839/H 09/2023

NOTES:

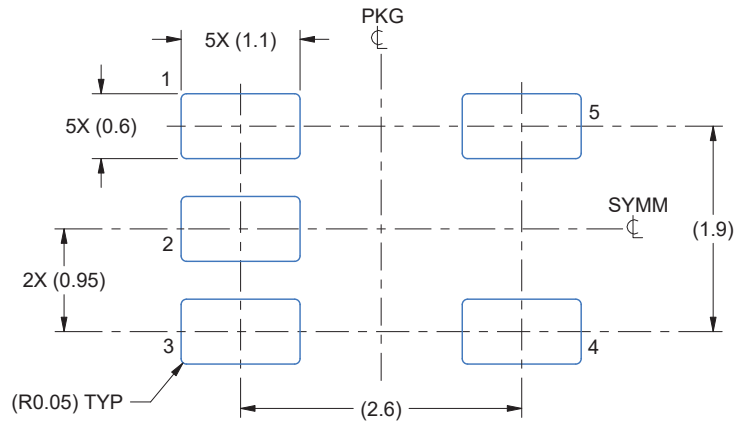
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

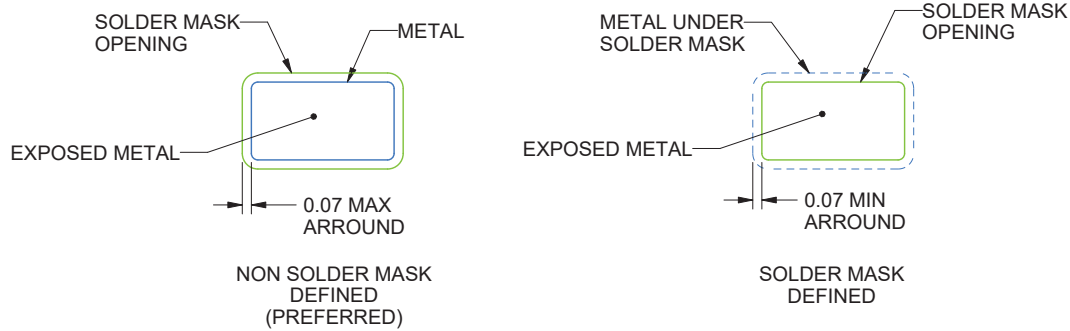
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SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

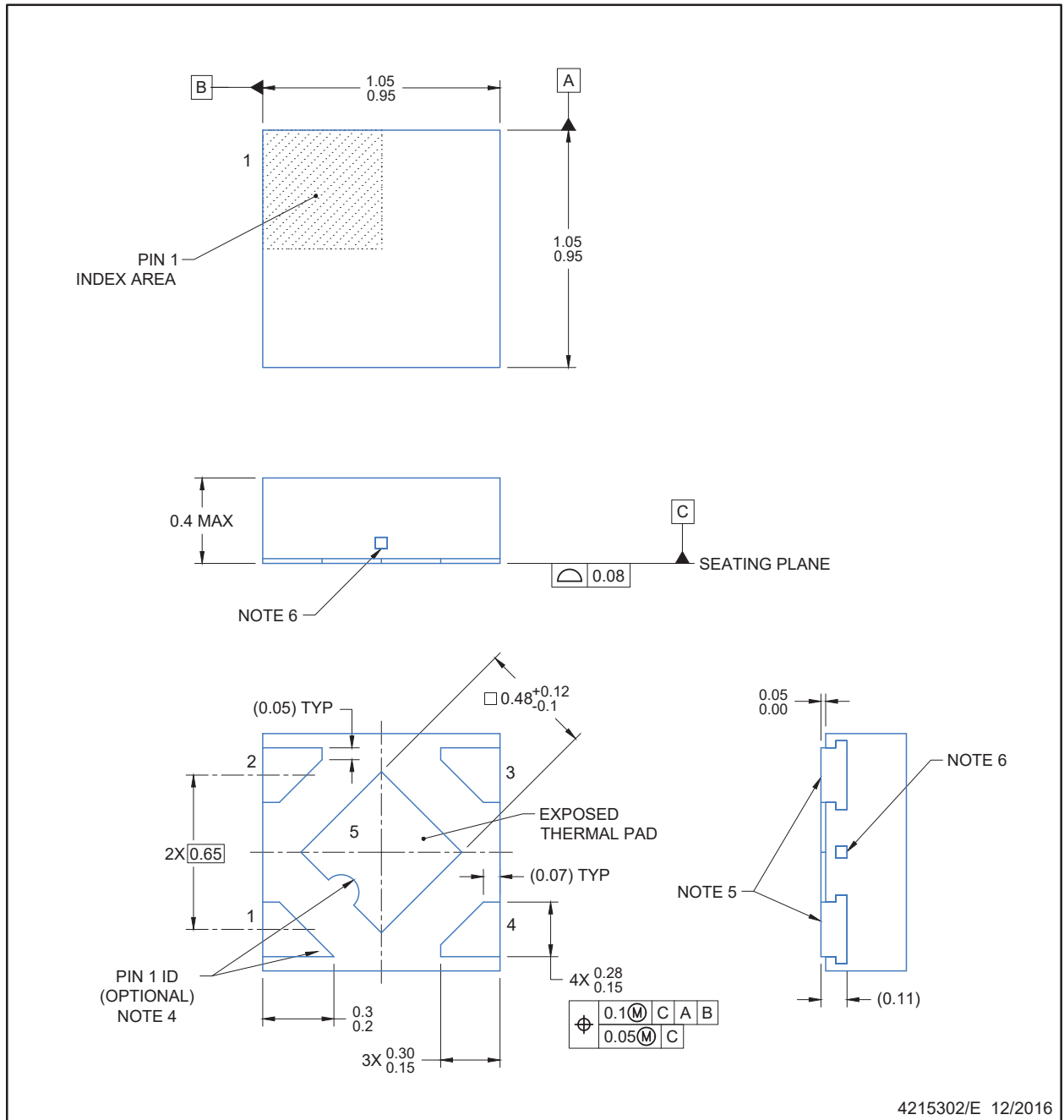
4214839/H 09/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

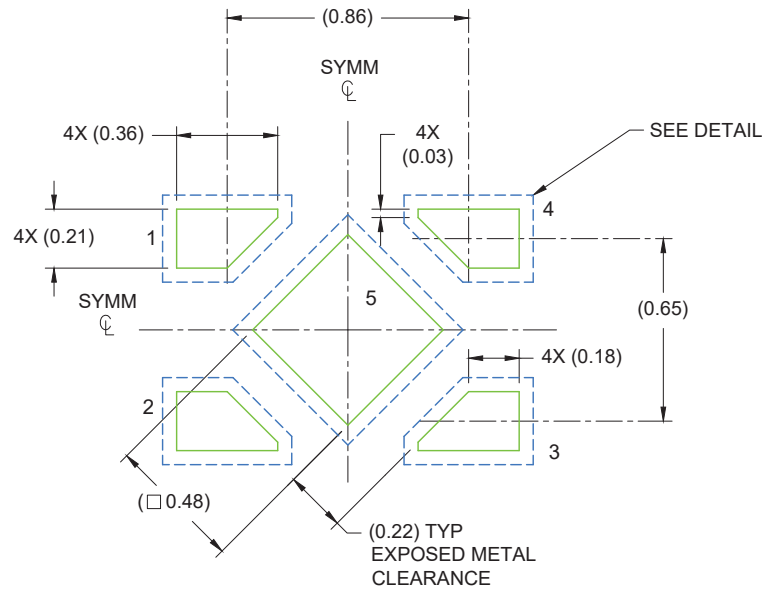


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

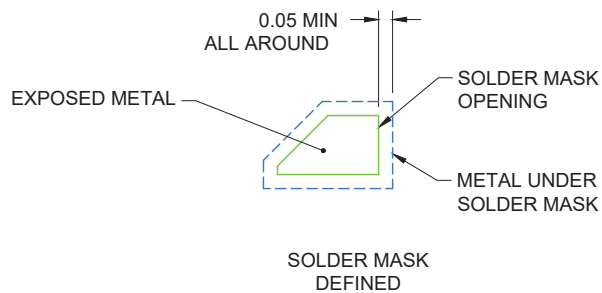


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



LAND PATTERN EXAMPLE
SCALE: 40X

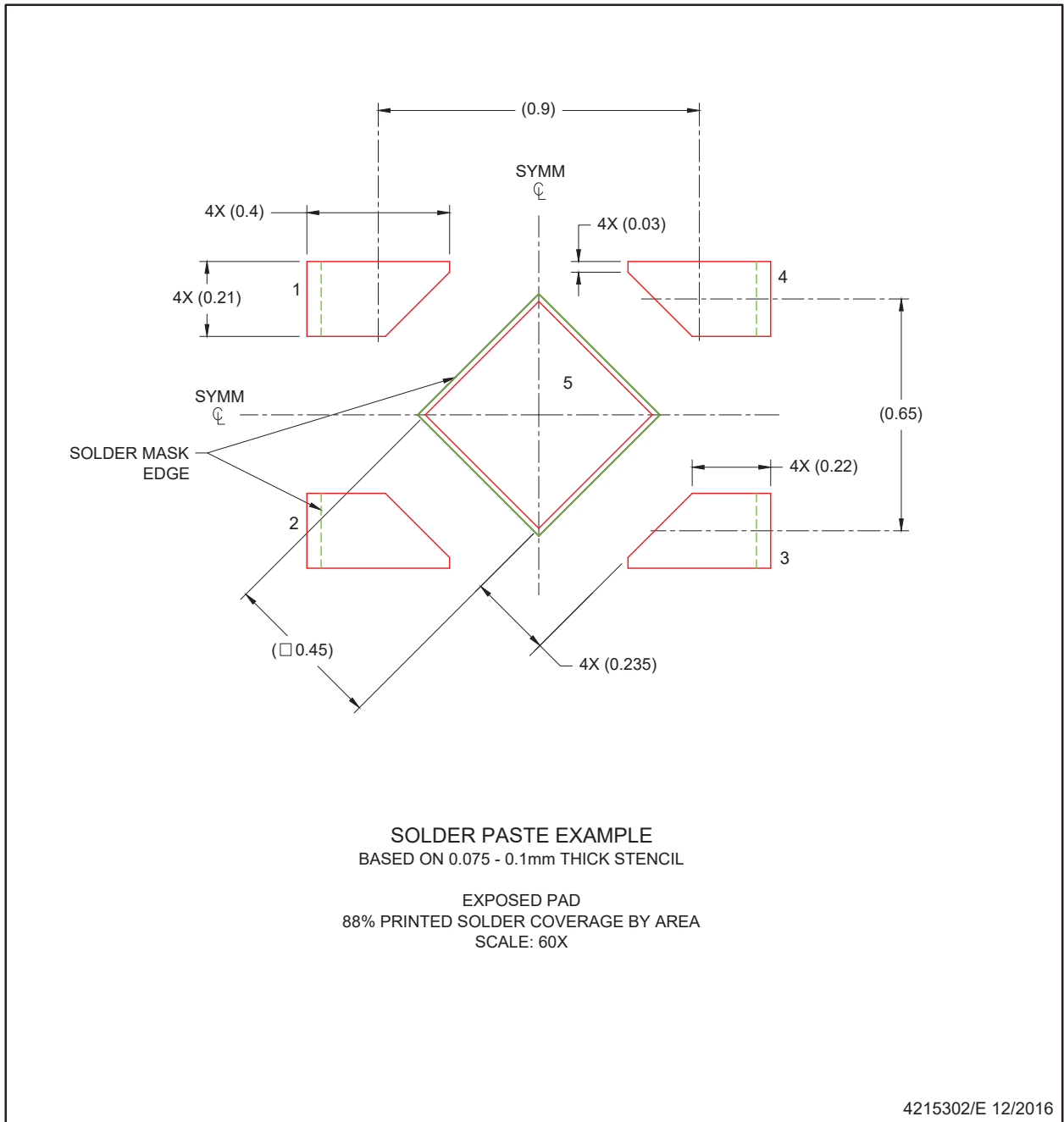


SOLDER MASK DETAIL

4215302/E 12/2016

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Exhibit 2

MAX25302A/MAX25302B**2A Automotive Low-Noise LDO Linear
Regulators****General Description**

The MAX25302A/MAX25302B are 1.7V to 5.5V V_{IN} , low-noise linear regulators that delivers up to 2A of output current with only 5.1 μ V_{RMS} of output noise from 10Hz to 100kHz. The regulator maintains $\pm 1\%$ output accuracy over a wide input voltage range, requiring only 100mV of input-to-output headroom at full load. The 1.3mA no-load supply current is independent of dropout voltage.

The output voltage on the MAX25302B can be adjusted to a value in the range of 0.6V to 5.0V by using two external resistors. The MAX25302B also includes an active-high POK signal for trouble-free load startup.

The MAX25302A has nine pin-selectable output voltages: 1.2V, 1.5V, 1.8V, 2.5V, 3.0V, 3.1V, 3.3V, 4.0V, and 5V.

All versions include a programmable output soft-start rate, output overcurrent, and thermal-overload protection.

The MAX25302A/MAX25302B are offered in a 3mm x 3.5mm, 14-pin TDFN package.

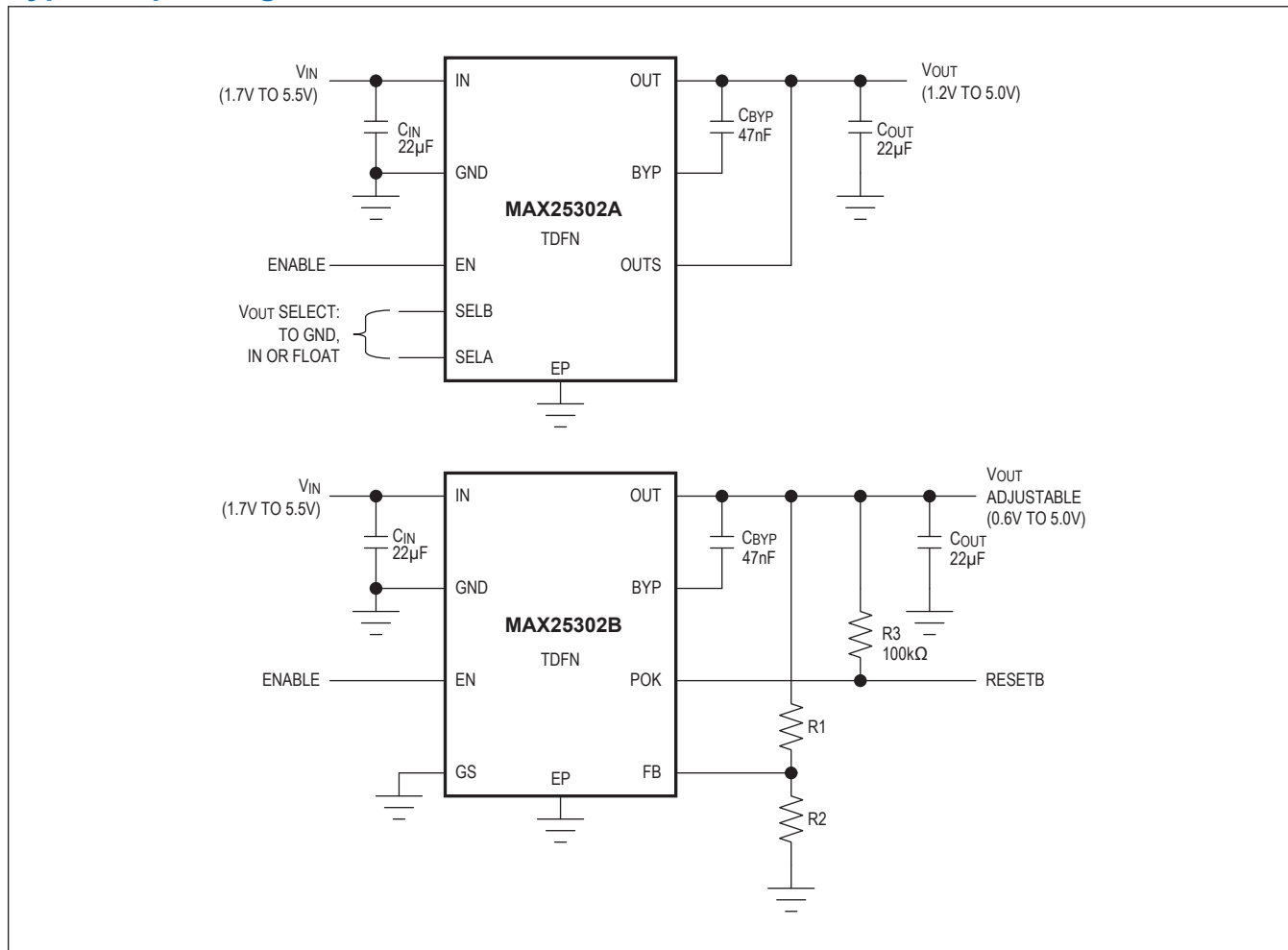
Applications

- Automotive Electronics
- High-End Audio Systems
- High-Resolution Data-Acquisition Systems

Benefits and Features

- Delivers Flexible Operating Range
 - 1.7V to 5.5V Input Voltage Range
 - 0.6V to 5.0V Programmable Output Voltage
 - 2A Maximum Output Current
 - 100mV Maximum Dropout at 2A Load
 - < 1.5 μ A Shutdown Supply Current
- Reduces Noise and Improves Accuracy
 - $\pm 1\%$ DC Accuracy over Load, Line, and Temperature
 - 5.1 μ V_{RMS} Output Noise, 10Hz to 100kHz
 - 1.3mA Quiescent Supply Current
 - > 70dB PSRR at 10kHz
- Enables Ease-of-Use and Robust Protection
 - Stable with 8 μ F (min) Output Capacitance
 - Programmable Soft-Start Rate
 - Overcurrent and Overtemperature Protection
 - Output-to-Input Reverse-Current Protection
 - Power-OK Status Pin
- Reduces PC Board Area
 - 3mm x 3.5mm, 14-pin TDFN Package
- AEC-Q100
 - -40°C to +125°C Operating Temperature

Typical Operating Circuits



Absolute Maximum Ratings

IN, OUT, SELA, SELB, EN to GND	-0.3V to +6V	Operating Temperature Range	-40°C to +125°C
POK, OUTS, FB, GS to GND	-0.3V to +6V	Maximum Junction Temperature	+150°C
BYP	-0.3V to +2V	Storage Temperature Range	-65°C to +150°C
Output Short-Circuit Duration	Continuous	Soldering Temperature (reflow)	+260°C
Continuous Power Dissipation TDFN (T _A = +70°C, derate 24.4mW/°C above +70°C.)	1951mW		

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TDFN

Package Code	T143A3+1C
Outline Number	21-100420
Land Pattern Number	90-100149
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ _{JA})	54°C/W
Junction to Case (θ _{JC})	8°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ _{JA})	41°C/W
Junction to Case (θ _{JC})	8°C/W

Electrical Characteristics

(V_{IN} = 3.6V, T_J = -40°C to +125°C, C_{BYP} = 47nF, C_{IN} = 22μF, C_{OUT} = 22μF, Typical Operating Circuit, unless otherwise specified. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V _{IN}	Guaranteed by output accuracy	1.7		5.5	V
Input Undervoltage Lockout	V _{UVLO}	V _{IN} rising, 100mV hysteresis	1.5	1.6	1.7	V
Output Voltage Range	V _{OUT}	V _{IN} > V _{OUT} + 0.1V	0.6		5.0	V
Output Capacitance	C _{OUT}	For stability and proper operation	8	22		μF
Supply Current	I _{IN}	V _{EN} = V _{IN} = 3.6V, I _{OUT} = 0mA		1300		μA
		V _{EN} = 0V	T _A = +25°C		0.04	
			T _A = 125°C		1.5	
FB Regulation Accuracy (MAX25302B Only)	ACC	I _{OUT} from 0.1mA to 2A, V _{IN} from V _{OUT} + 0.3V to 5.5V, V _{IN} > 1.7V	0.594	0.6	0.606	V
OUT Regulation Accuracy (MAX25302A Only)	ACC	I _{OUT} from 0.1mA to 2A, V _{IN} from V _{OUT} + 0.3V to 5.5V, V _{IN} > 1.7V	-1		+1	%
Load Regulation		V _{IN} = 2.8V, V _{OUT} = 2.5V, I _{OUT} from 0.1mA to 2A		0.032		%
Load Transient		Output voltage deviation with a load change of I _{OUT} = 50mA to 2.0A to 50mA, with t _{RISE} = t _{FALL} = 1μs		50		mVp-p

Electrical Characteristics (continued)

($V_{IN} = 3.6V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, $C_{BYP} = 47nF$, $C_{IN} = 22\mu F$, $C_{OUT} = 22\mu F$, Typical Operating Circuit, unless otherwise specified. (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Line Regulation		V_{IN} from 2.8V to 5.5V, $V_{OUT} = 2.5V$, $I_{OUT} = 800mA$			0.054		%/V
Line Transient		$V_{IN} = 4V$ to $5V$ to $4V$, $I_{OUT} = 2A$, $t_{RISE} = t_{FALL} = 5\mu s$			3		mV _{P-P}
Dropout Voltage (Note 2)		$I_{OUT} = 2A$	$V_{IN} = 3.6V$		47	100	mV
			$V_{IN} = 2.5V$ (Note 3)		65	200	
			$V_{IN} = 1.7V$		100	300	
Current Limit		$V_{OUT} = 95\%$ of regulation, $V_{IN} - V_{OUT} = 0.5V$, $V_{IN} = 3.6V$		2.2	2.8	3.4	A
Output Noise		$I_{OUT} = 100mA$, $C_{BYP} = 100nF$	$f = 10Hz$ to $100kHz$		5.1		μV_{RMS}
Power Supply Rejection Ratio	PSRR	$V_{IN} = V_{OUT} + 400mV$, $I_{OUT} = 1.6A$	$f = 1kHz$		70		dB
			$f = 10kHz$		70		
			$f = 100kHz$		60		
			$f = 1MHz$		40		
BYP Capacitor Range	C_{BYP}	Regulator remain stable		0.001		0.1	μF
BYP Soft-Start Current		From BYP to GND during startup			50		μA
EN Input Threshold		V_{IN} from 1.7V to 5.5V	EN rising		0.8	1.2	V
EN Input Threshold		V_{IN} from 1.7V to 5.5V	EN falling	0.4	0.7		V
EN Input Leakage Current		V_{EN} from 1.7V to 5.5V	$T_A = +25^{\circ}C$	-1	+0.001	+1	μA
		V_{EN} from 1.7V to 5.5V	$T_A = +125^{\circ}C$		0.01		
POK Threshold (MAX25302B Only)		V_{OUT} when POK switches	V_{OUT} rising	88	91	94	%
			V_{OUT} falling		88		
POK Voltage, Low (MAX25302B Only)	V_{OL}	$I_{POK} = 1mA$			10	100	mV
POK Leakage Current (MAX25302B Only)		$V_{POK} = 5.5V$	$T_A = +25^{\circ}C$	-0.1	+0.001	+0.1	μA
			$T_A = +125^{\circ}C$		0.01		
SELA/B Input Resistance (MAX25302A Only)	$R_{INSELA/B}$	When shorted to GND or IN				500	Ω
		When Hi-Z		1			M Ω
SELA/B Input Capacitance (MAX25302A Only)	$C_{INSELA/B}$	When Hi-Z				10	pF
IN Reverse-Current Threshold	I_{IN_REV}	$V_{OUT} = 3.6V$, when V_{IN} falls to 0V			800		mA
Thermal Shutdown Threshold		T_J when output turns on/off	T_J rising		165		$^{\circ}C$
			T_J falling		150		

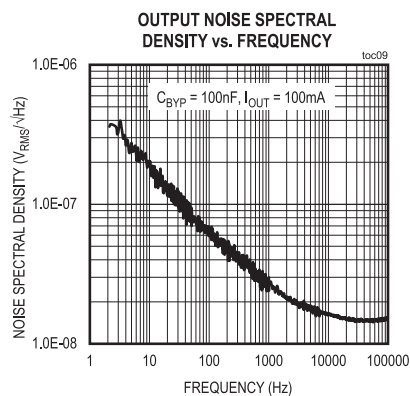
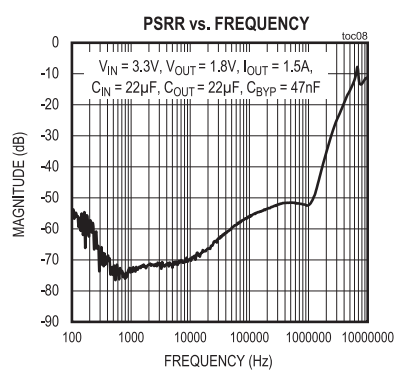
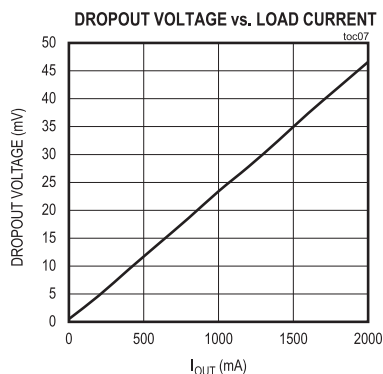
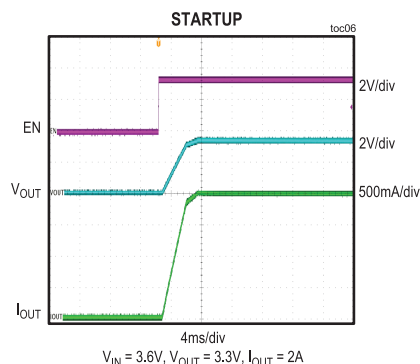
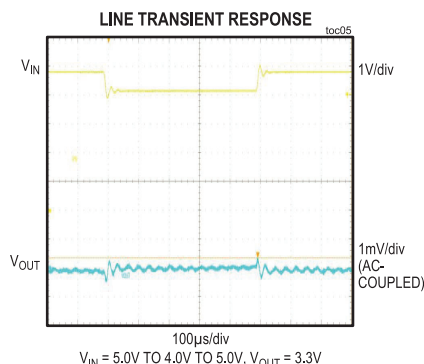
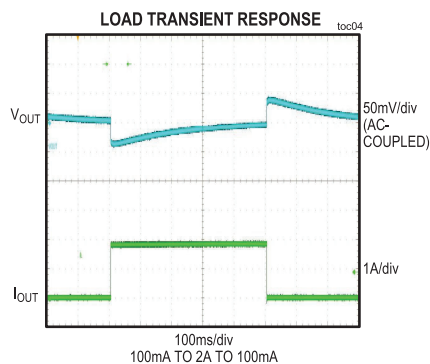
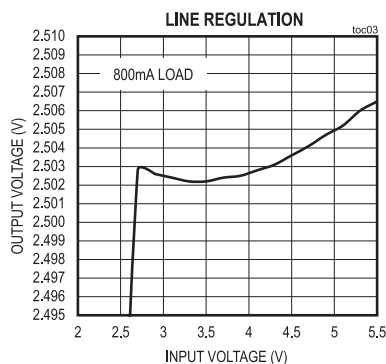
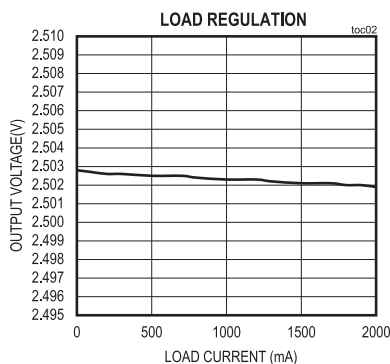
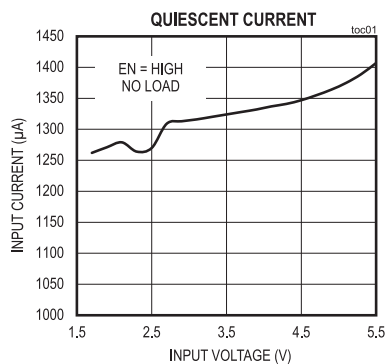
Note 1: Limits over the specified operating temperature and supply voltage range are guaranteed by design and characterization, and production tested at room temperature only.

Note 2: Dropout voltage is defined as $(V_{IN} - V_{OUT})$ when V_{OUT} is 95% of its nominal value.

Note 3: Guaranteed by design and characterization.

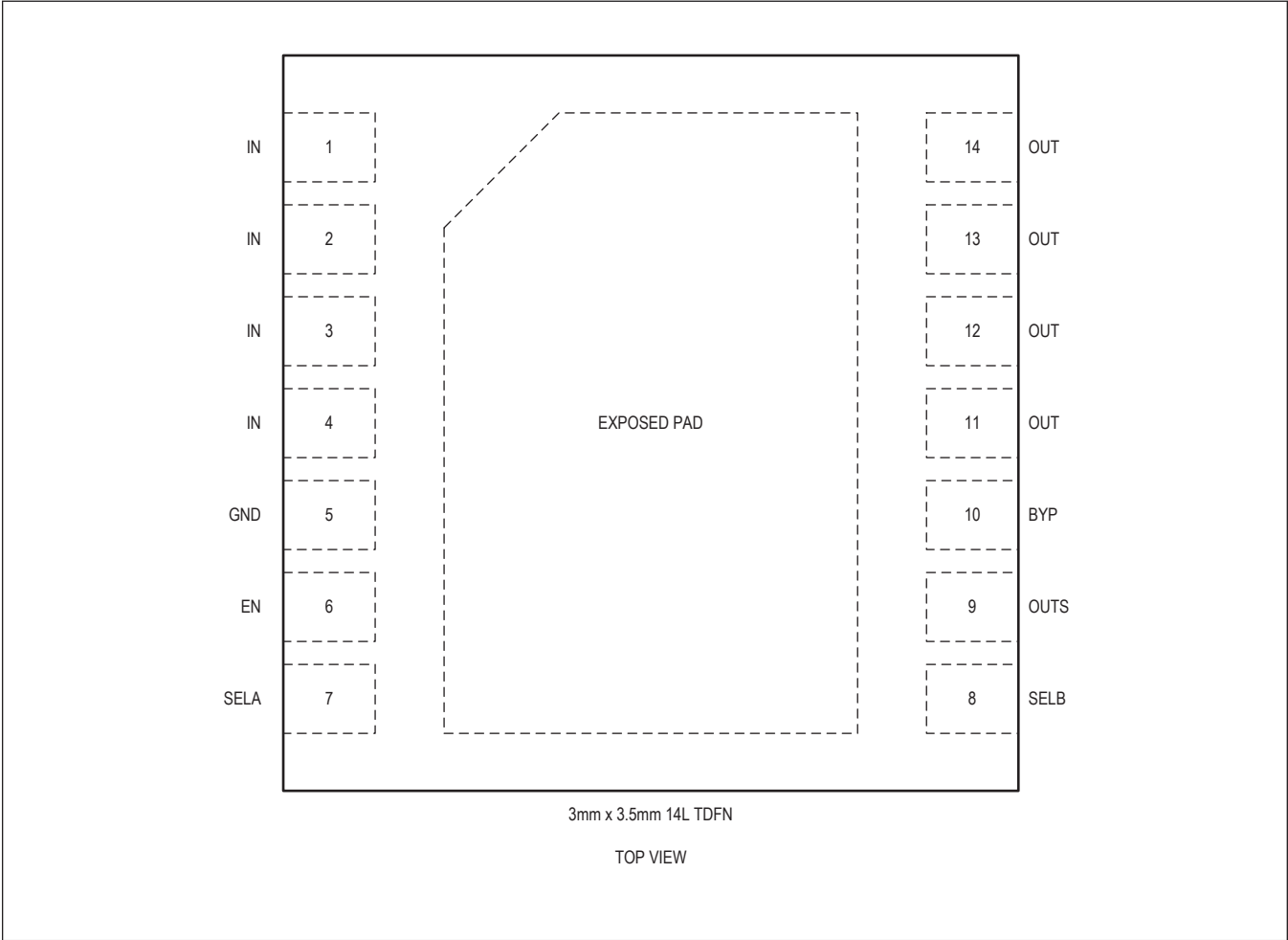
Typical Operating Characteristics

(MAX25302BATD+, $V_{IN} = 3.6V$, $V_{OUT} = 2.5V$, $C_{BYP} = 47nF$, $C_{IN} = 22\mu F$, $C_{OUT} = 22\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)

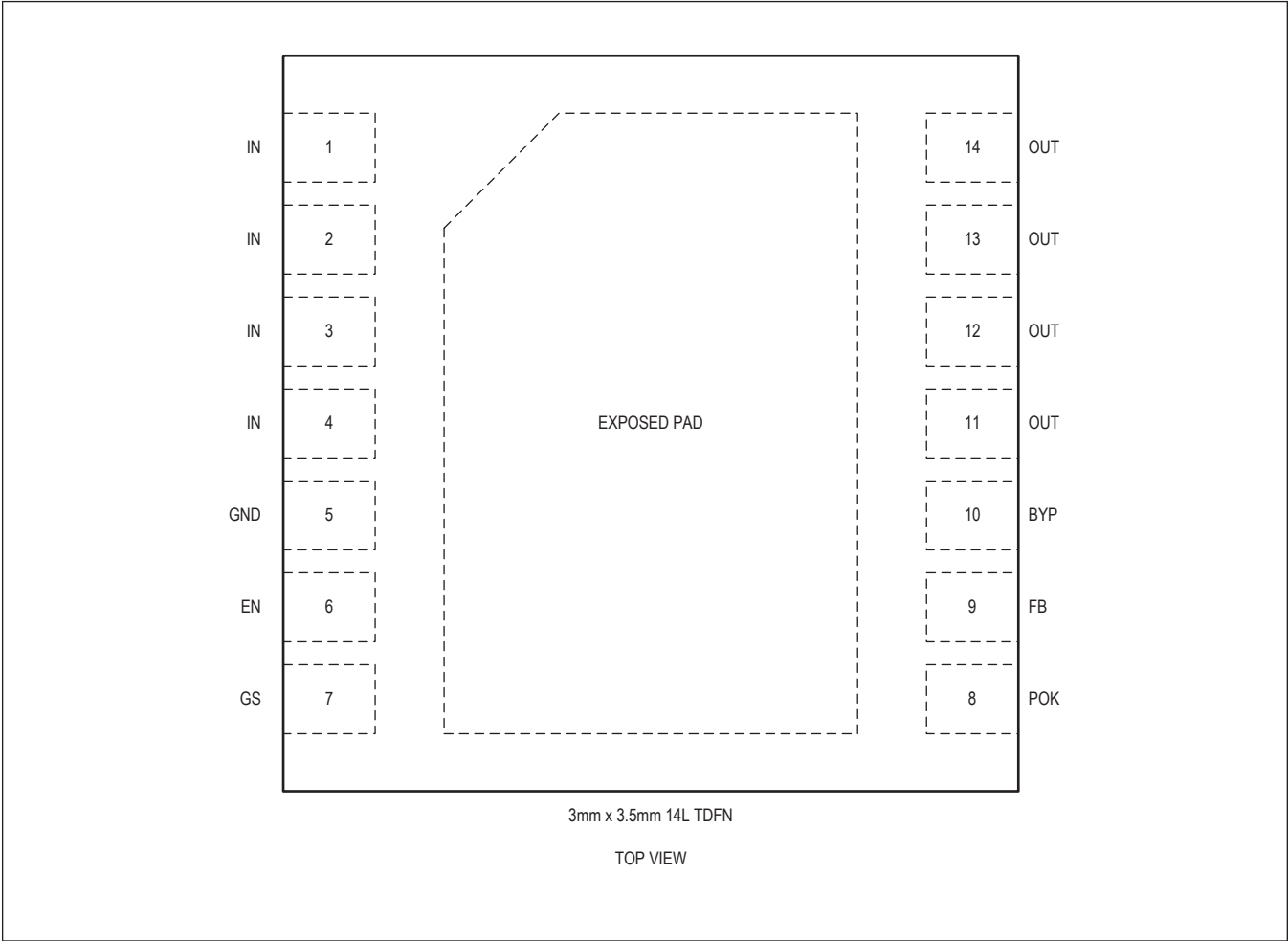


Pin Configurations

MAX25302A



MAX25302B



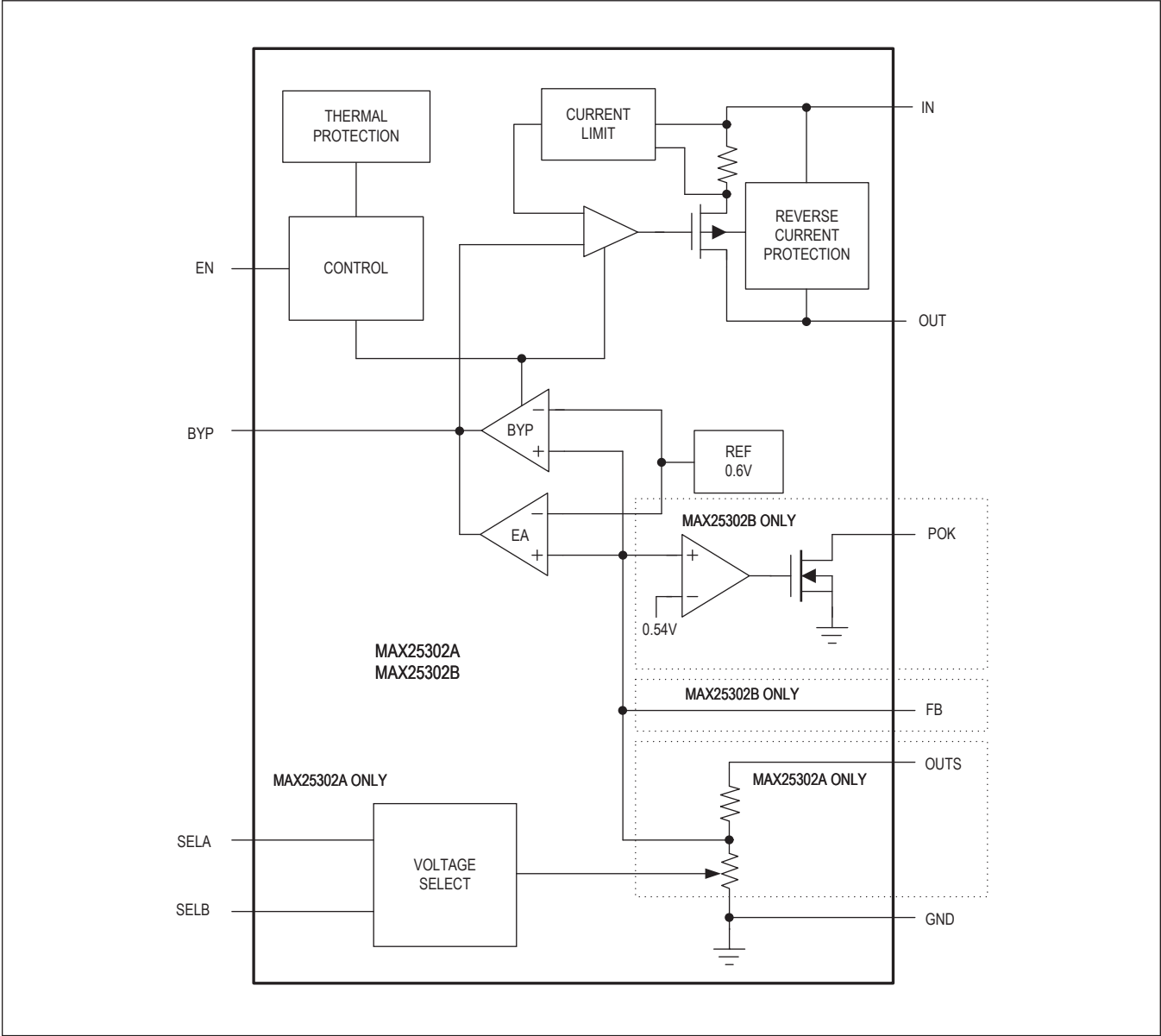
Pin Description

PIN		NAME	FUNCTION
MAX25302A	MAX25302B		
1, 2, 3, 4	1, 2, 3, 4	IN	Regulator Supply Input. Connect to a voltage between 1.7V and 5.5V and bypass with a 22μF capacitor from IN to GND.
5	5	GND	Regulator Ground. Connect IN and OUT bypass capacitor GND connections to this pin for best performance.
6	6	EN	Enable Input. Connect this pin to a logic signal to enable (V _{EN} high) or disable (V _{EN} low) the regulator output. Connect to IN to keep the output enable whenever a valid supply voltage is present.
7	—	SELA	Output Select Input. Connect to GND, IN, or Hi-Z to select one of three states. The states of the SELA and SELB pins are read when the device is enabled, and are used to select one of nine output voltages.
—	7	GS	Ground Sense. Connect GS to GND.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX25302A	MAX25302B		
8	—	SELB	Output Select Input. Connect to GND, IN, or Hi-Z to select one of three states. The states of the SELA and SELB pins are read when the device is enabled, and are used to select one of nine output voltages.
—	8	POK	Active-High Power-OK Output. Connect a pull-up resistor from this pin to a supply to create a reset signal that goes high after the regulator output has reached its regulation voltage.
9	—	OUTS	Output Voltage Sense Input. Connect to the load at a point where accurate regulation is required to eliminate resistive metal drops.
—	9	FB	Feedback Divider Input. Connect a resistor-divider string from OUT to GND with the midpoint tied to this pin to set the output voltage. In the Typical Application Circuits , $V_{OUT} = 0.6V \times (1 + R1/R2)$.
10	10	BYP	Bypass Capacitor Input. Connect a capacitor with a value from 0.001 μ F to 0.1 μ F between OUT and BYP to reduce output noise and set the regulator soft-start rate.
11, 12, 13, 14	11, 12, 13, 14	OUT	Regulator Output. Sources up to 2A at the output regulation voltage. Bypass with a 22 μ F (8 μ F minimum, including voltage derating) low-ESR (< 0.03 Ω) capacitor to GND.
EP	EP	EP	Exposed Pad (TDFN Only). Connect the exposed pad to a ground plane with low thermal resistance to ambient to provide best heat sinking.

Simplified Functional Diagram



Detailed Description

The MAX25302A/MAX25302B are high-performance pMOS linear regulators that are optimized for low noise, high-input-supply rejection, low dropout voltage, and small solution size. They can deliver up to a maximum load current of 2A while maintaining a low dropout voltage of 47mV. An enable input allows the regulator to be powered up and down, while an internal soft-start circuit controls the inrush current at the input. SELA and SELB inputs are provided on the A version for selecting one of nine output voltages and a power-OK output is provided on the B version for system power-up sequencing.

Enable (EN)

The MAX25302A/MAX25302B include an enable pin (EN). Pull EN low to shut down the output, or drive EN high to enable the output. If a separate shutdown signal is not available, connect EN to IN.

Bypass (BYP)

The capacitor connected from BYP to OUT filters noise at the reference, feedback resistors, and regulator input stage. It provides a high-speed feedback path for improved transient response. A 10nF capacitor rolls off noise at around 32Hz.

The slew rate of the output voltage during startup is also determined by the BYP capacitor. A 10nF capacitor sets the slew rate to 5V/ms. This startup rate results in a 110mA slew current drawn from the input at startup to charge 22μF output capacitance.

The BYP capacitor value can be adjusted from 1nF to 100nF to change the startup slew rate according to the following formula:

StartupSlewRate = $\frac{5V}{ms} \times \frac{10nF}{C_{BYP}}$

where C_{BYP} is in nF.

Note that this slew rate applies only at startup. Recovery from a short circuit will occur at a slew rate approximately 500 times slower.

Also, note that being a low-frequency filter node, BYP is sensitive to leakage. BYP leakage currents above 10nA cause measurable inaccuracy at the output and should be avoided.

Protection Features

The MAX25302A/MAX25302B are fully protected from an output short circuit by a current-limiting and thermal-overload circuit. If the output is shorted to GND, the output current is limited to 2.8A (typ). Under these conditions, the device quickly heats up. When the junction temperature reaches +165°C, a thermal-limit circuit shuts the output device off. Once the device cools to +150°C, the output turns back on in an attempt to reestablish regulation. If the fault persists, the output current cycles on and off as the junction temperature slews between +150°C and +165°C.

The MAX25302A/MAX25302B are also protected against reverse current when the output voltage is higher than the input. In the event that extra output capacitance is used at the output, a power down transient at the input would normally cause a large reverse current through a conventional regulator. The MAX25302A/MAX25302B include a reverse-voltage detector that trips when IN drops 10mV below OUT, shutting off the regulator and opening the pMOS body diode connection and preventing any reverse current.

Output Voltage Configuration (MAX25302A)

The MAX25302A has two configuration pins, SELA and SELB, that are read during power-up to determine the output regulation voltage.

Table 1. MAX25302A Output Configuration Table

V _{OUT} (V)	SELA	SELB
1.2	Hi-Z	IN
1.5	IN	Hi-Z

Table 1. MAX25302A Output Configuration Table (continued)

1.8	Hi-Z	GND
2.5	Hi-Z	Hi-Z
3.0	GND	GND
3.1	GND	IN
3.3	GND	Hi-Z
4.0	IN	GND
5.0	IN	IN

Output Voltage Configuration (MAX25302B)

The MAX25302B uses external feedback resistors to set the output regulation voltage as shown in the [Typical Operating Circuits](#). The output voltage can be set from 0.6V to 5.0V. Set the lower feedback resistor R2 to 300kΩ or less to minimize FB input bias current error. Then, calculate the value of the upper feedback resistor R1 as follows:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where V_{FB} is the feedback regulation voltage of 0.6V.

To set the output to 2.4V, for example, R1 should be:

$$R1 = 300k\Omega \times \left(\frac{2.4V}{0.6V} - 1 \right) = 900k\Omega$$

Power-OK (MAX25302B)

The MAX25302B includes an additional open-drain output, POK, that goes high to indicate that the output voltage is in regulation. Connect a pull-up resistor from this pin to an external supply. During startup, POK stays low until the output voltage rises to 91% (typ) of its regulation level. If an overload event occurs at the output, or the output is shutdown, POK goes low.

Input Capacitor

A 22μF ceramic capacitor is recommended for the input. Select a capacitor that does not degrade significantly over temperature and DC bias. Capacitors with X5R or X7R temperature characteristics generally perform well.

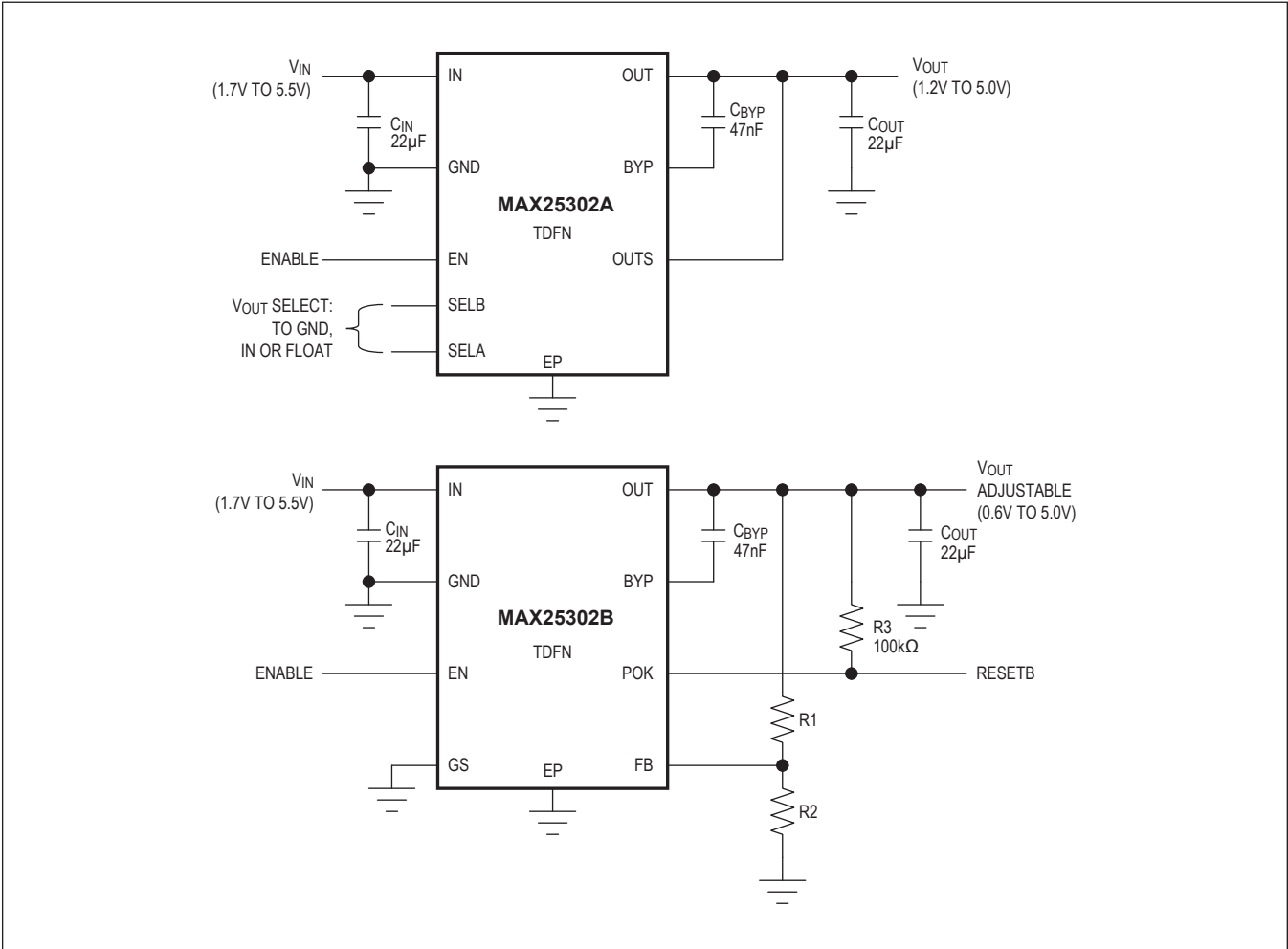
Output Capacitor

A minimum of 8μF capacitance is required at OUT to ensure stable operation. Select a ceramic capacitor that maintains its capacitance (8μF minimum) over temperature and DC bias. Capacitors with X5R or X7R temperature characteristics generally perform well.

Thermal Considerations

The MAX25302A/MAX25302B are packaged in a 14-pin, 3mm x 3.5mm TDFN package with an exposed paddle. The exposed paddle is the main thermal path for heat to escape the IC, and therefore, must be connected to a ground plane with thermal vias to allow heat to dissipate from the device. Thermal properties of the package are given in the [Package Information](#) section.

Typical Application Circuits



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	FEATURES
MAX25302AATD/V+	-40°C to +125°C	14-pin, 3mm x 3.5mm, TDFN	Pin-Selectable Output Voltage, Enable
MAX25302BATD/V+	-40°C to +125°C	14-pin, 3mm x 3.5mm, TDFN	External Resistor Feedback, POK Output with Delay, Enable

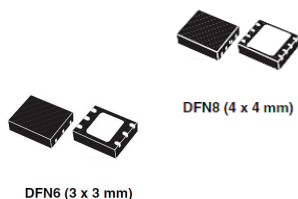
/V Denotes an automotive qualified part
+ Denotes a lead(Pb)-free/RoHS-compliant package.
Devices are also available in tape-and-reel packaging. Specify tape and reel by adding "T" to the part number when ordering.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/20	Initial release	—
1	1/23	Updated Pin Configuration, Pin Description table, Detailed Description, and Ordering Information table	7, 8, 9, 12, 13

Exhibit 3

2 A high PSRR ultra low drop linear regulator with reverse current protection



Features

- Input voltage from 1.25 V to 6.0 V
- Ultra low drop: 130 mV (typ.) at 2 A load
- 1 % output accuracy at 25 °C, 2 % in full temperature range
- High PSRR: 70 dB at 1 kHz
- Reverse current protection
- 2 A guaranteed output current
- Available in fixed and adjustable output voltage version from 0.5 V with 100 mV step
- Power Good
- Internal current and thermal limit
- Operating junction temperature range: -40 °C to 125 °C
- DFN6 (3 x 3 mm) and DFN8 (4 x 4 mm) packages

Applications

- Telecom infrastructure
- Medium power POL

Description

The **LD39200** provides 2 A of maximum current with an input voltage range from 1.25 V to 6.0 V, and a typical dropout voltage of 130 mV.

It is stable with ceramic capacitors on the output (10 µF).

Typical power supply rejection ratio is 70 dB at 1 kHz and starts to roll off at 20 kHz.

The enable logic control function puts the **LD39200** in shutdown mode, reducing the total current consumption to 10 nA (typ.).

Power Good flag is available on a dedicated pin.

The device also includes reverse current protection, short-circuit constant current limit and thermal protection.

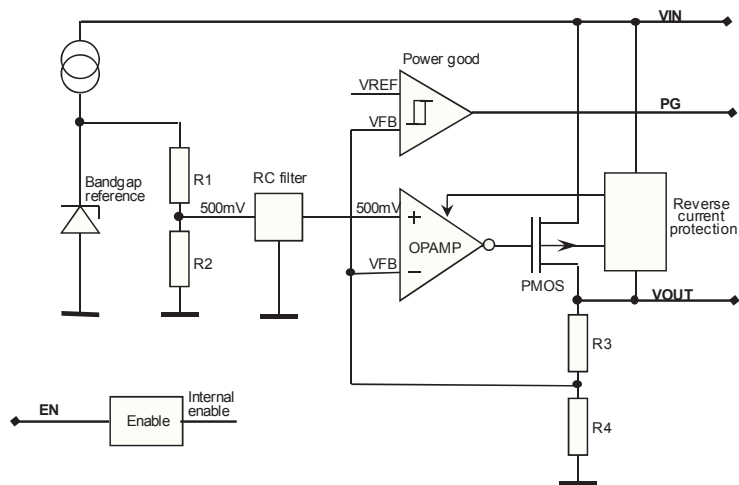
Typical applications are for Telecom infrastructure and consumer.

Maturity status link

[LD39200](#)

1 Block diagram

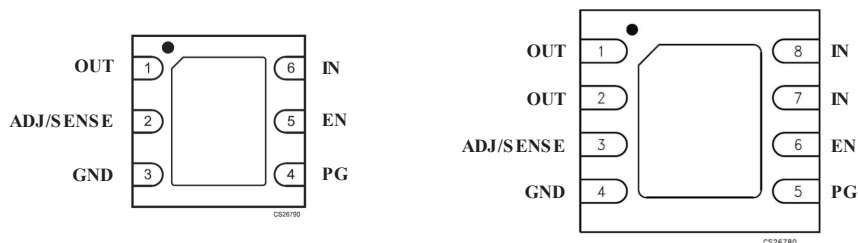
Figure 1. Block diagram



AM13907V1

2 Pin configuration and description

Figure 2. Pin configuration (top view)



AM13909V1

Table 1. DFN6 (3 x 3 mm) package pin description

Pin name	Pin number	Description
IN	6	Input voltage
GND	3	Ground
EN	5	Enable pin. The device is in OFF state when this pin is pulled low
ADJ/sense ⁽¹⁾	2	Adjustable pin on ADJ version can be connected to external resistor divider to set the output voltage. Output sense pin on the fixed version has to be connected to V_{OUT}
OUT	1	Output voltage
PG	4	Power Good
GND	Exposed pad	Exposed pad should be connected to GND

1. The output sense pin of the fixed version has to be connected to the output pin for proper operation.

Table 2. DFN8 (4 x 4 mm) package pin description

Pin name	Pin number	Description
IN ⁽¹⁾	7, 8	Input voltage
GND	4	Ground
EN	6	Enable pin. The device is in OFF state when this pin is pulled low
ADJ/sense ⁽²⁾	3	Adjustable pin on ADJ version can be connected to external resistor divider to set the output voltage. Output sense pin on the fixed version has to be connected to V_{OUT}
OUT ⁽³⁾	1, 2	Output voltage
PG	5	Power Good
GND	Exposed pad	Exposed pad should be connected to GND

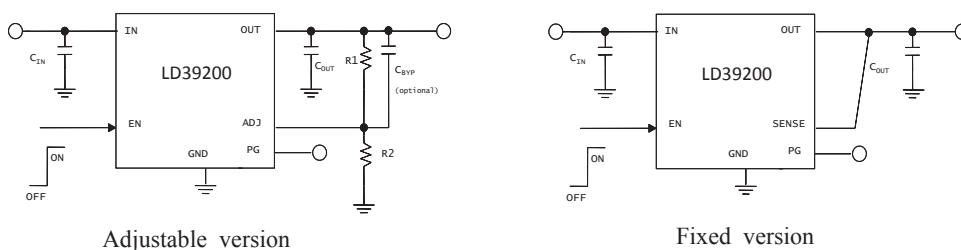
1. Both of input pins have to be connected together on the board.

2. The output sense pin of the fixed version has to be connected to the OUT pin for proper operation.

3. Both of output pins have to be connected together on the board.

3 Typical application

Figure 3. LD39200 typical application schematic



AM13909V1

Note: $R1$ and $R2$ are calculated according to the following formula: $R1 = R2 \times (V_{OUT} / V_{ADJ} - 1)$. Recommended value for C_{IN} and C_{OUT} is 10 μF .

4 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Input supply voltage	-0.3 to 7	V
V_{ADJ}	Adjustable voltage	-0.3 to 2	V
V_{OUT}/V_{SENSE}	Output voltage/output sense voltage	-0.3 to 7	V
I_{OUT}	Output current	Internally limited	A
EN	Enable pin voltage	-0.3 to 7	V
PG	Power Good pin voltage	-0.3 to 7	V
P_D	Power dissipation	Internally limited	W
ESD	Charge device model	±500	V
	Human body model	±2000	
T_{J-OP}	Operating junction temperature	-40 to 125	°C
T_{J-MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature	-55 to 150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Thermal data

Symbol	Parameter	DFN6 (3 x 3 mm)	DFN8 (4 x 4 mm)	Unit
R_{THJC}	Junction-to-case thermal resistance	10	4	°C/W
R_{THJA}	Junction-to- ambient thermal resistance	55	40	

5 Electrical characteristics

($T_J = 25\text{ }^{\circ}\text{C}$, $V_{IN} = V_{OUT} + 1\text{ V}$; $V_{OUT} = V_{ADJ}$; $C_{IN} = 10\text{ }\mu\text{F}$; $C_{OUT} = 10\text{ }\mu\text{F}$; $I_{OUT} = 10\text{ mA}$; $V_{EN} = V_{IN}$)

Table 5. Electrical characteristics, adjustable version

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range		1.25		6.0	V
V_{ADJ}	Adjustable pin voltage			0.5		V
	Adjustable pin voltage accuracy	$T_J = 25\text{ }^{\circ}\text{C}$	-1.0		1.0	%
		$-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$	-2.0		2.0	
I_{ADJ}	Adjustable pin current	$-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$		100		nA
$\Delta V_{ADJ}\% / \Delta V_{IN}$	Static line regulation	$V_{OUT} + 1\text{ V} < V_{IN} < 6.0\text{ V}$; $T_J = 25\text{ }^{\circ}\text{C}$		0.01		% / V
		$-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$			0.2	
$\Delta V_{ADJ}\% / \Delta I_{OUT}$	Static load regulation	$0\text{ mA} < I_{OUT} < 2\text{ A}$; $T_J = 25\text{ }^{\circ}\text{C}$		0.1		% / A
		$-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$			0.4	
V_{DROP}	Dropout voltage ⁽¹⁾	$V_{IN} = 1.4\text{ V}$; $I_{OUT} = 1\text{ A}$; $-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$		120	250	mV
		$V_{IN} = 2.5\text{ V}$; $I_{OUT} = 2\text{ A}$; $-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$		135	250	
		$V_{IN} = 5.3\text{ V}$; $I_{OUT} = 2\text{ A}$; $-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$		110	250	
eN	Output noise voltage	$V_{OUT} = V_{ADJ}$; $f = 10\text{ Hz to } 100\text{ kHz}$		45		$\mu\text{V}_{RMS} / V_{OUT}$
eN	Output noise voltage	$V_{IN} = V_{OUT} + 0.4\text{ V}$; $I_{OUT} = 700\text{ mA}$; $C_{IN} = C_{OUT} = 10\text{ }\mu\text{F}$, $R2 = 10\text{ k}\Omega$, $R1 = (V_{OUT} - 0.5) \times 20\text{ k}\Omega$, $C_{byp} = 470\text{ nF}$		24		μV_{RMS}
SVR	Supply voltage rejection	$V_{OUT} = 1.8\text{ V}$; $V_{IN} = V_{OUT} + 0.5\text{ V}$; $C_{OUT} = 10\text{ }\mu\text{F}$; $I_{OUT} = 10\text{ mA}$; $T_J = 25\text{ }^{\circ}\text{C}$; $f = 1\text{ kHz}$		70		dB
		$V_{OUT} = 1.8\text{ V}$; $V_{IN} = V_{OUT} + 0.5\text{ V}$; $C_{OUT} = 10\text{ }\mu\text{F}$; $I_{OUT} = 10\text{ mA}$; $T_J = 25\text{ }^{\circ}\text{C}$; $f = 100\text{ kHz}$		50		
		$V_{OUT} = 1.8\text{ V}$; $V_{IN} = V_{OUT} + 0.5\text{ V}$; $C_{OUT} = 10\text{ }\mu\text{F}$; $I_{OUT} = 10\text{ mA}$; $T_J = 25\text{ }^{\circ}\text{C}$; $f = 500\text{ kHz}$		50		dB
		$V_{OUT} = 1.8\text{ V}$; $V_{IN} = V_{OUT} + 0.5\text{ V}$; $C_{OUT} = 10\text{ }\mu\text{F}$; $I_{OUT} = 10\text{ mA}$; $T_J = 25\text{ }^{\circ}\text{C}$; $f = 1\text{ MHz}$		40		

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_Q	Quiescent current	$I_{OUT} = 0\text{ A}$		100		μA
		$I_{OUT} = 0\text{ A}; -40\text{ }^\circ\text{C} < T_J < 125\text{ }^\circ\text{C}$			300	
		$I_{OUT} = 2\text{ A};$		1		mA
		$I_{OUT} = 2\text{ A}; -40\text{ }^\circ\text{C} < T_J < 125\text{ }^\circ\text{C}$			3	
	Shutdown current	$V_{EN} = 0, V_{IN} = 6\text{ V}$		10		nA
I_{SC}	Short-circuit current	$V_{OUT} = 0\text{ V}$		3.5		A
I_{MIN}	Minimum output current				0	A
V_{EN}	Enable input logic low	$1.25\text{ V} < V_{IN} < 6.0\text{ V}$			0.5	V
	Enable input logic high	$-40\text{ }^\circ\text{C} < T_J < 125\text{ }^\circ\text{C}$	1.2			
I_{EN}	Enable pin input current	$V_{EN} = V_{IN}; 1.25 < V_{IN} < 6.0\text{ V}$		10		nA
PG	Power Good output threshold	Rising edge		$0.92 \cdot V_{OUT}$		V
		Falling edge		$0.8 \cdot V_{OUT}$		
	Power Good output voltage low	$I_{SINK} = 6\text{ mA}$ open drain output			0.4	
T_{SHDN}	Thermal shutdown			170		$^\circ\text{C}$
	Hysteresis			20		

1. Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value; this specification does not apply to nominal output voltages below 1.2 V.

($T_J = 25\text{ }^\circ\text{C}$, $V_{IN} = V_{OUT} + 1\text{ V}$; $C_{IN} = 10\text{ }\mu\text{F}$; $C_{OUT} = 10\text{ }\mu\text{F}$; $I_{OUT} = 10\text{ mA}$; $V_{EN} = V_{IN}$)

Table 6. Electrical characteristics, fixed version

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range		1.25		6.0	V
V_{OUT}	Output voltage accuracy	$T_J = 25\text{ }^\circ\text{C}$	-1.0		1.0	$\%$
		$-40\text{ }^\circ\text{C} < T_J < 125\text{ }^\circ\text{C}$	-2.0		2.0	
$\Delta V_{ADJ}\% / \Delta V_{IN}$	Static line regulation	$V_{OUT} + 1\text{ V} < V_{IN} < 6.0\text{ V};$ $T_J = 25\text{ }^\circ\text{C}$		0.01		$\%/V$
		$-40\text{ }^\circ\text{C} < T_J < 125\text{ }^\circ\text{C}$			0.1	
$\Delta V_{ADJ}\% / \Delta I_{OUT}$	Static load regulation	$0\text{ mA} < I_{OUT} < 2\text{ A}; T_J = 25\text{ }^\circ\text{C}$		0.05		$\%/A$
		$-40\text{ }^\circ\text{C} < T_J < 125\text{ }^\circ\text{C}$			0.4	
V_{DROP}	Dropout voltage	$V_{OUT} = 3.3\text{ V}; I_{OUT} = 2\text{ A};$ $-40\text{ }^\circ\text{C} < T_J < 125\text{ }^\circ\text{C}$		130	250	mV
e_N	Output noise voltage	$V_{OUT} = 2.5\text{ V}; f = 10\text{ Hz to } 100\text{ kHz}$		40		$\mu\text{V}_{RMS} / V_{OUT}$

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
SVR	Supply voltage rejection	$V_{OUT} = 1.8 \text{ V}$; $V_{IN} = V_{OUT} + 0.5 \text{ V}$; $C_{OUT} = 10 \text{ }\mu\text{F}$; $I_{OUT} = 10 \text{ mA}$; $T_J = 25 \text{ }^\circ\text{C}$; $f = 1 \text{ kHz}$		70		dB
		$V_{OUT} = 1.8 \text{ V}$; $V_{IN} = V_{OUT} + 0.5 \text{ V}$; $C_{OUT} = 10 \text{ }\mu\text{F}$; $I_{OUT} = 10 \text{ mA}$; $T_J = 25 \text{ }^\circ\text{C}$; $f = 100 \text{ kHz}$		50		
		$V_{OUT} = 1.8 \text{ V}$; $V_{IN} = V_{OUT} + 0.5 \text{ V}$; $C_{OUT} = 10 \text{ }\mu\text{F}$; $I_{OUT} = 10 \text{ mA}$; $T_J = 25 \text{ }^\circ\text{C}$; $f = 500 \text{ kHz}$		50		
		$V_{OUT} = 1.8 \text{ V}$; $V_{IN} = V_{OUT} + 0.5 \text{ V}$; $C_{OUT} = 10 \text{ }\mu\text{F}$; $I_{OUT} = 10 \text{ mA}$; $T_J = 25 \text{ }^\circ\text{C}$; $f = 1 \text{ MHz}$		40		
I_Q	Quiescent current	$I_{OUT} = 0 \text{ A}$		100		μA
		$I_{OUT} = 0 \text{ A}$; $-40 \text{ }^\circ\text{C} < T_J < 125 \text{ }^\circ\text{C}$			300	
		$I_{OUT} = 2 \text{ A}$;		1		mA
		$I_{OUT} = 2 \text{ A}$; $-40 \text{ }^\circ\text{C} < T_J < 125 \text{ }^\circ\text{C}$			3	
	Shutdown current	$V_{EN} = 0$, $V_{IN} = 6 \text{ V}$		50		nA
I_{SC}	Short-circuit current	$V_{OUT} = 0 \text{ V}$		3.5		A
I_{MIN}	Minimum output current				0	A
V_{EN}	Enable input logic low	$1.25 \text{ V} < V_{IN} < 6.0 \text{ V}$			0.5	V
	Enable input logic high	$-40 \text{ }^\circ\text{C} < T_J < 125 \text{ }^\circ\text{C}$	1.2			
I_{EN}	Enable pin input current	$V_{EN} = V_{IN}$; $1.25 < V_{IN} < 6.0 \text{ V}$		10		nA
PG	Power Good output threshold	Rising edge		$0.92 \cdot V_{OUT}$		V
		Falling edge		$0.8 \cdot V_{OUT}$		
	Power Good output voltage low	$I_{sink} = 6 \text{ mA}$ open drain output			0.4	
T_{SHDN}	Thermal shutdown			170		$^\circ\text{C}$
	Hysteresis			20		

6 Application information

6.1 Thermal and short-circuit protections

The LD39200 is self-protected from short-circuit conditions and overtemperature. When the output load is higher than the one supported by the device, the output current rises until the limit of typically 3.5 A is reached; at this point the current is kept constant even when the load impedance is zero. The thermal protection acts when the junction temperature reaches 170 °C. The IC enters the shutdown status. As soon as the junction temperature falls again below 150 °C the device starts working again. In order to calculate the maximum power the device can dissipate, keeping the junction temperature below T_{J-OP} , the following formula is used:

$$P_{DMAX} = (125 - T_{AMB}) / R_{THJ} - A \quad (1)$$

6.2 Output voltage setting for ADJ version

In the adjustable version, the output voltage can be set from 0.5 V up to the input voltage minus the voltage drop across the pass transistor (dropout voltage), by connecting a resistor divider between the ADJ pin and the output, allowing remote voltage sensing. The resistor divider can be selected using the following equation:

$$V_{OUT} = V_{ADJ} (1 + R1 / R2), \text{ with } V_{ADJ} = 0.5 V (typ.) \quad (2)$$

6.3 Enable pin

The LD39200 features an enable function. When the EN voltage is higher than 1.2 V the device is ON, and if it is lower than 0.5 V the device is OFF. In shutdown mode, the total current consumption is 10 nA (typ). The EN pin does not have an internal pull-up, therefore it cannot be left floating if it is not used.

6.4 Power Good pin (PG)

Some applications require a flag showing that the output voltage is in the correct range. Power Good threshold depends on the output voltage. When the output voltage is higher than $0.92 * V_{OUT(nom)}$, the PG pin goes to high impedance. If the output voltage is below $0.80 * V_{OUT(nom)}$ the PG pin goes to low impedance. If the device works well, the PG pin is at high impedance.

6.5 Reverse current protection

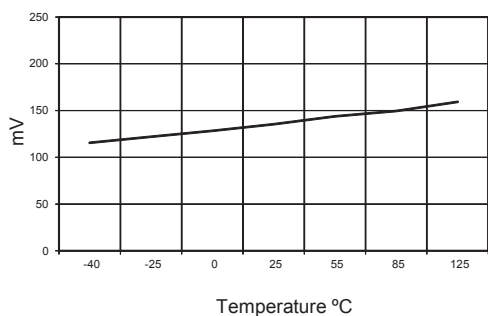
The device avoids the reverse current to flow from the output to the input during any operating condition (EN = 0 or EN = 1, $V_{IN} > V_{OUT} + V_{DROP}$). During fast turn-on/off this function prevents a big current from flowing to the input. Moreover it is used to avoid the reverse current to flow from the output pin to the input one, when other power supplies, providing a voltage higher than the input voltage, are connected to the output pin. If a power supply, providing a voltage lower than LDO output voltage, is connected to OUT pin, LDO works in current protection, causing high power dissipation inside the device.

When the device is disabled (EN = low) and $V_{OUT} > 0 V$, a small current (few μA) is sunk from the OUT pin.

7 Typical performance characteristics

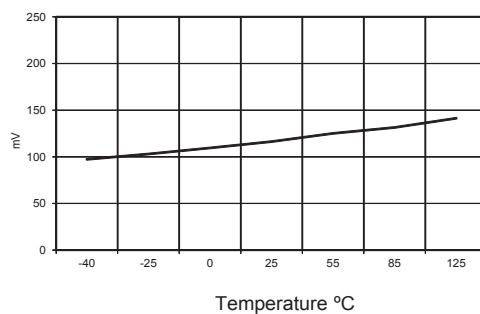
(The following plots are referred to the typical application circuit and, unless otherwise noted, at $T_A = 25\text{ }^{\circ}\text{C}$)

Figure 4. Dropout voltage vs. temperature
($V_{in} = 1.3\text{ V}$, $I_{out} = 1\text{ A}$)



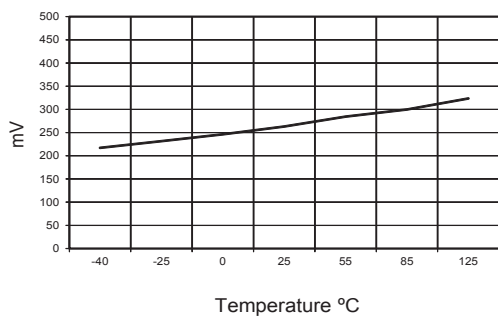
AM13910V1

Figure 5. Dropout voltage vs. temperature
($V_{in} = 1.4\text{ V}$, $I_{out} = 1\text{ A}$)



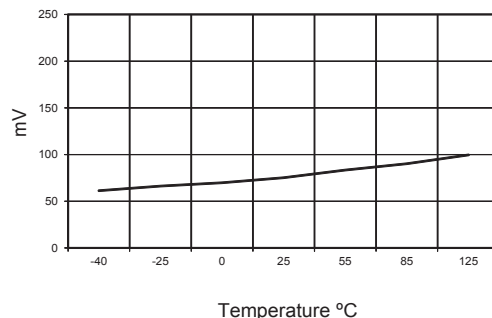
AM13911V1

Figure 6. Dropout voltage vs. temperature
($V_{in} = 1.4\text{ V}$, $I_{out} = 2\text{ A}$)

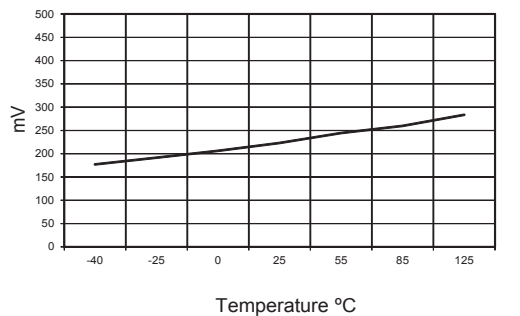


AM13912V1

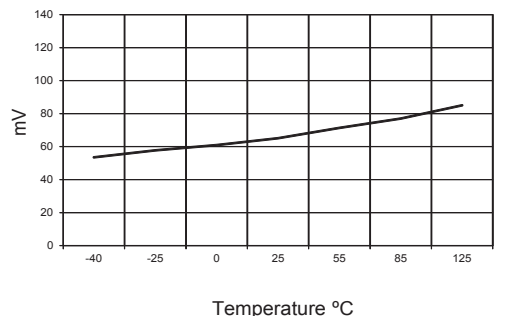
Figure 7. Dropout voltage vs. temperature
($V_{in} = 1.5\text{ V}$, $I_{out} = 1\text{ A}$)



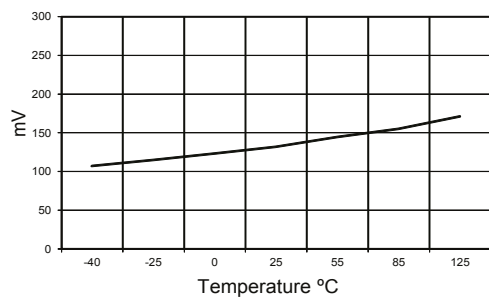
AM13913V1

Figure 8. Dropout voltage vs. temperature
 ($V_{in} = 1.5\text{ V}$, $I_{out} = 2\text{ A}$)


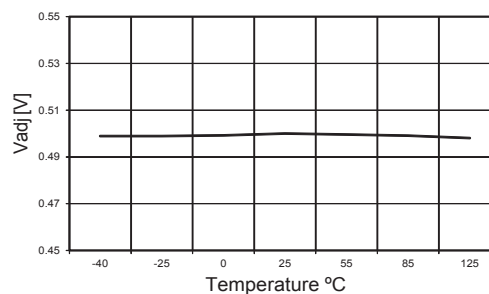
AM13914V1

Figure 9. Dropout voltage vs. temperature
 ($V_{in} = 2.5\text{ V}$, $I_{out} = 1\text{ A}$)


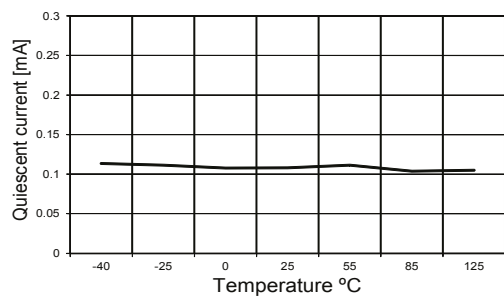
AM13915V1

Figure 10. Dropout voltage vs. temperature
 ($V_{in} = 2.5\text{ V}$, $I_{out} = 2\text{ A}$)


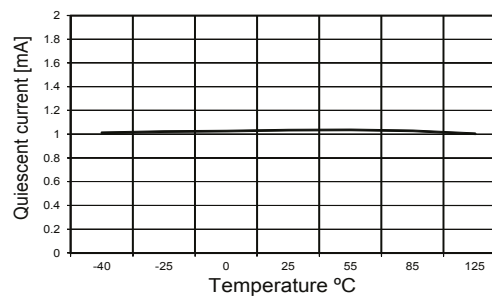
AM13916V1

Figure 11. Reference voltage vs. temperature
 ($V_{in} = 1.5\text{ V}$, $I_{out} = 10\text{ mA}$)


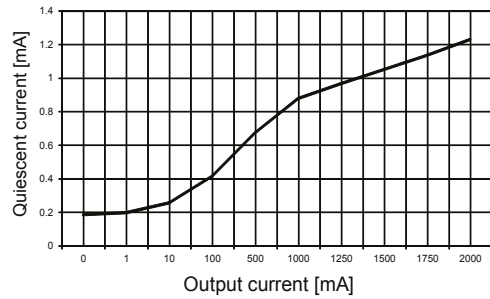
AM13917V1

Figure 12. Quiescent current vs. temperature
 ($V_{in} = 1.5\text{ V}$, $I_{out} = 0\text{ mA}$)


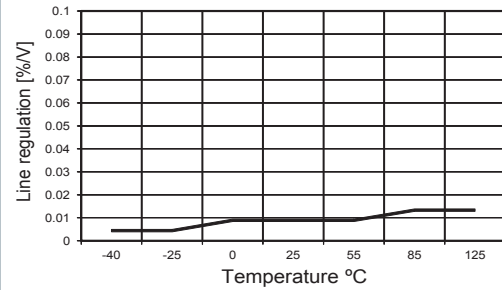
AM13918V1

Figure 13. Quiescent current vs. temperature
 ($V_{in} = 1.5\text{ V}$, $I_{out} = 2\text{ A}$)


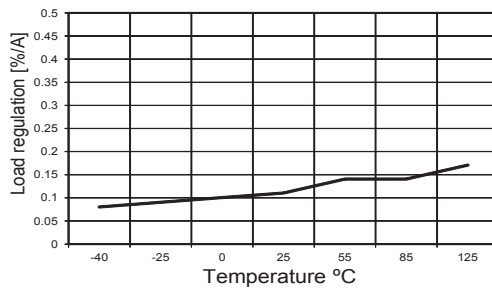
AM13919V1

Figure 14. Quiescent current vs. output current


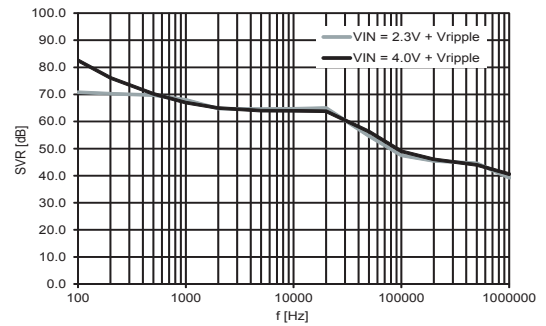
AM13920V2

Figure 15. Line regulation vs. temperature
 $(1.5\text{ V} \leq V_{in} \leq 6\text{ V}, I_{out} = 10\text{ mA})$


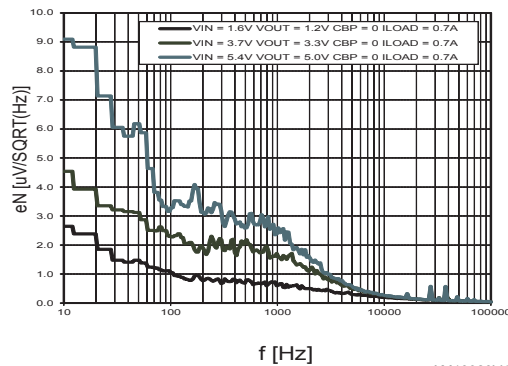
AM13920V1

Figure 16. Load regulation vs. temperature
 $(V_{in} = 1.5\text{ V}, 0 < I_{out} < 2\text{ A})$


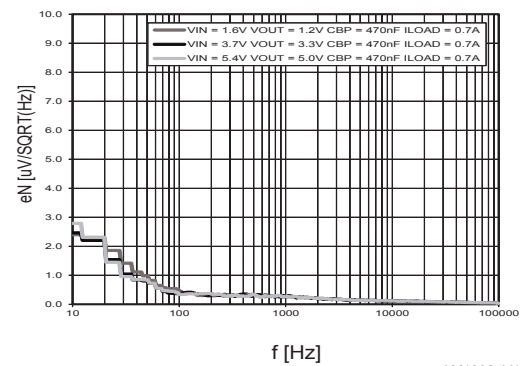
AM13921V1

Figure 17. SVR vs. frequency


AM13922V1

Figure 18. Noise spectral density (no Cbyp)


AM13923V1

Figure 19. Noise spectral density (Cbyp = 470 nF)


AM13924V1

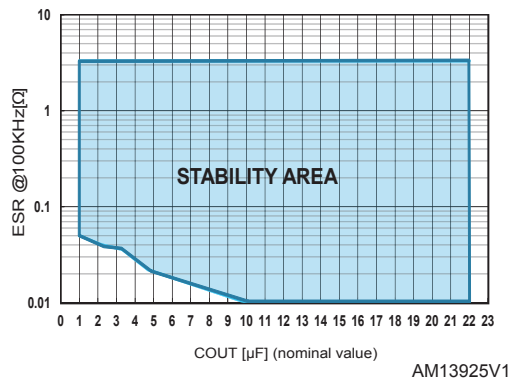
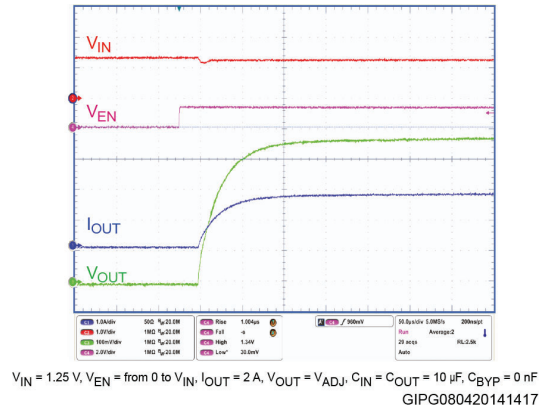
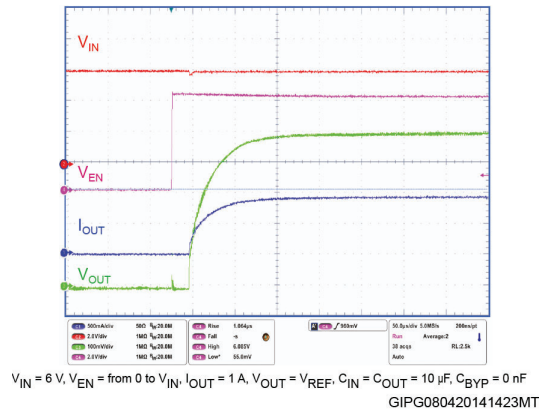
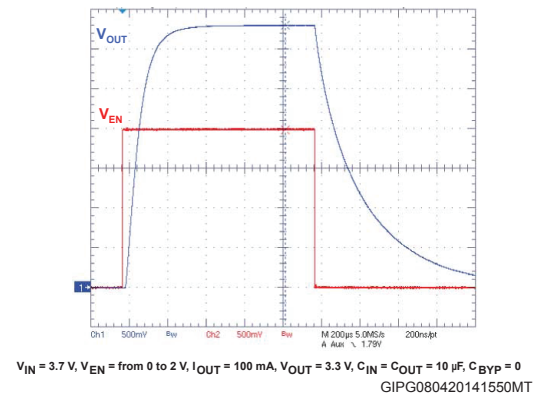
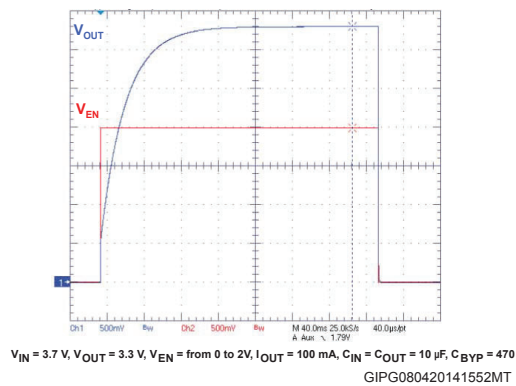
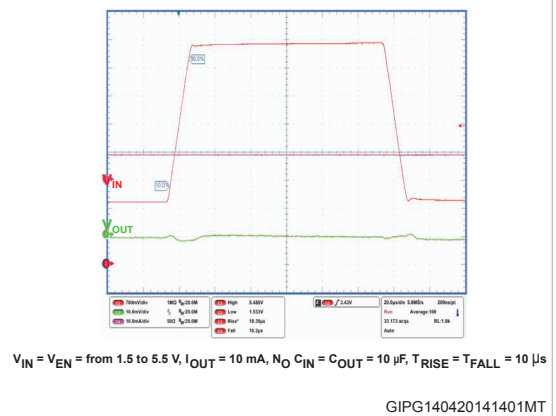
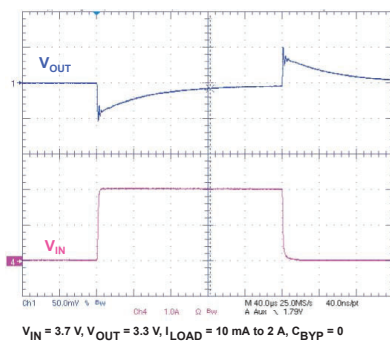
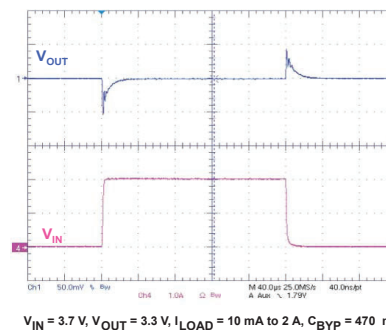
Figure 20. Stability plan

Figure 21. Enable startup, $V_{IN} = 1.25\text{ V}$, $I_{OUT} = 2\text{ A}$

Figure 22. Enable startup, $V_{IN} = 6\text{ V}$, $I_{OUT} = 2\text{ A}$

Figure 23. Enable startup, no Cbyp

Figure 24. Enable startup, $C_{byp} = 470\text{ nF}$

Figure 25. Line transient


Figure 26. Load transient, no Cbyp


GIPG140420141403MT

Figure 27. Load transient, Cbyp = 470 nF


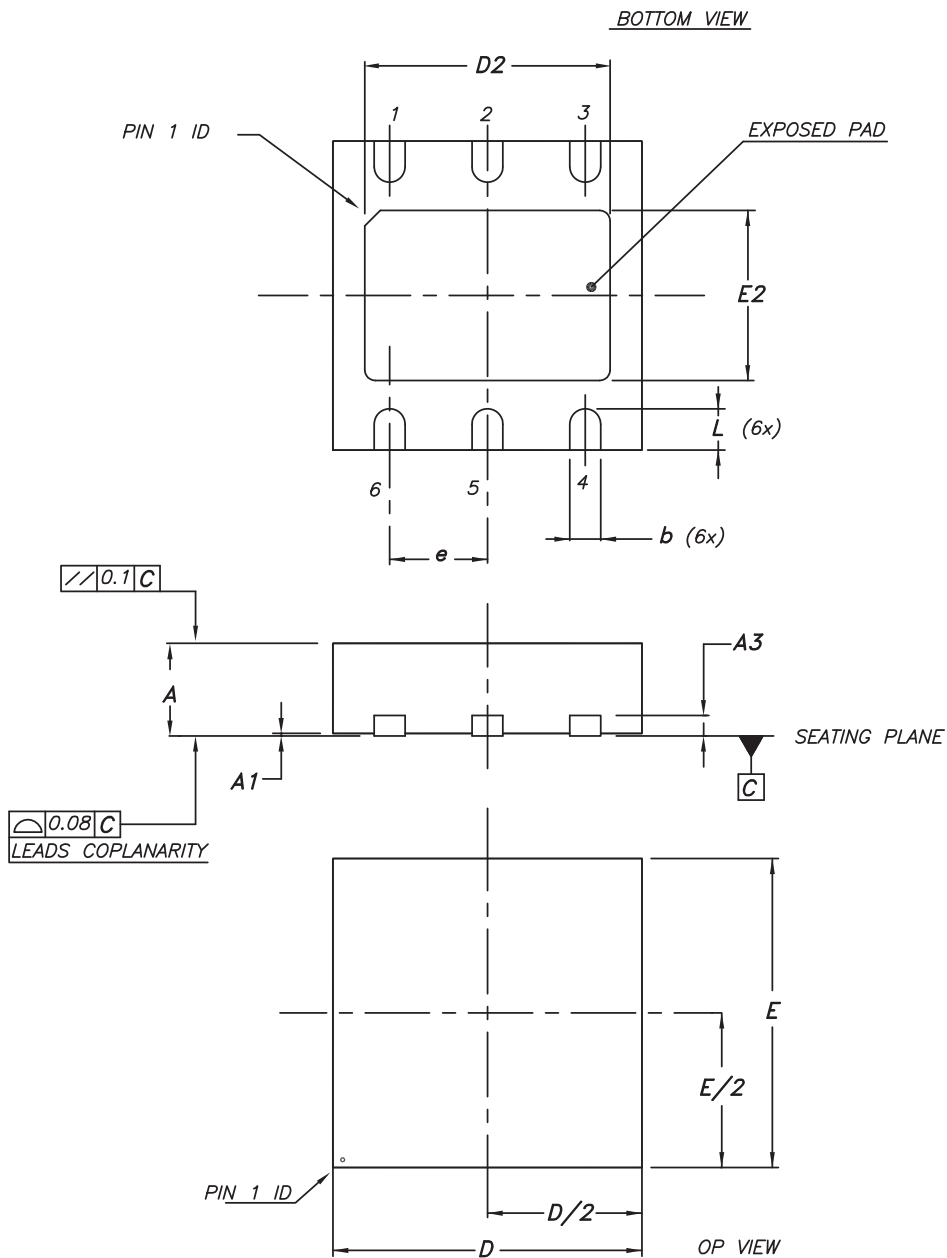
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8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

8.1 DFN6 (3 x 3 mm) mechanical data

Figure 28. DFN6 (3 x 3 mm) package outline

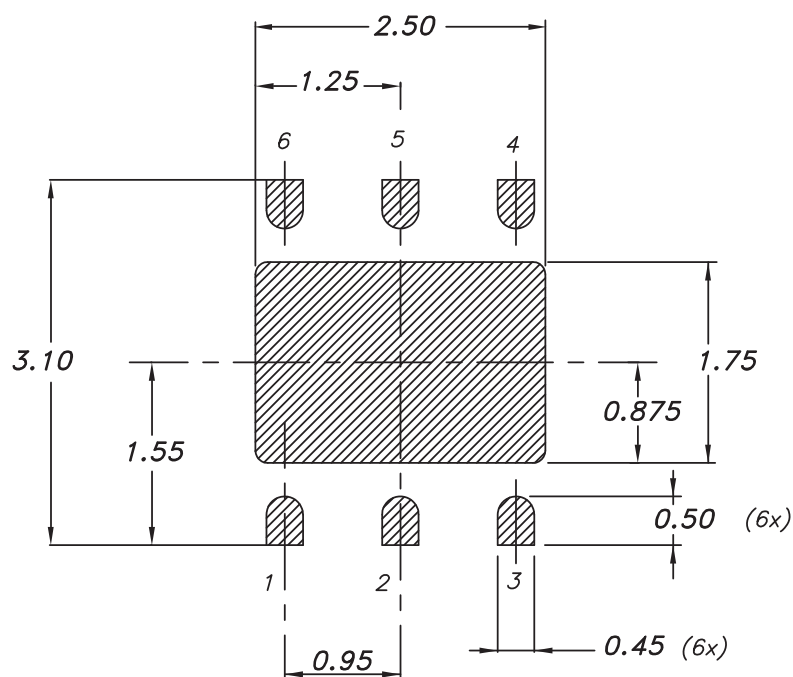


7946637_C

Table 7. DFN6 (3 x 3 mm) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1
A1	0	0.02	0.05
A3		0.20	
b	0.23		0.45
D	2.90	3	3.10
D2	2.23		2.50
E	2.90	3	3.10
E2	1.50		1.75
e		0.95	
L	0.30	0.40	0.50

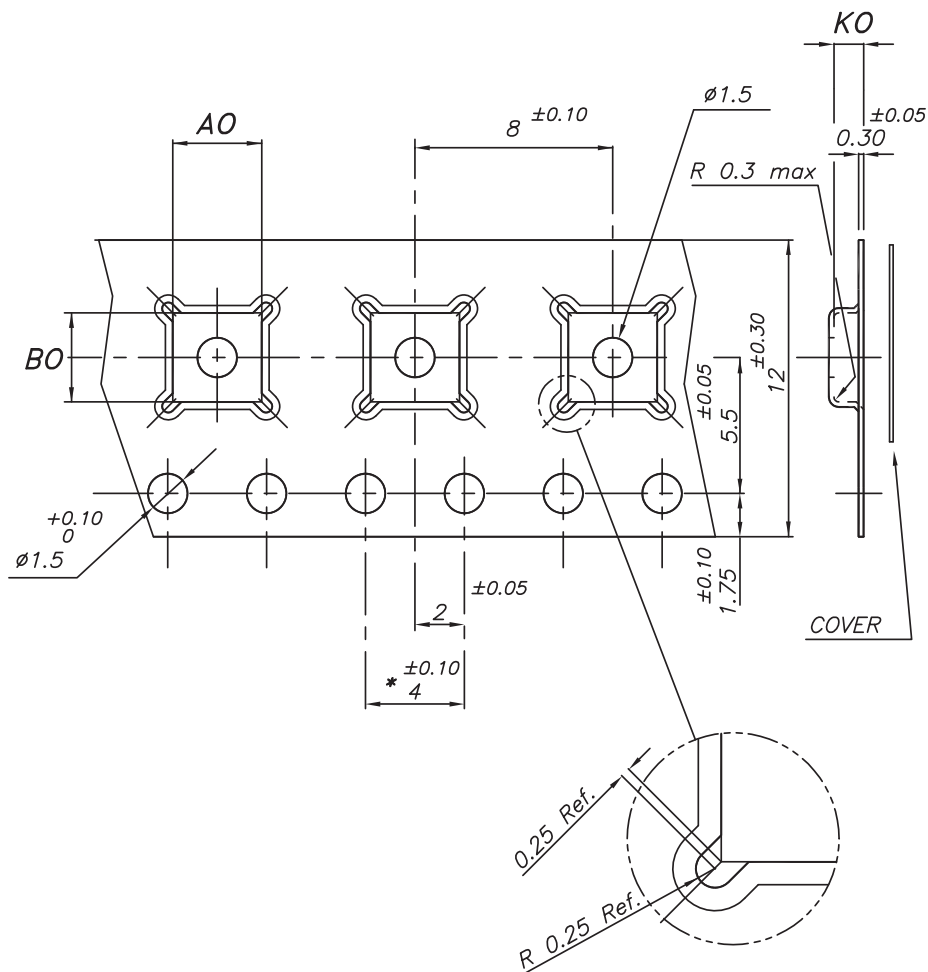
Figure 29. DFN6 (3 x 3 mm) recommended footprint (all dimensions are in mm)



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8.2 DFN6 (3 x 3 mm) tape and reel mechanical data

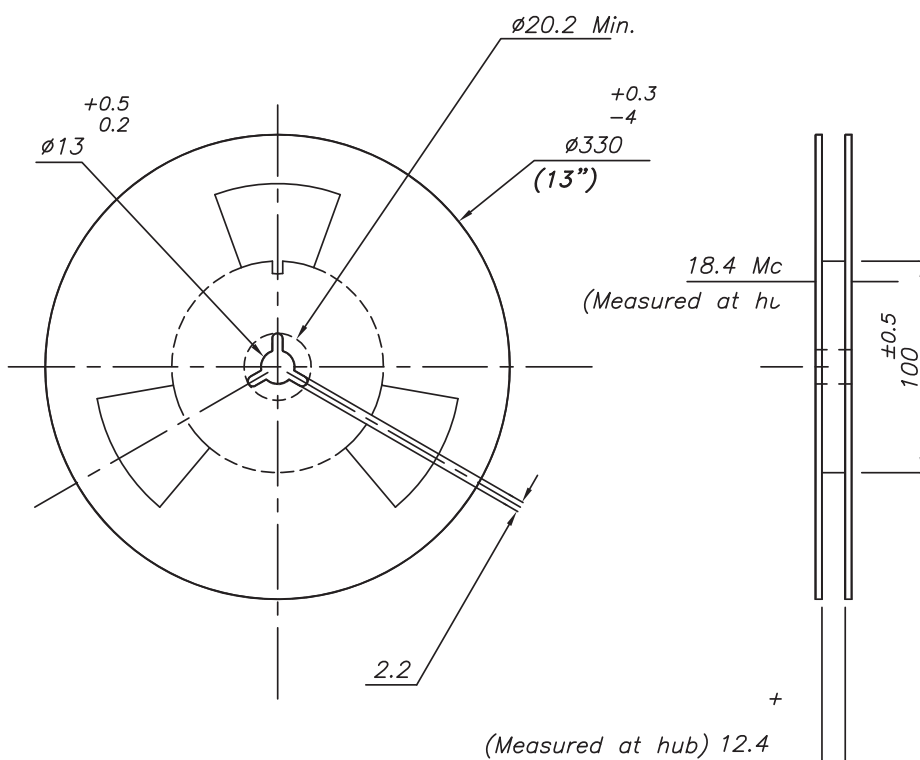
Figure 30. DFN6 (3 x 3 mm) tape outline



* ± 0.10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.20

7875978_N

Figure 31. DFN6 (3 x 3 mm) reel outline



7875978_N

Table 8. DFN6 (3 x 3 mm) tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A0	3.20	3.30	3.40
B0	3.20	3.30	3.40
K0	1	1.10	1.20

8.3 DFN8 (4 x 4 mm) mechanical data

Figure 32. DFN8 (4 x 4 mm) package outline

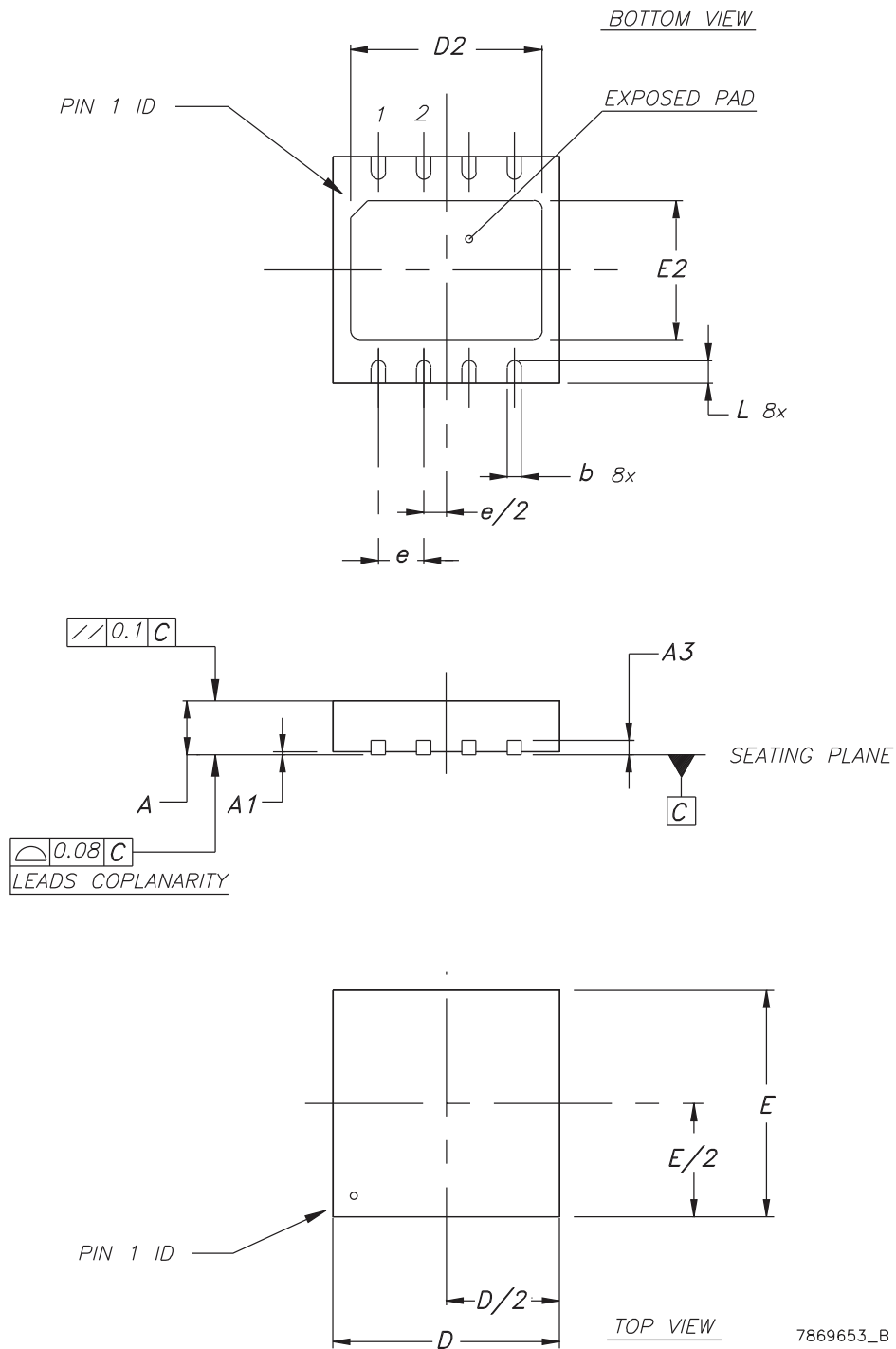
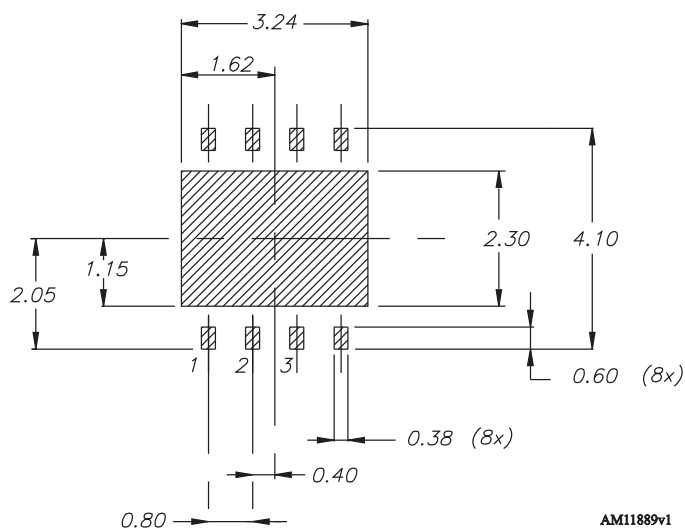


Table 9. DFN8 (4 x 4 mm) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1
A1	0	0.02	0.05
A3		0,20	
b	0.23	0.30	0.38
D	3.90	4	4.10
D2	2.82	3	3.23
E	3.90	4	4.10
E2	2.05	2.20	2.30
e		0.80	
L	0.40	0.50	0.60

Figure 33. DFN8 (4 x 4 mm) recommended footprint (all dimensions are in mm)



8.4 DFN8 (4 x 4 mm) reel mechanical data

Figure 34. DFN8 (4 x 4 mm) tape outline (all dimensions are in mm)

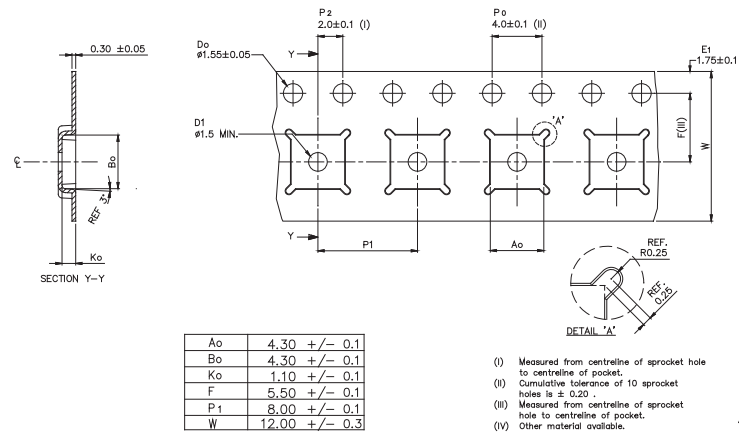
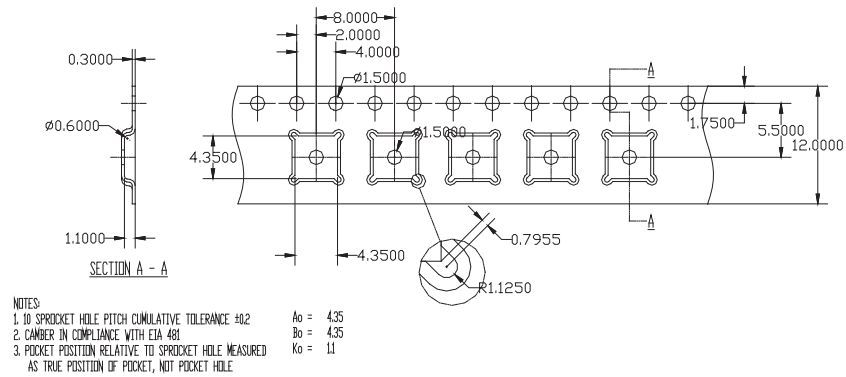
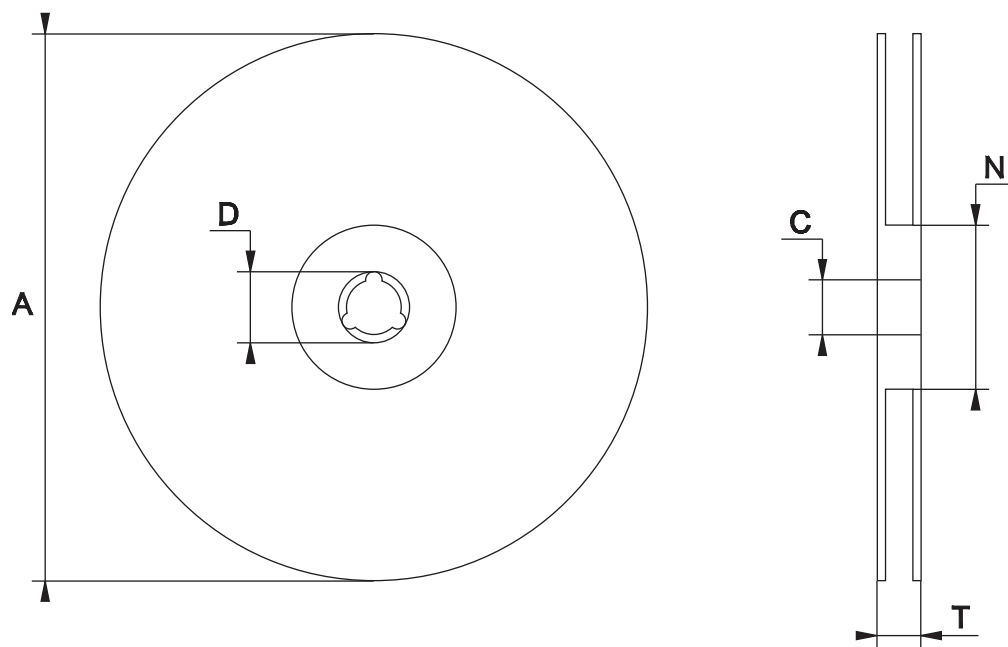


Figure 35. DFN8 (4 x 4 mm) reel outline



Note: Drawing not in scale

Table 10. DFN8 (4 x 4 mm) reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			330
C	12.8	13.0	13.2
D	20.2		
N	60		
T			22.4

9 Ordering information

Table 11. Order codes

DFN6 (3 x 3 mm)	DFN8 (4 x 4 mm)	Output voltage
LD39200PUR	LD39200DPUR	ADJ
LD39200PU33R		3.3 V

Revision history

Table 12. Document revision history

Date	Revision	Changes
08-Jul-2014	1	Initial release.
06-Jul-2017	2	Updated Table 11: "Order codes". Minor text changes.
17-Sep-2018	3	Updated note Section 3 Typical application .

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Exhibit 4

Description

The AP7331 is a 300mA, adjustable and fixed output voltage, low dropout linear regulator. The device included pass element, error amplifier, band-gap, current limit and thermal shutdown circuitry. The device is turned on when EN pin is set to logic high level.

The characteristics of low dropout voltage and low quiescent current make it suitable for low power applications, for example, battery powered devices. The typical quiescent current is approximately 65µA.

Built-in current-limit and thermal-shutdown functions prevent IC from damage in fault conditions.

The AP7331 is available in SOT25 and DFN2020-6 packages.

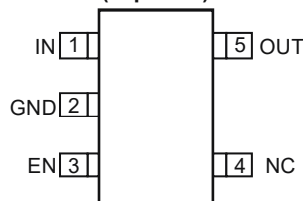
Features

- 300mA Low Dropout Regulator with EN
- Very low I_Q over full load: 65µA
- Wide input voltage range: 2V to 6V
- Wide adjustable output: 0.8V to 5.0V
- Fixed output options: 1.0V to 3.3V
- PSRR: 65dB typical at 100Hz
- Fast start-up time: 80µs
- Stable with low ESR, 1µF ceramic output capacitor
- Excellent Load/Line Transient Response
- Low dropout: 300mV typical at 300mA
- Current limit protection
- Short circuit protection
- Thermal shutdown protection
- Ambient temperature range: -40°C to 85°C
- SOT25 and DFN2020-6: Available in "Green" Molding Compound (No Br, Sb)
- Lead Free Finish/RoHS Compliant (Note 1)

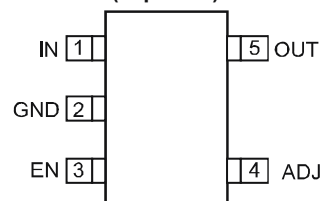
Notes: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at http://www.diodes.com/products/lead_free.html

Pin Assignments

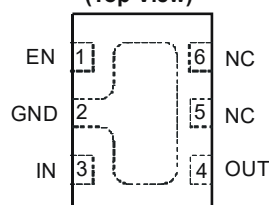
SOT25 (Fixed Output)
(Top View)



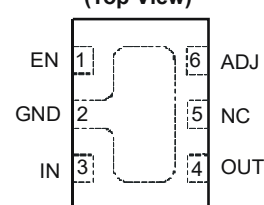
SOT25 (ADJ Output)
(Top View)



DFN2020-6 (Fixed Output)
(Top View)



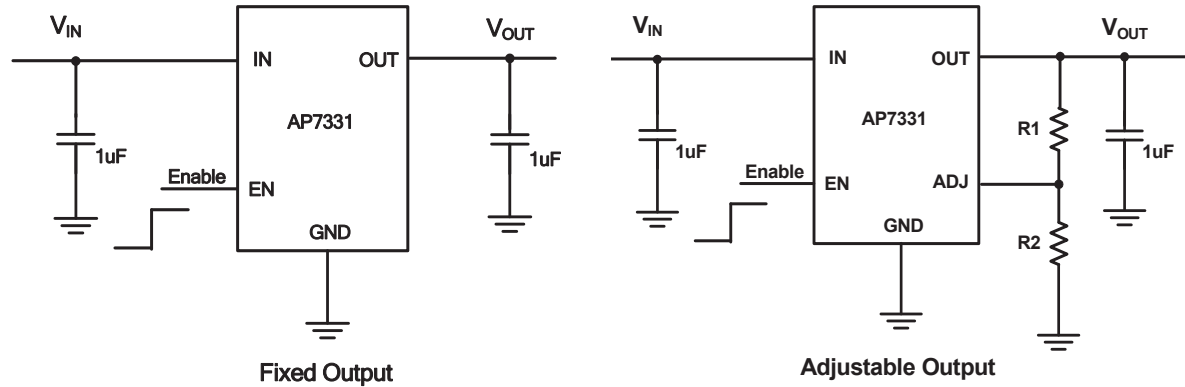
DFN2020-6 (ADJ Output)
(Top View)



Applications

- XDSL Routers
- Wireless LAN Cards
- Desktop and Notebook Computers
- Battery Powered Equipments

Typical Application Circuit

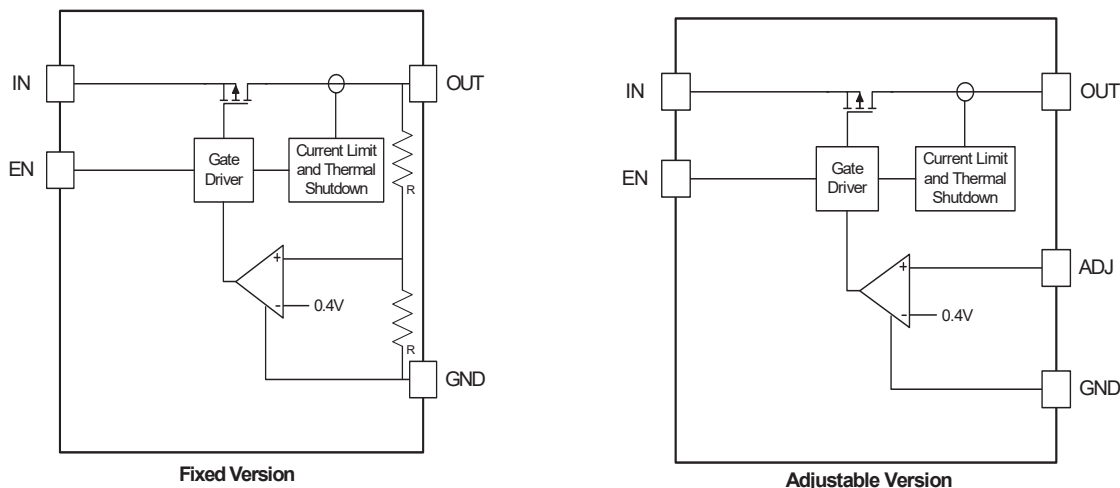


$$V_{OUT} = V_{REF} \left(1 + \frac{R_1}{R_2} \right)$$

Pin Descriptions

Pin Name	Pin Number				Description
	SOT25 (fixed)	DFN2020-6 (fixed)	SOT25 (adj)	DFN2020-6 (adj)	
IN	1	3	1	3	Voltage input pin. Bypass to ground through at least 1μF capacitor
GND	2	2	2	2	Ground
EN	3	1	3	1	Enable input, active high
ADJ	-	-	4	6	Output feedback pin
NC	4	5, 6	-	5	No connection
OUT	5	4	5	4	Voltage output pin. Bypass to ground through 1μF ceramic capacitor

Functional Block Diagram



Absolute Maximum Ratings

Symbol	Parameter		Ratings	Units
ESD HBM	Human Body Model ESD Protection		6	kV
ESD MM	Machine Model ESD Protection		400	V
V_{IN}	Input Voltage		7	V
	EN Voltage		$V_{IN} + 0.3$	V
	Continuous Load Current		Internal Limited	
T_{OP}	Operating Junction Temperature Range		-40 ~ 125	°C
T_{ST}	Storage Temperature Range		-65 ~ 150	°C
P_D	Power Dissipation (Note 2)	SOT25	640	mW
		DFN2020-6	740	mW
T_J	Maximum Junction Temperature		150	°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input voltage	2	6	V
I_{OUT}	Output Current (Note 3)	0	300	mA
T_A	Operating Ambient Temperature	-40	85	°C

Notes:

2. Ratings apply to ambient temperature at 25°C
3. The device maintains a stable, regulated output voltage without a load current.

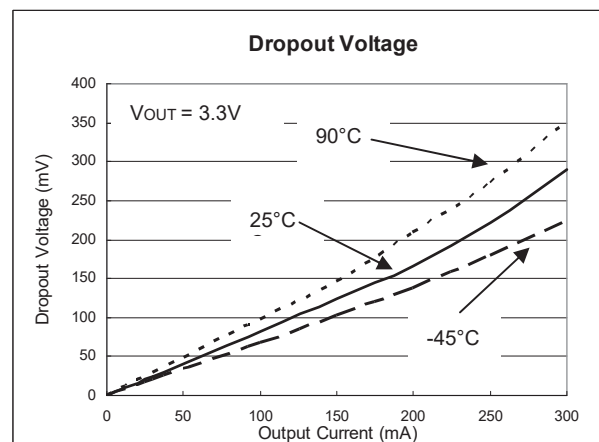
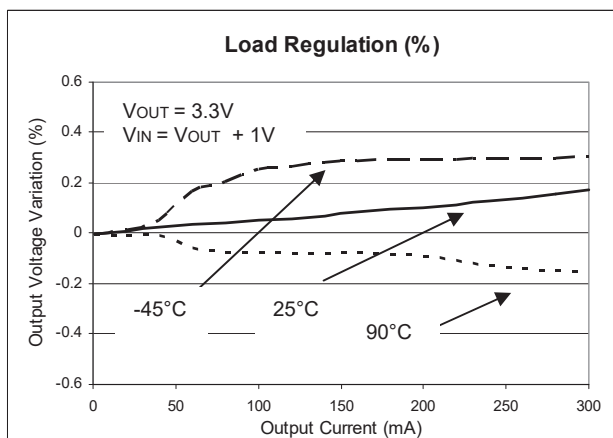
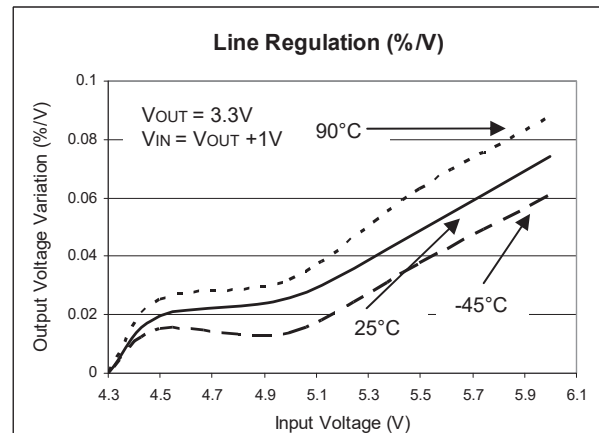
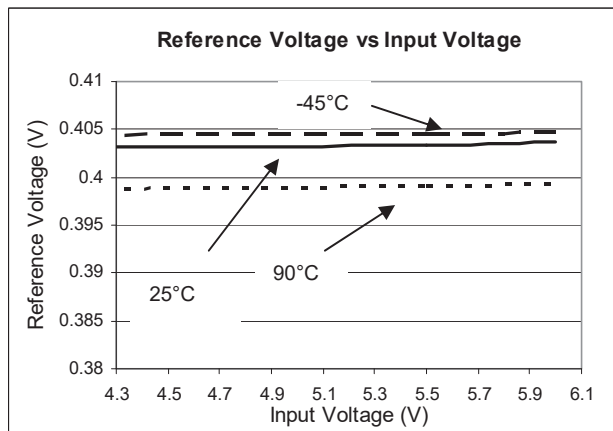
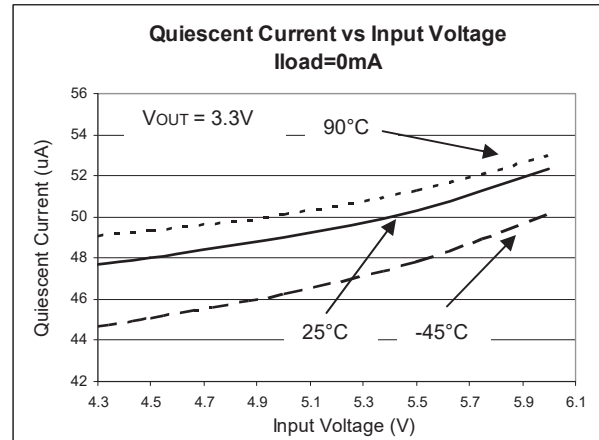
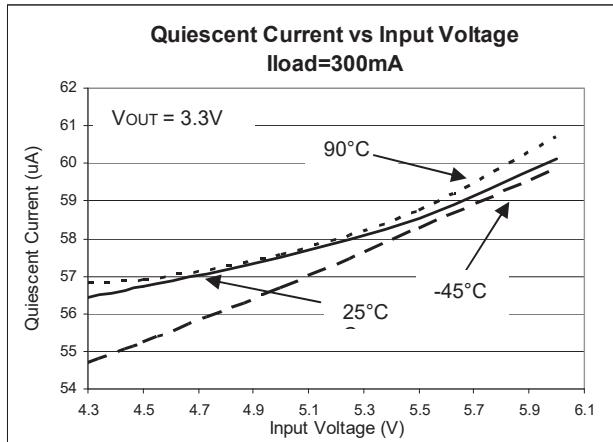
Electrical Characteristics

($T_A = 25^\circ\text{C}$, $V_{IN} = V_{OUT} + 1\text{V}$, $C_{IN} = 1\mu\text{F}$, $C_{OUT} = 1\mu\text{F}$, $V_{EN} = 2\text{V}$, unless otherwise stated)

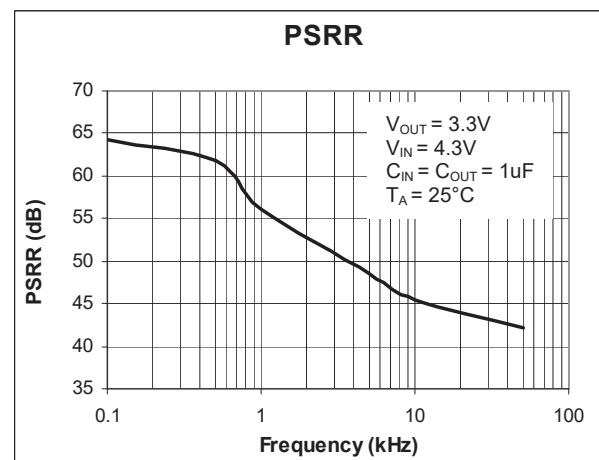
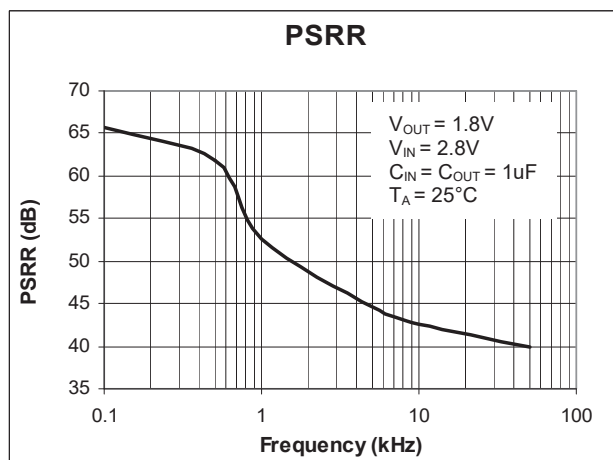
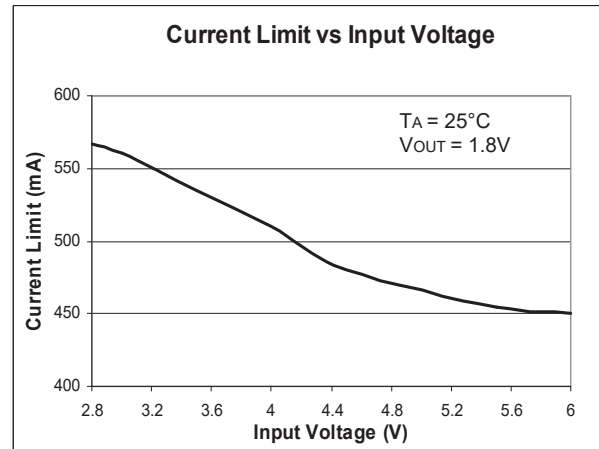
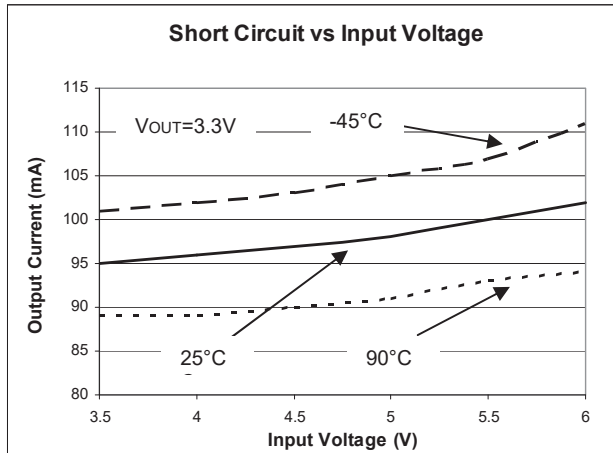
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
I_Q	Input Quiescent Current	$V_{EN} = V_{IN}$, $I_{OUT} = 0\text{mA}$	—	55	75	μA
		$V_{EN} = V_{IN}$, $I_{OUT} = 300\text{mA}$	—	65	85	
I_{SHDN}	Input Shutdown Current	$V_{EN} = 0\text{V}$, $I_{OUT} = 0\text{mA}$	—		1	μA
I_{LEAK}	Input Leakage Current	$V_{EN} = 0\text{V}$, OUT grounded	—		1	μA
$V_{Dropout}$	Dropout Voltage (Note 4)	$I_{OUT} = 300\text{mA}$		300	550	mV
V_{REF}	ADJ Reference Voltage (Adjustable version)	$I_{OUT} = 0\text{mA}$		0.4		V
I_{ADJ}	ADJ Leakage (Adjustable version)		—		1	μA
V_{OUT}	Output Voltage Accuracy	$T_A = -40^\circ\text{C}$ to 85°C , $I_{OUT} = 30\text{mA}$	-2		2	%
$\frac{\Delta V_{OUT}}{\Delta V_{IN}/V}$	Line Regulation	$V_{IN} = (V_{OUT} + 1\text{V})$ to V_{IN-Max} , $V_{EN} = V_{IN}$, $I_{OUT} = 1\text{mA}$		0.01	0.20	%/V
$\frac{\Delta V_{OUT}}{I_{OUT}}$	Load Regulation	$V_{IN} = (V_{OUT} + 1\text{V})$ to V_{IN-Max} , I_{OUT} from 1mA to 300mA	-0.6		0.6	%
t_{ST}	Start-up Time	$V_{EN} = 0\text{V}$ to 2.0V , $V_{OUT} = 1\text{V}$, $I_{OUT} = 300\text{mA}$		80		μs
PSRR	PSRR	$V_{IN} = [V_{OUT} + 1\text{V}]V_{DC} + 0.5V_{ppAC}$, $f = 100\text{Hz}$, $I_{OUT} = 30\text{mA}$		65		dB
I_{SHORT}	Short-circuit Current	$V_{IN} = V_{IN-Min}$ to V_{IN-Max} , $V_{OUT} < 0.2\text{V}$		100		mA
I_{LIMIT}	Current Limit	$V_{OUT}/R_{OUT} = 1\text{A}$	400	600		mA
V_{IL}	EN Input Logic Low Voltage	$V_{IN} = V_{IN-Min}$ to V_{IN-Max}			0.4	V
V_{IH}	EN Input Logic High Voltage	$V_{IN} = V_{IN-Min}$ to V_{IN-Max}	1.4			V
I_{EN}	EN Input Current	$V_{IN} = 0\text{V}$ or V_{IN-Max}	-1		1	μA
T_{SHDN}	Thermal Shutdown Threshold			140		$^\circ\text{C}$
T_{HYS}	Thermal Shutdown Hysteresis			15		$^\circ\text{C}$
θ_{JA}	Thermal Resistance Junction-to-Ambient	SOT25 (Note 5)		190		$^\circ\text{C/W}$
		DFN2020-6 (Note 6)		167		$^\circ\text{C/W}$

- Notes:
- Dropout voltage is the voltage difference between the input and the output at which the output voltage drops 2% below its nominal value. This parameter only applies to output voltages above 1.8V.
 - Test conditions for SOT25: Device mounted on FR-4 substrate PCB, with minimum recommended pad layout, 2oz copper, single sided
 - Test conditions for DFN2020-6: Device mounted on FR-4 substrate PCB, with minimum recommended pad layout, 2oz copper, double sided, bottom layer is a copper plane.

Typical Characteristics

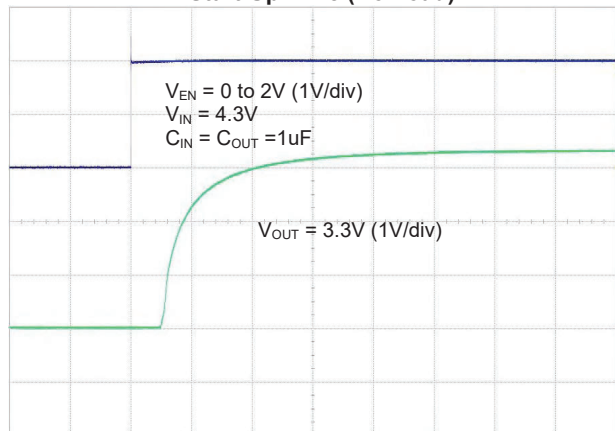


Typical Characteristics (Continued)



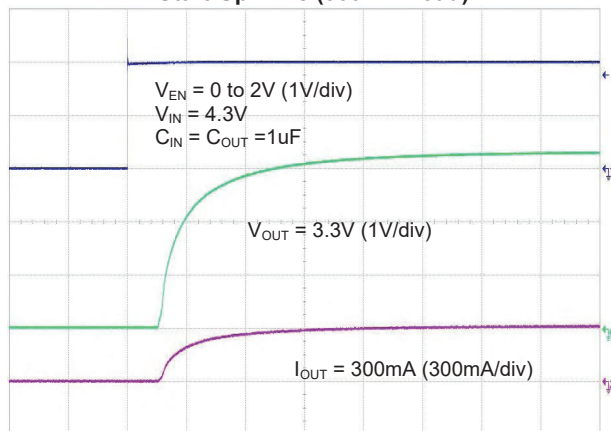
Typical Characteristics (Continued)

Start-Up Time (No Load)



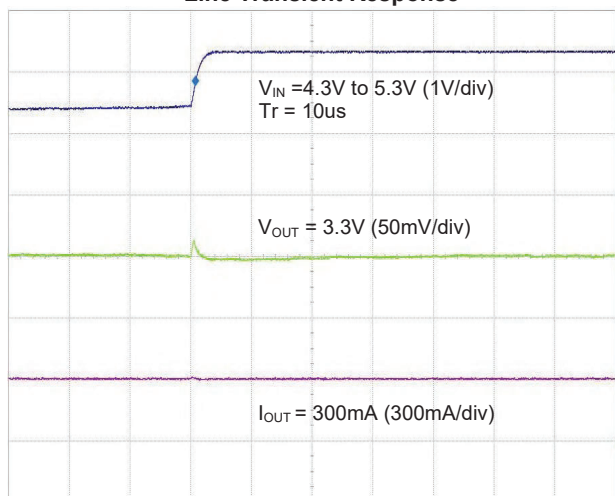
Time (50us/div)

Start-Up Time (300mA Load)



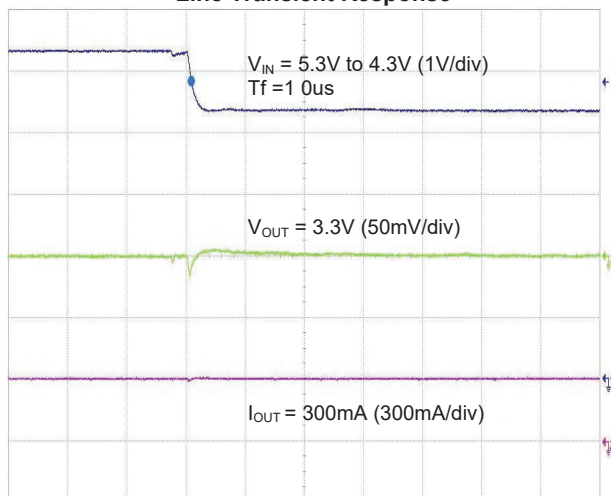
Time (50us/div)

Line Transient Response



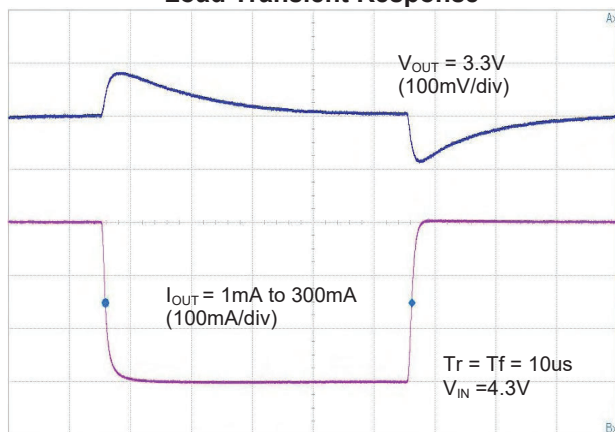
Time (50us/div)

Line Transient Response



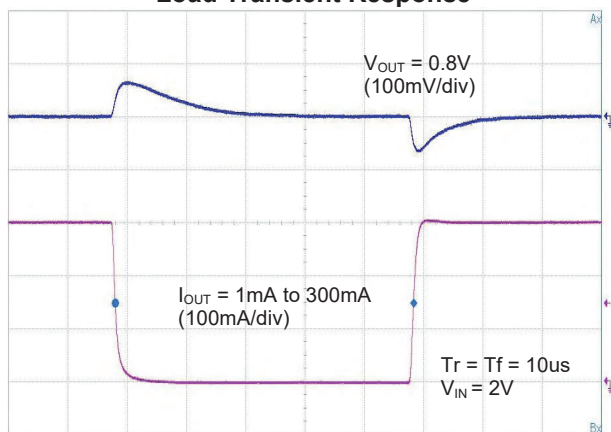
Time (50us/div)

Load Transient Response



Time (100us/div)

Load Transient Response



Time (100us/div)

Application Note

Input Capacitor

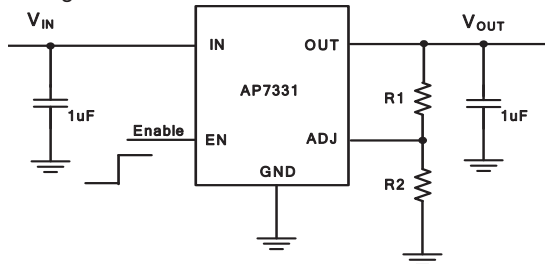
A 1μF ceramic capacitor is recommended to connect between V_{IN} and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both V_{IN} and GND. A lower ESR capacitor allows the use of less capacitance, while higher ESR type requires more capacitance.

Output Capacitor

The output capacitor is required to stabilize and help transient response for LDO. The AP7331 is stable with very small ceramic output capacitors. The recommended capacitance is from 1μF to 4.7μF, Equivalent Series Resistance (ESR) is from 10mΩ to 200mΩ, and temperature characteristic is X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins, and keep the leads as short as possible.

Adjustable Operation

The AP7331 provides output voltage from 0.8V to 5.0V through external resistor divider as shown below.



The output voltage is calculated by:

$$V_{OUT} = V_{REF} \left(1 + \frac{R_1}{R_2} \right)$$

Where V_{REF}=0.4V (the internal reference voltage)

Rearranging the equation will give the following that is used for adjusting the output to a particular voltage:

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$$

To maintain the stability of the internal reference voltage, R₂ need to be kept smaller than 125kΩ.

No Load Stability

Other than external resistor divider, no minimum load is required to keep the device stable. The device will remain stable and regulated in no load condition.

ON/OFF Input Operation

The AP7331 is turned on by setting the EN pin high, and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical

Characteristics section under V_{IL} and V_{IH}.

Current Limit Protection

When output current at OUT pin is higher than current limit threshold, the current limit protection will be triggered and clamp the output current to approximately 600mA to prevent over-current and to protect the regulator from damage due to overheating.

Short Circuit Protection

When OUT pin is short-circuit to GND or OUT pin voltage is less than 200mV, short circuit protection will be triggered and clamp the output current to approximately 100mA. This feature protects the regulator from over-current and damage due to overheating.

Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately +140°C, allowing the device to cool down. When the junction temperature reduces to approximately +125°C the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

Ultra Fast Start-up

After enabled, the AP7331 is able to provide full power in as little as tens of microseconds, typically 80μs, without sacrificing low ground current. This feature will help load circuitry move in and out of standby mode in real time, eventually extend battery life for mobile phones and other portable devices.

Fast Transient Response

Fast transient response LDOs can extend battery life. TDMA-based cell phone protocols such as Global System for Mobile Communications (GSM) have a transmit/receive duty factor of only 12.5 percent, enabling power savings by putting much of the baseband circuitry into standby mode in between transmit cycles. In baseband circuits, the load often transitions virtually instantaneously from 100μA to 100mA. To meet this load requirement, the LDO must react very quickly without a large voltage drop or overshoot — a requirement that cannot be met with conventional, general-purpose LDOs.

Application Note (Continued)

Fast Transient Response (Continued)

The AP7331's fast transient response from 0 to 300mA provides stable voltage supply for fast DSP and GSM chipset with fast changing load.

Small Overshoot and Undershoot

The AP7331 has small and controlled overshoot and undershoot in load and line transitions. This helps to protect supplied circuit from damage and operation error caused by glitches. This feature also permits the usage of small value output decoupling capacitor with AP7331.

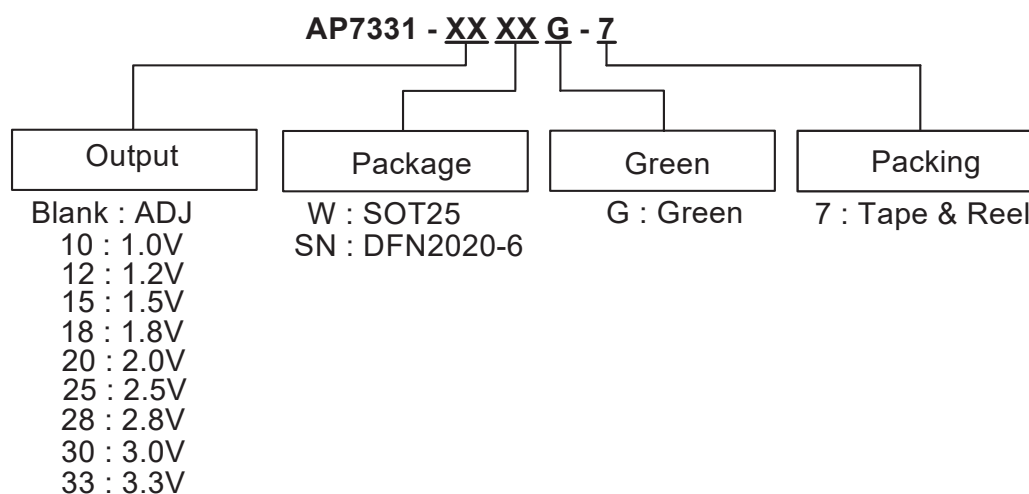
Low Quiescent Current

The AP7331, consuming only around 65µA for all input range and output loading, provides great power saving in portable and low power applications.

Wide Output Range

The AP7331, with a wide output range of 0.8V to 5.0V, provides a versatile LDO solution for many portable applications.

Ordering Information



Device	Package Code	Packaging (Note 7)	7" Tape and Reel	
			Quantity	Part Number Suffix
 AP7331-XXWG-7	W	SOT25	3000/Tape & Reel	-7
 AP7331-XXSNG-7	SN	DFN2020-6	3000/Tape & Reel	-7

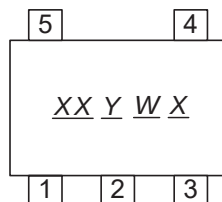
Note: 7. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com/datasheets/ap02001.pdf>.

Marking Information

1. SOT25

**300mA, LOW QUIESCENT CURRENT, FAST TRANSIENT
 LOW DROPOUT LINEAR REGULATOR**

(Top View)


XX : Identification code

Y : Year 0~9

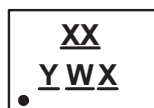
W : Week : A~Z : 1~26 week;
 a~z : 27~52 week; z represents
 52 and 53 week

X : A~Z : Green

Device	Package	Identification Code
AP7331-ADJ	SOT25	QJ
AP7331-10	SOT25	QK
AP7331-12	SOT25	QL
AP7331-15	SOT25	QM
AP7331-18	SOT25	QN
AP7331-20	SOT25	QT
AP7331-25	SOT25	QP
AP7331-28	SOT25	QQ
AP7331-30	SOT25	QR
AP7331-33	SOT25	QS

2. DFN2020-6

(Top View)


XX : Identification Code

Y : Year : 0~9

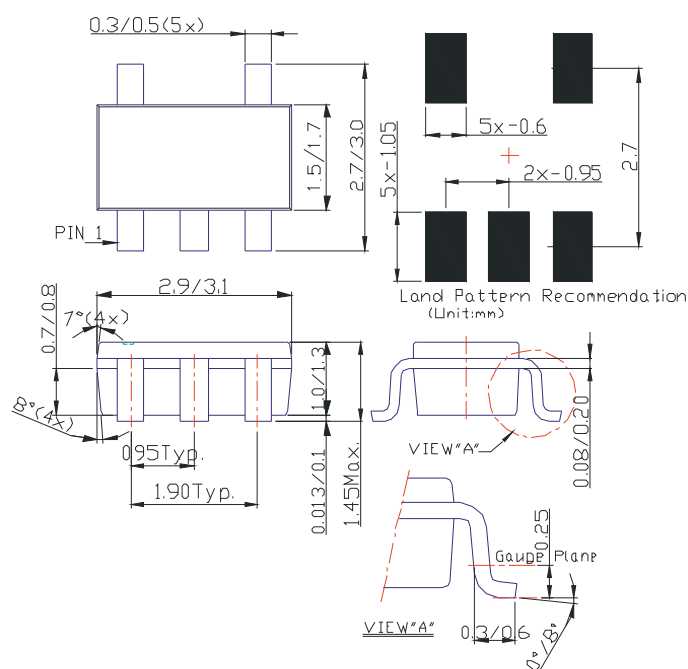
W : Week : A~Z : 1~26 week;
 a~z : 27~52 week; z represents
 52 and 53 week

X : A~Z : Green

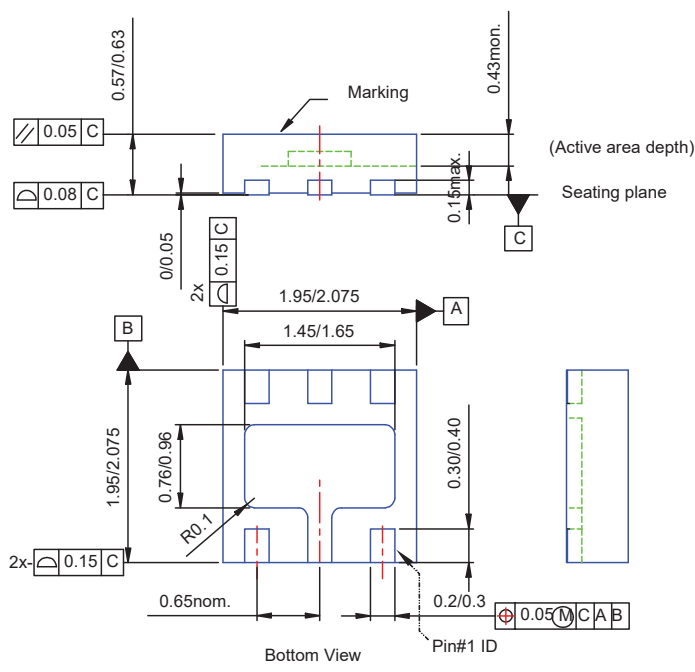
Device	Package	Identification Code
AP7331-ADJ	DFN2020-6	QJ
AP7331-10	DFN2020-6	QK
AP7331-12	DFN2020-6	QL
AP7331-15	DFN2020-6	QM
AP7331-18	DFN2020-6	QN
AP7331-20	DFN2020-6	QT
AP7331-25	DFN2020-6	QP
AP7331-28	DFN2020-6	QQ
AP7331-30	DFN2020-6	QR
AP7331-33	DFN2020-6	QS

Package Outline Dimensions (All Dimensions in mm)
1. Package Type: SOT25

300mA, LOW QUIESCENT CURRENT, FAST TRANSIENT LOW DROPOUT LINEAR REGULATOR



2. Package Type: DFN2020-6



Tape Orientation (Note 8)

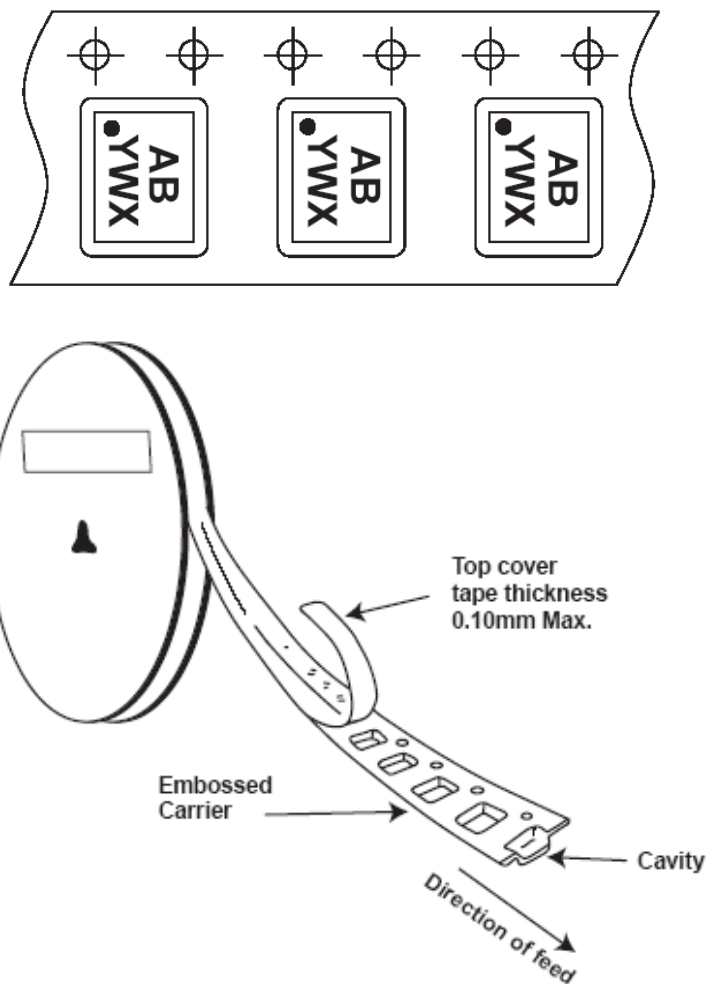
DFN2020-6

AP7331
Document number: DS31914 Rev. 3 - 2

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Aptiv Exhibit 1031 Page 158
Aptiv v. Microchip IPR2024-00646



Notes: 8. The taping orientation of the other package type can be found on our website at <http://www.diodes.com/datasheets/ap02007.pdf>

**300mA, LOW QUIESCENT CURRENT, FAST TRANSIENT
LOW DROPOUT LINEAR REGULATOR****IMPORTANT NOTICE**

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Exhibit 5

DIGITAL DESIGN

a systems approach

WILLIAM J. DALLY
R. CURTIS HARTING

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XOR function can be realized as shown in Figure 4.23(b). The switch networks here are not series-parallel networks. If inverted inputs are not available, it is more efficient to realize a two-input XOR gate using two CMOS gates in series, as shown in Figure 4.23(c). We leave the transistor-level design of this circuit as an exercise. An XOR symbol is shown in Figure 4.23(d).

EXAMPLE 4.4 CMOS gate synthesis

Draw a complex gate that outputs a 0 if and only if the input, cba , is a legal thermometer-coded signal.

First, we write the Boolean function and reduce it as follows:

$$\begin{aligned} f(c, b, a) &= \overline{(\bar{c} \wedge \bar{b} \wedge \bar{a}) \vee (\bar{c} \wedge \bar{b} \wedge a) \vee (\bar{c} \wedge b \wedge a) \vee (c \wedge b \wedge a)} \\ &= (\bar{c} \wedge \bar{b}) \vee (b \wedge a). \end{aligned}$$

Thus, our NFET switch-network function is given by

$$f_n = (\bar{c} \wedge \bar{b}) \vee (b \wedge a).$$

Next, in order to draw the PFET array correctly, we find the dual of our NFET function:

$$f_p(c, b, a) = (\bar{c} \vee \bar{b}) \wedge (b \vee a).$$

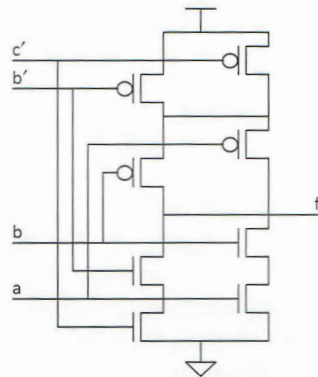


Figure 4.24. Schematic for the CMOS circuit to detect whether inputs abc represent a legal thermometer encoding.

Figure 4.24 shows our final answer. In order to implement this circuit in a single stage, the complements to inputs c and b are required.

4.3.4 Tri-state circuits

On occasion we want to build a distributed multiplexer function where we drive a value onto a signal node from point A when logic signal a is true and from point B when logic signal b is true. We can realize this functionality with a *tri-state* inverter. This circuit, shown in Figure 4.25(a) and (b) drives $\bar{a}$ onto x when e is true and presents a high impedance (drives neither 1 nor 0)

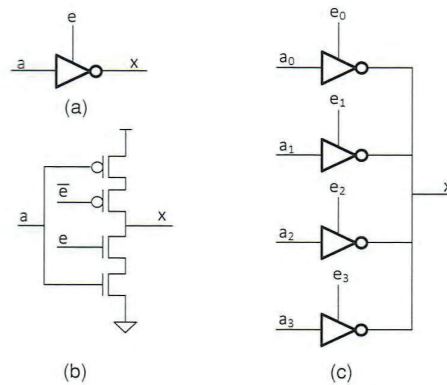


Figure 4.25. A tri-state inverter has two inputs and a single output, (a). Transistor level schematic, (b), when enable e is low, there is no supply connected to the output. When e is high, the output is driven to $\bar{a}$. Four tri-state inverters implement a bus or distributed multiplexer, (c). When exactly one enable e_i is high, the output is $\bar{a}_i$. When all enables are low, the output is indeterminate. If multiple enables are high, permanent damage may occur.

to the output when e is false. When the enable e is high ($\bar{e}$ is low), the middle two transistors are on. The outer transistors, controlled by a , then function as a normal inverter. With e low ($\bar{e}$ high), the enable transistors are off and no value is driven to the output. In this state, the value at the output is initially equal to the previous output, but will eventually leak into an unknown state. In Verilog, a wire that is not being driven is denoted with a z symbol.

The tri-state inverter is *not* a *gate* as defined in Section 4.3.1 because its output is *not* a restored logic function of its input. Its pull-down function $f_n(a, e) = a \wedge e$ is not equal to the complement of its pull-up function $f_p = \bar{a} \wedge e$. The *no-pull* function $f_z = \bar{f}_n \wedge \bar{f}_p = \bar{e}$ is true when f_n and f_p are both false, and indicates when x goes to the high impedance or z state. Because this circuit produces three output states, 0, 1, and z , we refer to it as a *tri-state* circuit. This is not to be confused with *ternary* logic circuits that use signals that can take on three values.

Tri-state circuits are not restricted to inverters. We can modify any CMOS gate circuit to gate the output off when an enable signal e is low. We are also not restricted to a single enable signal. An arbitrary logic function can determine when the circuit is enabled. This function can differ for pull-up and pull-down, and the enable function can be a function of the other circuit inputs. Any CMOS circuit where $f_z \neq 0$ is a tri-state circuit. Not all of these are useful.

Tri-state inverters can be used to realize multiplexers and distributed multiplexers, as shown in Figure 4.25(c). Here, four tri-state inverters all drive the same output wire, x . If exactly one enable signal e_i is asserted, $x = \bar{a}_i$. If all enable signals are low, there is no drive to x – it is in the high-impedance or z state. If more than one enable is asserted simultaneously (even for a very short period of time), a short circuit may form, causing static current to flow from the power supply of one gate to the ground of another. At the very least, this increases power dissipation and gives an invalid output. At worst, the high currents involved can vaporize metal traces, irreversibly damaging the chip. Even if only one enable signal is asserted each clock cycle, skew (see Chapter 15) between the clocks generating the different enables can lead to a fatal overlap. Distributed multiplexers, which often motivate the use of tri-state circuits, are particularly vulnerable because a large clock skew can develop over the distance between point A and point B .

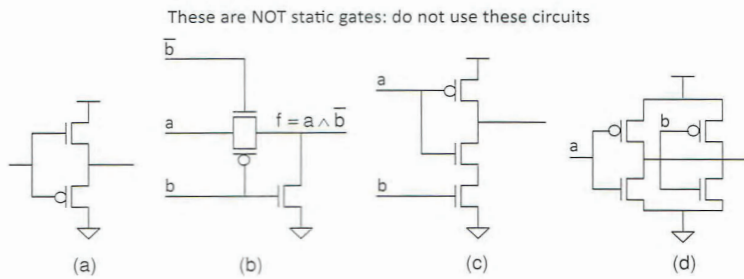


Figure 4.26. Three circuits that are *not* gates and should not be used: circuit (a) attempts to pass a 1 through an NFET and a 0 through a PFET; circuit (b) does not restore high output values; circuit (c) does not drive the output when $a = 1$ and $b = 0$; circuit (d) conducts static current when $a \neq b$.

Because of the potential for a short circuit, tri-state circuits should be avoided. If they are used, strong measures should be taken to ensure that there is no possibility of overlap between enable signals. One approach is to leave an idle cycle – with all enable signals low – between the assertion of one enable signal and another. Alternatively, one can ensure a *break before make* action by designing the circuits driving the enable signals to have a long delay on the rising edge and a short delay on the falling edge – with the difference in delays being large enough to compensate for clock skew and other factors. In most cases, the best approach is to build the required function – even a distributed multiplexer or bus (see Section 24.2) – with static CMOS gates (NANDs and NORs).

4.3.5 Circuits to avoid

Before closing this chapter it is worth examining a few more circuits that are not gates and do not work but represent common errors in CMOS circuit design. Figure 4.26 shows four representative mistakes. The would-be buffer in Figure 4.26(a) does not work because it attempts to pass a 1 through a PFET and a 0 through an NFET. The transistors cannot reliably pass those values and so the output signal is undefined – attenuated from the input swing at best. The AND-NOT circuit of Figure 4.26(b) does in fact implement the logical function $f = a \wedge \bar{b}$. However, it violates the digital abstraction in that it does not *restore* its output. If $b = 0$, a noise on input a is passed directly to the output.¹¹ Any noise on the output is also passed onto the input signal and all of the input's driven gates.

The circuit of Figure 4.26(c) leaves its output disconnected when $a = 1$ and $b = 0$. Due to parasitic capacitance, the previous output value will be *stored* for a short period of time on the output node. However, after a period, the stored charge will leak off and the output node becomes an undefined value. The final circuit, Figure 4.26(d), will have both the pull-up and pull-down networks conducting when a and b are not equal. This static current from power to ground outputs an undefined logic value, wastes power, and potentially damages the chip.

¹¹ Such circuits can be used with care in isolated areas, but must be followed by a restoring stage before a long wire or another non-restoring gate. In most cases it is better to steer clear of such *shortcut* gates.