APTIV SERVICES US LLC,
Petitioner,
v.
MICROCHIP TECHNOLOGY INC.,
Patent Owner.

Patent Owner's Oral Hearing Demonstratives

IPR2024-00646

June 27, 2025

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  - POSITA
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- **Petitioner Fails to Show Obviousness for Three Reasons**
  - Failure to establish a non-hindsight motivation to combine
  - Failure to show "gm-enhance[ment]" limitation is met
  - Failure to show "biasing circuit … to set a biasing ratio for gm-boost"

The Parties' Experts

Petitioner's Expert
Dr. Michael Chen



Patent Owner's Expert
Dr. Greg Taylor



POSITA

The Definition of a POSITA

- The parties largely agree on the definition of a POSITA
- Patent Owner should **prevail under either definition**

Petitioner's Level of Skill in the Art

III. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA in the field of the '074 patent in 2013 would have had at least a Master's Degree in Electrical Engineering, or alternatively a Bachelor's Degree in Electrical Engineering and two years of experience working on analog circuit design. (EX1002, ¶ 38.)

Pet. (Paper 1), 9

PO's Level of Skill in the Art

(Paper 11), 9. PO submits a POSITA in 2013 would have a bachelor's degree in electrical engineering, computer science, or equivalent technical degree and substantial experience (e.g., several years) in analog/mixed-signal IC design. Additional education related to the hardware, architecture, and circuit design aspects could be substituted for professional experience, and vice versa. EX2021 ("Taylor"), ¶¶30-36.

POR (Paper 19), 2-3

Petitioner Should Prevail Under Either Definition

> To the extent Petitioner believes there are any substantive differences in the level of skill in the art—and concomitantly the knowledge of a POSITA—PO believes its assertions are correct and supported by substantial evidence, including the testimony of Dr. Taylor. Regardless, PO submits the IPR outcome should result in a determination that no challenged claim is obvious under either party's articulation.

POR (Paper 19), 3

THE ’074 PATENT

Microchip's '074 Patent

(12) **United States Patent**
Zhou et al.

(10) **Patent No.: US 9,471,074 B2**
(45) **Date of Patent: Oct. 18, 2016**

(54) **USB REGULATOR WITH CURRENT BUFFER TO REDUCE COMPENSATION CAPACITOR SIZE AND PROVIDE FOR WIDE RANGE OF ESR VALUES OF EXTERNAL CAPACITOR**

(71) Applicant: **Microchip Technology Incorporated**, Chandler, AZ (US)

(72) Inventors: **Huamin Zhou**, Chandler, AZ (US); **Woowai Martin**, Phoenix, AZ (US); **Cristian Albina**, Chandler, AZ (US); **Fritz Schlunder**, Gilbert, AZ (US); **Minh Le**, Gilbert, AZ (US)

(73) Assignee: **MICROCHIP TECHNOLOGY INCORPORATED**, Chandler, AZ (US)

USPC 323/280
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,246,221	B1 *	6/2001	Xi	G05F 1/575 323/280
7,312,598	B1	12/2007	Huang et al.	323/280
7,656,224	B2 *	2/2010	Perez	H03F 1/0261 323/282
7,683,720	B1 *	3/2010	Yehui	H03F 3/45192 30/252
2002/0171403	A1 *	11/2002	Lopata	H03F 3/45183 323/280

(Continued)

FOREIGN PATENT DOCUMENTS

EX1001, 1

Microchip's '074 Patent

(21) Appl. No.: **14/204,011**

(22) Filed: **Mar. 11, 2014**

(65) **Prior Publication Data**

US 2014/0266107 A1 Sep. 18, 2014

Related U.S. Application Data

(60) Provisional application No. 61/780,985, filed on Mar. 14, 2013.

(51) **Int. Cl.**
G05F 1/575 (2006.01)
H03F 3/45 (2006.01)

(52) **U.S. Cl.**
CPC ***G05F 1/575*** (2013.01); ***H03F 3/45192*** (2013.01); *H03F 2200/45* (2013.01); *H03F 2203/45192* (2013.01); *H03F 2203/45626* (2013.01)

(58) **Field of Classification Search**
CPC G05F 1/575; H03F 3/45192

OTHER PUBLICATIONS

Al-Shyoukh et al., Aug. 2007, IEEE, JOSSC vol. 42 No. 8, 1732-1742.*

(Continued)

Primary Examiner — Jue Zhang

(74) *Attorney, Agent, or Firm* — Slayden Grubert Beard PLLC

(57) **ABSTRACT**

A voltage regulator has a large gm current buffer driver added between a first stage of an operation amplifier and a last stage power transistor. This current buffer allows a significant reduction in the maximum internal and external compensation capacitances needed for regulator stability. The current buffer compensation circuit allows a wide range of external capacitor sizes that increases the flexibility in choosing the external capacitor types (with low to high ESR ratings).

18 Claims, 8 Drawing Sheets

EX1001, 1

Microchip's '074 Patent

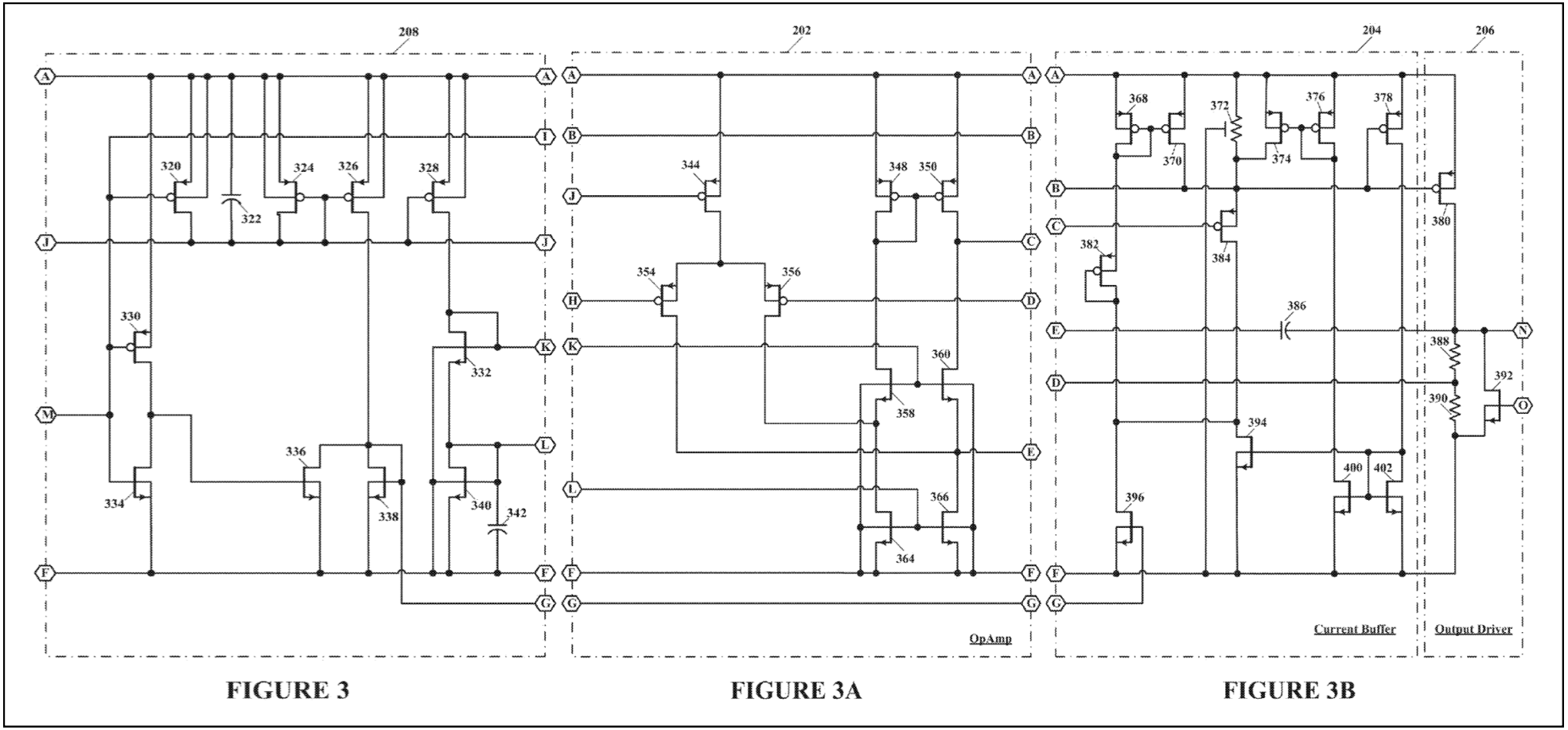


FIGURE 3 FIGURE 3A FIGURE 3B

EX1001, Figs. 3, 3A, 3B

Microchip's '074 Patent – Enable/Disable

buffer driver. According to a further embodiment, an enable/disable function may be provided to enable/disable the biasing circuit for reducing standby current. According to a

EX1001, 2:9-11

The ’074 Patent File History

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5, 7-17, 20 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Al-Shyoukh et al. (NPL_IEEE_JSSC_2007, hereinafter Al-Shyoukh).

Ex. 2005 (File History), 107

The ’074 Patent File History

Allowable Subject Matter

9. Claims 6, 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matters:

For claim 6, the prior art does not disclose or suggest, in combination with the limitations of the base claim and any intervening claims, primarily, the voltage regulator further having … an enable/disable function to enable/disable the biasing circuit for reducing standby current.

EX2005 (File History), 112

’074 Patent Independent Claim 1

Missing from the prior art

Missing from the prior art

No motivation to combine

1. A voltage regulator, comprising:
an operational amplifier;
a gm enhanced current buffer driver;
a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver;
an enable/disable function to enable/disable the biasing circuit for reducing standby current:
an output power driver, wherein the current buffer driver is coupled between the operational amplifier and the output power driver;
a current feedback circuit coupled between the output power driver and the current buffer driver; and
a feedback loop coupled between the output power driver and the operational amplifier.

EX1001, cl. 1

THE ASSERTED PRIOR ART

Summary of Prior Art Grounds

Ground	35 U.S.C. §	Claims	Prior Art
1	103	1-18	*Al-Shyoukh (EX1004)* Ivanov (EX1005) Stanescu (EX1006)
2	103	1-18	*Rincon-Mora (EX1013)* *Rincon-Mora Paper (EX1014)* Al-Shyoukh (EX1004) Ivanov (EX1005) Stanescu (EX1006)

Rincon Mora Patent (EX1013)

United States Patent [19]

Rincon-Mora et al.

[11] **Patent Number: 6,046,577**

[45] **Date of Patent: Apr. 4, 2000**

[54] **LOW-DROPOUT VOLTAGE REGULATOR INCORPORATING A CURRENT EFFICIENT TRANSIENT RESPONSE BOOST CIRCUIT**

[75] Inventors: **Gabriel A. Rincon-Mora**, Margate, Fla.; **Nicolas Salamina**, Sachse, Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

5,130,635	7/1992	Kase	323/280
5,686,820	11/1997	Riggio, Jr.	323/273

Primary Examiner—Peter S. Wong
Assistant Examiner—Rajnikant D. Patel
Attorney, Agent, or Firm—Mark E. Courtney; W. James Brady III; Richardson L. Donaldson

Rincon-Mora (EX1013), 1

Rincon Mora Patent (EX1013)

[21] Appl. No.: **09/001,057**

[22] Filed: **Dec. 30, 1997**

Related U.S. Application Data

[60] Provisional application No. 60/035,726, Jan. 2, 1997.

[51] **Int. Cl.**[7] **G05F 1/40**

[52] **U.S. Cl.** **323/282**; 323/279; 323/280; 323/281

[58] **Field of Search** 323/282, 280, 323/281, 276, 279

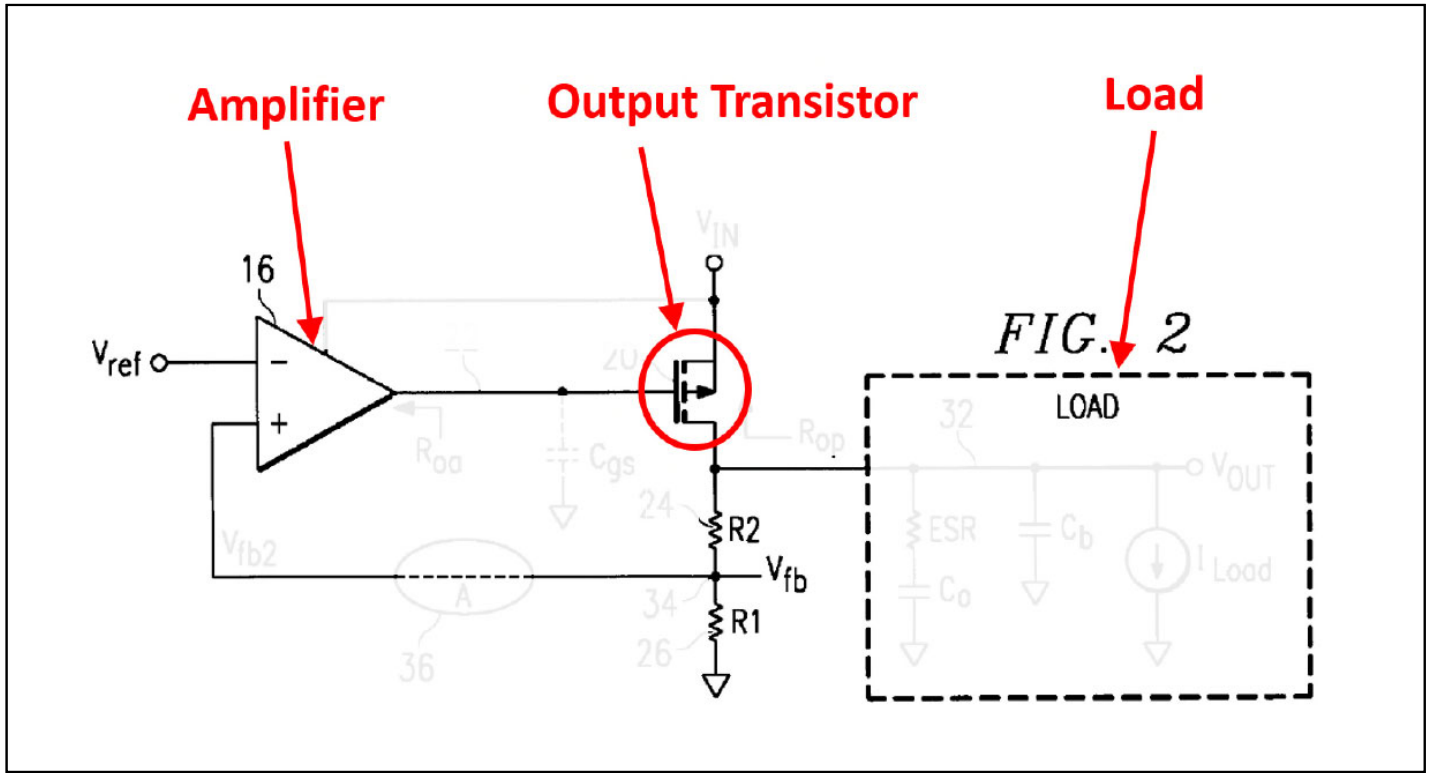
[56] **References Cited**

[57] **ABSTRACT**

An improved low-dropout ("LDO") voltage regulator incorporates a transient response boost circuit which is added to the slew-rate limited node at the control terminal of the LDO voltage regulator output transistor and provides improved transient response performance to the application of various load current step stimuli while requiring no standby or quiescent current during zero output current load conditions. The transient boost circuit supplies current to the slew-rate limited node only upon demand and may be constructed as either a localized positive feedback loop or a number of switching devices which conduct current only during slew-rate conditions.

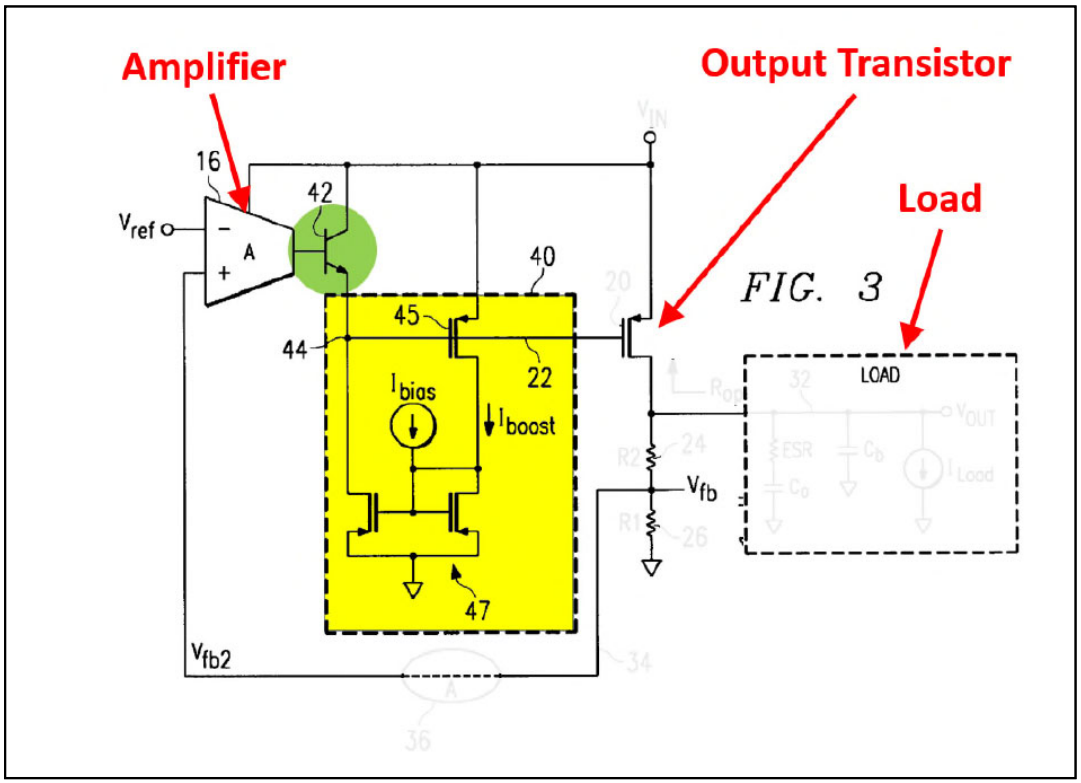
Rincon-Mora (EX1013), 1

Rincon Mora Patent (EX1013)



Rincon-Mora (EX1013), Fig. 2 (annotated)

Rincon Mora Patent (EX1013)



Rincon-Mora (EX1013), Fig. 3 (annotated)

Rincon Mora Patent (EX1013)

[57] **ABSTRACT**

An improved low-dropout ("LDO") voltage regulator incorporates a transient response boost circuit which is added to the slew-rate limited node at the control terminal of the LDO voltage regulator output transistor and provides improved transient response performance to the application of various load current step stimuli while requiring no standby or quiescent current during zero output current load conditions. The transient boost circuit supplies current to the slew-rate limited node only upon demand and may be constructed as either a localized positive feedback loop or a number of switching devices which conduct current only during slew-rate conditions.

Rincon-Mora (EX1013), Abstract

Rincon Mora Patent (EX1013)

BACKGROUND OF THE INVENTION

The present invention relates, ir general, to the field of integrated circuit semiconductor technology low-dropout ("LDO") voltage regulators. More particularly, the present invention relates to a current efficient LDO voltage regulator incorporating a transient response boost circuit which may be added to selectively apply current to a slew-rate limited node and yet requires no standby current during zero output current load conditions of the LDO voltage regulator.

Rincon-Mora (EX1013), 1:10-17

Rincon Mora Patent (EX1013)

the like. As a consequence, standby and quiescent current flow are major concerns in their design and some LDO voltage regulators incorporate a separate enable terminal to switch the device into a standby mode of operation to minimize power consumption when the associated device is disabled.

Rincon-Mora (EX1013), 1:24-27

Rincon Mora Patent (EX1013)

conditions. As a consequence, known techniques result in circuit designs that either necessitate the toleration of relatively large output glitch specifications or those that require more quiescent current flow than is desired during zero load current conditions.

Rincon-Mora (EX1013), 1:48-52

Rincon Mora Patent (EX1013)

techniques. The circuit and method of the present invention is straightforward in design and inexpensively implemented in a current efficient design which provides improved transient response to the application of various load current step stimuli.

In a preferred embodiment disclosed herein, a transient boost circuit is added to the slew-rate limited node and requires no standby current during zero output current load conditions. Alternative embodiments of the transient boost circuit are disclosed which supply current to the slew-rate limited node only upon demand. A first embodiment may be

Rincon-Mora (EX1013), 1:66-2:9

Rincon Mora Patent (EX1013)

With respect additionally now to FIG. **4**, at I_{Load}=0 Amps, P1 is low thereby making the unity gain frequency low. The parasitic pole P3 must only be greater than UGF[I_{Load}=0 A] which condition can be effectuated with approximately 1 μA. At this point, I_{boost} is zero because the aspect ratio of the PMOS transistor **45** forming a portion of the transient boost circuit **40** is much less than that of the output PMOS transistor **20**, thus yielding low quiescent current.

Rincon-Mora (EX1013), 4:41-48

Rincon Mora Patent (EX1013)

to the current mirror **47**. However, due to the provision of a relatively high mirror ratio, the current sourced by transistor **45** is negligible and it consumes no power. If the output at

Rincon-Mora (EX1013), 5:9-11

Rincon Mora Paper (EX1014)

A Low-Voltage, Low Quiescent Current, Low Drop-Out Regulator

Gabriel A. Rincon-Mora, *Member, IEEE*, and Phillip E. Allen, *Fellow, IEEE*

Rincon-Mora Paper (EX1014), 1

0018–9200/98$10.00 © 1998 IEEE

Rincon Mora Paper (EX1014)

Abstract-The demand for low-voltage, low drop-out (LDO) regulators is increasing because of the growing demand for portable electronics, i.e., cellular phones, pagers, laptops, etc. … **This paper discusses some techniques that enable the practical realizations of low quiescent current LDO's** at low voltages and in existing technologies. The proposed circuit exploits the frequency response dependence on load-current to **minimize quiescent current flow**. … An LDO prototype incorporating the aforementioned techniques was fabricated. The circuit was operable down to input voltages of 1 V with a **zero-load quiescent current flow of 23µA**.

Rincon-Mora Paper (EX1014), Abstract

Dr. Chen Equates the Rincon-Mora Patent and Paper



Q. Would it be fair to say that in your view the disclosure in the Rincon-Mora patent applies to the Rincon-Mora paper as well?

A. Yes. That's why I see them as one unit or one group.

EX2018 (Dr. Chen), 124:17-22

Rincon-Mora Does NOT Disclose Enable/Disable



Q. What elements of Claim 1 are missing from the Rincon-Mora reference?
MR. LIU: Objection to form.
A. Yeah, so counsel, the combination for Rincon-Mora is Claim 1D, the enable/disable function.

EX2018 (Dr. Chen), 129:1-6

POR (Paper 19), 55 (citing EX2014 (Dr. Chen), 128:17-129:6)

Al-Shyoukh (EX1004)

A Transient-Enhanced Low-Quiescent Current Low-Dropout Regulator With Buffer Impedance Attenuation

Mohammad Al-Shyoukh, Hoi Lee, *Member, IEEE*, and Raul Perez, *Member, IEEE*

EX1004, 1

4. Claims 1-5, 7-17, 20 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Al-Shyoukh et al. (NPL_IEEE_JSSC_2007, hereinafter Al-Shyoukh).

Ex. 2005 (File History), 107 (cited at POR (Paper 19), 19)

Al-Shyoukh (EX1004)

Abstract-This paper presents a low-dropout regulator (LDO) for portable applications with an impedance-attenuated buffer for driving the pass device … without dissipating large quiescent current. …The LDO with the proposed impedance-attenuated buffer has been implemented in a 0.35-µm twin-well CMOS process. The proposed LDO dissipates 20-µA quiescent current at no-load condition and is able to deliver up to 200-mA load current.

EX1004, Abstract

Al-Shyoukh (EX1004)

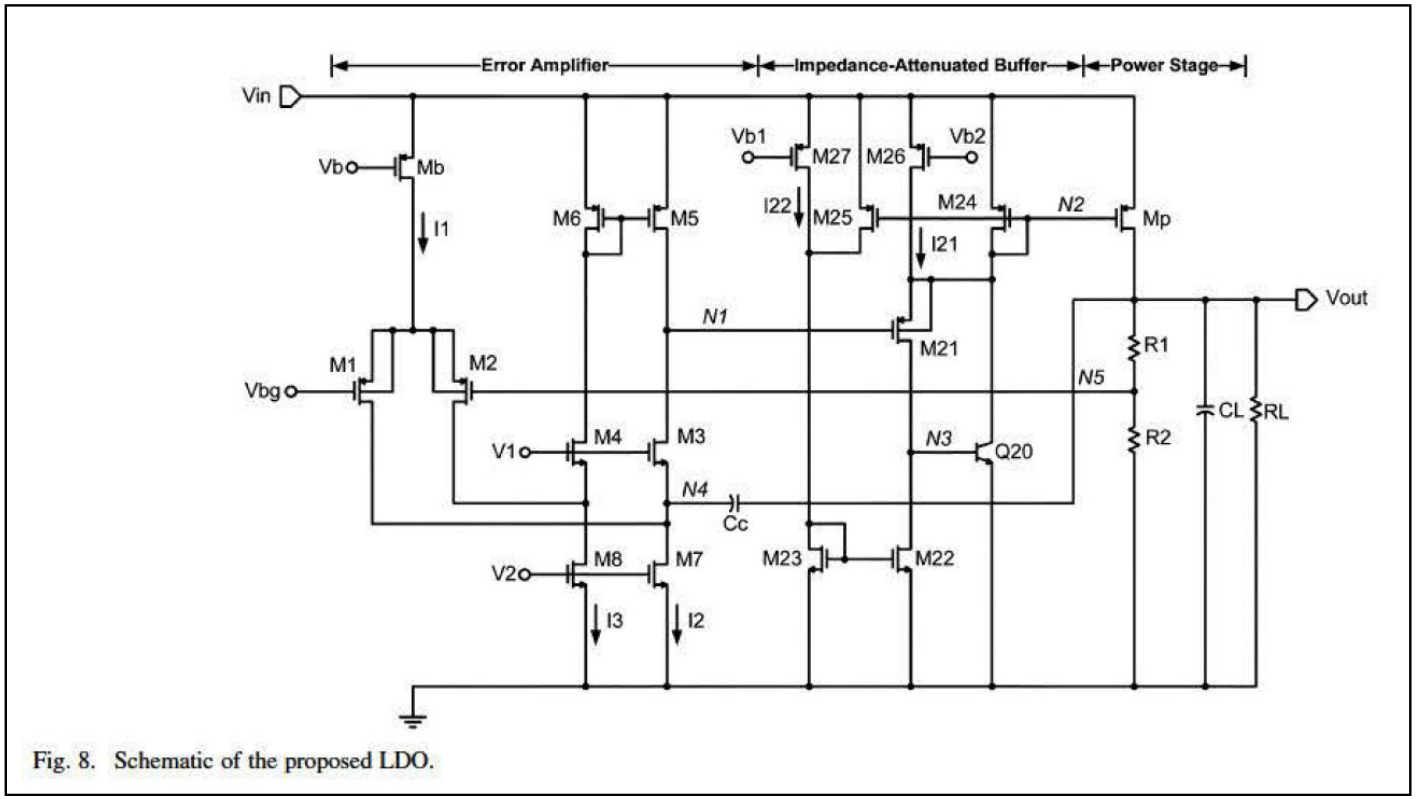
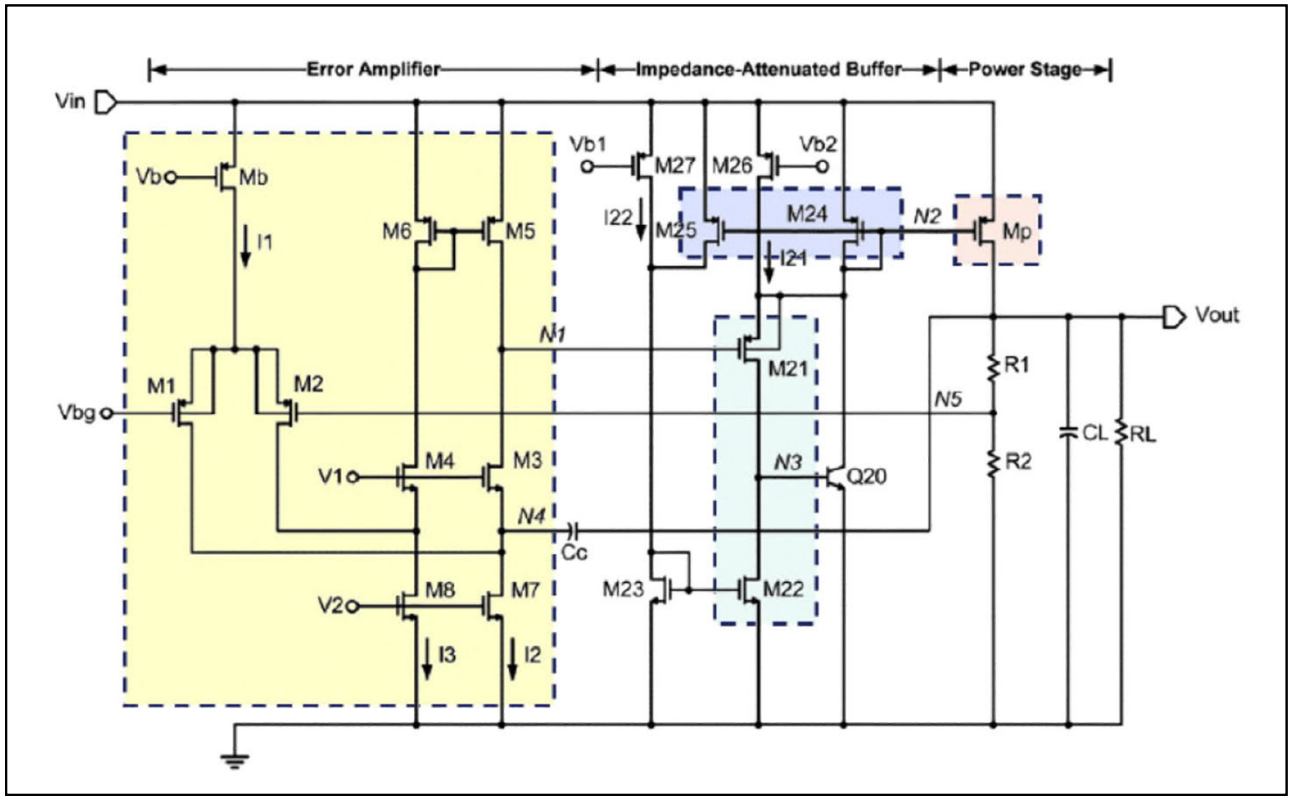


Fig. 8. Schematic of the proposed LDO.

EX1004, Fig. 8

Al-Shyoukh (EX1004) – Petitioner's Mapping



Al-Shyoukh (EX1004), Fig. 8 (annotated)

Petitioner's Admission re Al-Shyoukh

1. Summary of Al-Shyoukh

Al-Shyoukh discloses an LDO suitable for "battery-powered portable devices such as cellular phones and PDAs in order to reduce the standby power and prolong the battery runtime." (EX1004, 1732.) Due to "the increased level of integration" in such devices, the LDO must "deliver high load current" while keeping "the no-load quiescent current" low for efficiency. (*Id.*; *see also* EX1002 ¶¶ 41-42.)

Petition (Paper 1), 10

Al-Shyoukh's Low Quiescent Current

Regarding the "buffer[] driver" (in green above), Al-Shyoukh explains that "to further improve LDO performances, buffer impedance attenuation technique (BIA) is first proposed to realize an intermediate stage for driving the pMOS pass device." Al-Shyoukh, 2. This circuit operates similarly to Rincon-Mora's "boost" circuit, and achieves the same effect. Taylor, ¶92. As Al-Shyoukh explains, "[t]he BIA technique thus allows the LDO to dissipate low quiescent current." Al-Shyoukh, 2; *see also id.*, 3 (similar).

POR (Paper 19), 33 (citing Al-Shyoukh, 2)

Al-Shyoukh's Low Quiescent Current

Al-Shyoukh explains "the use of a pMOS transistor [for M_{21}] to implement the source-follower in the proposed buffer is extremely critical to minimize the quiescent current at no-load condition." Al-Shyoukh. 7. "Under no-load condition, the pass device M_p is almost turned off." *Id.* Al-Shyoukh provides measured results, touting that its "LDO consumes small quiescent current of 20 µA under no-load conditions." *Id.*, 10; *see also id.*, Table I. Al-Shyoukh compares its regulator with others in Table II.

POR (Paper 19), 33-34 (citing Al-Shyoukh, 7, 10)

Al-Shyoukh's Low Quiescent Current

TABLE II
PERFORMANCE COMPARISON WITH PREVIOUSLY REPORTED LDOS

	1998 [1]	2000 [3]	2003 [4]	2004 [5]	2005 [17]	**This Work**
Technology (μm)	2.0	1.0	0.6	0.5	0.09	**0.35**
V_{do} (V)	0.3	N.A.	0.2	N.A.	0.3	**0.2**
$I_{L,max}$ (mA)	50	200	100	160	100	**200**
I_q (mA)	0.023	0.03	0.038	0.025	6	**0.02**
Current Efficiency at $I_{L,max}$ (%)	99.5	N.A.	N.A.	N.A.	94.3	**99.8**
ΔV_{out} (mV)	19	220	130	200	90	**54**
T_r (μs)	1.8	1.1	2	2.75	0.00054	**0.27**
C_L (μF)	4.7	1	10	2.2	0.00060	**1**
ESR Zero Required	No	Yes	Yes	No	No	**No**
FOM (ns)	8.2	0.165	4.9	0.43	0.032	**0.027**

Rincon-Mora

Al-Shyoukh

POR (Paper 19), 34 (citing Al-Shyoukh, Table II (annotated))

Al-Shyoukh Does NOT Disclose Enable/Disable

Al-Shyoukh also touts that its full-load quiescent current is so low that its regulator design has "worst-case current efficiency of 99.8%." Al-Shyoukh., 8. Because "[c]urrent efficiency above 99% is critical if the LDO is designed for portable applications as the current efficiency determines the battery lifetime," Al-Shyoukh's design is well-suited for portable battery powered applications. *Id.*, 9; *see also id.*, 1 ("This paper present a low-dropout regulator (LDO) for portable applications … without dissipating large quiescent current."). Consistent with these results and assertions, Al-Shyoukh does not disclose enable/disable functionality.

POR (Paper 19), 33-34 (citing Al-Shyoukh, 8-9)

Al-Shyoukh Does NOT Disclose Enable/Disable



Q. What claim elements in Claim 1 are missing from the Al-Shyoukh reference?
A. Counsel, let me check my report just to confirm.
MR. LIU: I'll object to the form of the question.
A. So Al-Shyoukh satisfies most of these claims, except for the 1D, the enable/disable function.

EX2018 (Dr. Chen), 128:17-25

Ivanov (EX1005)

(12) **United States Patent**
Ivanov et al.

(10) **Patent No.: US 6,400,207 B1**
(45) **Date of Patent: Jun. 4, 2002**

(54) **QUICK TURN-ON DISABLE/ENABLE BIAS CONTROL CIRCUIT FOR HIGH SPEED CMOS OPAMP**

(75) Inventors: **Vadim V. Ivanov**; **Shilong Zhang**, both of Tucson, AZ (US)

(73) Assignee: **Texas Instruments Incorporated**, Dallas, TX (US)

6,057,721	A		5/2000	Nolan et al.	327/143
6,118,263	A	*	9/2000	O'Neill et al.	323/315
6,177,825	B1	*	1/2001	Nayebi et al.	327/374

* cited by examiner

Primary Examiner—Dinh T. Le
(74) *Attorney, Agent, or Firm*—W. Daniels Swayze, Jr.; W. James Brady; Frederick J. Telecky, Jr.

Ivanov (EX1005), 1

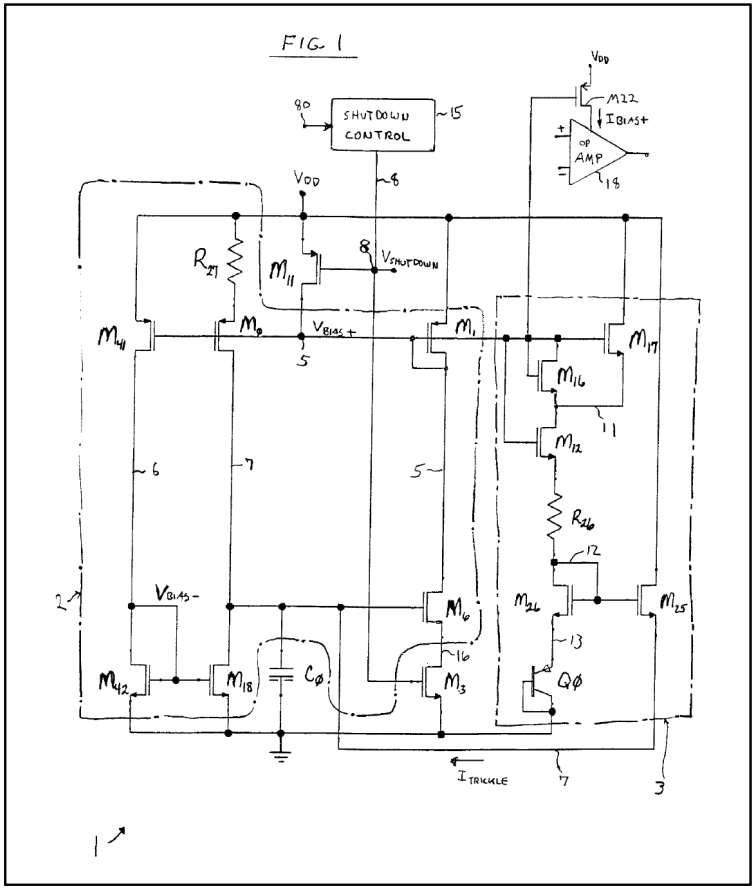
Ivanov's Primary Intended Use

BACKGROUND OF THE INVENTION

The present invention relates generally to start-up circuits for integrated circuit applications. More particularly, the present invention relates to a quick turn-on disable/enable bias control circuit for use in conjunction with high speed CMOS amplifiers, particularly CMOS amplifiers used in high speed video multiplexing applications.

Ivanov (EX1005), 1:5-11

Ivanov's Complex Circuit



Ivanov (EX1005), Fig. 1

Ivanov (EX1005)

transistor M22. EX1005, 2:15-19. But it has nothing to do with—and is completely silent on—*set[ting] a biasing ratio for gm-boost of the current buffer driver*, as required by '074 patent claim 1. Taylor, ¶¶98, 103. In other words, Ivanov exclusively concerns "reference generation" (*i.e.*, generating a reference current/voltage to place active circuitry in a ready state), not with the functionality, design, transconductance, or operation of the active circuitry itself. Taylor, ¶¶98-103.

POR (Paper 19), 36

Ivanov Introduces Delay

> While Ivanov purports to provide a "quick turn-on disable/enable bias control circuit" (*id.*, Title), no matter how fast it operates it still introduces additional delay into any circuit that would otherwise be enabled. Taylor, ¶98. The techniques Ivanov employs (*e.g.*, trickle charge circuit) to reduce delay requires extra circuitry and power consumption. *Id.*, ¶¶100-103. A POSITA would understand the time

POR (Paper 19), 38-39

Ivanov Requires User Control

connected to conductor **7**. The shutdown control circuit **15** ordinarily would simply be a buffer circuit or a Schmitt trigger circuit having its output connected to conductor **8** and its input connected to an external conductor **80** on which a user applies an external control signal to disable/enable bias control circuit

Ivanov (EX1005), 4:20-25

Ivanov Dissipates Current When Disabled

Transistor **M17** is designed to have a very long channel length, so as to produce a drain and source current of only approximately 0.1 to 5 microamperes. Transistors **M16** and **M12** in combination perform the function of preventing a possible unstable condition in quasi PTAT circuit **2** by causing part of the "charging reference current" in transistor **M26** to be supplied from transistor **M16** and causing the sum of the currents in transistors **M16** and **M17** (approximately 0.1 to 5 microamperes) to flow through transistor **M12** and resistor **R26**, and therefore through transistor **M26** and diode-connected PNP transistor **Q0**.

Ivanov (EX1005), 5:39-49

PETITIONER'S INADEQUATE MOTIVATION TO COMBINE

Summary of Prior Art Grounds

Ground	35 U.S.C. §	Claims	Prior Art
1	103	1-18	*Al-Shyoukh (EX1004)* Ivanov (EX1005) Stanescu (EX1006)
2	103	1-18	*Rincon-Mora (EX1013)* *Rincon-Mora Paper (EX1014)* Al-Shyoukh (EX1004) Ivanov (EX1005) Stanescu (EX1006)

No anticipation grounds!

’074 Patent Independent Claim 1

Missing from Rincon-Mora and Al-Shyoukh

1. A voltage regulator, comprising:

an operational amplifier;

a gm enhanced current buffer driver;

a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver;

an enable/disable function to enable/disable the biasing circuit for reducing standby current:

an output power driver, wherein the current buffer driver is coupled between the operational amplifier and the output power driver;

a current feedback circuit coupled between the output power driver and the current buffer driver; and

a feedback loop coupled between the output power driver and the operational amplifier.

EX1001, cl. 1

Dr. Chen Admits Rincon-Mora and Al-Shyoukh Lack a Disable Function



Q. What claim elements in Claim 1 are missing from the Al-Shyoukh reference?
A. Counsel, let me check my report just to confirm.
MR. LIU: I'll object to the form of the question.
A. So Al-Shyoukh satisfies most of these claims, except for the 1D, the enable/disable function.
Q. What elements of Claim 1 are missing from the Rincon-Mora reference?
MR. LIU: Objection to form.
A. Yeah, so counsel, the combination for Rincon-Mora is Claim 1D, the enable/disable function.

EX2018 (Dr. Chen), 128:17-129:6

Petitioner Bears the Burden of Proving Obviousness

We agree with Magnum that the Board improperly shifted the burden to it, as the patentee, to prove nonobviousness. Because McClinton failed to separately meet its burden of establishing obviousness in view of Lehr, Cockrell, and Kristiansen, we reverse.

The final written decision is replete with examples where, rather than require McClinton to prove its assertion of obviousness, the Board improperly shifted the burden to Magnum to disprove obviousness.

In re Magnum Oil Tools Int'l, Ltd.,829 F.3d 1364 at 1377-78 (Fed. Cir. 2016)

Petitioner Bears the Burden of Proving Obviousness

Moreover, the issue is not whether Hayafuji "teaches away" from removing other aspects of positive power supply variations, or whether it would have been "trivial" or an "obvious design choice" to do so. *See* Reply 21; Pet. 68–70. The issue is whether a skilled artisan would have been motivated to do so based on teachings of the references; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue. *KSR*, 550 U.S. at 418.

Samsung Display Co. et al. v. Polaris PowerLED Techs., LLC, IPR2023-00771, Paper 40, 60 (PTAB Oct., 11, 2024)

Petitioner's One-Paragraph Motivation to Combine

A POSITA would have been motivated to use Ivanov's disable/enable control mechanism for the biasing circuit for Rincon-Mora's LDO. Both Rincon-Mora and Ivanov are highly concerned with power efficiency, and Ivanov's mechanism saves power by shutting off unused circuitry. (*Compare* EX1013, 1:18-30 (noting that "standby and quiescent current flow are major concerns" in LDO design), 5:18-21 (explaining that a benefit of the proposed transient response boost circuit is that it is "power efficient" because "it only sinks current upon demand") *with* EX1005, 1:6-

Pet. (Paper 1), 64

Petitioner's One-Paragraph Motivation to Combine

A POSITA would have been motivated to use Ivanov's disable/enable control mechanism for Al-Shyoukh's biasing circuit. Al-Shyoukh is highly concerned with power efficiency, and Ivanov's mechanism saves power by shutting off circuitry when it is not needed. (*Compare* EX1004, 1732 (describing LDOs as "critical power management modules" and identifying "low no-load quiescent current" as a major performance requirement of the LDO) *with* EX1005, 1:6-18 (proposing disabling not-in-use circuitry for "a quiescent, low-power state").) Ivanov, moreover, identifies voltage regulators as an intended application for its circuit. (EX1005,

Pet. (Paper 1), 25

Petitioner Hindsight-Driven Argument Fails for Two Reasons

> Petitioner's argument fails because it (1) rests on a false premise rebutted by the art itself; and (2) is conclusory and fails to account for countervailing factors and trade-offs. In summary, Petitioner's bare bones assertion is nothing more than a hindsight-driven results-oriented approach that uses the claim as a roadmap.

POR (Paper 19), 56

POR (Paper 19), 56-57

Petitioner's Argument Rests on a False Premise

1. Petitioner Fundamentally Misunderstands the Prior Art and Its Logic Rests on a False Premise

The first link in Petitioner's logical reasoning chain rests on a false premise—*viz.*, that Rincon-Mora and Al-Shyoukh require further power reduction. Pet., 25, 64. This is fatal to Petitioner's purported motivation to combine. In other words, Petitioner's motivation does not even cross the start line.

POR (Paper 19), 58

Petitioner's Reason for Combining Does Not Apply

Petitioner's Reply argues the law—*viz.*, that because enable/disable functionality was "known," it need not show anything more. Reply, 23. That is like saying that because heated driveways were known for homes in Aspen, Colorado (*viz.*, to melt snow during winter) that it would have been obvious (or "suitable" to use Petitioner's verbiage) to install heated driveways in Miami, Florida. Petitioner's head-in-the-sand approach to obviousness fails. Just because installing a heated

Sur-reply (Paper 29), 25

Petitioner's Reason for Combining Does Not Apply

Rincon-Mora expressly teaches its LDO voltage regulator "require[es] no standby or quiescent current during zero output current load conditions." Rincon-Mora, Abstract. Against this backdrop, Petitioner proposes adding/modifying not-shown biasing circuitry to enable/disable voltage regulator circuitry which already draws "no standby or quiescent current." This is the epitome of hindsight reasoning.

POR (Paper 19), 57

Petitioner's Reason for Combining Does Not Apply

> But these statements simply set the stage for Al-Shyoukh to discuss its voltage regulator design, which Al-Shyoukh goes on to tout "minimize[s] the quiescent current at no-load condition," "consumes small quiescent current of 20 µA," has "low quiescent current," and achieves "worst-case current efficiency of 99.8%." *See* §VI.B (quoting and summarizing Al-Shyoukh).

POR (Paper 19), 62

Petitioner's Reason for Combining Does Not Apply

TABLE II
PERFORMANCE COMPARISON WITH PREVIOUSLY REPORTED LDOS

	1998 [1]	2000 [3]	2003 [4]	2004 [5]	2005 [17]	**This Work**
Technology (μm)	2.0	1.0	0.6	0.5	0.09	**0.35**
V_{do} (V)	0.3	N.A.	0.2	N.A.	0.3	**0.2**
$I_{L,max}$ (mA)	50	200	100	160	100	**200**
I_q (mA)	0.023	0.03	0.038	0.025	6	**0.02**
Current Efficiency at $I_{L,max}$ (%)	99.5	N.A.	N.A.	N.A.	94.3	**99.8**
ΔV_{out} (mV)	19	220	130	200	90	**54**
T_r (μs)	1.8	1.1	2	2.75	0.00054	**0.27**
C_L (μF)	4.7	1	10	2.2	0.00060	**1**
ESR Zero Required	No	Yes	Yes	No	No	**No**
FOM (ns)	8.2	0.165	4.9	0.43	0.032	**0.027**

Rincon-Mora

Al-Shyoukh

Al-Shyoukh, Table II (annotated)

Tradeoffs Cannot be Ignored

[T]he benefits, *both lost and gained*, should be weighed against one another. … The Board recognized that Iwaguchi discloses a TPM sensor but found that a skilled artisan would have been dissuaded from integrating Iwaguchi's sensor into Kauffman's system. … Considering the prior art as a whole, we conclude that substantial evidence supports the Board's finding of no motivation to combine.

Henny Penny Corp. v. Frymaster LLC, 938 F.3d 1324, 1331-32 (Fed. Cir. 2019)

Dr. Chen Admits "So Many Consideration[s]" Affect Whether to Add Disable



Q. Would the amount of quiescent current that a voltage regulator uses relative to the amount of current used by an overall system impact a POSITA's decision on whether to add an enable signal to the voltage regulator?

A. I don't think I can offer that answer at this point. As I mentioned earlier, when you decide the circuiting system, there are just so many consideration to consider, right. It's not just in one single angle on this biasing of the regulators or whatever the circuit that you provide.

Also, there's also part of the SOC that you need to consider. So typically that would need to be considered jointly.

EX2018 (Dr. Chen), 263:6-16

Dr. Chen's Testimony Regarding Quiescent Current



Q. Would a POSITA consider the amount of quiescent current that a voltage regulator uses when determining whether to add an enable function to that voltage regulator?

MR. LIU: Objection to form.

A. I think it will be one of the consideration, but as I mention earlier there are also other consideration that the designer will consider collective.

EX2018 (Dr. Chen), 264:13-22

Dr. Chen's Testimony Regarding Quiescent Current



Q. If a voltage regulator had high quiescent current, would that provide a motivation for a POSITA to add an enable/disable function to the voltage regulator?

A. If that's a large quiescent current, it should start to, you know, contribute significant part of the overall power consumptions, right. Then that would motivate a POSITA to use the enable/disable circuits, you know, to reduce the currents.

EX2018 (Dr. Chen), 262:13-23

Dr. Chen's Testimony Regarding Circuit Size



Q. Would a POSITA consider the size of the additional circuitry necessary to when deciding whether to add an enable function?

A. Well, again, this would be another generic question, right. So, in general, when POSITA design the circuits, you always need to concern about the size that you use, right, the size that you use for all these devices, you know, will affect the circuit performance.

EX2018 (Dr. Chen), 261:22-262:12

Dr. Chen's Testimony Regarding Circuit Size



Q. Would you agree with me that adding an enable/disable function would require additional circuitry?

A. That one is possible. You add the enable and disable signal. You may add some circuits, but that require further analysis to see exactly what context and circuit you would need it at.

EX2018 (Dr. Chen), 255:13-20

Rincon-Mora Touts Its "Low Component Count"

> conditions. The resulting circuit takes maximum advantage of the transistors utilized to yield low component count and low overall ground current. Furthermore, the current

Rincon-Mora Paper (EX1014), 8

POR (Paper 19), 66 (citing Rincon-Mora Paper (EX1014), 8)

Dr. Chen Did Not Analyze the Impact of Enable/Disable on Circuit Speed



Did you do any analysis in your report regarding how adding an enable/disable function would impact the speed of the Rincon-Mora or Al-Shyoukh voltage regulators?

MR. LIU: Objection to form.

A. I don't remember that, that I did analysis of that enable and disable and how that impact the regulator speed of Rincon-Mora and Al-Shyoukh.

EX2018 (Dr. Chen), 257:4-13

Dr. Chen Admits He Analyzed No Other Considerations



Q. And you didn't analyze any of those considerations in your report, did you?

MR. LIU: Objection to form.

A. I don't recall that, but counsel let me quickly check this.

So, counsel, the most relevant ones regarding to our discussions is on page 38, paragraph 70, and that's the power efficiency that we just talk about -- or I just talk about. I don't see other considerations that I've analyzed in my report.

EX2018 (Dr. Chen), 264:23-265:10

Dr. Chen Admits He Analyzed No Drawbacks to Adding Enable/Disable



Q. What are the drawbacks to using an enable/disable circuit?

MR. LIU: Objection to form.

A. I suppose that were related to some system design concerns. As I mentioned earlier, I did not perform system analysis in this particular case at this point. So I'm not ready to offer that opinions by sitting here today.

Q. And you didn't render any such opinions in your report, correct?

MR. LIU: Objection to form.

A. I don't recall that. I don't recall that I offered that kind of opinions other than showing that Ivanov circuit examples, you know, has this enable/disable signals.

EX2018 (Dr. Chen), 254:13-255:4

POR (Paper 19), 68-69 (citing EX2018 (Dr. Chen), 254:13-255:4)

Petitioner's *Intel* Argument

- Citing *Intel Corp. v. PACT XPP Schweiz AG*, Petitioner argues it only has to show that a "known technique was a '***suitable option***.'" Reply (Paper 25), 18.
- Petitioner argues "that ***power efficiency was a known problem***, that either Ivanov or the conventional use of enable/disable helped improve power efficiency." *Id*.

Reply (Paper 25), 18

Petitioner's *Intel* Argument Fails for Two Independent Reasons

- ***First***, *Intel* applies where there exists a "known problem" in the art
  - We have the opposite situation--***it was known no quiescent current problem existed*** in either Rincon-Mora or Al-Shyoukh

- ***Second***, *Intel* dealt with replacing one secondary cache with another
  - ***No "replacement" is at issue*** here where both Rincon-Mora and Al-Shyoukh lack disable circuitry altogether

Petitioner's "Suitability" Argument Fails

Petitioner's Reply argues the law—*viz.*, that because enable/disable functionality was "known," it need not show anything more. Reply, 23. That is like saying that because heated driveways were known for homes in Aspen, Colorado (*viz.*, to melt snow during winter) that it would have been obvious (or "suitable" to use Petitioner's verbiage) to install heated driveways in Miami, Florida. Petitioner's head-in-the-sand approach to obviousness fails. Just because installing a heated driveway (analogous to enable/disable function) was known ***where a need existed and under the right circumstances***, does not make installing it obvious/suitable where ***the need is not present*** or is outweighed by countervailing considerations such as cost, complexity, speed/delay, expected benefit, etc.

Sur-reply (Paper 29), 25

Petitioner's *Intel* Argument Fails

Citing *Intel Corp. v. PACT XPP Schweiz AG*, Petitioner argues it need only show that a "known technique was a 'suitable option,' as opposed to 'an improvement in a categorical sense.'" Reply (Paper 25), 18.

> Petitioner's reliance on *Intel Corp. v. PACT XPP Schweiz AG* is also misplaced. Reply, 18. Indeed, Petitioner admits *Intel* applies to "a 'known problem' in the art." Reply, 18 (citing *Intel*, 61 F.4th 1373 at 1381). Here, it was expressly known that no quiescent current problem existed in Rincon-Mora or Al-Shyoukh. POR, §§VI.A (Rincon-Mora), VI.B (Al-Shyoukh), VII.C (discussing

Sur-reply (Paper 29), 19

Petitioner's *Intel* Argument Fails

Citing *Intel Corp. v. PACT XPP Schweiz AG*, Petitioner argues it need only show that a "known technique was a 'suitable option,' as opposed to 'an improvement in a categorical sense.'" Reply (Paper 25), 18.

or quiescent current …"). Moreover, *Intel* dealt with *replacing* one secondary cache with another. *Intel*, 61 F.4th 1373 at 1381. No "replacement" is at issue here where both primary references lack disable circuitry altogether.

Sur-reply (Paper 29), 19

Dr. Chen's "Hindsight" Problem

transistors, behave in predictable ways." Ex. 1002 ¶ 203. Yet neither Petitioner nor Dr. Chen explains what reason or motivation one of ordinary skill in the art would have had to combine those embodiments. *See id.* ¶¶ 199–202; Pet. 65. Dr. Chen's conclusory analysis here suffers from hindsight bias. *See ActiveVideo Networks, Inc. v. Verizon Commc'ns, Inc.*,

EX2010 (IPR2024-00803, Paper 10 (Order Denying Institution)), 26-27

POR (Paper 19), 57-58 (citing EX2010)

Dr. Chen Has Employed Hindsight Before

> [N]either Petitioner nor Dr. Chen explains what reason or motivation one of ordinary skill in the art would have had to combine those embodiments. [cite omitted] Dr. Chen's conclusory analysis here suffers from hindsight bias.

Aptiv Services US, LLC, v. Microchip Technology Inc., IPR2024-00803, Paper 10 (Order Denying Institution), 28 (P.T.A.B., Nov. 7, 2024)

> Dr. Chen's declaration merely repeats the Petition's argument. [cite omitted]. Thus, Dr. Chen's assertions (EX1002 ¶ 206) are entitled to little weight.

Id., 26

PETITIONER FAILS TO SHOW "GM-ENHANCE[MENT]"

’074 Patent Independent Claim 1

Missing from the prior art

Present in the prior art

1. A voltage regulator, comprising:
an operational amplifier;
a gm enhanced current buffer driver;
a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver;
an enable/disable function to enable/disable the biasing circuit for reducing standby current:
an output power driver, wherein the current buffer driver is coupled between the operational amplifier and the output power driver;
a current feedback circuit coupled between the output power driver and the current buffer driver; and
a feedback loop coupled between the output power driver and the operational amplifier.

EX1001, cl. 1

Different Claim Terms Are Presumed to Have Different Meanings

In the absence of any evidence to the contrary, we must presume that the use of these different terms in the claims connotes different meanings. [cite omitted] Here, this suggests that "bottom plane" refers to a surface lying within the more general "bottom" of the groove.

CAE Screenplates, Inc. v. Heinrich Fiedler Gmbh & Co. Kg, 224 F.3d 1308, 1317 (Fed. Cir. 2000)

The general presumption that different terms have different meanings remains.

Chi. Bd. Options Exch., Inc. v. Int'l Sec. Exch., LLC, 677 F.3d 1361, 1369 (Fed. Cir. 2012)

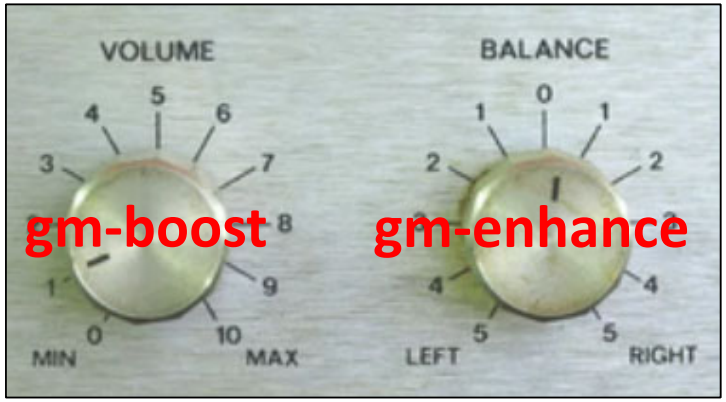
"gm enhance[ment]" and "gm-boost" are Different

- "**gm-boost**" and "**gm enhance[ment]**" are ***different terms*** and are presumed to have ***different meanings***
- Both increase gm, but do so in ***different ways*** using different circuit techniques, *e.g.*:
  - "gm-boost" → changes the overall ***magnitude*** of the standing current
  - "gm-enhance[ment]" → changes the ***allocation*** of where the current is deployed
- Techniques are ***complementary/additive*** and employing both increases gm more than either alone could

"gm enhance[ment]" and "gm-boost" are Different

But, as the POR (and Dr. Taylor) explain at length, ***gm-boost*** and ***gm enhance[ment]*** are different concepts achieved via different circuit techniques, akin to increasing the overall speaker volume (***gm-boost***) versus re-balancing existing sound output between left and right speakers (***gm-enhance[ment]***). POR,

Sur-reply (Paper 29), 4-5

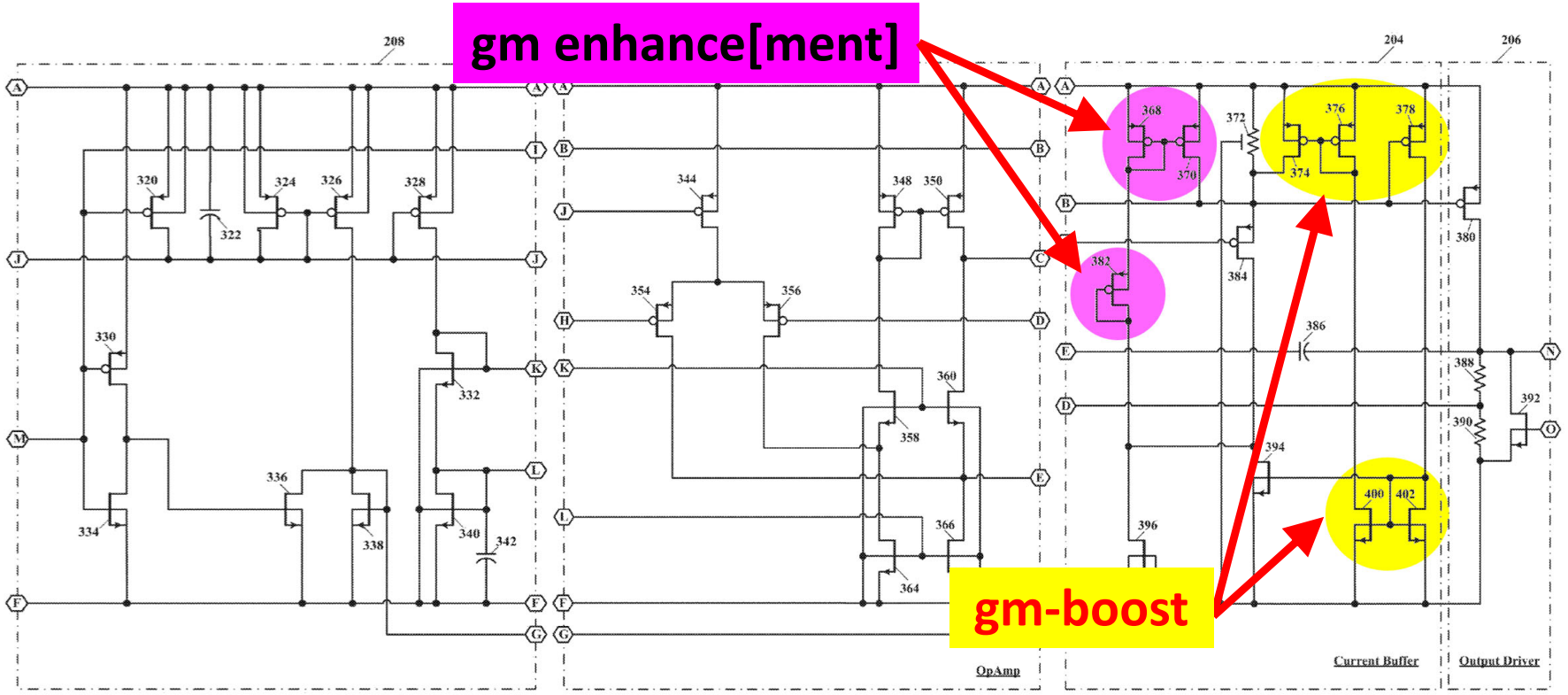


"gm enhance[ment]" and "gm-boost" are Different

does not. While both techniques serve to increase the gm of transistor 384, they do so in fundamentally different ways. One (gm-boost) acts to increase gm by adding current through transistor 384, while the other (gm-enhancement) increases gm by steering current around transistor 384. Taylor, ¶¶75, 87, 66-71.

POR (Paper 19), 17

The Patent Confirms “gm enhance[ment]” and “gm-boost” are Different



EX1001, Figs. 3/3A/3B (annotated)

POR (Paper 19), 17-18 (citing EX1001, Figs. 3/3A/3B (annotated))

"gm enhance[ment]"

If the voltage on node C rises, the current through source follower 384 is reduced (because it is a PMOS transistor), causing the excess bias current to be redirected through current mirror 368/370 into node B (*viz*., the gate capacitance of the power output transistor 380). Taylor, ¶86. Where PMOS transistors 368 and

POR (Paper 19), 22

enhanced. *Id*. If the voltage on node C drops, transistor 384 sources more current because it is a PMOS device and its Vgs increased. *Id*. This, in turn, enhances gm because some current previously flowing through transistor 368 now flows through 384 to account for the increased current through transistor 384. *Id*. This is "gm enhancement" to which element 1[b] refers, and is not the same as "gm-boost"

POR (Paper 19), 23

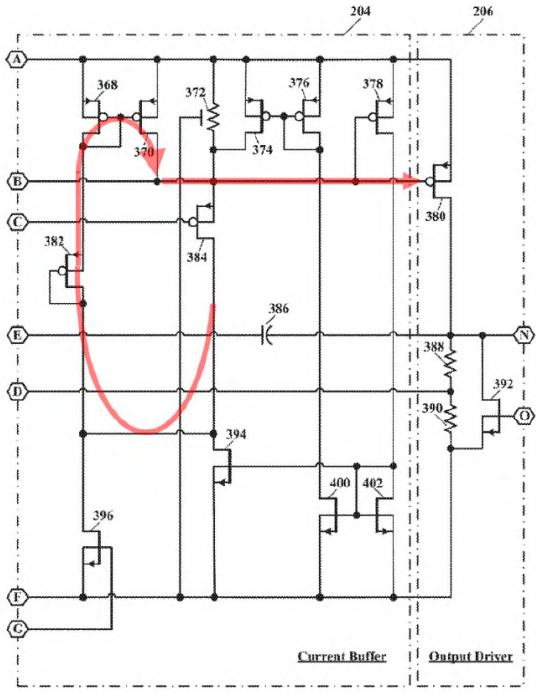
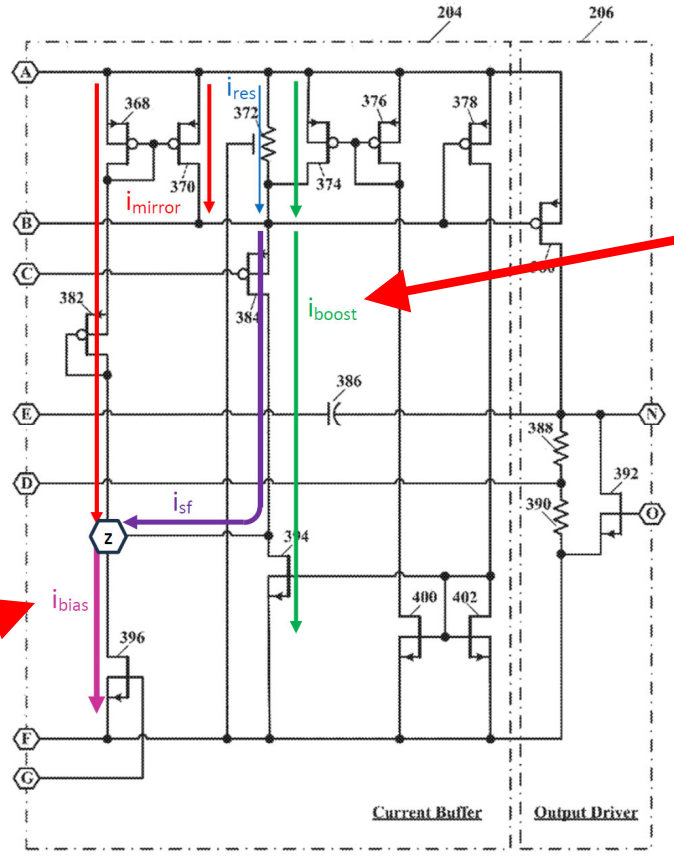


FIGURE 3B

EX1001, Fig. 3B (annotated)

“gm enhance[ment]” vs. “gm-boost”



gm-boost *increases* i_{boost}

gm-enhance *reallocates* steady-state i_{bias} current between i_{sf} and i_{mirror}

EX1001, Fig. 3B (annotated)

Taylor (EX2021), ¶¶76-81 (citing EX1001, Fig. 3B (annotated))

"gm enhance[ment]" vs. "gm-boost"

81. Phrasing this explanation differently, gm-boost controls the gm of source follower 384 by changing the current that flows through it, biasing it with a current that is proportional to the output driver current. When output current is high, *gm-boost[ing]* delivers a high current into node B through PMOS 374 and then out of node B through source follower 384. When output current is low, these same currents into and out of node B are lowered together. Unlike *gm-boosting*, *gm enhance[ment]* steers the bias currents that are already flowing in Figure 3B in the steady state.

Taylor (EX2021), ¶81

"gm-boost" and "gm enhance[ment]" are Additive

As Dr. Taylor explains, the combined effects of *gm-boost* and *gm-enhance[ment]* are cumulatively greater than the effect either could achieve alone. Taylor, ¶41. Equating "gm enhancement" with "gm-boost" would negate this cumulative effect, and improperly conflates the analysis of elements 1[b] and 1[c]

POR (Paper 19), 23

Dr. Chen's Reply Declaration Testimony



7. Because node B responds quickly and follows node C closely, increases in V_{gs} caused by a drop in the voltage of node C would be negligible. Thus, the "gm enhancement" effect described by Dr. Taylor would also be negligible, because it depends on V_{gs} increasing.

EX1028 (Dr. Chen Reply), ¶7

Sur-reply (Paper 29), 4 (citing EX1028 (Dr. Chen Reply), ¶7).

The Petition Conflates "gm-boost" and "gm-enhance[ment]"

> While the Petition recites the claim elements under separate headings, the substance of its analysis (and the underlying circuitry it points to) is substantially the same for both elements, essentially collapsing the two requirements into one. This is true for both the Rincon-Mora and Al-Shyoukh grounds. *See* Pet., 16-21 (for Al-Shyoukh) and 58-62 (for Rincon-Mora).

POR (Paper 19), 40

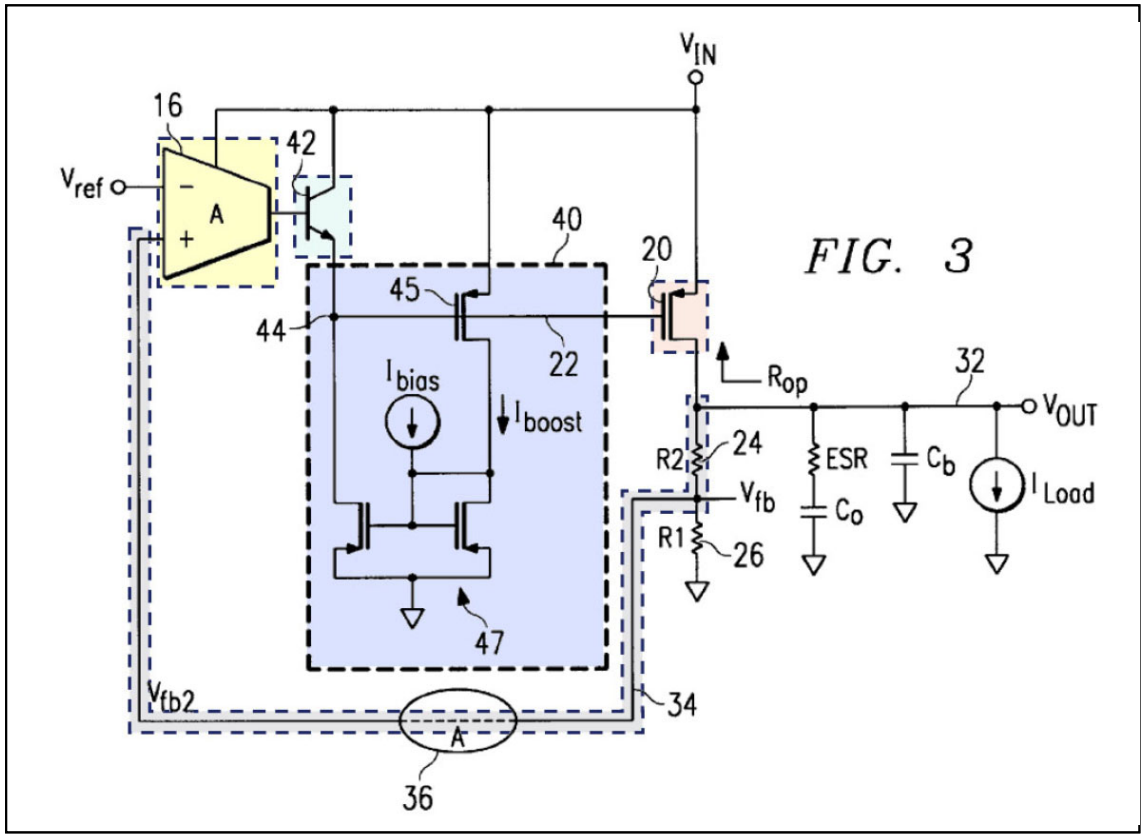
The Petition Conflates "gm-boost" and "gm-enhance[ment]"

[b] *a gm enhanced current buffer driver;*

Rincon-Mora's buffer driver is "gm enhanced" because the transient boost circuit, comprising transistor 45 and current mirror 47, increases its gm. (*See* Section IV.B.1, *supra*; EX1013, 3:38-43, 4:33-38, 5:10-13, 7:42-44, Fig. 3; *see also* EX1002 ¶¶ 126-36, 142-44.)

Pet. (Paper 1), 58 (Rincon-Mora ground)

“Transistor 45” and “Current Mirror 47” Are In the Transient Boost Circuit 40



Rincon-Mora (EX104), Fig. 3 (annotated)

The Petition Conflates "gm-boost" and "gm-enhance[ment]"

[b] *a gm enhanced current buffer driver;*

Al-Shyoukh's buffer driver discloses this limitation. Centered on the driver transistor M_{21}, Al-Shyoukh's buffer is "gm enhanced" because it receives a gm boost from a current feedback circuit comprising M_{24} and M_{25}, as detailed above. (Section

Pet. (Paper 1), 16 (Al-Shyoukh ground)

Dr. Chen Conflates "gm-boost" and "gm-enhance[ment]"



Q. How is the claim gm-boost different from the claim gm enhancement?

A. As I mentioned exactly on page 25, you -- because you have this feedback circuits, you have gm-boost, right, and as a result you increase the current for that for the buffer transistors. So you enhance that gm and that's how I understand a gm enhanced.

So you almost think that as outcome of that gm-boost.

EX2018 (Dr. Chen), 251:9-19

Dr. Chen Conflates “gm-boost” and “gm-enhance[ment]”



Q. Yeah, and my question is a little bit different, which is simply looking at Claim 1 are gm enhancement and gm-boost the same thing or are they different?

MR. LIU: Objection to form.

A. Sitting here, I don't recall that the '074 actually defined gm enhanced or gm-boost separately. But it's my understanding that I show in the report because you do the gm-boost, you increase the current, you know, particularly to the transistor M21, and hence you increase the gm. That's how I understand this enhanced -- or sorry, the gm enhanced buffer.

EX2018 (Dr. Chen), 249:8-22

Dr. Chen Conflates "gm-boost" and "gm-enhance[ment]"



Q. My question was not about gm-boost. It was about gm enhancement. What transistor in Al-Shyoukh Figure 8 performs gm enhancement?

A. So counsel, as I mentioned before, the way I understand the gm enhance is the outcome of the gm-boost because you increase the current through this M21. That's why the gm increase, that's why you are gm enhanced.

So gm enhanced is outcome of the circuit that we built. That's the way I understand it.

EX2018 (Dr. Chen), 252:15-253:2

The ID Recognized Petitioner Did Not Construe "gm enhance[ment]"

C.F.R. § 42.100(b). However, it appears at this stage that Petitioner relies on Dr. Chen's expertise to interpret the prior art and the '074 specification, but not to interpret the claim language. *See, e.g.*, Pet. 16–17, 20–22, 26–27, 31, 36–38, 46–48, 58, 62, 70–71, 75, 83–84. Thus, this error does not affect our determination of whether Petitioner is reasonably likely to prevail with respect to at least one of the challenged claims.

ID (Paper 11), 12-13

Rincon-Mora ("gm-enhanced")

Al-Shyoukh ("gm-enhanced")

The Petition Fails to Show "gm enhance[ment]"

- Having conflated "gm-boost" with "gm enhance[ment]," the Petition fails to show how the "gm enhance[ment]" limitation is met
  - *See* Pet. 16-17 (Al-Shyoukh)
  - *See* Pet. 58-59 (Rincon-Mora)
- Petitioner's element 1[b] analysis focused on why "current buffer" read on a "voltage buffer" (an issue not in dispute here)

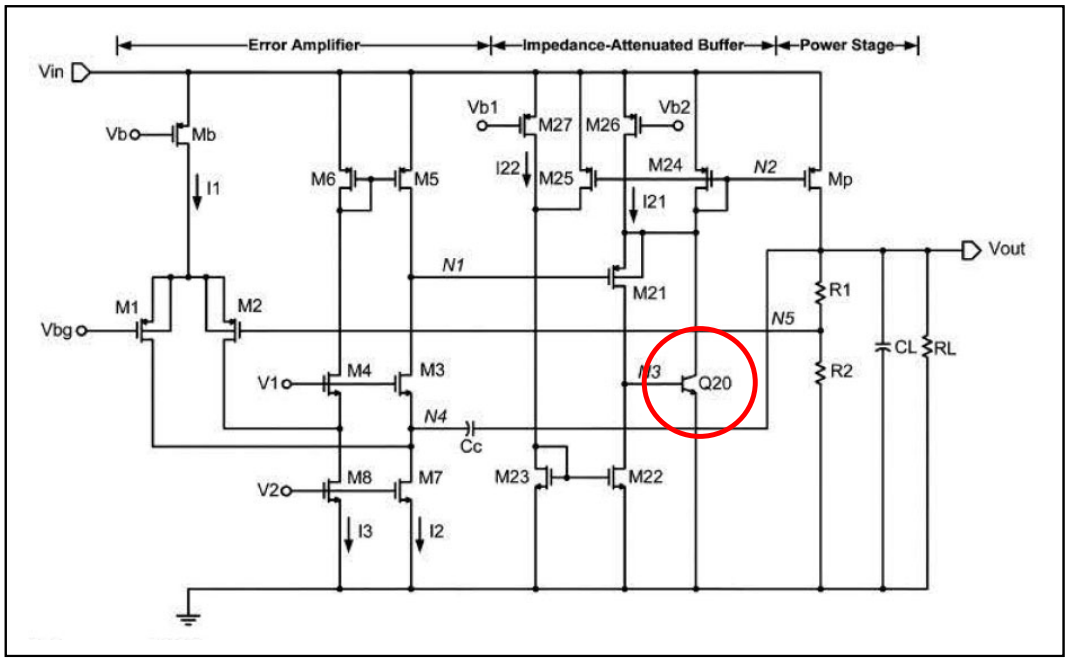
Petitioner's Reply Argument is Procedurally Improper and Fails on the Merits

- Petitioner's Reply (§II.E) raised a new Al-Shyoukh invalidity theory in which "transistor Q20 is now included in the buffer driver" (Reply, 10)
  - Petitioner does not raise a new theory for Rincon-Mora
- Patent Owner moved to strike Petitioner's new theory as untimely and improper (Paper 27)
- Petitioner's new Al-Shyoukh theory fails on the merits (Sur-reply, 9-11)

Reply (Paper 25), 9-11; Motion to Strike (Paper 27); Sur-reply (Paper 29), 9-11

Petitioner's Untimely Reply Theory

- In Petitioner's new theory, the "portion representing the buffer driver has been expanded to include transistor Q20" (EX1028 (Chen), ¶13)



Al-Shyoukh (EX1004), Fig. 8 (annotated)

Patent Owner's New Take on "gm-enhancement" Fails

> Thus, if "gm enhancement" entails a second transistor helping to charge or discharge the source node of the driver, Al-Shyoukh discloses it. (EX1028 ¶¶ 12-15.)

Reply (Paper 25), 11

Patent Owner Prevails Even Under Petitioner's New Theory

Regardless, Petitioner's new Al-Shyoukh theory (Reply, §II.E) fails on the merits. Petitioner glosses over the distinction—at the heart of PO's construction—between raising overall current (*gm-boost*) to increase gm and re-allocating existing current (*gm-enhance[ment]*) to increase gm. Reply, 11. Instead, Petitioner reframes *gm-enhance[ment]* as merely "entail[ing] a second transistor helping to charge or discharge the source node of the driver." Reply, 10-11. That is incomplete and insufficient.

Sur-reply (Paper 29), 10

Patent Owner Prevails Even Under Petitioner's New Theory

Nor does Dr. Chen discuss the key concept of current re-allocation.

EX1028, ¶¶12-15. Rather, Dr. Chen relies (¶14) on the "descri[ption] for the '074 patent" provided Dr. Taylor's declaration, ¶79. But this is the passage Dr. Chen misunderstood (or at least mischaracterized vis-à-vis node B "respond[ing] slowly") in his reply declaration at §I.A. Given that Dr. Chen fundamentally misunderstands the circuit's operation and fails to address the key distinction between ***gm-boost*** and ***gm-enhance[ment]***, his testimony (even if considered) cannot help Petitioner. Moreover, Dr. Chen's new testimony is fundamentally

Sur-reply (Paper 29), 10-11

The Board Should Strike Petitioner's New Reply Argument

It is well established a Petitioner must make out its case in the Petition, and is prohibited from introducing new invalidity theories in reply. *See* 2019 Consolidated Trial Practice Guide, 74. There is no dispute the Petition never pointed to Al-Shyoukh transistor Q20 for the ***gm-enhance[ment]*** limitation. Nevertheless, Petitioner's Reply (§II.E) introduces a new invalidity theory—pointing to transistor Q20 for the first time—for why Al-Shyoukh satisfies the ***gm-enhance[ment]*** limitation. This is improper.

Motion to Strike (Paper 27), 2

The *Axonics* Case is Distinguishable

Petitioner seeks to justify its new Reply theory by citing *Axonics, Inc. v. Medtronic, Inc.*, 75 F.4th 1374 (Fed. Cir. 2023), which allowed a reply brief to map the prior art under a patent owner's construction. Reply, 9. But *Axonics* is readily distinguishable because "[t]he Board made no finding that [petitioner] clearly anticipated the two-input construction." *Axonics*, 1374 F.4th at 1383 (n.10). Here, by contrast, the Board can—and should—make such a finding (*viz.*, Petitioner should have known different claim terms connote different meanings). *See* §I.

Motion to Strike (Paper 27), 2-3

The *Axonics* Court's Reasoning Favors Patent Owner

> The Federal Circuit's reasoning in *Axonics* favors PO here. The Federal Circuit was concerned that "[b]arring argument and evidence in a reply directed to a new claim construction proposed by the patent owner would create opportunities for sandbagging by the patent owner." *Axonics*, 1374 F.4th at 1384. Here, it is Petitioner—not PO—that sought a tactical advantage by sandbagging (*viz.*, avoiding claim construction in a manner contrary to well-established claim construction principles to shift the burden to PO to explain the terms and disclose its position first, and only then introduce Petitioner's invalidity theory). 37 CFR §42.104(b)(3); *CAE Screenplates*, 224 F.3d at 1317.

Motion to Strike (Paper 27), 3

FAILURE TO SHOW "BIASING CIRCUIT … TO SET A BIASING RATIO FOR GM-BOOST"

’074 Patent Independent Claim 1

Missing from the prior art

1. A voltage regulator, comprising:

an operational amplifier;

a gm enhanced current buffer driver;

a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver;

an enable/disable function to enable/disable the biasing circuit for reducing standby current:

an output power driver, wherein the current buffer driver is coupled between the operational amplifier and the output power driver;

a current feedback circuit coupled between the output power driver and the current buffer driver; and

a feedback loop coupled between the output power driver and the operational amplifier.

EX1001, cl. 1

Petitioner's Argument Fails for Three Separate Reasons

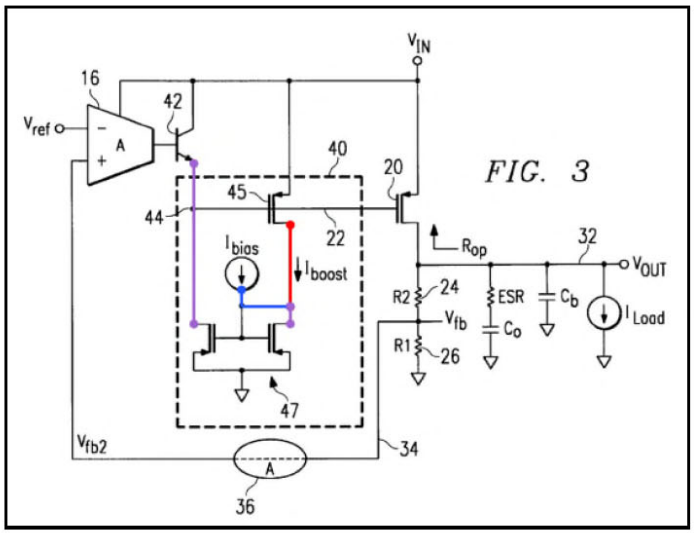
- Petitioner ***inconsistently maps the "biasing circuitry"*** for elements 1[c] and 1[d], but they must be the same circuit
- Petitioner draws a ***false equivalency*** to '074 circuitry which itself does not "set a biasing ratio for gm-boost"
- Petitioner's mapping does not "***set*** a biasing ratio …" because it ***compares fixed and variable currents***, making any ratio arbitrary

The "Biasing Circuit" Claim Language – Just One "Biasing Circuit"

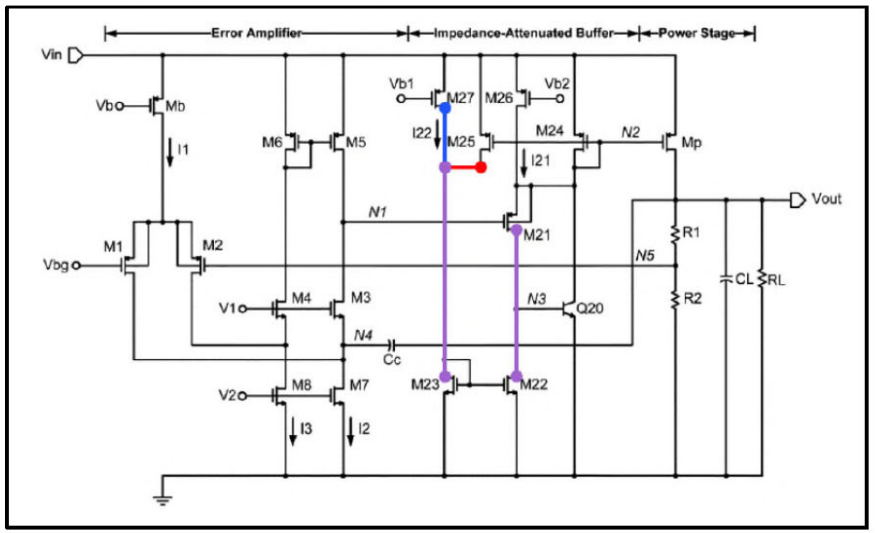
- The claimed "***biasing circuit***" must be the same for both 1[c] and 1[d]
- The antecedent basis for "***the*** biasing circuit" in element 1[d] refers to "biasing circuit" introduced in element 1[c] ("***a*** biasing circuit …")
  - 1[c] requires the biasing circuit "to set a biasing ratio for gm-boost"
  - 1[d] requires enabling/disabling ***the same biasing circuit***

The Petition Fails to Identify the "Biasing Circuit"

- The "biasing circuit" is ***a circuit***, but the Petition points to ***currents***



Pet., 61 (Rincon-Mora)
(annotated by Petitioner)



Pet., 19 (Al-Shyoukh)
(annotated by Petitioner)

Dr. Chen Admits Rincon-Mora and Al-Shyoukh Do Not Show a "Biasing Circuit"



Q. You would agree with me that either Rincon-Mora nor Al-Shyoukh discloses Element 1D, correct?

A. Rincon-Mora and --

MR. LIU: Objection to form.

A. To the extent that they show, I cannot see, even see the biasing circuits. So there's -- unfortunately I cannot, you know, make that judgment. I don't see that, you know, based on the information you provide.

EX2018 (Dr. Chen), 225:6-20

Dr. Chen Admits Rincon-Mora and Al-Shyoukh Do Not Show a "Biasing Circuit"



A. I believe I mentioned that before. Because they do not show the biasing circuits, both Rincon-Mora and Al-Shyoukh, and that's why I cannot make that decision or judgment to even look for those enable and disable signals.

EX2018 (Dr. Chen), 254:1-6

POR (Paper 19), 48 (citing EX2014 (Dr. Chen), 254:1-6)

Dr. Chen "Identifies" the Claimed "Biasing Circuit" (Rincon-Mora)



Q. What do you identify, if anything, in Rincon-Mora Figure 3 as the claimed biasing circuit that is recited in Claim Element 1C?

A. So that would be the blue box that you highlight earlier. Because you can see that bias current eventually will be coupled to the buffer driver 42. Yes.

Q. Okay. So I've placed a blue box around the I-Bias that you referenced, correct?

A. Correct.

EX2018 (Dr. Chen), 213:3-14

Dr. Chen "Identifies" the Claimed "Biasing Circuit" (Rincon-Mora)



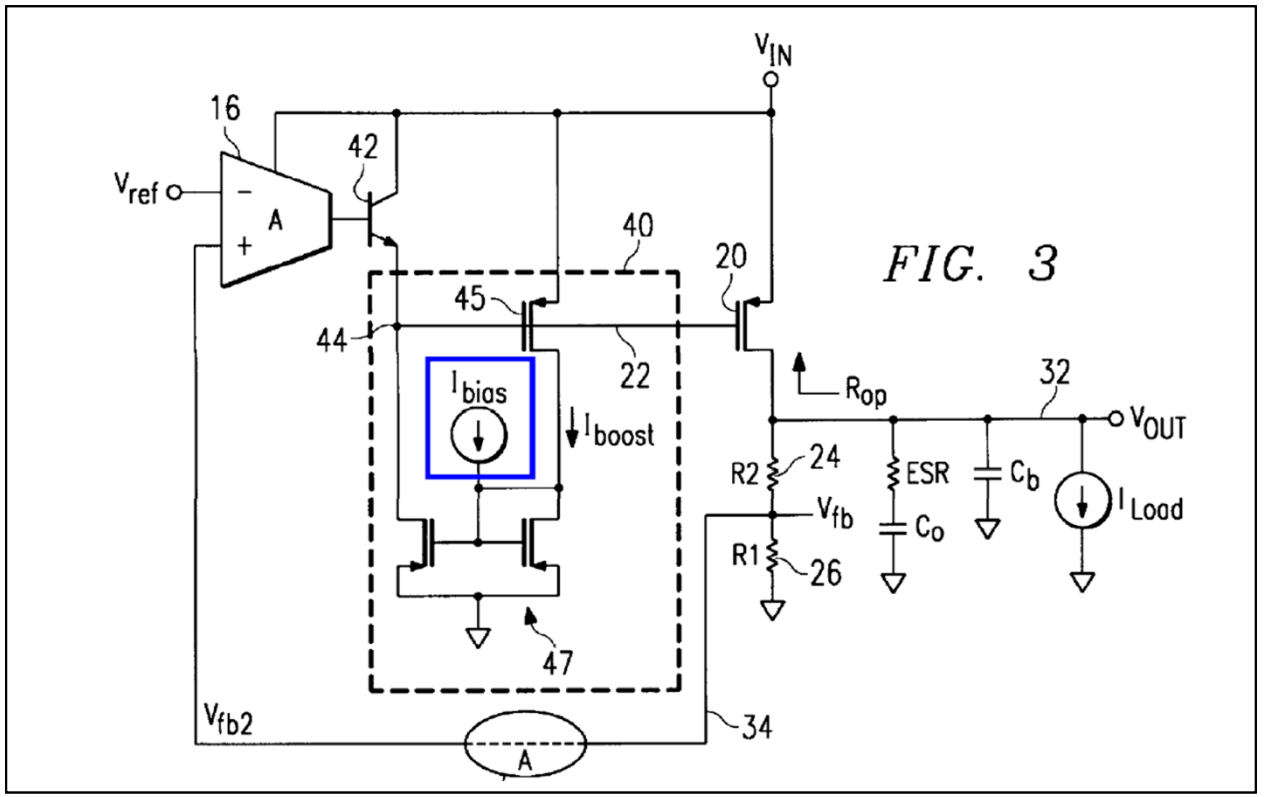


FIG. 3

EX2014 (Rincon-Mora), Fig. 3 (annotated at Chen deposition)

Dr. Chen "Identifies" the Claimed "Biasing Circuit" (Al-Shyoukh)



Under the first interpretation that you offer, what transistors do you map to the biasing circuit in Al-Shyoukh Figure 8?

A. Again, in the first interpretation, right, the biasing circuits is consists of Vb1 because that drive the gate of M27. So that's where we identify, you know, as that biasing circuits.

EX2018 (Dr. Chen), 222:7-223:7

Dr. Chen "Identifies" the Claimed "Biasing Circuit" (Al-Shyoukh)



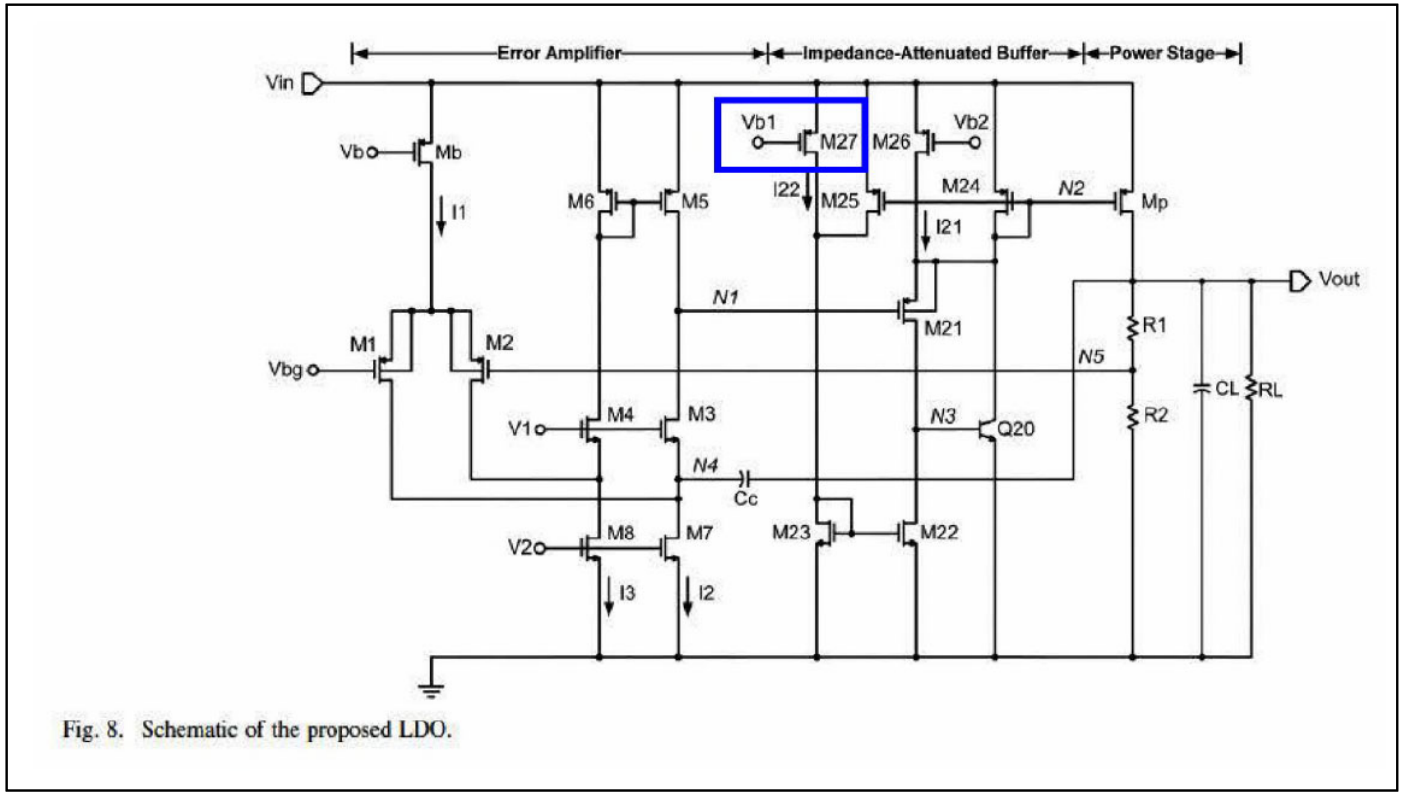


Fig. 8. Schematic of the proposed LDO.

EX2015 (Al-Shyoukh), Fig. 8 (annotated at Chen deposition)

Dr. Chen's "Biasing" Transistors Do NOT "set a biasing ratio *for gm-boost*"



Q. And which two currents in Al-Shyoukh Figure 8 set the claimed biasing ratio under your first interpretation?

A. Counsel, that's what I mentioned earlier. In the first interpretation, the transistor M23, M22 now we're determining the current ratio.

EX2018 (Dr. Chen), 247:21-248:2

1. **This is different than the "biasing circuit" Patent Owner cites elsewhere**

2. **Petitioner's off-chip "bias circuit" does not "set a biasing ratio for gm-boost"**

Petitioner's Argument Fails for Three Separate Reasons

- Petitioner ***inconsistently maps the "biasing circuitry"*** for elements 1[c] and 1[d], but they must be the same circuit
- Petitioner draws a ***false equivalency*** to '074 circuitry which itself does not "set a biasing ratio for gm-boost"
- Petitioner's mapping does not "***set*** a biasing ratio …" because it ***compares fixed and variable currents***, making any ratio arbitrary

Petitioner Maps to the Wrong Circuitry in the '074 Patent

"[Al-Shyoukh] matches the patent's description of a bias network 'fixed by transistor 396' such that the current from the network is 'ratio'ed in transistors 368 and 370' with a feedback current."

Pet. (Paper 1), 17-18

"The same occurs in Rincon-Mora's LDO."

Id., 60

Pet. (Paper 1), 17-18 and 59-61

"Set[ting] the Biasing Ratio for gm-boost " in the '074 Patent

[7] The '074 bias circuitry that ***set[s] the biasing ratio for gm-boost*** (the ratio of boost current through source follower 384 to the regulator output current) comprises transistors 378, 380, 394, and 402. Because current is proportional to transistor width, the ratio would be $\frac{378*394}{380*402}$, where transistor numbers represent each transistor's respective width.

Sur-reply (Paper 29), 13

Petitioner's Argument Fails for Three Separate Reasons

- Petitioner ***inconsistently maps the "biasing circuitry"*** for elements 1[c] and 1[d], but they must be the same circuit
- Petitioner draws a ***false equivalency*** to '074 circuitry which itself does not "set a biasing ratio for gm-boost"
- Petitioner's mapping does not "***set*** a biasing ratio …" because it ***compares fixed and variable currents***, making any ratio arbitrary

Petitioner's "Biasing Circuit" Does NOT "set a biasing ratio for gm-boost"

current in the output transistor to the buffer driver. Taylor, ¶¶80, 118. Petitioner's expert (Dr. Chen) acknowledges as much. *See* EX1002, ¶¶145-146 (discussing the "ratio between [Rincon-Mora] transistors 20 [the output driver] and 45 [the buffer driver]"). Petitioner's problem is that the ***biasing circuit*** Petitioner relies on (for both Rincon-Mora and Al-Shyoukh) does not ***set a biasing ratio for gm-boost of the current buffer driver***.

POR (Paper 19), 46

Petitioner's "Biasing Circuit" Does NOT "set a biasing ratio for gm-boost"

> Regardless of whether the not-shown ***bias[] circuit*** comes from Ivanov or not, it makes no difference since such circuitry would simply generate a reference voltage for the Rincon-Mora and Al-Shyoukh regulator circuits, which is not what the claims require. Taylor, ¶¶114, 120.

POR (Paper 19), 46

Petitioner's "Biasing Circuit" Does NOT "set a biasing ratio for gm-boost"

current in the output transistor to the buffer driver. Taylor, ¶¶80, 118. Petitioner's expert (Dr. Chen) acknowledges as much. *See* EX1002, ¶¶145-146 (discussing the "ratio between [Rincon-Mora] transistors 20 [the output driver] and 45 [the buffer driver]"). Petitioner's problem is that the ***biasing circuit*** Petitioner relies on (for both Rincon-Mora and Al-Shyoukh) does not ***set a biasing ratio for gm-boost of the current buffer driver***.

POR (Paper 19), 46

Petitioner's "Biasing Circuit" Does NOT "set a biasing ratio for gm-boost"

122. Thus, the "bias circuit" (*viz.*, the I_{bias} block) is completely independent of the bias ratio between Rincon-Mora's transistors 20 and 45. At most, Petitioner posits a circuit coupled to another/different circuit that ***set[s] a biasing ratio***, but which does not itself participate in set[ting] a bias ratio. *Id.* Thus, Petitioner has failed to show Ground I satisfies element 1[c].

POR (Paper 19), 50

Petitioner's "Biasing Circuit" Does NOT "set a biasing ratio for gm-boost"

Petitioner contends "a bias current I_{bias} [] is mirrored in current mirror 47 to set a biasing ratio for gm-boost." Pet., 59; *see also id.*, 61 ("This sum current is 'ratio'ed' in current mirror 47"). To the extent Petitioner and Dr. Chen rely on comparing Rincon-Mora's current mirror 47 transistors to the purportedly "ratio'ed in transistors 368 and 370" (*see* Pet., 59) in Fig. 3 of the '074 patent, they draw a false comparison as those transistors are not what ***set[s] a biasing ratio for gm-boost of the current buffer driver***. Taylor, ¶¶120-122. Accordingly, this argument fails for the same reason above.

POR (Paper 19), 50

THE BOARD SHOULD DENY PETITIONER'S MOTION TO EXCLUDE/STRIKE

The Board Should Deny Petitioner's Motions to Strike/Exclude

Patent Owner ("PO") respectfully submits this Opposition to Petitioner's Motion to Strike (Paper 33, the "Motion" or "Mot."). The Board should deny Petitioner's Motion for at least three reasons. *First*, Petitioner opened the door to the line of argument it complains about at Dr. Taylor's deposition and then elected not to ask follow-up questions on re-cross. §I. *Second*, the Sur-reply properly responds to arguments raised in the Reply. §II. *Third*, Petitioner applies the wrong temporal reference point (and thus engages in legal error) by ignoring that obviousness is assessed as of the priority date ***of the challenged patent***. §III.

PO's Opposition to Motion to Strike (Paper 37), 1

Petitioner Asked Dr. Taylor About Quiescent Current



25	Q.	And are there certain component characteristics	12:30:04
1	or parameters that would affect quiescent current?		12:30:10
2	A.	Yes.	12:30:13
3	Q.	And what are those?	12:30:14
4	A.	The precise values of the resistors, the leakage	12:30:17
5	in the transistors.	We talked earlier about operating	12:30:23
6	points. And so the resistors are here to establish		12:30:29

EX1029 (Taylor), 91:25-92:22

Petitioner Asked Dr. Taylor About Transistor Size Impact on Quiescent Current



20	Q.	Do the -- the sizes of the transistors affect	12
21	quiescent current?		12:31:35
22	A.	Yes.	12:31:35
23	Q.	And you're not assuming all the transistors are	
24	the same size?		12:31:43
25	A.	I know they're not. Some of the transistors are	

EX1029 (Taylor), 91:25-92:22

’074 Patent Independent Claim 1

Missing from the prior art

Missing from the prior art

No motivation to combine

1. A voltage regulator, comprising:
an operational amplifier;
a gm enhanced current buffer driver;
a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver;
an enable/disable function to enable/disable the biasing circuit for reducing standby current:
an output power driver, wherein the current buffer driver is coupled between the operational amplifier and the output power driver;
a current feedback circuit coupled between the output power driver and the current buffer driver; and
a feedback loop coupled between the output power driver and the operational amplifier.

EX1001, cl. 1

THANK YOU

CERTIFICATE OF SERVICE

The undersigned certifies that on June 24, 2025 a copy of the following was served in its entirety via electronic mail, upon the following attorneys of record for Petitioner:

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