

Petitioner's Demonstratives

Aptiv Services US LLC v. Microchip Technology Inc.

IPR2024-00646

U.S. Patent No. 9,471,074

June 27, 2025

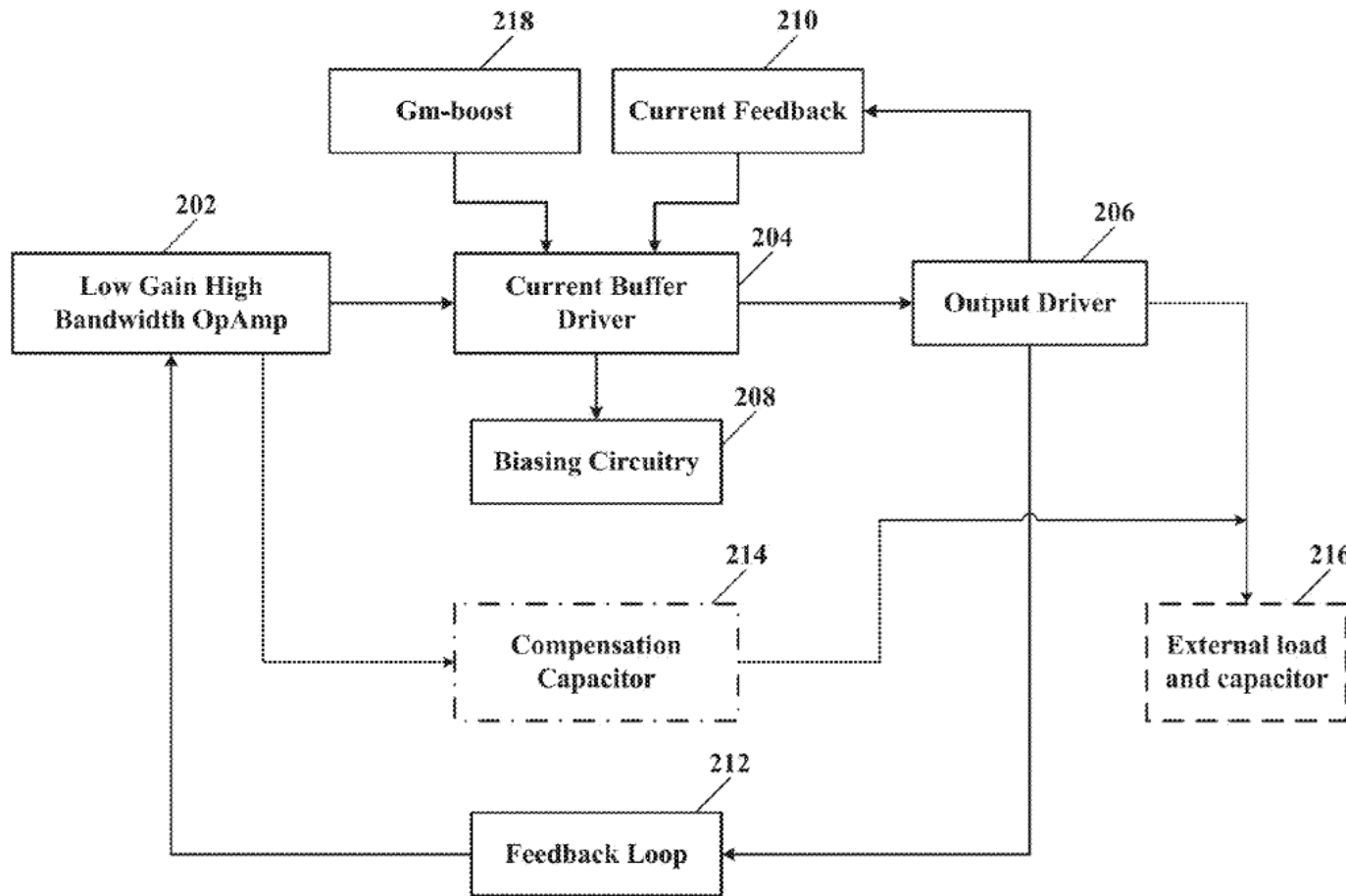
Instituted Grounds

Claims Challenged	35 U.S.C. §	References
1-18	103(a)	<u>Al-Shyoukh</u> , Ivanov, Stanescu
1-18	103(a)	<u>Rincon-Mora, Rincon-Mora Paper</u> , Al-Shyoukh, Ivanov, Stanescu

Roadmap

- **Claim 1[b]: a “gm enhanced” current buffer driver**
- **Claim 1[c]: “biasing ratio”**
- **Claim 1[d]: motivation to add “enable/disable”**

The '074 Patent



EX1001, Fig. 2

1. A voltage regulator, comprising:
 - an operational amplifier;
 - a gm enhanced current buffer driver;
 - a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver;
 - an enable/disable function to enable/disable the biasing circuit for reducing standby current;
 - an output power driver, wherein the current buffer driver is coupled between the operational amplifier and the output power driver;
 - a current feedback circuit coupled between the output power driver and the current buffer driver; and
 - a feedback loop coupled between the output power driver and the operational amplifier.

EX1001, Claim 1

Petition (Paper 1), 4-7

Claim 1[b] a “gm enhanced” current buffer driver

Claim 1

1. A voltage regulator, comprising:
 - an operational amplifier;
 - 1[b] a gm enhanced current buffer driver;
 - 1[c] a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver;
 - an enable/disable function to enable/disable the biasing circuit for reducing standby current;
 - an output power driver, wherein the current buffer driver is coupled between the operational amplifier and the output power driver;
 - a current feedback circuit coupled between the output power driver and the current buffer driver; and
 - a feedback loop coupled between the output power driver and the operational amplifier.

Petition: “gm boost” → “gm enhanced”

[b] a gm enhanced current buffer driver;

Al-Shyoukh’s buffer driver discloses this limitation. Centered on the driver transistor M₂₁, Al-Shyoukh’s buffer is “gm enhanced” because it receives a gm boost from a current feedback circuit comprising M₂₄ and M₂₅, as detailed above. (Section IV.A.1, *supra*; EX1004, 1733-35, Figs. 3, 4, 8; *see also* EX1002 ¶ 53.)

[b] a gm enhanced current buffer driver;

Rincon-Mora’s buffer driver is “gm enhanced” because the transient boost circuit, comprising transistor 45 and current mirror 47, increases its gm. (See Section IV.B.1, *supra*; EX1013, 3:38-43, 4:33-38, 5:10-13, 7:42-44, Fig. 3; *see also* EX1002 ¶¶ 126-36, 142-44.)

“gm” in the '074 Patent

According to a further embodiment, a gm-boost circuit may be coupled to the current buffer driver. According to a further embodiment, the gm-boost circuit increases the current buffer driver input impedance. According to a further embodiment, the gm-boost circuit enables the current buffer driver to have a large gm value. According to a further embodiment, a biasing circuit may be coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver. According to a further embodiment, an enable/

EX1001, 2:1-9

splitting effect. To achieve this, it is necessary to provide a fairly large gm value of the current buffer driver 204. The gm-boost circuit 218 may provide a gm-boost technique that will increase the impedance value of the current buffer driver 204 with the help of the current feedback 210 which may sense the current change at the output of the output driver 206. The current feedback 210 also may behave like a

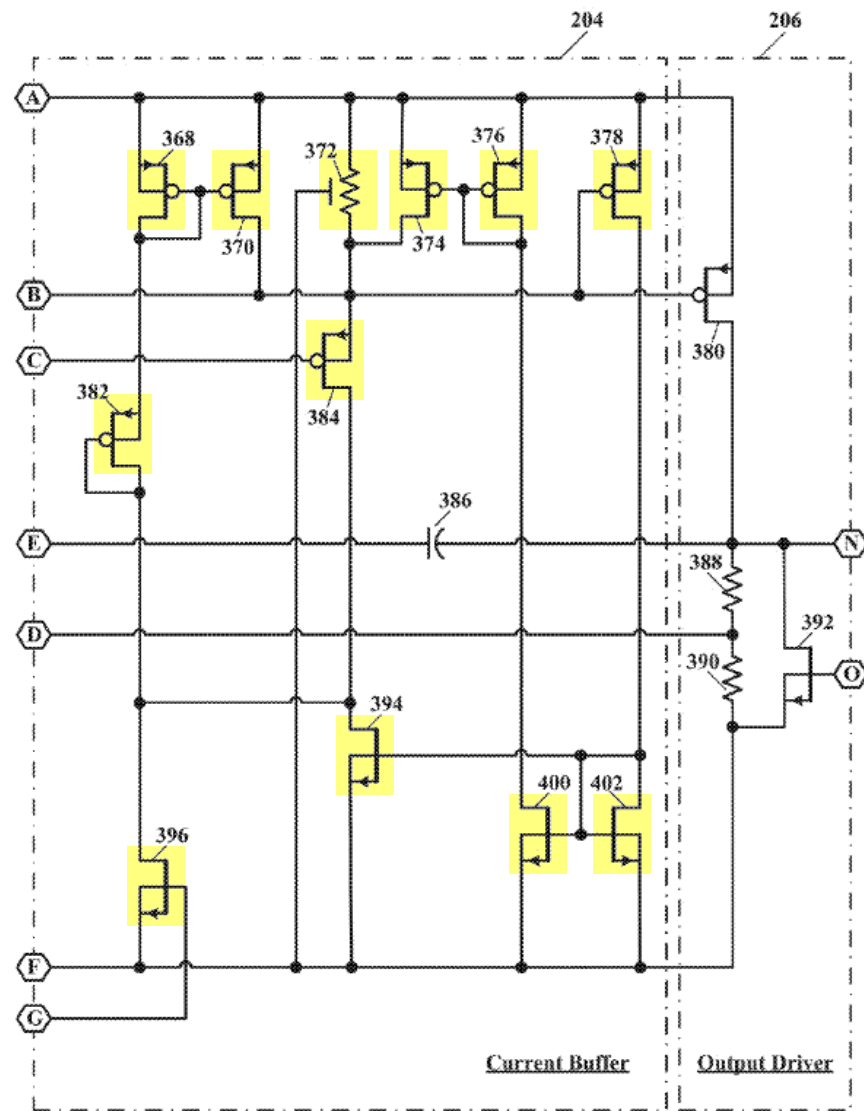
EX1001, 4:14-20

(OpAmp 202, FIG. 3A, node C). By literally pushing the pole at the gate of transistor 380 to a high frequency domain, effectively leaves the only dominant pole at the output (node C) of the OpAmp 202 during full-load conditions. To achieve such operation, a gm-boost stage may be used.

EX1001, 5:3-7

Reply (Paper 25), 5-6

'074 Patent: "gm-boost"



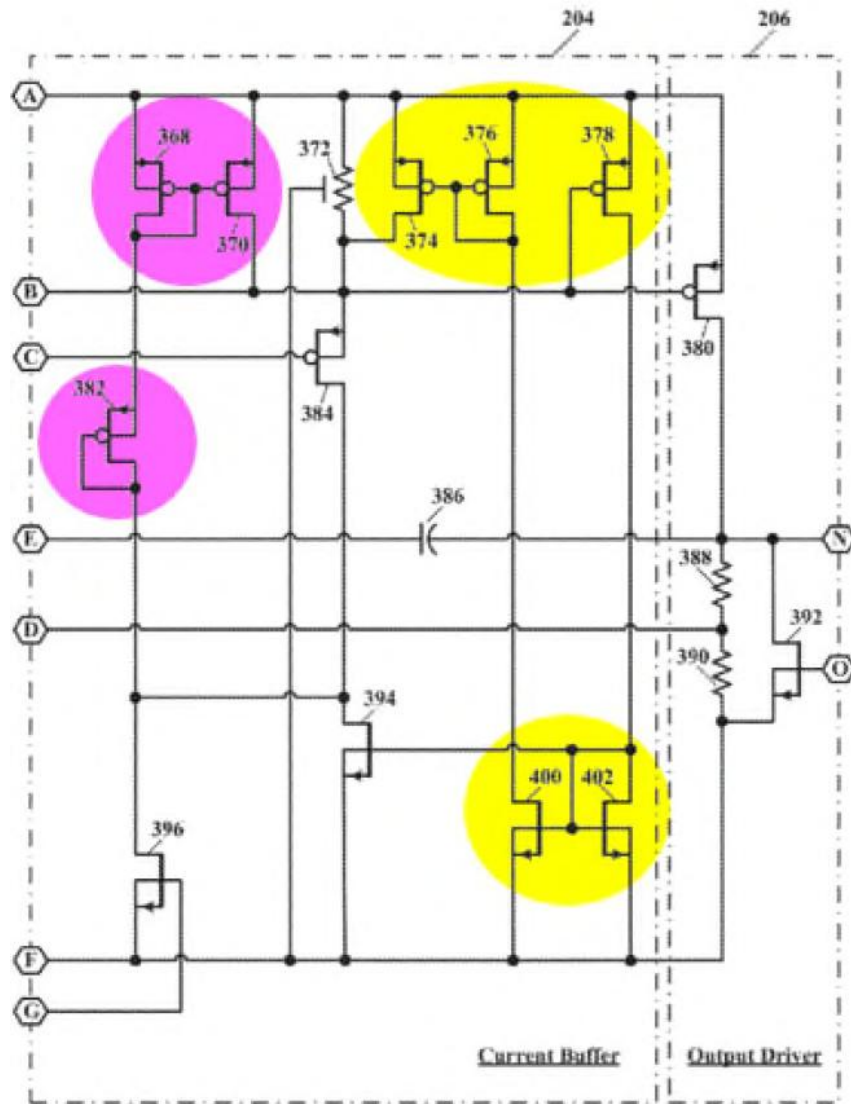
The gm-boost stage 218 may comprise transistors 368, 370, 374, 376, 378, 382, 396, 394, 400, 402, 384 and resistor 372 shown in FIG. 3B of the current buffer 204. The current

EX1001, 5:8-10

EX1001, Fig. 3B

Reply (Paper 25), 3

Patent Owner: “gm-boost” + “gm-enhancement”



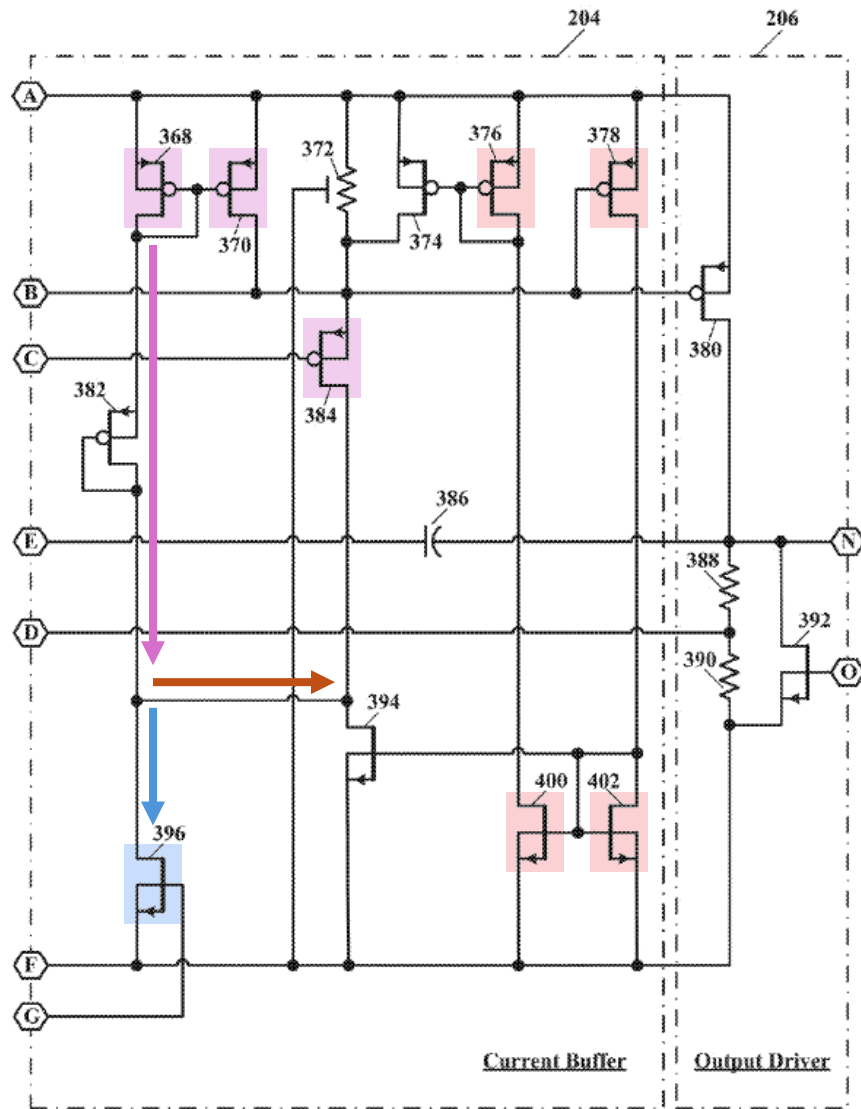
be more specific. The gm-boost circuitry is highlighted in yellow, and the gm-enhancement circuitry in pink. As shown, the gm-boost circuitry relies on current feedback from output buffer 380. In contrast, the gm-enhancement circuitry in pink does not. While both techniques serve to increase the gm of transistor 384, they do so in fundamentally different ways. One (gm-boost) acts to increase gm by adding current through transistor 384, while the other (gm-enhancement) increases gm by steering current around transistor 384. Taylor, ¶¶75, 87, 66-71.

POR (Paper 19), 18

POR (Paper 19), 18

Reply (Paper 25), 2-3

'074 Patent: Current Feedback to 368/370



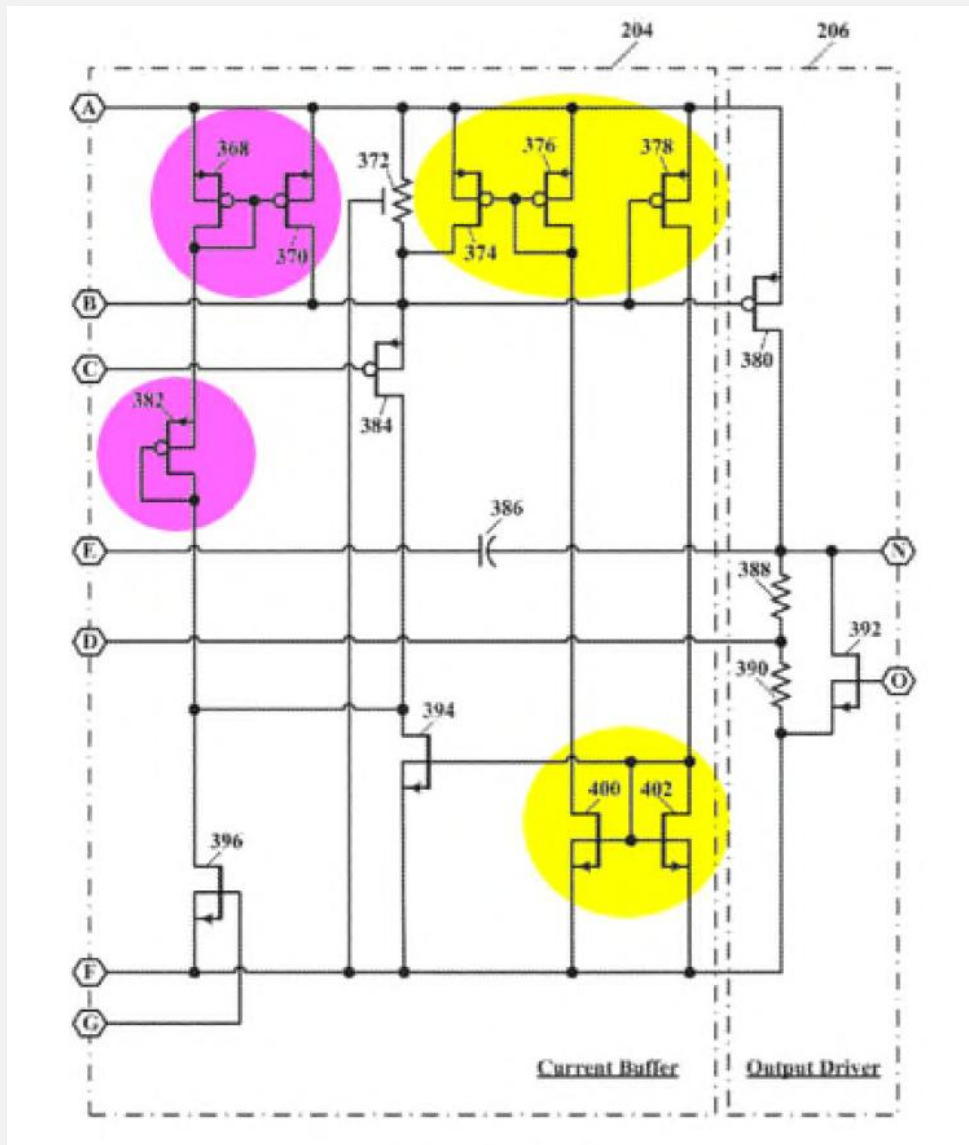
current buffer 204. The gm of the PMOS current buffer driver 204 may comprise transistor 384 and may be coupled to two sources of currents, one from the bias network and the other as current feedback 210 comprising transistors 378, 400, 402 and 376 from the power output stage 206 that may comprise transistor 380. The bias network may be fixed by transistor 396. Then these currents are ratio'd in transistors 368 and 370 to provide a sufficient amount of current for the driver transistor 384 but not enough to increase more current based upon a limited current mirror by transistor 396.

EX1001, 5:15-24

EX1001, Fig. 3B

Petition (Paper 1), 6-7, 17-19, 59-60
Reply (Paper 25), 4-5

Patent Owner: No Current Feedback to 368/370



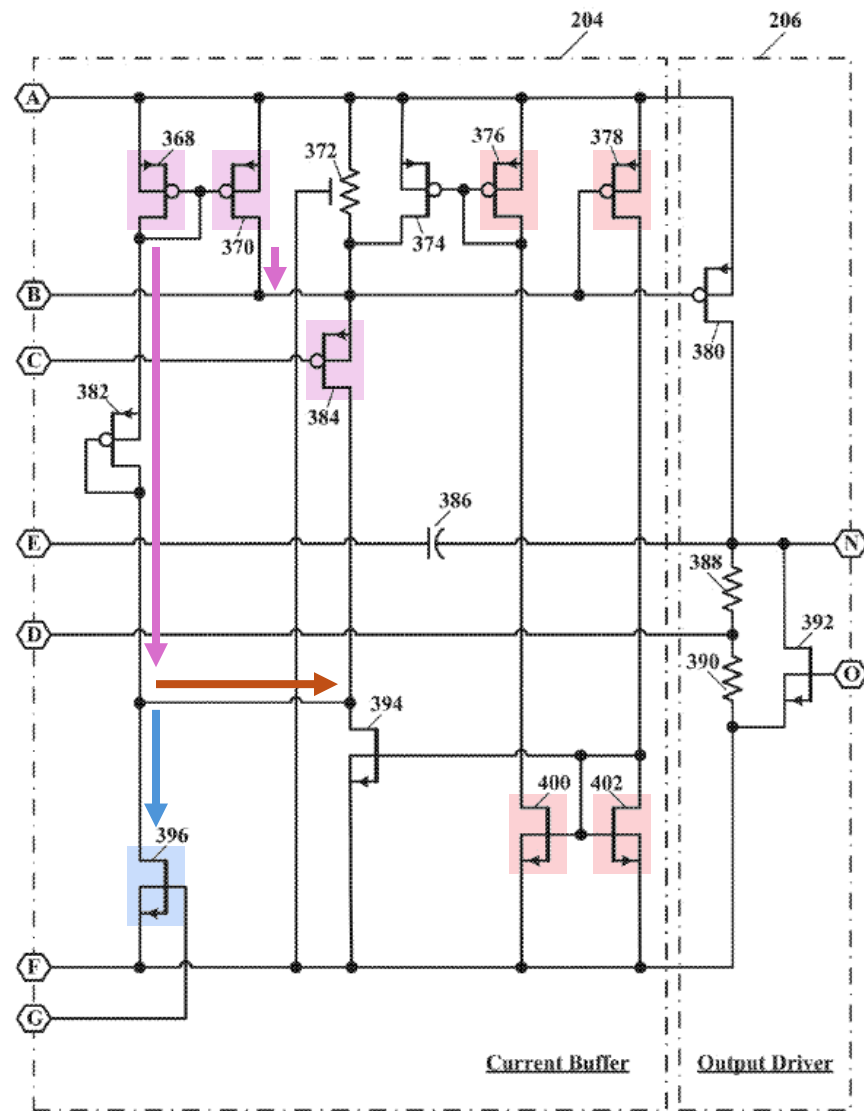
be more specific. The gm-boost circuitry is highlighted in yellow, and the gm-enhancement circuitry in pink. As shown, the gm-boost circuitry relies on current feedback from output buffer 380. In contrast, the gm-enhancement circuitry in pink does not. While both techniques serve to increase the gm of transistor 384, they do so in fundamentally different ways. One (gm-boost) acts to increase gm by adding current through transistor 384, while the other (gm-enhancement) increases gm by steering current around transistor 384. Taylor, ¶¶75, 87, 66-71.

POR (Paper 19), 18

POR (Paper 19), 18

Reply (Paper 25), 4

'074 Patent: 368/370 Provide "Sufficient Amount of Current" to 384



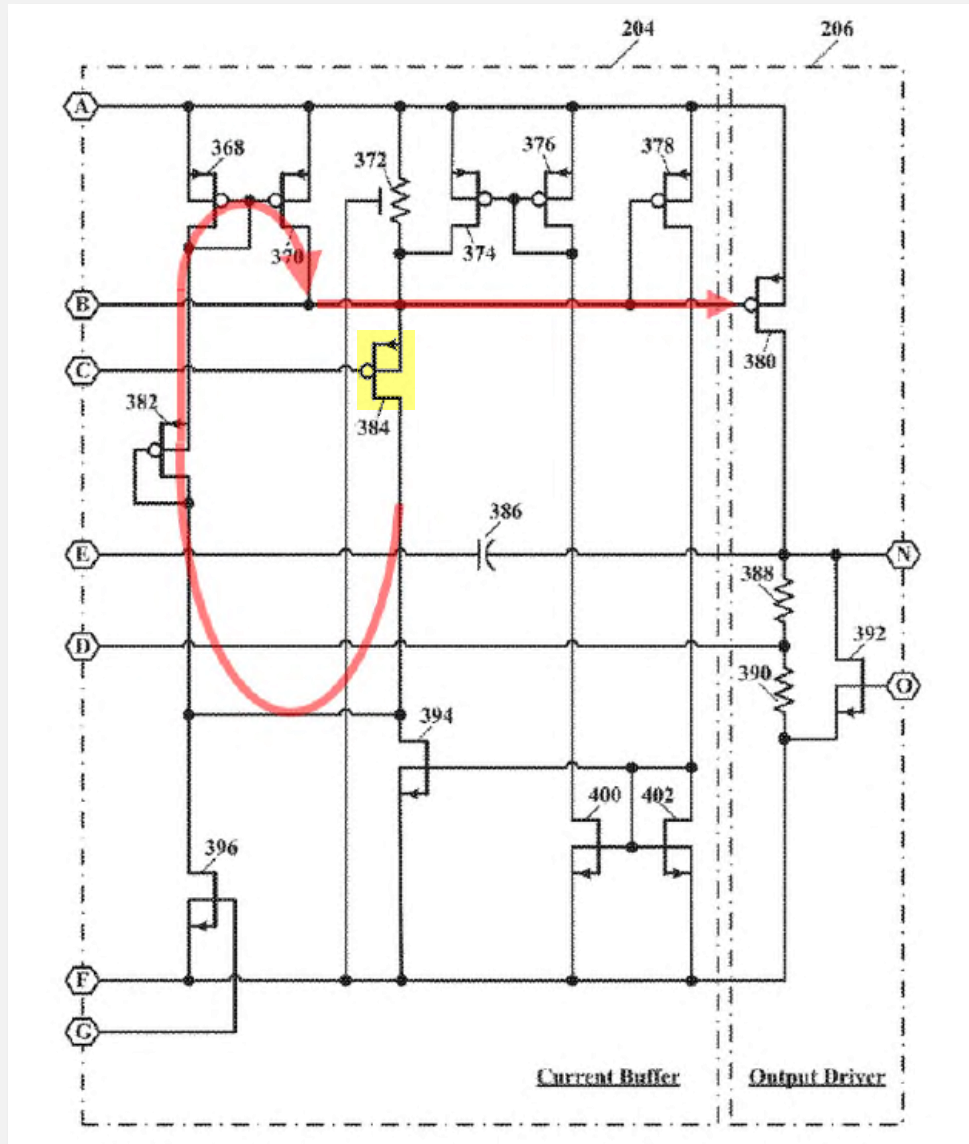
current buffer 204. The gm of the PMOS current buffer driver 204 may comprise transistor 384 and may be coupled to two sources of currents, one from the bias network and the other as current feedback 210 comprising transistors 378, 400, 402 and 376 from the power output stage 206 that may comprise transistor 380. The bias network may be fixed by transistor 396. Then these currents are ratio'd in transistors 368 and 370 to provide a sufficient amount of current for the driver transistor 384 but not enough to increase more current based upon a limited current mirror by transistor 396.

EX1001, 5:15-24

EX1001, Fig. 3B

Reply (Paper 25), 4

Patent Owner: 368/370 “Redirect” or “Allocate” Current from 384



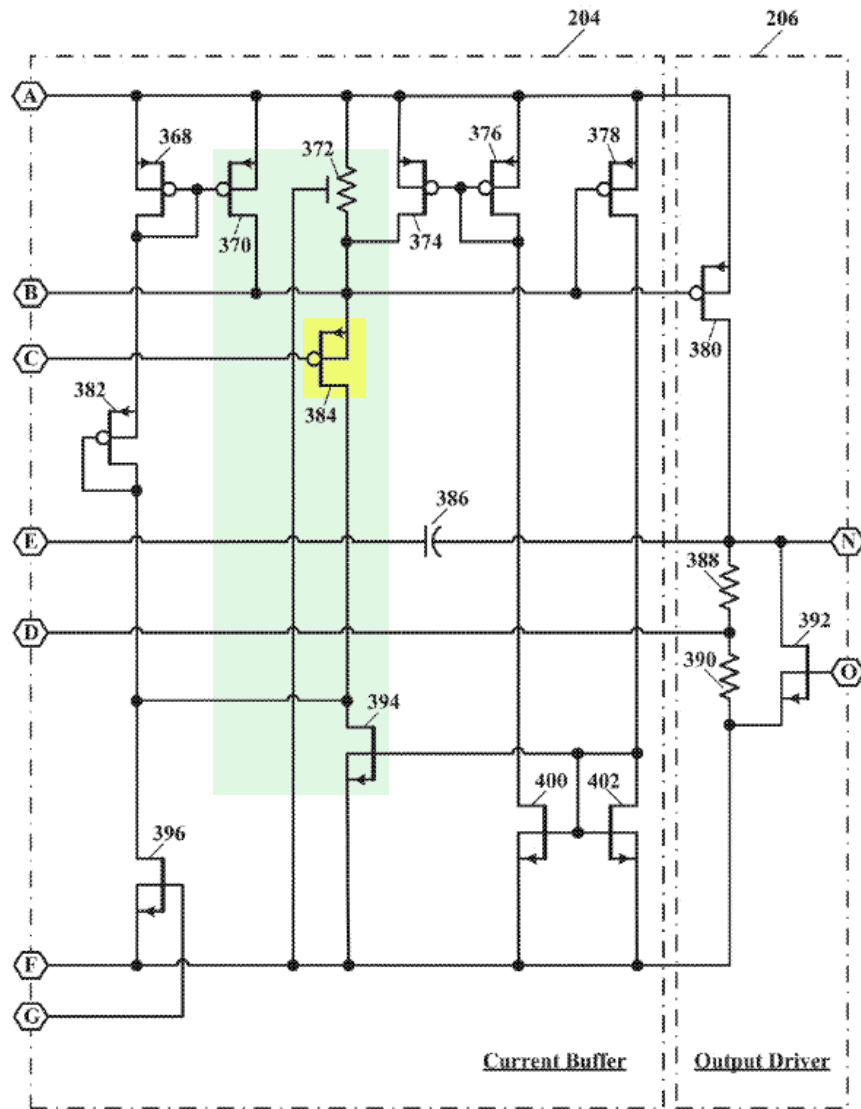
If the voltage on node C rises, the current through source follower 384 is reduced (because it is a PMOS transistor), causing the excess bias current to be redirected through current mirror 368/370 into node B (viz., the gate capacitance of the power output transistor 380). Taylor, ¶86. Where PMOS transistors 368 and (which employs a different mechanism). *Id.*, ¶¶83-87, 75-81, 66-71. In other words, gm-boost changes the overall *magnitude* of the standing current, whereas gm-enhancement changes the *allocation* of where the current is deployed. See, e.g., *Id.*, ¶86.

POR (Paper 19), 22-23

POR (Paper 19), 22 (annotated)

Reply (Paper 25), 4

'074 Patent: gm of current buffer driver = gm of 384



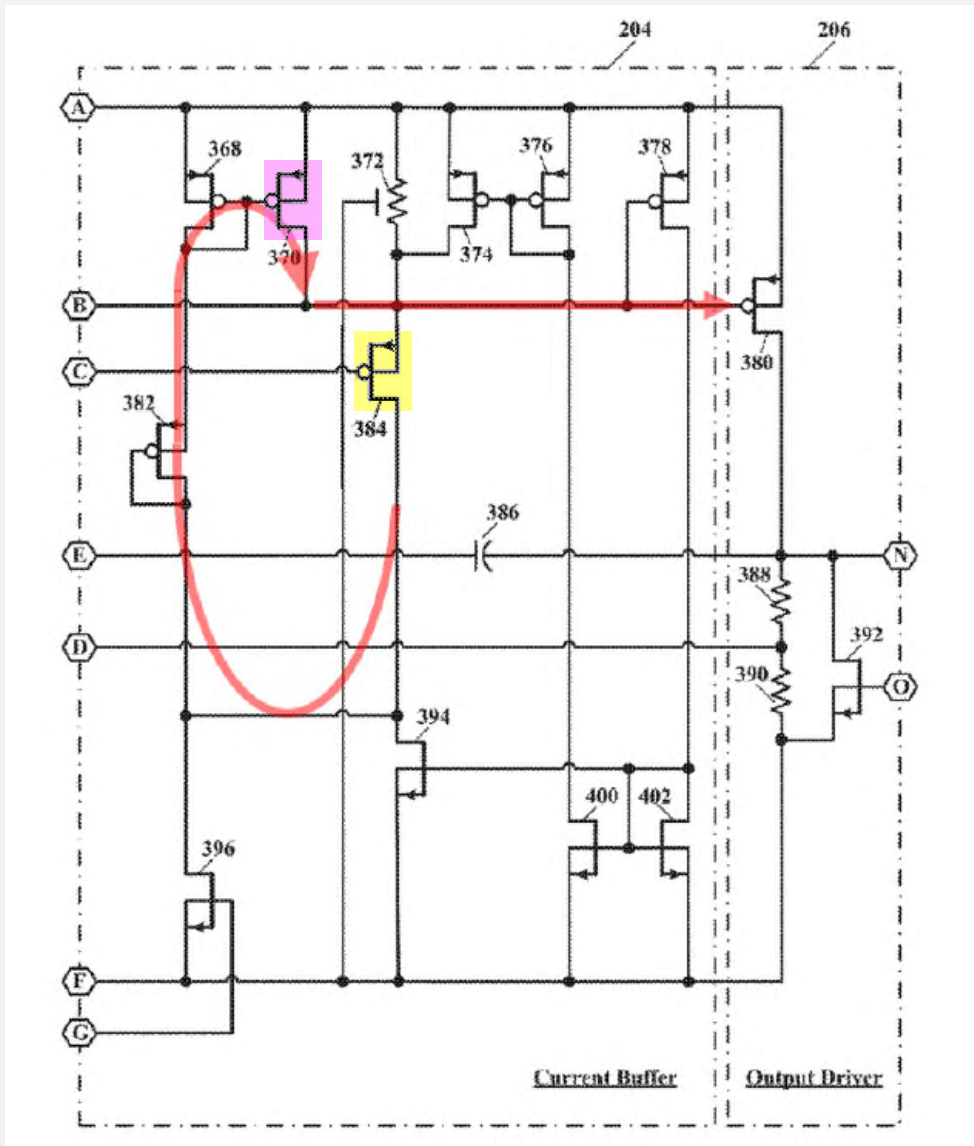
372 shown in FIG. 3B of the current buffer 204. The current driver may comprise transistors 370, 384 and 394, and resistor 372 shown in FIG. 3B of the current buffer 204, and the current feedback circuits 210 may comprise transistors 374, 376, 378, 400, 402, and 394 shown in FIG. 3B of the current buffer 204. The gm of the PMOS current buffer driver 204 may comprise transistor 384 and may be coupled to two sources of currents, one from the bias network and the other as current feedback 210 comprising transistors 378, 400, 402 and 376 from the power output stage 206 that may comprise transistor 380. The bias network may be fixed by

EX1001, 5:15-20

EX1001, Fig. 3B

Reply (Paper 25), 5

Patent Owner: gm of current buffer driver = gm of 384 + gm of 370



If the voltage on node C rises, the current through source follower 384 is reduced (because it is a PMOS transistor), causing the excess bias current to be redirected through current mirror 368/370 into node B (viz., the gate capacitance of the power output transistor 380). Taylor, ¶86. Where PMOS transistors 368 and 370 are the same size, the redirected current provides additional gm equal to that of source follower 384, doubling the overall gm of the circuit. *Id.* Sizing PMOS transistor 370 to be larger than transistor 368 will cause the gm to be further enhanced. *Id.* If the voltage on node C drops, transistor 384 sources more current

POR (Paper 19), 22-23

POR (Paper 19), 22
(purple/yellow highlights
added by Petitioner)

Reply (Paper 25), 5

The '074 Patent Does Not Describe “Allocation” of Current

Reply

Across 12 pages of discussion (*see id.*, 16-18, 21-23, 39-44), Patent Owner cites the patent just twice for its view of “gm enhanced” (*see id.*, 16). First, it cites a snippet that just parrots claim language without shedding any light on what “gm enhanced” means. (*Id.* (citing EX1001, 1:60-62).) Second, Patent Owner baldly states that “col. 5:8-49” discusses “a different and independent approach from gm-boost.” (*Id.*) It does not elaborate because it cannot: The cited passage explicitly defines the *gm-boost* circuit to include the very transistors—368, 370, and 382—that Patent Owner contends provide the alleged “gm enhancement.” (EX1001, 5:8-10.) Nor does the passage say anything about “steering current around transistor 384” or changing the “allocation of where the current is deployed,” which is how Patent Owner contends “gm enhancement” works. (*See* POR, 17, 23.)

Reply (Paper 25), 3

Sur-Reply

B. The Patent Supports PO’s Construction

Petitioner’s response to PO’s explanation is that “[PO] never explains where the patent describes this mechanism” (Reply, 2). This is odd given that the POR expressly states “[t]he separate gm-boost and gm-enhancement circuits are most easily seen in [’074] Figs. 3, 3A, and 3B,” and “[t]he gm-boost circuitry is highlighted in yellow, and the gm enhancement circuitry in pink.” POR, 17.

Petitioner’s criticism that PO relies on “a single patent figure” (Reply, 2) is both incorrect (PO also relies on claim language, expert testimony, and Rincon-Mora to inform its construction)⁴ and disingenuous. In advancing numerous

Sur-Reply (Paper 29), 5-6

Patent Owner Does Not Rely on Rincon-Mora for “Gm-Enhanced”

Gm-boost. As noted previously, the '074 patent uses similar “boost” terminology as Rincon-Mora to describe dynamically controlling the current through the source follower buffer so that g_m is proportional to the voltage regulator’s output current. Taylor, ¶¶70, 84-86. Rincon-Mora refers to this circuit technique as both a “transient response boost circuit” and a “transient boost circuit.” Rincon-Mora, Fig. 3, 1:10-17, 2:57-64. In like manner the '074 patent uses calls this approach “ g_m -boost,” stating: “The *gm-boost circuit 218* may provide a *gm-boost technique* that will increase the impedance value of the current buffer driver 204 with the help of the current feedback 210 which may sense the current change at the output of the output driver 206.” Ex., 1001, 4:15-20.

Patent Owner's Expert Identifies No Support in the '074 Patent's Written Description for Alleged “Gm Enhancement”

79. If the load current increases, it pulls the output N of the regulator down. The error amplifier responds to this change by dropping node C. This increases the V_{gs} of PMOS 384, increasing the current through it and pulling nodes B and Z closer together. Because B has a lot of capacitance due to the large size of driver 380, it moves more slowly. But when node Z rises, it shifts current from i_{mirror} to i_{sf} which results in i_{mirror} through PMOS 370 pulling up less strongly on node B, helping source follower 384 pull node B down. If the transistors in current mirror 368/370 are the same size as each other then this action doubles the g_m contribution made by the diverted current. If transistor 370 is larger than transistor 368, then the diverted current makes an even larger g_m contribution to current buffer driver 204. As a result, current buffer driver 204 has a g_m that is larger than the g_m of just source follower 384. If the load current decreases, the same reactions occur but in the opposite direction and again the g_m of current buffer driver 204 is larger than the g_m of just source follower 384.

EX2021 ¶ 79

Reply (Paper 25), 3

Patent Owner's Expert Analysis Depends on Increase in V_{gs}

79. If the load current increases, it pulls the output N of the regulator down. The error amplifier responds to this change by dropping node C. This increases the V_{gs} of PMOS 384, increasing the current through it and pulling nodes B and Z closer together. Because B has a lot of capacitance due to the large size of driver 380, it moves more slowly. But when node Z rises, it shifts current from i_{mirror} to i_{sf} which results in i_{mirror} through PMOS 370 pulling up less strongly on node B, helping source follower 384 pull node B down. If the transistors in current mirror 368/370 are the same size as each other then this action doubles the gm contribution made by the diverted current. If transistor 370 is larger than transistor 368, then the diverted

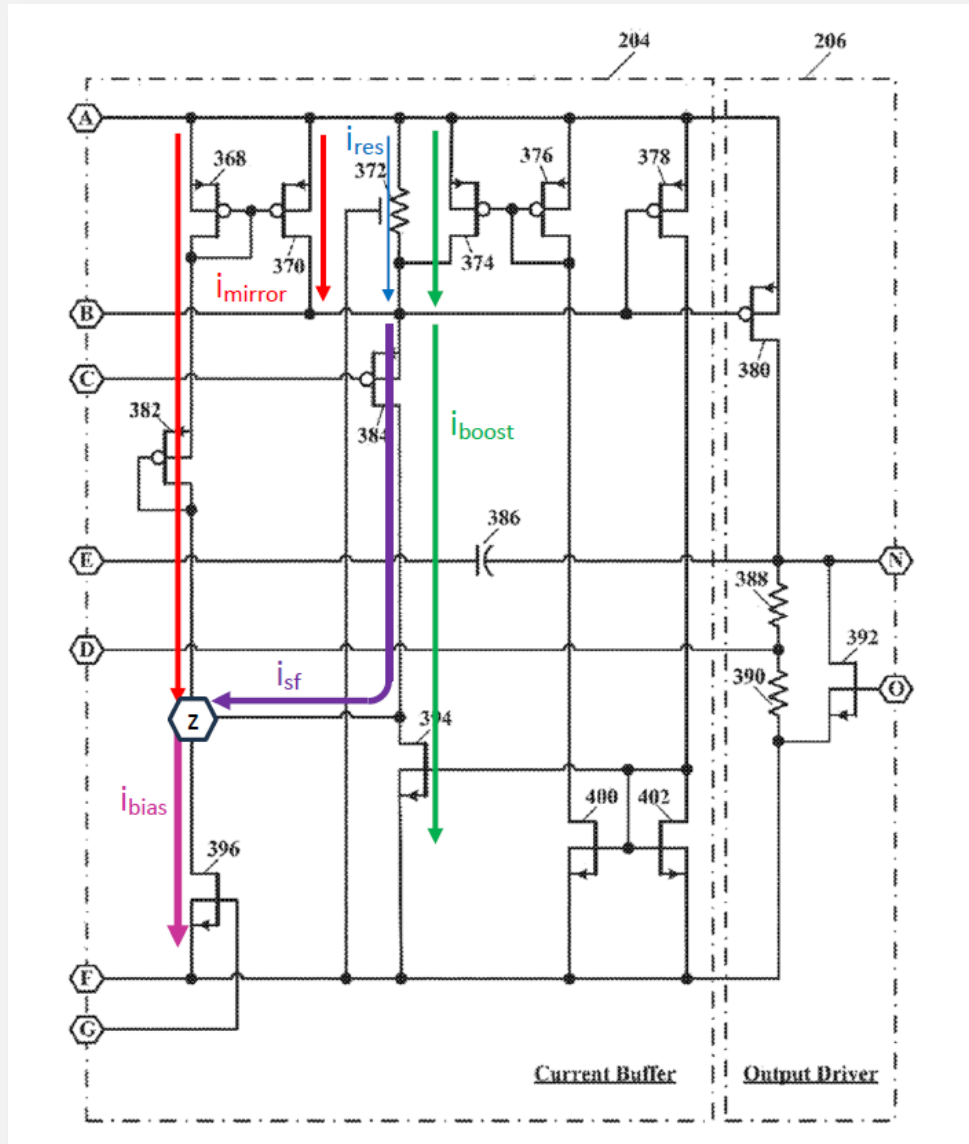
Petitioner's Expert Dr. Chen: Increase in V_{gs} Is Negligible

7. Because node B responds quickly and follows node C closely, increases in V_{gs} caused by a drop in the voltage of node C would be negligible. Thus, the “gm enhancement” effect described by Dr. Taylor would also be negligible, because it depends on V_{gs} increasing.

EX1028 ¶ 7

Reply (Paper 25), 7-8

Patent Owner's Expert Fails to Account for Current Feedback to 368/370



current buffer **204**. The gm of the PMOS current buffer driver **204** may comprise transistor **384** and may be coupled to two sources of currents, one from the bias network and the other as current feedback **210** comprising transistors **378**, **400**, **402** and **376** from the power output stage **206** that may comprise transistor **380**. The bias network may be fixed by transistor **396**. Then these currents are ratio'd in transistors **368** and **370** to provide a sufficient amount of current for the driver transistor **384** but not enough to increase more current based upon a limited current mirror by transistor **396**.

EX1001, 5:15-24

EX2021 ¶ 76

Reply (Paper 25), 8

Presumption Rebutted



“Appellant seeks to turn the general presumption that different phrases have different meanings into a bright line rule that saves the patent from unpatentability. We have rejected such an inflexible rule before, and we continue to do so here.”

Uniloc 2017 LLC. v. Netflix, Inc., No. 2021-2085, 2022 WL 17688150, at *6 (Fed. Cir. Dec. 15, 2022)



“Dr. Baran argues that the use of different terms implies that they have different meanings . . . but that implication is overcome where, as here, the evidence indicates that the patentee used the two terms interchangeably.”

Baran v. Med. Device Techs., Inc., 616 F.3d 1309, 1316 (Fed. Cir. 2010)

Reply (Paper 25), 6

Petitioner's Interpretation



Consistent with plain and ordinary meaning of claim language (providing a “gm-boost” makes the buffer driver “gm enhanced”).



Consistent with '074 specification, which does not describe any separate mechanism for increasing gm.



Consistent with relevant caselaw.

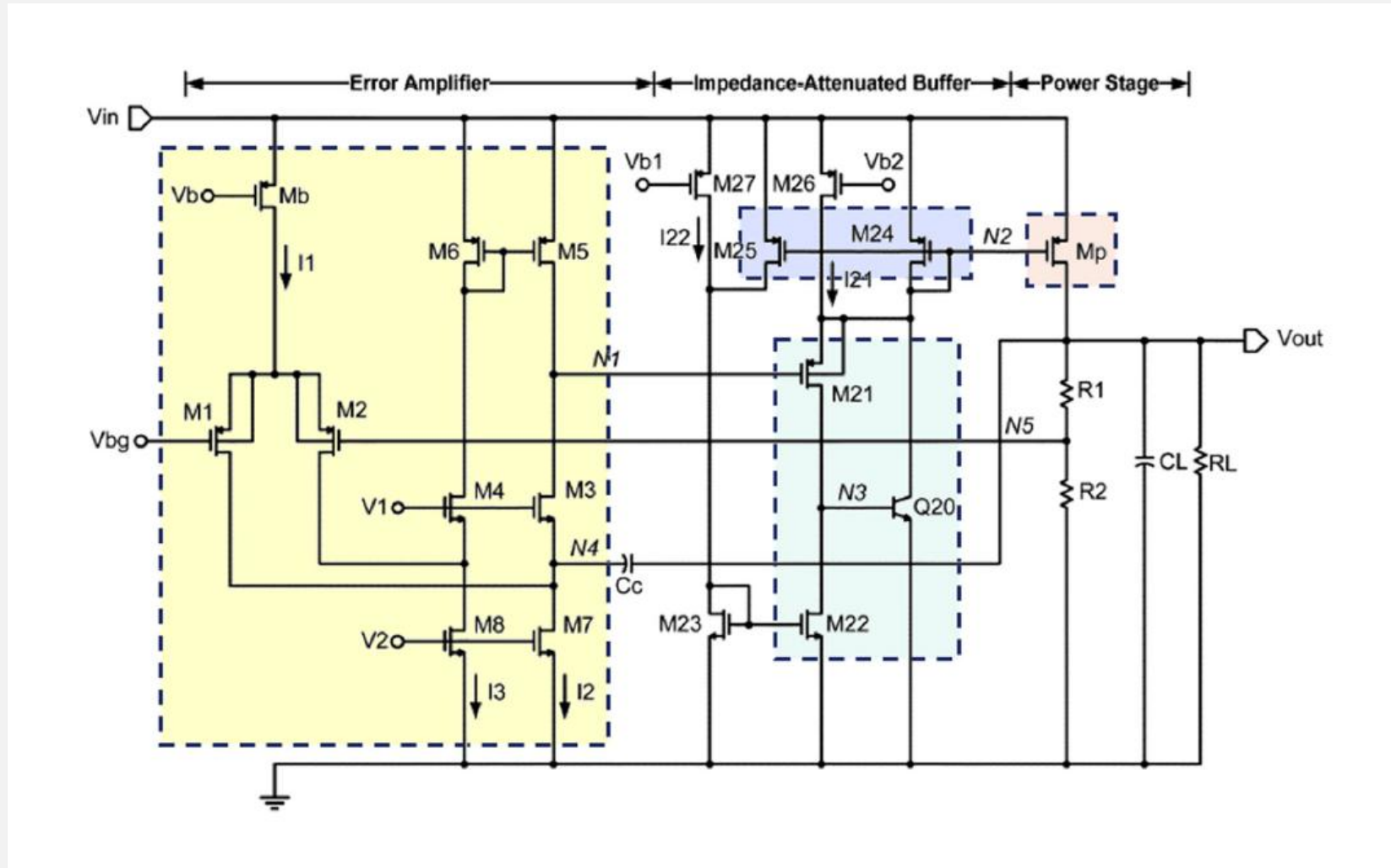
Reply (Paper 25), 4-6

Patent Owner's Interpretation

-  No description in '074 patent of a separate “gm-enhanced” mechanism.
-  Proposed construction is narrow and unsupported.
-  Overreliance on rebuttable presumption that different terms have different meanings.

Reply (Paper 25), 4-8

Al-Shyoukh Discloses Patent Owner's Alleged Mechanism



EX1004, Fig. 8 (annotated)

Reply (Paper 25), 9-11
EX1028 ¶¶ 12-15

Al-Shyoukh Discloses Patent Owner's Alleged Mechanism

During the transition from no load to full load, the decrease in the voltage at N_1 causes an increase in the transient current through M_{21} , which flows through the base of Q_{20} . The collector current of Q_{20} then increases to discharge the large gate capacitance of the pass device C_p and the voltage at N_2 decreases with a faster slewing.

EX1004, 1734

79. If the load current increases, it pulls the output N of the regulator down. The error amplifier responds to this change by dropping node C. This increases the V_{gs} of PMOS 384, increasing the current through it and pulling nodes B and Z closer together. Because B has a lot of capacitance due to the large size of driver 380, it moves more slowly. But when node Z rises, it shifts current from i_{mirror} to i_{sf} which results in i_{mirror} through PMOS 370 pulling up less strongly on node B, helping source follower 384 pull node B down. If the transistors in current mirror 368/370 are the same size as each other then this action doubles the gm contribution made by the diverted current. If transistor 370 is larger than transistor 368, then the diverted

EX2021 ¶ 79

Reply (Paper 25), 9-11
EX1028 ¶¶ 12-15

Patent Owner Proposes a Narrow Definition for “Enhanced”

Regardless, Petitioner’s new Al-Shyoukh theory (Reply, §II.E) fails on the merits. Petitioner glosses over the distinction—at the heart of PO’s construction—between raising overall current (*gm-boost*) to increase gm and re-allocating existing current (*gm-enhance[ment]*) to increase gm. Reply, 11. Instead, Petitioner reframes *gm-enhance[ment]* as merely “entail[ing] a second transistor helping to charge or discharge the source node of the driver.” Reply, 10-11. That is incomplete and insufficient.

Sur-Reply (Paper 29), 10

Petitioner's Alternative Argument Is Proper



“[W]here a patent owner in an IPR first proposes a claim construction in a patent owner response, a petitioner must be given the opportunity in its reply to argue and present evidence of anticipation or obviousness under the new construction, at least where it relies on the same embodiments for each invalidity ground as were relied on in the petition.”

Axonics, Inc. v. Medtronic, Inc., 75 F.4th 1374, 1384 (Fed. Cir. 2023)

Opp. to PO's Motion to Strike (Paper 31), 2

Petitioner's Alternative Argument Is Proper



“[T]he regulation that governs the content of a petition . . . does not direct a petitioner to raise, address, and apply alternative possible constructions, but instead requires a petitioner affirmatively to state how the challenged claim is to be construed.”

Axonics, Inc. v. Medtronic, Inc., 75 F.4th 1374, 1383 n.10 (Fed. Cir. 2023) (cleaned up)

[b] a gm enhanced current buffer driver;

Al-Shyoukh’s buffer driver discloses this limitation. Centered on the driver transistor M₂₁, Al-Shyoukh’s buffer is “gm enhanced” because it receives a gm boost from a current feedback circuit comprising M₂₄ and M₂₅, as detailed above. (Section IV.A.1, *supra*; EX1004, 1733-35, Figs. 3, 4, 8; *see also* EX1002 ¶ 53.)

Petition (Paper 1), 16

Opp. to PO’s Motion to Strike (Paper 31), 2-3

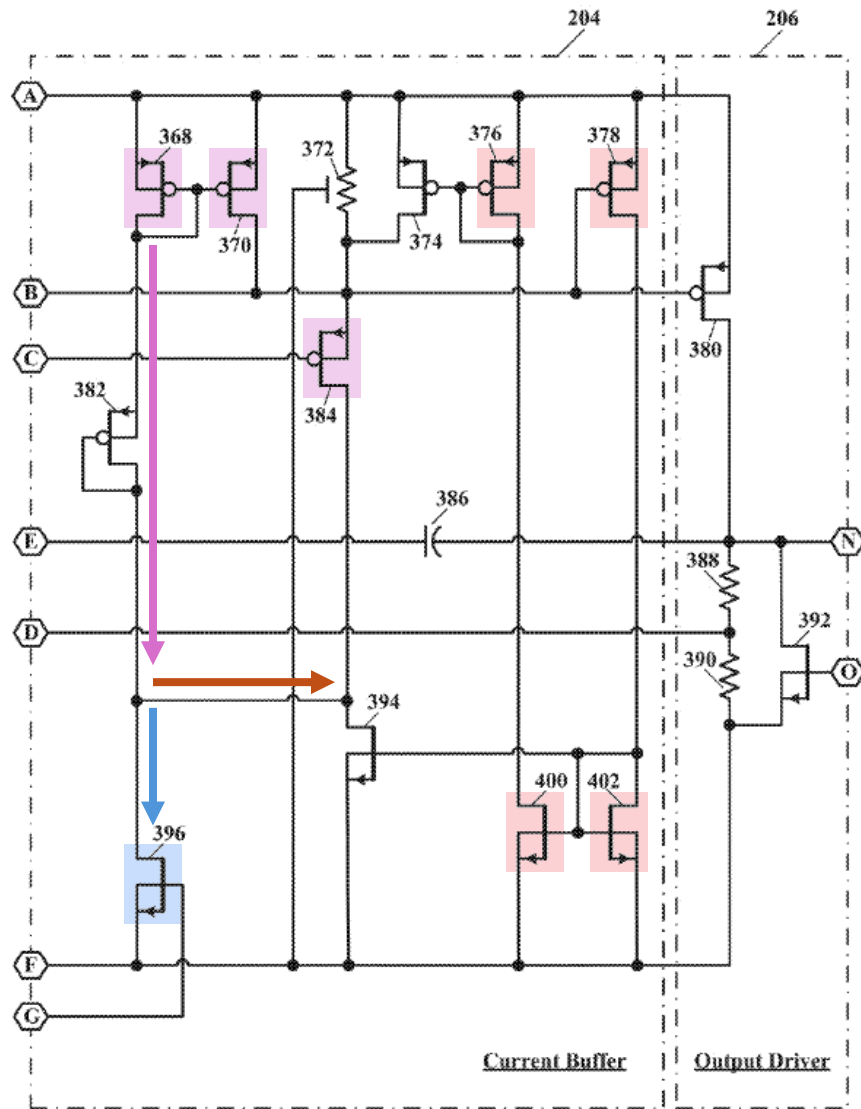
Claim 1[c] “biasing ratio”

“biasing circuit coupled to the current buffer driver to set a biasing ratio”

- 1[c] 1. A voltage regulator, comprising:
an operational amplifier;
a gm enhanced current buffer driver;
a biasing circuit coupled to the current buffer driver to set
a biasing ratio for gm-boost of the current buffer driver;
an enable/disable function to enable/disable the biasing
circuit for reducing standby current:
an output power driver, wherein the current buffer driver
is coupled between the operational amplifier and the
output power driver;
a current feedback circuit coupled between the output
power driver and the current buffer driver; and
a feedback loop coupled between the output power driver
and the operational amplifier.

EX1001, Claim 1

'074 Patent



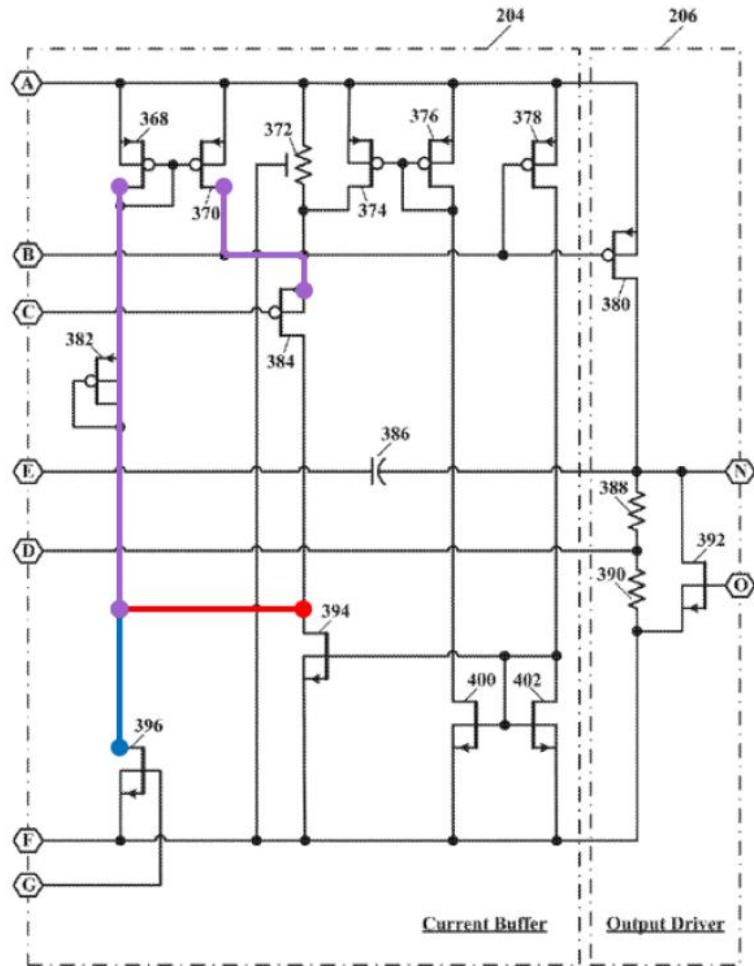
current buffer 204. The gm of the PMOS current buffer driver 204 may comprise transistor 384 and may be coupled to two sources of currents, one from the bias network and the other as current feedback 210 comprising transistors 378, 400, 402 and 376 from the power output stage 206 that may comprise transistor 380. The bias network may be fixed by transistor 396. Then these currents are ratio'd in transistors 368 and 370 to provide a sufficient amount of current for the driver transistor 384 but not enough to increase more current based upon a limited current mirror by transistor 396.

EX1001, 5:15-24

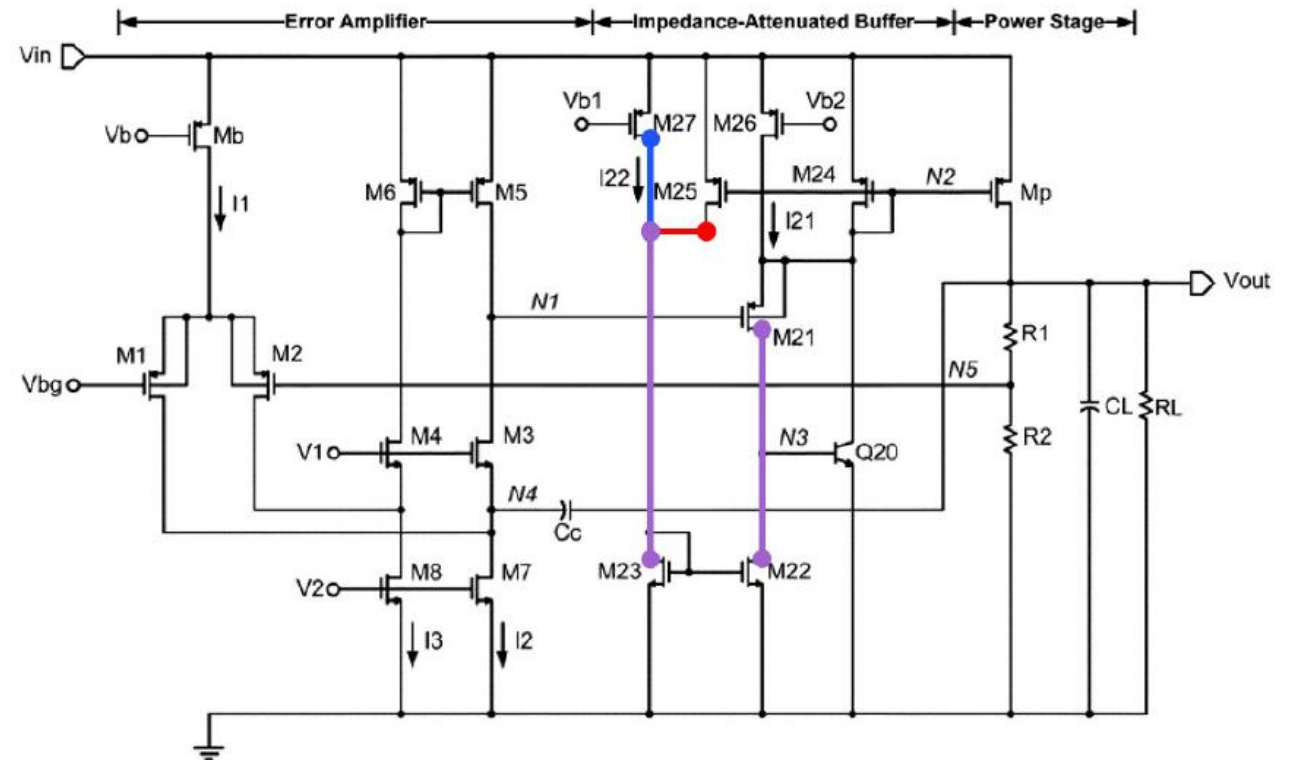
EX1001, Fig. 3B

Petition (Paper 1), 6-7, 17-19, 59-60
Reply (Paper 25), 4-5, 14-15

'074 Patent & Al-Shyoukh



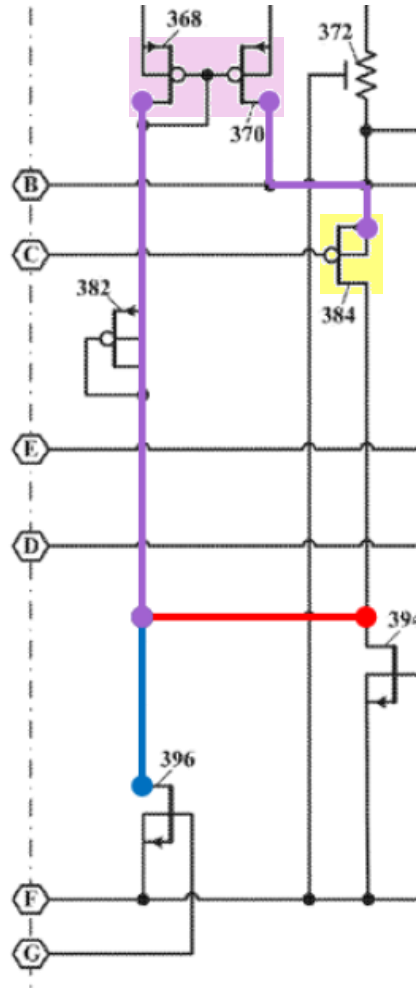
EX1001, Fig. 3B



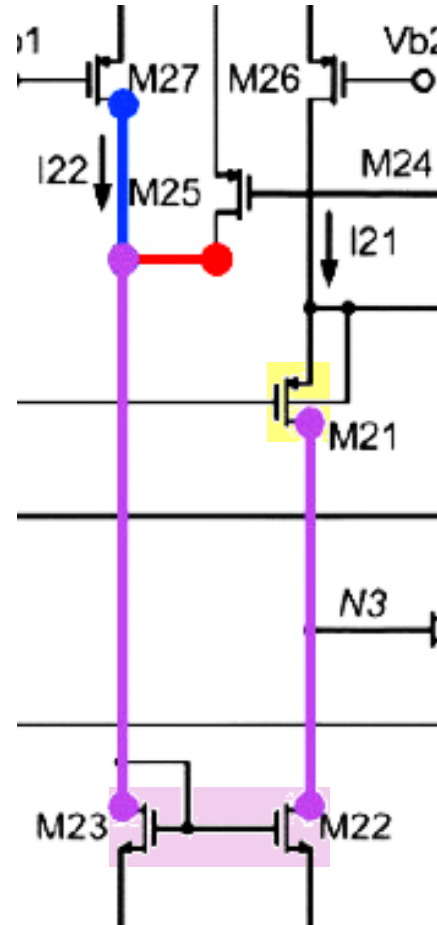
EX1004, Fig. 8

Petition (Paper 1), 17-19
EX1002 ¶¶ 56-58

'074 Patent & Al-Shyoukh



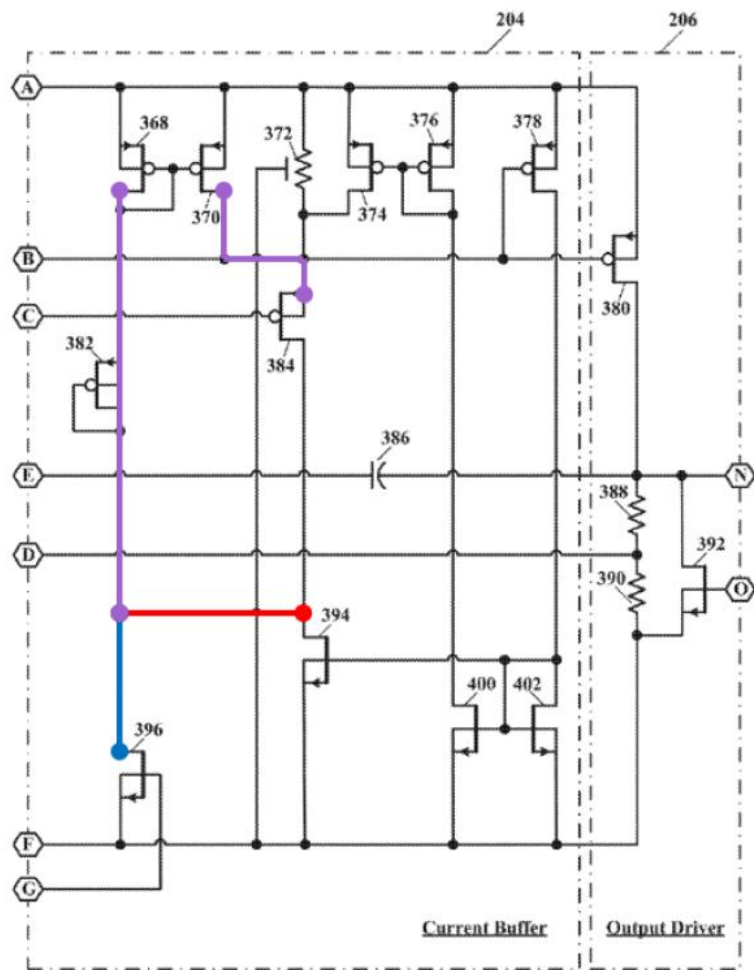
EX1001, Fig. 3B



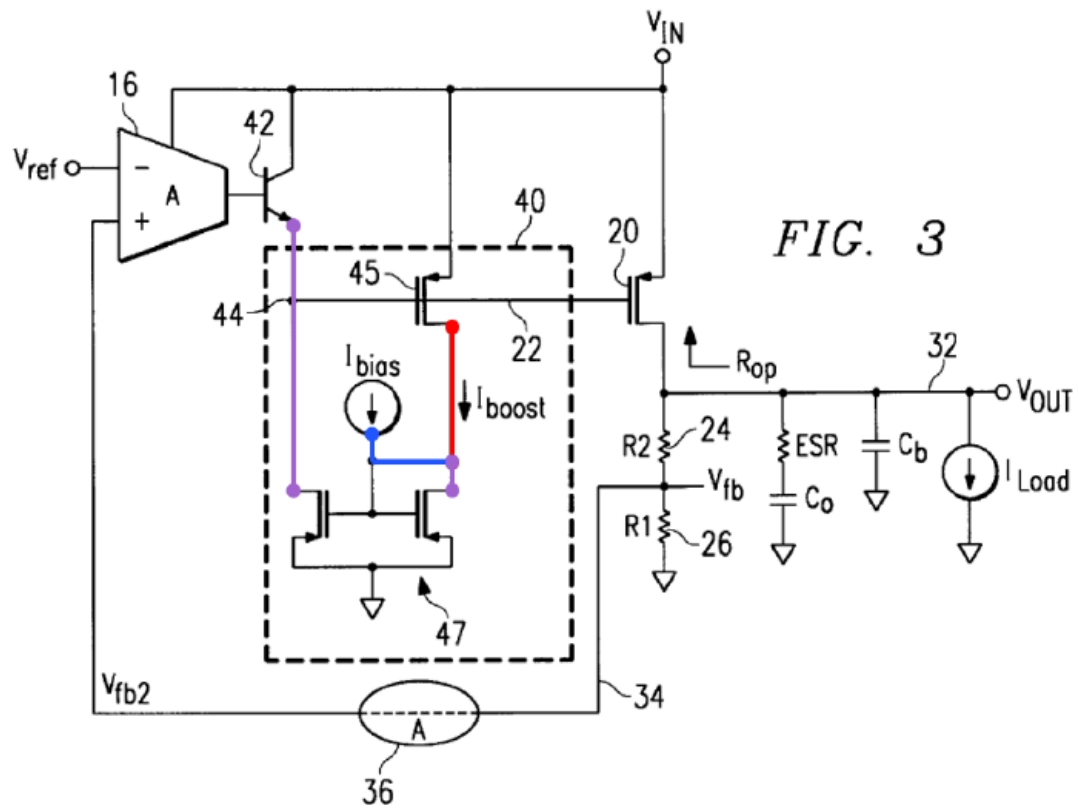
EX1004, Fig. 8

Petition (Paper 1), 17-19
EX1002 ¶¶ 56-58

'074 Patent & Rincon-Mora



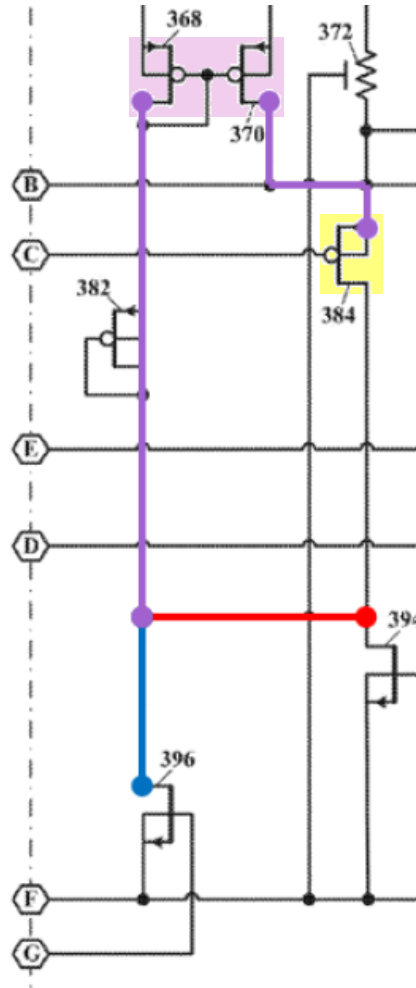
EX1001, Fig. 3B



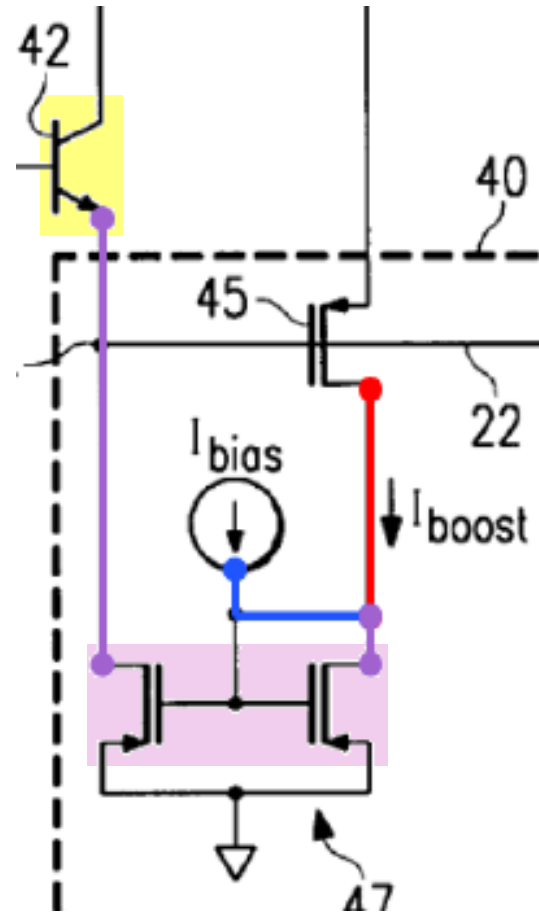
EX1013, Fig. 3

Petition (Paper 1), 59-61
EX1002 ¶¶ 145-148

'074 Patent & Rincon-Mora



EX1001, Fig. 3B



EX1013, Fig. 3

Petition (Paper 1), 59-61
EX1002 ¶¶ 145-148

Decision on Institution

Petitioner argues that “Al-Shyoukh’s LDO uses a biasing circuit coupled to the buffer driver to set a voltage V_{b1} at the gate of transistor M_{27} , providing a bias current I_{22} that is mirrored across transistors M_{23} and M_{22} to set a biasing ratio for gm-boost of the current buffer driver.” Pet. 17 (citing Ex. 1004, Fig. 8; Ex. 1002 ¶¶ 56–58). According to Petitioner, Al-Shyoukh’s biasing circuit operates the same way as the biasing circuit in the ’074 patent. Pet. 17–19 (citing Ex. 1001, 5:13–24, Fig. 3B; Ex. 1004, 1734, Fig. 8; Ex. 1002 ¶¶ 56–57).

Alternatively, “to the extent Patent Owner argues that ‘biasing ratio’ should be understood to mean a ratio of current that the current buffer draws from DC relative to the current feedback circuit,” Petitioner argues that Al-Shyoukh discloses this ratio. Pet. 20–21 & n.2 (citing Ex. 1004, Fig. 8; Ex. 1002 ¶ 59).

Patent Owner does not currently contest these arguments. *See* Prelim. Resp. At this stage, we find Petitioner’s arguments sufficiently persuasive.

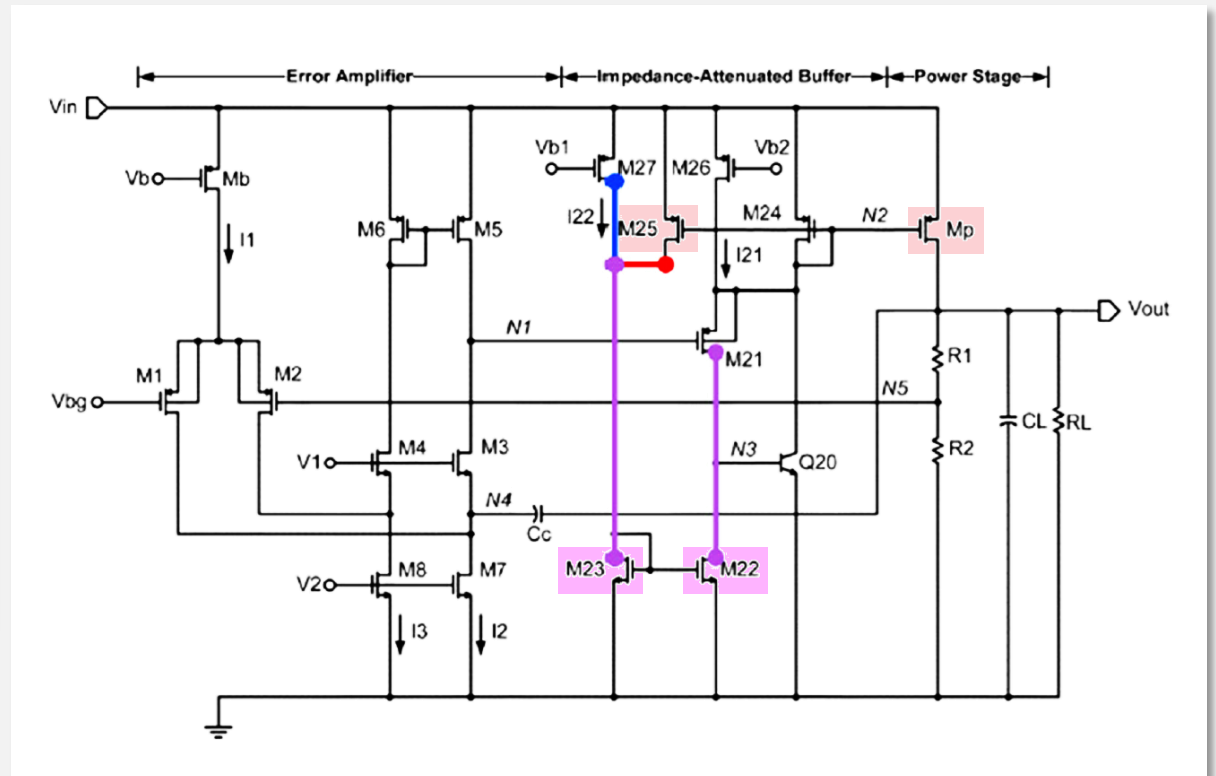
Patent Owner's Construction

the ratio sets *gm-boost*. In the context of the claimed voltage regulator and the '074 patent specification, a POSITA would understand that this ratio refers to **the ratio of current in the output transistor to the buffer driver**. Taylor, ¶¶80, 118. Petitioner's

Patent Owner's Expert's Construction Excludes Bias Current

his depiction. A POSITA would recognize that in this schematic the *gm-boost* is supplied by the current provided by M25, and the *biasing ratio for gm-boost* (the fraction of the output driver current that biases the source follower) is given by the size ratio: $\frac{M25 \times M22}{M_p \times M23}$. The design of the identified bias circuit and the size of M27 do

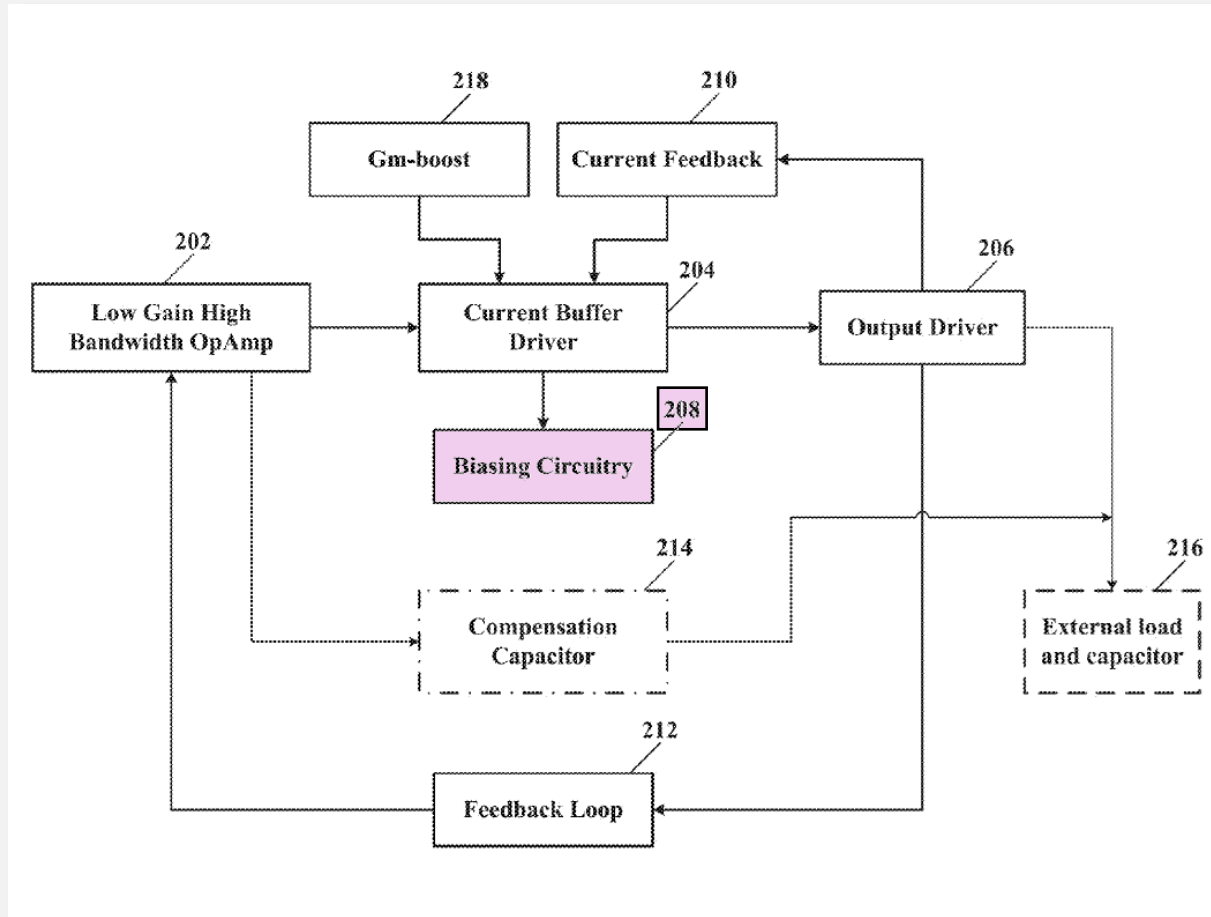
EX2021 ¶ 118



EX1004, Fig. 8

Reply (Paper 25), 12-13

'074 Patent: Biasing Circuit = Circuit 208



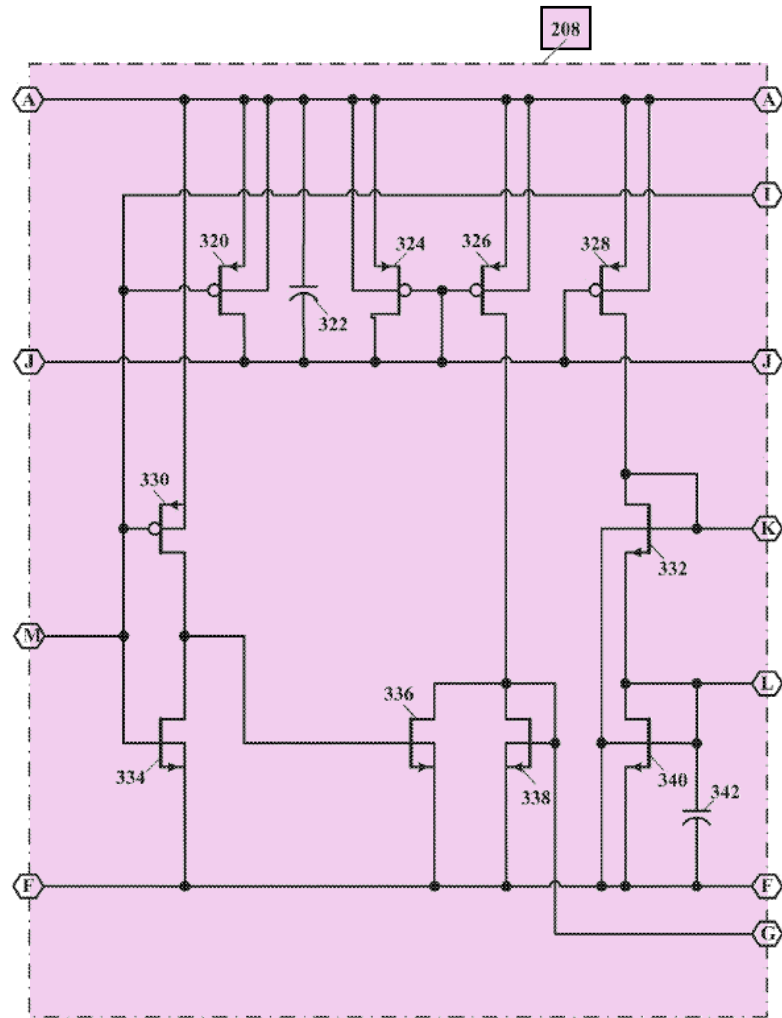
EX1001, Fig. 2

output driver 206. The voltage regulator of FIG. 2 may further comprise biasing circuits 208, current feedback 210, a feedback loop 212, a compensation capacitor 214 and a gm-boost circuit 218. This voltage regulator may supply

EX1001, 3:62-65

Reply (Paper 25), 13-14

'074 Patent: Biasing Circuit = Circuit 208



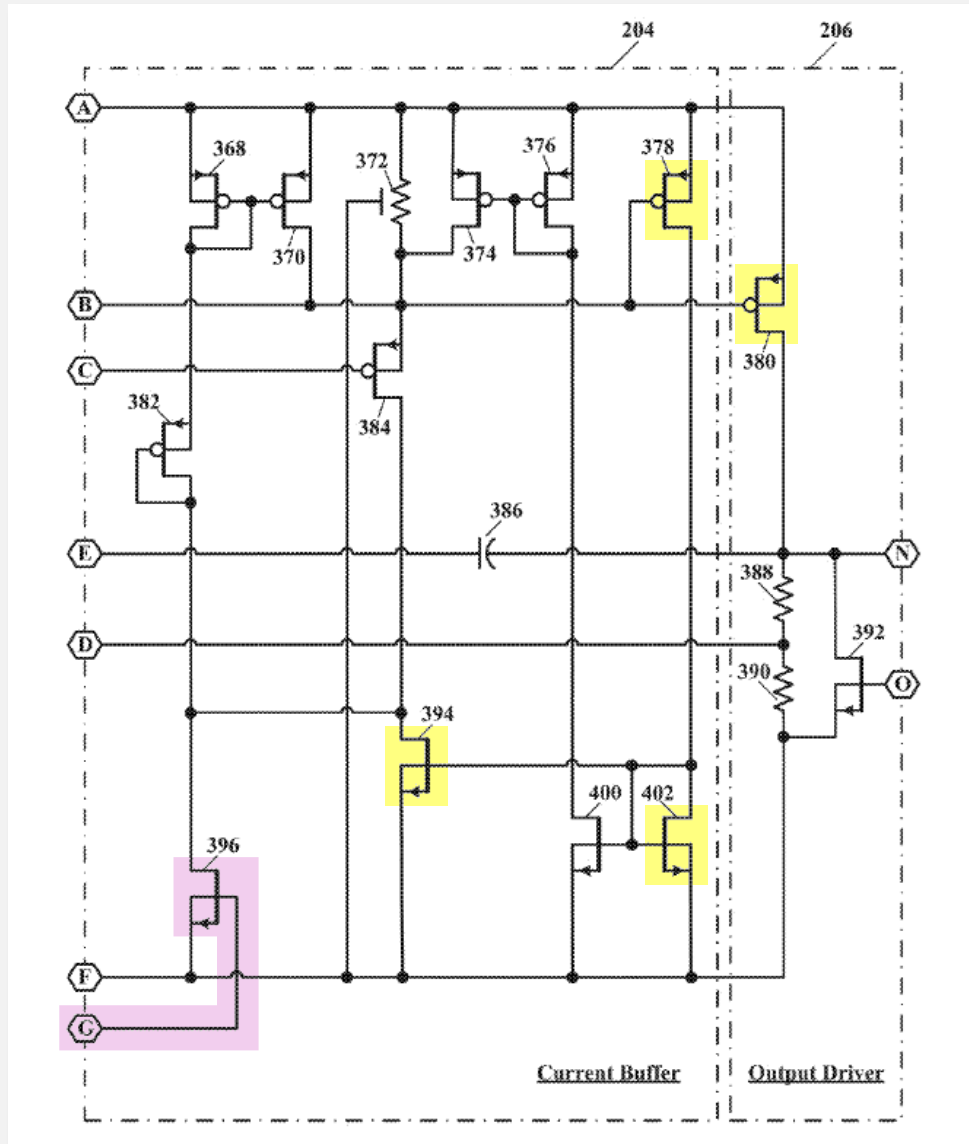
Shown in FIG. 3 is the bias circuit 208 for the USB regulator. Transistors 320, 330, 334 and 336 may be shut off during disabling/power down operation to make sure this circuit will consume substantially no DC current. Capacitors 322 and 342 are coupling capacitors to improve the VDD noise cancellation making sure the gates of transistors 324, 326 and 328 are moving the same way as VDD (node A) to cancel the power noise resulting with $V_{sg_noise}=0$. 342 acts similarly to help transistor 340 have better ground noise immunity resulting in $V_{gs_noise}=0$. Node M is the enable signal coming to the regulator circuit so that the module can be turned off when disabled.

EX1001, 4:43-54

EX1001, Fig. 3

Reply (Paper 25), 13-14

Patent Owner: Biasing Circuit = Transistors 378, 380, 394, 402

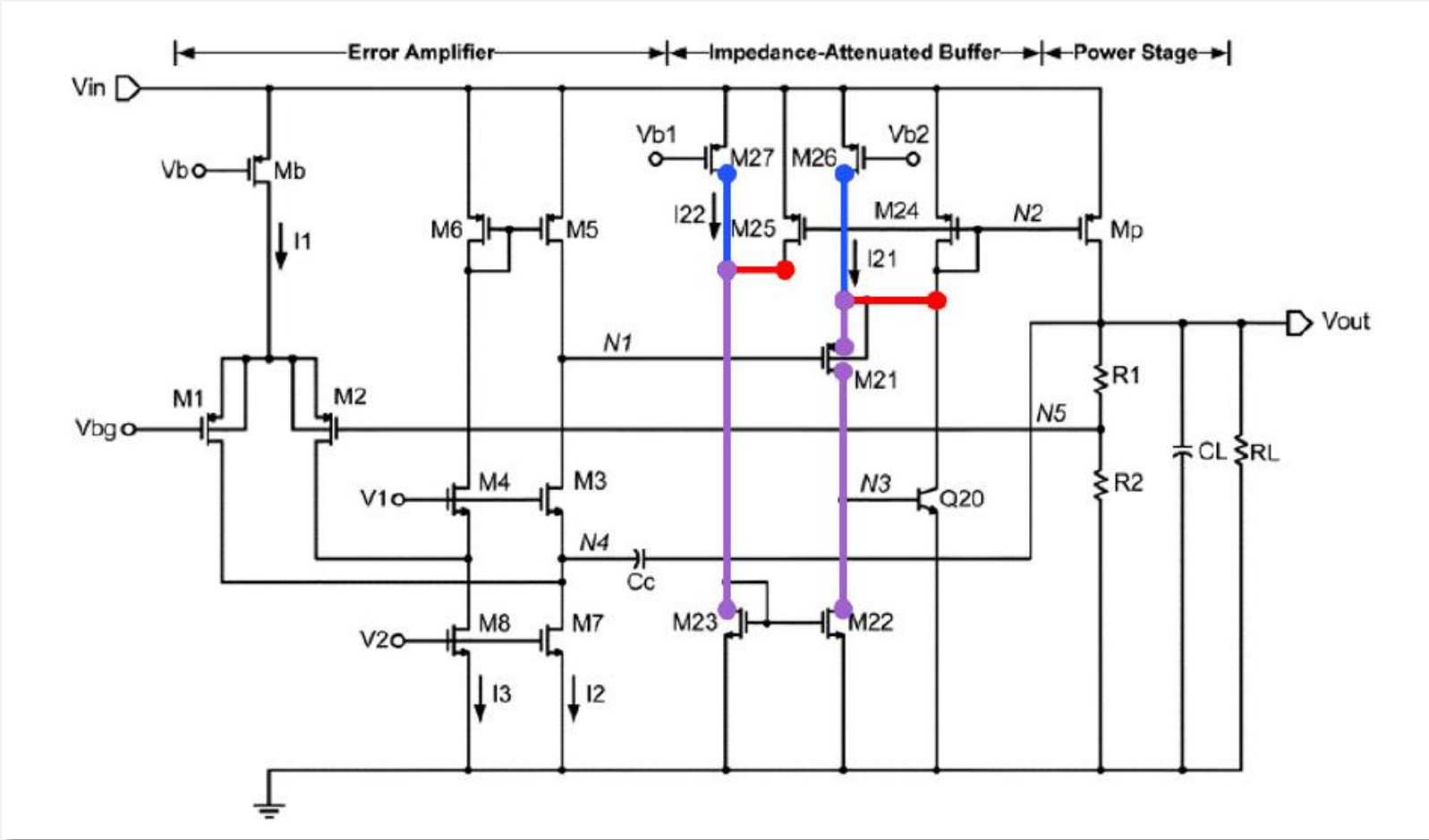


⁷ The '074 bias circuitry that *set[s] the biasing ratio for gm-boost* (the ratio of boost current through source follower 384 to the regulator output current) comprises transistors 378, 380, 394, and 402. Because current is proportional to transistor width, the ratio would be $\frac{378 \cdot 394}{380 \cdot 402}$, where transistor numbers represent each transistor's respective width.

Sur-Reply (Paper 29), 13-14

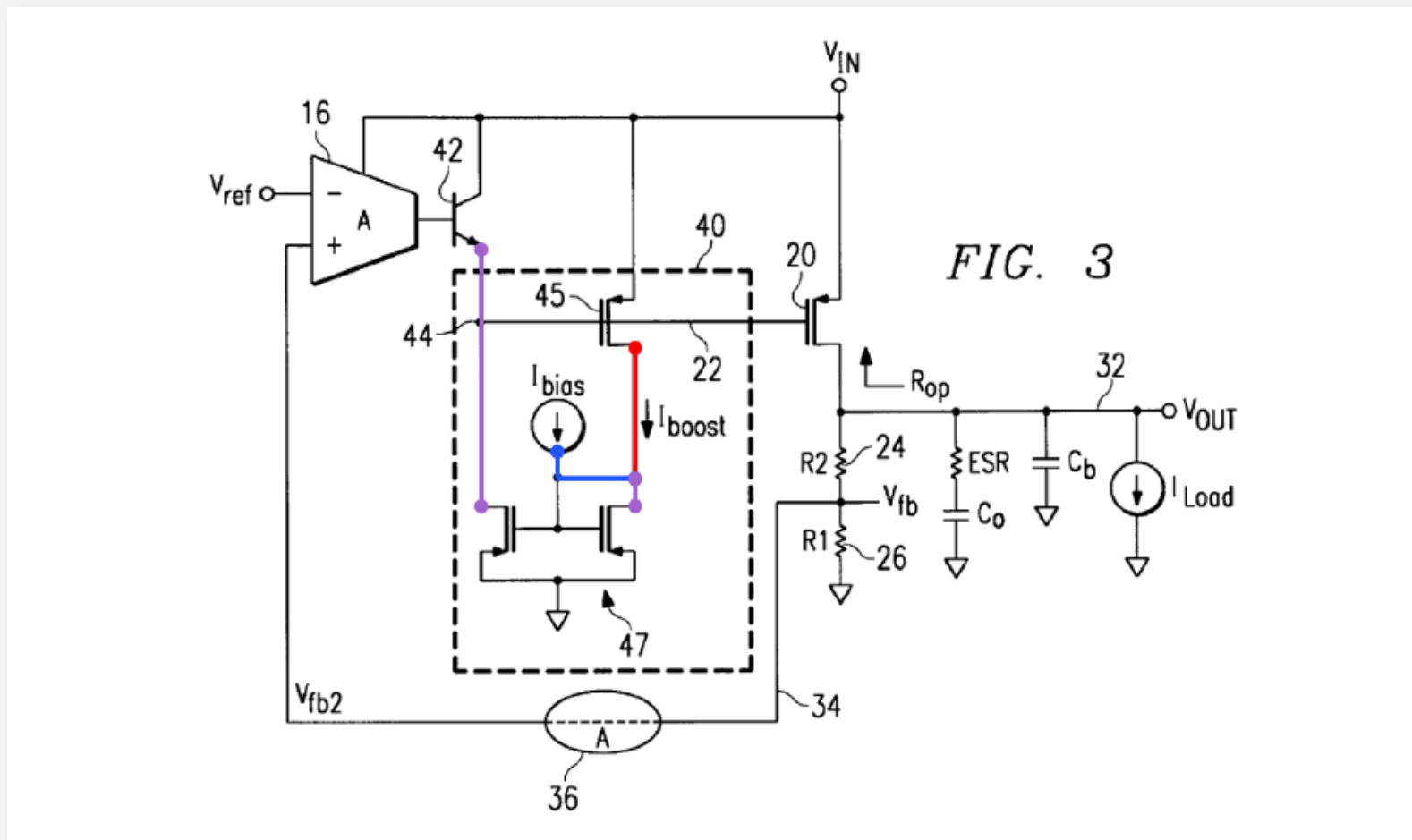
EX1001, Fig. 3B

Al-Shyoukh's Biasing Circuit Sets a Ratio of Current from DC Relative to Feedback



EX1004, Fig. 8

Rincon-Mora's Biasing Circuit Sets a Ratio of Current from DC Relative to Feedback



EX1013, Fig. 3

Petition (Paper 1), 61-62

Petitioner's Mapping Is Consistent with the '074 Patent

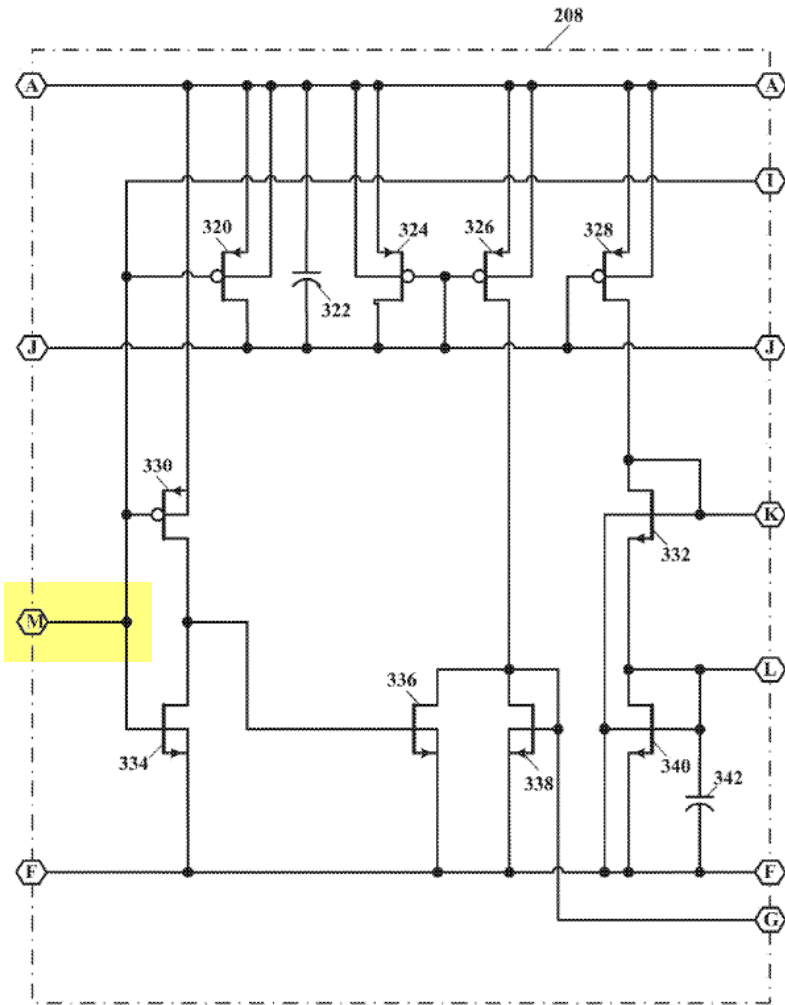
1. A voltage regulator, comprising:
 - an operational amplifier;
 - a gm enhanced current buffer driver;
 - 1[c] a biasing circuit coupled to the current buffer driver to set a biasing ratio for gm-boost of the current buffer driver;
 - 1[d] an enable/disable function to enable/disable the biasing circuit for reducing standby current:
 - an output power driver, wherein the current buffer driver is coupled between the operational amplifier and the output power driver;
 - a current feedback circuit coupled between the output power driver and the current buffer driver; and
 - a feedback loop coupled between the output power driver and the operational amplifier.

EX1001, Claim 1

Reply (Paper 25), 15-16

Claim 1[d] motivation to add “enable/disable”

'074 Patent



Shown in FIG. 3 is the bias circuit 208 for the USB regulator. Transistors 320, 330, 334 and 336 may be shut off during disabling/power down operation to make sure this circuit will consume substantially no DC current. Capacitors 322 and 342 are coupling capacitors to improve the VDD noise cancelation making sure the gates of transistors 324, 326 and 328 are moving the same way as VDD (node A) to cancel the power noise resulting with $V_{sg_noise}=0$. 342 acts similarly to help transistor 340 have better ground noise immunity resulting in $V_{gs_noise}=0$. Node M is the enable signal coming to the regulator circuit so that the module can be turned off when disabled.

EX1001, 4:43-54

EX1001, Fig. 3

EX1002 ¶¶ 69, 160

Enable/Disable Was Well-Known and Conventional

Dr. Chen

EX1002 ¶¶ 70, 161

161. I note further that the concept of an enable/disable for biasing circuitry was known widely beyond Ivanov. Power efficiency was a basic concern in analog circuit design, and it was well known that a way to save energy was to disable parts of a circuit that were not in use, biasing circuitry being a frequent candidate. Thus,

Patent Owner's Expert

EX2007, 50

57. In particular, a POSITA would have understood the term refers to an input for turning one or more transistors on or off like a switch to enable or disable the flow of current. A POSITA would have recognized that there are only a limited number of ways for enabling/disabling the flow of current in a circuit and that by far the most common way is to turn on or off the transistor itself through which current is flowing. This is a fundamental technique that is used in all types of applications, such as disabling current in a smartphone circuit or disabling the coils in a room heater when a given temperature is reached.

58. Moreover, because engineers routinely use an input to a circuit to enable or disable it, they often use the term “enable” as the name of that structural input. For example, a review of

Reply (Paper 25), 17

Known Technique



“And if there’s a known technique to address a known problem using prior art elements according to their established functions, then there is a motivation to combine. And we specify *address* a known problem because it’s not necessary to show that a combination is the *best* option, only that it be a *suitable* option.”

Intel Corp. v. PACT XPP Schweiz AG, 61 F.4th 1373, 1380 (Fed. Cir. 2023) (cleaned up)

Reply (Paper 25), 17-18

Patent Owner Misparses Rincon-Mora

Rincon-Mora

EX1013, 1:12-17, 2:4-7

(“LDO”) voltage regulators. More particularly, the present invention relates to a current efficient LDO voltage regulator incorporating a transient response boost circuit which may be added to selectively apply current to a slew-rate limited node and yet requires no standby current during zero output current load conditions of the LDO voltage regulator.

In a preferred embodiment disclosed herein, a transient boost circuit is added to the slew-rate limited node and requires no standby current during zero output current load conditions. Alternative embodiments of the transient boost

Patent Owner

POR (Paper 19), 27, 59-60

(“LDO”) voltage regulators. More particularly, the present invention relates to a current efficient LDO voltage regulator

[. . .]

requires no standby current during zero output current load conditions of the LDO voltage regulator.

Reply (Paper 25), 19-20

Rincon-Mora Does Not Equate Its Quiescent Current to Zero

With respect additionally now to FIG. 4, at $I_{Load}=0$ Amps, P1 is low thereby making the unity gain frequency low. The parasitic pole P3 must only be greater than $UGF[I_{Load}=0 \text{ A}]$ which condition can be effectuated with approximately $1 \mu\text{A}$. At this point, I_{boost} is zero because the aspect ratio of the PMOS transistor 45 forming a portion of the transient boost circuit 40 is much less than that of the output PMOS transistor 20, thus yielding low quiescent current.

EX1013, 4:41-48

$0 \mu\text{A} \neq 23 \mu\text{A}$

through the output transistor Mpo. During low load-current conditions, the current fed back (I_{boost}) is negligible, thereby yielding high overall current efficiency and not aggravating battery life. Consequently, the current through the emitter follower is simply I_{bias} when load-current is low. During

EX1014, 37

Reply (Paper 25), 20

Rincon-Mora Does Not Criticize, Discredit, or Discourage Enable/Disable

the like. As a consequence, standby and quiescent current flow are major concerns in their design and some LDO voltage regulators incorporate a separate enable terminal to switch the device into a standby mode of operation to minimize power consumption when the associated device is disabled.

EX1013, 1:25-30



“A reference that merely expresses a general preference for an alternative invention but does not criticize, discredit, or otherwise discourage investigation into the claimed invention does not teach away.”

Meiresonne v. Google, Inc., 849 F.3d 1379, 1382 (Fed. Cir. 2017) (cleaned up)

Reply (Paper 25), 18, 20-21

Sufficiency Does Not Demotivate Modification



“Reviewing Runte, we conclude that substantial evidence supports the Board’s fact finding that Runte does not teach away from substituting its CRT with an LCD. While Runte does disclose that its table top gaming device already provides comfortable seating for its players, it does not discourage the provision of additional legroom that an LCD or plasma display may provide.”

Cole Kepro Int’l, LLC v. VSR Indus., Inc., 695 F. App’x 566, 570 (Fed. Cir. 2017) (cleaned up)

Reply (Paper 25), 21

Petitioner Relies on Prior Art Circuit Topologies, Not Specific Test Chips

Al-Shyoukh

In order to verify the proposed buffer impedance attenuation technique, the LDO shown in Fig. 8 was fabricated in a $0.35\text{-}\mu\text{m}$ twin-well 7-V CMOS process. Fig. 9 shows the die micrograph of the proposed LDO, which was fabricated as part of an integrated power IC. The effective die area of the LDO is 0.264 mm^2 . It should be noted that the output voltage of the LDO is bonded with only a single bonding wire from the pad to the pin in order to minimize the cost.

EX1004, 1738

Rincon-Mora

Fig. 9 illustrates the final integrated circuit design of the low-voltage, LDO regulator. The circuit was fabricated in MOSIS CMOS $2\text{-}\mu\text{m}$ technology with an added p-base layer. The Schottky diode was not included in the layout but instead implemented discretely. The aspect ratio of the power device M_{po} is $30\text{ k}\mu\text{m}/\mu\text{m}$. The LDO produced a maximum output current of 18 and 50 mA at input voltages of 1 and 1.2 V. The circuit achieved approximately a 65% output current improvement over its noncurrent boosted counterpart, as shown in Fig. 10. The quiescent current flow was $23\text{ }\mu\text{A}$ at zero load-current and $230\text{ }\mu\text{A}$ at 50 mA of load-current, illustrated in Fig. 11. The maximum quiescent current at full

EX1014, 43

Reply (Paper 25), 21-22

Full-Load Performance Is Not Relevant to Enable/Disable

TABLE II
PERFORMANCE COMPARISON WITH PREVIOUSLY REPORTED LDOs

	1998 [1]	2000 [3]	2003 [4]	2004 [5]	2005 [17]	This Work
Technology (μm)	2.0	1.0	0.6	0.5	0.09	0.35
V_{do} (V)	0.3	N.A.	0.2	N.A.	0.3	0.2
$I_{L,\text{max}}$ (mA)	50	200	100	160	100	200
I_q (mA)	0.023	0.03	0.038	0.025	6	0.02
Current Efficiency at $I_{L,\text{max}}$ (%)	99.5	N.A.	N.A.	N.A.	94.3	99.8
ΔV_{out} (mV)	19	220	130	200	90	54
T_r (μs)	1.8	1.1	2	2.75	0.00054	0.27
C_L (μF)	4.7	1	10	2.2	0.00060	1
ESR Zero Required	No	Yes	Yes	No	No	No
FOM (ns)	8.2	0.165	4.9	0.43	0.032	0.027

EX1004, 1741

Reply (Paper 25), 22

Patent Owner's Expert Compares Different "Quiescent Current" Metrics

	1998 EX1013	2009 EX1004	2009 EX1011	2013 EX2011	2012 EX2012	2012 EX2016	2012 EX2019	2003 EX2020
Technology (μm)	2	0.35	N.A.	N.A.	N.A.	N.A.	N.A.	N.A.
V_{do} (V)	0.3	0.2	0.205	<1	2	1.2	0.39	<0.5
$I_{\text{L,max}}$ (mA)	50	200	3000	1000	500	1500	300	3000
I_{q} (mA)	0.023	0.02	7.5	5	6	10	0.16	10
I_{SHUTDOWN} (mA)	N.A.	N.A.	<0.01	N.A.	N.A.	N.A.	0.06	0.02
Current Efficiency at $I_{\text{L,max}}$ (%)	99.5	99.8	95.2	95.2	98.8	98.8	99.9	99.7
ΔV_{out} (mV)	19	54	60	40	500	130	100	N.A.
T_{r} (μs)	1.8	0.27	0.02	0.04	0.1	1.63	0.33	N.A.
C_{L} (μF)	4.7	1	1	1	0.1	10	1	47
ESR Zero Required	No	No	No	Yes	No	Yes	Yes	No
FOM (ns)	8.2	0.027	0.05	0.2	1.2	20.3	0.18	N.A.

EX2021 ¶ 136

Q. And can you tell from this what quiescent current means?

A. Can I tell what it means? No. I can tell what they think it is.

Q. I'm not sure I understand the nuance there that you're articulating.

A. What it means, I interpret it to mean, what does the two-word -- what do the two words "quiescent current" mean. That is not specified here. What I can see here is what are they promising the quiescent current to be.

Q. I see. So -- so you do understand that they're reporting the quiescent current to be 6 milliamps?

A. I do understand that to be a maximum of 6 --

Q. A maximum.

A. -- milliamps.

Q. But you're not sure exactly they mean by quiescent current when they're saying it's 6 --

A. Some people do have different definitions. As we saw on the earlier three-pin regulator, their definition of quiescent current was simply everything that's left over. In other places, quiescent current means there is no output, it is quiescent.

EX1029, 79:9-80:9

Reply (Paper 25), 22

Patent Owner's Expert Compares Different "Quiescent Current" Metrics

	1998 EX1013	2009 EX1004	2009 EX1011	2013 EX2011	2012 EX2012	2012 EX2016	2012 EX2019	2003 EX2020
Technology (μm)	2	0.35	N.A.	N.A.	N.A.	N.A.	N.A.	N.A.
V_{do} (V)	0.3	0.2	0.205	<1	2	1.2	0.39	<0.5
$I_{\text{L,max}}$ (mA)	50	200	3000	1000	500	1500	300	3000
I_{q} (mA)	0.023	0.02	7.5	5	6	10	0.16	10
I_{SHUTDOWN} (mA)	N.A.	N.A.	<0.01	N.A.	N.A.	N.A.	0.06	0.02
Current Efficiency at $I_{\text{L,max}}$ (%)	99.5	99.8	95.2	95.2	98.8	98.8	99.9	99.7
ΔV_{out} (mV)	19	54	60	40	500	130	100	N.A.
T_{r} (μs)	1.8	0.27	0.02	0.04	0.1	1.63	0.33	N.A.
C_{L} (μF)	4.7	1	1	1	0.1	10	1	47
ESR Zero Required	No	No	No	Yes	No	Yes	Yes	No
FOM (ns)	8.2	0.027	0.05	0.2	1.2	20.3	0.18	N.A.

EX2021 ¶ 136

Q. What does supply current mean?

A. So I would interpret supply current to mean the current that this particular -- that the regulator consumes from the supply, not to be confused with the current that the regulator supplies to its own load.

Q. And how is that different from quiescent current?

A. The word "quiescent" means quiet. So in some usages of quiescent current, quiescent would mean what is the power drawn by the regulator when there's no load. In the usage we saw in the 2990, quiescent current had nothing to do with it being quiescent, but was simply the power -- the current dissipated in the regulator. And so this use of supply current is consistent with the 2990 quiescent current. It's not consistent with the usage of quiescent current in Rincon-Mora and Al-Shyoukh.

EX1029, 86:18-87:9

Reply (Paper 25), 22

Ivanov Presents No Start-up Time Issues

The disable/enable bias control circuit 1 of FIG. 1 described above, when in its shutdown condition, can rapidly disable the bias core circuitry 2 and the shutdown the bias circuitry of amplifier 18 in approximately 50 ns, and can then rapidly produce the desired value of V_{BIAS+} on conductor 5 and turn on the bias circuitry M22 to bias up CMOS amplifier 18 in only about 100 to 150 nanoseconds in response to a fast transition of $V_{SHUTDOWN}$ from a low logic level to a high logic level. This is approximately 100 times faster than has been achieved using prior techniques. Thus,

EX1005, 6:28-37; EX2021 ¶ 101

Reply (Paper 25), 23-24

USB Timing Requirements Do Not Demotivate

Table 6-21. LFPS Transmitter Timing¹

	tBurst				tRepeat		
	Min	Typ	Max	Minimum Number of LFPS Cycles ²	Min	Typ	Max
Polling.LFPS	0.6 μ s	1.0 μ s	1.4 μ s		6 μ s	10 μ s	14 μ s
Ping.LFPS	40 ns		200 ns	2	160 ms	200 ms	240 ms
tReset ³	80 ms	100 ms	120 ms				
U1 Exit ^{4,5}	300 ns		900 ns/2 ms ⁶				
U2 / Loopback Exit ^{4,5}	80 μ s ⁷		2 ms				
U3 Wakeup ^{4,5}	80 μ s ⁷		10 ms				

EX2022, 162

Reply (Paper 25), 23-24

The Prior Art Does Not Prioritize Speed

of the LDO are needed. First, low dropout voltage across the pass device of the LDO is required provide high power efficiency. In addition, the increased level of integration in portable devices not only demands the LDO to deliver high load current, but also requires the no-load quiescent current of the LDO to be minimized for improving the current efficiency [1]. Good load transient response with small output-voltage variation including overshoots and undershoots upon load switching is critical to prevent an accidental turn off or resetting of the portable device. These four major performance requirements of the LDO, including low dropout voltage, high output current, low no-load quiescent current, and small output transient undershoots and overshoots are, however, difficult to achieve simultaneously.

EX1004, 1732; EX2021 ¶¶ 57-61

Reply (Paper 25), 23-24

Ivanov's Enable/Disable Would Reduce Quiescent Current

Transistor M17 is designed to have a very long channel length, so as to produce a drain and source current of only approximately 0.1 to 5 microamperes. Transistors M16 and M12 in combination perform the function of preventing a possible unstable condition in quasi PTAT circuit 2 by causing part of the “charging reference current” in transistor M26 to be supplied from transistor M16 and causing the sum of the currents in transistors M16 and M17 (approximately 0.1 to 5 microamperes) to flow through transistor M12 and resistor R26, and therefore through transistor M26 and diode-connected PNP transistor Q0.

Transistor M26 and diode-connected transistor Q0 function as a threshold or reference circuit which determines the voltage to which compensation capacitor C0 is to be charged by the subsequently described all charging current $I_{TRICKLE}$. Resistor R26 has a very high resistance which is added to the very high combined resistance of transistors M12, M16 and M17, so as to provide the several megohm resistance needed to produce the very low 1–2 microampere trickle charging current from V_{DD} , which typically is 5 volts.

$$0.1 \mu A + 1 \mu A = 1.1 \mu A < 20 \text{ or } 23 \mu A$$

$$2 \mu A + 5 \mu A = 7 \mu A < 20 \text{ or } 23 \mu A$$

EX1005, 5:39-58

Reply (Paper 25), 24

MIC3385 Datasheet

Electrical Characteristics⁽⁴⁾

$V_{IN} = V_{EN} = V_{LOWQ} = 3.6V$; $L = 0.47\mu H$; $C_{OUT} = 10\mu F$; $T_A = 25^\circ C$, unless noted. **Bold values indicate $-40^\circ C \leq T_J \leq +125^\circ C$.**

Parameter	Condition	Min.	Typ.	Max.	Units
Supply Voltage Range		2.7		5.5	V
Under-Voltage Lockout Threshold	(turn-on)	2.45	2.55	2.65	V
UVLO Hysteresis			100		mV
Quiescent Current, PWM mode	$V_{FB} = 0.9 \cdot V_{NOM}$ (not switching)		690	900	μA
Quiescent Current, LDO mode	$V_{LOWQ} = 0V$; $I_{OUT} = 0mA$		16	29	μA
Shutdown Current	$V_{EN} = 0V$		0.01	5	μA
[Adjustable] Feedback Voltage	$\pm 1\%$	0.99	1	1.01	V
	$\pm 2\%$ (over temperature)	0.98		1.02	V
FB pin input current			1		nA
Current Limit in PWM Mode	$V_{FB} = 0.9 \cdot V_{NOM}$	0.75	1	1.85	A
Output Voltage Line Regulation	$V_{OUT} > 2V$; $V_{IN} = V_{OUT} + 300mV$ to $5.5V$; $I_{LOAD} = 100mA$		0.13		%
	$V_{OUT} < 2V$; $V_{IN} = 2.7V$ to $5.5V$; $I_{LOAD} = 100mA$				%
Output Voltage Load Regulation, PWM Mode	$20mA < I_{LOAD} < 300mA$		0.2		%
Output Voltage Load Regulation, LDO Mode	$100\mu A < I_{LOAD} < 50mA$ $V_{LOWQ} = 0V$		0.1		%
Maximum Duty Cycle	$V_{FB} \leq 0.4V$	100			%
PWM Switch ON-Resistance	$I_{SW} = 50mA$ $V_{FB} = 0.7V_{FB_NOM}$ (High Side Switch)		0.4		Ω
	$I_{SW} = -50mA$ $V_{FB} = 1.1V_{FB_NOM}$ (Low Side Switch)		0.4		
Oscillator Frequency		7.2	8	8.8	MHz
LOWQ threshold voltage		0.5	0.85	1.3	V
LOWQ Input Current			0.1	2	μA
Enable Threshold		0.5	0.85	1.3	V
Enable Input Current			0.1	2	μA
LDO Dropout Voltage	$I_{OUT} = 50mA$, Note 5		110		mV

EX1030, 3

Reply (Paper 25), 24-25

AP7331 Datasheet

Electrical Characteristics

($T_A = 25^\circ\text{C}$, $V_{IN} = V_{OUT} + 1\text{V}$, $C_{IN} = 1\mu\text{F}$, $C_{OUT} = 1\mu\text{F}$, $V_{EN} = 2\text{V}$, unless otherwise stated)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
I_Q	Input Quiescent Current	$V_{EN} = V_{IN}$, $I_{OUT} = 0\text{mA}$	—	55	75	μA
		$V_{EN} = V_{IN}$, $I_{OUT} = 300\text{mA}$	—	65	85	
I_{SHDN}	Input Shutdown Current	$V_{EN} = 0\text{V}$, $I_{OUT} = 0\text{mA}$	—		1	μA
I_{LEAK}	Input Leakage Current	$V_{EN} = 0\text{V}$, OUT grounded	—		1	μA
$V_{Dropout}$	Dropout Voltage (Note 4)	$I_{OUT} = 300\text{mA}$		300	550	mV
V_{REF}	ADJ Reference Voltage (Adjustable version)	$I_{OUT} = 0\text{mA}$		0.4		V
I_{ADJ}	ADJ Leakage (Adjustable version)		—		1	μA
V_{OUT}	Output Voltage Accuracy	$T_A = -40^\circ\text{C}$ to 85°C , $I_{OUT} = 30\text{mA}$	-2		2	%
$\Delta V_{OUT} / \Delta V_{IN} / V$	Line Regulation	$V_{IN} = (V_{OUT} + 1\text{V})$ to V_{IN-Max} , $V_{EN} = V_{IN}$, $I_{OUT} = 1\text{mA}$		0.01	0.20	%/V
$\Delta V_{OUT} / V_{OUT}$	Load Regulation	$V_{IN} = (V_{OUT} + 1\text{V})$ to V_{IN-Max} , I_{OUT} from 1mA to 300mA	-0.6		0.6	%
t_{ST}	Start-up Time	$V_{EN} = 0\text{V}$ to 2.0V , $V_{OUT} = 1\text{V}$, $I_{OUT} = 300\text{mA}$		80		μs
PSRR	PSRR	$V_{IN} = [V_{OUT} + 1\text{V}]V_{DC} + 0.5V_{ppAC}$, $f = 100\text{Hz}$, $I_{OUT} = 30\text{mA}$		65		dB
I_{SHORT}	Short-circuit Current	$V_{IN} = V_{IN-Min}$ to V_{IN-Max} , $V_{OUT} < 0.2\text{V}$		100		mA
I_{LIMIT}	Current Limit	$V_{OUT}/R_{OUT} = 1\text{A}$	400	600		mA
V_{IL}	EN Input Logic Low Voltage	$V_{IN} = V_{IN-Min}$ to V_{IN-Max}			0.4	V
V_{IH}	EN Input Logic High Voltage	$V_{IN} = V_{IN-Min}$ to V_{IN-Max}	1.4			V
I_{EN}	EN Input Current	$V_{IN} = 0\text{V}$ or V_{IN-Max}	-1		1	μA
T_{SHDN}	Thermal Shutdown Threshold			140		$^\circ\text{C}$
T_{HYS}	Thermal Shutdown Hysteresis			15		$^\circ\text{C}$
θ_{JA}	Thermal Resistance Junction-to-Ambient	SOT25 (Note 5)		190		$^\circ\text{C}/\text{W}$
		DFN2020-6 (Note 6)		167		$^\circ\text{C}/\text{W}$

EX1031, 151

Reply (Paper 25), 24-25

General Tradeoffs Do Not Discourage a Combination



“In Valencell’s view, transmittal-type PPGs are not faced with the same short-circuit issue and thus can pursue other tradeoffs such as improving robustness at the expense of unfocused light. . . . But we agree with the Board’s finding that a generalized statement discussing tradeoffs in design does not rise to the level of discouraging the combination[.]”

Valencell, Inc. v. Fitbit, Inc., 786 F. App’x 247, 250 (Fed. Cir. 2019)

Reply (Paper 25), 23

Patent Owner's Sur-Reply Argument on 2013 Manufacturing Technology Is New

Even reading the MIC3385 datasheet as Petitioner suggests does not help because the current savings for Rincon-Mora and Al-Shyoukh's architectures would be far lower due to manufacturing technology advances between the prior art publication dates (late 1990s for Rincon-Mora and mid-2000s for Al-Shyoukh) and the '074 patent priority date (2013). EX2021, ¶95 (discussing 5-generation advancement); EX1029 (Taylor Tr.), 114:2-118:21 (explaining impact of manufacturing advancements on leakage/quiescent current); EX1029, 117:16-118:1 (Dr. Taylor discussing "vast difference" between Rincon-Mora/Al-Shyoukh manufacturing technologies (2 μ m and 0.35 μ m respectively) and 2013 manufacturing). "You're comparing an antique to a really modern process, and

Sur-Reply (Paper 29), 27-28

(200mA versus 50mA) at a slightly lower quiescent current. It's unclear how much of this improvement is due to the higher gm available in the 0.35 μ m technology used by Al-Shyoukh versus the 2 μ m technology used by Rincon-Mora (5 generations of technology). [EX1004, Table II]

EX2021 ¶ 95

Pet. Motion to Strike (Paper 33), 1-3

APPENDIX

Dependent Claims

2. The voltage regulator according to claim 1, further comprising a gm-boost circuit coupled to the current buffer driver.

3. The voltage regulator according to claim 2, wherein the gm-boost circuit increases the current buffer driver input impedance.

4. The voltage regulator according to claim 2, wherein the gm-boost circuit enables the current buffer driver to have a large gm value.

5. The voltage regulator according to claim 1, further comprising a compensation capacitor coupled between the output power driver and a cascode node of the operational amplifier.

EX1001, Claims 2-5

Dependent Claims

6. The voltage regulator according to claim 1, wherein the voltage regulator is a low drop out (LDO) voltage regulator.

7. The voltage regulator according to claim 1, wherein the operational amplifier has a first input adapted for coupling to a voltage reference, and a second input coupled to the feedback loop.

8. The voltage regulator according to claim 1, wherein the operational amplifier is a low gain and high bandwidth amplifier.

9. The voltage regulator according to claim 8, wherein the low gain and high bandwidth amplifier is a folded-cascode amplifier.

EX1001, Claims 6-9

Dependent Claims

10. The voltage regulator according to claim 9, wherein the operational amplifier comprises diode connected PMOS transistors for lowering an output impedance of the folded-cascode amplifier.

11. The voltage regulator according to claim 1, wherein the current buffer driver is an operational transconductance amplifier (OTA).

12. The voltage regulator according to claim 1, wherein the current feedback circuit senses a current change at the output power driver.

13. The voltage regulator according to claim 1, wherein the current feedback circuit provides transient enhancement for improved load regulation.

EX1001, Claims 10-13

Dependent Claims

14. The voltage regulator according to claim 1, wherein the current feedback circuit provides a feedback voltage from an output voltage node.

15. The voltage regulator according to claim 1, wherein the current buffer driver has a low output impedance.

16. The voltage regulator according to claim 1, further comprising capacitors in the biasing circuit for improving noise immunity thereof.

17. The voltage regulator according to claim 1, wherein the voltage regulator is a USB voltage regulator.

18. The voltage regulator according to claim 1, wherein the current buffer driver has low input impedance and provides a high frequency pole that does not substantially affect the voltage regulator dominant pole.

EX1001, Claims 14-18

Certificate of Service (37 C.F.R. § 42.6(e)(4))

I hereby certify that the attached PETITIONER’S DEMONSTRATIVES was served as of the below date via e-mail (by agreement) to the following counsel of record for the Patent Owner:

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