

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APTIV SERVICES US, LLC,
Petitioner,

v.

MICROCHIP TECHNOLOGY INC.,
Patent Owner.

Case No. IPR2024-00646

U.S. Patent No. 9,471,074 B2

**PATENT OWNER'S REQUEST FOR DIRECTOR REVIEW
OF THE PANEL'S FINAL WRITTEN DECISION**

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	ARGUMENT.....	4
A.	The Board’s Motivation Finding Constitutes Material Error and Is an Abuse of Discretion Because Both Primary References Present Standby Current as a Solved Problem.....	4
B.	The Board Misapplied <i>KSR</i> ’s “Known Technique” Framework.....	10
C.	The Board Improperly Dismissed Patent Owner’s Teaching-Away and Tradeoff Arguments and Evidence.	11
III.	CONCLUSION	15

Microchip Technology Inc. (“Patent Owner”) respectfully requests Director Review of the Board’s Final Written Decision (“FWD,” Paper 49) finding all challenged claims of U.S. Pat. 9,471,074 (“the ’074 patent”) unpatentable as obvious over Al-Shyoukh (Ex. 1004), Ivanov (Ex. 1005), and Stanescu (Ex. 1006).

I. INTRODUCTION

The ’074 patent relates to voltage regulator design. Among other elements, independent claim 1 recites “an enable/disable function to enable/disable the biasing circuit for reducing standby current” (limitation 1[d]). Petitioner concedes that neither primary reference—Al-Shyoukh or Rincon-Mora—discloses this limitation, and in each instance relies on Ivanov to supply the missing limitation. *See* Pet. at 22; Ex. 2018, 128:17–129:6, 225:6–20. Petitioner’s entire motivation to combine argument amounted to the assertion that Al-Shyoukh is “concerned with power efficiency” and “Ivanov’s mechanism saves power by shutting off circuitry when it is not needed.” Pet. at 25–26.¹ Likewise, Petitioner’s expert declaration was equally

¹ The entirety of Petitioner’s motivation to combine analysis consists of the two short sentences below (which are substantially identical for both the Rincon-Mora and Al-Shyoukh grounds):

A POSITA would have been motivated to use Ivanov’s disable/enable control mechanism for the biasing circuit for Rincon-Mora’s LDO. Both Rincon-Mora and Ivanov are highly concerned with power efficiency, and Ivanov’s mechanism saves power by shutting off unused

conclusory and simply regurgitated Petitioner’s brief. Ex. 1002, ¶67. The Board adopted this conclusory “reasoning.” FWD at 34–36. In doing so, the Board legally erred and committed several material errors of fact and abuses of discretion.

First, the Board ignored Petitioner’s own primary reference, Rincon-Mora (Ex. 1013), which—together with the companion Rincon-Mora Paper (Ex. 1014) (collectively “Rincon-Mora”)—establishes that a person of ordinary skill in the art (“POSITA”) would have considered the no-load quiescent current in these voltage regulators to be effectively zero, and thus not a problem that needing solving. This was material error because Patent Owner’s arguments and evidence regarding Rincon-Mora were a predicate for (and incorporated into) its argument as to why a POSITA would not be motivated to combine the Ivanov reference with Al-Shyoukh. In particular, Patent Owner’s briefing on the Rincon-Mora ground addressed in detail the treatment of standby current in the prior art, including why the specific prior art at issue taught away from combining Ivanov. The Board’s selective approach deprived it of the very analysis that would have illuminated the deficiencies in its Al-Shyoukh–Ivanov finding.

circuitry. [cites to Ivanov and Rincon-Mora] In addition, Ivanov specifically states that voltage regulators were an intended application for its circuit.

Pet. at 64 (Rincon-Mora); *see also* Pet. at 25 (Al-Shyoukh).

To justify ignoring Rincon-Mora, the Board pointed to the fact that the oral hearing occurred one month before Chief Administrative Patent Judge Boalick issued his memo requiring final written decisions to address all grounds. FWD at 2. But this is no excuse: Federal Circuit precedent required the Board to address all grounds, the Board gave itself six additional months to develop a complete analysis, and, as noted, the Board’s failure to address Rincon-Mora here is particularly problematic because Patent Owner’s Al-Shyoukh analysis was expressly predicated on Rincon-Mora. The Board has left the parties, the Director, and ultimately, the Federal Circuit, with an incomplete decision that evades meaningful review.

Second, the Board committed legal error by misapplying *KSR*’s “known technique” framework. In particular, the Board’s misunderstood *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023). In *Intel*, a known component was substituted for a functionally equivalent alternative already present in the prior art (*see Intel*, 61 F.4th at 1381), but here, Petitioner proposed adding an entirely new subsystem—enable/disable circuitry—to a reference that never contained such a component to begin with and whose designers touted that they had eliminated the need for such a component.

Third, the Board improperly collapsed Patent Owner’s distinct motivation and teaching-away arguments, effectively shifting the burden of proof. The Board swept all countervailing considerations and tradeoffs under the rug in a single sentence, and failed to address whether the combination would actually be operable or

beneficial. These errors are not harmless: every challenged claim requires limitation 1[d], and the Board’s unsupported finding on that limitation is the dispositive issue.

II. ARGUMENT

The Director reviews final Board decisions for “(a) an abuse of discretion, (b) important issues of law or policy, (c) erroneous findings of material fact, or (d) erroneous conclusions of law.” www.uspto.gov/patents/ptab/decisions/director-review-process, §II.B (Feb. 6, 2026).

A. **The Board’s Motivation Finding Constitutes Material Error and Is an Abuse of Discretion Because Both Primary References Present Standby Current as a Solved Problem.**

The Board’s entire motivation analysis rests on the premise that Al-Shyoukh’s quiescent current presented a problem that Ivanov’s enable/disable mechanism would help solve. FWD at 34–35. Indeed, the Board asked at oral argument whether there was evidence that the quiescent current in the range of 20 microamps was *de minimis* or negligible. Paper 44 (“Hearing Tr.”), 18:4-24. Counsel for Petitioner responded that neither Rincon-Mora nor Al-Shyoukh say this. *Id.* But the record evidence establishes the opposite: both Al-Shyoukh and Rincon-Mora present their no-load quiescent current as effectively zero—*i.e.*, there was no problem left to solve. Indeed, both references tout as one of their principal advantages that their respective voltage regulator designs are extremely current efficient and thus, unlike other prior art voltage regulators, do not need to incur the overhead, expense, and tradeoffs involved in adding an enable/disable function.

Rincon-Mora. The Rincon-Mora patent (Ex. 1013) states in its Abstract that it “provides improved transient response performance to the application of various load current step stimuli while requiring *no standby or quiescent current during zero output current load conditions.*” Ex. 1013, Abstract (emphasis added). Not low. Not reduced. *No* standby current. The Board parsed a sentence in column 1 to conclude that this “no standby current” language referred only to the transient boost circuit, not the entire regulator. FWD at 35. But the Board ignored the Abstract, which attributes this characteristic to the “LDO voltage regulator” as a whole. The Board also ignored that the companion Rincon-Mora Paper (Ex. 1014), which Petitioner’s own expert described as effectively the same reference (Ex. 2018, 124:17–22), reports the achieved quiescent current as 23 μA —meaning that to Rincon-Mora, 23 μA *was* effectively zero. Ex. 1014, Abstract, Table I, Fig. 11.

This conclusion is confirmed by the Rincon-Mora Paper’s own analytical framework. The paper states that “the biasing conditions for the case of zero load-current can be designed to utilize a *minimum* amount of current, which yields maximum current efficiency and prolonged battery life.” Ex. 1014 at 2 (emphasis added). The word is “minimum”: categorical, not aspirational. Table I of the Rincon-Mora Paper shows that all three circuit variants (full LDO, without current boost, without transient boost) achieve exactly 23 μA at no-load. *Id.* at 7. The current boosting and transient boosting techniques add zero quiescent current at no load. There is nothing left to remove.

Moreover, even under Petitioner’s own reading of Rincon-Mora (that the “no standby current” language refers just to the transient response boost circuit (box 40 in Figure 3), not the LDO as a whole) Patent Owner’s argument is even stronger. The Petitioner’s proposed combination maps Ivanov’s enable/disable to the I-bias current source inside box 40. Hearing Tr., 37:22–24. But if box 40 already consumes zero quiescent current, as all parties agreed, then adding an enable/disable circuit that itself *consumes* current (up to 7 μ A, as Petitioner’s counsel conceded, Hearing Tr., 48:6) to disable a circuit drawing zero current results in a ***net increase*** in quiescent current. The result is the same under either reading of the reference: there is no motivation to combine. Rather than engaging with these facts, the Board focused on grammatically parsing a single sentence from the Rincon-Mora patent and reached a conclusion that is belied by Rincon-Mora’s express disclosures. This was material error and an abuse of discretion.

Critically, the Rincon-Mora patent itself acknowledges, in its Background, that “some LDO voltage regulators incorporate a separate enable terminal to switch the device into a standby mode of operation to minimize power consumption when the associated device is disabled.” Ex. 1013, 1:22–27. Rincon-Mora was aware of enable/disable techniques and touted that its proposed architecture eliminated the need for an enable/disable function for its biasing circuit. This is not an omission—it is a deliberate design choice reflecting the view that the achieved quiescent current required no further mitigation.

Al-Shyoukh. Al-Shyoukh achieves an even lower quiescent current of 20 μ A at no-load—the lowest of any comparable design in its comparison table. Ex. 1004 at 10 (Table II). Al-Shyoukh describes this as “small quiescent current” without qualification. *Id.* at 8. The paper reports 99.8% worst-case current efficiency at full load. *Id.* Similar to Rincon-Mora, Al-Shyoukh’s disclosure—*viz.*, its novel buffer impedance attenuation (BIA) technique—is directed to preventing quiescent current from *increasing*. *Id.* at 2. The paper never frames 20 μ A as a compromise, a tradeoff, or a value that could be improved. It is presented as the solution. The paper identifies no future work geared toward quiescent current reduction. *Id.* at 9–10.

The Board cited Al-Shyoukh’s general “concern” with power efficiency as motivation to combine with Ivanov. FWD at 35. But a generic concern that the reference itself fully resolves is not substantial evidence of motivation to look to a secondary reference for further improvement. *See, e.g., Arctic Cat Inc. v. Polaris Indus., Inc.*, 795 F. App’x 827, 833 (Fed. Cir. 2019) (no motivation to combine where patent challenger “failed to prove that the[] alleged problems with [the primary reference] existed such that a skilled artisan would been motivated to combine [the primary reference]with the other prior art to overcome those alleged problems.”). Al-Shyoukh is “concerned with power efficiency” (Pet. at 25) in the same way that every engineering paper is concerned with its subject matter. The fact that Al-Shyoukh addresses power efficiency does not mean it left a power-efficiency problem unsolved.

The Board sought to justify its failure to conduct the requisite analysis by noting that the IPR petition was filed shortly before Chief Administrative Patent Judge Boalick's July 2025 directive took effect that required all grounds to be addressed.² But even before Judge Boalick's memo, the Federal Circuit instructed that, "if the Board institutes an IPR, it must similarly address all grounds of unpatentability raised by the petitioner." *AC Techs. S.A. v. Amazon.com, Inc.*, 912 F.3d 1358, 1364 (Fed. Cir. 2019); *see also id.* at 1360 ("Precedent mandates that the Board consider all grounds of unpatentability raised in an instituted petition."); *Cook Grp. Inc. v. Bos. Sci. Scimed, Inc.*, 809 F. App'x 990, 997 (Fed. Cir. 2020) ("We agree that the Board's failure to address Cook's Embodiment #2 arguments was error"). Even setting that aside, the fact that the prevailing rule (which now requires resolution of all grounds) was not in effect when oral argument was held does not justify the Board's failure here for several reasons. **First**, addressing the Rincon-Mora ground was a necessary predicate to analyzing Al-Shyoukh. In failing to address the underlying substance of Patent Owner's motivation to combine argument, the Board failed to conduct the analysis necessary to decide the Al-Shyoukh ground (which is precisely the kind of holistic analysis the Director now

² The memo is available at

www.uspto.gov/sites/default/files/documents/20250729095727582.pdf.

requires in all IPRs).³ **Second**, the stated purpose is that, “[a]mong other reasons, this approach will promote compact decision making and ensure that panels will not be required to address grounds for the first time in the event of a remand from a Director Review decision or Federal Circuit appeal.” This applies with particular force here because, as noted, Patent Owner’s Al-Shyoukh analysis was explicitly predicated on its treatment of Rincon-Mora. **Third**, the Board afforded itself an additional six months to issue the FWD, which should have afforded ample time to address all grounds. Paper 46. Finally, in the event that Patent Owner appeals, the Federal Circuit will need the Board’s full and complete analysis to enable meaningful review (which, as Judge Boalick noted, is the reason for the memo).

Moreover, Patent Owner presented un rebutted evidence—including data sheets for commercially available voltage regulators (Exs. 2011, 2019, 2020, 2012, 2016)—showing that contemporaneous voltages regulators that do employ an

³ The Board’s overall inattentiveness is apparent from the first page of the FWD, where the Board misidentified the Patent Owner as “Immersion Corporation” instead of Microchip Technology Inc. FWD at 1. Moreover, the Board appears to have been pressed for time as it granted itself a six-month extension to issue the FWD. Paper 46. These are not indications of the care that should be demanded of an administrative body entrusted with adjudicating (and in this case revoking) important private property rights.

enable/disable function still do not achieve the reduced 20–23 μ A quiescent current achieved by Al-Shyoukh and Rincon-Mora (which both lack an enable/disable function). Paper 19 (“POR”) at 64–65. The Board ignored this evidence too.

Finally, the prosecution history of the ’074 patent underscores the point. During prosecution, the examiner rejected claims over Al-Shyoukh, and the addition of the enable/disable limitation overcame that rejection. Ex. 2005 at 107-112 and 140. If the combination of Al-Shyoukh with a known enable/disable technique were as straightforward as Petitioner contends, the Examiner—who examined the very same Al-Shyoukh reference at issue here—would not have allowed the claims.

B. The Board Misapplied KSR’s “Known Technique” Framework

The Board endorsed Petitioner’s argument that enable/disable was a “known technique” applied to prior art “ready for improvement” under *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007). FWD at 33, 35. But the *KSR* framework requires that the known technique yield “predictable results” when applied. *KSR*, 550 U.S. at 416. The Board made no finding about predictable results.

Moreover, the “ready for improvement” prong requires evidence that the prior art was actually deficient in the relevant respect—*i.e.*, there was a “known problem” with the art. *Intel*, 61 F.4th at 1380 (“[I]f there’s a known technique to address a known problem using ‘prior art elements according to their established functions,’ then there is motivation to combine.”) (quoting *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 799-800 (Fed. Cir. 2021)). As explained above, both Rincon-Mora and

Al-Shyoukh already solved the quiescent problem. The Board cited no evidence that Al-Shyoukh was “ready for improvement” with respect to quiescent current—let alone that bolting on Ivanov’s enable/disable function would actually work or provide improvement. Petitioner relied on *Intel v. PACT XPP* for the proposition that applying a known technique to solve a known problem is obvious. Paper 25 (“Reply”) at 17–18. But the premise of *Intel* is that there must be a known problem. Here, both Al-Shyoukh and Rincon-Mora establish that there isn’t one: both references present their quiescent current as effectively zero. A POSITA would have had no reason to apply Ivanov to solve a problem that the prior art itself declares to have resolved. And unlike in *Intel*, where a known component was substituted for a functionally equivalent alternative already present in the prior art, *see Intel*, 61 F.4th at 1381, here Petitioner proposes adding an entirely new subsystem—enable/disable circuitry—to a reference that never contained such a component to begin with and whose designers were quite proud to report eliminated the need for such a component. The *Intel* framework does not support obviousness where the proposed modification addresses a non-existent deficiency and introduces current-consuming complexity to a circuit already optimized for minimal current consumption.

C. The Board Improperly Dismissed Patent Owner’s Teaching-Away and Tradeoff Arguments and Evidence.

Patent Owner raised two distinct arguments, that: (a) Petitioner failed to show a motivation to combine, and (b) the prior art teaches away from the proposed

combination. POR at 61–72. The Board applied the teaching-away standard—whether the prior art “criticizes, discredits, or otherwise discourages investigation”—to reject both. FWD at 35 (quoting *Meiresonne v. Google, Inc.*, 849 F.3d 1379, 1382 (Fed. Cir. 2017)). Conflating these was legal error.

Lack of motivation is not the same as teaching away, and the former requires a lower threshold. The burden remains on Petitioner to establish an affirmative reason why a POSITA would have looked to Ivanov to modify Al-Shyoukh. By applying the teaching-away standard to the motivation inquiry, the Board effectively required Patent Owner to prove that the combination was affirmatively discouraged, rather than requiring Petitioner to prove it was motivated. This improperly shifted the burden of proof. *See In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1377–78 (Fed. Cir. 2016); *see also Samsung Display Co. et al. v. Polaris PowerLED Techs., LLC*, IPR2023-00771, Paper 40 at 60 (PTAB Oct. 11, 2024).

As to teaching away specifically, the Board stated that “Patent Owner has not pointed to anything in the prior art that criticizes, discredits, or otherwise discourages investigation into the claimed invention.” FWD at 35. This assertion is factually incorrect and a material error. If both primary references present their standby current as effectively zero, this necessarily discourages investigation into techniques for reducing it further. A reference need not contain the words “do not add an enable/disable circuit” to teach away; presenting a design parameter as already optimized discourages further optimization of that parameter.

The Board also categorically dismissed Patent Owner’s un rebutted evidence of tradeoffs with a single citation to *Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006), for the proposition that “simultaneous advantages and disadvantages” do not “necessarily obviate motivation.” FWD at 36. But *Medichem* requires the Board (and the petitioner) to actually ***consider*** the tradeoffs, not dismiss them categorically. 437 F.3d at 1165; *see also Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1331–32 (Fed. Cir. 2019) (“[T]he benefits, *both lost and gained*, should be weighed against one another.”).

Al-Shyoukh expressly states there are “four major [LDO voltage regulator] performance requirements,” that “are, however, difficult to achieve simultaneously.” Ex. 1004 at 1; *see also id.* at 9 (discussing “***evaluating the tradeoffs*** between the response time T_r , the quiescent current I_q and the maximum load current $I_{L,max}$.” (emphasis added)). It was undisputed that voltage regulator design considerations “include circuit size, speed, complexity, cost, regulator stability, drop-out voltage, system-level considerations, intended applications, etc.” *E.g.*, POR at 65 and §III.D; Ex. 2021, ¶63 (a POSITA would need to consider speed, power consumption, application usage, cost, longevity, operating environment and conditions, part lifetime, development time and complexity, among many others); Ex. 1014 at 1.

Petitioner’s expert admitted that “when you decide the circuiting [sic] system, there are just so many consideration[s] to consider, right. It’s not just in one single angle on this biasing of the regulators or whatever the circuit that you provide. Also,

there's also part of the SOC that you need to consider. So typically that would need to be considered jointly." Ex. 2018, 263:6–16. And yet Petitioner's expert admitted he performed *no analysis* of such tradeoffs and considerations whatsoever. Ex. 2018, 254:13–265:10. For example, Petitioner's expert admitted the following:

"I don't think I can offer that opinions or analysis, you know, as to, you know, what cost that is adding." Ex. 2018, 257:14–258:1 (emphasis added).

"Q. What are the drawbacks to using an enable/disable circuit? A. I suppose that were related to some system design concerns. As I mentioned earlier, *I did not perform system analysis in this particular case at this point*. So I'm not ready to offer that opinion[]." *Id.*, 254:13–255:4.

"Q. And you didn't analyze any of those considerations in your report, did you? ... A. *I don't see other considerations [besides power efficiency] that I've analyzed in my report.*" *Id.*, 264:23–265:10 (emphasis added).

"Q. Did you do any analysis in your report regarding how adding an enable/disable function would impact the speed of the Rincon-Mora or Al-Shyoukh voltage regulators? ... A. *I don't remember that, that I did analysis of that enable and disable and how that impact the regulator speed of Rincon-Mora and Al-Shyoukh.*" *Id.*, 257:4–13 (emphasis added).

"Q. Would you agree with me that there are drawbacks to implementing an enable/disable function? [] A. *As I said, that would also be related to system level concerns, you know. I'm not ready to give that analysis or offer my opinions at this point.*" *Id.*, 255:5–24 (emphasis added).

Petitioner chose not to submit a supplement declaration from Dr. Chen with its Reply brief to address any of the tradeoffs Dr. Chen ignored but admitted would need to be considered. Nor did the Board explain why a POSITA would accept degraded transient response, slower speed, extra circuitry, higher costs, larger chip size, etc. in exchange for (at most) a *de minimus* reduction in an already-minimized (or nonexistent) quiescent current.

Making matters worse, as explained above, neither Petitioner nor the Board has shown that adding Ivanov's enable/disable mechanism to Al-Shyoukh's biasing circuit would, in fact, *work*, or that it would produce a meaningful reduction in quiescent current. In sum, not only did Petitioner and the Board fail to consider the tradeoffs of adding the Al-Shyoukh enable/disable functionality, they had no baseline "benefit" against which to measure the cost of the tradeoffs. *Henny Penny*, 938 F.3d at 1331–32 ("[T]he benefits, *both lost and gained*, should be weighed against one another."). The Board's wholesale failure to engage with the unrebutted tradeoff evidence is an abuse of discretion.

III. CONCLUSION

Patent Owner respectfully requests that the Director reverse the FWD, or at a minimum vacate the FWD and remand for further proceedings consistent with a proper motivation to combine analysis.

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing paper was caused to be served on April 17, 2026 via email upon counsel for Petitioner at the addresses indicated:

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