

State-of-the-Art and Future Prospects for Analogue Signal Processing -A Tutorial

Gabor C. Temes, Lawrence E. Larson and Kenneth W. Martin

University of California
Los Angeles, CA 90024, USA

ABSTRACT

Despite the proliferation of VLSI digital integrated circuits, the development of analog interface circuits continues to advance rapidly. This paper outlines the major trends in analog integrated signal processing. A/D and D/A converters are becoming the dominant analog components in major systems, and converters that rely on digital post-processing and error correction are becoming increasingly popular. These, and other trends, will be highlighted.

INTRODUCTION

Even though predictions in the rapidly changing area of integrated circuits are risky, certain tendencies are clearly visible. Signal processing, switching and control functions increasingly use digital techniques. This is due to the accuracy, flexibility, programmability and modularity of digital systems, in addition to the high levels of integration achievable in modern digital integrated circuits. As a result, in many signal processors with analog inputs and outputs, the majority of the components are becoming digital, with only a relatively few functions remaining in analog form. These analog circuits usually include the S/H, preamplifier, input/output buffers, pre- and post-filter, equalizers, multiplexer/demultiplexer stages, and A/D and D/A converters. These circuits are necessary for conditioning an analog input signal for digital manipulation, or a digital output signal for analog transmission [1].

In addition to A/D and D/A conversion tasks, analog interface systems are increasingly used for high-speed data transmission, in disk drive systems, and linear fiber-optic ICs for inter-board communications.

A development interesting for those of us who earn their living by designing the circuits performing these functions is that, despite the increased use of digital techniques, R & D activities in the analog area are intensifying, rather than diminishing. One measure of the continuing evolution of analog integrated circuits is the relative number of sessions devoted to analog and digital circuits at the ISSCC. At the 1988 conference, five sessions were devoted to analog techniques, and eight to digital.

The accelerating evolution of analog integrated circuits occurs in part, because as digital integrated circuit technology improves the performance of the analog interface modules must also improve in terms of increased speed and accuracy, as well as reduced chip area and power dissipation. This is made more difficult by the changes (primarily the reduced supply voltage) aimed at improving the reliability, power dissipation, speed and density of the digital circuitry. With the current trend towards low-voltage (3 V) single-supply IC's, the prospect of a dual-supply arrangement is becoming attractive for mixed analog-digital chips.

Overall, especially for parallel digital systems or systems where signals can be stored and post-processed digitally in non-real time, the analog interface is often the bottleneck in mixed analog-digital signal processing. In addition, while the simulation, design and testing of digital logic circuitry has been well supplied with CAD tools, the CAD of analog circuits is still not mature. Because of the wide range and large number of design parameters (such as frequency range, dynamic range, process variables, accuracy, supplies, signal levels, etc.) the development of fully automated analog design techniques, or even of a complete library of pre-designed modules, is very unlikely. Thus, analog circuit design is likely to remain, for the foreseeable future, an art rather than an automated menial task. (It should, however, be noted that with the reduction of device dimensions to the submicron range, high-speed digital circuit design is also becoming a similarly sophisticated task - in fact it is becoming essentially analog circuit design!)

Finally, even for some "purely digital" ICs, such as dynamic and static RAMs, major improvements in speed have been obtained due to faster analog components (bus drivers, sense amplifiers, etc.)

In the next sections, recent developments in some of the most important analog signal processing circuits will be briefly discussed. The discussion will be restricted to circuits realized in MOS and GaAs technologies, since the writers' interest and experience is mostly in these fields.

DATA CONVERTERS

In terms of importance, variety, sophistication and difficulty, A/D and D/A converters represent perhaps the greatest challenge for today's circuit designer.

Next, we list some interesting recent developments in this area. No attempt is made to make this survey complete or even fully representative of the global activities in the field.

Figure 1 (compiled by Tanju Cataltepe of UCLA) illustrates the performance of some MOS and GaAs A/D converters reported recently, in an accuracy-vs-speed coordinate system. The plot demonstrates the difficulty in overcoming technological limitations on both accuracy and speed. Major improvements in the conversion speed are currently being triggered by the use of submicron bipolar, MOS and especially GaAs technologies. As an example, Table I summarizes the performance of a recent high-speed (1 GS/s) interleaved A/D converter [2]. It requires two GaAs and four Si bipolar integrated circuits. The GaAs chips provide accurate sampling, while the Si chips act as flash ADC's. A 6-bit accuracy was achieved. This project also demonstrated an optimum use of the different high-speed technologies, since GaAs is very attractive for sample-and-hold functions, due to the availability of Schottky diodes and the low input leakage current, and Si bipolar technology is attractive for flash ADC's, due to the small offset voltage and hysteresis of the resulting comparators.

GaAs heterojunction bipolar transistor (HBT) technology promises to be the "ultimate" vehicle for ADC applications, since it combines the intrinsic high speed of GaAs with the excellent matching properties of silicon bipolar technology. A 4-bit 2.5GS/s HBT flash ADC was recently announced [3]. The comparator uniformity was comparable with 6-bit operation, and higher levels of integration are planned. Simulations indicate that a 12-14 bit resolution at sample rates approaching 100 MHz is possible with this approach.

An economical solution for high-speed and medium-accuracy data conversion is to use a pipelined - or multi-pass - configuration. Several architectures have been suggested for pipelined ADC's [5]-[7]. In a recent paper [8], a 9-bit 5 MS/s pipelined converter was realized in a 3 μ m CMOS technology. Its performance is summarized in Table II. It achieved its accuracy by using an off-chip digital correction circuitry, which corrected for comparator offset voltage limitations.

At the other end of the spectrum, very high accuracy (14 - 16-bit) conversion can be achieved using oversampling and noise shaping techniques. The basic technique (often called Δ - Σ or Σ - Δ modulation) has existed for over 25 years; however, a number of theoretical and technical innovations occurred recently that renewed interest in the field. These included the discovery that the performance of a high-order Δ - Σ loop can also be achieved by using a number of coupled first-order (and hence absolutely stable) loops. A CMOS system which achieves 16 bits using three coupled stages is described in [4]. Its performance is summarized in Table III; the block diagram is shown in Figure 2.

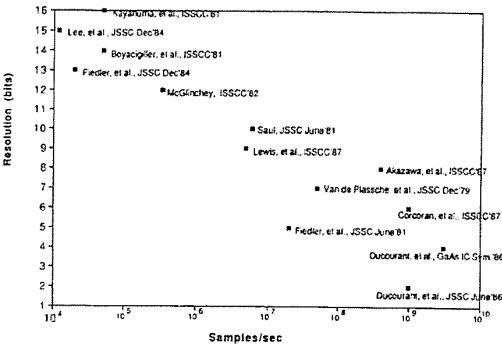


Figure 1. A/D converter performances

Table I. GaAs-BJT ADC performance [2]

Sample Rate	1 Gs/s (and lower)
Bandwidth (3 dB)	1.7 GHz
Input Range	± 0.64 V
Random Noise	< 5 mV pp < 0.25 LSB
Effective Bits	
1 Gs/s, 1 GHz input	5.2 bits
1 Gs/s, 200 kHz input	6.9 bits
Power	16 W

Table II. Pipelined CMOS ADC performance [8]

Technology	3- μ CMOS
Resolution	9 bits
Conversion Rate	5 Ms/s
Area*	8500 mils ²
Power Supplies	± 5 V
Power Dissipation	180 mW
Input Capacitance	3 pF
Input Offset	< 1 LSB
CM Input Range	± 5 V
DC PSRR	50 dB

Table III. Δ - Σ CMOS ADC performance [4]

Resolution	16 bit
Sampling frequency(fs)	≤ 3 MHz
Signal bandwidth	fs/128
Signal/(Noise+THD)	91 dB
THD	0.002 %
Supply voltage	5 V
Power Dissipation	110 mW

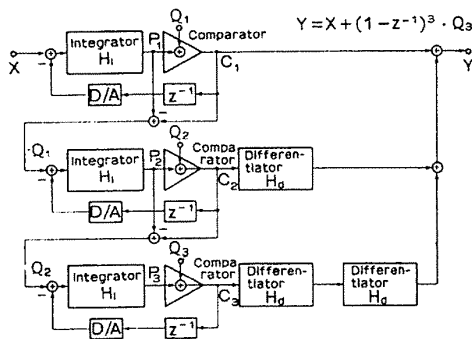


Figure 2. A recently proposed [4] Δ - Σ A/D converter architecture

A pipelined D/A converter, whose analog circuitry consists only of a small number of equal-valued grounded capacitors, switches and a buffer, is described in a companion paper [9]. The basic scheme is shown in Figure 3; the measured performance of an integrated version, fabricated in 3 μ m CMOS technology, is summarized in Table IV. Another pipelined DAC, presented in another companion paper [10], is illustrated in Figure 4. It utilizes the MSB first and the LSB last, and hence can be used to provide the reference voltages needed in the pipelined ADC of ref.[7].

ANALOG FILTERS

The design of integrated analog filters is often considered to be a mature area, with many techniques available for synthesizing high-performance precision circuits. Nevertheless, a number of novel design ideas have appeared recently. In the switched-capacitor (SC) realization area, new integrator and gain stages which are insensitive to both the offset and the finite gain of the op-amps have been published [11]-[13]. These stages have been used recently to design a number of GaAs SC circuits [14] with clock rates exceeding 100 MHz and signal frequencies up to 10 MHz. Figure 5 illustrates the response of an elliptic GaAs filter with a 100 MHz clock rate.

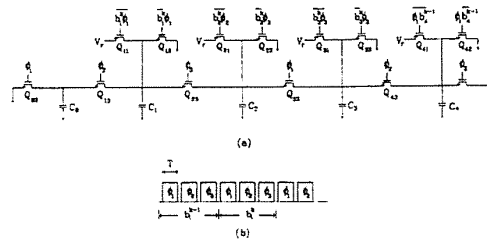


Figure 3. A pipelined D/A converter: a. configuration; b. clock signals

Table IV. Measured performance of the DAC of Figure 3

Nominal Resolution	10 bits
Accuracy Resolution	11 bits
Differential Nonlinearity	± 0.235 LSB
Integral Nonlinearity	0.2% of full scale
Analog Output Voltage	3.2V max.
Supply Voltage	10V
Data conversion Rate	333 kS/s
Chip Area	0.73 mm ²

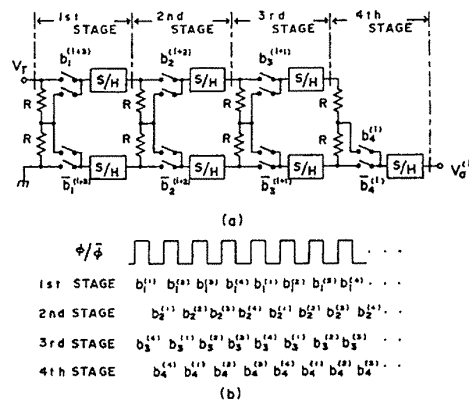


Figure 4. An alternative DAC which converts the MSB first

An alternative approach to sampled data analog filtering was presented by Vallancourt and Tsividis [15]. It is based on determining the value of each branch gain by the duty cycle of a digitally controlled analog transmission gate. The resulting circuit is

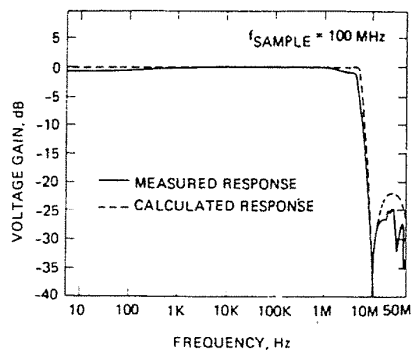


Figure 5. The measured response of a GaAs SC filter [14]

digitally programmable, and programming of the topology is also possible, so that high-pass, band-pass and low-pass configurations can be realized with the same structure.

A number of different architectures have been developed for realizing unswitched (continuous-time) integrated analog filters [16]-[18]. These circuits are not subject to the signal and wideband noise aliasing of switched-capacitor filters. On the other hand, they require fairly sophisticated control circuitry to achieve accurately controlled time constants, and also some way must be found to eliminate harmonic distortion. The latter goal can be achieved by using fully differential signal paths, and special cross-coupling circuitry [19].

APPLICATIONS

Most commercial integrated analog signal processing circuits have been developed for specific applications. In the past, the largest-volume area has been telecommunications. In digital voice transmission systems, coder/decoder (codec) chips are used to perform the transformation of an analog voice signal into a PCM digital bit stream for transmission, and to perform the reverse operation at the receiving apparatus. These tasks involve a multiplicity of analog functions, such as prefiltering, A/D and D/A conversion, S/H, voltage reference generation, amplification and buffering, etc. Over the past 10 years, more and more of these functions have been integrated on a single chip, along with the necessary digital logic functions. As an example, Figure 6 shows the block diagram of an early single-chip codec, the AMI S3506.

Another popular telecommunication chip contains the modulator-demodulator (modem). The modem converts the digital bit stream generated in data transmission systems into a signal which falls into the passband range of voice-grade telephone facilities. They may use frequency-shift keying (FSK) or phase-shift keying

(PSK) modulation. Figure 7 illustrates the organization of a single-chip modem (Sierra Semiconductor's SC 11004).

In the past, both the sophistication (as measured, e.g., by the number of on-chip functions, or the total number of on-chip transistors) and the speed (bit rate) of these chips have been rapidly increasing, due to stiff competition. It is expected that this trend will continue in the foreseeable future.

There are many other high-volume communication applications for analog signal processing circuits, such as the generation and detection of dual-tone

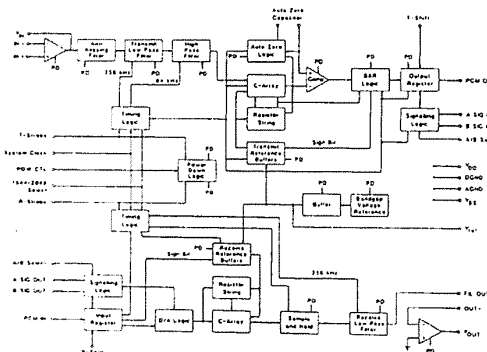


Figure 6. The block diagram of the AMI S3506 codec

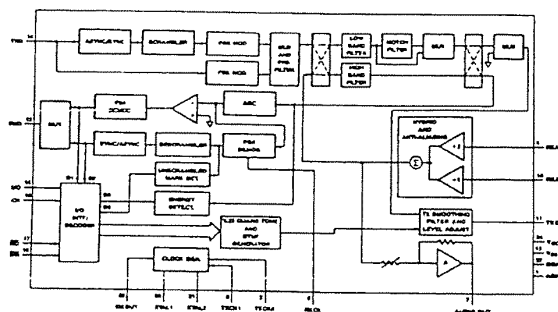


Figure 7. Block diagram of the SC 1104 modem

A very promising future application of fully-integrated analog signal processing is the realization of FM radio receivers. If these can be produced in a cost-effective way, a very large market will open up for them in, e.g., radio controls, pagers, inexpensive radios, etc. In a recent paper [21], B.S. Song described a chip realizing a narrow-band high-selectivity FM receiver, using SC filters. The block diagram of the receiver is shown in Figure 9; the measured performance in Table V. The operation is not adequate for high-fidelity reception, but it does illustrate the feasibility of single-chip high-performance FM radios.

[illegible]

Figure 8. The block diagram of an ISDN burst transceiver [20]

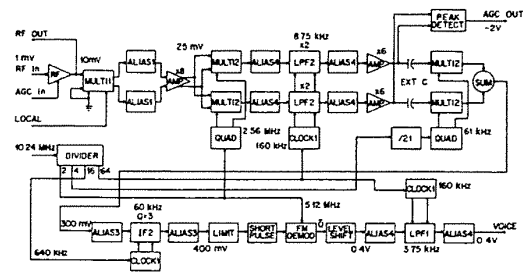


Figure 9. A schematic diagram of a monolithic FM receiver [21]

CONCLUSIONS

References

- [1] P. R. Gray, "Analog ICs in the Submicron Era: Trends and Perspectives," Proc. 1987 International Electron Devices Mtg., Washington, D.C., pp. 5-9.
- [2] K. Poulton, J. Corcoran and T. Hornak, "A 1-GHz 6-bit ADC System", IEEE J. Solid-State Circuits, Vol. SC-22, PP. 962-970, Dec. 1987.
- [3] K.C. Wang, et al, "A 4-Bit Quantizer with AlGaAs/GaAs Heterojunction Bipolar Transistors," Proc. 1987 IEEE GaAs IC Symposium, pp. 83-86.
- [4] Y. Matsuya et al, "A 16-bit Oversampling A-to-D Conversion Technology Using Triple-Integration Noise Shaping" IEEE J. Solid-State Circuits, Vol. SC-22, pp. 921-929, Dec. 1987.
- [5] K. Martin, "A High-Speed, High-Accuracy Pipelined A/D Converter", Conf. Rec. Asilomar Conf. on Circuits, Systems and Computers, Pacific Grove, CA, pp. 489-492, 1981.
- [6] S. Masuda et al, "A CMOS Pipelined Algorithmic Converter", Proc. IEEE Custom IC Conf., Rochester, NY, pp. 559-562, 1984.

- [7] G. C. Temes, "High Accuracy Pipelined A/D Converter Configuration", *Elec. Letters*, Vol. 2, pp. 762-763, Aug. 1985.
- [8] S. H. Lewis and P. R. Gray, "A Pipelined 5 MS/s 9-bit A-to-D Converter", *IEEE J. Solid-State Circuits*, Vol. SC-22, pp. 954-961, Dec. 1987.
- [9] G. C. Temes and F. J. Wang, "Novel Pipelined Data Converters", *Proc. 1988 IEEE Internat. Symp. Circuits and Systems*, Espoo, Finland, June 1988.
- [10] K. Watanabe, G. C. Temes and Y. Moriuchi, "A New D-to-A Conversion Algorithm", *ibid.*
- [11] K. Nagaraj et al., "Switched Capacitor Circuits with Reduced Sensitivity to Finite Amplifier Gain", *Proc. IEEE Internat. Symp. Circuits and Systems*, San Jose, CA, pp. 618-621, 1986.
- [12] K. Haug, G. C. Temes and K. Martin, "Improved Offset Compensation Schemes", *ibid.*, pp. 1054-1057, 1984.
- [13] L. E. Larson and G. C. Temes, "Switched-Capacitor Gain Stage with Reduced Sensitivity to Finite Amplifier Gain and Offset Voltage", *Elec. Letters*, Vol. 22, pp. 1281-1283, Nov. 1986.
- [14] L. E. Larson, K. Martin and G. C. Temes, "GaAs Switched-Capacitor Circuits for High-Speed Signal Processing", *IEEE J. Solid-State Circuits*, Vol. SC-22, pp. 971-981, Dec. 1987.
- [15] D. Vallancourt and Y. P. Tsividis, "A Fully-Programmable Sampled Data Analog CMOS Filter", *ibid.*, pp. 1022-1030.
- [16] Y. Tsividis, M. Banu and J. F. Khoury, "Continuous-Time MOSFET-C Filters in VLSI", *IEEE Trans. Circuits and Systems*, Vol. 33, pp. 125-140, Feb. 1986.
- [17] H. Khorramabadi and P. R. Gray, "High-Frequency CMOS Continuous Time Filters", *IEEE J. Solid-State Circuits*, Vol. SC-19, pp. 939-948, Dec. 1984.
- [18] C. S. Park and R. Schaumann, "Design of an 8th-Order Fully Integrated CMOS 4 MHz Continuous-Time Bandpass Filter", *Proc. Internat. Symp. Circuits and Systems*, pp. 754-757, 1987.
- [19] Z. Czarnul, S. C. Fang and Y. Tsividis, "Improving Linearity in MOS Fully-Integrated Continuous-Time Filters", *Proc. Internat. Symp. Circuits and Systems*, pp. 1169-1172, San Jose, CA., 1986.
- [20] G. J. Smolka et al., "A 384-kbit/s ISDN Burst Transceiver", *IEEE J. Solid-State Circuits*, Vol. SC-22, pp. 1004-1010, Dec. 1987.
- [21] B. S. Song, "A Narrow-Band CMOS FM Receiver Based on Single-Sideband Modulation IF Filtering", *ibid.*, pp. 1147-1154.
- [22] M. J. Steyeart, et. al., "A Micropower Low-Noise Instrumentation Amplifier for Medical Purposes", *ibid.*, pp. 1163-1168.