

SURFACE MICROMACHINED, DIGITALLY FORCE-BALANCED ACCELEROMETER WITH INTEGRATED CMOS DETECTION CIRCUITRY

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ABSTRACT

A surface micromachined, force-balanced capacitive accelerometer is designed and fabricated with on-chip detection circuitry. It has demonstrated the modular integration of CMOS with polysilicon surface micromachining. The capacitive sensing structure consists of two polysilicon layers with the sensing and feedback electrodes underneath and the suspended plate as proof mass, and the sensing axis is perpendicular to the substrate. A unity gain buffer with low input capacitance is designed to actively drive (bootstrap) the ground plane to minimize the parasitic capacitance. Σ - Δ modulation technique is employed in the feedback control loop, in which the mechanical proof mass is used to replace the two integrators in the Σ - Δ loop. This approach provides large dynamic range and directly digital output. To reduce the temperature sensitivity, package-induced stress, and residual stress in the spring, two accelerometers with different proof mass are built side by side and their digital outputs are subtracted. The readout circuits have been characterized successfully. The accelerometer is tested in the self-testing mode and its DC and transient open loop performance have been measured.

INTRODUCTION

Silicon microaccelerometers are a rapidly expanding sensor market segment, with automotive applications driving the development of commercial products [1, 2]. The promise of silicon microaccelerometers is their potential low cost through the application of batch fabrication techniques. First-generation applications will require low-to-intermediate sensitivity: air-bag deployment (50-100g) and chassis control (1-5g) [3]. Microaccelerometers of higher sensitivity (sub milli-g) could be useful for automobile position localization in automated highways, as well as in aerospace navigation systems. As a research vehicle, a low-cost, high performance microaccelerometer is attractive for stimulating new approaches to the micromechanical sense element, position sensing structures and interface electronics, and the overall system architecture, as well as for identifying basic limits and tradeoffs. This paper describes research in the design, fabrication, simulation, and initial self-testing of a high-resolution (sub milli-g), high dynamic range microaccelerometer.

Surface micromachining has clear advantages for fabricating the suspension and proof mass for low-cost microaccelerometers. Thin-film microstructures have lateral dimensions on the order of 100-500 μm -- much smaller than a typical integrated-circuit die size of about 2.5 mm square. Multiple sensing elements to provide ratioed response, auto-ranging, or multi-axis sensing are feasible on a single chip. In contrast, proof masses fabricated by anisotropic etching through the silicon wafer are much larger, leading to a larger, more expensive chip. For surface microstructures, overrange protection is provided by the substrate in one direction, and can be supplied by other micromachined limit stops in other directions, if

necessary. There is no need for one or more capping wafers, as is the case for conventional bulk-micromachined sensing elements.

Capacitive measurement of the proof mass position is naturally suited to surface-micromachined sense elements, given that vertical or lateral gaps on the order of 1 μm are quite feasible. However, sense capacitances are on the order of 100 fF - 1 pF, with on-chip parasitic capacitances which can be substantially larger. The accurate measurement of the sense capacitance is much easier with an on-chip MOS buffer amplifier. Integration of surface microstructures with on-chip MOS electronics using a unique, merged fabrication sequence was demonstrated in 1984 [4, 5]. Recently, a commercial 50 g accelerometer has been reported which merges a single-level polysilicon surface micromachining process with a proprietary Bi-MOS precision analog IC process [6]. This monolithic accelerometer uses a force-balance approach, in which an analog feedback loop applies electrostatic forces to null deflections due to acceleration. Another monolithic accelerometer uses an open-loop design, implemented using an electroformed metal sense element fabricated after standard CMOS capacitive detection and signal-conditioning electronics [7]. Finally, a second polysilicon accelerometer is described for the first time at this workshop [8].

The microaccelerometer described here also uses a polysilicon suspension and proof mass, integrated with CMOS sense and control circuitry. However, we use a modular fabrication sequence, which has been developed in order to provide a generic solution to integrating polysilicon micromechanics with IC processes [9, 10]. In order to achieve linearity and high dynamic range, the proof mass position is sensed capacitively and then input to a one-bit quantizer, which provides a high-frequency pulse train. After digital processing, a 2-bit signal applies electrostatic force to the sense element, nulling its deflection. The suspended proof mass supplies a double integration in the feedback loop, by converting input acceleration into position. Digital force-balance schemes, based on Σ - Δ modulation technique [11], are attractive for achieving high dynamic range and good linearity [12]. Moreover, the asymmetrical feedback electrode layout in the research vehicle makes analog feedback approaches impractical, since they depend on symmetry for cancellation of non-linearities in the electrostatic force. The proof mass is levitated with a DC force generated by interdigitated comb fingers, whereas parallel-plate capacitors are used to provide the negative feedback force. Finally, we exploit the inherent matching of mechanical and electrical parameters between adjacent structures by using a dual-channel architecture, in order to suppress built-in offsets and to minimize long-term drifts.

After describing the modular fabrication process, we describe the sense element design, electronic interface, and digital feedback loop architecture. Experimental results are reported for the open-loop response of one channel to simulate accelerations generated by pulsing feedback and levitation electrodes.

FABRICATION TECHNOLOGY: THE MICS PROCESS

Surface micromachining of polysilicon structures utilizes standard integrated circuit materials and processes, enabling it to be integrated with an MOS fabrication sequence in several ways [5, 6, 13]. By interleaving the two processes -- using MOS steps in the microstructure process and vice versa -- it is possible to develop an optimized, custom process. However, this option is open only to those with control over an IC fabrication line.

In order to minimize the barrier to fabricating polysilicon structures together with CMOS integrated circuits, we have investigated a modular process in which the highly optimized CMOS process is carried out with no modification (making it possible to use a silicon foundry for this part of the process.) In order to raise the temperature ceiling for subsequent sensor processing, we replace aluminum with tungsten for the CMOS interconnect layer and add a TiN/TiSi₂ diffusion barrier at metal/silicon contacts [9, 10]. Low-pressure CVD oxide and nitride films are then deposited to isolate the CMOS from the polysilicon microstructure fabrication steps. The process is called the **Modular Integration of CMOS with micro-Structures**, or MICS.

The initial IC process is a conventional 3 μ m design rule, p-well, double-poly, single metal CMOS technology used at UC Berkeley [14]. Tungsten is selected as the material for metallization among other refractory metals for its close matching in thermal coefficient of expansion to that of silicon and its relatively low resistivity. Since tungsten will react with silicon at the contact at around 600°C, a titanium nitride layer is used as a barrier layer at the contact using a self-aligned process. After the contact opening, titanium is sputtered and rapid-thermal annealed at 600°C in nitrogen ambient for 30 seconds to form a titanium compound layer at the contact. The unreacted titanium layer is removed in a 3:1 NH₄:H₂O₂ solution selectively. The contact is then sintered by RTA at 1000°C in nitrogen for 10 seconds and titanium nitride and titanium silicide is formed at the contact. It has been shown that MOS transistors will not have any noticeable degradation for temperatures below 850°C

with this metallization technique [9]. Thus, polysilicon and nitride films can be deposited without degrading the circuit performance.

Figure 1 shows the cross section of CMOS integrated with surface micromachined structures fabricated in MICS process. After the completion of the CMOS process with tungsten metallization, a 3000Å LTO is deposited and the wafer is then encapsulated with a 2000Å LPCVD silicon nitride layer to protect the CMOS circuitry from subsequent etching steps in the sensor process. This nitride layer also serves as the starting layer of the microstructures. After etching the contacts in the nitride and oxide layer, the first polysilicon layer in the sensor process is deposited and forms the bottom electrodes for sensing and feedback capacitors, as well as the ground plane. This in-situ doped polysilicon layer (3500Å) is also used as the interconnection between sensor and the readout circuits. Note that instead of contacting with the tungsten layer directly, this polysilicon layer is contacted to capacitor poly which is used as a "jumper" between the first polysilicon layer and tungsten. This is to prevent any contamination in the polysilicon tube due to the out-diffusion of the mobile ions in the sputtered tungsten film. A 1 μ m phosphosilicate glass (PSG) layer is then deposited and used as the sacrificial layer. The second in-situ doped polysilicon layer is 2 μ m thick and forms the proof mass, the suspensions, and the levitation comb fingers. Before the etching of the second polysilicon, a 0.5 μ m PSG is deposited. The structural polysilicon is now sandwiched by PSG layers top and bottom so that stress gradient in the polysilicon is minimized after the stress anneal. Polysilicon stress is typically annealed by a 1050°C, an hour furnace anneal [15]. This is not permissible in MICS process since CMOS is completed. Stress anneal using rapid thermal processing is an alternative to the furnace annealing. Experiments have shown that residual stress in the polysilicon structures can be reduced after a 1 minute rapid-thermal annealing at 1000°C in nitrogen ambient. Higher temperature anneal can result better stress release, but blistering of the nitride layer is observed. After the stress anneal, the structural polysilicon is etched and the sacrificial oxide is removed in a buffered HF solution to release the structure from the substrate. The MICS is now completed and the wafers are ready to be diced and packaged.

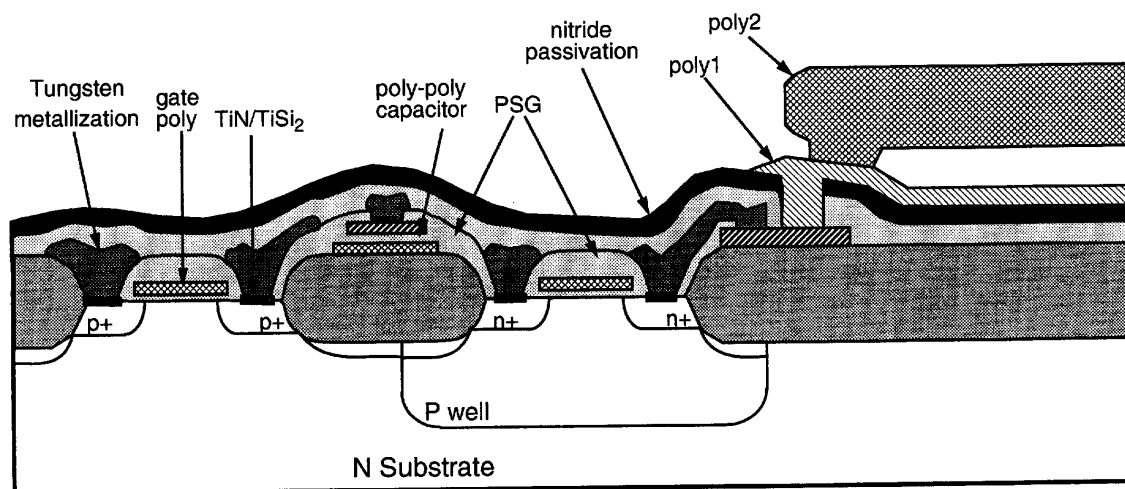


Fig. 1. Cross sectional view of CMOS and microstructure fabricated in MICS process.

SENSOR DESIGN

The capacitive sensing element is fabricated using surface micromachining technique and consists of two layers of in-situ doped polysilicon, shown in Fig. 2. The first polysilicon layer defines the sensing electrode, the feedback electrodes, and the ground plane. The bottom sensing electrode is $100\mu\text{m}$ on each side and is located at the center underneath the proof mass. The feedback electrodes are $25\mu\text{m} \times 25\mu\text{m}$ and are located symmetrically around the sensing electrode to avoid exciting higher-mode vibrations. The ground plane is bootstrapped to minimize the parasitic capacitance on the proof mass. The second polysilicon layer forms the proof mass, the interdigitated fingers for levitating, and the folded suspension. The proof mass is $2\mu\text{m}$ thick and $500\mu\text{m}$ on each side. The gap between the two polysilicon layers is $1\mu\text{m}$. Arrays of etch holes are used on the movable plate to help accelerate the final release etch. The suspension springs are anchored on the first polysilicon layer, which is connected to the readout electronics.

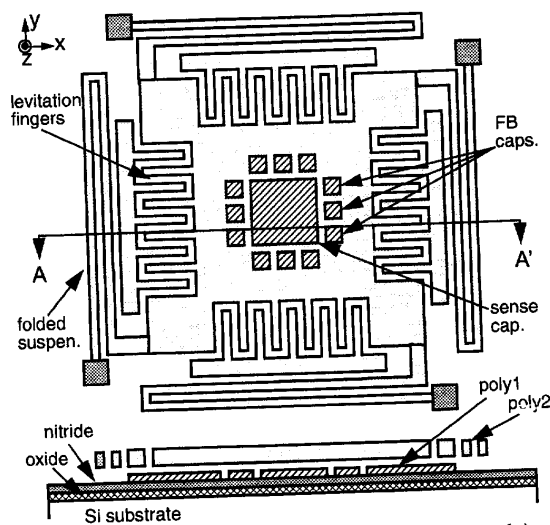


Fig. 2. Plane and cross sectional view (not to scale)

Folded suspensions are employed in the design and are attached to the four corners of the movable plate. Since the sensing axis is perpendicular to the substrate, the spring can be made very compliant by using another thin polysilicon layer for suspension, if sensitivity is the primary consideration. This design also provides low-cross axis sensitivity. The lateral movement of the plate in x-direction is constrained by the top and bottom springs, and the movement in y-direction is constrained by the left and right springs. Analysis shows the cross axis sensitivity is less than 0.1% [16]. The folded design relieves the residual stress in the suspension.

The feedback capacitors are driven by a high frequency, density-modulated pulse train. The pulse density is controlled by the feedback loop and is directly proportional to the acceleration. When there is no acceleration, the pulse train will have 50 percent duty cycle. Since these feedback capacitors generate a pull-down force and there is no feedback capacitors above the proof mass to have pull-up force, interdigitated fingers at the perimeter of the plate are used to generate a constant levitation force [17]. Because of the

presence of the ground plane underneath the fingers, there are more electrical field terminated on the top side of the fingers on the proof mass than that at the bottom side, which results a electrostatic levitation force on the proof mass fingers [17]. This levitation force is balanced by the pull down force from gravity, the sensing electrode, and the feedback electrodes so that the plate is at its neutral position. When acceleration causes the proof mass to move downward, the pulse density on the feedback capacitors reduces so that the pull-down force decreases and the plate moves back up to it is neutral position. Similarly, the pulse density increases when the plate moves upwards due to acceleration. Therefore, the movable plate can be maintained at a stable position.

Since the suspension is very compliant, fuses are used to hold the plate and the suspension in place during the process and are severed by sending a current through after the completion of all processing steps [19]. Figure 3 shows the SEM picture of a corner of the structure: the fuse-held folded suspension, the interdigitated levitation fingers, and the sensing plate with etching holes.

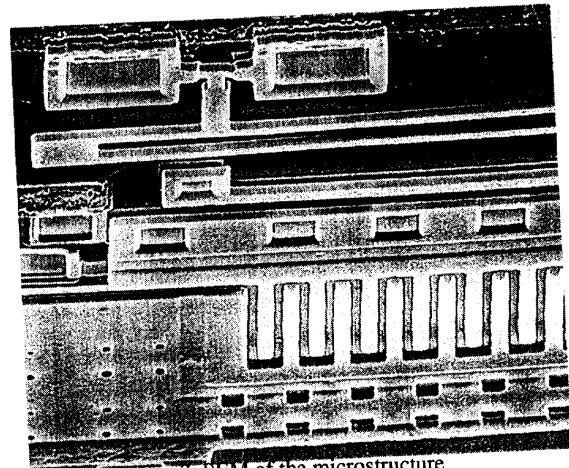


Fig. 3. SEM of the microstructure

SYSTEM ARCHITECTURE

Electrostatic force between the two electrodes of a capacitor is proportional to the square of the applied voltage and is always attractive regardless of the polarity of the voltage. In this design, the feedback capacitors are located underneath the movable plate. If there are feedback electrodes located on both sides of the proof mass symmetrically, the squared term between the feedback voltage and force can be canceled by applying a differential feedback signal with a DC bias to the two electrodes [18]. Since the feedback electrodes are all located underneath the plate, the feedback cannot be linearize by using this technique. If the feedback control is realized in the analog domain, a circuit that has a square-root function has to be designed in the feedback path in order to have a linear system. It is not trivial to design a circuit with that transfer function over a large dynamic range, which can degrade the linearity and the dynamic range of the accelerometer.

Σ - Δ modulation technique is a popular technique to design analog-to-digital converters. By sampling the input signal at frequencies much higher than the Nyquist frequency, the modulator suppresses the quantization noise in the baseband where the input signal is, and pushes the noise to high frequency. Even though a 1-

bit quantizer is used in the modulator, high resolution can be achieved by filtering out the high frequency noise with a decimation filter [11, 12].

There are several advantages to use $\Sigma\Delta$ modulator for feedback control in accelerometers. First, the feedback system has intrinsic linearity because the feedback is a 1-bit signal and the magnitude of the feedback force is proportional to the number of pulses in a given period. This property ensures the accelerometer to have large dynamic range. Second, the requirements for the readout circuits are less demanding because the 1-bit quantizer only concerns the polarity of the signal. This is especially important for integrated accelerometers where the transistor characteristics may be changed due to the sensor process. At last, its digital output makes it easy to interface with rest of the system.

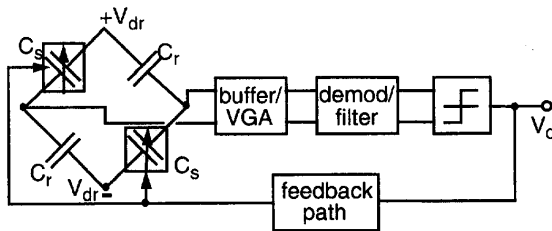


Fig. 4. System block diagram.

The system block diagram of this accelerometer is shown in Fig. 4, where two identical sensing capacitors (C_s 's) and two reference capacitors (C_r 's) of the same value forms the capacitive bridge. Note that two suspended plates are needed to have a full bridge, since the sense capacitor is one-sided. The bridge is driven by a 1MHz square wave. The output of the bridge is linearly proportional to the displacement of the proof mass. Since the displacement is the double integration of the input acceleration, the two integrators in a conventional second-order $\Sigma\Delta$ modulator can be realized with the mechanical proof mass in this electro-mechanical system. The displacement signal is then quantized into a 1-bit signal. A compensation network is placed in the feedback path to insure loop stability and proper noise shaping. It consists of direct feedback and also feedback passing through a differentiator. The feedback signal through the differentiator is equivalently fed back as "electrical damping" on the plate. The output from the feedback path is a 2-bit signal because of the differentiation. The twelve feedback electrodes, shown in Fig. 2, are split into three sets symmetrically. The 2-bit feedback signal determines the number of feedback capacitor sets to be connected to the DC feedback voltage. The force-balanced accelerometer is therefore a second-order electro-mechanical $\Sigma\Delta$ modulator.

Since the sensing capacitance is small, the output voltage of the capacitive bridge can be overwhelmed by the parasitic capacitance and the input capacitance to electronics. A unity gain buffer with low input capacitance is designed to bootstrap the ground plane, shown in Fig. 5. The input capacitance to the buffer consists of gate-to-source capacitance C_{gs} , gate-to-body capacitance C_{gb} , and gate-to-drain capacitance C_{gd} of the input transistor M_1 , where C_{gs} is the main contributor. The C_{gs} and C_{gb} can be minimized by using a source follower at the input. M_2 is a level shifter that insures the out-

put has the same DC level as the input. The C_{ds} capacitance is also bootstrapped using positive feedback. Transistors M_3 and M_4 take the output voltage and drive the drain the input transistor M_1 . The effective input capacitance is 16fF from simulation -- about 5% of the C_{gs} of the input transistor. Since the output of the buffer has the same DC level as the input, we can use it to bootstrap the ground plane without concern about introducing a DC electrostatic force on the plate. The buffer is simulated to have a bandwidth of 50MHz with 1pF capacitive load. A variable gain amplifier (VGA) follows the buffer to amplify the signal with its gain controlled externally.

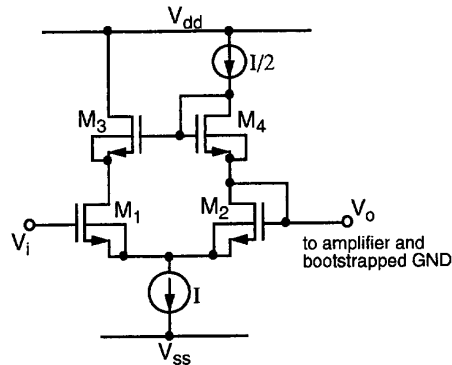


Fig. 5. Unity gain buffer with low input capacitance

Performance of accelerometers can be degraded due to signal feedthrough. In this design, sensing and feedback are operated in two non-overlapping clock phases. During the sensing clock phase, the feedback electrodes are grounded and detection circuits are enabled. During feedback clock phase, the readout circuit is disabled and the feedback electrodes are turned on. Thus, the signal feedthrough is minimized to great extent. Offset voltages from the buffer and the amplifier can also limit the resolution of the accelerometer. Since the offset voltages are at DC and the input signal is modulated to the carrier frequency, chopper stabilization technique can remove the offset with a cosine filter. To minimize the tempera-

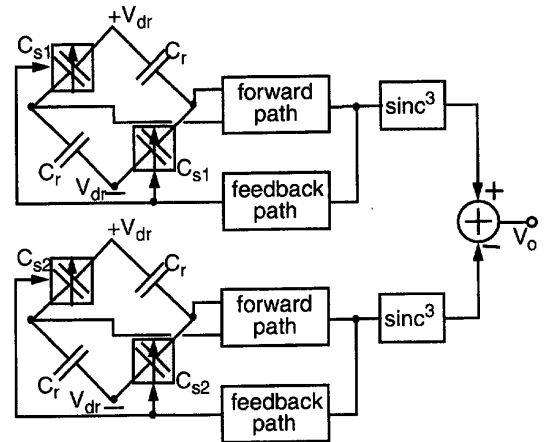


Fig. 6. System Block Diagram of Dual Loop Design

ture sensitivity, potential drift due to the mechanical suspension, and package induced stress effect, two accelerometers are built, where they are exactly identical (Fig. 6) except that the proof mass in one accelerometer (C_{s2} 's) is half of the other one (C_{s1} 's). Since they are built side by side, the temperature, the drift, and package induced stress are common mode signals for the two channels and can be eliminated by subtracting the output in digital domain.

EXPERIMENTAL RESULTS

The accelerometer was fabricated using MICS process in the Berkeley microfabrication facility. The die photo of the device is shown in Fig. 6. The two square structures on the right are the movable plates forming the sensing capacitor C_{s1} 's, and the two on the left are the sensing capacitors with half of the mass (C_{s2} 's). The two structures in the center form the four reference capacitor C_r 's, where two reference capacitors are shared with one top plate. The detection circuit is located in the middle, which includes the low input capacitance buffer, a variable gain amplifier, a demodulator and a cosine filter, a 1-bit quantizer, as well as the bias circuits. The layout is fully symmetrical to ensure that the environmental changes will affect the two accelerometers in the same fashion and are canceled at the output. The feedback control circuit is operated in digital domain and will be constructed off-chip potentially. The chip contains about 500 transistors and the die area is $2.5 \times 5 \text{ mm}^2$.

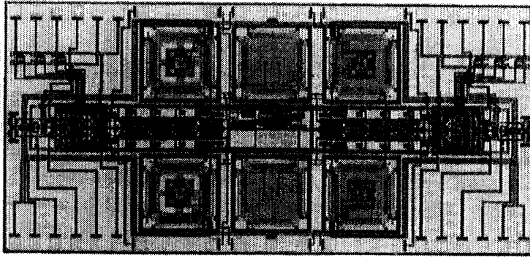


Fig. 7. Die photo of the accelerometer

The circuit performance was evaluated by wafer-level probing. The input buffer is measured to have a gain of 0.9 and a bandwidth around 500kHz which is limited by the parasitic capacitance from the probes and coaxial cables to the measurement instrument. The voltage gain of the variable gain amplifier is controlled externally and can be varied from unity to 40. Its differential output swing is 1.5V.

The accelerometer has been characterized in the open-loop self-testing mode by applying a voltage to the feedback electrodes and the levitation fingers. The suspended plate is moved and we measure the output. Figure 8 show the output voltage versus the levitation voltage at two different driving voltage V_{dr} , 250mV and 150mV. With feedback electrodes grounded, gravity and electrostatic force from sensing electrode pull the proof mass below the equilibrium position giving an offset voltage at the output. As the levitation voltage increases, the levitation force pulls the plate

towards to the equilibrium position and the output voltage decreases.

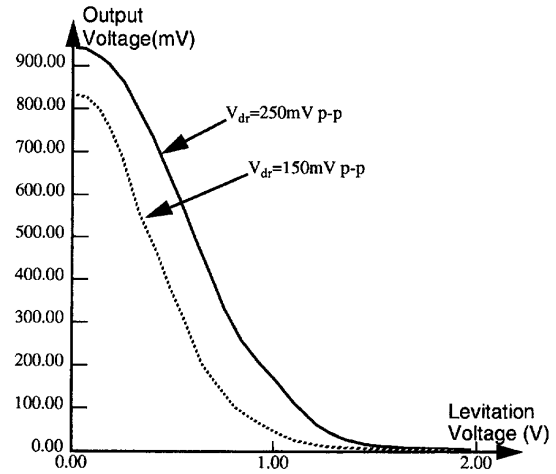


Fig. 8 Output voltage vs. levitation voltage

The open-loop dynamic behavior is also measured by applying a pulse to the feedback or levitation fingers and measuring the transient response at the output. Figure 9 shows a digital scope photo of the envelop of the high frequency sinusoidal output when a 500ms, 0.5V pulse is applied to the levitation fingers. The magnitude of the envelop is the output voltage. By measuring the settling time, the damping factor is derived to be around $1.2 \times 10^{-3} \text{ Nms}^{-1}$, while theoretical calculation predicts the damping factor to be 1 Nms^{-1} [20]. Similar output with opposite sign is also observed when the pulse is applied to the feedback electrodes.

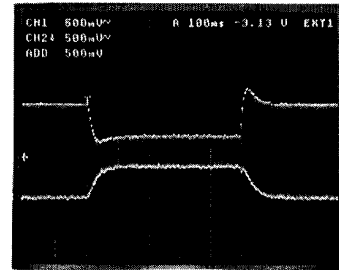


Fig. 9. Transient response of the accelerometer

CONCLUSION

In this paper, we have described a surface micromachined accelerometer with digital electrostatic feedback using Σ - Δ modulation technique, fabricated in a modular CMOS/microstructure process. Detection circuits have been tested successfully. The unity gain buffer with low input capacitance can also be used for other capacitive detection applications. The accelerometer has been characterized in the self-testing mode and has demonstrated the functionality of the device. The accelerometer will be packaged for 2g turnover test.

ACKNOWLEDGMENT

The authors would like to thank Clark Nguyen for his assistance in the fabrication and the staff at Berkeley Microfabrication laboratory. The Berkeley Sensor & Actuator Center (BSAC) is funded by National Science Foundation and a consortium of corporations and government agencies.

This work is performed as part of the PATH Program of the University of California, in cooperation with the State of California, Business and Transportation Agency, Department of Transportation, and the United States Department of Transportation, Federal Highway Administration.

The contents of this report reflect the views of the authors who are responsible for the facts and the accuracy of the data presented herein. The contents do not necessarily reflect the official views or policies of the State of California or the Federal Highway Administration. This report does not constitute a standard, specification, or regulation.

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