COMPOSITION BOOK

WIDE RULED

80 Sheets • 10" x 7 7/8"

HIRAM MCCALL

818 700 7072 2/6/99-12 pages

#26-250

0 74319 26250 3

AMPAD

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Made in Brazil

- Texas state funding letter — CALTIP
- Devny to write letter
- dres up abstract.
- John Morgan Drey done
- start with old proposal and improve upon it.
- X Lin X

818 865 8330 Agoura Hills
20K – 1M Gate VHDL $3995 to $4900
2K – 40K VHDL VERILOG $1995
Design Entry — Alliance Series
Sim
Place and route — FPGA
download

cable to parallel port
to download parts

CADENCE = 1-800-746-6223
SYNOPSIS
MENTOR
New Horizons Distributors
Avnet

- Trip for FT. Eustis & for J.S.C Houston
- slides or Demo?

leave 6:52 10.8 hrs

MONDAY 6/7/99 arrive 8:05

- Win CE is being set up.
- Working with Hp to get scope & voltmeter
- Find flux value
- Get Display s/w from Marty
- Houston PH II get out word Design w MEMS IMU

Put in more detail about electronics piecing together
For Task II. how electronics ball need to see real
implementation. How we make prototype & how it is
Integrated into nav. system. ← get ~~block~~ diagram of Nav system
Take out reference to Mitel chipsets.
Put in more design description
Mike Franck & Johnson SPC Demos the same
More effort into the. Put window CE ref into
beginning.
JSC wants to see Prototype IMU for space applications.
PHSC goal is to flight test the space packaged ~~qualified~~ IMU.
Call it Miniature MEMS IMU.

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- Make subject clear. MEMSIMU for space use.
- Put task 4,5,6 into one task
- Put photo of development setup in Dryden & Johnson PH II proposal
- For presentation we study what system to do in phase I. In phase II we make Asic & repackage
- Show presentation in sync along with slides.
- diagram of NAV system showing MEMS fitting into it
- PH II not doing design but doing repackage and packaging
- Wants product to be ~~product~~ realized.
- More HW SW features to be incorporated
- Due 14TH June - Final
- AGNC unique features
  - hinges design
  - mass distribution for resonance mode
  - resonance mode locking circuitry by unique phase & amplitude for each mode
  - displacement amplitude regulation to reference for SF consistency
  - temperature stabilization - bias & SF
  - Low damping - vacuum moderate package unique Getter placement
  - P.O. sensing circuitry for minimizing bias & S.F. changes.

Leave 7:10 11.1 hrs

Tues 6/8/99 arrive 8:06

Charges to B&P June 15, 16, 17

- RTI - watchout
- Fengs proposal ph II by Tomorrow morning.
- worked on reset of switches and on the SW for the 62.5 HZ processing

Leave 7:12 11.1 hrs

W 6/9/99 Arrive 8:06

Synopsis VHDL tool trial basis

JPL - PH II Fengs proposal

subst twin figures on page 14

- Demo Dos? next Week?

HP

1800 629 - 4444 Denise

X3061

→ scope here today

→ ASIC tools quotes

→ all data needs to be substantiated

- Loaner Sope arrived - Sandy Angus to call back and provide request info on to send back old scope for repair

1800-403-0801

model - 54601A

and serial 3227A07726

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IPR2024-00668
AGNC EX2005

F 9/3/99 IN 7:53
✓ Do WPR
✓ VAL to Get drawings of Gyro off the LASI files
- Ed Prabehalla called and said we can use our amplifier
- James says our Altera FPGA is SRAM, so it needs to be downloaded every time it is powered down.
- file is out for board fabrication
- parts are ordered

leave 6:50 10.9 hrs

MON-Holiday
TUES 9/7/99 arrive 8:13
- An Dong to complete SW document
- final Garry at Avanti Circuits says spacing problems spacing from pads to tracing - 602-866 X122 Garry 7227
✓ Testing and test specs for circuit sub assemblies
✓ Michael Young 4 units wire bond - $900.00 next week completion
✓ new Gyros were sent to ASCI in IR VINE They will be ready next week

- work on the card test specifications and procedures
✓ new Gyros have been sent to ASCI 9/7/99
→ ? find rate Gyro
→ range of voltage
- more description of MEMS device
more " " " " response and range of the voltage signal to the angular rate
- how are the angle and velocity increments correlated.
- beginning to page 15 confirm the description of the process or add to it.
→ be back on Thursday
especially page 12-13 2.1 2.2 2.3 2.4
is it broad enough?

leave 7:05 10.8 hrs

Wed 9/8/99 In 8:02
✓ get James to look at FPGA broad board testing
✓ spice model from VAL and simulation
- check cabling for the Rate table
✓ Michael Young 949 453-8988. HE did receive the parts.

leave 7:16 11.2 hrs

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