DECLARATION OF THE UNIVERSITY OF TEXAS AT AUSTIN LIBRARIES REGARDING THE "LAYOUT MINIMIZATION OF CMOS CELLS" REFERENCE

OPEN RECORDS REQUEST NO. R003570-102022

I, Sean O'Bryan, declare as follows:

1. I am over the age of 18, have never been convicted of a felony or crime of moral turpitude, and am legally competent to make this declaration. I have personal knowledge of the matters stated herein.

2. I am a librarian at University of Texas Libraries ("UT Libraries") located within the University of Texas, Austin, TX.

3. I have been employed by UT Libraries for 21 years.

4. I familiar with the routine record-keeping practices of UT Libraries.

5. The UT Libraries' records that are regularly maintained in the course of its operation reflect that "Layout Minimization of CMOS Cells" by Robert L. Maziasz and John P. Hayes is in the UT Libraries' collection. According to our records, this item was catalogued on July 16, 1998.

6. A true and accurate copy of the cataloging record for "Layout Minimization of CMOS Cells" is attached as Exhibit A.

7. At the time of the acquisition of "Layout Minimization of CMOS Cells", the UT Libraries typically made newly catalogued items available to the public within 3 business days of cataloging.

8. I have reviewed the portions of "Layout Minimization of CMOS Cells" attached as Exhibit B and they reflect a true and accurate copy of the corresponding portions of the item as it exists in the UT Libraries.

* Note: In January 2020, UT Libraries completed a migration to/implementation of a new Library Services Platform (ExLibris' Alma Library Services Platform) as our catalog of record. Prior to January 2020, Innovative Interfaces' Sierra ILS was employed as our catalog. Prior to 2007, UT Libraries employed a locally developed catalog system (UTCAT/UTNetCat). All item accession data prior to

2020 required migration to the new Alma platform from one or sometimes both previous systems and was required to be archived in available fields in the new Alma system. The “catalog date” for records from the UTCAT/UTNetCat system was archived in Alma at the item-level as “UT DATE:” in Statistics note 1.

I, Sean O’Bryan, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the Unites States Code.

Executed on October 28, 2022.

Sean O’Bryan
Assistant Director of Access
University of Texas Libraries

Exhibit A

LDR	01602pam a2200373 a 4500
001	991024329859706011
005	20200731162159.0
008	910830s1992 maua b 001 0 eng
010	__ |a 91034031
015	__ |a GB92-695
020	__ |a 0792391829 (alk. paper)
035	__ |a (IXA)b44602558-01utau_inst
035	__ |a (OCoLC)24429749 |9 ExL
040	__ |a DLC |c DLC |d UKM |d IXA
049	__ |a IXAm
050	00 |a TK7871.99.M44 |b M33 1992
082	00 |a 621.381/52 |2 20
100	1_ |a Maziasz, Robert L., |d 1952-
245	10 |a **Layout minimization of CMOS** cells / |c by Robert L. Maziasz and John P. Hayes.
260	__ |a Boston : |b Kluwer Academic Publishers, |c c1992.
300	__ |a xii, 169 p. : |b ill. ; |c 25 cm.
490	1_ |a Kluwer international series in engineering and computer science ; |v SECS 160
504	__ |a Includes bibliographical references (p. 157-165) and index.
583	__ |a digitized |z temporary access |f HathiTrust |u https://www.hathitrust.org/digital_library
650	_0 |a Metal oxide semiconductors, Complementary |x Design and construction |x Data processing.
650	_0 |a Computer-aided design.
653	0_ |a Integrated circuits |a Design |a Use **of** |a Computers
700	1_ |a Hayes, John P. |q (John Patrick), |d 1944-
830	_0 |a Kluwer international series in engineering and computer science ; |v SECS 160.
907	__ |a .b44602558 |b 07-23-12 |c 03-09-07

915	__ |a (TxU)9369237
915	__ |a 24429749
945	__ |a TK 7871.99 M44 M33 1992 |e - - |g 1 |i 059173006048988 |j 0 |l sfen |o - |p $0.00 |q - |r - |s - |t 10 |u 52 |v 0 |w 0 |x 0 |y .i153911219 |z 03-09-07
998	__ |a sfen |b 03-01-07 |c m |d a |e - |f eng |g mau |h 0 |i 1

Functional Notes

Public note	-
Fulfillment note	-

Internal Notes

Internal note 1	-
Internal note 2	-
Internal note 3	CIRC NOTE: 08-27-02 19:06 | ITEM FIELD: 050 TK 7871.99 M44 M33 1992 059173006048988 eng 08-27-02 19:06 52 0 10 1998-07-16

Statistics Notes

Statistics note 1	UT DATE: 1998-07-16
Statistics note 2	-
Statistics note 3	-

Layout minimization of CMOS cells / by Robert L. Maziasz and John P. Hayes.
Maziasz, Robert L., 1952-
Kluwer Academic Publishers, Boston : c1992.
[0792391829 (alk. paper)]

Holdings
Library Storage Facility: sfen Library Storage Facility Engineering Library; TK 7871.99 M44 M33 1992

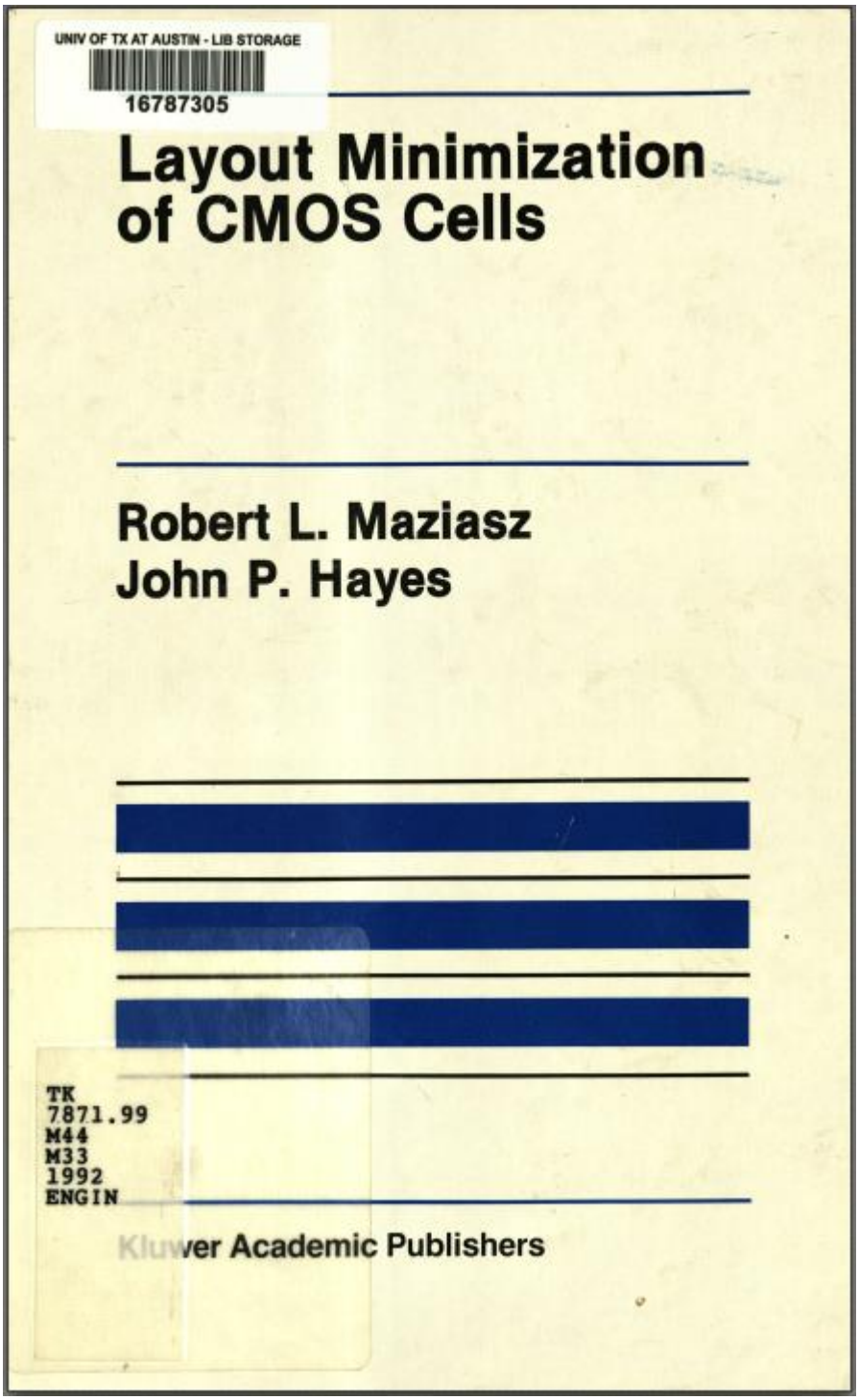
Holdings ID
22306569320006011

View all holdings

Barcode
059173006048988

Item ID
23306569290006011

Exhibit B


UNIV OF TX AT AUSTIN - LIB STORAGE
16787305
Layout Minimization of CMOS Cells
Robert L. Maziasz
John P. Hayes
TK
7871.99
M44
M33
1992
ENGIN
Kluwer Academic Publishers

LAYOUT MINIMIZATION OF CMOS CELLS

by

Robert L. Maziasz
and
John P. Hayes

The University of Michigan

Kluwer Academic Publishers
Boston/Dordrecht/London

Distributors for North America:
Kluwer Academic Publishers
101 Philip Drive
Assinippi Park
Norwell, Massachusetts 02061 USA

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Distribution Centre
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3300 AH Dordrecht, THE NETHERLANDS

Library of Congress Cataloging-in-Publication Data

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Layout minimization of CMOS cells / by Robert L. Maziasz and John P. Hayes.
p. cm. -- (The Kluwer international series in engineering and computer science : SECS 160)
Includes bibliographical references and index.
ISBN 0-7923-9182-9 (alk. paper)
1. Metal oxide semiconductors, Complementary--Design and construction--Data processing. 2. Computer-aided design.
I. Hayes, John P. (John Patrick), 1944- . II. Title.
III. Series.
TK7871.99.M44M33 1992
621.381'52--dc20 91-34031
CIP

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