DECLARATION OF MARTIN L. KNOTT

Declaration of Martin L. Knott Regarding
Authentication and Public Accessibility of Publication

I, Martin L. Knott, declare as follows:

1. I am a librarian and Metadata and Linked Data Strategist within the University of Michigan Library's Technical Services Department, located at 913 S. University, Ann Arbor, MI 48109-1190. I hold a Master of Science in Information from the University of Michigan, where I studied library and information science. I joined the University Library in August of 1992. Through the course of my employment and based on the University Library's business records, I have personal knowledge of the University Library's normal business practices, including during the time period starting in the early 2000s. The University Library's normal business practices, which follows standard library practices, are described in further detail below.

2. This Declaration relates to the dates of receipt and public availability of the following:

> **Rabaey, J. M., Chandrakasan, A. P., & Nikolić, B. (2003). *Digital integrated circuits : a design perspective*. (2nd ed.). Upper Saddle River, N.J. : Pearson Education.**

3. *Standard operating procedures for materials at the University of Michigan Libraries*. During the early 2000s and through the present, when a journal volume or other publication was or is received by the University Library, it would be checked in, inscribed with the date of receipt, added to library holdings records, and made available to library patrons or visitors (*i.e.*, the general public) for review, photocopying, and/or

borrowing as soon after its arrival as possible. This procedure normally took a few days or as long as 4 months when there were high numbers of new materials in the workflow.

4. The image attached to this Declaration is a true and accurate copy of ***Digital integrated circuits*** with a University Library date inscription of January 20, 2003 from the University of Michigan Library collection. The date inscription on the page following the title page indicates that ***Digital integrated circuits*** was received by the University of Michigan Library Technical Services located in the Harlan Hatcher Graduate Library on January 20, 2003. ***Digital integrated circuits*** was purchased for and transported to the Media Union Art, Architecture & Engineering Library, one of several University of Michigan campus libraries, for user access.

5. Based on the information in the attached image, it is clear that ***Digital integrated circuits*** was received by the Art, Architecture & Engineering Library on January 20, 2003, and was catalogued and available to the public within a few days or at most 4 months later, after which the public could search for it by at least subject matter, title, author, year, and/or topic in the University Library's online catalog.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Declaration of Martin L. Knott Regarding
Authentication and Public Accessibility of Publication

Date: March 19, 2019



Martin L. Knott
Metadata and Linked Data Strategist

University of Michigan Library
913 S. University
Ann Arbor, MI 48109-1190

NOTICE CONCERNING COPYRIGHT RESTRICTIONS

The material copied here may be protected by copyright law in the United States and/or in other jurisdictions. This copy was made in compliance with U.S. copyright law and is provided to you for the purposes of private study, scholarship, or research.

If you use the copy for a different purpose, such as posting on a course website, the copyright analysis that supported making the copy does not apply. It is your responsibility to address copyright for any other uses. For assistance, you may wish to consult the library's guides to Copyright Basics and Copyright and Course Websites. You can also contact the University of Michigan Library Copyright Office at copyright@umich.edu.

Prentice Hall Electronics and VLSI Series

Charles S. Sodini, Series Editor

LEE, SHUR, FIELDLY, YTTERDAL *Semiconductor Devices Modeling for VLSI*

LEUNG *VLSI for Wireless Communications*

PLUMMER, DEAL, GRIFFIN *Silicon VLSI Technology: Fundamentals, Practice, and Modeling*

RABAEY, CHANDRAKASAN, NIKOLIĆ *Digital Integrated Circuits: A Design Perspective*, Second Edition

DIGITAL INTEGRATED CIRCUITS

A DESIGN PERSPECTIVE
SECOND EDITION

JAN M. RABAEY
ANANTHA CHANDRAKASAN
BORIVOJE NIKOLIĆ

PRENTICE HALL ELECTRONICS AND VLSI SERIES
CHARLES G. SODINI, SERIES EDITOR



Pearson Education, Inc.
Upper Saddle River, New Jersey 07458

Uma Patel
TK
7874.65
.R33
2003
V6/K5

Library of Congress Cataloging-in-Publication Data on file.

Vice President and Editorial Director, ECS: *Marcia J. Horton*
Publisher: *Tom Robbins*
Editorial Assistant: *Eric Van Ostenbridge*
Vice President and Director of Production and Manufacturing, ESM: *David W. Riccardi*
Executive Managing Editor: *Vince O'Brien*
Managing Editor: *David A. George*
Production Editor: *Daniel Sandin*
Director of Creative Services: *Paul Belfanti*
Creative Director: *Carole Anson*
Art and Cover Director: *Jayne Conte*
Art Editor: *Greg Dulles*
Manufacturing Manager: *Trudy Pisciotti*
Manufacturing Buyer: *Lisa McDowell*
Marketing Manager: *Holly Stark*

About the Cover: Detail of "Wet Orange," by Joan Mitchell (American, 1925–1992). Oil on canvas, 112 × 245 in. (284.5 × 622.3 cm). Carnegie Museum of Art, Pittsburgh, PA. Gift of Kaufmann's Department Store and the National Endowment for the Arts, 74.11. Photograph by Peter Harholdt, 1995.



© 2003, 1996 by Pearson Education, Inc.
Pearson Education, Inc.
Upper Saddle River, NJ 07458

The author and publisher of this book have used their best efforts in preparing this book. These efforts include the development, research, and testing of the theories and programs to determine their effectiveness. The author and publisher shall not be liable in any event for incidental and consequential damages in connection with, or arising out of, the furnishing, performance, or use of these programs.

All rights reserved. No part of this book may be reproduced, in any form or by any means, without permission in writing from the publisher.

Printed in the United States of America

10 9 8 7 6 5 4 3 2 1

ISBN 0-13-597444-5

Pearson Education Ltd., *London*
Pearson Education Australia Pty, Ltd., *Sydney*
Pearson Education Singapore, Pte. Ltd.
Pearson Education North Asia Ltd., *Hong Kong*
Pearson Education Canada Inc., *Toronto*
Pearson Educación de Mexico, S.A. de C.V.
Pearson Education—Japan, *Tokyo*
Pearson Education Malaysia, Pte. Ltd.
Pearson Education Inc., *Upper Saddle River, New Jersey*

Ummvlbks
u1830775
e/tr
1/20/03

To Kathelijn, Karthiyayani, Krithivasan, and our Parents

"Qu'est-ce que l'homme dans la nature?
Un néant a l'égard de l'infini,
un tout al l'égard du néant,
un milieu entre rien et tout."

"What is man in nature?
Nothing in relation to the infinite,
everything in relation to nothing,
a mean between nothing and everything."

Blaise Pascal, *Pensées*, n. 4, 1670.

Contents

	Preface		**vii**
Part 1	**The Fabrics**		**1**
Chapter 1	**Introduction**		**3**
	1.1	A Historical Perspective	4
	1.2	Issues in Digital Integrated Circuit Design	6
	1.3	Quality Metrics of a Digital Design	15
		1.3.1 Cost of an Integrated Circuit	16
		1.3.2 Functionality and Robustness	18
		1.3.3 Performance	27
		1.3.4 Power and Energy Consumption	30
	1.4	Summary	31
	1.5	To Probe Further	31
		Reference Books	32
		References	33
Chapter 2	**The Manufacturing Process**		**35**
	2.1	Introduction	36
	2.2	Manufacturing CMOS Integrated Circuits	36
		2.2.1 The Silicon Wafer	37
		2.2.2 Photolithography	37
		2.2.3 Some Recurring Process Steps	41
		2.2.4 Simplified CMOS Process Flow	42
	2.3	Design Rules—The Contract between Designer and Process Engineer	47
	2.4	Packaging Integrated Circuits	51
		2.4.1 Package Materials	52
		2.4.2 Interconnect Levels	53
		2.4.3 Thermal Considerations in Packaging	59
	2.5	Perspective—Trends in Process Technology	61
		2.5.1 Short-Term Developments	61
		2.5.2 In the Longer Term	63
	2.6	Summary	64

2.7 To Probe Further 64
References 64

Design Methodology Insert A **IC LAYOUT** **67**
A.1 To Probe Further 71
References 71

Chapter 3 **The Devices** **73**
3.1 Introduction 74
3.2 The Diode 74
3.2.1 A First Glance at the Diode—The Depletion Region 75
3.2.2 Static Behavior 77
3.2.3 Dynamic, or Transient, Behavior 80
3.2.4 The Actual Diode—Secondary Effects 84
3.2.5 The SPICE Diode Model 85
3.3 The MOS(FET) Transistor 87
3.3.1 A First Glance at the Device 87
3.3.2 The MOS Transistor under Static Conditions 88
3.3.3 The Actual MOS Transistor—Some Secondary Effects 114
3.3.4 SPICE Models for the MOS Transistor 117
3.4 A Word on Process Variations 120
3.5 Perspective—Technology Scaling 122
3.6 Summary 128
3.7 To Probe Further 129
References 130

Design Methodology Insert B **Circuit Simulation** **131**
References 134

Chapter 4 **The Wire** **135**
4.1 Introduction 136
4.2 A First Glance 136
4.3 Interconnect Parameters—Capacitance, Resistance, and Inductance 138
4.3.1 Capacitance 138
4.3.2 Resistance 144
4.3.3 Inductance 148
4.4 Electrical Wire Models 150
4.4.1 The Ideal Wire 151
4.4.2 The Lumped Model 151
4.4.3 The Lumped *RC* Model 152
4.4.4 The Distributed *rc* Line 156
4.4.5 The Transmission Line 159

4.5 SPICE Wire Models 170
4.5.1 Distributed *rc* Lines in SPICE 170
4.5.2 Transmission Line Models in SPICE 170
4.5.3 Perspective: A Look into the Future 171
4.6 Summary 174
4.7 To Probe Further 174
References 174

Part 2 A Circuit Perspective 177

Chapter 5 The CMOS Inverter 179
5.1 Introduction 180
5.2 The Static CMOS Inverter—An Intuitive Perspective 180
5.3 Evaluating the Robustness of the CMOS Inverter: The Static Behavior 184
5.3.1 Switching Threshold 185
5.3.2 Noise Margins 188
5.3.3 Robustness Revisited 191
5.4 Performance of CMOS Inverter: The Dynamic Behavior 193
5.4.1 Computing the Capacitances 194
5.4.2 Propagation Delay: First-Order Analysis 199
5.4.3 Propagation Delay from a Design Perspective 203
5.5 Power, Energy, and Energy Delay 213
5.5.1 Dynamic Power Consumption 214
5.5.2 Static Consumption 223
5.5.3 Putting It All Together 225
5.5.4 Analyzing Power Consumption Using SPICE 227
5.6 Perspective: Technology Scaling and its Impact on the Inverter Metrics 229
5.7 Summary 232
5.8 To Probe Further 233
References 233

Chapter 6 Designing Combinational Logic Gates in CMOS 235
6.1 Introduction 236
6.2 Static CMOS Design 236
6.2.1 Complementary CMOS 237
6.2.2 Ratioed Logic 263
6.2.3 Pass-Transistor Logic 269
6.3 Dynamic CMOS Design 284
6.3.1 Dynamic Logic: Basic Principles 284
6.3.2 Speed and Power Dissipation of Dynamic Logic 287

6.3.3 Signal Integrity Issues in Dynamic Design 290
6.3.4 Cascading Dynamic Gates 295
6.4 Perspectives 303
6.4.1 How to Choose a Logic Style? 303
6.4.2 Designing Logic for Reduced Supply Voltages 303
6.5 Summary 306
6.6 To Probe Further 307
References 308

Design Methodology Insert C **How to Simulate Complex Logic Circuits** **309**
C.1 Representing Digital Data as a Continuous Entity 310
C.2 Representing Data as a Discrete Entity 310
C.3 Using Higher-Level Data Models 315
References 317

Design Methodology Insert D **Layout Techniques for Complex Gates** **319**

Chapter 7 **Designing Sequential Logic Circuits** **325**
7.1 Introduction 326
7.1.1 Timing Metrics for Sequential Circuits 327
7.1.2 Classification of Memory Elements 328
7.2 Static Latches and Registers 330
7.2.1 The Bistability Principle 330
7.2.2 Multiplexer-Based Latches 332
7.2.3 Master-Slave Edge-Triggered Register 333
7.2.4 Low-Voltage Static Latches 339
7.2.5 Static SR Flip-Flops—Writing Data by Pure Force 341
7.3 Dynamic Latches and Registers 344
7.3.1 Dynamic Transmission-Gate Edge-triggered Registers 344
7.3.2 C^2MOS—A Clock-Skew Insensitive Approach 346
7.3.3 True Single-Phase Clocked Register (TSPCR) 350
7.4 Alternative Register Styles* 354
7.4.1 Pulse Registers 354
7.4.2 Sense-Amplifier-Based Registers 356
7.5 Pipelining: An Approach to Optimize Sequential Circuits 358
7.5.1 Latch- versus Register-Based Pipelines 360
7.5.2 NORA-CMOS—A Logic Style for Pipelined Structures 361
7.6 Nonbistable Sequential Circuits 364
7.6.1 The Schmitt Trigger 364
7.6.2 Monostable Sequential Circuits 367
7.6.3 Astable Circuits 368
7.7 Perspective: Choosing a Clocking Strategy 370
7.8 Summary 371

7.9 To Probe Further 372
References 372

Part 3 **A System Perspective** **375**

Chapter 8 **Implementation Strategies for Digital ICS** **377**
8.1 Introduction 378
8.2 From Custom to Semicustom and Structured-Array Design Approaches 382
8.3 Custom Circuit Design 383
8.4 Cell-Based Design Methodology 384
8.4.1 Standard Cell 385
8.4.2 Compiled Cells 390
8.4.3 Macrocells, Megacells and Intellectual Property 392
8.4.4 Semicustom Design Flow 396
8.5 Array-Based Implementation Approaches 399
8.5.1 Prediffused (or Mask-Programmable) Arrays 399
8.5.2 Prewired Arrays 404
8.6 Perspective—The Implementation Platform of the Future 420
8.7 Summary 423
8.8 To Probe Further 423
References 424

Design Methodology Insert E **Characterizing Logic and Sequential Cells** **427**
References 434

Design Methodology Insert F **Design Synthesis** **435**
References 443

Chapter 9 **Coping with Interconnect** **445**
9.1 Introduction 446
9.2 Capacitive Parasitics 446
9.2.1 Capacitance and Reliability—Cross Talk 446
9.2.2 Capacitance and Performance in CMOS 449
9.3 Resistive Parasitics 460
9.3.1 Resistance and Reliability—Ohmic Voltage Drop 460
9.3.2 Electromigration 462
9.3.3 Resistance and Performance—*RC* Delay 464
9.4 Inductive Parasitics* 469
9.4.1 Inductance and Reliability— Voltage Drop 469
9.4.2 Inductance and Performance—Transmission-line Effects 475
9.5 Advanced Interconnect Techniques 480

9.5.1 Reduced-Swing Circuits 480
9.5.2 Current-Mode Transmission Techniques 486
9.6 Perspective: Networks-on-a-Chip 487
9.7 Summary 488
9.8 To Probe Further 489
References 489

Chapter 10 **Timing Issues in Digital Circuits** **491**
10.1 Introduction 492
10.2 Timing Classification of Digital Systems 492
10.2.1 Synchronous Interconnect 492
10.2.2 Mesochronous interconnect 493
10.2.3 Plesiochronous Interconnect 493
10.2.4 Asynchronous Interconnect 494
10.3 Synchronous Design—An In-depth Perspective 495
10.3.1 Synchronous Timing Basics 495
10.3.2 Sources of Skew and Jitter 502
10.3.3 Clock-Distribution Techniques 508
10.3.4 Latch-Based Clocking* 516
10.4 Self-Timed Circuit Design* 519
10.4.1 Self-Timed Logic—An Asynchronous Technique 519
10.4.2 Completion-Signal Generation 522
10.4.3 Self-Timed Signaling 526
10.4.4 Practical Examples of Self-Timed Logic 531
10.5 Synchronizers and Arbiters* 534
10.5.1 Synchronizers—Concept and Implementation 534
10.5.2 Arbiters 538
10.6 Clock Synthesis and Synchronization Using a Phase-Locked Loop* 539
10.6.1 Basic Concept 540
10.6.2 Building Blocks of a PLL 542
10.7 Future Directions and Perspectives 546
10.7.1 Distributed Clocking Using DLLs 546
10.7.2 Optical Clock Distribution 548
10.7.3 Synchronous versus Asynchronous Design 549
10.8 Summary 550
10.9 To Probe Further 551
References 551

Design Methodology Insert G **Design Verification** **553**
References 557

Chapter 11 **Designing Arithmetic Building Blocks** **559**
11.1 Introduction 560
11.2 Datapaths in Digital Processor Architectures 560
11.3 The Adder 561
11.3.1 The Binary Adder: Definitions 561
11.3.2 The Full Adder: Circuit Design Considerations 564
11.3.3 The Binary Adder: Logic Design Considerations 571
11.4 The Multiplier 586
11.4.1 The Multiplier: Definitions 586
11.4.2 Partial-Product Generation 587
11.4.3 Partial-Product Accumulation 589
11.4.4 Final Addition 593
11.4.5 Multiplier Summary 594
11.5 The Shifter 594
11.5.1 Barrel Shifter 595
11.5.2 Logarithmic Shifter 596
11.6 Other Arithmetic Operators 596
11.7 Power and Speed Trade-offs in Datapath Structures* 600
11.7.1 Design Time Power-Reduction Techniques 601
11.7.2 Run-Time Power Management 611
11.7.3 Reducing the Power in Standby (or Sleep) Mode 617
11.8 Perspective: Design as a Trade-off 618
11.9 Summary 619
11.10 To Probe Further 620
References 621

Chapter 12 **Designing Memory and Array Structures** **623**
12.1 Introduction 624
12.1.1 Memory Classification 625
12.1.2 Memory Architectures and Building Blocks 627
12.2 The Memory Core 634
12.2.1 Read-Only Memories 634
12.2.2 Nonvolatile Read-Write Memories 647
12.2.3 Read-Write Memories (RAM) 657
12.2.4 Contents-Addressable or Associative Memory (CAM) 670
12.3 Memory Peripheral Circuitry* 672
12.3.1 The Address Decoders 672
12.3.2 Sense Amplifiers 679
12.3.3 Voltage References 686
12.3.4 Drivers/Buffers 689
12.3.5 Timing and Control 689

12.4 Memory Reliability and Yield* 693
12.4.1 Signal-to-Noise Ratio 693
12.4.2 Memory Yield 698
12.5 Power Dissipation in Memories* 701
12.5.1 Sources of Power Dissipation in Memories 701
12.5.2 Partitioning of the Memory 702
12.5.3 Addressing the Active Power Dissipation 702
12.5.4 Data-Retention Dissipation 704
12.5.5 Summary 707
12.6 Case Studies in Memory Design 707
12.6.1 The Programmable Logic Array (PLA) 707
12.6.2 A 4-Mbit SRAM 710
12.6.3 A 1-Gbit NAND Flash Memory 712
12.7 Perspective: Semiconductor Memory Trends and Evolutions 714
12.8 Summary 716
12.9 To Probe Further 717
References 718

Design Methodology Insert H **Validation and Test of Manufactured Circuits** **721**

H.1 Introduction 721
H.2 Test Procedure 722
H.3 Design for Testability 723
H.3.1 Issues in Design for Testability 723
H.3.2 Ad Hoc Testing 725
H.3.3 Scan-Based Test 726
H.3.4 Boundary-Scan Design 729
H.3.5 Built-in Self-Test (BIST) 730
H.4 Test-Pattern Generation 734
H.4.1 Fault Models 734
H.4.2 Automatic Test-Pattern Generation (ATPG) 736
H.4.3 Fault Simulation 737
H.5 To Probe Further 737
References 737

Problem Solutions **739**

Index **745**