EXHIBIT 12

Exhibit D-1 to Greenthread's Preliminary Infringement Contentions (4/29/2022)

U.S. Patent No. 10,510,842	Accused Products
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Sony Accused Products include a semiconductor device. Sony provides CMOS image sensors, and the Dell-Sony Accused Products include Sony CMOS image sensors, each of which is a semiconductor device. Sony Develops World's First[*1] Stacked CMOS Image Sensor Technology with 2-Layer Transistor Pixel Widens Dynamic Range and Reduces Noise by Approximately Doubling[*2] Saturation Signal Level[*3] Sony Semiconductor Solutions Corporation *See* https://www.sony-semicon.co.jp/e/news/2021/2021121601.html As an example, the Sony 12 MP 1.0 µm Pixel Pitch, Stacked Back-Illumination CMOS Image Sensor is found in an Apple iPhone 11, and upon information and belief, this image sensor has similar components and functionality as the Sony CMOS image sensor in the Dell-Sony Accused Products. Usage of a Sony CMOS image sensor in Dell products is shown below, for example: Dell UltraSharp 4K Webcam ★★★★½ 4.3 (400) **Tech Specs** Quick Specs **Resolution / FPS** 4K UHD / 24, 30 Full HD / 24, 30, 60 HD / 24, 30, 60 **Megapixel** 8.3MP **Sensor Brand** Large Sony STARVIS™ CMOS sensor **Field of View (FOV)** 65, 78, 90 degree

U.S. Patent No. 10,510,842	Accused Products
	See https://deals.dell.com/en-us/productdetail/dtvv This representative Sony image sensor has been analyzed via tear-down, as explained below. The above Sony image sensor is discussed in this claim chart and other infringement contention claim charts (e.g., Exhibits D-2 through D-6) as an example of a Sony image sensor used in Dell-Sony Accused products. Upon information and belief, such a Sony image sensor is representative of Sony image sensors used in the Dell-Sony Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other Sony image sensors used in Dell-Sony Accused Products would have similarly been advantageously designed to move carriers and achieve the performance enhancements described and claimed in the '842 patent (and the other asserted patents). For example, other Sony image sensors would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '842 patent (and the other asserted patents). Therefore, upon information and belief, other Sony image sensors used in Dell-Sony Accused Products contain similar features as the Sony 12 MP 1.0 µm Pixel Pitch, Stacked Back-Illumination CMOS Image Sensor, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Dell-Sony Accused Products meet this limitation. For example, the Sony CMOS image sensor discussed above for Claim 1, Preamble, was imaged using scanning electron microscopy (SEM) and scanning capacitance microscopy (SCM), at the cross-section indicated below:

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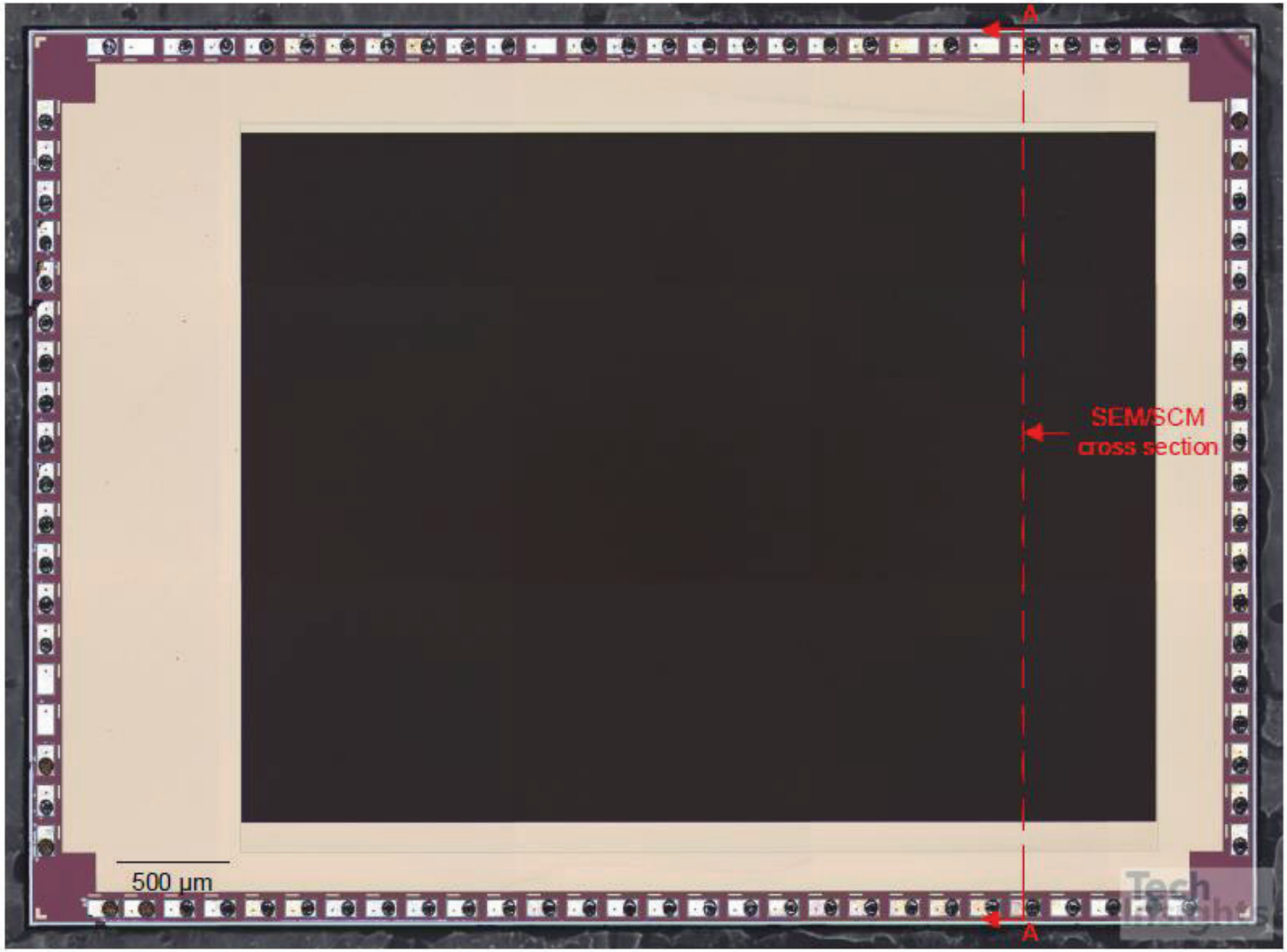
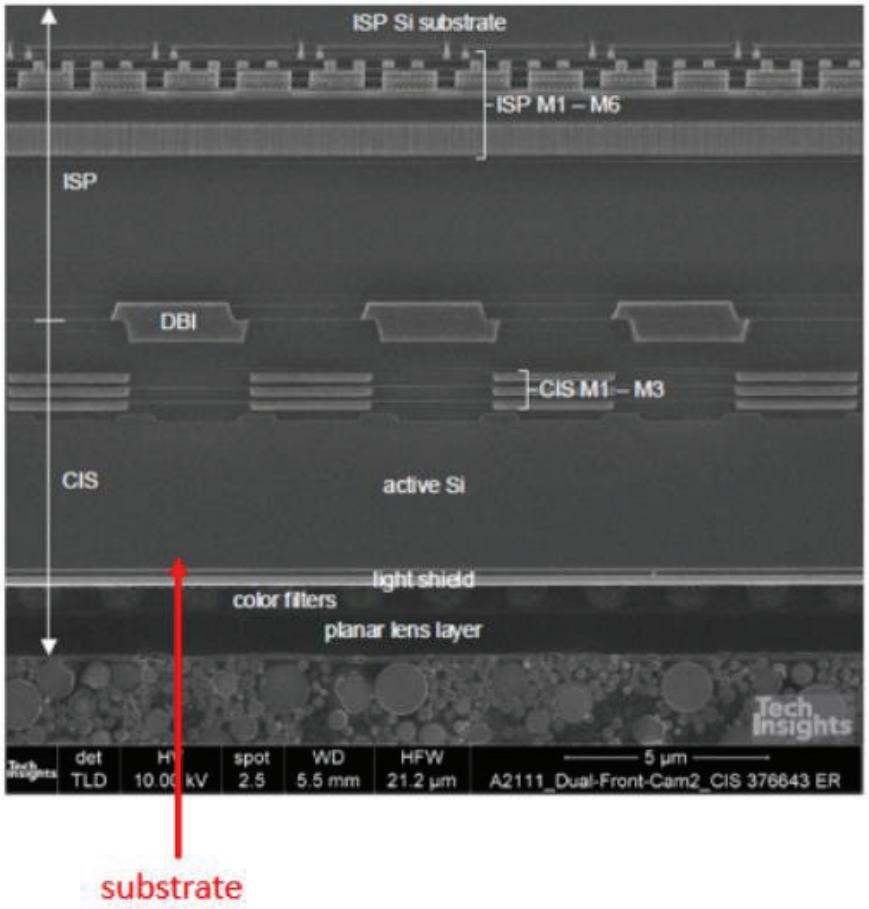
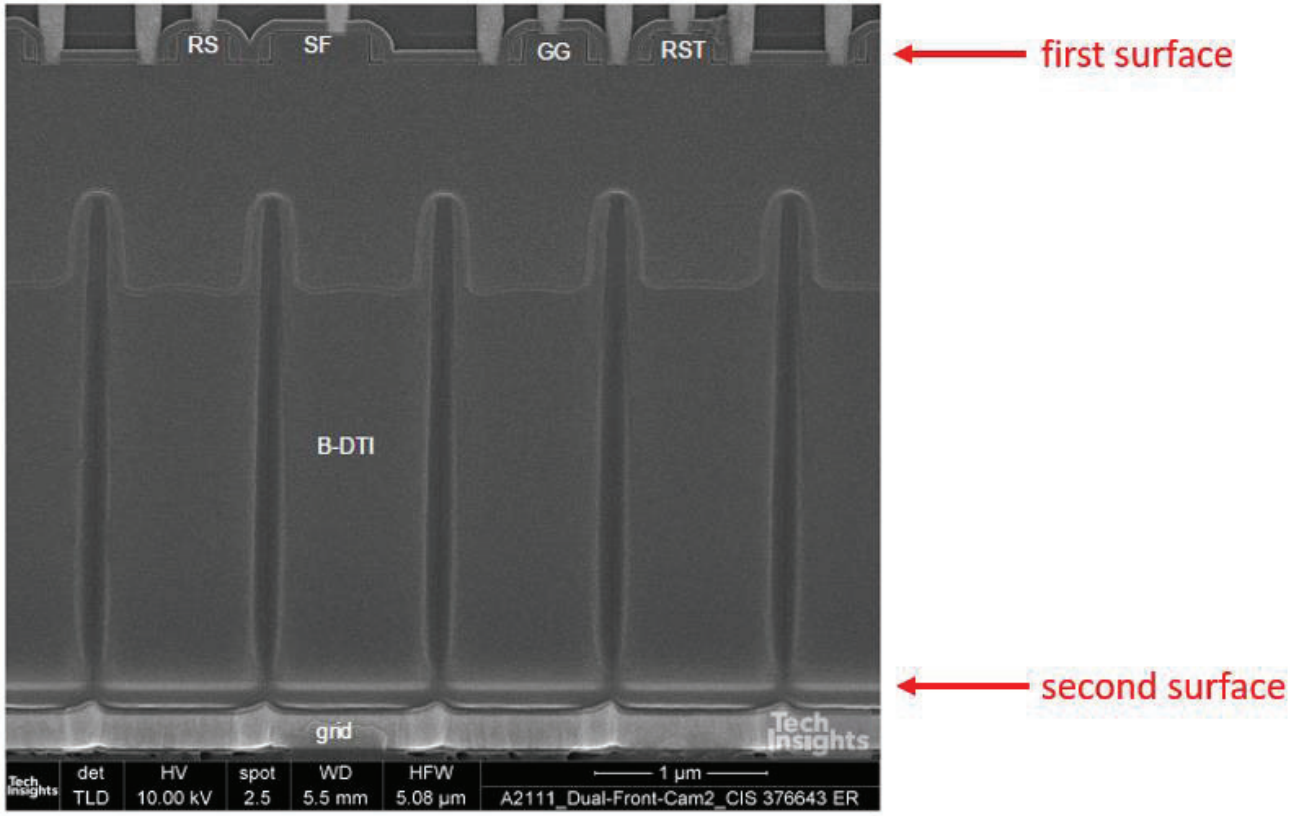
U.S. Patent No. 10,510,842	Accused Products
	 The SEM cross-sectional image below shows the image signal processor (ISP) / CMOS image sensor (CIS) die stack in the periphery region, with a direct bond interconnect (DBI) connecting the two wafers corresponding to the ISP and CIS, respectively:

Exhibit D-1 to Greenthread's Preliminary Infringement Contentions (4/29/2022)

U.S. Patent No. 10,510,842	Accused Products
	 The substrate has first and second surfaces, as shown in the following SEM cross-sectional image taken at the red dashed line labeled "A" and "SEM/SCM cross-section" in the first figure above:

U.S. Patent No. 10,510,842	Accused Products
	 Secondary ion mass spectroscopy (SIMS) was performed to analyze doping profiles. For example, a SIMS sample was used as shown below, with the location of SIMS craters annotated:

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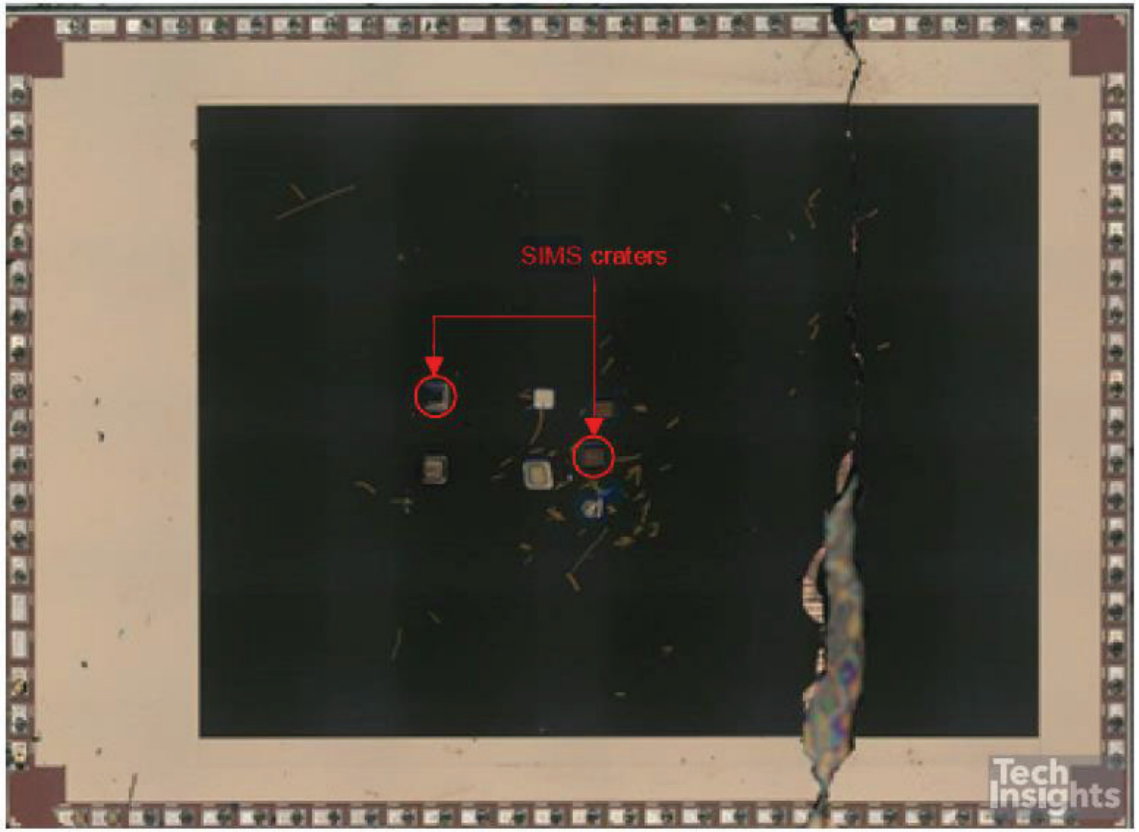
U.S. Patent No. 10,510,842	Accused Products
	 The sample was prepared by removing the back layers down to the back of the active silicon. The SIMS crater for boron (B) analysis is 100 × 100 µm, and 80 × 80 µm for the remaining elements shown in the legend at the right side of the below graph.

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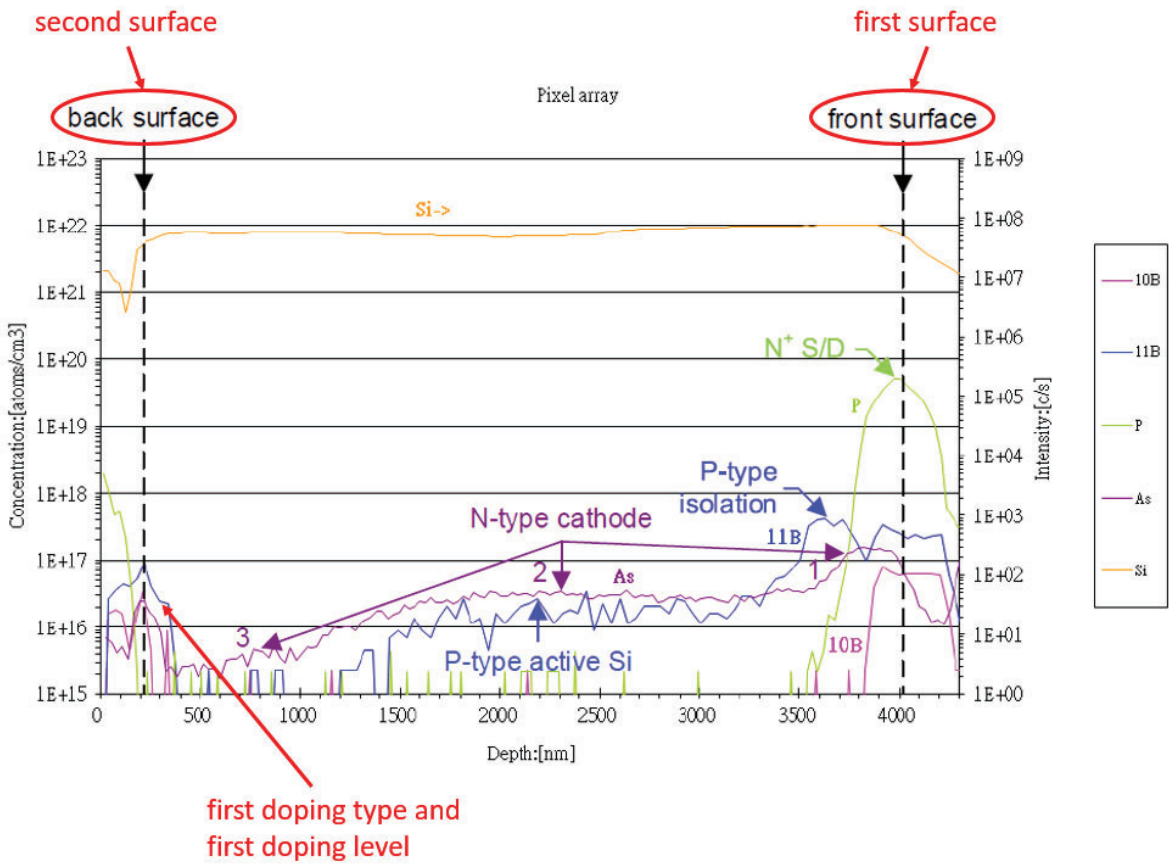
U.S. Patent No. 10,510,842	Accused Products
	 As shown above, the substrate is p-type (a first doping type) and has a first doping level.
[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-Sony Accused Products meet this limitation. For example, the following scanning electron microscope (SEM) bevel image shows two adjacent rows of shared pixels, and thus shows first and second active regions. Transistors are formed in the first active region as shown below. Upon information and belief, the first active region (shown below) is n-type (a second doping type opposite in conductivity to the first doping type).

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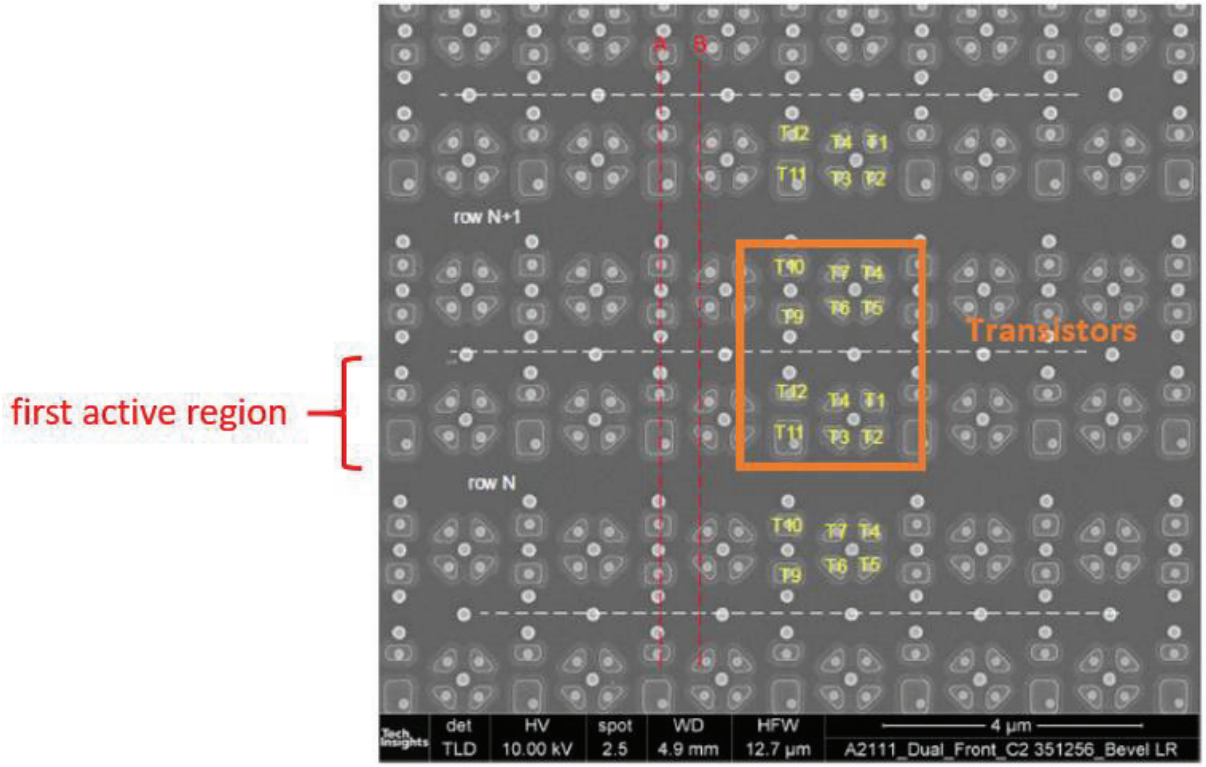
U.S. Patent No. 10,510,842	Accused Products
	 The first active region is disposed adjacent the first surface of the substrate, as shown in the following SEM cross-sectional image discussed above for Element 1:

Exhibit D-1 to Greenthread's Preliminary Infringement Contentions (4/29/2022)

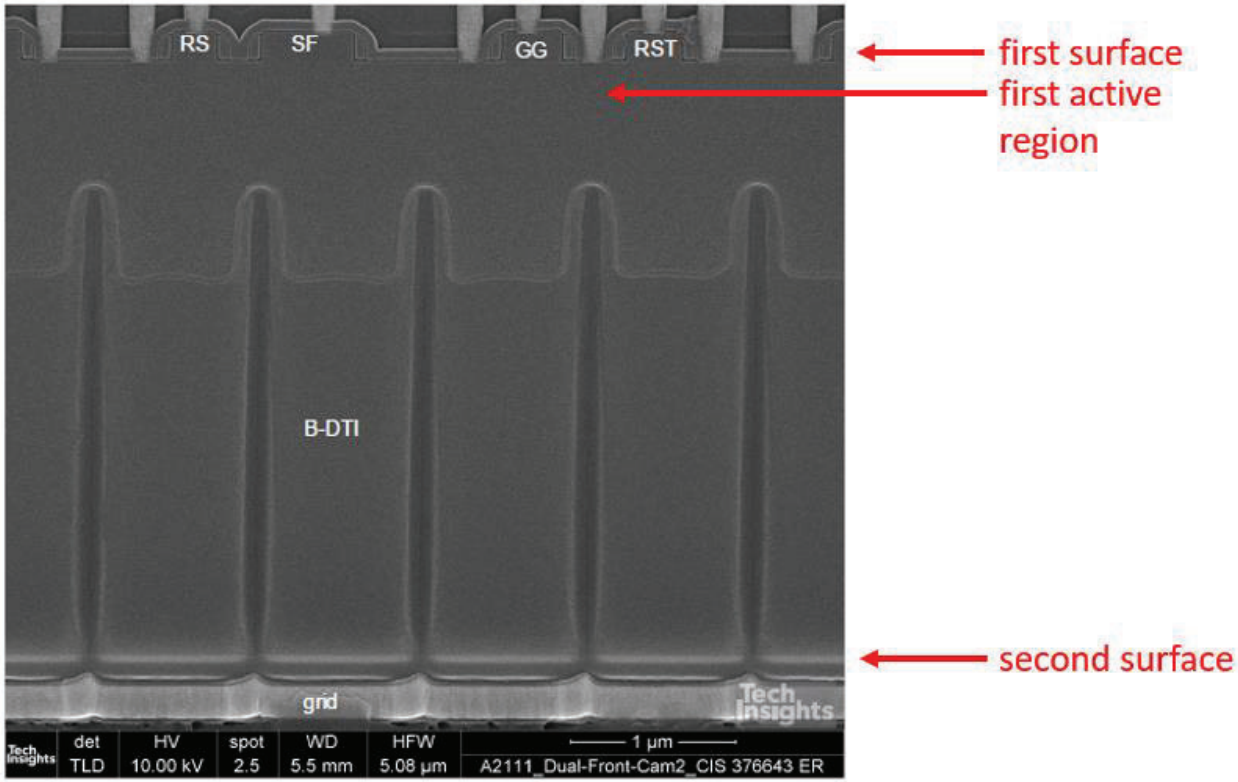
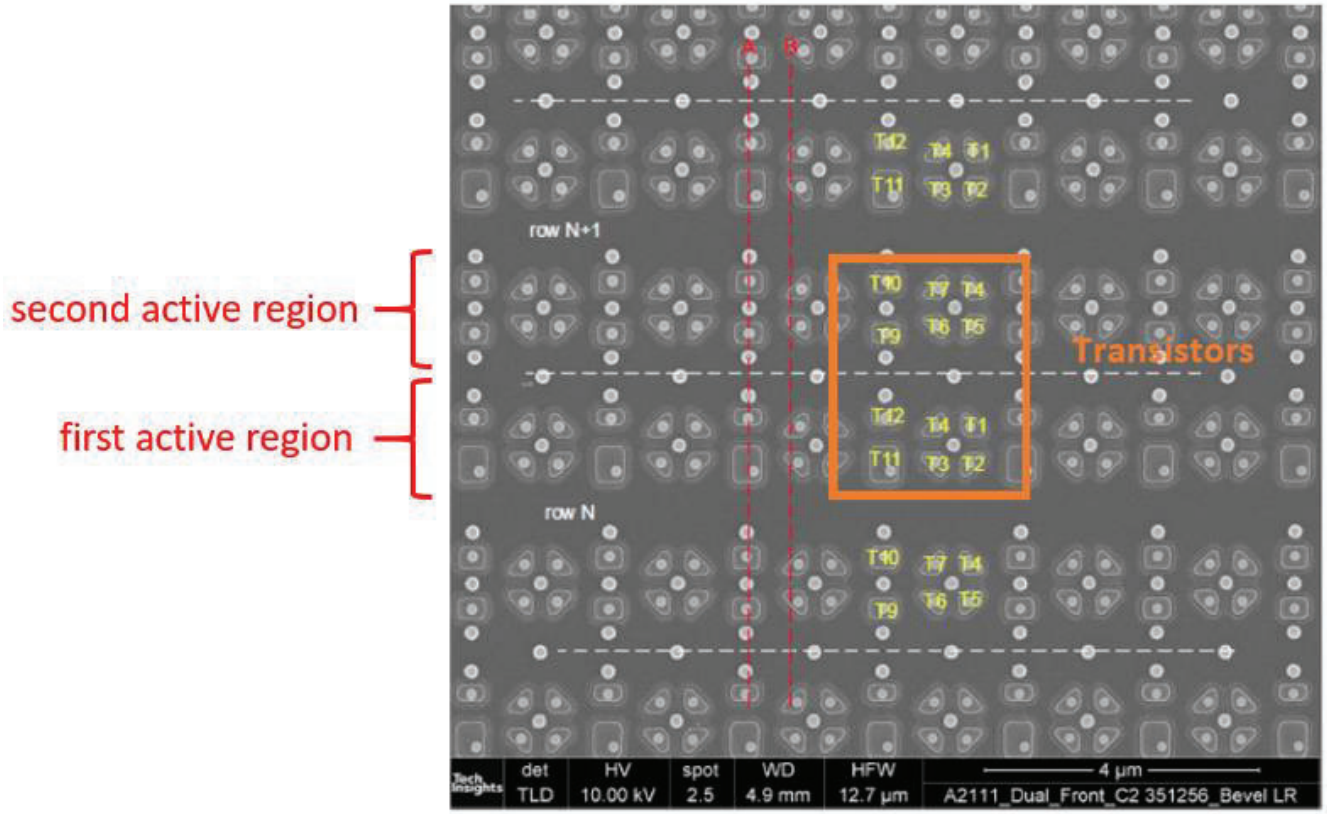
U.S. Patent No. 10,510,842	Accused Products
	
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Sony Accused Products meet this limitation. For example, this is shown by the following SEM image of the Sony CMOS image sensor discussed above for Element 2. As discussed above for Element 2, the SEM image shows two adjacent rows of shared pixels, and thus shows first and second active regions.

Exhibit D-1 to Greenthread's Preliminary Infringement Contentions (4/29/2022)

U.S. Patent No. 10,510,842	Accused Products
	
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region; and	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Elements 2-3.
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first	The Dell-Sony Accused Products meet this limitation. For example, this is shown by the SEM and scanning microwave impedance microscopy (SMIM) images below and the SIMS graph below. The contrast in the SMIM image is proportional to the capacitance of the sample under inspection, so that brighter green corresponds to higher dopant concentration, and darker green/black corresponds to lower dopant concentration.

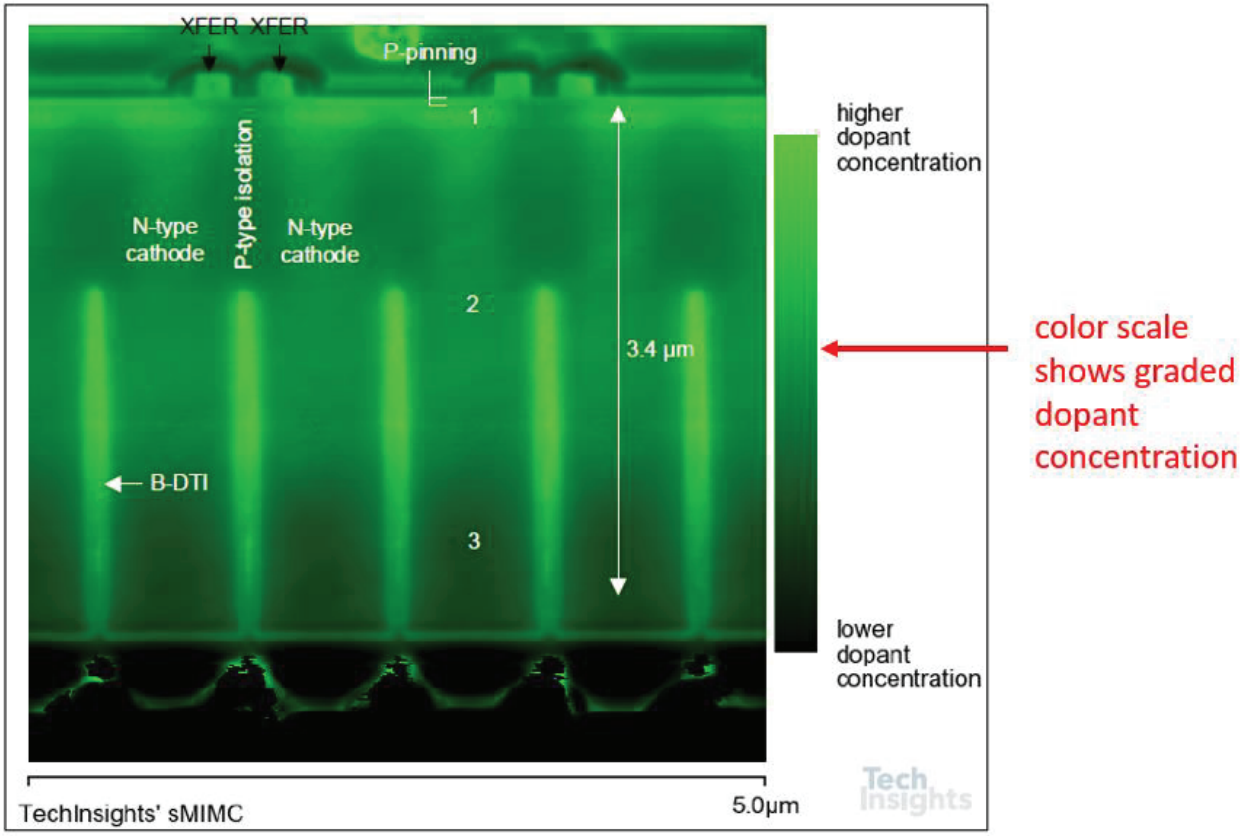
U.S. Patent No. 10,510,842	Accused Products
surface to the second surface of the substrate.	 **SMIM-C** As shown by the slope of the blue plot (boron-11, which is p-type) and the dark purple plot (arsenic, which is n-type) in the SIMS graph below, at least a portion of at least one of the first and second active regions has at least one graded dopant concentration to aid carrier movement from the front surface (first surface) to the back surface (second surface) of the substrate.

Exhibit D-1 to Greenthread's Preliminary Infringement Contentions (4/29/2022)

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	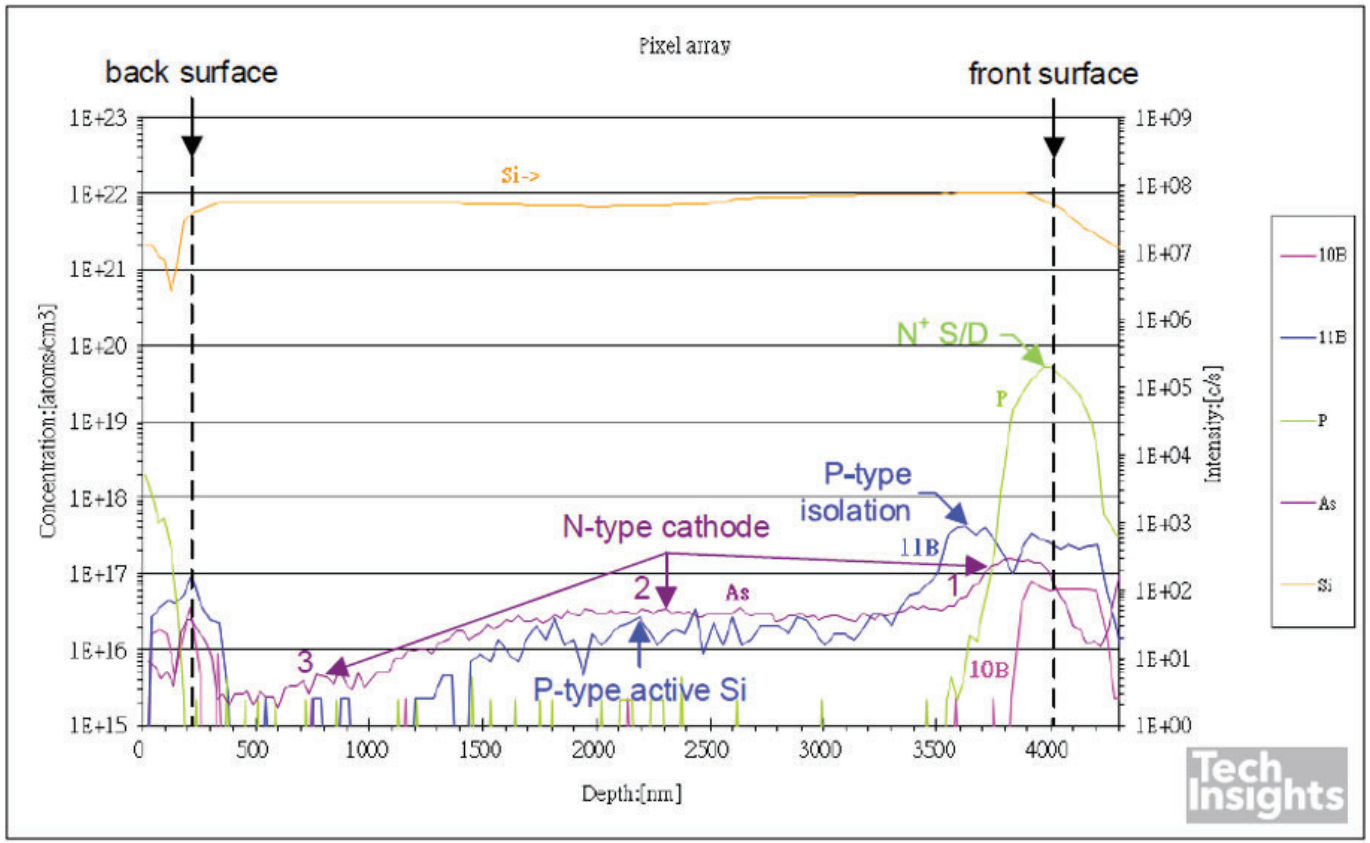 For example, at least one downward sloped portion is shown in each of the boron-11 and arsenic plots above, viewed from right (more depth) to left (less depth).
2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The substrate of the semiconductor device of the Dell-Sony Accused Products is a p-type substrate, as discussed above for Claim 1, Element 1.
5. The semiconductor device of claim 1, wherein the first active region and second active region	The Dell-Sony Accused Products meet this limitation. Upon information and belief, the first active region and second active region contain NMOS transistors (n-channel devices) or PMOS transistors (p-channel devices).

Exhibit D-1 to Greenthread's Preliminary Infringement Contentions (4/29/2022)

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contain one of either p-channel and n-channel devices.	
7. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The Dell-Sony Accused Products meet this limitation. Upon information and belief, the first active region and second active region are each separated by at least one isolation region to avoid one pixel electrically interfering with an adjacent pixel. Information about isolation regions in Dell-Sony Accused Products is in the possession of the Dell Defendants and is expected to be obtained through discovery.
8. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, for the Dell-Sony Accused Products, the graded dopant is fabricated with an ion implantation process. For example, ion implantation is the prevalent process for implementing doping in semiconductor devices, and is believed to be used for the Dell-Sony Accused Products. Information about the fabrication process for Dell-Sony Accused Products, including usage of an ion implantation process, is in the possession of the Dell Defendants and is expected to be obtained through discovery.
[Claim 9, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Sony Accused Products include a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 9, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 1.
[Claim 9, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 2. Upon information and belief, transistors can be formed in the surface of the first active region. Details regarding formation of transistors are in the possession of the Dell Defendants and are expected to be obtained through discovery.
[Claim 9, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 3. Upon information and belief, transistors can be formed in the surface of the second active region. Details regarding formation of transistors are in the possession of the Dell Defendants and are expected to be obtained through discovery.
[Claim 9, Element 4] transistors formed in at least one	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 4.

Exhibit D-1 to Greenthread's Preliminary Infringement Contentions (4/29/2022)

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of the first active region or second active region; and	
[Claim 9, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate.	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 5.
10. The semiconductor device of claim 9, wherein the substrate is a p-type substrate.	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 2.
13. The semiconductor device of claim 9, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 5.
15. The semiconductor device of claim 9, wherein the first active region and second active region are each separated by at least one isolation region.	Upon information and belief, the Dell-Sony Accused Products meet this limitation. *See* above at Claim 7.
16. The semiconductor device of claim 9, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, the Dell-Sony Accused Products meet this limitation. *See* above at Claim 8.
17. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Elements 2-3.
18. The semiconductor device of claim 1, wherein the transistors which can be formed in the first	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Preamble and Elements 2-3 (discussing CMOS). CMOS transistors require a source, a drain, a gate, and a channel region.

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and second active regions are CMOS transistors requiring a source, a drain, a gate and a channel region.	

Exhibit D-2 to Greenthread's Preliminary Infringement Contentions (4/29/2022)

U.S. Patent No. 10,734,481	Accused Products
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Sony Accused Products include a semiconductor device. *See* Exhibit D-1, Claim 1, Preamble. The Sony 12 MP 1.0 µm Pixel Pitch, Stacked Back-Illumination CMOS Image Sensor referenced in Exhibit D-1 for tear-down analysis is discussed in this claim chart and other infringement contention claim charts as an example of an image sensor representative of the Dell-Sony Accused Products. Upon information and belief, such a Sony image sensor is representative of image sensors used in the Dell-Sony Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other image sensors used in Dell-Sony Accused Products would have similarly been advantageously designed to move carriers and achieve the performance enhancements described and claimed in the '481 patent (and the other asserted patents). For example, other image sensors would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '481 patent (and the other asserted patents). Therefore, upon information and belief, other image sensors used in Dell-Sony Accused Products contain similar features as the Sony 12 MP 1.0 µm Pixel Pitch, Stacked Back-Illumination CMOS Image Sensor, and function in a similar way, with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 1.
[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 2.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 3.
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 4.

Exhibit D-2 to Greenthread's Preliminary Infringement Contentions (4/29/2022)

U.S. Patent No. 10,734,481	Accused Products
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 5.
[Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.	Upon information and belief, the Dell-Sony Accused Products meet this limitation. Information about well regions and doping in such regions is in the possession of the Dell Defendants, and is expected to be obtained through discovery.
2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 2.
4. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 5.
6. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 7.
7. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 8.
8. The semiconductor device of claim 1, wherein the first and second	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Elements 1-3.

Exhibit D-2 to Greenthread's Preliminary Infringement Contentions (4/29/2022)

U.S. Patent No. 10,734,481	Accused Products
active regions are formed adjacent the first surface of the substrate.	
9. The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 5 (SIMS graph showing p-type boron-11 doping).
13. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring at least a source, a drain, a gate and a channel.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 18.
19. The semiconductor device of claim 1, wherein the device is an image sensor.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Preamble.
[Claim 20, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Sony Accused Products meet include a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 20, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 1.
[Claim 20, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 9, Element 2.
[Claim 20, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 9, Element 3.

Exhibit D-2 to Greenthread's Preliminary Infringement Contentions (4/29/2022)

U.S. Patent No. 10,734,481	Accused Products
which transistors can be formed in the surface thereof;	
[Claim 20, Element 4] transistors formed in at least one of the first active region or second active region;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 4.
[Claim 20, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate; and	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 5.
[Claim 20, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 6.
22. The semiconductor device of claim 20, wherein the substrate is a p-type substrate.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 2.
24. The semiconductor device of claim 20, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 5.
26. The semiconductor device of claim 20, wherein the first active region and second active region are each separated by at least one isolation region.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 7.

Exhibit D-2 to Greenthread's Preliminary Infringement Contentions (4/29/2022)

U.S. Patent No. 10,734,481	Accused Products
27. The semiconductor device of claim 20, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 9.
31. The semiconductor device of claim 20, wherein the graded dopant is fabricated with an ion implantation process.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 8.
36. The semiconductor device of claim 20, wherein the device is an image sensor.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Preamble.

Exhibit D-3 to Greenthread's Preliminary Infringement Contentions (4/29/2022)

U.S. Patent No. 11,121,222	Accused Products
[Claim 1, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Sony Accused Products include a VLSI semiconductor device. The Sony image sensor discussed for claim 1 of Exhibit D-1 is a semiconductor device (*see* Exhibit D-1, Claim 1, Preamble) and is a VLSI semiconductor device upon information and belief. Details regarding transistor count are in the possession of the Dell Defendants and are expected to be obtained through discovery. The Sony 12 MP 1.0 µm Pixel Pitch, Stacked Back-Illumination CMOS Image Sensor referenced in Exhibit D-1 is discussed in this claim chart and other infringement contention claim charts as an example of an image sensor representative of the Dell-Sony Accused Products. Upon information and belief, such a Sony image sensor is representative of image sensors used in the Dell-Sony Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other image sensors used in Dell-Sony Accused Products would have similarly been advantageously designed to move carriers and achieve the performance enhancements described and claimed in the '222 patent (and the other asserted patents). For example, other image sensors would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '222 patent (and the other asserted patents). Therefore, upon information and belief, other image sensors used in Dell-Sony Accused Products contain similar features as the Sony 12 MP 1.0 µm Pixel Pitch, Stacked Back-Illumination CMOS Image Sensor, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having a surface;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 1.
[Claim 1, Element 2] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 2.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 3.
[Claim 1, Element 4] transistors formed in at least one of the first	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 4.

Exhibit D-3 to Greenthread's Preliminary Infringement Contentions (4/29/2022)

U.S. Patent No. 11,121,222	Accused Products
active region or second active region;	
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 5. For example, referencing the SIMS graph discussed at Exhibit D-1, Claim 1, Element 5 and shown below, there are no active regions at the left side of the graph, e.g., at depths of less than about 1500 nm.
[Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.	Upon information and belief, the Dell-Sony Accused Products meet this limitation. Details regarding well regions and transistors of the Dell-Sony Accused Products are in the possession of the Dell Defendants and are expected to be obtained through discovery.
2. The VLSI semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 2.
4. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain digital logic formed by one of either p-channel and n-channel devices.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 5; Exhibit D-2, Claim 4. Upon information and belief, the first and second active regions contain digital logic as claimed. *See* above at Claim 1, Element 6.
6. The VLSI semiconductor device of claim 1, wherein the first active region and second	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 7.

Exhibit D-3 to Greenthread's Preliminary Infringement Contentions (4/29/2022)

U.S. Patent No. 11,121,222	Accused Products
active region are each separated by at least one isolation region.	
7. The VLSI semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 8.
8. The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Elements 1-3.
9. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-2, Claim 9.
13. The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-2, Claim 13. Upon information and belief, the transistors which can be formed in the first and second active regions are CMOS digital logic transistors as claimed. *See* above at Claim 1, Element 6.
19. The VLSI semiconductor device of claim 1, wherein the device is an image sensor.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Preamble.
20. The VLSI semiconductor device of claim 1, wherein each of the first and second active regions are in the lateral or vertical direction.	Upon information and belief, the Dell-Sony Accused Products meet this limitation.

Exhibit D-3 to Greenthread's Preliminary Infringement Contentions (4/29/2022)

U.S. Patent No. 11,121,222	Accused Products
[Claim 21, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Sony Accused Products include a semiconductor device. *See* above at Claim 1, Preamble.
[Claim 21, Element 1] a substrate of a first doping type at a first doping level having a surface;	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 1.
[Claim 21, Element 2] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 9, Element 2.
[Claim 21, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 9, Element 3.
[Claim 21, Element 4] transistors formed in at least one of the first active region or second active region;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 4.
[Claim 21, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 5.

Exhibit D-3 to Greenthread's Preliminary Infringement Contentions (4/29/2022)

U.S. Patent No. 11,121,222	Accused Products
[Claim 21, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-2, Claim 1, Element 6. As shown by SIMS analysis (*see* Exhibit D-1, Claim 1, Element 5), the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof. For example, the quasilinear nature of the concentration is shown in the SIMS graph discussed at Exhibit D-1, Claim 1, Element 5.
23. The VLSI semiconductor device of claim 21, wherein the substrate is a p-type substrate.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 2.
25. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 5.
27. The VLSI semiconductor device of claim 21, wherein the first active region and second active region are each separated by at least one isolation region.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 7.
28. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-2, Claim 9.

Exhibit D-3 to Greenthread's Preliminary Infringement Contentions (4/29/2022)

U.S. Patent No. 11,121,222	Accused Products
32. The VLSI semiconductor device of claim 21, wherein the graded dopant is fabricated with an ion implantation process.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 8.
37. The VLSI semiconductor device of claim 21, wherein the device is an image sensor.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Preamble.
38. The VLSI semiconductor device of claim 21, wherein each of the first and second active regions are in the lateral or vertical direction.	Upon information and belief, the Dell-Sony Accused Products meet this limitation.
[Claim 39, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Sony Accused Products include a semiconductor device. *See* Exhibit D-1, Claim 1, Preamble.
[Claim 39, Element 1] a substrate of a first doping type at a first doping level;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 1.
[Claim 39, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 2.
[Claim 39, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 3.
[Claim 39, Element 4] transistors formed in at least one	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 4.

Exhibit D-3 to Greenthread's Preliminary Infringement Contentions (4/29/2022)

U.S. Patent No. 11,121,222	Accused Products
of the first active region or second active region; and	
[Claim 39, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 5; *see* above at Claim 21, Element 5.
[Claim 41, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Dell-Sony Accused Products include a semiconductor device. *See* above at Claim 39, Preamble.
[Claim 41, Element 1] a substrate of a first doping type at a first doping level;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 1.
[Claim 41, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 39, Element 2.
[Claim 41, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 39, Element 3.
[Claim 41, Element 4] transistors formed in at least one of the first active region or second active region; and	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Element 4.

Exhibit D-3 to Greenthread's Preliminary Infringement Contentions (4/29/2022)

U.S. Patent No. 11,121,222	Accused Products
[Claim 41, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 21, Element 5. The SIMS graph discussed at Exhibit D-1, Claim 1, Element 5 shows at least one graded dopant acceptor concentration (e.g., boron-11 concentration) as claimed.

Exhibit D-6 to Greenthread's Preliminary Infringement Contentions (4/29/2022)

U.S. Patent No. 11,316,014	Accused Products
[Claim 1, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the Dell-Sony Accused Products include an electronic system. *See* Exhibit D-1, Claim 1, Preamble; Exhibit D-1, Claim 1, Preamble. Each Dell-Sony Accused Product is an electronic system, because a computer is an electronic system. The Sony 12 MP 1.0 µm Pixel Pitch, Stacked Back-Illumination CMOS Image Sensor referenced in Exhibit D-1 is discussed in this claim chart and other infringement contention claim charts as an example of an image sensor representative of the Dell-Sony Accused Products. Upon information and belief, such a Sony image sensor is representative of image sensors used in the Dell-Sony Accused Products for purposes of this claim chart and the other infringement contention claim charts because, e.g., other image sensors used in Dell-Sony Accused Products would have similarly been advantageously designed to move carriers and achieve the performance enhancements described and claimed in the '014 patent (and the other asserted patents). For example, other image sensors would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '014 patent (and the other asserted patents). Therefore, upon information and belief, other image sensors used in Dell-Sony Accused Products contain similar features as the Sony 12 MP 1.0 µm Pixel Pitch, Stacked Back-Illumination CMOS Image Sensor, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Preamble.
[Claim 1, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 1, Element 1.
[Claim 1, Element 1c] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 1, Element 2; Exhibit D-1, Claim 9, Element 2.
[Claim 1, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 1, Element 3; Exhibit D-1, Claim 9, Element 3.
[Claim 1, Element 1e] transistors formed in at least one of the first active region or second active region;	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 1, Element 4.

Exhibit D-6 to Greenthread's Preliminary Infringement Contentions (4/29/2022)

U.S. Patent No. 11,316,014	Accused Products
[Claim 1, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 1, Element 5.
[Claim 1, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the semiconductor device.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 1, Element 6; Exhibit D-3, Claim 21, Element 6.
2. The system of Claim 1, wherein the substrate of the at least one semiconductor device is a p-type substrate.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 2.
4. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain digital logic formed by one of either p-channel and n-channel devices.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 4.
6. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 6.
7. The system of Claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 7.
8. The system of Claim 1, wherein the first and second active regions of	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 8.

Exhibit D-6 to Greenthread's Preliminary Infringement Contentions (4/29/2022)

U.S. Patent No. 11,316,014	Accused Products
the at least one semiconductor device are formed adjacent the first surface of the substrate of the at least one semiconductor device.	
9. The system of Claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 9.
13. The system of claim 1, wherein the transistors which can be formed in the first and second active regions of the at least one semiconductor device are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 13.
19. The system of Claim 1, wherein the at least one semiconductor device is an image sensor.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-1, Claim 1, Preamble.
20. The system of Claim 1, wherein each of the first and second active regions of the at least one semiconductor device are in the lateral or vertical direction.	Upon information and belief, the Dell-Sony Accused Products meet this limitation.
[Claim 21, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the Dell-Sony Accused Products include an electronic system. *See* above at Claim 1, Preamble.
[Claim 21, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 1a.
[Claim 21, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 1b.
[Claim 21, Element 1c] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 1c; Exhibit D-1, Claim 9, Element 2.

Exhibit D-6 to Greenthread's Preliminary Infringement Contentions (4/29/2022)

U.S. Patent No. 11,316,014	Accused Products
and within which transistors can be formed in the surface thereof;	
[Claim 21, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 1d; Exhibit D-1, Claim 9, Element 3.
[Claim 21, Element 1e] transistors formed in at least one of the first active region or second active region;	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 1e.
[Claim 21, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 1f; Exhibit D-1, Claim 9, Element 5.
[Claim 21, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier thereof movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.	The Dell-Sony Accused Products meet this limitation. *See* above at Claim 1, Element 1g; Exhibit D-3, Claim 21, Element 6.
23. The system of Claim 21, wherein the substrate of the at least one semiconductor device is a p-type substrate.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 23.
25. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain at	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 25.

Exhibit D-6 to Greenthread's Preliminary Infringement Contentions (4/29/2022)

U.S. Patent No. 11,316,014	Accused Products
least one of either p-channel and n-channel devices.	
27. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 27.
28. The system of Claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.	The Dell-Sony Accused Products meet this limitation. *See* Exhibit D-3, Claim 28.