

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

GREENTHREAD, LLC

Plaintiff,

vs.

TEXAS INSTRUMENTS INCORPORATED

Defendants.

Civil Action No. 2:23-cv-157

JURY TRIAL DEMANDED

ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Greenthread, LLC (“Greenthread” or “Plaintiff”) files this Original Complaint against Texas Instruments Incorporated (“Texas Instruments” or “Defendant”) and hereby alleges as follows:

THE NATURE OF THE ACTION

1. Greenthread owns a family of patents related to transistors and other components of integrated semiconductor devices. Greenthread’s patented inventions describe semiconductor devices that employ graded dopants and well regions for creating electric fields for aiding and/or limiting the movement of carriers to (or from) the semiconductor surface to (or from) the semiconductor substrate. These inventions improve semiconductor devices by (1) creating faster, more efficient, and more reliable processors, logic devices, DRAM and NAND flash, and image sensors and (2) allowing manufacturers to scale down the feature size of their semiconductor products.

2. Defendant has infringed and continue to infringe six Greenthread patents: U.S. Patent Nos. 8,421,195 (the “195 Patent”), 9,190,502 (the “502 Patent”), 10,510,842 (the “842

Patent”), 10,734,481 (the “’481 Patent”), 11,121,222 (the “’222 Patent”), and 11,316,014 (the “’014 Patent”), (collectively “the Greenthread Patents”), copies of which are attached hereto as Exhibits 1-6, respectively. Defendant has infringed and continue to infringe the Greenthread Patents by making, using, selling, offering for sale, and/or importing into the United States, semiconductor devices with infringing graded dopant regions and/or electronic products containing the same.

THE PARTIES

3. Plaintiff Greenthread, LLC (“Greenthread”) is a limited liability company organized and existing under the laws of Texas, having its principal place of business at 7424 Mason Dells Drive, Dallas, Texas 75230-3244.

4. Defendant Texas Instruments Incorporated is a corporation organized and existing under the laws of the State of Delaware with its principal place of business at 12500 TI Boulevard, Dallas, Texas 75243.

5. Texas Instruments is “a global semiconductor company that designs, manufactures, tests, and sells analog and embedded processing chips.”¹ Texas Instruments designs, manufactures, tests, and sells semiconductor devices to approximately 100,000 customers from a portfolio of about 80,000 products with 14 manufacturing sites worldwide.²

6. Texas Instruments maintains at least three offices in this District, including, but not limited to, at 300 W Renner Road, Richardson, Texas, 75080, 6412 S. U.S. 75, Sherman, TX, 75090, and 2501 TX-121 Bus, Lewisville, TX 75067. At two of these locations, Richardson and

¹ <https://www.ti.com/about-ti/company/overview.html>

² <https://www.ti.com/about-ti/company/what-we-do.html>

Sherman, Texas Instruments manufactures semiconductor devices, including, on information and belief, products which infringe the Greenthread Patents.³

SUBJECT MATTER JURISDICTION

7. This action arises under the patent laws of the United States, namely 35 U.S.C. §§ 271, 281, and 284-285, among others.

8. This court has subject matter jurisdiction over the patent infringement claims asserted in this case under 28 U.S.C. §§ 1331 and 1338(a).

PERSONAL JURISDICTION AND VENUE

9. This Court has personal jurisdiction over Texas Instruments in accordance with the Texas Long Arm Statute, Tex. Civ. Prac. & Rem. Code § 17.041, *et seq.*, and constitutional due process, because, among other things, Texas Instruments does business in this State and maintains offices in this District. Specifically, Texas instruments has engaged, and continues to engage, in continuous, systematic, and substantial activities within this State, including the substantial marketing, making, using, manufacturing, and sale of products and services within this State and this District. Further, Texas Instruments has derived substantial revenue from its goods and services provided to individuals in this State and this District, and maintains regular and established places of business in this District, including the locations referenced in the preceding section.

10. Venue is proper under 28 U.S.C. §§ 1391(b) and 1400(b) because Texas Instruments has regular and established places of business in this District and has committed acts

³ <https://www.ti.com/about-ti/company/ti-at-a-glance/manufacturing/richardson.html>; *see also* <https://news.ti.com/texas-instruments-breaks-ground-on-new-300-mm-semiconductor-wafer-fabrication-plants-in-sherman-texas>

of infringement in this District, including, on information and belief, by manufacturing accused products at its facilities in 6412 U.S. Highway 75, Sherman, Texas 75090; 300 W. Renner Road, Richardson, Texas 75080; and 2501 S. State Highway 121 Bus., Lewisville, Texas 75067.

11. “Texas Instruments Accused Products” are products accused of meeting the claim limitations of a Greenthread Patent in this suit. Specifically, Texas Instruments designs and manufactures semiconductor products, including, but not limited to, amplifiers, audio processors, digital-to-analog converters, analog-to-digital converters, digital clocks, interface ICs, isolation ICs, microcontrollers and processors, digital signal processors, digital light processors, motor drivers, power management, switches & multiplexers, radio frequency and microwave ICs, wireless connectivity ICs, logic & voltage translation, sensors, and other ICs (“Texas Instruments Accused Products”). An exemplary, non-exhaustive, list of the various types or categories of Texas Instruments Accused Products is identified in Exhibit 8 and is herein incorporated by reference.

12. Exhibit 8 demonstrates how exemplary TI Accused Products meet the claim limitations of Greenthread Patents and is herein incorporated by reference. The exemplary products identified therein meet each and every element of at least one claim of the Greenthread Patents.

THE GREENTHREAD PATENTS

13. On April 16, 2013, the U.S. Patent and Trademark Office duly and legally issued U.S. Patent No. 8,421,195 (“the ’195 Patent”), entitled “Semiconductor Devices with Graded Dopant Regions,” listing Dr. Mohan Rao as the inventor, from a patent application filed January 12, 2007. The ’195 Patent claims priority from U.S. Patent Application No. 10/934,915,⁴ filed on

⁴ Pub. No. US 2006/0049464.

September 3, 2004. A true and correct copy of the '195 Patent is attached hereto as Exhibit 1 and incorporated herein by reference.

14. On November 17, 2015, the U.S. Patent and Trademark Office duly and legally issued U.S. Patent No. 9,190,502 (“the '502 Patent”), entitled “Semiconductor Devices with Graded Dopant Regions,” listing Dr. Mohan Rao as the inventor, from a patent application filed October 16, 2014. The '502 Patent claims priority from U.S. Patent Application No. 10/934,915,⁵ filed on September 3, 2004. A true and correct copy of the '502 Patent is attached hereto as Exhibit 2 and incorporated herein by reference.

15. On December 17, 2019, the U.S. Patent and Trademark Office duly and legally issued U.S. Patent No. 10,510,842 (“the '842 Patent”), entitled “Semiconductor Devices with Graded Dopant Regions,” listing Dr. Mohan Rao as the inventor, from a patent application filed on May 9, 2017. The '842 Patent claims priority from U.S. Patent Application No. 10/934,915,⁶ filed on September 3, 2004. A true and correct copy of the '842 Patent is attached hereto as Exhibit 3 and incorporated herein by reference.

16. On August 4, 2020, the U.S. Patent and Trademark Office duly and legally issued U.S. Patent No. 10,734,481 (“the '481 Patent”), entitled “Semiconductor Devices with Graded Dopant Regions,” listing Dr. Mohan Rao as the inventor, from a patent application filed on December 17, 2019. The '481 Patent claims priority from U.S. Patent Application No. 10/934,915,⁷ filed on September 3, 2004. A true and correct copy of the '481 Patent is attached hereto as Exhibit 4 and incorporated herein by reference.

17. On September 14, 2021, the U.S. Patent and Trademark Office duly and legally

⁵ Pub. No. US 2006/0049464.

⁶ Pub. No. US 2006/0049464.

⁷ Pub. No. US 2006/0049464.

issued U.S. Patent No. 11,121,222 (“the ’222 Patent”), entitled “Semiconductor Devices with Graded Dopant Regions,” listing Dr. Mohan Rao as the inventor, from a patent application filed on July 27, 2020. The ’222 Patent claims priority from U.S. Patent Application No. 10/934,915,⁸ filed on September 3, 2004. A true and correct copy of the ’222 Patent is attached hereto as Exhibit 5 and incorporated herein by reference.

18. On April 26, 2022, the U.S. Patent and Trademark Office duly and legally issued U.S. Patent No. 11,316,014 (“the ’014 Patent”), entitled “Semiconductor Devices with Graded Dopant Regions,” listing Dr. Mohan Rao as the inventor, from a patent application filed on July 9, 2021. The ’014 Patent claims priority from U.S. Patent Application No. 10/934,915,⁹ filed on September 3, 2004. A true and correct copy of the ’014 Patent is attached hereto as Exhibit 6 and incorporated herein by reference.

19. The ’195, ’502, ’842, ’481, ’222, and ’014 Patents are collectively referred to as the “Greenthread Patents.”

20. Greenthread exclusively owns all rights, title, and interest in the Greenthread Patents necessary to bring this action, including the right to recover past and future damages. Certain of the Greenthread Patents were previously owned by Dr. G.R. Mohan Rao (“Dr. Rao”). On April 27, 2015, Dr. Rao assigned to Greenthread the then-issued Greenthread Patents and all related “continuations, continuations-in-part and extensions of said Applications and Patents and any pending applications or issued patents that directly claim or are amended to claim priority to any of the Applications or Patents.” Dr. Rao’s assignment was recorded with the U.S. Patent and Trademark Office on May 13, 2015, and again on July 22, 2021, and is attached hereto as Exhibit

⁸ Pub. No. US 2006/0049464.

⁹ Pub. No. US 2006/0049464.

7. Greenthread has therefore owned all rights to the Greenthread Patents necessary to bring this action throughout the period of Texas Instrument's infringement and still owns those rights to the Greenthread Patents.

21. Defendant is not currently licensed to practice the Greenthread Patents.

22. The Greenthread Patents are valid and enforceable.

FACTUAL BACKGROUND

23. Dr. G.R. Mohan Rao ("Dr. Rao"), the sole inventor of the Greenthread Patents, has been an innovator in the semiconductor industry since the 1960s. He is a named inventor on more than 100 Patents worldwide and authored numerous technical publications over the last 50 years.

24. In September 1968, Dr. Rao received a Ph.D. in physics with a specialization in electronics from Andhra University in Waltair, India. He then traveled to the United States to attend a graduate program in physics at the University of Cincinnati.

25. After learning of an opportunity to work with Professor William Carr of Southern Methodist University ("SMU"), Dr. Rao transferred to SMU where he earned a Ph.D. in Electrical Engineering. While there, he worked in the SMU laboratory with Jack Kilby of Texas Instruments (a pioneering electrical engineer who would later receive a Nobel Prize for his work), on metal-oxide-silicon transistors ("MOS devices"), which are used for switching and amplifying electronic signals in electronic devices. MOS devices form the basis of modern electronics and are the most widely used semiconductor devices in the world. The U.S. Patent and Trademark Office has called this device a "groundbreaking invention that transformed life and culture around the world."¹⁰ Dr. Rao built these devices from scratch while a graduate student at SMU.

26. Through his mentor, Jack Kilby, Dr. Rao interviewed with—and was ultimately

¹⁰ <https://www.uspto.gov/about-us/news-updates/remarks-director-iancu-2019-international-lectual-property-conference>

hired by—Texas Instruments to continue his work on MOS devices in 1972. Dr. Rao worked at Texas Instruments for the next twenty-two years, rising from an engineer to a Senior Fellow. At that time, Texas Instruments had only 12 Senior Fellows out of approximately 20,000 engineers. Eventually, Dr. Rao moved into a management position at Texas Instruments, ultimately becoming a Senior Vice President in 1985.

27. At Texas Instruments, Dr. Rao received his first patent while working in a process and product engineering capacity to solve a production problem with Texas Instruments' 4-kilobit RAM product. That patent was merely the beginning of Dr. Rao's long inventive career. Indeed, from the late 1970s through the mid-1980s, Dr. Rao worked on or managed projects relating to Texas Instruments' 64kb RAM, 256Kb RAM, 1Mb RAM, 4 Mb RAM, EEPROM, SRAM, and microcontrollers. For that work, Dr. Rao received numerous additional U.S. Patents.

28. The USPTO was not the only organization to recognize Dr. Rao's achievements. Some of Dr. Rao's work at Texas Instruments was so remarkable that it has been credited in multiple exhibits in the National Museum of American History at the Smithsonian Institution.¹¹ For example, the Smithsonian has displayed Texas Instruments' experimental 1-megabit CMOS DRAM, produced in April 1985 under Dr. Rao's leadership, and credited Dr. Rao for the achievement.¹²

¹¹ <http://smithsonianchips.si.edu/texas/wafer.htm>

¹² http://smithsonianchips.si.edu/texas/t_360.htm



29. In 1994, Dr. Rao left Texas Instruments for Cirrus Logic. During his two-year tenure at Cirrus Logic, he received more U.S. Patents relating to his work on integrated graphics controllers and memory.

30. In 1996, Dr. Rao started a company called Silicon Aquarius. Through a relationship between Silicon Aquarius and Matsushita, Dr. Rao led a design team in working on a 256Mb DRAM chip. After Silicon Aquarius ceased operations, Dr. Rao did consulting work for a number of different consulting companies and devoted much of his free time to thinking about various challenges and problems with which the semiconductor industry had struggled for years.

31. In 2003, Dr. Rao and Philip John founded Greenthread to continue Dr. Rao's pioneering work. A focal point of Dr. Rao's research was poor refresh time and the related problem of how to deal with and control the movement of both wanted and unwanted carriers in semiconductor devices, including memory and logic devices. Dr. Rao realized that graded dopants

could be used to create a “drift layer” and other structures to facilitate the movement—in an upward or downward direction, as appropriate—of carriers from the semiconductor surfaces down into the substrate and vice versa. It was Dr. Rao’s work on this problem that culminated in the Greenthread Patents.

TEXAS INSTRUMENT’S INFRINGEMENT

32. Texas Instruments has directly infringed, and continues to infringe, one or more claims of each of the Greenthread Patents through making, using, offering to sell, selling within the United States, and/or importing into the United States semiconductor products, including, but not limited to, amplifiers, audio processors, digital-to-analog converters, analog-to-digital converters, digital clocks, interface ICs, isolation ICs, microcontrollers and processors, digital signal processors, digital light processors, motor drivers, power management, switches & multiplexers, radio frequency and microwave ICs, wireless connectivity ICs, logic & voltage translation, sensors, and other ICs, that practice the claimed inventions (*i.e.*, the Texas Instruments Accused Products). A non-exhaustive, exemplary list of the types or categories of products or devices that infringe are further identified in Exhibit 8.

33. As shown in Exhibit 8, an exemplary Texas Instrument Accused Product, BQ25123, meets each and every element of at least one claim of the Greenthread Patents.

34. Upon information and belief, Texas Instruments fabricates and designs the Texas Instruments Accused Products using similar designs according to a limited number of processes, many or all of which utilize substantially similar process steps, including process steps for creating regions with graded dopant concentrations, because the invention would have application in those categories of products, for example by improving switching time in transistors in the Texas Instruments Accused Products. Upon information and belief, the Texas Instruments Accused

Products are in relevant part substantially similar to the exemplary BQ25123 shown in Exhibit 8, particularly with regard to the manner in which the exemplary BQ25123 includes and utilizes regions with graded dopant concentrations. Exhibit 8 is thus illustrative of the manner in which the Texas Instruments Accused Products meet the claim limitations of the Greenthread Patents.¹³

35. Texas Instruments' infringement is willful. Texas Instruments had knowledge of the Greenthread Patents at least through the USPTO's citation of Greenthread's application as prior art during prosecution of Texas Instrument's U.S. Patent No. 8,278,683, entitled "Lateral Insulated Gate Bipolar Transistor," filed on August 6, 2009.

COUNT I: INFRINGEMENT OF U.S. PATENT NO. 8,421,195

36. Greenthread incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint and exhibits attached hereto as if fully set forth herein.

¹³ Multiple courts have upheld Greenthread's construction of the Greenthread Patents in related matters. In *Greenthread, LLC v. Samsung Electronics Co., Ltd. et al.*, Case No. 2:19-cv-00147-JRG (E.D. Tex.), the Eastern District of Texas Court adopted Greenthread's claim construction. *See* Dkt. 67. In *Greenthread, LLC v. Intel Corp., et al.*, Case No. 6:22-cv-00105-ADA (W.D. Tex), the Western District of Texas similarly issued a preliminary claim construction order adopting Greenthread's construction. *See* Dkt. 36-21 in *Greenthread, LLC v. Intel Corp.*, Case No. 3:22-cv-02001-JR (attaching as an exhibit the Western District of Texas's preliminary claim construction order in a status update before the District of Oregon). The claims in this matter against Intel were ultimately severed and transferred to Oregon, and the District of Oregon adopted the Western District of Texas' preliminary claim construction. *See* Dkt. 44 ("The Court also finds that the WDTX's preliminary constructions and summary judgment rulings are neither legally incorrect nor factually distinguishable. As a result, the Court adopts the WDTX's preliminary constructions and summary judgment rulings as its own. . ."). The Western District of Texas also denied Defendants' motions to dismiss and for summary judgment on similar grounds. *See* Dkt. 36-22 in *Greenthread, LLC v. Intel Corp.*, Case no. 3:22-cv-02001-JR (attaching as an exhibit the Western District of Texas' denial of Defendants' motion for summary judgment); Dkt. 110 in *Greenthread LLC v. Intel Corp.*, Case No. 6:22-cv-00105-ADA (W.D. Tex). The District of Oregon similarly adopted these rulings. *See* Dkt. 44 in *Greenthread, LLC v. Intel Corp.*, Case no. 3:22-cv-02001-JR.

37. The following allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Texas Instruments Accused Products. Greenthread reserves the right to modify this description, including, for example, on the basis of information about the Texas Instruments Accused Products that it obtains during discovery.

38. Defendant's infringement has damaged and continues to damage Greenthread in an amount yet to be determined, of at least a reasonable royalty.

39. As alleged above and in Exhibit 8, the products analyzed in Exhibit 8 meet each and every one of the claim limitations of at least one claim of the '195 Patent.

40. As alleged above, the products analyzed in Exhibit 8 are exemplary of the Texas Instruments Accused Products.

41. As alleged above, Defendant has infringed and continue to infringe at least one claim of the '195 Patent by making, using, offering to sell, selling within the United States, and/or importing into the United States Texas Instruments Accused Products. As alleged above, Defendant has and continues to infringe at least one claim of the '195 Patent by making, using, offering to sell, selling within the United States, and/or importing into the United States Texas Instruments Accused Products. Defendant's infringement is and continues to be willful.

42. Defendant's infringement has damaged and continues to damage Greenthread in an amount yet to be determined, of at least a reasonable royalty.

COUNT II: INFRINGEMENT OF U.S. PATENT NO. 9,190,502

43. Greenthread incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint and exhibits attached hereto as if fully set forth herein.

44. The following allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Texas Instruments Accused Products.

Greenthread reserves the right to modify this description, including, for example, on the basis of information about the Texas Instruments Accused Products that it obtains during discovery.

45. As alleged above and in Exhibit 8, the products analyzed in Exhibit 8 meet each and every one of the claim limitations of at least one claim of the '502 Patent.

46. As alleged above, the products analyzed in Exhibit 8 are exemplary of the Texas Instruments Accused Products.

47. As alleged above, Defendant has infringed and continues to infringe at least one claim of the '502 Patent by making, using, offering to sell, selling within the United States, and/or importing into the United States Texas Instruments Accused Products. Defendant's infringement is and continues to be willful.

48. Defendant's infringement has damaged and continues to damage Greenthread in an amount yet to be determined, of at least a reasonable royalty.

COUNT III: INFRINGEMENT OF U.S. PATENT NO. 10,510,842

49. Greenthread incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint and exhibits attached hereto as if fully set forth herein.

50. The following allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Texas Instruments Accused Products. Greenthread reserves the right to modify this description, including, for example, on the basis of information about the Texas Instruments Accused Products that it obtains during discovery.

51. As alleged above and in Exhibits 8, the products analyzed in Exhibit 8 meet each and every one of the claim limitations of at least one claim of the '842 Patent.

52. As alleged above, the products analyzed in Exhibit 8 are exemplary of the Texas Instruments Accused Products.

53. As alleged above, Defendants have infringed and continue to infringe at least one claim of the '842 Patent by making, using, offering to sell, selling within the United States, and/or importing into the United States Texas Instruments Accused Products. Defendant's infringement is and continues to be willful.

54. Defendants' infringement has damaged and continues to damage Greenthread in an amount yet to be determined, of at least a reasonable royalty.

COUNT IV: INFRINGEMENT OF U.S. PATENT NO. 10,734,481

55. Greenthread incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint and exhibits attached hereto as if fully set forth herein.

56. The following allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Texas Instruments Accused Products. Greenthread reserves the right to modify this description, including, for example, on the basis of information about the Texas Instruments Accused Products that it obtains during discovery.

57. As alleged above and in Exhibits 8, the products analyzed in Exhibit 8 meet each and every one of the claim limitations of at least one claim of the '481 Patent.

58. As alleged above, the products analyzed in Exhibit 8 are exemplary of the Texas Instruments Accused Products.

59. As alleged above, Defendant has infringed and continue to infringe at least one claim of the '481 Patent by making, using, offering to sell, selling within the United States, and/or importing into the United States Texas Instruments Accused Products. Defendant's infringement is and continues to be willful.

60. Defendant's infringement has damaged and continues to damage Greenthread in an amount yet to be determined, of at least a reasonable royalty.

COUNT V: INFRINGEMENT OF U.S. PATENT NO. 11,121,222

61. Greenthread incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint and exhibits attached hereto as if fully set forth herein.

62. The following allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Texas Instruments Accused Products. Greenthread reserves the right to modify this description, including, for example, on the basis of information about the Texas Instruments Accused Products that it obtains during discovery.

63. As alleged above and in Exhibit 8, the products analyzed in Exhibit 8 meet each and every one of the claim limitations of at least one claim of the '222 Patent.

64. As alleged above, the products analyzed in Exhibit 8 are exemplary of the Texas Instruments Accused Products.

65. As alleged above, Defendant has infringed and continues to infringe at least one claim of the '222 Patent by making, using, offering to sell, selling within the United States, and/or importing into the United States Texas Instruments Accused Products.

66. Defendant's infringement has damaged and continues to damage Greenthread in an amount yet to be determined, of at least a reasonable royalty.

COUNT VI: INFRINGEMENT OF U.S. PATENT NO. 11,316,014

67. Greenthread incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint and exhibits attached hereto as if fully set forth herein.

68. The following allegations are based on publicly available information and a reasonable investigation of the structure and operation of the Texas Instruments Accused Products. Greenthread reserves the right to modify this description, including, for example, on the basis of information about the Texas Instruments Accused Products that it obtains during discovery.

69. As alleged above and in Exhibits 8, the products analyzed in Exhibit 8 meet each and every one of the claim limitations of at least one claim of the '014 Patent.

70. As alleged above, the products analyzed in Exhibit 8 are exemplary of the Texas Instruments Accused Products.

71. As alleged above, Defendant has infringed and continue to infringe at least one claim of the '014 Patent by making, using, offering to sell, selling within the United States, and/or importing into the United States Texas Instruments Accused Products. Defendant's infringement is and continues to be willful.

72. Defendant's infringement has damaged and continues to damage Greenthread in an amount yet to be determined, of at least a reasonable royalty.

DAMAGES

73. As a result of Defendant's acts of infringement, Greenthread has suffered and continues to suffer actual and consequential damages. However, Greenthread does not yet know the full extent of the infringement and the amount of damages cannot be ascertained except through discovery and special accounting. To the fullest extent permitted by law, Greenthread seeks recovery of damages at least for reasonable royalties, unjust enrichment, and benefits received by Defendant as a result of using the patented technology. Greenthread further seeks any other damages to which Greenthread is entitled under law or in equity.

DEMAND FOR JURY TRIAL

74. Greenthread hereby demands a jury trial for all issues so triable.

PRAYER FOR RELIEF

WHEREFORE, Greenthread respectfully requests that this Court enter judgment in its

favor as follows:

A. That Judgment be entered that Defendant has infringed one or more claims of the Greenthread Patents, literally and under the doctrine of equivalents;

B. That, in accordance with 35 U.S.C. § 283, Defendant and all its affiliates, employees, agents, officers, directors, attorneys, successors, and assigns and all those acting on behalf of or in active concert or participation with any of them, be preliminarily and permanently enjoined from (1) infringing the Greenthread Patents and (2) making, using, selling, and offering for sale, or importing into the United States, the Texas Instruments Accused Products;

C. An award of damages sufficient to compensate Greenthread for Defendant's infringement under 35 U.S.C. § 284;

D. That the case be found exceptional under 35 U.S.C. § 285 and that Greenthread be awarded its reasonable attorneys' fees;

E. Costs and expenses in this action;

F. Damages for pre-issuance infringement under 35 U.S.C. § 154(d);

G. An award of prejudgment and post-judgment interest; and

H. Such other and further relief as the Court may deem just and proper.

Dated: April 6, 2023.

McKOOL SMITH, P.C.

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***ATTORNEYS FOR PLAINTIFF
GREENTHREAD, LLC***

EXHIBIT 1



US008421195B2

(12) **United States Patent**
Rao

(10) **Patent No.:** **US 8,421,195 B2**
(45) **Date of Patent:** **Apr. 16, 2013**

(54) **SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS**

(76) Inventor: **G. R. Mohan Rao**, McKinney, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **11/622,496**

(22) Filed: **Jan. 12, 2007**

(65) **Prior Publication Data**

US 2007/0158790 A1 Jul. 12, 2007

Related U.S. Application Data

(62) Division of application No. 10/934,915, filed on Sep. 3, 2004, now abandoned.

(51) **Int. Cl.**
H01L 21/02 (2006.01)

(52) **U.S. Cl.**
USPC **257/655**; 257/611; 257/E33.048;
438/510

(58) **Field of Classification Search** 257/655,
257/269
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,160,985 A * 7/1979 Kamins et al. 257/443
4,481,522 A * 11/1984 Jastrzebski et al. 257/229
5,029,277 A * 7/1991 Kane 250/214 C
5,517,052 A * 5/1996 Ishaque 257/462
5,637,898 A * 6/1997 Baliga 257/330

6,831,292 B2 * 12/2004 Currie et al. 257/19
2002/0056883 A1 * 5/2002 Baliga 257/390
2002/0084430 A1 * 7/2002 Bamji et al. 250/559.05
2002/0093281 A1 * 7/2002 Cathey 313/336
2002/0102783 A1 * 8/2002 Fujimoto et al. 438/200
2002/0134419 A1 * 9/2002 Macris 136/204
2003/0042511 A1 * 3/2003 Rhodes 257/232
2006/0113592 A1 * 6/2006 Pendharkar et al. 257/335

OTHER PUBLICATIONS

A. S. Grove, Physics and Technology of Semiconductor Devices, John Wiley Sons, Inc., New York, Nov. 1967.

W. Murray Bullis and W. R. Runyan, Influence of Mobility and Lifetime Variations on Drift-Field Effects in Silicon-Junction Devices, IEEE Transactions on Electron Devices, vol. Ed-14, No. 2, Feb. 1967.

Berinder Brar et al., Herb's Bipolar Transistors, IEEE Transactions on Electron Devices, vol. 48, No. 11, Nov. 2001.

* cited by examiner

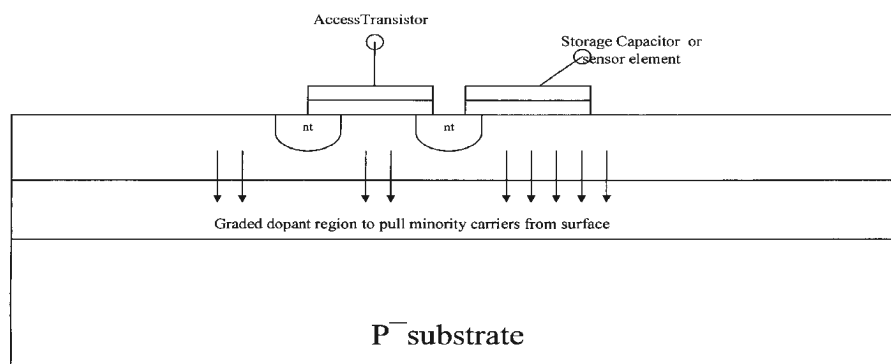
Primary Examiner — Ajay K Arora

(74) *Attorney, Agent, or Firm* — Eugene M. Cummings, P.C.

(57) **ABSTRACT**

Most semiconductor devices manufactured today, have uniform dopant concentration, either in the lateral or vertical device active (and isolation) regions. By grading the dopant concentration, the performance in various semiconductor devices can be significantly improved. Performance improvements can be obtained in application specific areas like increase in frequency of operation for digital logic, various power MOSFET and IGBT ICS, improvement in refresh time for DRAM's, decrease in programming time for nonvolatile memory, better visual quality including pixel resolution and color sensitivity for imaging ICs, better sensitivity for varactors in tunable filters, higher drive capabilities for JFET's, and a host of other applications.

14 Claims, 10 Drawing Sheets



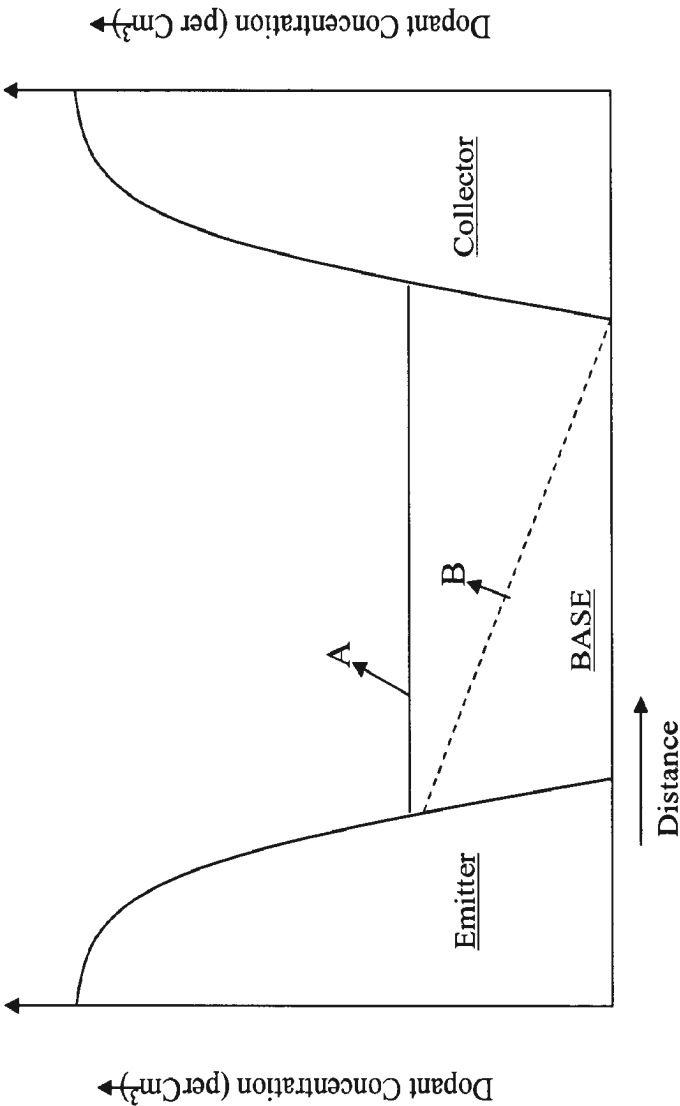


Figure 1 Prior Art

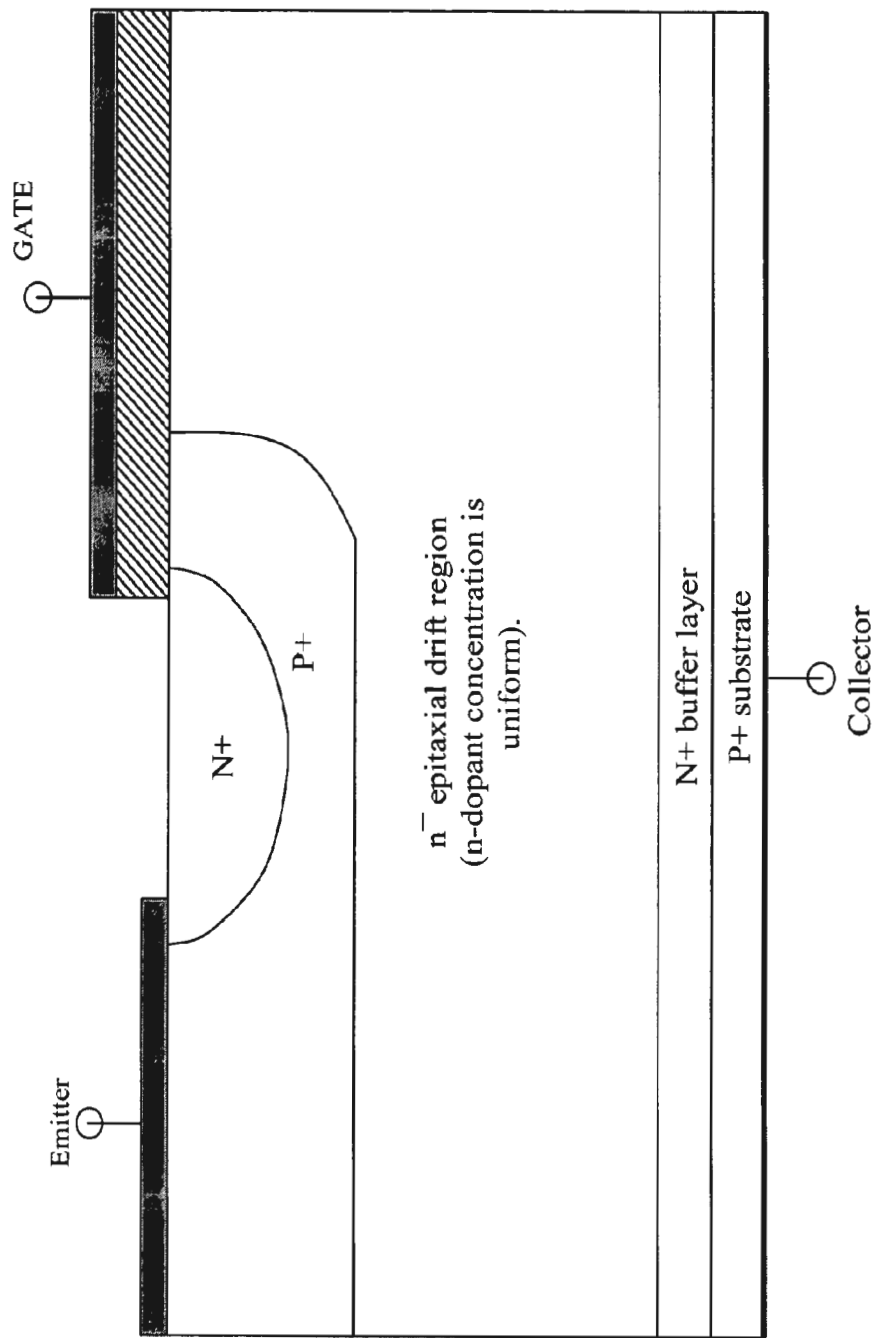


FIGURE 2 Prior art

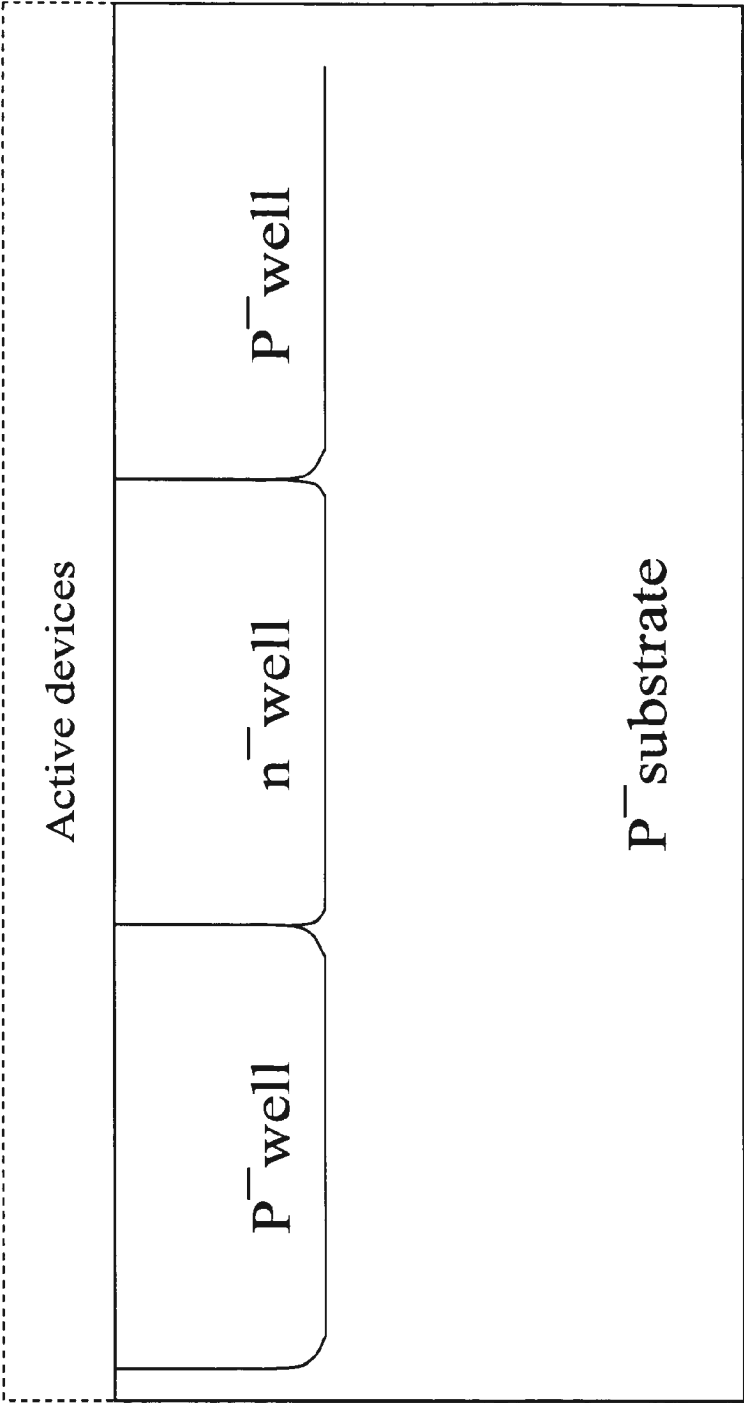


FIGURE 3(a) Prior art (Twin well CMOS) for a CMOS integrated circuit

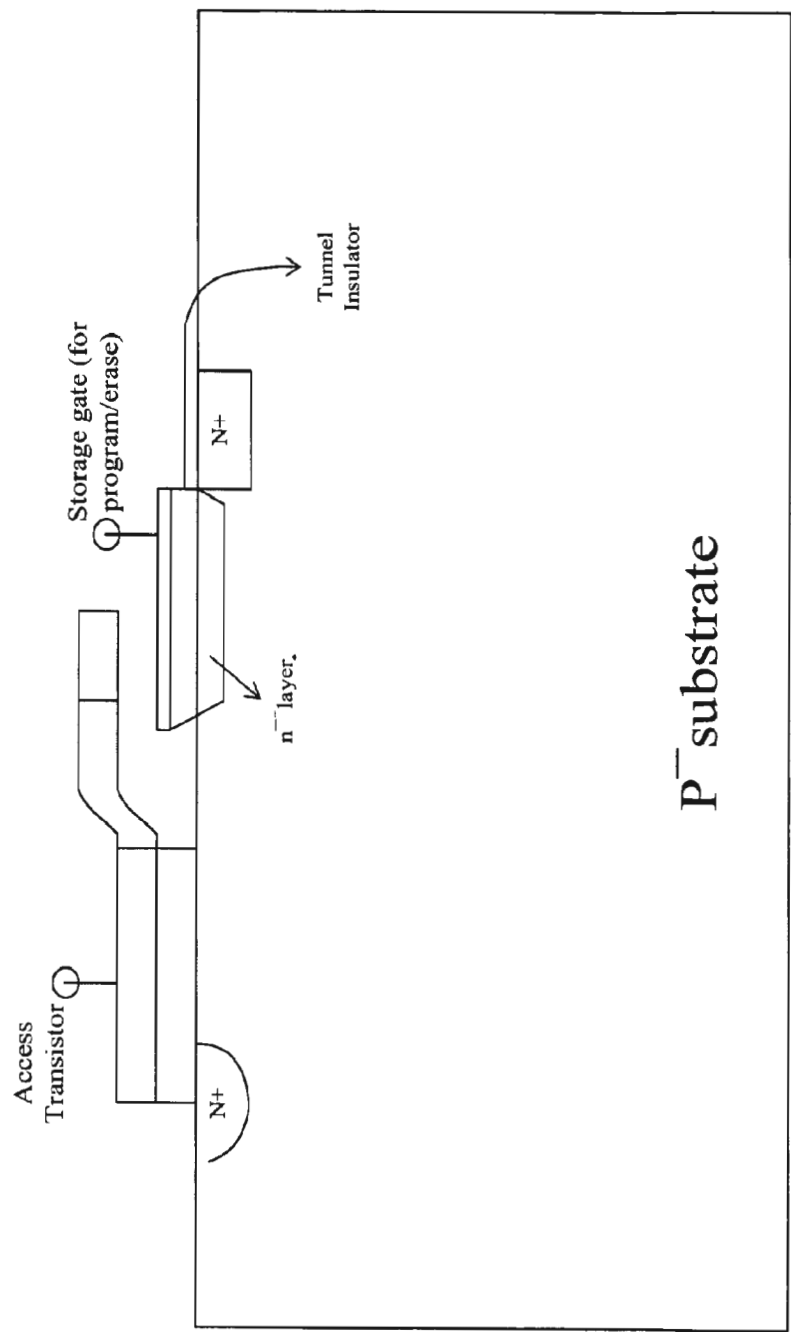


FIGURE 3(b) Prior art for a two-device EEPROM memory cell

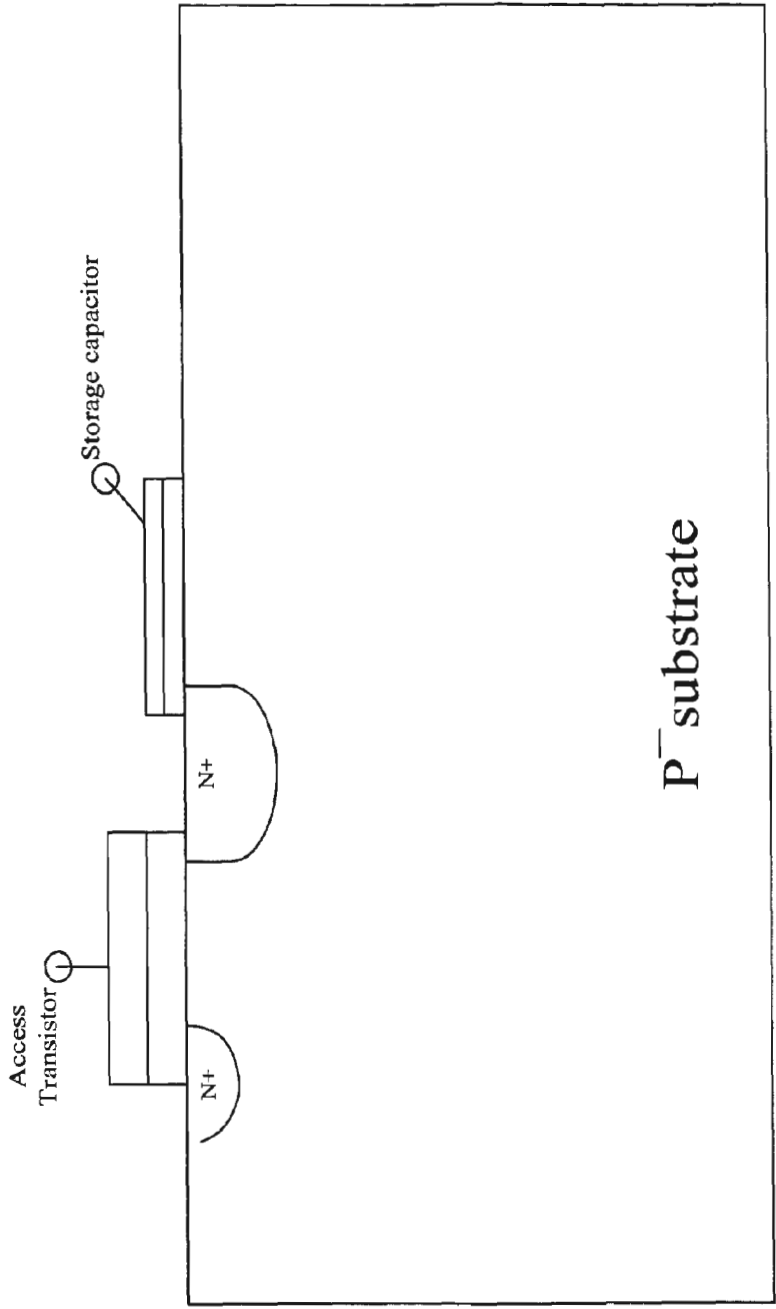


FIGURE 3(c) Prior art for a 1T-1C DRAM memory cell

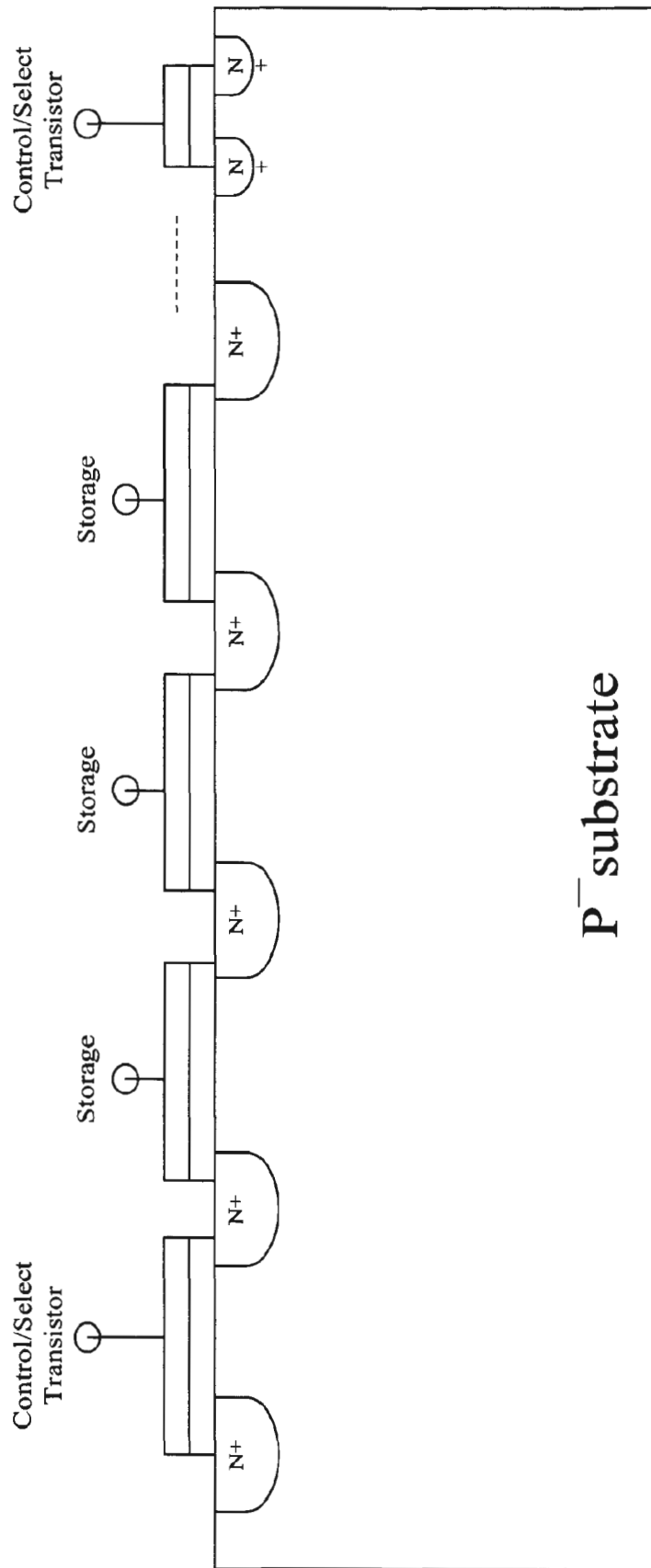


FIGURE 3(d) Prior art for a NAND flash memory cell

Note: Control/ Sect transistors have a single insulator - traditional MOS transistor.

Storage nodes have a stacked gate structure, typically with a floating gate and control gate comprising the stack.

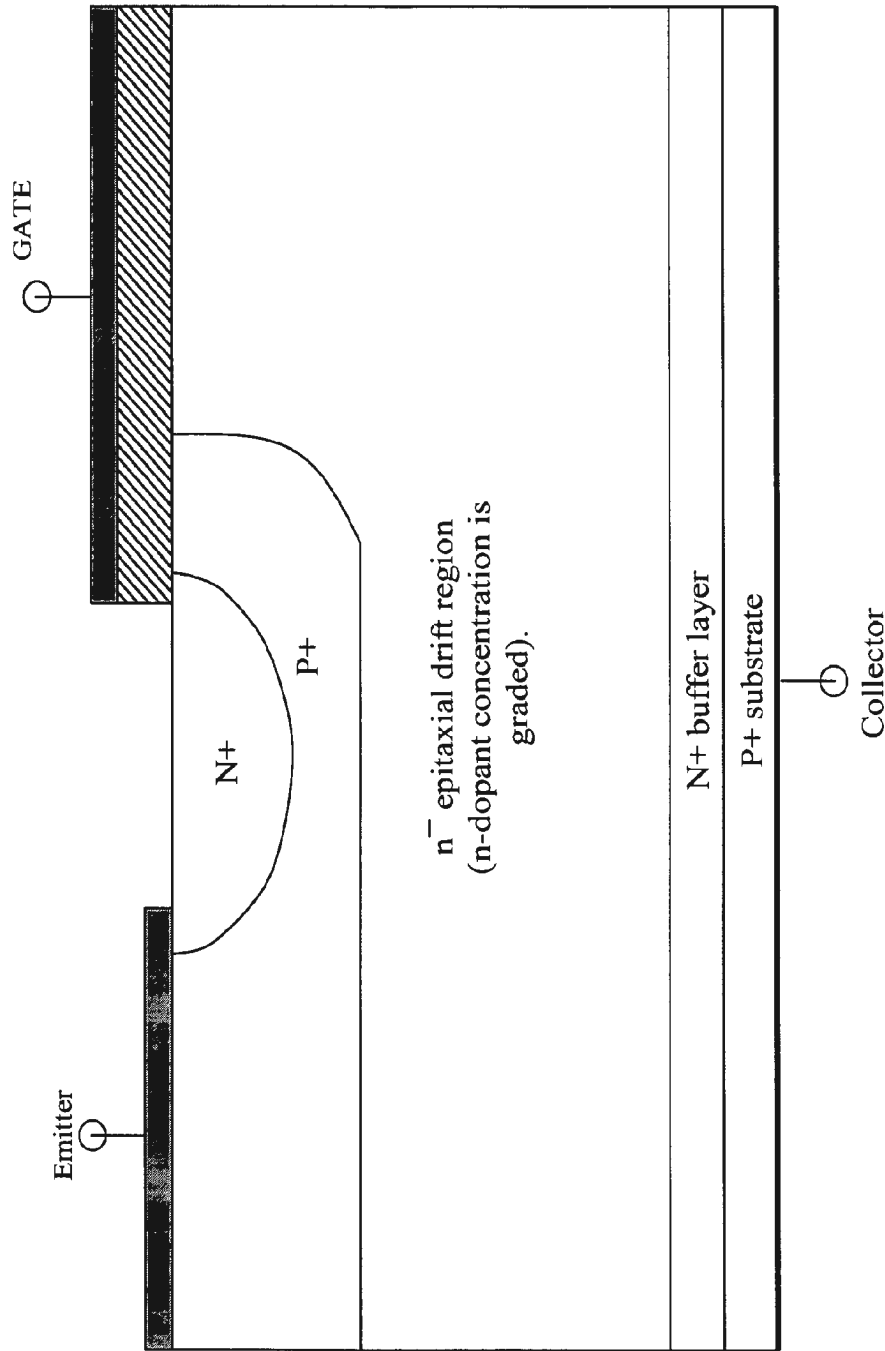


FIGURE 4 A dopant - concentration graded drift region in a IGBT

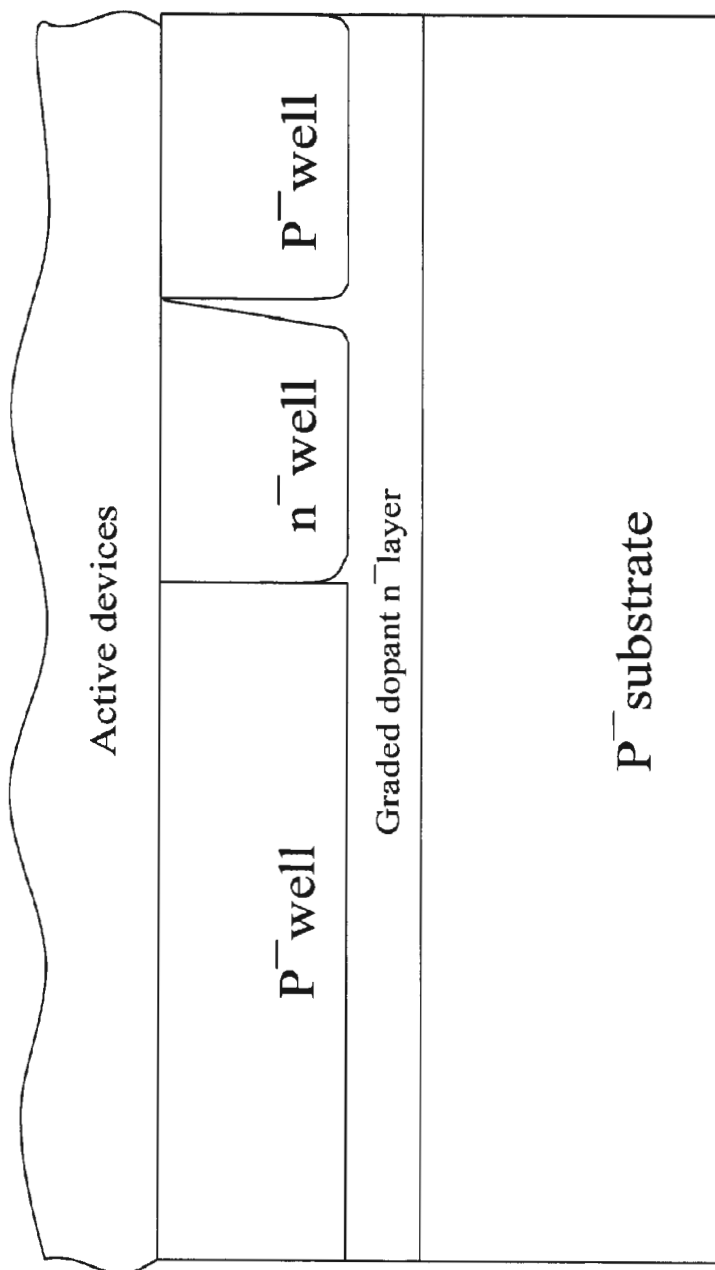


FIGURE 5(a) A CMOS Substrate for digital, mixed, signal, and sensors IC's

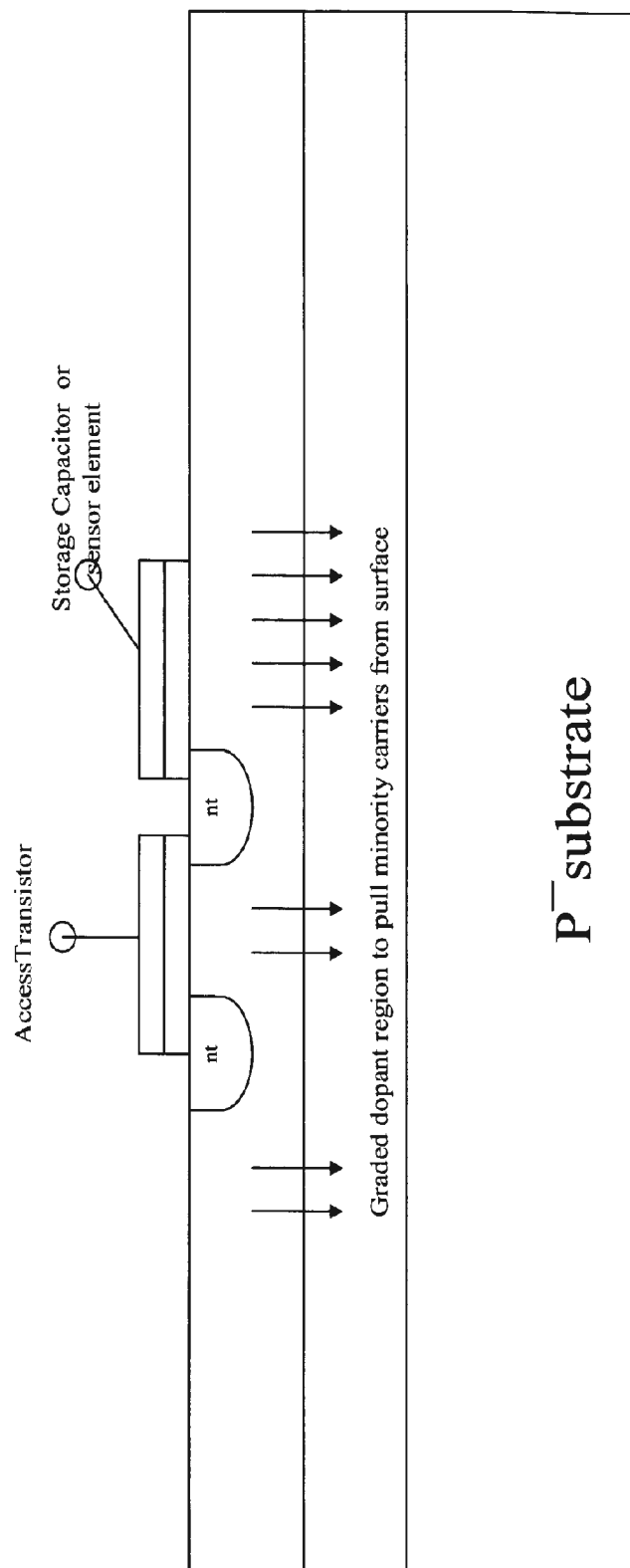


FIGURE 5(b) CMOS Substrate for a DRAM or image sensor, with one embodiment of the invention

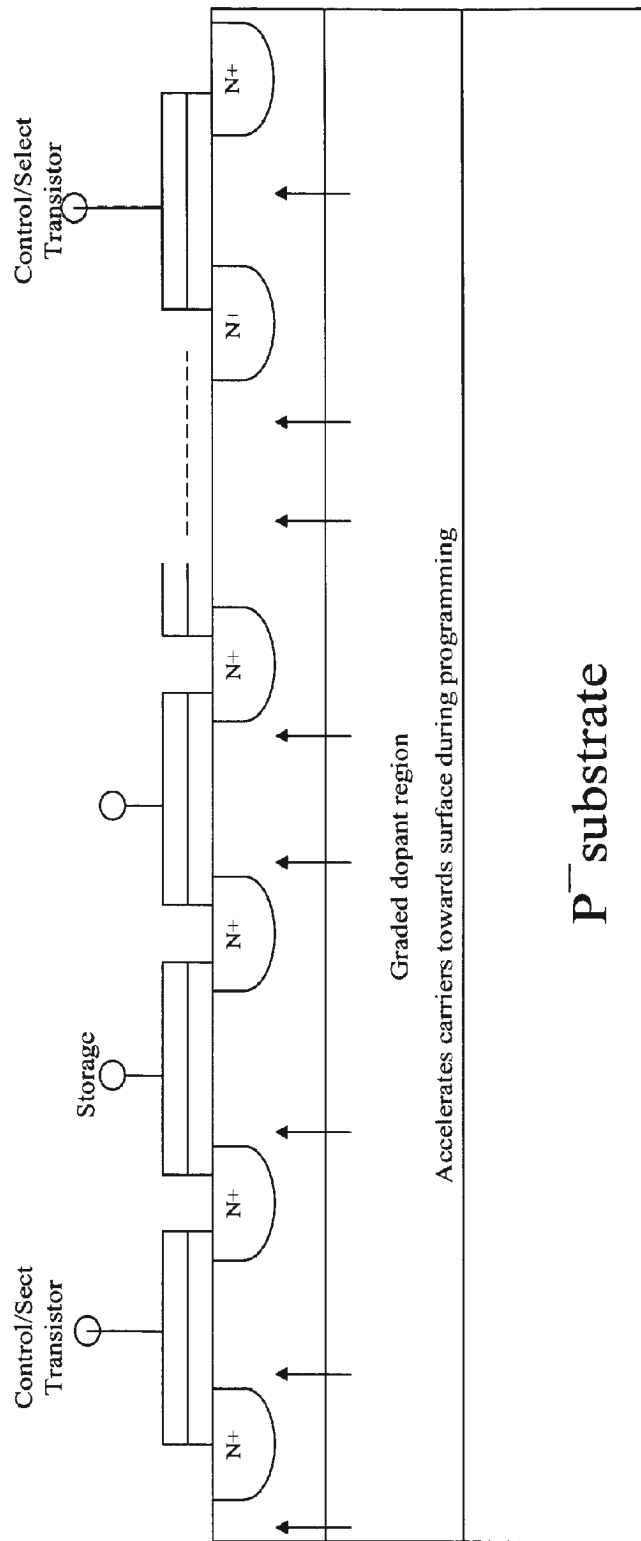


FIGURE 5(c) CMOS Substrate for a NAND flash device to improve programming times

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**SEMICONDUCTOR DEVICES WITH
GRADED DOPANT REGIONS****CROSS-REFERENCE TO RELATED
APPLICATION**

This application is a Divisional of U.S. application Ser. No. 10/934,915, filed on Sep. 3, 2004, now abandoned which application is incorporated herein by reference.

FIELD OF INVENTION

This present invention relates to all semiconductor devices and systems. Particularly it applies to diffused diodes, avalanche diodes, Schottky devices, power MOS transistors, JFET's, RF bipolar transistors, IGBTs (Insulated Gate Bipolar Transistors), varactors, digital VLSI, mixed signal circuits and sensor devices including camera ICs employing CCD (Charge Coupled Device) as well as CMOS technologies.

BACKGROUND OF INVENTION

Bipolar Junction transistors (BJT) are minority carrier devices as the principle device conduction mechanism. However, majority carriers also a small yet finite role in modulating the conductivity in BJTs. Consequently, both carriers (electrons and holes) play a role in the switching performance of BJTs. The maximum frequency of operation in BJTs is limited by the base transit time as well as the quick recombination of the majority carriers when the device is switched off (prior to beginning the next cycle). The dominant carrier mechanism in BJTs is carrier diffusion. Carrier drift current component is fairly small, especially in uniformly doped base BJTs. Efforts have been made in graded base transistors to create an 'aiding drift field', to enhance the diffusing minority carrier's speed from emitter to collector. However, most semiconductor devices, including various power MOSFETs (traditional, DMOS, lateral, vertical and a host of other configurations), IGBT's (Insulated Gated Base Transistors), still use a uniformly doped drift epitaxial region in the base. FIG. 1 shows the relative doping concentration versus distance in a BJT. FIG. 2 shows the uniformly doped epi region' in a IGBT. In contrast to BJTs, MOS devices are majority carrier devices for conduction. The conduction is channel dominated. The channel can be a surface in one plane in planar devices. The surface can also be on the sidewalls in a vertical device. Other device architectures to combine planar and vertical conduction are also possible. The maximum frequency of operation is dictated primarily by source-drain separation distance. Most MOS devices use a uniformly doped substrate (or a well region). When a MOSFET is optimally integrated with a BJT in a monolithic fashion, an IGBT results. The IGBT inherits the advantages of both MOSFET and BJT. It also brings new challenges because the required characteristics (electron transit and hole recombination as fast as possible in the case of an n-channel IGBT) require different dopant gradients either in the same layer at different positions, or at the interfaces of similar or dissimilar layers.

'Retrograde' wells have been attempted, with little success, to help improve soft error immunity in SRAM's and visual quality in imaging circuits. FIG. 3(a) shows a typical CMOS VLSI device employing a twin well substrate, on which active devices are subsequently fabricated. FIGS. 3(b), 3(c), and 3(d) illustrate device cross sections, as practiced today. 'Retrograde' and 'halo' wells have also been attempted to improve refresh time in DRAM's (dynamic random access memories), as well as, reducing dark current (background noise)

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and enhance RGB (Red, Green, Blue) color resolution in digital camera Ics. Most of these techniques either divert the minority carriers away from the active regions of critical charge storage nodes at the surface, or, increase minority carrier density locally as the particular application requires.

BRIEF DESCRIPTION OF DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. 1 illustrates the relative doping profiles of emitter, base, and collector, for the two most popular bipolar junction transistors: namely, A—uniform base, and B—graded base;

FIG. 2 illustrates the cross section of a commercial IGBT with a uniform epitaxial drift region (base);

FIGS. 3(a), 3(b), 3(c), 3(d) illustrate cross sections commonly used CMOS silicon substrate with two wells (one n-well in which p-channel transistors are subsequently fabricated, and, one p-well in which n-channel transistors are subsequently fabricated)—typical IC, EEPROM using tunnel insulator, DRAM and NAND flash;

FIG. 4 illustrates the cross section of a IGBT, using one embodiment of the invention described here, where the dopant is optimally graded in the epitaxial drift region; and

FIGS. 5(a), 5(b), 5(c) illustrate the cross sections of a MOS silicon substrate with two wells, and, an underlying layer using embodiments of the invention to improve performance in each application—VLSI logic, DRAM/image IC, nonvolatile memory IC.

DETAILED DESCRIPTION OF THE INVENTION

The relative doping concentrations of emitter and collector regions varies from 10^{18} to $10^{20}/\text{cm}^3$, where as the base region is 10^{14} to $10^{16}/\text{cm}^3$ depending on the desired characteristics of the BJT. In graded base p-n-p transistors, the donor dopant concentration may be 10 to 100x at the emitter-base junction, relative to the base-collector junction (1x). The gradient can be linear, quasi linear, exponential or complimentary error function. The relative slope of the donor concentration throughout the base, creates a suitable aiding drift electric field, to help the holes (p-n-p transistor) transverse from emitter to collector. Since the aiding drift field helps hole conduction, the current gain at a given frequency is enhanced, relative to a uniformly-doped-(base) BJT. The improvement in cut-off frequency (or, frequency at unity gain, f_T) can be as large as 2x-5x. Similar performance improvements are also applicable to n-p-n transistors.

As illustrated in FIG. 4, in one embodiment according to the invention, a donor gradient is established from the emitter-drift epitaxial base region junction of the punch-through IGBT, to the drift epitaxial base region—n' buffer layer boundary (electrons in this case are accelerated in their transit from emitter to collector). The 'average' base resistance is optimized, so that conductivity modulation and lifetime (for minority carriers) in base region are not compromised. By sweeping the carriers towards the n' buffer region two advantages are obtained—the frequency of operation (combination of t_{on} and t_{off} as is known in the IGBT commercial nomenclature) can be enhanced. More importantly, during t_{off} , holes can be recombined much quicker at the n' buffer layer, compared to a uniformly doped n' epitaxial drift region by establishing a different dopant gradient near the n+buffer layer. It should be noted that the drift region can also be a non-epitaxial silicon substrate. Epitaxy enhances lifetime, but epitaxy is

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not mandatory. Different layers of dopant regions can be transferred through wafer to wafer bonding (or other similar transfer mechanisms) for eventual device fabrication. The “reverse recovery time” for an IGBT is significantly improved due to the optimized graded dopant in the so called “drift region” as well as at the interfaces of the drift region. Graded dopants can also be implemented in the n+ buffer layer as well as other regions adjacent to the respective layers. Two important performance enhancements are the result of dopant gradients. For example, in an n-channel IGBT, electrons can be swept from source to drain rapidly, while at the same time holes can be recombined closer to the n+ buffer layer. This can improve t(on) and t(off) in the same device.

As illustrated in FIGS. 5(a), 5(b), 5(c), donor gradient is also of benefit to very large scale integrated circuits (VLSI)–VLSI logic, DRAM, nonvolatile memory like NAND flash. Spurious minority carriers can be generated by clock switching in digital VLSI logic and memory IC’S. These unwanted carriers can discharge dynamically-held ‘actively held high’ nodes. Statically held nodes (with V_{cc}) can not be affected, in most cases. Degradation of refresh time in DRAM’s is one of the results, because the capacitor holds charge dynamically. Similarly, degradation of CMOS digital images, in digital imaging IC’s is another result of the havoc caused by minority carriers. Pixel and color resolution can be significantly enhanced in imaging IC’s with the embodiments described here. Creating ‘Sub Terrain’ recombination centers underneath the wells (gold doping, platinum doping) as is done in some high-voltage diodes is not practical for VLSI circuits. Hence, a novel technique has been described here by creating a drift field to sweep these unwanted minority carriers into the substrate as quickly as possible, from the active circuitry at the surface. In a preferred embodiment, the subterrain n-layer has a graded donor concentration to sweep the minority carriers deep into the substrate. One or more of such layers can also be implemented through wafer to wafer bonding or similar “transfer” mechanisms. This n-layer can be a deeply-implanted layer. It can also be an epitaxial layer. The n-well and p-well also can be graded or retrograded in dopants, as desired, to sweep those carriers away from the surface as well. The graded dopant can also be implemented in surface channel MOS devices to accelerate majority carriers towards the drain. In nonvolatile memory devices, to decrease programming time, carriers should be accelerated towards the surface when programming of memory cells is executed. The graded dopant can also be used to fabricate superior Junction field-effect transistors where the “channel pinchoff” is controlled by a graded channel instead of a uniformly doped channel (as practiced in prior art).

One of ordinary skill and familiarity in the art will recognize that the concepts taught herein can be customized and tailored to a particular application in many advantageous ways. For instance, minority carriers can be channeled to the surface, to aid programming in nonvolatile memory devices (NOR, NAND, multivalued-cell). Moreover, single well, as well triple-well CMOS fabrication techniques can also be optimized to incorporate these embodiments, individually and collectively. Any modifications of such embodiments (described here) fall within the spirit and scope of the invention. Hence, they fall within the scope of the claims described below

Although the invention has been described with reference to specific embodiments, these descriptions are not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as alternative embodiments of the invention will become apparent to persons skilled in the art upon reference to the description of the invention. It

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should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

It is therefore, contemplated that the claims will cover any such modifications or embodiments that fall within the true scope of the invention.

What is claimed is:

1. A CMOS Semiconductor device comprising:

a surface layer;

a substrate;

an active region including a source and a drain, disposed on one surface of said surface layer;

a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and

at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

2. The CMOS Semiconductor device of claim 1, wherein the said drift layer is a deeply-implanted layer.

3. The CMOS Semiconductor device of claim 1, wherein said drift layer is an epitaxial layer.

4. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a linear gradient.

5. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a quasi-linear gradient.

6. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows an exponential gradient.

7. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a complimentary error function gradient.

8. A CMOS Semiconductor device comprising:

a surface layer;

a substrate;

an active region including a source and a drain, disposed on one surface of said surface layer,

a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said substrate to said surface layer; and

at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said substrate TO SAID SURFACE LAYER.

9. The CMOS Semiconductor device of claim 8, wherein said drift layer is deeply-implanted layer.

10. The CMOS Semiconductor device of claim 8, wherein said drift layer is an epitaxial layer.

11. The CMOS Semiconductor device of claim 8, wherein said graded concentration follows a linear gradient.

12. The CMOS Semiconductor device of claim 8, wherein said graded concentration follows a quasi-linear gradient.

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13. The CMOS Semiconductor device of claim 8, wherein said graded concentration follows a exponential gradient.

14. The CMOS Semiconductor device of claim 8, wherein said graded concentration follows a complimentary error function gradient.

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* * * * *

EXHIBIT 2



US009190502B2

(12) **United States Patent**
Rao

(10) **Patent No.:** **US 9,190,502 B2**

(45) **Date of Patent:** ***Nov. 17, 2015**

(54) **SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS**

(71) Applicant: **G. R. Mohan Rao**, Allen, TX (US)

(72) Inventor: **G. R. Mohan Rao**, Allen, TX (US)

(73) Assignee: **Greenthread, LLC**, Dallas, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **14/515,584**

(22) Filed: **Oct. 16, 2014**

(65) **Prior Publication Data**

US 2015/0035004 A1 Feb. 5, 2015

Related U.S. Application Data

(60) Continuation of application No. 13/854,319, filed on Apr. 1, 2013, now abandoned, which is a continuation of application No. 11/622,496, filed on Jan. 12, 2007, now Pat. No. 8,421,195, which is a division of application No. 10/934,915, filed on Sep. 3, 2004, now abandoned.

(51) **Int. Cl.**

H01L 21/02 (2006.01)
H01L 29/739 (2006.01)
H01L 27/115 (2006.01)
H01L 29/36 (2006.01)
H01L 27/02 (2006.01)
H01L 27/108 (2006.01)

(52) **U.S. Cl.**

CPC **H01L 29/7395** (2013.01); **H01L 27/11521** (2013.01); **H01L 27/11524** (2013.01); **H01L 29/36** (2013.01); **H01L 27/0214** (2013.01); **H01L 27/10844** (2013.01)

(58) **Field of Classification Search**

CPC H01L 29/7395
USPC 438/37
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,160,985 A * 7/1979 Kamins et al. 257/443
2001/0040622 A1 * 11/2001 Maruyama 348/64
2003/0030488 A1 * 2/2003 Huetting et al. 330/57

* cited by examiner

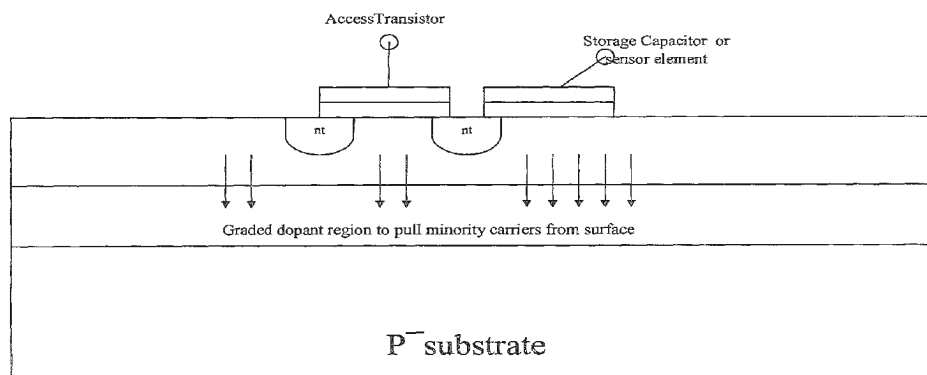
Primary Examiner — Ajay K Arora

(74) *Attorney, Agent, or Firm* — Howison & Arnott, LLP

(57) **ABSTRACT**

Most semiconductor devices manufactured today, have uniform dopant concentration, either in the lateral or vertical device active (and isolation) regions. By grading the dopant concentration, the performance in various semiconductor devices can be significantly improved. Performance improvements can be obtained in application specific areas like increase in frequency of operation for digital logic, various power MOSFET and IGBT ICS, improvement in refresh time for DRAM's, decrease in programming time for nonvolatile memory, better visual quality including pixel resolution and color sensitivity for imaging ICs, better sensitivity for varactors in tunable filters, higher drive capabilities for JFET's, and a host of other applications.

12 Claims, 10 Drawing Sheets



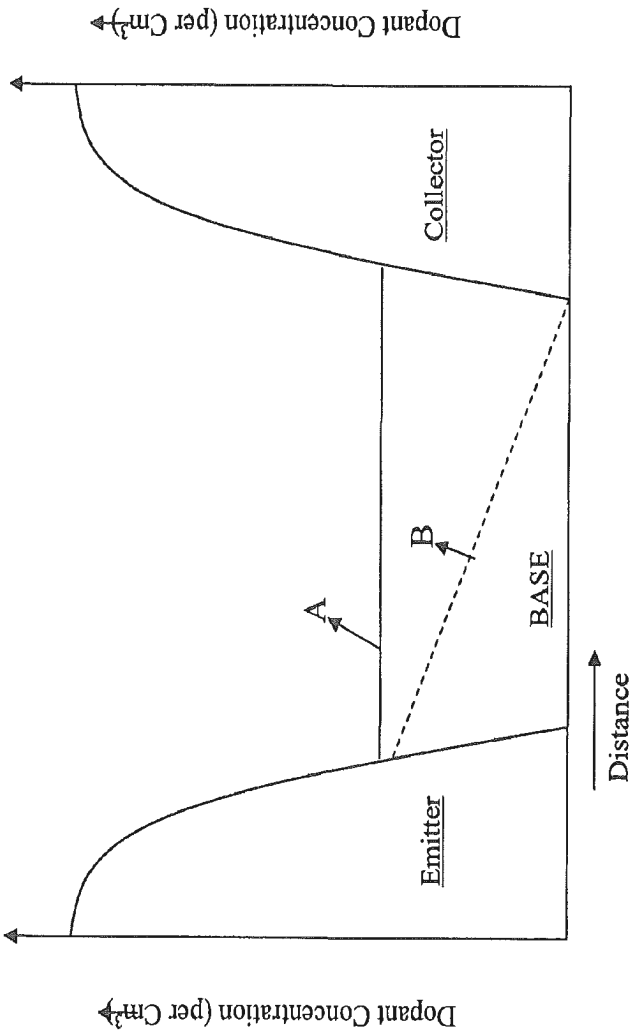


Figure 1 Prior Art

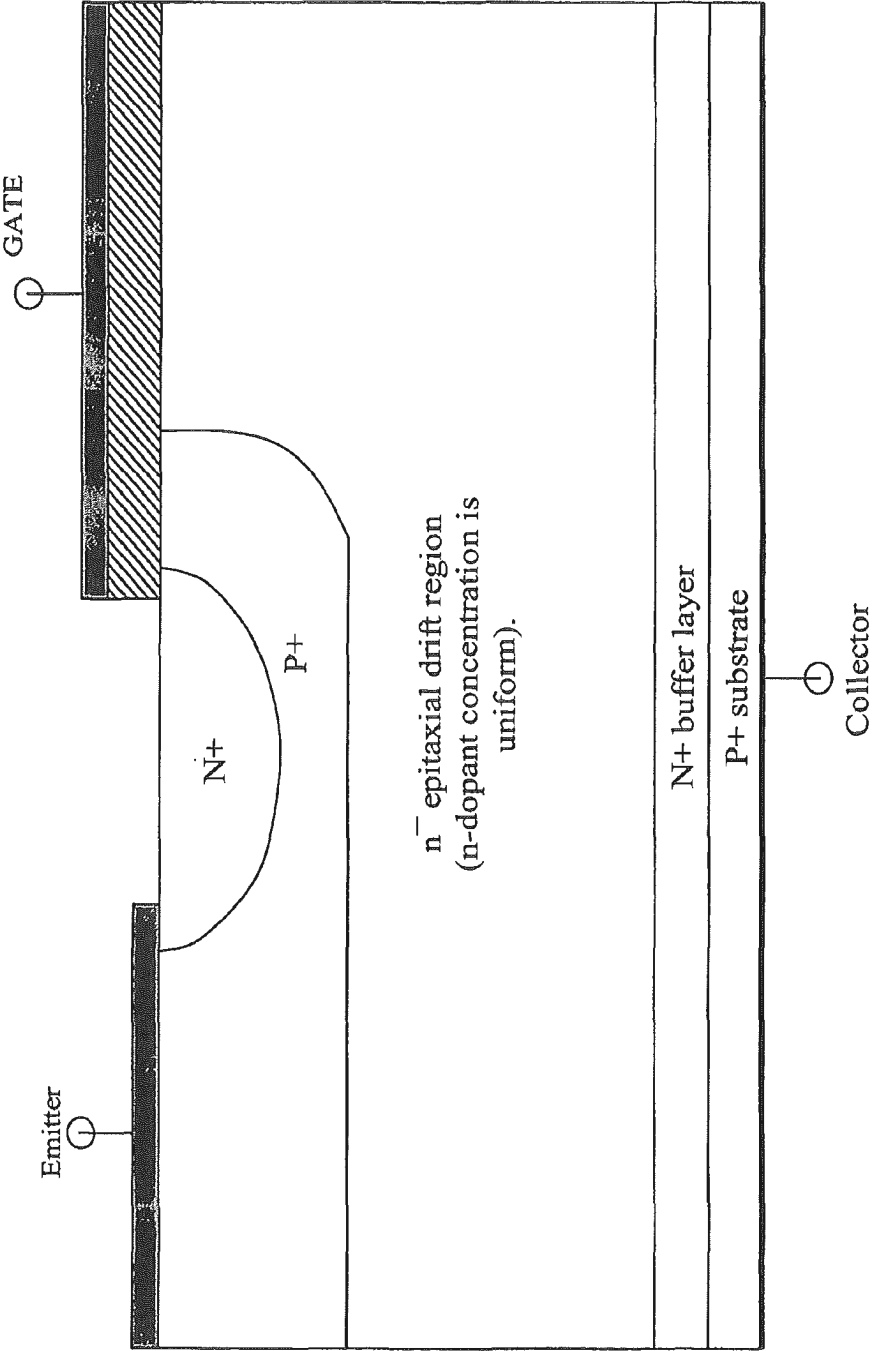


FIGURE 2 Prior art

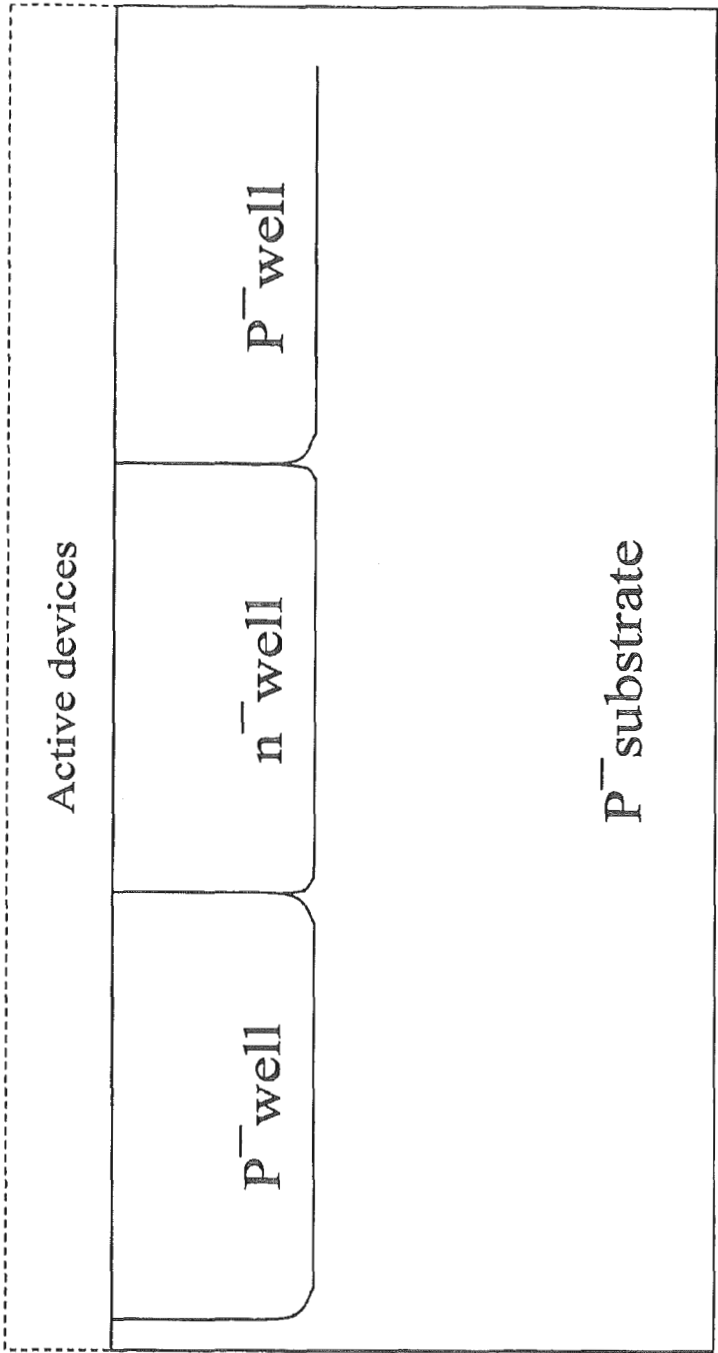


FIGURE 3(a) Prior art (Twin well CMOS) for a CMOS integrated circuit

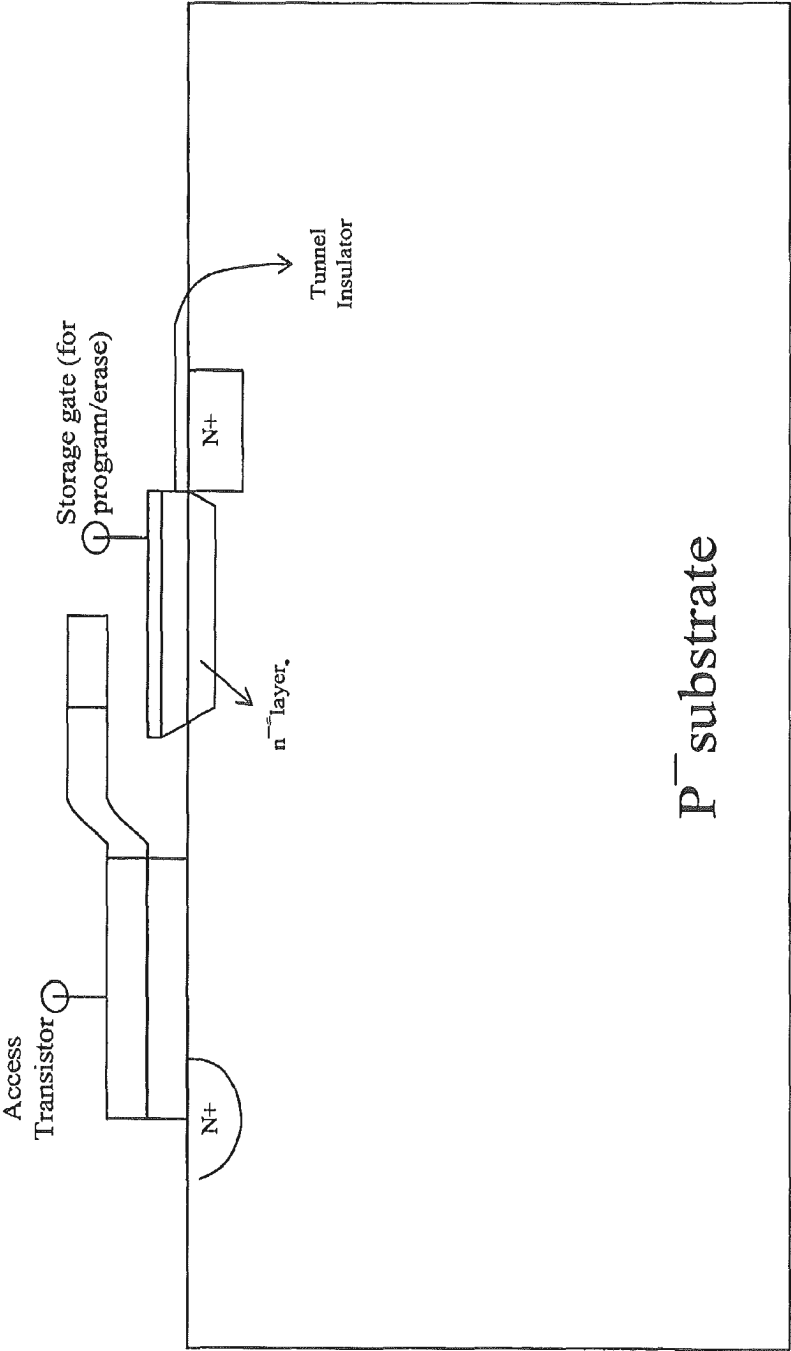


FIGURE 3(b) Prior art for a two-device EEPROM memory cell

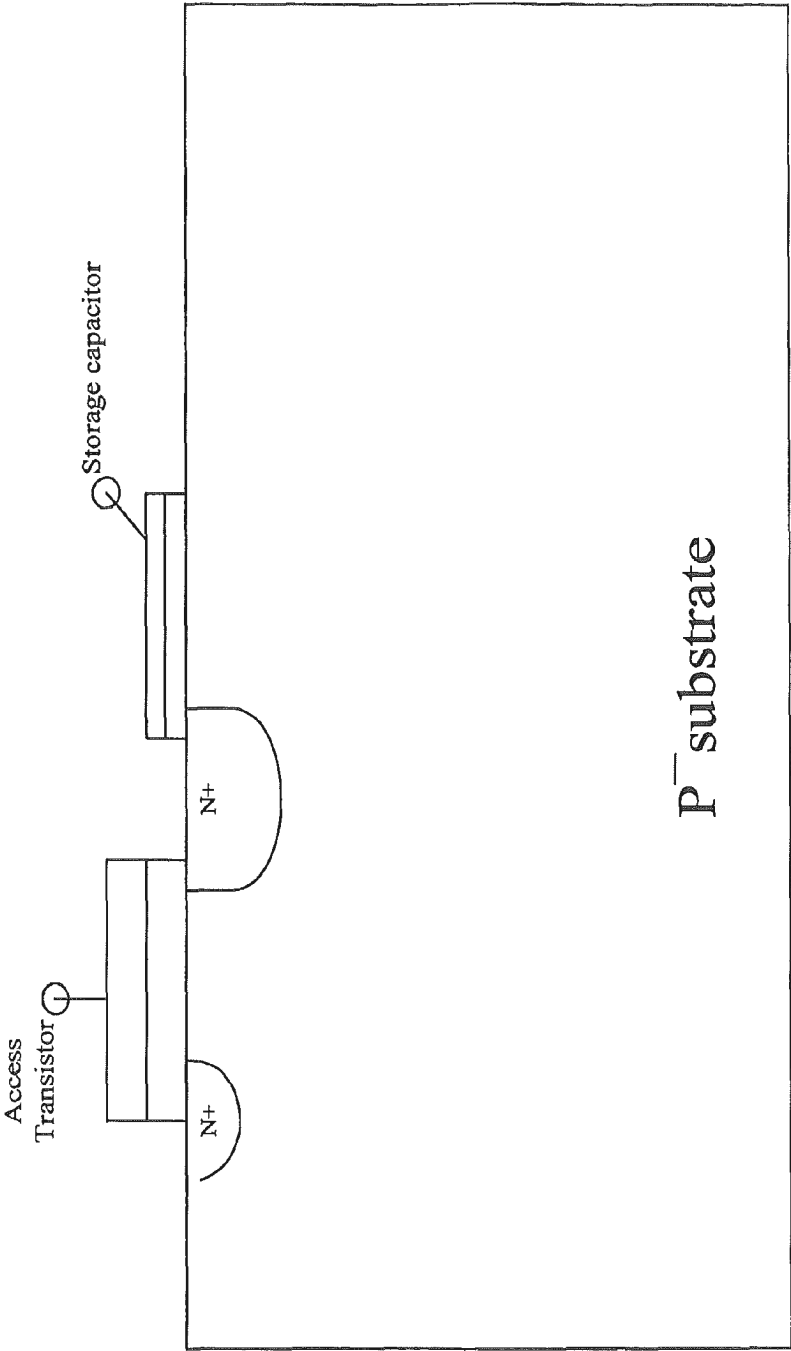


FIGURE 3(c) Prior art for a 1T-1C DRAM memory cell

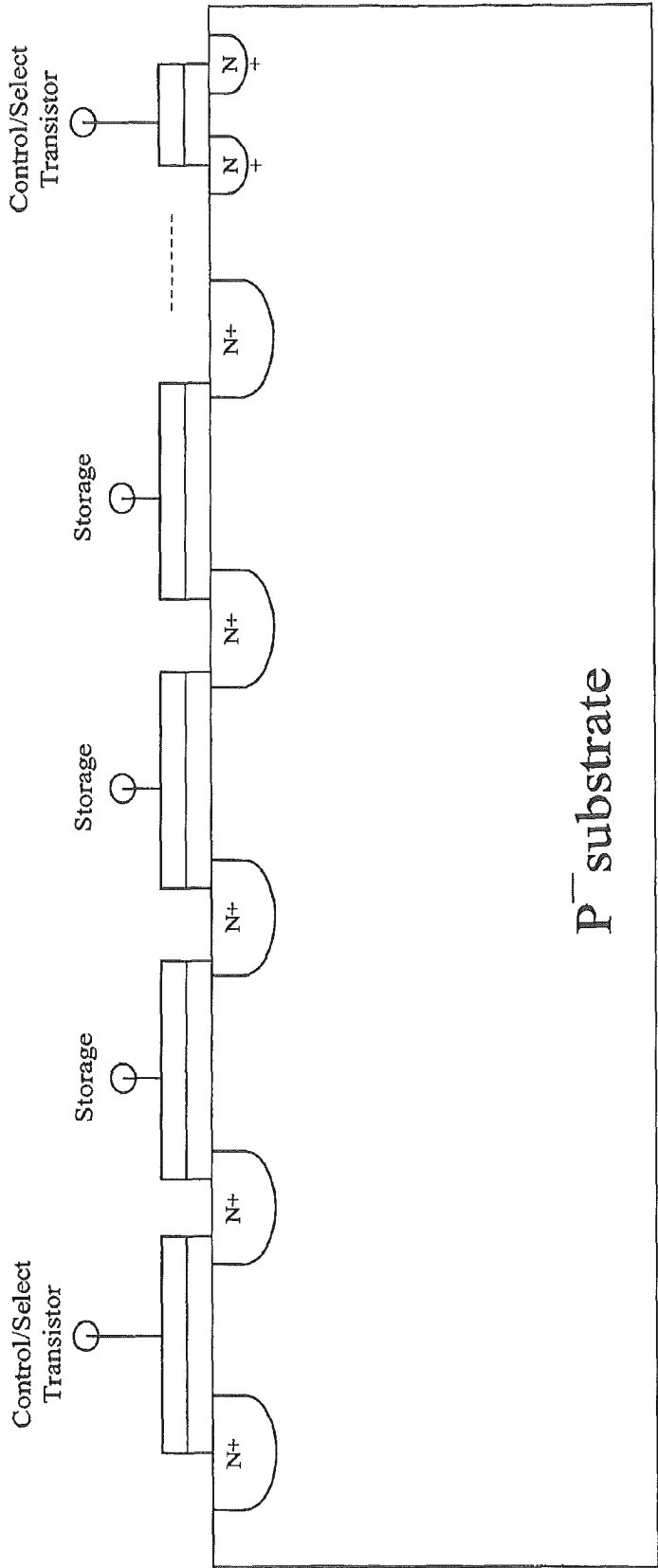


FIGURE 3(d) Prior art for a NAND flash memory cell

Note: Control/ Sect transistors have a single insulator - traditional MOS transistor.
Storage nodes have a stacked gate structure, typically with a floating gate and control gate comprising the stack.

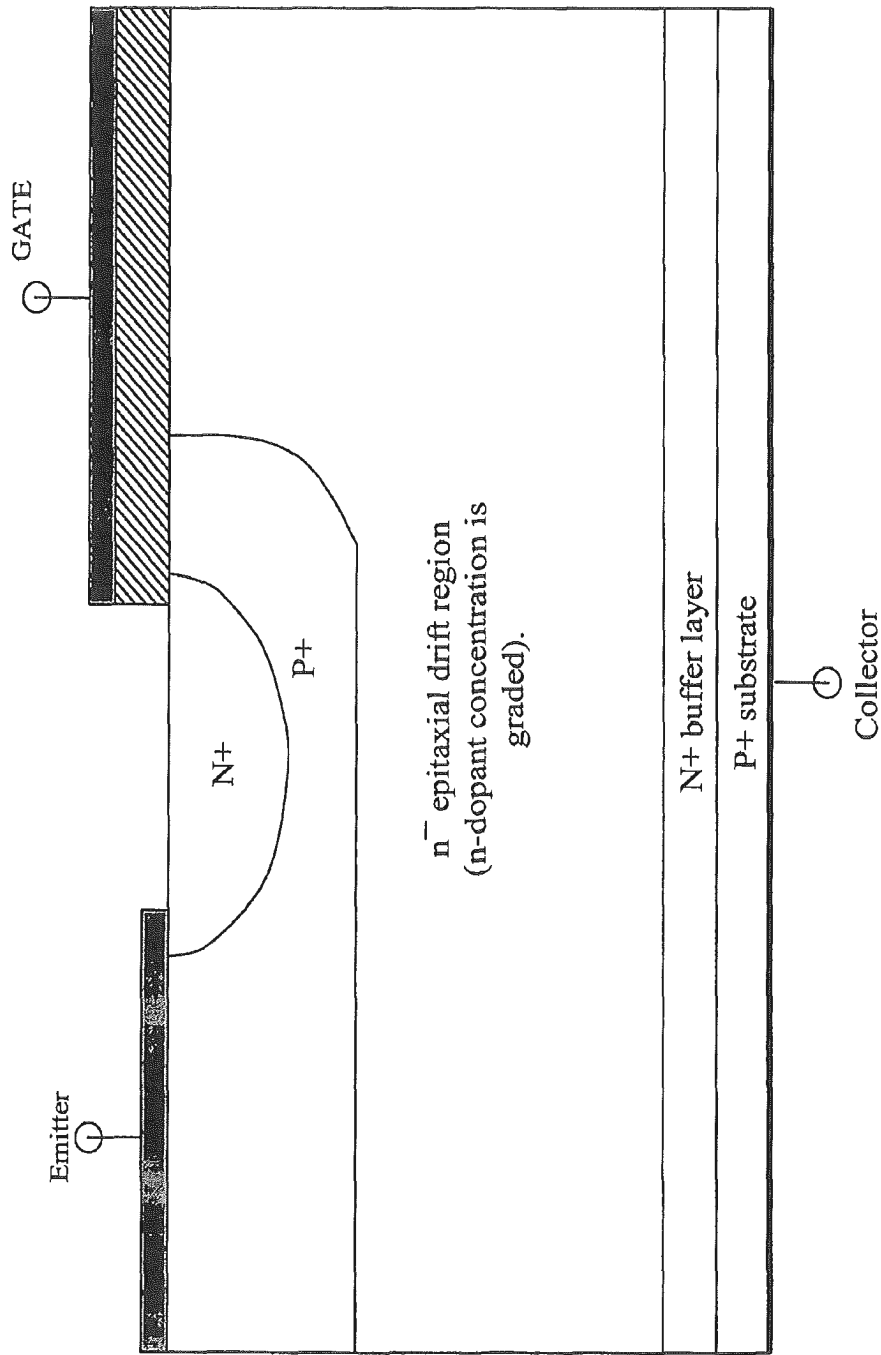


FIGURE 4 A dopant - concentration graded drift region in a IGBT

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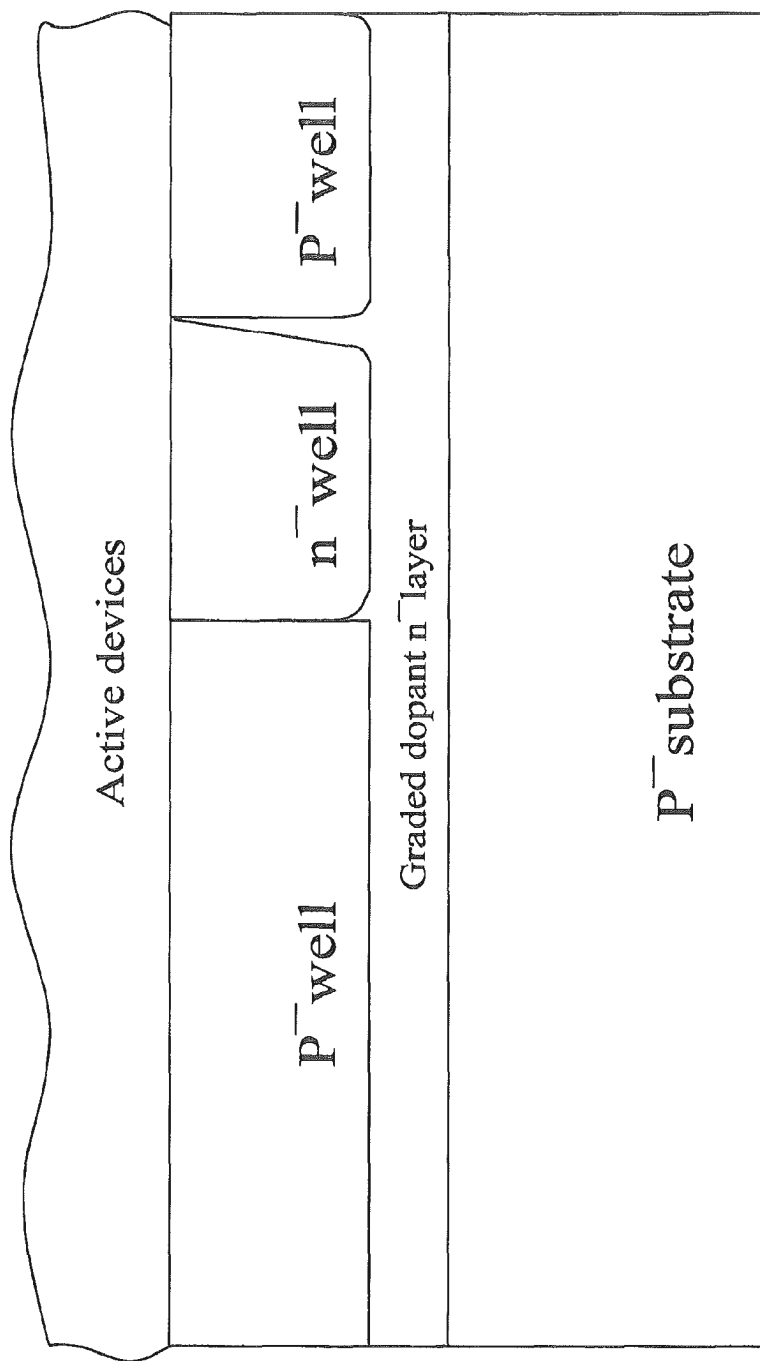


FIGURE 5(a) A CMOS Substrate for digital, mixed, signal, and sensors IC's

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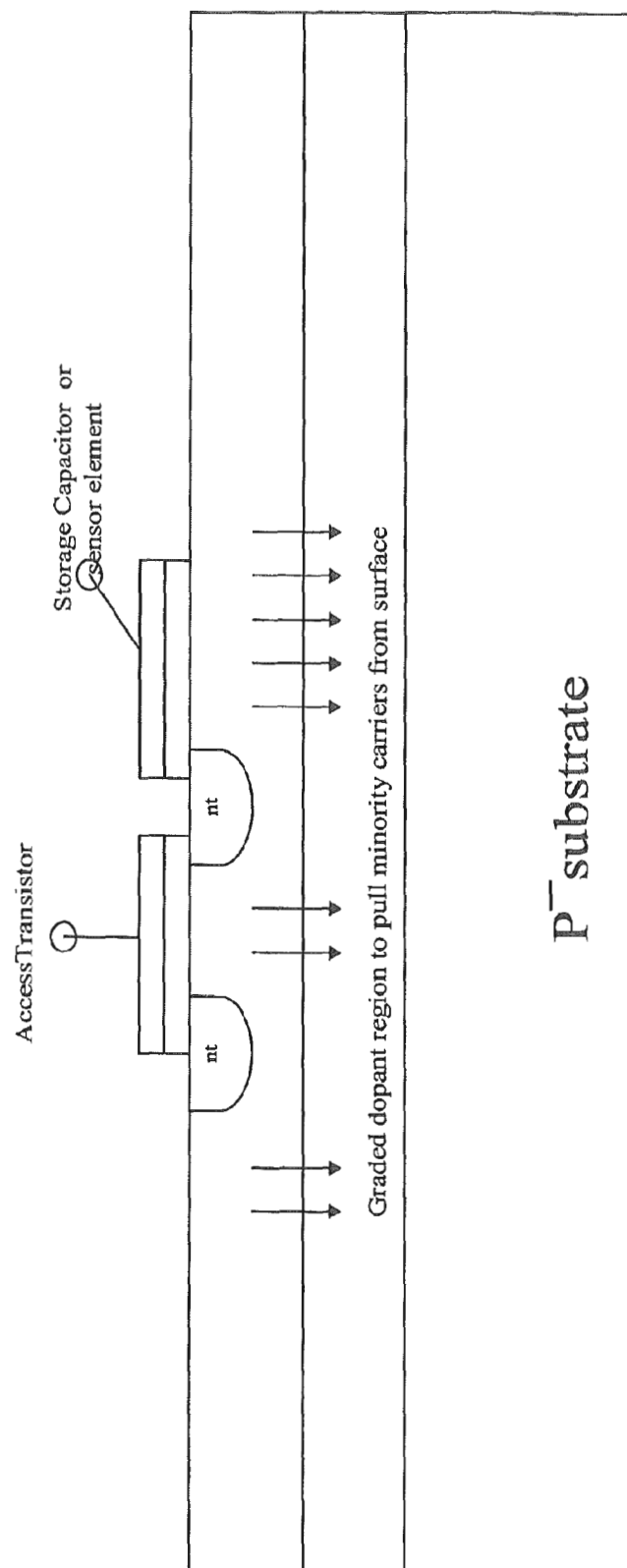


FIGURE 5(b) CMOS Substrate for a DRAM or image sensor, with one embodiment of the invention

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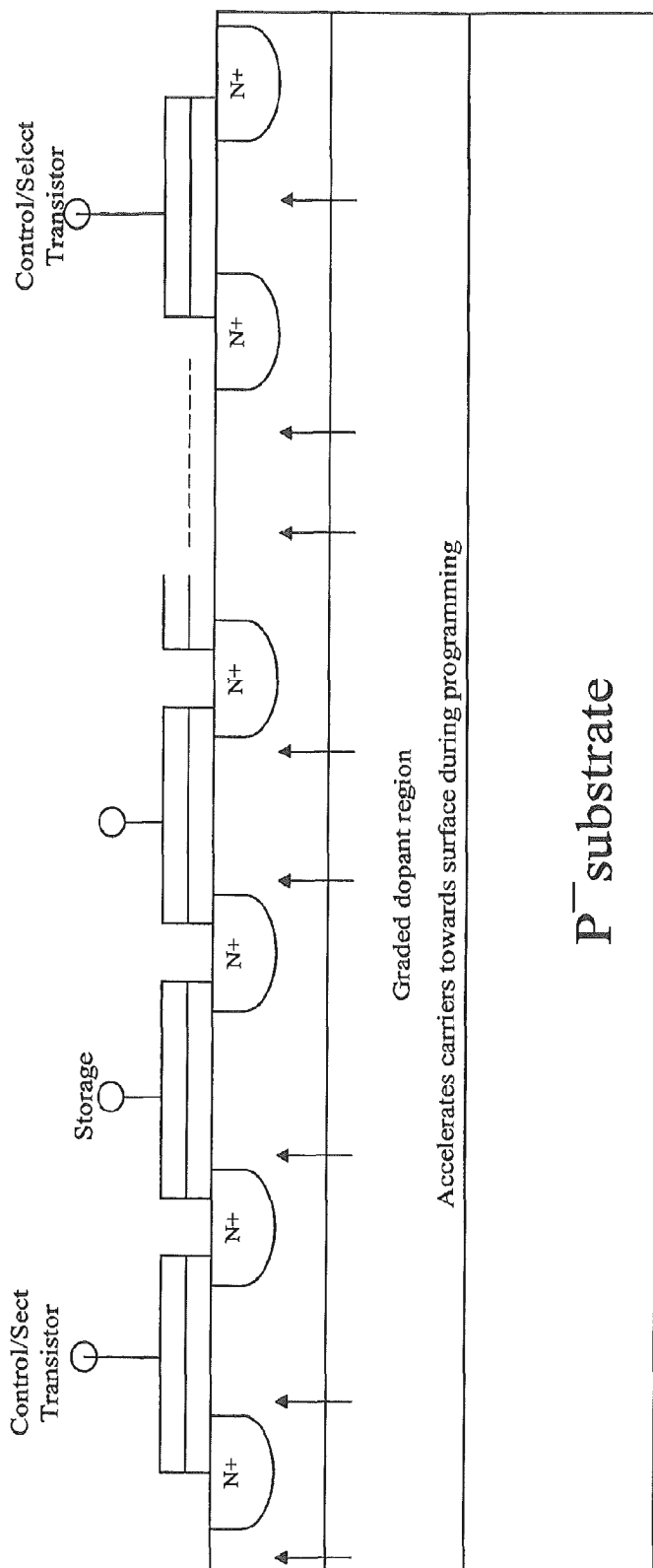


FIGURE 5(c) CMOS Substrate for a NAND flash device to improve programming times

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SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

CROSS-REFERENCE TO RELATED APPLICATION

This continuation application claims priority to and the benefit of U.S. application Ser. No. 13/854,319, filed on Apr. 1, 2013, which is a continuation of U.S. application Ser. No. 11/622,496, filed Jan. 12, 2007, now U.S. Pat. No. 8,421,195, which is a divisional of U.S. application Ser. No. 10/934,915, filed on Sep. 3, 2004, now abandoned, all of which are incorporated by reference.

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Bipolar Junction transistors (BJT) are minority carrier devices as the principle device conduction mechanism. However, majority carriers also a small yet finite role in modulating the conductivity in BJTs. Consequently, both carriers (electrons and holes) play a role in the switching performance of BJTs. The maximum frequency of operation in BJTs is limited by the base transit time as well as the quick recombination of the majority carriers when the device is switched off (prior to beginning the next cycle). The dominant carrier mechanism in BJTs is carrier diffusion. Carrier drift current component is fairly small, especially in uniformly doped base BJTs. Efforts have been made in graded base transistors to create an 'aiding drift field', to enhance the diffusing minority carrier's speed from emitter to collector. However, most semiconductor devices, including various power MOSFETs (traditional, DMOS, lateral, vertical and a host of other configurations), IGBT's (Insulated Gated Base Transistors), still use a uniformly doped drift epitaxial region in the base. FIG. 1 shows the relative doping concentration versus distance in a BJT. FIG. 2 shows the 'uniformly doped epi region' in a IGBT. In contrast to BJTs, MOS devices are majority carrier devices for conduction. The conduction is channel dominated. The channel can be a surface in one plane in planar devices. The surface can also be on the sidewalls in a vertical device. Other device architectures to combine planar and vertical conduction are also possible. The maximum frequency of operation is dictated primarily by source-drain separation distance. Most MOS devices use a uniformly doped substrate (or a well region). When a MOSFET is optimally integrated with a BJT in a monolithic fashion, an IGBT results. The IGBT inherits the advantages of both MOSFET and BJT. It also brings new challenges because the required characteristics (electron transit and hole recombination as fast as possible in the case of an n-channel IGBT) require different dopant gradients either in the same layer at different positions, or at the interfaces of similar or dissimilar layers.

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3(d) illustrate device cross sections, as practiced today. 'Retrograde' and 'halo' wells have also been attempted to improve refresh time in DRAM's (dynamic random access memories), as well as, reducing dark current (background noise) and enhance RGB (Red, Green, Blue) color resolution in digital camera Ics. Most of these techniques either divert the minority carriers away from the active regions of critical charge storage nodes at the surface, or, increase minority carrier density locally as the particular application requires.

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For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

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FIG. 2 illustrates the cross section of a commercial IGBT with a uniform epitaxial drift region (base);

FIGS. 3(a), 3(b), 3(c), 3(d) illustrate cross sections commonly used CMOS silicon substrate with two wells (one n-well in which p-channel transistors are subsequently fabricated, and, one p-well in which n-channel transistors are subsequently fabricated)—typical IC, EEPROM using tunnel insulator, DRAM and NAND flash;

FIG. 4 illustrates the cross section of a IGBT, using one embodiment of the invention described here, where the dopant is optimally graded in the epitaxial drift region; and

FIGS. 5(a), 5(b), 5(c) illustrate the cross sections of a MOS silicon substrate with two wells, and, an underlying layer using embodiments of the invention to improve performance in each application—VLSI logic, DRAM/image IC, nonvolatile memory IC.

DETAILED DESCRIPTION OF THE INVENTION

The relative doping concentrations of emitter and collector regions varies from 10^{18} to $10^{20}/\text{cm}^3$, where as the base region is 10^{14} to $10^{16}/\text{cm}^3$ depending on the desired characteristics of the BJT. In graded base p-n-p transistors, the donor dopant concentration may be 10 to 100× at the emitter-base junction, relative to the base-collector junction (1×). The gradient can be linear, quasi linear, exponential or complimentary error function. The relative slope of the donor concentration throughout the base, creates a suitable aiding drift electric field, to help the holes (p-n-p transistor) transverse from emitter to collector. Since the aiding drift field helps hole conduction, the current gain at a given frequency is enhanced, relative to a uniformly-doped-(base) BJT. The improvement in cut-off frequency (or, frequency at unity gain, f_T) can be as large as 2×-5×. Similar performance improvements are also applicable to n-p-n transistors.

As illustrated in FIG. 4, in one embodiment according to the invention, a donor gradient is established from the emitter-drift epitaxial base region junction of the punch-through IGBT, to the drift epitaxial base region—n' buffer layer boundary (electrons in this case are accelerated in their transit from emitter to collector). The 'average' base resistance is optimized, so that conductivity modulation and lifetime (for minority carriers) in base region are not compromised. By sweeping the carriers towards the n' buffer region two advantages are obtained—the frequency of operation (combination of t_{on} and t_{off} as is known in the IGBT commercial nomenclature) can be enhanced. More importantly, during t_{off} holes can be recombined much quicker at the n' buffer layer compared

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to a uniformly doped n^- epitaxial drift region by establishing a different dopant gradient near the n^+ buffer layer. It should be noted that the drift region can also be a non-epitaxial silicon substrate. Epitaxy enhances lifetime, but, epitaxy is not mandatory. Different layers of dopant regions can be transferred through wafer to wafer bonding (or other similar transfer mechanisms) for eventual device fabrication. The “reverse recovery time” for an IGBT is significantly improved due to the optimized graded dopant in the so called “drift region” as well as at the interfaces of the drift region. Graded dopants can also be implemented in the n^+ buffer layer as well as other regions adjacent to the respective layers. Two important performance enhancements are the result of dopant gradients. For example, in an n -channel IGBT, electrons can be swept from source to drain rapidly, while at the same time holes can be recombined closer to the n^+ buffer layer. This can improve t_{on} and t_{off} in the same device.

The following paragraph, beginning on page 5, line 6, and ending on page 11, line 28, is amended as indicated in the marked up version below:

As illustrated in FIGS. 5(a), 5(b), 5(c), donor gradient is also of benefit to very large scale integrated circuits (VLSI)—VLSI logic, DRAM, nonvolatile memory like NAND flash. Spurious minority carriers can be generated by clock switching in digital VLSI logic and memory IC’s. These unwanted carriers can discharge dynamically-held ‘actively held high’ nodes. Statically held nodes (with V_{cc}) can not be affected, in most cases. Degradation of refresh time in DRAM’s is one of the results, because the capacitor holds charge dynamically. Similarly, degradation of CMOS digital images, in digital imaging IC’s is another result of the havoc caused by minority carriers. Pixel and color resolution can be significantly enhanced in imaging IC’s with the embodiments described here. Creating ‘Sub Terrain’ recombination centers underneath the wells (gold doping, platinum doping) as is done in some high-voltage diodes is not practical for VLSI circuits. Hence, a novel technique has been described here by creating a drift field to sweep these unwanted minority carriers into the substrate as quickly as possible, from the active circuitry at the surface. In a preferred embodiment, the subterrain n -layer has a graded donor concentration to sweep the minority carriers deep into the substrate. One or more of such layers can also be implemented through wafer to wafer bonding or similar “transfer” mechanisms. This n -layer can be a deeply-implanted layer. It can also be an epitaxial layer. The n -well and p -well also can be graded or retrograded in dopants, as desired, to sweep those carriers away from the surface as well. The graded dopant can also be implemented in surface channel MOS devices to accelerate majority carriers towards the drain. In nonvolatile memory devices, to decrease programming time, carriers should be accelerated towards the surface when programming of memory cells is executed. The graded dopant can also be used to fabricate superior Junction field-effect transistors where the “channel pinchoff” is controlled by a graded channel instead of a uniformly doped channel (as practiced in prior art).

One of ordinary skill and familiarity in the art will recognize that the concepts taught herein can be customized and tailored to a particular application in many advantageous ways. For instance, minority carriers can be channeled to the surface, to aid programming in nonvolatile memory devices (NOR, NAND, multivalued-cell). Moreover, single well, as well triple-well CMOS fabrication techniques can also be optimized to incorporate these embodiments, individually and collectively. Any modifications of such embodiments

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(described here) fall within the spirit and scope of the invention. Hence, they fall within the scope of the claims described below

Although the invention has been described with reference to specific embodiments, these descriptions are not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as alternative embodiments of the invention will become apparent to persons skilled in the art upon reference to the description of the invention. It should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

It is therefore, contemplated that the claims will cover any such modifications or embodiments that fall within the true scope of the invention.

What is claimed is:

1. A semiconductor device comprising:

a surface layer;

a substrate;

an active region including a source and a drain, disposed on one surface of said surface layer;

a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said substrate to said surface layer; and

at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said substrate to said surface layer.

2. The semiconductor device of claim 1 wherein said first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions.

3. The semiconductor device of claim 1 wherein the semiconductor device is a central processing unit (CPU).

4. The semiconductor device of claim 1 wherein the semiconductor device is a DRAM device.

5. The semiconductor device of claim 1 wherein the semiconductor device is a flash memory device.

6. The semiconductor device of claim 1 wherein the semiconductor device is an image sensor device.

7. A semiconductor device comprising:

a surface layer;

a substrate;

an active region including a source and a drain, disposed on one surface of said surface layer;

a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and

at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

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8. The semiconductor device of claim 7 wherein said first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions.

9. The semiconductor device of claim 7 wherein the semiconductor device is a central processing unit (CPU). 5

10. The semiconductor device of claim 7 wherein the semiconductor device is a DRAM device.

11. The semiconductor device of claim 7 wherein the semiconductor device is a flash memory device. 10

12. The semiconductor device of claim 7 wherein the semiconductor device is an image sensor device.

* * * * *

EXHIBIT 3



US010510842B2

(12) **United States Patent**
Rao

(10) **Patent No.:** **US 10,510,842 B2**

(45) **Date of Patent:** **Dec. 17, 2019**

(54) **SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS**

H01L 29/7395 (2013.01); *H01L 27/0214* (2013.01); *H01L 27/10844* (2013.01)

(71) Applicant: **GREENTHREAD, LLC**, Dallas, TX (US)

(58) **Field of Classification Search**

CPC *H01L 29/1095*

USPC 257/655

See application file for complete search history.

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(73) Assignee: **GREENTHREAD, LLC**, Dallas, TX (US)

(56) **References Cited**

U.S. PATENT DOCUMENTS

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

4,001,864 A 1/1977 Gibbons
4,160,985 A 7/1979 Kamins et al.
(Continued)

(21) Appl. No.: **15/590,282**

OTHER PUBLICATIONS

(22) Filed: **May 9, 2017**

(65) **Prior Publication Data**

US 2017/0243876 A1 Aug. 24, 2017

P.D. Moor, Advanced CMOS-based pixel sensors, <https://indico.cern.ch/event/122027/contributions/88236/attachments/69340/99377/FEEimecPdM.pdf>, 2011, 41 pages.

(Continued)

Related U.S. Application Data

(60) Continuation of application No. 14/931,636, filed on Nov. 3, 2015, now Pat. No. 9,647,070, which is a continuation of application No. 14/515,584, filed on Oct. 16, 2014, now Pat. No. 9,190,502, which is a continuation of application No. 13/854,319, filed on (Continued)

Primary Examiner — Ajay Arora

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(51) **Int. Cl.**

H01L 21/02 (2006.01)

H01L 29/10 (2006.01)

H01L 27/11524 (2017.01)

H01L 27/146 (2006.01)

H01L 27/11521 (2017.01)

H01L 29/739 (2006.01)

H01L 29/36 (2006.01)

(Continued)

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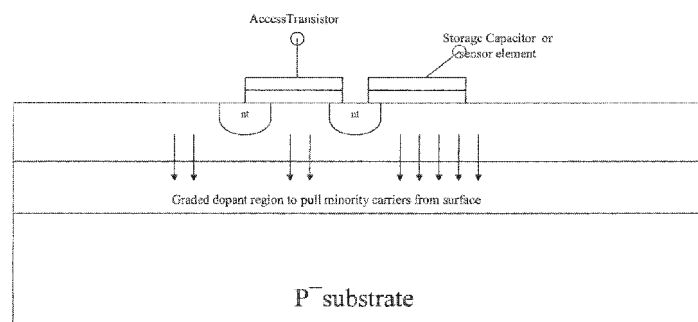
ABSTRACT

Most semiconductor devices manufactured today, have uniform dopant concentration, either in the lateral or vertical device active (and isolation) regions. By grading the dopant concentration, the performance in various semiconductor devices can be significantly improved. Performance improvements can be obtained in application specific areas like increase in frequency of operation for digital logic, various power MOSFET and IGBT ICs, improvement in refresh time for DRAMs, decrease in programming time for nonvolatile memory, better visual quality including pixel resolution and color sensitivity for imaging ICs, better sensitivity for varactors in tunable filters, higher drive capabilities for JFETs, and a host of other applications.

18 Claims, 10 Drawing Sheets

(52) **U.S. Cl.**

CPC *H01L 29/1095* (2013.01); *H01L 27/11521* (2013.01); *H01L 27/11524* (2013.01); *H01L 27/14643* (2013.01); *H01L 29/36* (2013.01);



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Related U.S. Application Data

Apr. 1, 2013, now abandoned, which is a continuation of application No. 11/622,496, filed on Jan. 12, 2007, now Pat. No. 8,421,195, which is a division of application No. 10/934,915, filed on Sep. 3, 2004, now abandoned.

(51) Int. Cl.

H01L 27/02 (2006.01)
H01L 27/108 (2006.01)

(56)

References Cited

U.S. PATENT DOCUMENTS

4,347,654 A 9/1982 Allen et al.
4,481,522 A 11/1984 Jastrzebski et al.
4,866,000 A 9/1989 Okita
5,029,277 A 7/1991 Kane
5,130,262 A 7/1992 Masquelier et al.
5,213,988 A 5/1993 Yamauchi et al.
5,262,345 A 11/1993 Nasser et al.
5,329,144 A 7/1994 Luryi
5,448,087 A 9/1995 Streit et al.
5,480,816 A 1/1996 Uga et al.
5,496,746 A 3/1996 Matthews
5,517,052 A 5/1996 Ishaque
5,569,612 A 10/1996 Frisina et al.
5,575,862 A 11/1996 Nishida
5,637,898 A 6/1997 Baliga
5,797,999 A 8/1998 Sannomiya et al.
5,888,857 A 3/1999 Zhang et al.
5,973,575 A 10/1999 Kamogawa et al.
6,211,028 B1 4/2001 Tsai et al.
6,310,366 B1 10/2001 Rhodes et al.
RE37,441 E 11/2001 Yamazaki
6,452,086 B1 9/2002 Muller
6,465,862 B1 10/2002 Harris
6,472,715 B1 10/2002 Liu et al.
6,670,544 B2 12/2003 Kibbel et al.
6,683,343 B2 1/2004 Matsudai et al.
6,696,314 B2 2/2004 Rhodes
6,706,550 B2 3/2004 Lee et al.
6,713,813 B2 3/2004 Marchant
6,720,622 B1 4/2004 Yu
6,737,722 B2 5/2004 Yamamoto et al.
6,744,117 B2 6/2004 Dragon et al.
6,747,883 B2 6/2004 Yasumura
6,753,202 B2 6/2004 Chen et al.
6,754,093 B2 6/2004 Lien
6,756,616 B2 6/2004 Rhodes
6,780,713 B2 8/2004 Bromberger et al.
6,831,292 B2 12/2004 Currie et al.

6,878,603 B2 4/2005 Bromberger et al.
6,921,943 B2 7/2005 Kenney et al.
6,933,215 B2 8/2005 Bromberger et al.
7,064,385 B2 6/2006 Dudek et al.
7,115,925 B2 10/2006 Rhodes
7,233,044 B2 6/2007 Dudek
7,307,327 B2 12/2007 Bahl et al.
7,504,692 B2 3/2009 Dudek et al.
8,164,124 B2 4/2012 Liu et al.
2001/0040622 A1 11/2001 Maruyama
2002/0056883 A1 5/2002 Baliga
2002/0074585 A1 6/2002 Tsang et al.
2002/0084430 A1 7/2002 Bamji et al.
2002/0093281 A1 7/2002 Cathey
2002/0102783 A1 8/2002 Fujimoto et al.
2002/0134419 A1 9/2002 Macris
2003/0026126 A1 2/2003 Uemura
2003/0030488 A1 2/2003 Hueting et al.
2003/0042511 A1 3/2003 Rhodes
2004/0027753 A1 2/2004 Friedrichs et al.
2006/0113592 A1 6/2006 Pendharkar et al.
2007/0045682 A1* 3/2007 Hong H01L 27/14601
257/292
2012/0048462 A1* 3/2012 Lee B32B 37/185
156/272.8
2013/0001661 A1 1/2013 Mao et al.
2015/0200314 A1 7/2015 Webster

OTHER PUBLICATIONS

E. Parton, CMOS Sensors, Laser Focus World, <http://www.laserfocusworld.com/articles/print/volume-49/issue-10/features/cmos-sensors-cmos-based-specialty-imagers-reach-new-performance-levels.html>, Oct. 14, 2013, 5 pages.
Z. Cao, Design of Pixel for High Speed CMOS Image Sensors, http://www.imagesensors.org/Past%20Workshops/2013%20Workshop/2013%20Papers/07-11_072-Cao_paper.pdf, 4 pages.
M. Tanenbaum, BSTJ: Diffused Emitter and Base Silicon Transistors, The Bell System Technical Journal, Jan. 1956, 22 pages, vol. XXXV, <https://archive.org/details/bstj35-1-1>.
IMEC Image Sensors and Vision Systems, <http://www2.imec.be/content/user/File/Brochures/cmos%20imagers%20brochure-april26.pdf>, Apr. 2014, 2 pages.
A. S. Grove, Physics and Technology of Semiconductor Devices, John Wiley Sons, Inc., New York, Nov. 1967.
W. Murray Bullis and W. R. Runyan, Influence of Mobility and Lifetime Variations on Drift-Field Effects in Silicon-Junction Devices, IEEE Transactions on Electron Devices, vol. Ed-14, No. 2, Feb. 1967.
Berinder Brar et al., Herb's Bipolar Transistors, IEEE Transactions on Electron Devices, vol. 48, No. 11, Nov. 2001.

* cited by examiner

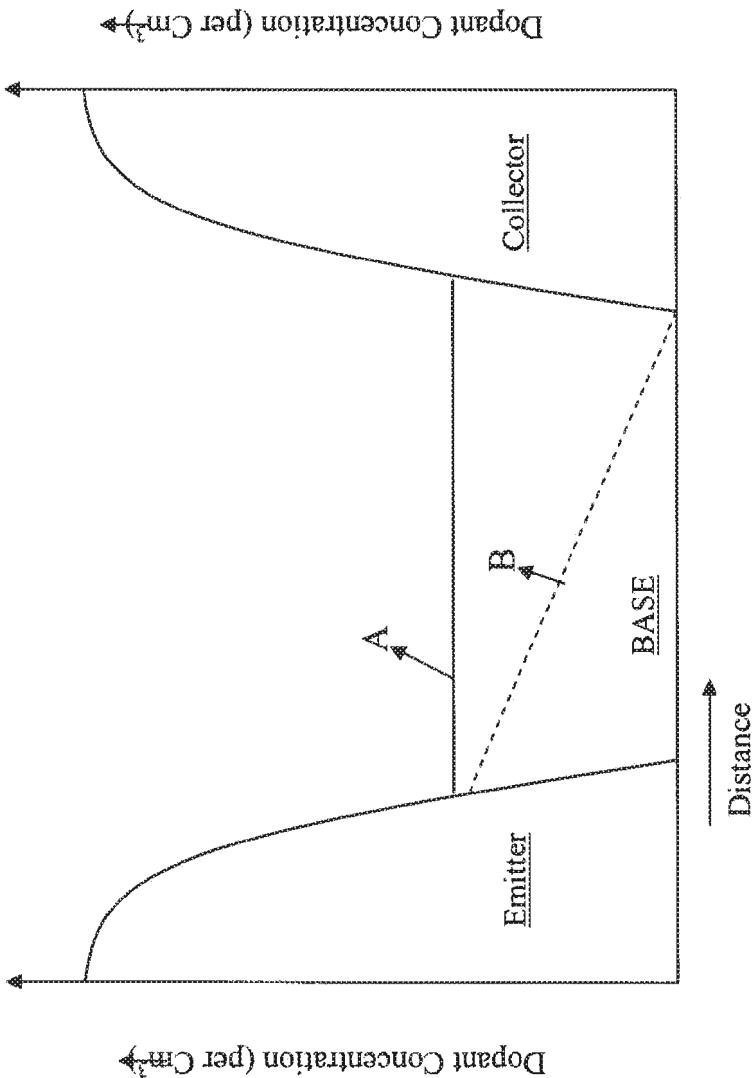


Figure 1 Prior Art

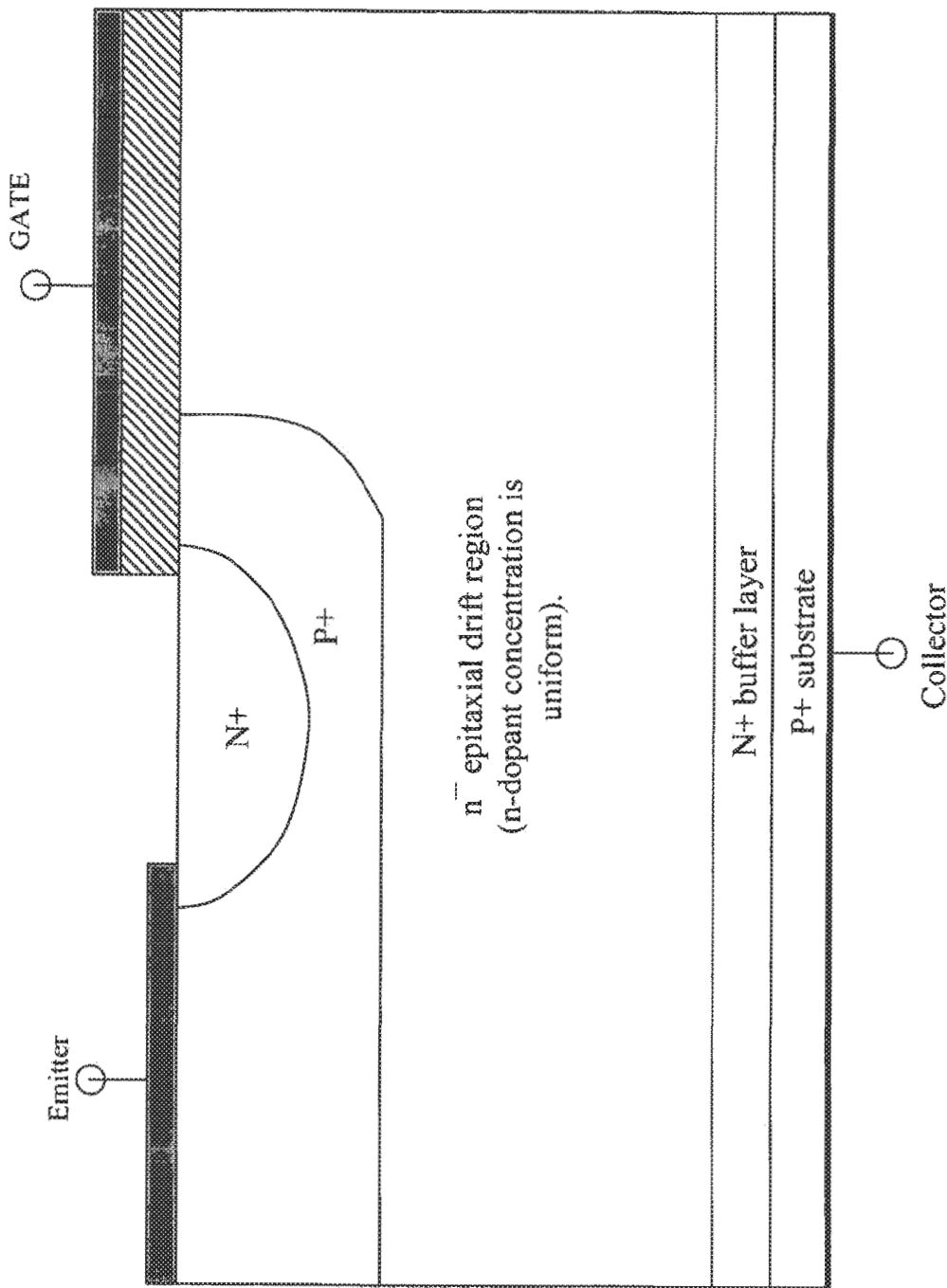


FIGURE 2 Prior art

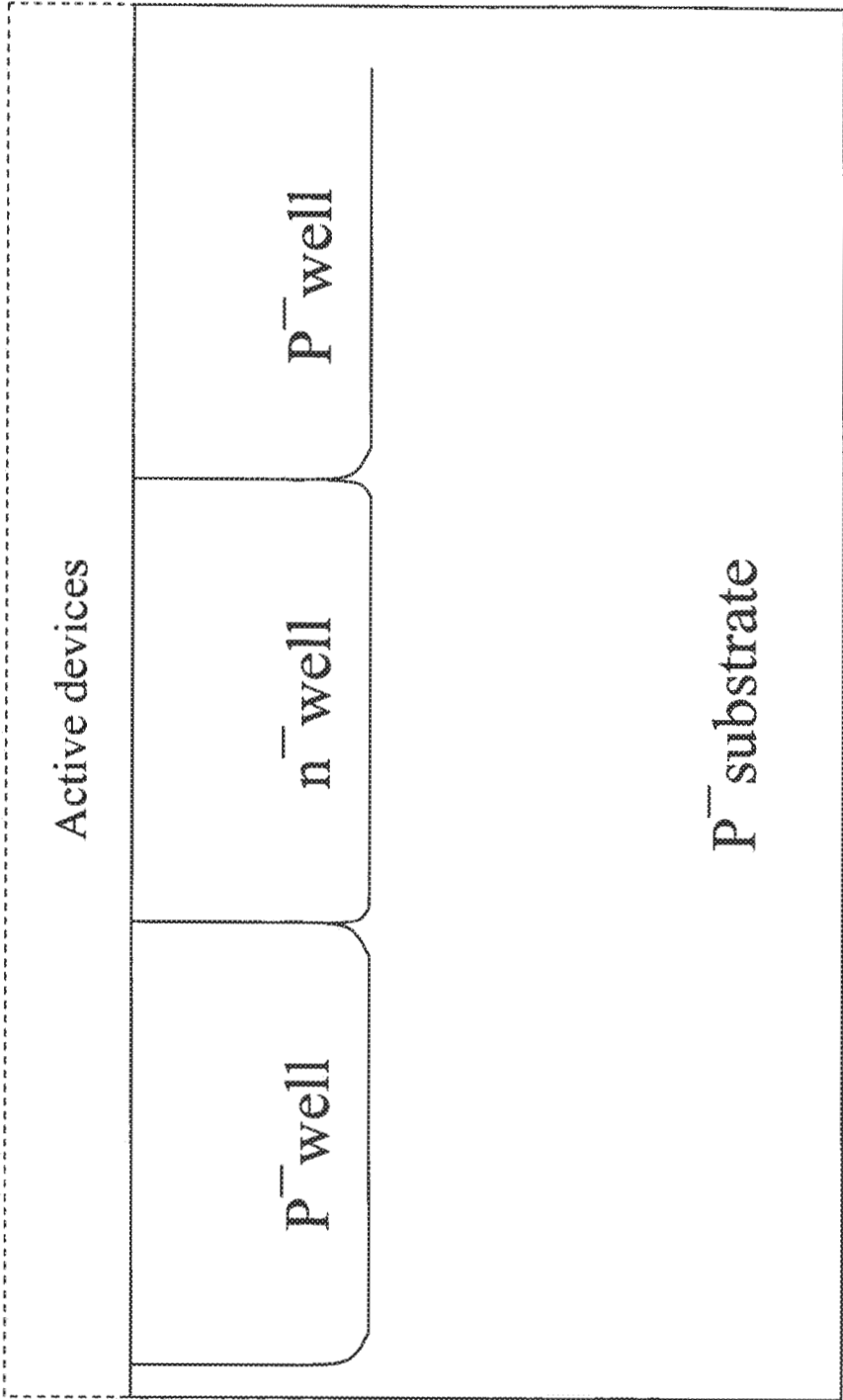


FIGURE 3A Prior art (Twin well CMOS) for a CMOS integrated circuit

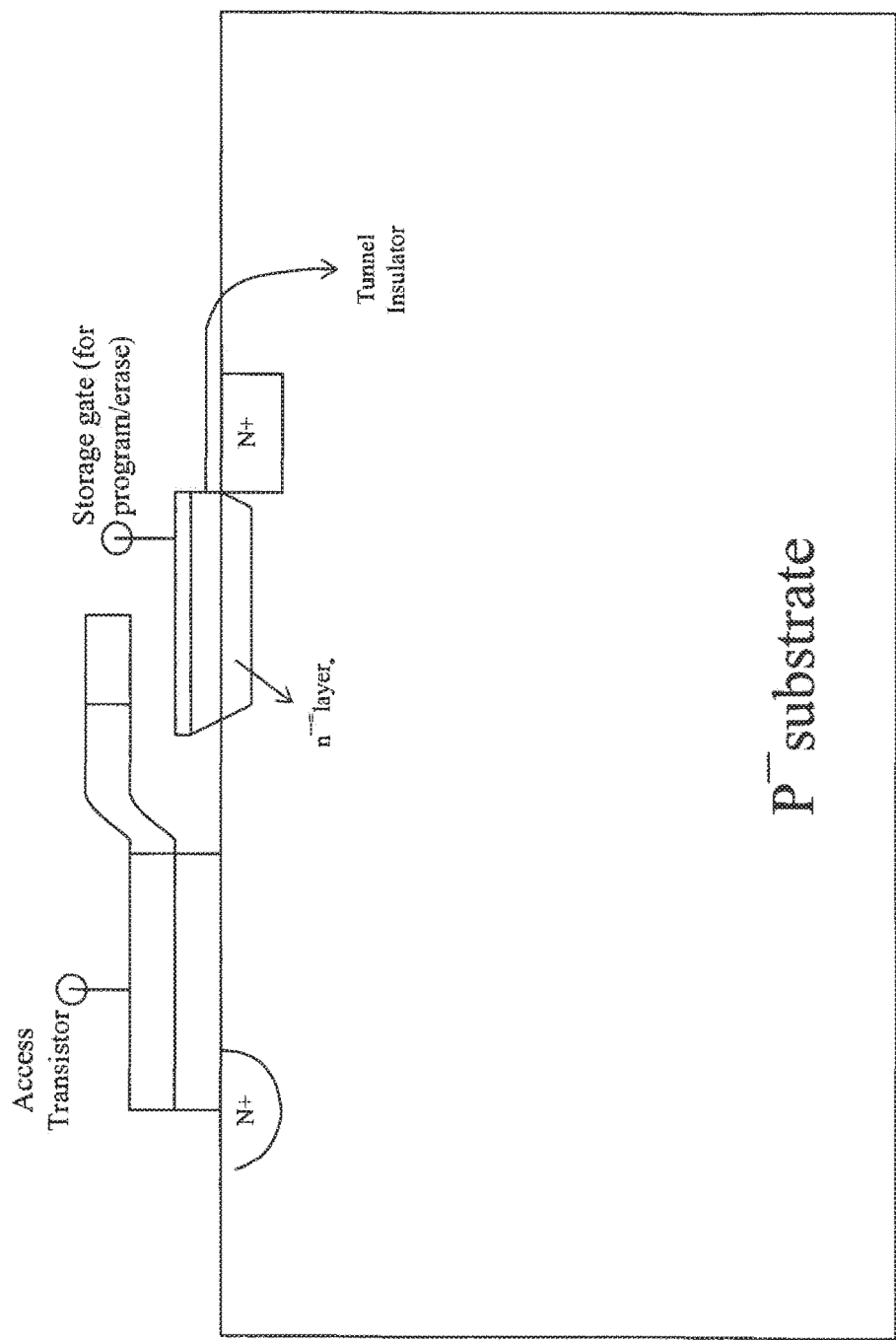


FIGURE 3B Prior art for a two-device EEPROM memory cell

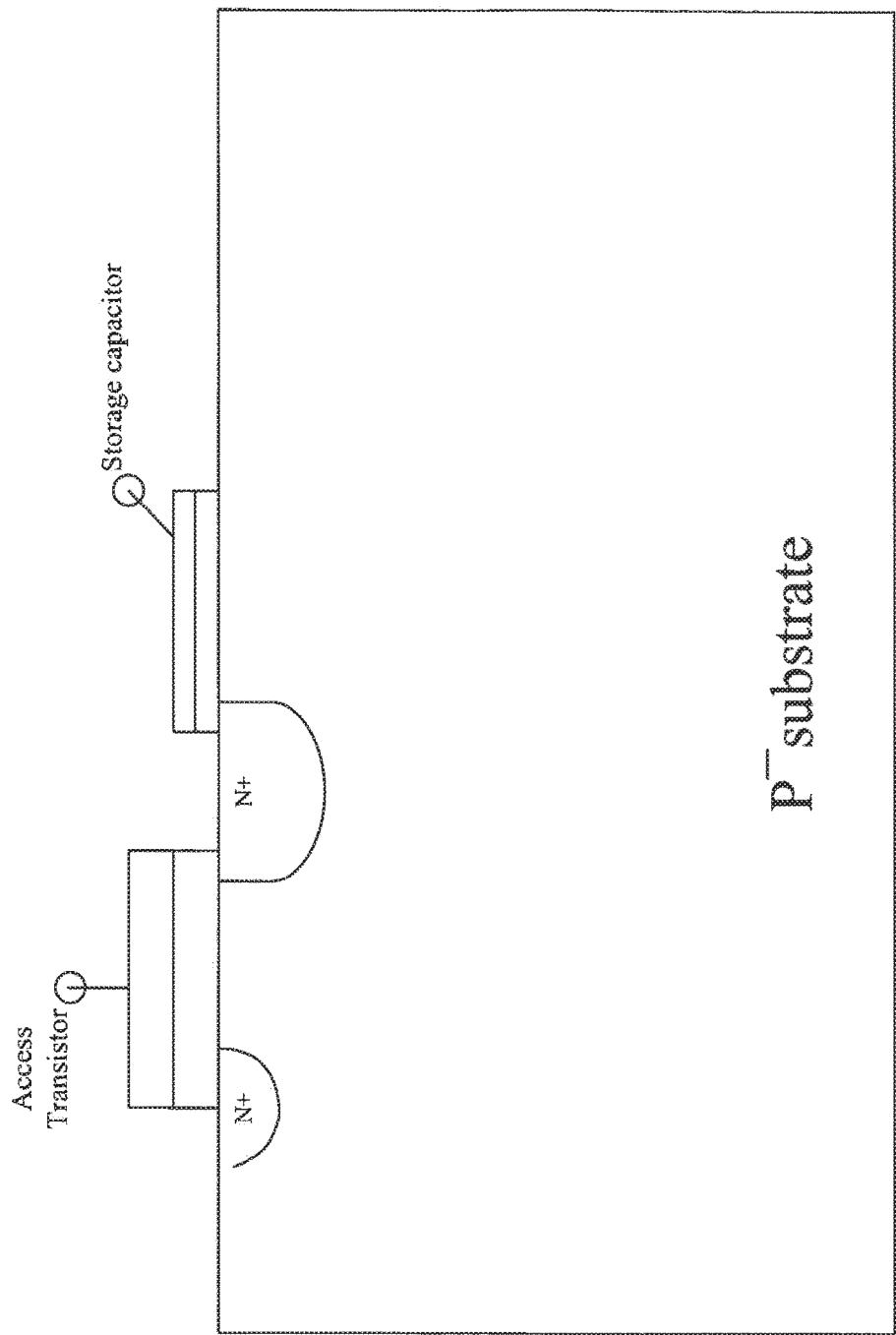


FIGURE 3C Prior art for a 1T-1C DRAM memory cell

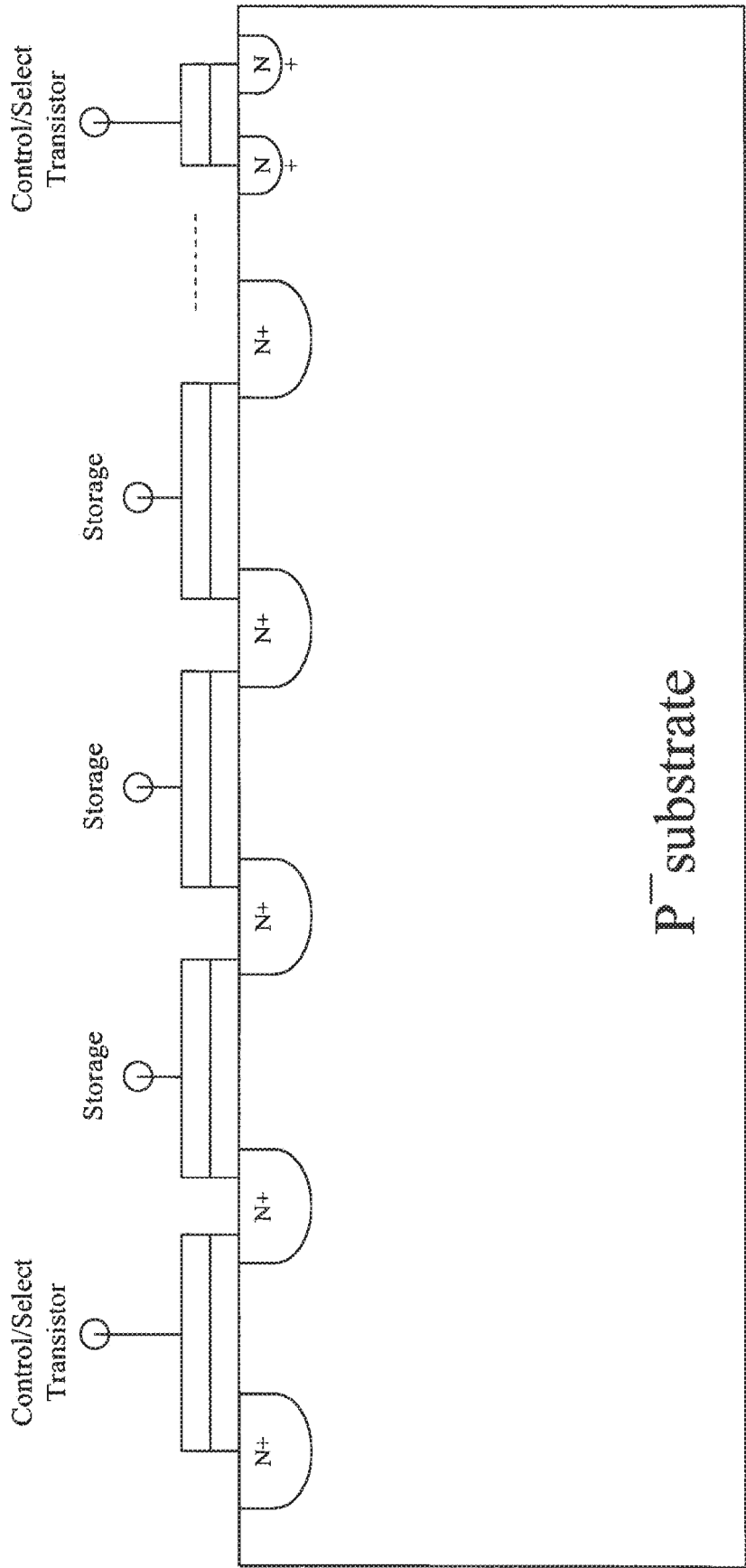


FIGURE 3D Prior art for a NAND flash memory cell

Note: Control/ Select transistors have a single insulator - traditional MOS transistor.
Storage nodes have a stacked gate structure, typically with a floating gate and control gate comprising the stack.

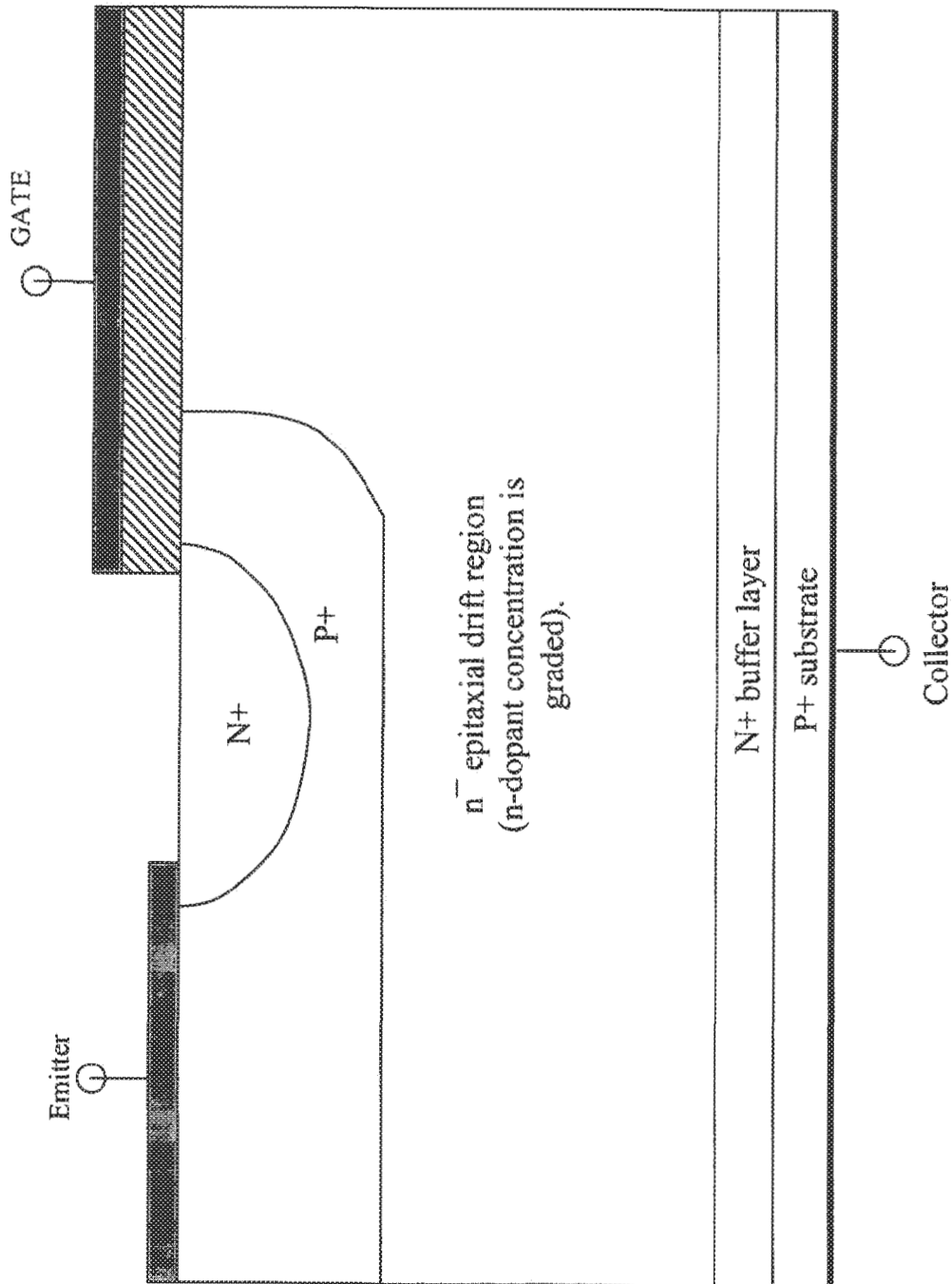


FIGURE 4 A dopant - concentration graded drift region in a IGBT

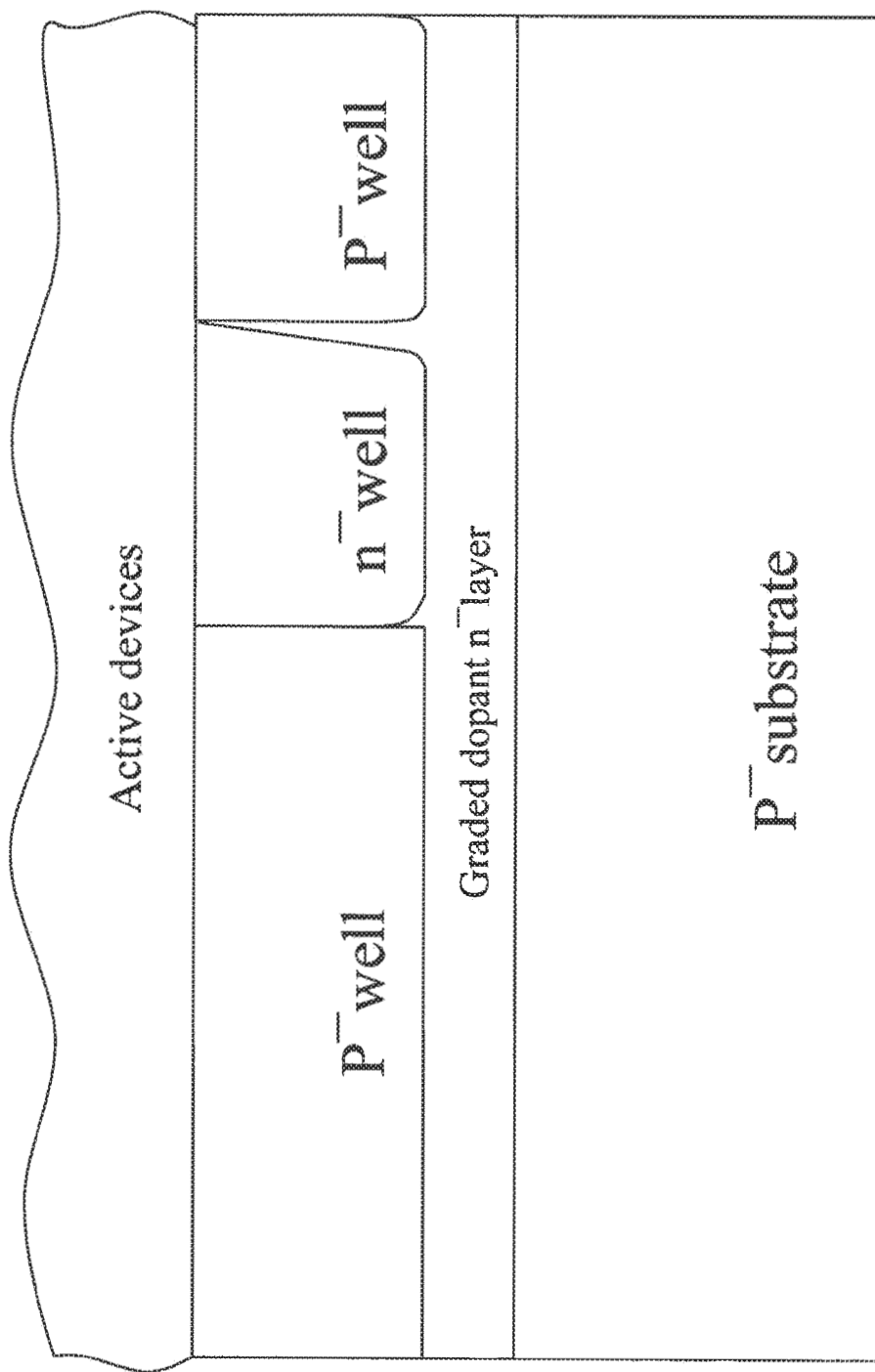


FIGURE 5A A CMOS Substrate for digital, mixed, signal, and sensors IC's

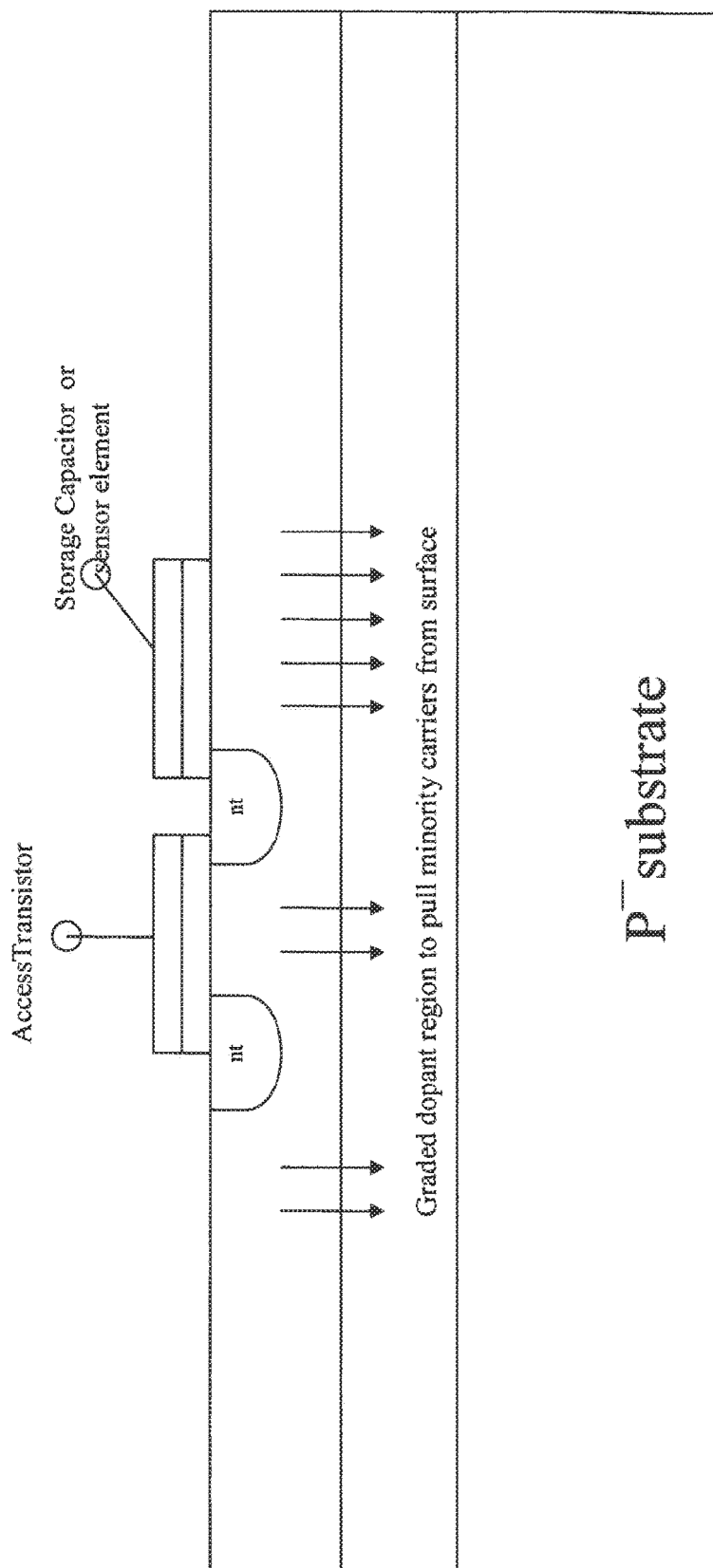


FIGURE 5B CMOS Substrate for a DRAM or image sensor, with one embodiment of the invention

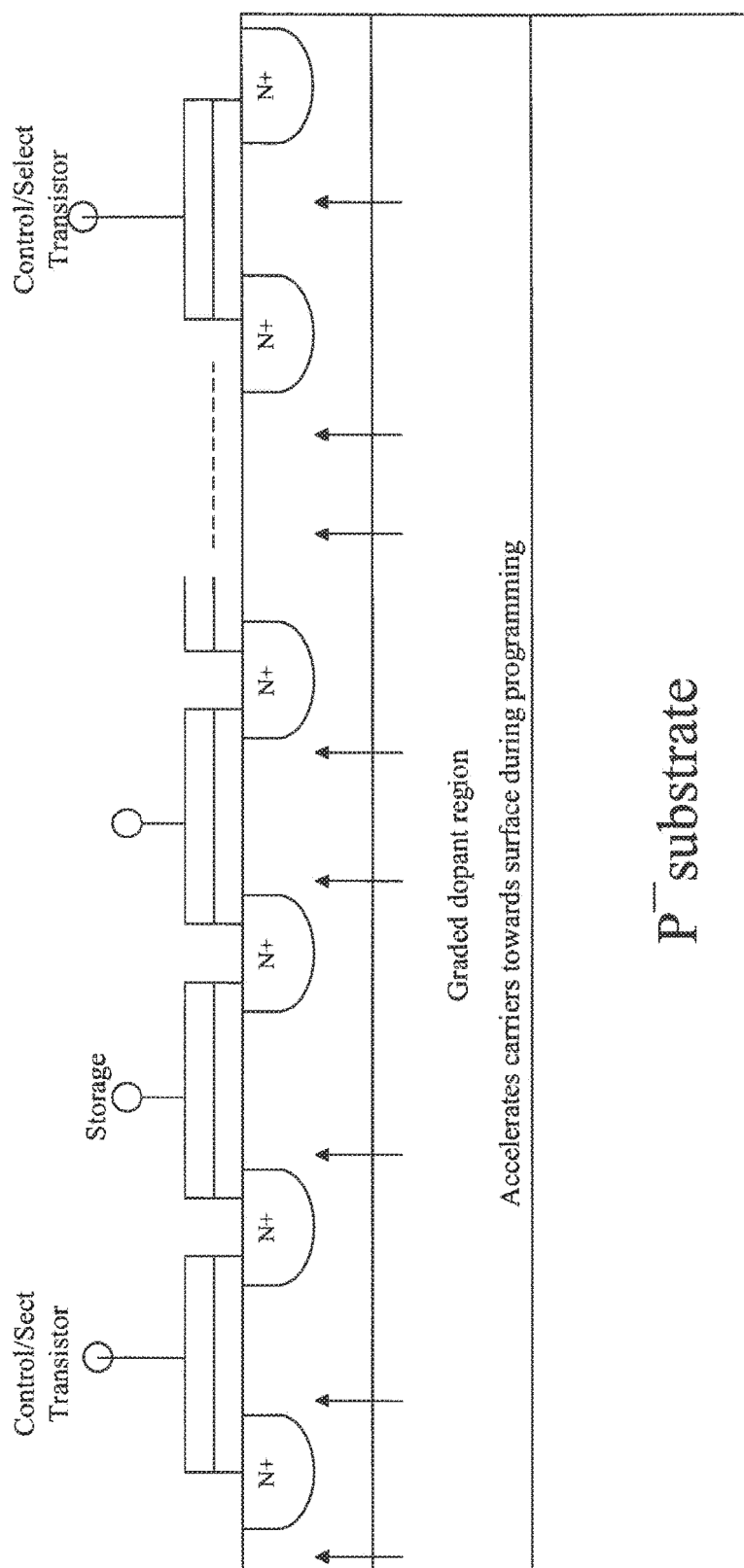


FIGURE 5C CMOS Substrate for a NAND flash device to improve programming times

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SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a Continuation of U.S. patent application Ser. No. 14/931,636, filed Nov. 3, 2015, published on Jun. 16, 2016 as U.S. Publication No. 2016-0172447, now U.S. Pat. No. 9,647,070, issued on May 9, 2017. Application Ser. No. 14/931,636 is a continuation of U.S. patent application Ser. No. 14/515,584, filed Oct. 16, 2014, published on Feb. 5, 2015, as U.S. Publication No. 2015-0035004, now U.S. Pat. No. 9,190,502, issued on Nov. 17, 2015. Application Ser. No. 14/515,584 is a Continuation of U.S. patent application Ser. No. 13/854,319 filed Apr. 1, 2013, published on Aug. 29, 2013, as U.S. Publication No. 2013-0221488. Application Ser. No. 13/854,319 is a Continuation of Ser. No. 11/622,496, filed Jan. 12, 2007, published on Jul. 12, 2007, as Publication No. 2007-0158790, now U.S. Pat. No. 8,421,195, issued on Apr. 16, 2013. Application Ser. No. 11/622,496, is a Division of U.S. patent application Ser. No. 10/934,915, filed Sep. 3, 2004, published on Mar. 9, 2006, as U.S. Publication No. 2006-0049464. U.S. Pat. Nos. 9,647,070, 9,190,502, and 8,421,195, and Patent Application Publication Nos. 2016-0172447, 2015-0035004, 2013-0221488, 2007-0158790, and 2006-0049464, are incorporated herein by reference in their entirety.

TECHNICAL FIELD

This present invention relates to all semiconductor devices and systems. Particularly it applies to diffused diodes, avalanche diodes, Schottky devices, power MOS transistors, JFET's, RF bipolar transistors, IGBTs (Insulated Gate Bipolar Transistors), varactors, digital VLSI, mixed signal circuits and sensor devices including camera ICs employing CCD (Charge Coupled Device) as well as CMOS technologies.

BACKGROUND

Bipolar Junction Transistors (BJT) are classified as minority carrier devices because minority carriers are the principle device conduction mechanism. However, majority carriers also play a small but finite role in modulating the conductivity in BJTs. Consequently, both carriers (electrons and holes) play a role in the switching performance of BJTs. The maximum frequency of operation in BJTs is limited by the base transit time as well as the quick recombination of the majority carriers when the device is switched off (prior to beginning the next cycle). The dominant carrier mechanism in BJTs is carrier diffusion. The carrier drift current component is fairly small, especially in uniformly doped base BJTs. Efforts have been made in graded base transistors to create an aiding drift field to enhance the diffusing minority carrier's speed from emitter to collector. However, most semiconductor devices, including various power MOSFETs (traditional, DMOS, lateral, vertical and a host of other configurations), IGBT's (Insulated Gated Base Transistors), still use a uniformly doped 'drift epitaxial' region in the base. FIG. 1 shows the relative doping concentration versus distance in a BJT. FIG. 2 shows the uniformly doped epi region in an IGBT. In contrast to BJTs, MOS devices are majority carrier devices for conduction. The conduction is channel dominated. The channel can be a surface in one plane in planar devices. The surface can also be on the

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sidewalls in a vertical device. Other device architectures to combine planar and vertical conduction are also possible. The maximum frequency of operation is dictated primarily by source-drain separation distance. Most MOS devices use a uniformly doped substrate (or a well region). When a MOSFET is optimally integrated with a BJT in a monolithic fashion, an IGBT results. The IGBT inherits the advantages of both MOSFET and BJT. It also brings new challenges because the required characteristics (electron transit and hole recombination as fast as possible in n-channel IGBT) necessitate different dopant gradients either in the same layer at different positions, or at the interfaces of similar or dissimilar layers.

Retrograde wells have been attempted, with little success, to help improve soft error immunity in SRAMs and visual quality in imaging circuits. FIG. 3A shows a typical CMOS VLSI device employing a twin well substrate, on which active devices are subsequently fabricated. FIGS. 3B, 3C, and 3D illustrate device cross sections, as practiced today. Retrograde and halo wells have also been attempted to improve refresh time in DRAMs (dynamic random-access memories), as well as, reducing dark current (background noise) and enhance RGB (Red, Green, Blue) color resolution in digital camera ICs. Most of these techniques either divert the minority carriers away from the active regions of critical charge storage nodes at the surface, or, increase minority carrier density locally as the particular application requires.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. 1 illustrates the relative doping profiles of emitter, base and collector for the two most popular bipolar junction transistors: namely, uniform base ("A") and graded base ("B");

FIG. 2 illustrates the cross section of a commercial IGBT with a uniform epitaxial drift region (base);

FIGS. 3A, 3B, 3C, and 3D illustrate cross sections of commonly used prior art CMOS silicon substrates; FIG. 3A showing a typical prior art IC with two wells (one n⁻well in which p-channel transistors are subsequently fabricated and one p⁻well in which n-channel transistors are subsequently fabricated); FIG. 3B showing a prior art EEPROM (Electrically Erasable Programmable Read-Only Memory) memory cell having a tunnel insulator; FIG. 3C showing a prior art DRAM memory cell; and FIG. 3D showing a prior art NAND flash memory cell;

FIG. 4 illustrates the cross section of an IGBT, using one embodiment of the invention described here, where the dopant is optimally graded in the epitaxial drift region; and

FIGS. 5A, 5B, and 5C illustrate the cross sections of a CMOS silicon substrate with two wells and an underlying layer using embodiments of the invention to improve performance in each application—VLSI logic, DRAM/image IC, nonvolatile memory IC.

DETAILED DESCRIPTION

The relative doping concentrations of emitter and collector regions varies from 10^{18} to $10^{20}/\text{cm}^3$, whereas the base region is 10^{14} to $10^{16}/\text{cm}^3$ depending on the desired characteristics of the BJT. In graded base p-n-p transistors, the donor dopant concentration may be 10 to 100× at the emitter-base junction, relative to the base region.

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(1×). The gradient can be linear, quasi linear, exponential or complimentary error function. The relative slope of the donor concentration throughout the base creates a suitable aiding drift electric field, to help the holes (p-n-p transistor) transverse from emitter to collector. Since the aiding drift electric field helps hole conduction, the current gain at a given frequency is enhanced, relative to a uniformly-doped (base) BJT. The improvement in cut-off frequency (or, frequency at unity gain, f_T) can be as large as 2×-5×. Similar performance improvements are also applicable to n-p-n transistors.

As illustrated in FIG. 4, in one embodiment according to the invention, a donor gradient is established from the emitter-drift epitaxial base region junction of the punch-through IGBT, to the drift epitaxial base region—n⁺ buffer layer boundary (electrons in this case are accelerated in their transit from emitter to collector). The “average” base resistance is optimized so that conductivity modulation and lifetime (for minority carriers) in the base region are not compromised. By sweeping the carriers towards the n⁺ buffer region a number of advantages are obtained. First, the frequency of operation (combination of t_{on} and t_{off} as is known in the IGBT commercial nomenclature) can be enhanced. Second, and maybe more importantly, during t_{off} , holes can be recombined much quicker at the n⁺ buffer layer, compared to the uniformly doped n⁻ epitaxial drift region by establishing a different dopant gradient near the n⁺ buffer layer. It should be noted that the drift region can also be a non-epitaxial silicon substrate. Although epitaxy enhances lifetime, it is not mandatory. Different layers of dopant regions can be transferred through wafer to wafer bonding (or other similar transfer mechanisms) for eventual device fabrication. The “reverse recovery time” for an IGBT is significantly improved due to the optimized graded dopant in the so called “drift region” as well as at the interfaces of the drift region. Graded dopants can also be implemented in the n⁺ buffer layer as well as other regions adjacent to the respective layers. Two important performance enhancements are the result of dopant gradients. For example, in an n-channel IGBT, electrons can be swept from source to drain rapidly, while at the same time holes can be recombined closer to the n⁺ buffer layer. This can improve t_{on} and t_{off} in the same device.

As illustrated in FIGS. 5A, 5B, and 5C, donor gradient is also of benefit to very large scale integrated circuits (VLSI)—VLSI logic, DRAM, nonvolatile memory like NAND flash. Spurious minority carriers can be generated by clock switching in digital VLSI logic and memory ICs. These unwanted carriers can discharge dynamically-held “actively held high” nodes. In most cases, statically-held nodes (with V_{cc}) cannot be affected. Degradation of refresh time in DRAMs is one of the results, because the capacitor holds charge dynamically. Similarly, degradation of CMOS digital images in digital imaging ICs is another result of the havoc caused by minority carriers. Pixel and color resolution can be significantly enhanced in imaging ICs with the embodiments described herein. Creating “subterranean” recombination centers underneath the wells (gold doping, platinum doping) as is done in some high-voltage diodes is not practical for VLSI circuits. Hence, a novel technique is described herein which creates a drift field to sweep these unwanted minority carriers from the active circuitry at the surface into the substrate in a monolithic die as quickly as possible. In a preferred embodiment, the subterranean n⁻ layer has a graded donor concentration to sweep the minority carriers deep into the substrate. One or more of such layers can also be implemented through wafer to wafer

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bonding or similar “transfer” mechanisms. This n⁻ layer can be a deeply-implanted layer. It can also be an epitaxial layer. As desired, the n⁻ well and p⁻ wells can also be graded or retrograded in dopants to sweep those carriers away from the surface as well. The graded dopant can also be implemented in surface channel MOS devices to accelerate majority carriers towards the drain. To decrease programming time in nonvolatile memory devices, carriers should be accelerated towards the surface when programming of memory cells is executed. The graded dopant can also be used to fabricate superior Junction Field-Effect transistors where the “channel pinch-off” is controlled by a graded channel instead of a uniformly doped channel (as practiced in the prior art).

One of ordinary skill and familiarity in the art will recognize that the concepts taught herein can be customized and tailored to a particular application in many advantageous ways. For instance, minority carriers can be channeled to the surface to aid programming in nonvolatile memory devices (NOR, NAND, multivalued-cell). Moreover, single-well, and triple-well CMOS fabrication techniques can also be optimized to incorporate these embodiments individually and collectively. Any modifications of such embodiments (described here) fall within the spirit and scope of the invention. Hence, they fall within the scope of the claims described below.

Although the invention has been described with reference to specific embodiments, these descriptions are not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as alternative embodiments of the invention will become apparent to persons skilled in the art upon reference to the description of the invention. It should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

It is therefore, contemplated that the claims will cover any such modifications or embodiments that fall within the true scope of the invention.

What is claimed is:

1. A semiconductor device, comprising:
 - a substrate of a first doping type at a first doping level having first and second faces;
 - a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
 - a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
 - transistors formed in at least one of the first active region or second active region; and
 - at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.
2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.
3. The semiconductor device of claim 1, wherein the substrate is an n-type substrate.
4. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a non-epitaxial substrate.

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5. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.

6. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.

7. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.

8. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.

9. A semiconductor device, comprising:

a substrate of a first doping type at a first doping level having first and second surfaces;

a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof; transistors formed in at least one of the first active region or second active region; and

at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate.

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10. The semiconductor device of claim 9, wherein the substrate is a p-type substrate.

11. The semiconductor device of claim 9, wherein the substrate is an n-type substrate.

12. The semiconductor device of claim 9, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

13. The semiconductor device of claim 9, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.

14. The semiconductor device of claim 9, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.

15. The semiconductor device of claim 9, wherein the first active region and second active region are each separated by at least one isolation region.

16. The semiconductor device of claim 9, wherein the graded dopant is fabricated with an ion implantation process.

17. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.

18. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring a source, a drain, a gate and a channel region.

* * * * *

EXHIBIT 4



US010734481B2

(12) **United States Patent**
Rao

(10) **Patent No.:** **US 10,734,481 B2**

(45) **Date of Patent:** **Aug. 4, 2020**

(54) **SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS**

H01L 29/7395 (2013.01); *H01L 27/0214* (2013.01); *H01L 27/10844* (2013.01)

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(58) **Field of Classification Search**

CPC *H01L 29/1095*

USPC 257/25

See application file for complete search history.

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(56)

References Cited

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

U.S. PATENT DOCUMENTS

4,001,864 A 1/1977 Gibbons
4,160,985 A 7/1979 Kamins et al.

(Continued)

(21) Appl. No.: **16/717,950**

(22) Filed: **Dec. 17, 2019**

OTHER PUBLICATIONS

(65) **Prior Publication Data**

US 2020/0127095 A1 Apr. 23, 2020

P.D. Moor, Advanced CMOS-based pixel sensors, <https://indico.cern.ch/event/122027/contributions/88236/attachments/69340/99377/FEEimecPdM.pdf>, 2011, 41 pages.

(Continued)

Related U.S. Application Data

(60) Continuation of application No. 15/590,282, filed on May 9, 2017, now Pat. No. 10,510,842, which is a continuation of application No. 14/931,636, filed on Nov. 3, 2015, now Pat. No. 9,647,070, which is a continuation of application No. 14/515,584, filed on (Continued)

Primary Examiner — Ajay Arora

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(51) **Int. Cl.**

H01L 29/06 (2006.01)

H01L 29/10 (2006.01)

H01L 29/36 (2006.01)

H01L 29/739 (2006.01)

H01L 27/146 (2006.01)

H01L 27/11524 (2017.01)

H01L 27/11521 (2017.01)

H01L 27/02 (2006.01)

H01L 27/108 (2006.01)

(52) **U.S. Cl.**

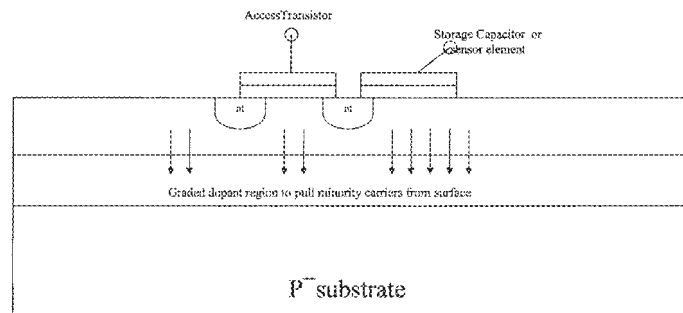
CPC *H01L 29/1095* (2013.01); *H01L 27/11521* (2013.01); *H01L 27/11524* (2013.01); *H01L 27/14643* (2013.01); *H01L 29/36* (2013.01);

(57)

ABSTRACT

Most semiconductor devices manufactured today, have uniform dopant concentration, either in the lateral or vertical device active (and isolation) regions. By grading the dopant concentration, the performance in various semiconductor devices can be significantly improved. Performance improvements can be obtained in application specific areas like increase in frequency of operation for digital logic, various power MOSFET and IGBT ICs, improvement in refresh time for DRAMs, decrease in programming time for nonvolatile memory, better visual quality including pixel resolution and color sensitivity for imaging ICs, better sensitivity for varactors in tunable filters, higher drive capabilities for JFETs, and a host of other applications.

36 Claims, 10 Drawing Sheets



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Related U.S. Application Data

Oct. 16, 2014, now Pat. No. 9,190,502, which is a continuation of application No. 13/854,319, filed on Apr. 1, 2013, now abandoned, which is a continuation of application No. 11/622,496, filed on Jan. 12, 2007, now Pat. No. 8,421,195, which is a division of application No. 10/934,915, filed on Sep. 3, 2004, now abandoned.

(56)

References Cited**U.S. PATENT DOCUMENTS**

4,347,654 A 9/1982 Allen et al.
 4,481,522 A 11/1984 Jastrzebski et al.
 4,866,000 A 9/1989 Okita
 5,029,277 A 7/1991 Kane
 5,130,262 A 7/1992 Masquelier et al.
 5,213,988 A 5/1993 Yamauchi et al.
 5,262,345 A 11/1993 Nasser et al.
 5,329,144 A 7/1994 Luryi
 5,448,087 A 9/1995 Streit et al.
 5,480,816 A 1/1996 Uga et al.
 5,496,746 A 3/1996 Matthews
 5,517,052 A 5/1996 Ishaque
 5,569,612 A 10/1996 Frisina et al.
 5,575,862 A 11/1996 Nishida
 5,637,898 A 6/1997 Baliga
 5,797,999 A 8/1998 Sannomiya et al.
 5,888,857 A 3/1999 Zhang et al.
 5,973,575 A 10/1999 Kamogawa et al.
 6,211,028 B1 4/2001 Tsai et al.
 6,310,366 B1 10/2001 Rhodes et al.
 RE37,441 E 11/2001 Yamazaki
 6,452,086 B1 9/2002 Muller
 6,465,862 B1 10/2002 Harris
 6,472,715 B1 10/2002 Liu et al.
 6,670,544 B2 12/2003 Kibbel et al.
 6,683,343 B2 1/2004 Matsudai et al.
 6,696,314 B2 2/2004 Rhodes
 6,706,550 B2 3/2004 Lee et al.
 6,713,813 B2 3/2004 Marchant
 6,720,622 B1 4/2004 Yu
 6,737,722 B2 5/2004 Yamamoto et al.
 6,744,117 B2 6/2004 Dragon et al.
 6,747,883 B2 6/2004 Yasumura
 6,753,202 B2 6/2004 Chen et al.
 6,754,093 B2 6/2004 Lien
 6,756,616 B2 6/2004 Rhodes
 6,780,713 B2 8/2004 Bromberger et al.
 6,831,292 B2 12/2004 Currie et al.
 6,878,603 B2 4/2005 Bromberger et al.
 6,921,946 B2 7/2005 Kenney et al.
 6,933,215 B2 8/2005 Bromberger et al.
 7,064,385 B2 6/2006 Dudek et al.

7,115,925 B2 10/2006 Rhodes
 7,233,044 B2 6/2007 Dudek
 7,307,327 B2 12/2007 Bahl et al.
 7,504,692 B2 3/2009 Dudek et al.
 8,164,124 B2 4/2012 Liu et al.
 8,421,195 B2 4/2013 Rao
 9,190,502 B2 11/2015 Rao
 9,647,070 B2 5/2017 Rao
 10,510,842 B2 12/2019 Rao
 2001/0040622 A1 11/2001 Maruyama
 2002/0056883 A1 5/2002 Baliga
 2002/0074585 A1 6/2002 Tsang et al.
 2002/0084430 A1 7/2002 Bamji et al.
 2002/0093281 A1 7/2002 Cathey
 2002/0102783 A1 8/2002 Fujimoto et al.
 2002/0134419 A1 9/2002 Maoris
 2003/0026126 A1 2/2003 Uemura
 2003/0030488 A1* 2/2003 Hueting H01L 29/0821
 330/57
 2003/0042511 A1 3/2003 Rhodes
 2004/0027753 A1 2/2004 Friedrichs et al.
 2004/0063288 A1 4/2004 Kenney et al.
 2006/0113592 A1 6/2006 Pendharkar et al.
 2007/0045682 A1* 3/2007 Hong H01L 27/14601
 257/292
 2012/0048462 A1 3/2012 Lee
 2013/0001661 A1 1/2013 Mao et al.
 2015/0200314 A1 7/2015 Webster

OTHER PUBLICATIONS

E. Parton, CMOS Sensors, Laser Focus World, <http://www.laserfocusworld.com/articles/print/volume-49/issue-10/features/cmos-sensors-cmos-based-specialty-imagers-reach-new-performance-levels.html>, Oct. 14, 2013, 5 pages.
 Z. Cao, Design of Pixel for High Speed CMOS Image Sensors, http://www.imagesensors.org/Past%20Workshops/2013%20Workshop/2013%20Papers/07-11_072-Cao_papers.pdf, 4 pages.
 M. Tanenbaum, BSTJ: Diffused Emitter and Base Silicon Transistors, The Bell System Technical Journal, Jan. 1956, 22 pages, vol. XXXV, <https://archive.org/details/bstj35-1-1>.
 IMEC Image Sensors and Vision Systems, <http://www2.imec.be/content/user/File/Brochures/cmos%20imagers%20brochure-april126.pdf>, Apr. 2014, 2 pages.
 A.S. Grove, Physics and Technology of Semiconductor Devices, John Wiley Sons, Inc., New York, Nov. 1967.
 W. Murray Bullis and W. R. Runyan, Influence of Mobility and Lifetime Variations on Drift-Field Effects in Silicon-Junction Devices, IEEE Transactions on Electron Devices, vol. Ed-14, No. 2, Feb. 1967.
 Berinder Brar et al., Herb's Bipolar Transistors, IEEE Transactions on Electron Devices, vol. 48, No. 11, Nov. 2001.

* cited by examiner

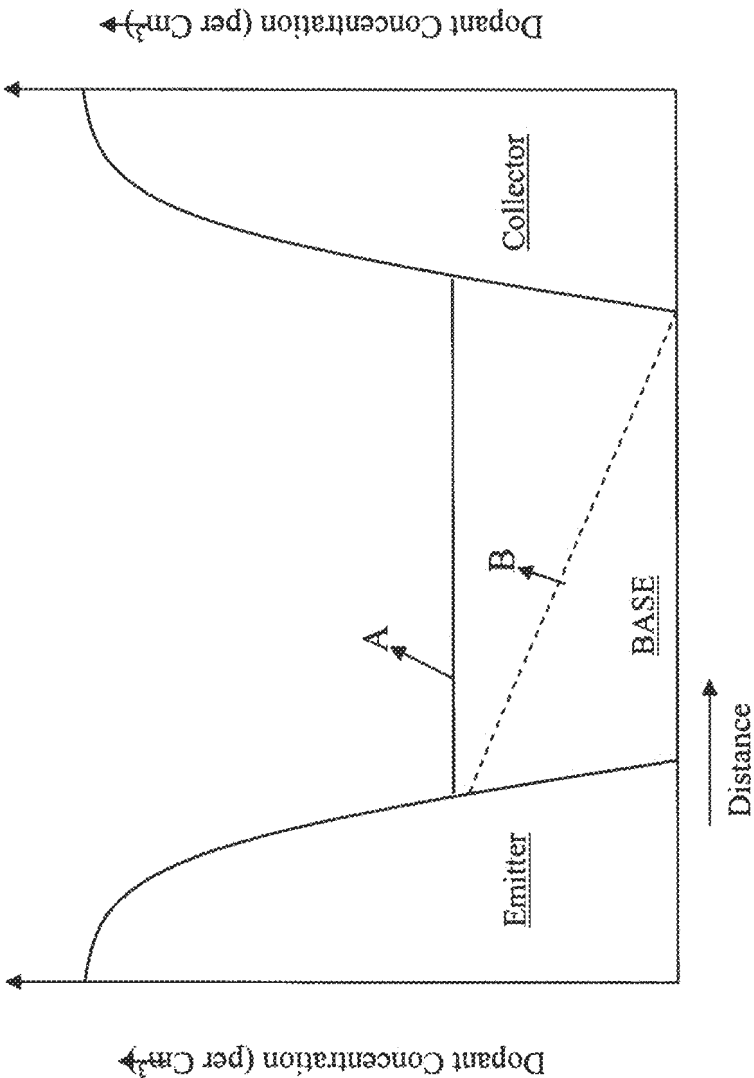


Figure 1 Prior Art

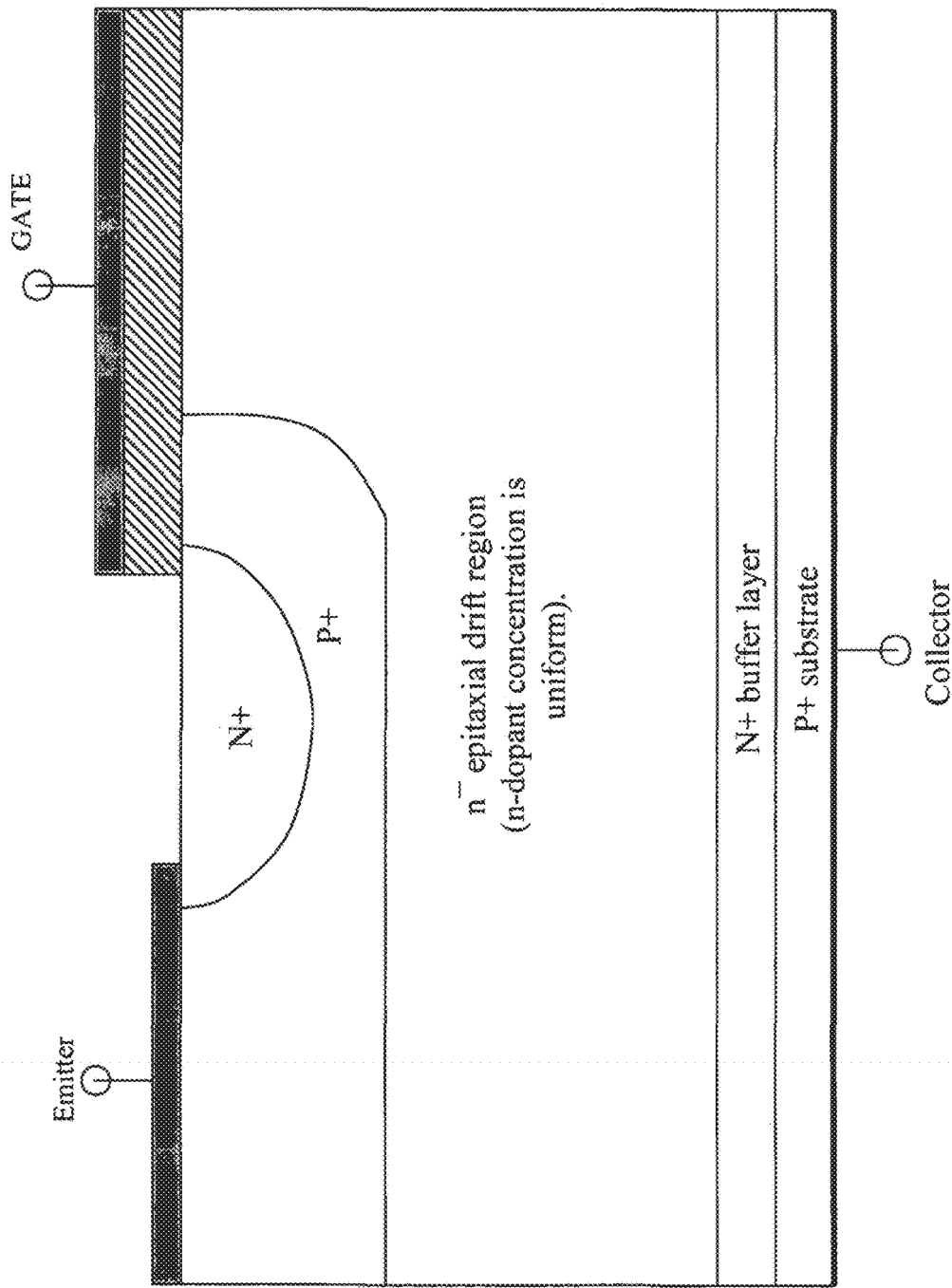


FIGURE 2 Prior art

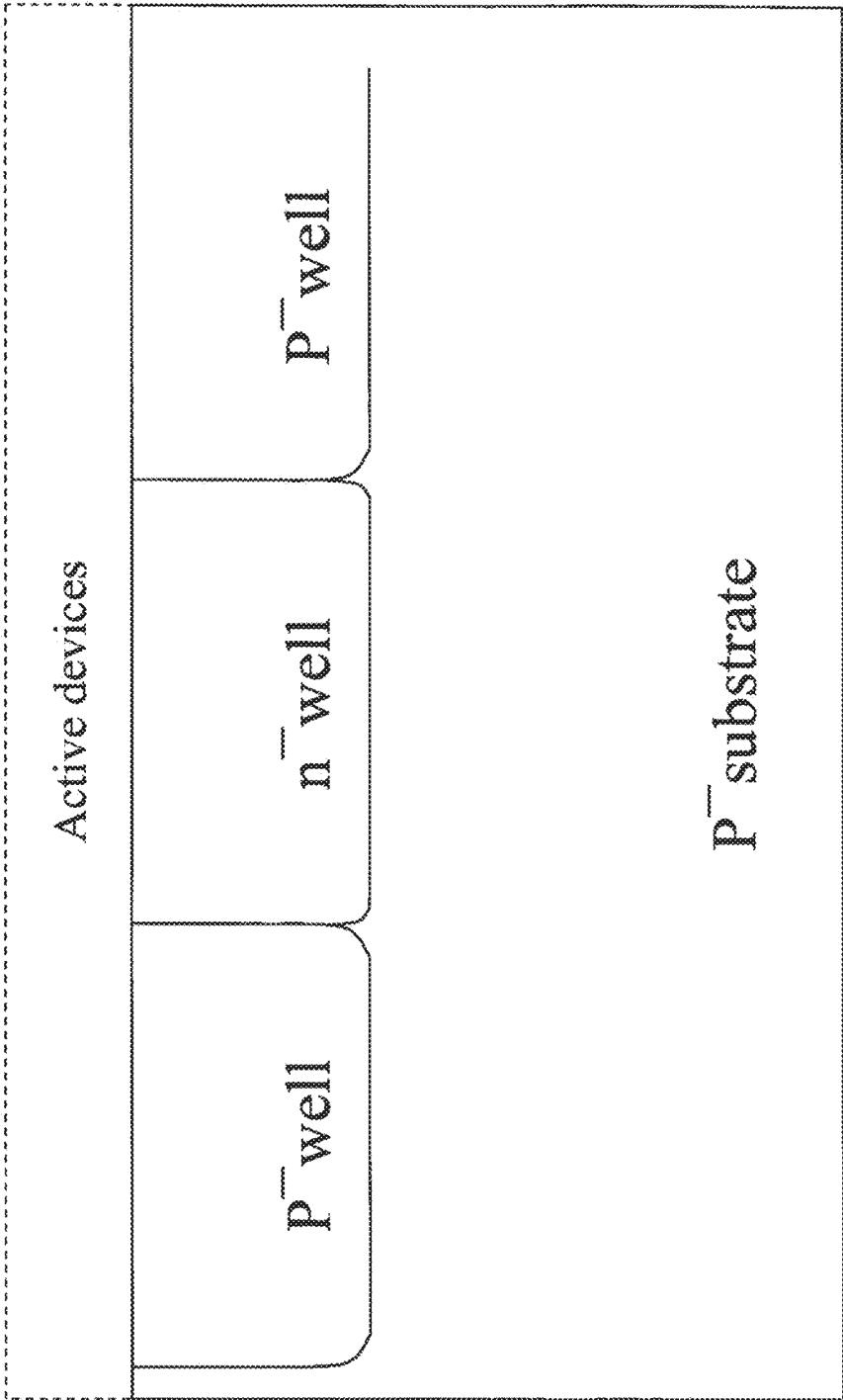


FIGURE 3A Prior art (Twin well CMOS) for a CMOS integrated circuit

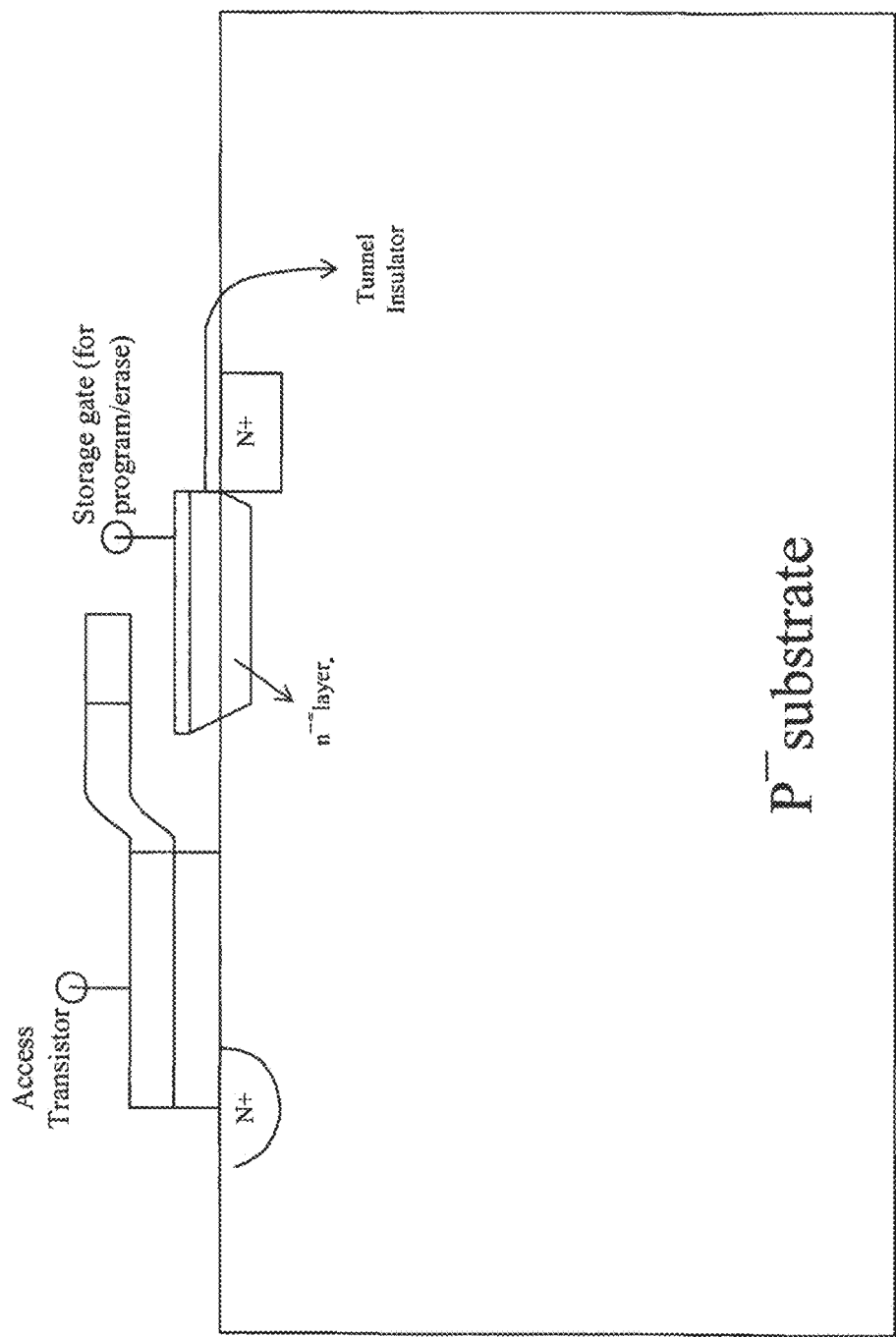


FIGURE 3B Prior art for a two-device EEPROM memory cell

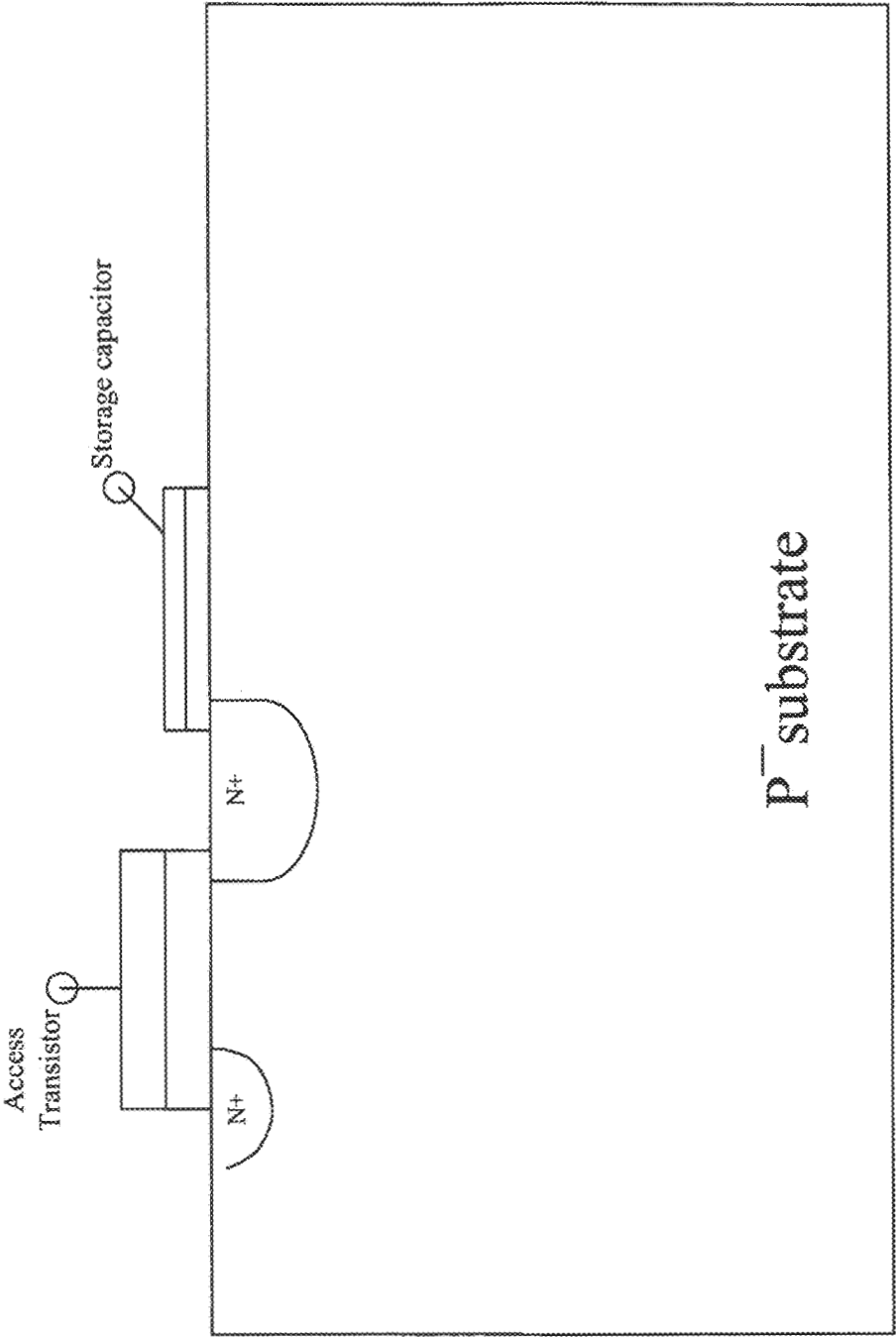


FIGURE 3C Prior art for a 1T-1C DRAM memory cell

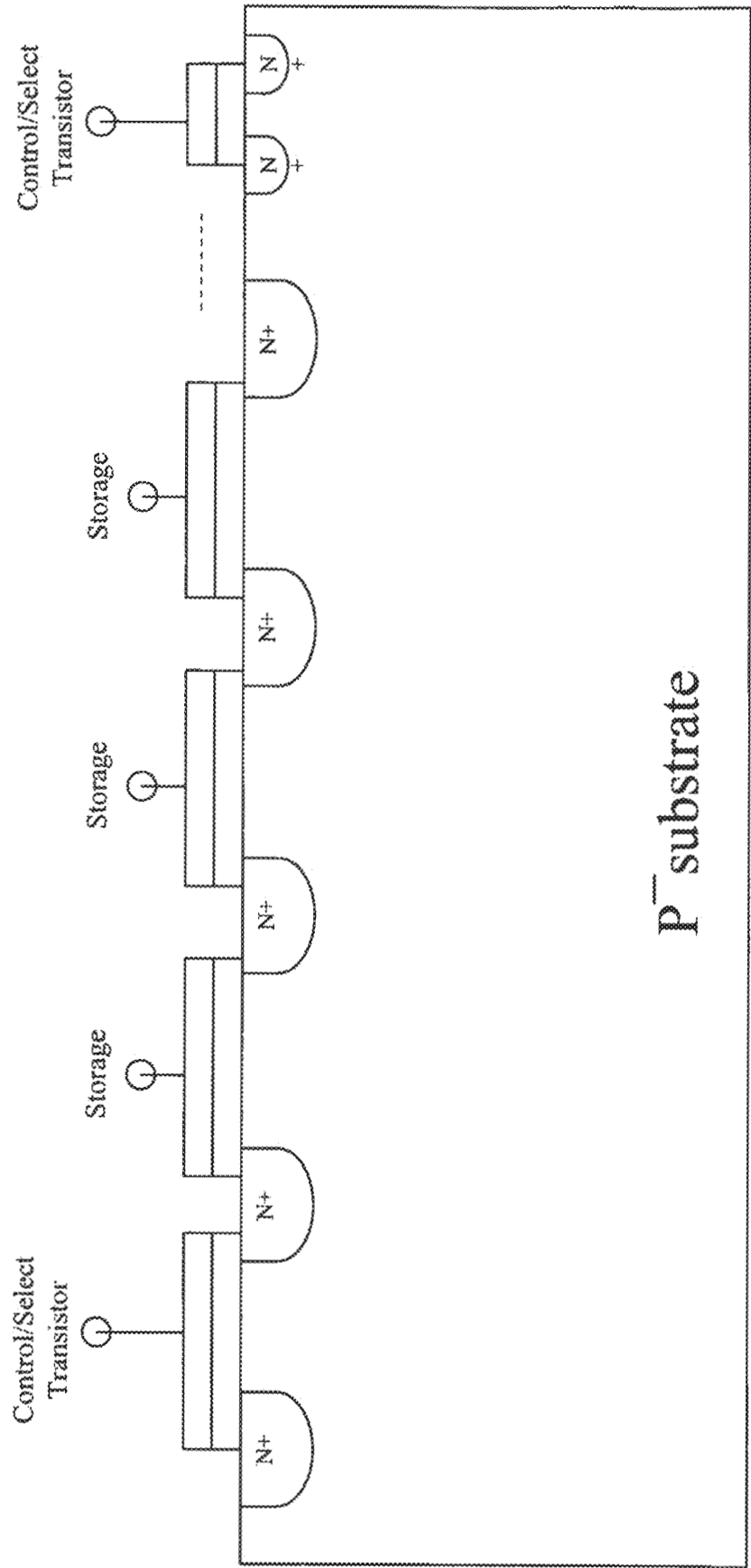


FIGURE 3D Prior art for a NAND flash memory cell

Note: Control/ Sect transistors have a single insulator - traditional MOS transistor.
Storage nodes have a stacked gate structure, typically with a floating gate and control gate comprising the stack.

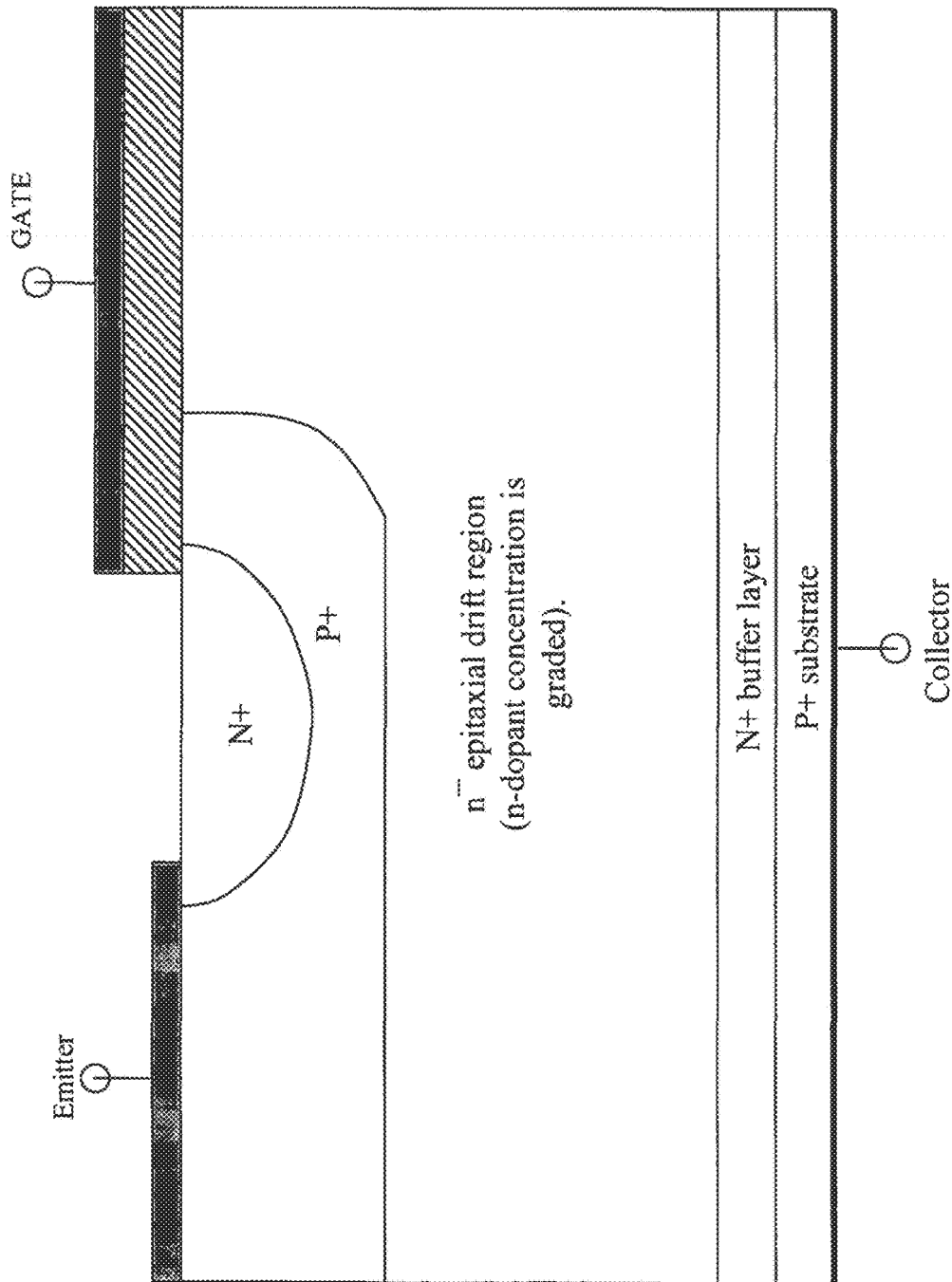


FIGURE 4 A dopant - concentration graded drift region in a IGBT

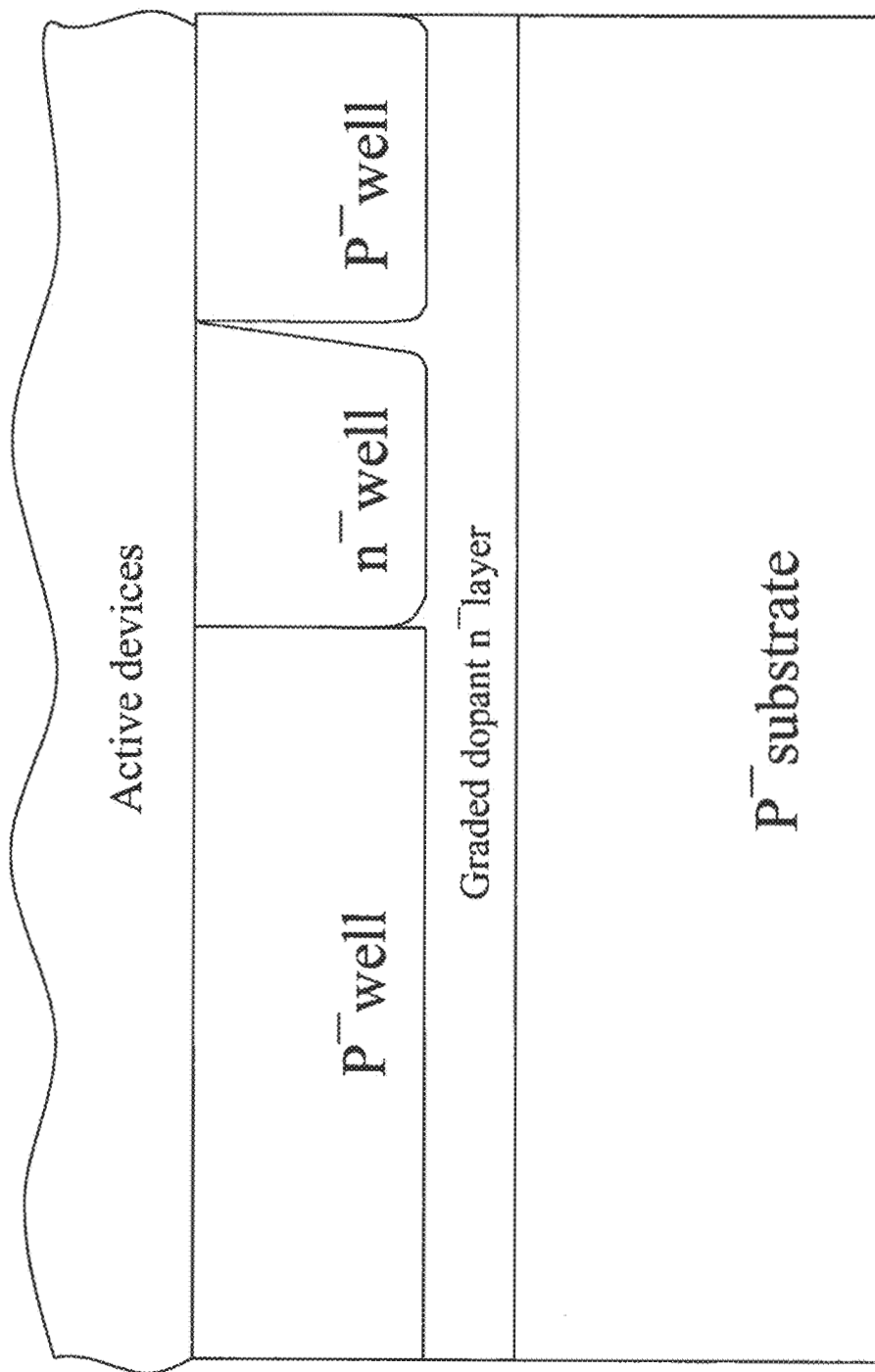


FIGURE 5A A CMOS Substrate for digital, mixed, signal, and sensors IC's

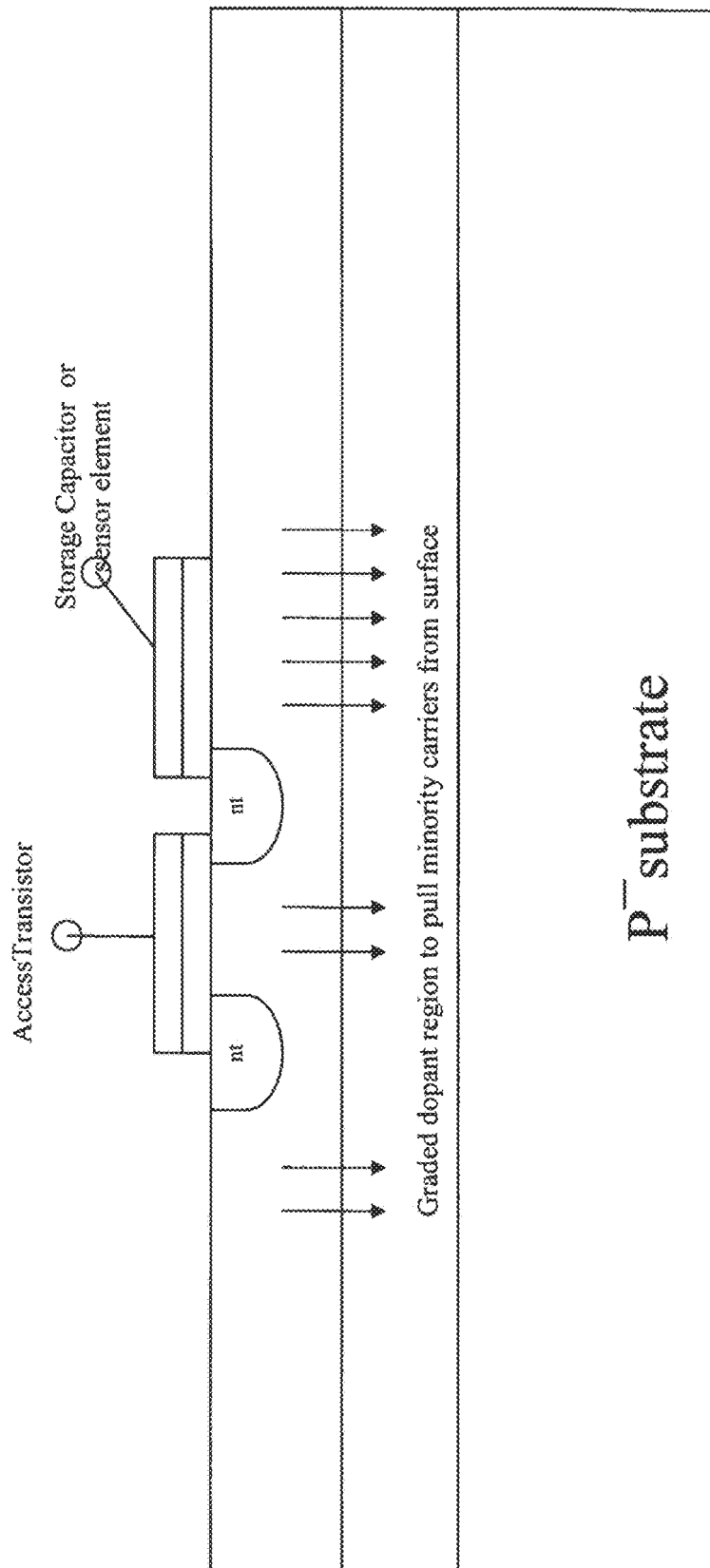


FIGURE 5B CMOS Substrate for a DRAM or image sensor, with one embodiment of the invention

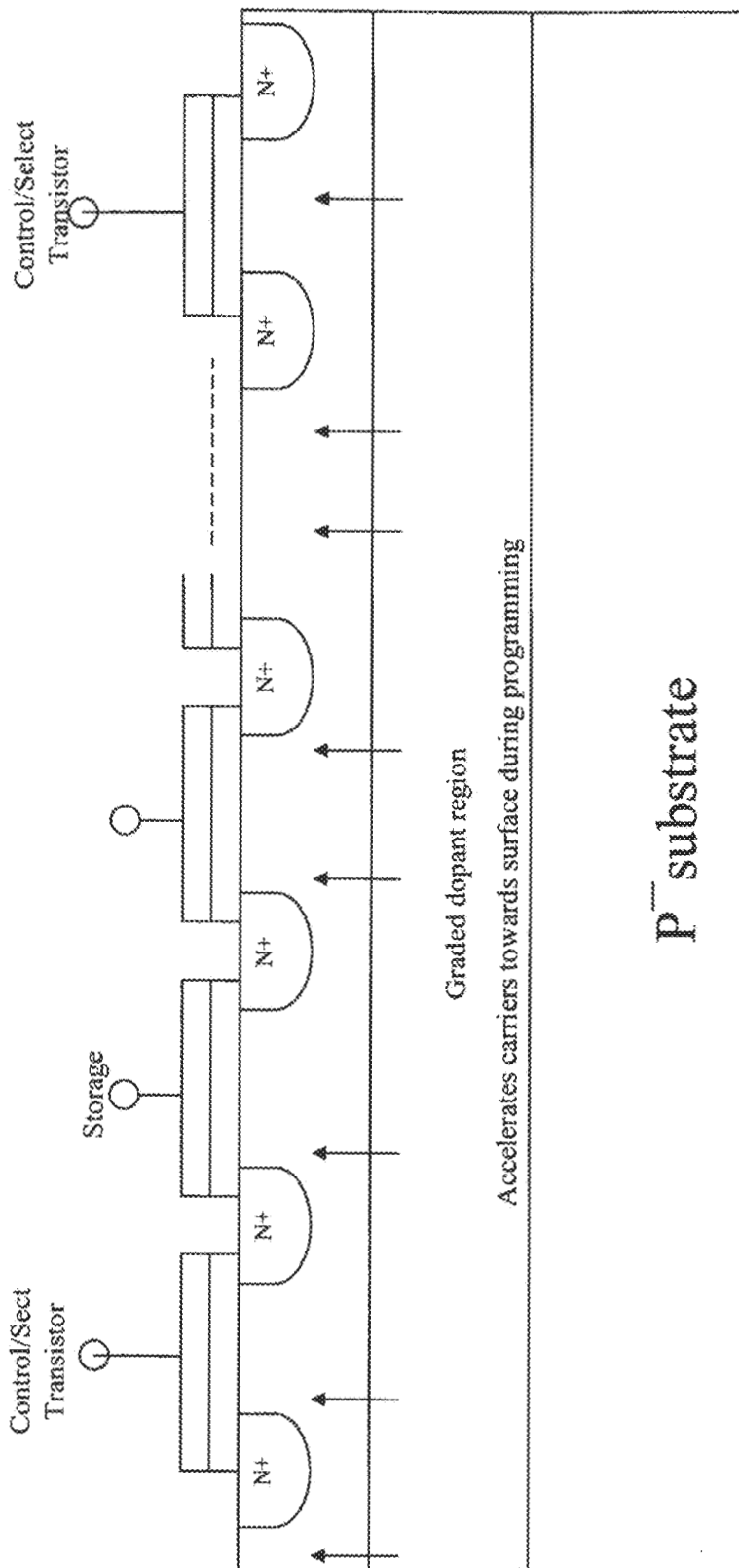


FIGURE 5C CMOS Substrate for a NAND flash device to improve programming times

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SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a Continuation of U.S. patent application Ser. No. 15/590,282, filed May 9, 2017, published on Aug. 24, 2017, as U.S. Publication No. 2017-0243876. application Ser. No. 15/590,282 is a continuation of U.S. patent application Ser. No. 14/931,636, filed Nov. 3, 2015, published on Jun. 16, 2016 as U.S. Publication No. 2016-0172447, now U.S. Pat. No. 9,647,070, issued on May 9, 2017. Application Ser. No. 14/931,636 is a continuation of U.S. patent application Ser. No. 14/515,584, filed Oct. 16, 2014, published on Feb. 5, 2015, as U.S. Publication No. 2015-0035004, now U.S. Pat. No. 9,190,502, issued on Nov. 17, 2015. Application Ser. No. 14/515,584 is a Continuation of U.S. patent application Ser. No. 13/854,319 filed Apr. 1, 2013, published on Aug. 29, 2013, as U.S. Publication No. 2013-0221488. Application Ser. No. 13/854,319 is a Continuation of Ser. No. 11/622,496, filed Jan. 12, 2007, published on Jul. 12, 2007, as Publication No. 2007-0158790, now U.S. Pat. No. 8,421,195, issued on Apr. 16, 2013. Application Ser. No. 11/622,496, is a Division of U.S. patent application Ser. No. 10/934,915, filed Sep. 3, 2004, published on Mar. 9, 2006, as U.S. Publication No. 2006-0049464. U.S. Pat. Nos. 9,647,070, 9,190,502, and 8,421,195, and Patent Application Publication Nos. 2017-0243876, 2016-0172447, 2015-0035004, 2013-0221488, 2007-0158790, and 2006-0049464, are incorporated herein by reference in their entirety.

TECHNICAL FIELD

This present invention relates to all semiconductor devices and systems. Particularly it applies to diffused diodes, avalanche diodes, Schottky devices, power MOS transistors, JFET's, RF bipolar transistors, IGBTs (Insulated Gate Bipolar Transistors), varactors, digital VLSI, mixed signal circuits and sensor devices including camera ICs employing CCD (Charge Coupled Device) as well as CMOS technologies.

BACKGROUND

Bipolar Junction Transistors (BJT) are classified as minority carrier devices because minority carriers are the principle device conduction mechanism. However, majority carriers also play a small but finite role in modulating the conductivity in BJTs. Consequently, both carriers (electrons and holes) play a role in the switching performance of BJTs. The maximum frequency of operation in BJTs is limited by the base transit time as well as the quick recombination of the majority carriers when the device is switched off (prior to beginning the next cycle). The dominant carrier mechanism in BJTs is carrier diffusion. The carrier drift current component is fairly small, especially in uniformly doped base BJTs. Efforts have been made in graded base transistors to create an aiding drift field to enhance the diffusing minority carrier's speed from emitter to collector. However, most semiconductor devices, including various power MOSFETs (traditional, DMOS, lateral, vertical and a host of other configurations), IGBT's (Insulated Gated Base Transistors), still use a uniformly doped 'drift epitaxial' region in the base. FIG. 1 shows the relative doping concentration versus distance in a BJT. FIG. 2 shows the uniformly doped epi

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region in an IGBT. In contrast to BJTs, MOS devices are majority carrier devices for conduction. The conduction is channel dominated. The channel can be a surface in one plane in planar devices. The surface can also be on the sidewalls in a vertical device. Other device architectures to combine planar and vertical conduction are also possible. The maximum frequency of operation is dictated primarily by source-drain separation distance. Most MOS devices use a uniformly doped substrate (or a well region). When a MOSFET is optimally integrated with a BJT in a monolithic fashion, an IGBT results. The IGBT inherits the advantages of both MOSFET and BJT. It also brings new challenges because the required characteristics (electron transit and hole recombination as fast as possible in n-channel IGBT) necessitate different dopant gradients either in the same layer at different positions, or at the interfaces of similar or dissimilar layers.

Retrograde wells have been attempted, with little success, to help improve soft error immunity in SRAMs and visual quality in imaging circuits. FIG. 3A shows a typical CMOS VLSI device employing a twin well substrate, on which active devices are subsequently fabricated. FIGS. 3B, 3C, and 3D illustrate device cross sections, as practiced today. Retrograde and halo wells have also been attempted to improve refresh time in DRAMs (dynamic random-access memories), as well as, reducing dark current (background noise) and enhance RGB (Red, Green, Blue) color resolution in digital camera ICs. Most of these techniques either divert the minority carriers away from the active regions of critical charge storage nodes at the surface, or, increase minority carrier density locally as the particular application requires.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. 1 illustrates the relative doping profiles of emitter, base and collector for the two most popular bipolar junction transistors: namely, uniform base ("A") and graded base ("B");

FIG. 2 illustrates the cross section of a commercial IGBT with a uniform epitaxial drift region (base);

FIGS. 3A, 3B, 3C, and 3D illustrate cross sections of commonly used prior art CMOS silicon substrates; FIG. 3A showing a typical prior art IC with two wells (one n⁻ well in which p-channel transistors are subsequently fabricated and one p⁻ well in which n-channel transistors are subsequently fabricated); FIG. 3B showing a prior art EEPROM (Electrically Erasable Programmable Read-Only Memory) memory cell having a tunnel insulator; FIG. 3C showing a prior art DRAM memory cell; and FIG. 3D showing a prior art NAND flash memory cell;

FIG. 4 illustrates the cross section of an IGBT, using one embodiment of the invention described here, where the dopant is optimally graded in the epitaxial drift region; and

FIGS. 5A, 5B, and 5C illustrate the cross sections of a CMOS silicon substrate with two wells and an underlying layer using embodiments of the invention to improve performance in each application—VLSI logic, DRAM/image IC, nonvolatile memory IC.

DETAILED DESCRIPTION

The relative doping concentrations of emitter and collector regions varies from 10¹⁸ to 10²⁰ cm⁻³ and from the 2023

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region is 10^{14} to $10^{16}/\text{cm}^3$ depending on the desired characteristics of the BJT. In graded base p-n-p transistors, the donor dopant concentration may be 10 to 100× at the emitter-base junction, relative to the base-collector junction (1×). The gradient can be linear, quasi linear, exponential or complimentary error function. The relative slope of the donor concentration throughout the base creates a suitable aiding drift electric field, to help the holes (p-n-p transistor) transverse from emitter to collector. Since the aiding drift electric field helps hole conduction, the current gain at a given frequency is enhanced, relative to a uniformly-doped (base) BJT. The improvement in cut-off frequency (or, frequency at unity gain, f_T) can be as large as 2×-5×. Similar performance improvements are also applicable to n-p-n transistors.

As illustrated in FIG. 4, in one embodiment according to the invention, a donor gradient is established from the emitter-drift epitaxial base region junction of the punch-through IGBT, to the drift epitaxial base region— n^+ buffer layer boundary (electrons in this case are accelerated in their transit from emitter to collector). The “average” base resistance is optimized so that conductivity modulation and lifetime (for minority carriers) in the base region are not compromised. By sweeping the carriers towards the n^+ buffer region a number of advantages are obtained. First, the frequency of operation (combination of t_{on} and t_{off} as is known in the IGBT commercial nomenclature) can be enhanced. Second, and maybe more importantly, during t_{off} , holes can be recombined much quicker at the n^+ buffer layer, compared to the uniformly doped n^- epitaxial drift region by establishing a different dopant gradient near the n^+ buffer layer. It should be noted that the drift region can also be a non-epitaxial silicon substrate. Although epitaxy enhances lifetime, it is not mandatory. Different layers of dopant regions can be transferred through wafer to wafer bonding (or other similar transfer mechanisms) for eventual device fabrication. The “reverse recovery time” for an IGBT is significantly improved due to the optimized graded dopant in the so called “drift region” as well as at the interfaces of the drift region. Graded dopants can also be implemented in the n^+ buffer layer as well as other regions adjacent to the respective layers. Two important performance enhancements are the result of dopant gradients. For example, in an n-channel IGBT, electrons can be swept from source to drain rapidly, while at the same time holes can be recombined closer to the n^+ buffer layer. This can improve t_{on} and t_{off} in the same device.

As illustrated in FIGS. 5A, 5B, and 5C, donor gradient is also of benefit to very large scale integrated circuits (VLSI)—VLSI logic, DRAM, nonvolatile memory like NAND flash. Spurious minority carriers can be generated by clock switching in digital VLSI logic and memory ICs. These unwanted carriers can discharge dynamically-held “actively held high” nodes. In most cases, statically-held nodes (with V_{cc}) cannot be affected. Degradation of refresh time in DRAMs is one of the results, because the capacitor holds charge dynamically. Similarly, degradation of CMOS digital images in digital imaging ICs is another result of the havoc caused by minority carriers. Pixel and color resolution can be significantly enhanced in imaging ICs with the embodiments described herein. Creating “subterranean” recombination centers underneath the wells (gold doping, platinum doping) as is done in some high-voltage diodes is not practical for VLSI circuits. Hence, a novel technique is described herein which creates a drift field to sweep these unwanted minority carriers from the active circuitry at the surface into the substrate in a monolithic die as quickly as

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possible. In a preferred embodiment, the subterranean n^- layer has a graded donor concentration to sweep the minority carriers deep into the substrate. One or more of such layers can also be implemented through wafer to wafer bonding or similar “transfer” mechanisms. This n^- layer can be a deeply-implanted layer. It can also be an epitaxial layer. As desired, the n^- well and p^- wells can also be graded or retrograded in dopants to sweep those carriers away from the surface as well. The graded dopant can also be implemented in surface channel MOS devices to accelerate majority carriers towards the drain. To decrease programming time in nonvolatile memory devices, carriers should be accelerated towards the surface when programming of memory cells is executed. The graded dopant can also be used to fabricate superior Junction Field-Effect transistors where the “channel pinch-off” is controlled by a graded channel instead of a uniformly doped channel (as practiced in the prior art).

One of ordinary skill and familiarity in the art will recognize that the concepts taught herein can be customized and tailored to a particular application in many advantageous ways. For instance, minority carriers can be channeled to the surface to aid programming in nonvolatile memory devices (NOR, NAND, multivalued-cell). Moreover, single-well, and triple-well CMOS fabrication techniques can also be optimized to incorporate these embodiments individually and collectively. Any modifications of such embodiments (described here) fall within the spirit and scope of the invention. Hence, they fall within the scope of the claims described below.

Although the invention has been described with reference to specific embodiments, these descriptions are not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as alternative embodiments of the invention will become apparent to persons skilled in the art upon reference to the description of the invention. It should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

It is therefore, contemplated that the claims will cover any such modifications or embodiments that fall within the true scope of the invention.

What is claimed is:

1. A semiconductor device, comprising:

- a substrate of a first doping type at a first doping level having first and second surfaces;
- a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
- a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
- transistors formed in at least one of the first active region or second active region;
- at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and
- at least one well region adjacent to the first or second active region containing at least one graded dopant

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region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.

2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.

3. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

4. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.

5. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.

6. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.

7. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.

8. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.

9. The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.

10. The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region are both p-type and n-type.

11. The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the second active region are both p-type and n-type.

12. The semiconductor device of claim 1, wherein dopants of the graded dopant region in the well region are both p-type and n-type.

13. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring at least a source, a drain, a gate and a channel.

14. The semiconductor device of claim 1, wherein the device is a dynamic random access memory (DRAM).

15. The semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.

16. The semiconductor device of claim 1, wherein the device is a flash memory.

17. The semiconductor device of claim 1, wherein the device is a logic device.

18. The semiconductor device of claim 17, wherein the device is central processing unit.

19. The semiconductor device of claim 1, wherein the device is an image sensor.

20. A semiconductor device, comprising:

a substrate of a first doping type at a first doping level having first and second surfaces;

a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;

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a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof; transistors formed in at least one of the first active region or second active region;

at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate; and

at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.

21. The semiconductor device of claim 20, wherein the substrate is an n-type substrate.

22. The semiconductor device of claim 20, wherein the substrate is a p-type substrate.

23. The semiconductor device of claim 20, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

24. The semiconductor device of claim 20, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.

25. The semiconductor device of claim 20, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.

26. The semiconductor device of claim 20, wherein the first active region and second active region are each separated by at least one isolation region.

27. The semiconductor device of claim 20, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.

28. The semiconductor device of claim 20, wherein dopants of the graded dopant concentration in the first active region are both p-type and n-type.

29. The semiconductor device of claim 20, wherein dopants of the graded dopant concentration in the second active region are both p-type and n-type.

30. The semiconductor device of claim 20, wherein dopants of the graded dopant region in the well region are both p-type and n-type.

31. The semiconductor device of claim 20, wherein the graded dopant is fabricated with an ion implantation process.

32. The semiconductor device of claim 20, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.

33. The semiconductor device of claim 20, wherein the device is a flash memory.

34. The semiconductor device of claim 20, wherein the device is a logic device.

35. The semiconductor device of claim 34, wherein the device is central processing unit.

36. The semiconductor device of claim 20, wherein the device is an image sensor.

* * * * *

EXHIBIT 5



US011121222B2

(12) **United States Patent**
Rao

(10) **Patent No.:** **US 11,121,222 B2**
(45) **Date of Patent:** **Sep. 14, 2021**

(54) **SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **16/947,294**

(22) Filed: **Jul. 27, 2020**

(65) **Prior Publication Data**

US 2021/0005716 A1 Jan. 7, 2021

Related U.S. Application Data

(60) Continuation of application No. 16/717,950, filed on Dec. 17, 2019, now Pat. No. 10,734,481, which is a (Continued)

(51) **Int. Cl.**
H01L 29/10 (2006.01)
H01L 27/11524 (2017.01)
(Continued)

(52) **U.S. Cl.**
CPC **H01L 29/1095** (2013.01); **H01L 27/11521** (2013.01); **H01L 27/11524** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC H01L 29/1095
(Continued)

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,001,864 A 1/1977 Gibbons
4,160,985 A 7/1979 Kamins et al.
(Continued)

FOREIGN PATENT DOCUMENTS

JP s6482563 A 3/1989
JP 2003051551 A 2/2003
(Continued)

OTHER PUBLICATIONS

P.D. Moor, Advanced CMOS-based pixel sensors, <https://indico.cern.ch/event/122027/contributions/88236/attachments/69340/99377/FEEimecPdM.pdf>, 2011, 41 pages.

(Continued)

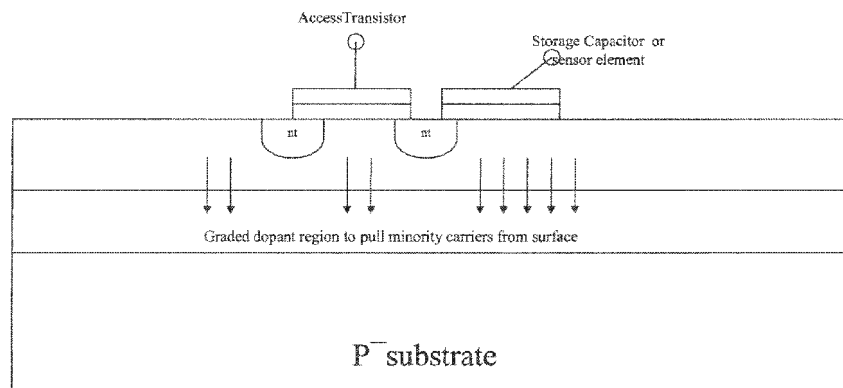
Primary Examiner — Ajay Arora

(74) *Attorney, Agent, or Firm* — Gregory M. Howison

(57) **ABSTRACT**

Most semiconductor devices manufactured today, have uniform dopant concentration, either in the lateral or vertical device active (and isolation) regions. By grading the dopant concentration, the performance in various semiconductor devices can be significantly improved. Performance improvements can be obtained in application specific areas like increase in frequency of operation for digital logic, various power MOSFET and IGBT ICs, improvement in refresh time for DRAMs, decrease in programming time for nonvolatile memory, better visual quality including pixel resolution and color sensitivity for imaging ICs, better sensitivity for varactors in tunable filters, higher drive capabilities for JFETs, and a host of other applications.

44 Claims, 10 Drawing Sheets



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Related U.S. Application Data

continuation of application No. 15/590,282, filed on May 9, 2017, now Pat. No. 10,510,842, which is a continuation of application No. 14/931,636, filed on Nov. 3, 2015, now Pat. No. 9,647,070, which is a continuation of application No. 14/515,584, filed on Oct. 16, 2014, now Pat. No. 9,190,502, which is a continuation of application No. 13/854,319, filed on Apr. 1, 2013, now abandoned, which is a continuation of application No. 11/622,496, filed on Jan. 12, 2007, now Pat. No. 8,421,195, which is a division of application No. 10/934,915, filed on Sep. 3, 2004, now abandoned.

(51) Int. Cl.

H01L 27/146 (2006.01)
H01L 27/11521 (2017.01)
H01L 29/739 (2006.01)
H01L 29/36 (2006.01)
H01L 27/02 (2006.01)
H01L 27/108 (2006.01)

(52) U.S. Cl.

CPC *H01L 27/14643* (2013.01); *H01L 29/36* (2013.01); *H01L 29/7395* (2013.01); *H01L 27/0214* (2013.01); *H01L 27/10844* (2013.01)

(58) Field of Classification Search

USPC 257/25
 See application file for complete search history.

(56)

References Cited

U.S. PATENT DOCUMENTS

4,347,654 A 9/1982 Allen et al.
 4,481,522 A 11/1984 Jastrzebski et al.
 4,684,971 A 8/1987 Payne
 4,688,063 A 8/1987 Lu et al.
 4,866,000 A 9/1989 Okita
 4,907,058 A 3/1990 Sakai
 4,994,887 A 2/1991 Hutter et al.
 5,029,277 A 7/1991 Kane
 5,130,262 A 7/1992 Masquelier et al.
 5,213,988 A 5/1993 Yamauchi et al.
 5,262,345 A 11/1993 Nasser et al.
 5,329,144 A 7/1994 Luryi
 5,448,087 A 9/1995 Streit et al.
 5,480,816 A 1/1996 Uga et al.
 5,496,746 A 3/1996 Matthews
 5,517,052 A 5/1996 Ishaque
 5,569,612 A 10/1996 Frisina et al.
 5,575,862 A 11/1996 Nishida
 5,637,898 A 6/1997 Baliga
 5,797,999 A 8/1998 Sannomiya et al.
 5,835,402 A 11/1998 Rao et al.
 5,888,857 A 3/1999 Zhang et al.
 5,973,575 A 10/1999 Kamogawa et al.
 6,025,237 A 2/2000 Choi
 6,211,028 B1 4/2001 Tsai et al.
 6,310,366 B1 10/2001 Rhodes et al.
 RE37,441 E 11/2001 Yamazaki
 6,384,431 B1 5/2002 Takahashi et al.
 6,452,086 B1 9/2002 Muller
 6,465,862 B1 10/2002 Harris
 6,472,715 B1 10/2002 Liu et al.
 6,670,544 B2 12/2003 Kibbel et al.
 6,683,343 B2 1/2004 Matsudai et al.
 6,696,314 B2 2/2004 Rhodes
 6,706,550 B2 3/2004 Lee et al.
 6,713,813 B2 3/2004 Marchant
 6,720,622 B1 4/2004 Yu
 6,737,722 B2 5/2004 Yamamoto et al.
 6,744,117 B2 6/2004 Dragon et al.

6,747,883 B2 6/2004 Yasumura
 6,753,202 B2 6/2004 Chen et al.
 6,754,093 B2 6/2004 Lien
 6,756,616 B2 6/2004 Rhodes
 6,780,713 B2 8/2004 Bromberger et al.
 6,831,292 B2 12/2004 Currie et al.
 6,878,603 B2 4/2005 Bromberger et al.
 6,921,946 B2 7/2005 Kenney et al.
 6,933,215 B2 8/2005 Bromberger et al.
 7,064,385 B2 6/2006 Dudek et al.
 7,115,925 B2 10/2006 Rhodes
 7,233,044 B2 6/2007 Dudek
 7,307,327 B2 12/2007 Bahl et al.
 7,504,692 B2 3/2009 Dudek et al.
 8,164,124 B2 4/2012 Liu et al.
 8,421,195 B2 4/2013 Rao
 9,190,502 B2 11/2015 Rao
 9,647,070 B2 5/2017 Rao
 10,510,842 B2 12/2019 Rao
 10,734,481 B2 8/2020 Rao
 2001/0028097 A1 10/2001 Matsuo et al.
 2001/0040622 A1 11/2001 Maruyama
 2002/0056883 A1 5/2002 Baliga
 2002/0074585 A1 6/2002 Tsang et al.
 2002/0084430 A1 7/2002 Bamji et al.
 2002/0093281 A1 7/2002 Cathey
 2002/0102783 A1 8/2002 Fujimoto et al.
 2002/0134419 A1 9/2002 Macris
 2002/0195656 A1 12/2002 Hattori
 2003/0026126 A1 2/2003 Uemura
 2003/0030488 A1 2/2003 Hueting et al.
 2003/0042511 A1 3/2003 Rhodes
 2003/0183856 A1 10/2003 Wiczorek
 2004/0027753 A1 2/2004 Friedrichs et al.
 2004/0063288 A1 4/2004 Kenney et al.
 2006/0113592 A1 6/2006 Pendharkar et al.
 2007/0045682 A1* 3/2007 Hong H01L 27/14689
 257/292
 2008/0142899 A1 6/2008 Morris
 2012/0048462 A1 3/2012 Lee
 2013/0001661 A1 1/2013 Mao et al.
 2014/0034997 A1* 2/2014 Rahimo H01L 29/861
 257/139
 2015/0200314 A1 7/2015 Webster
 2017/0243876 A1 8/2017 Rao

FOREIGN PATENT DOCUMENTS

JP 2003218356 A 7/2003
 WO 2004049453 A1 6/2004

OTHER PUBLICATIONS

E. Parton, CMOS Sensors, Laser Focus World, <http://www.laserfocusworld.com/articles/print/volume-49/issue-10/features/cmos-sensors-cmos-based-specialty-imagers-reach-new-performance-levels.html>, Oct. 14, 2013, 5 pages.
 Z. Cao, Design of Pixel for High Speed CMOS Image Sensors, http://www.imagesensors.org/Past%20Workshops/2013%20Workshop/2013%20Papers/07-11_072-Cao_papers.pdf, 4 pages.
 M. Tanenbaum, BSTJ: Diffused Emitter and Base Silicon Transistors, The Bell System Technical Journal, Jan. 1956, 22 pages, vol. XXXV, <https://archive.org/details/bstj35-1-1>.
 IMEC Image Sensors and Vision Systems, <http://www2.imec.be/content/user/File/Brochures/cmos%20imagers%20brochure-april26.pdf>, Apr. 2014, 2 pages.
 A.S. Grove, Physics and Technology of Semiconductor Devices, John Wiley Sons, Inc., New York, Nov. 1967.
 W. Murray Bullis and W. R. Runyan, Influence of Mobility and Lifetime Variations on Drift-Field Effects in Silicon-Junction Devices, IEEE Transactions on Electron Devices, vol. Ed-14, No. 2, Feb. 1967.
 Berinder Brar et al., Herb's Bipolar Transistors, IEEE Transactions on Electron Devices, vol. 48, No. 11, Nov. 2001.
 IPR2020-00288—Exhibit 1029—Claim Construction District Court 4 20-2020.

US 11,121,222 B2

Page 3

(56)

References Cited

OTHER PUBLICATIONS

IPR2020-00288—Exhibit 2007—Minutes for Markman Hearing Held via Video Conference Before U.S. District Judge Rodney Gilstrap, *Greenthread, LLC v. Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-CV-147-JRG, Dkt. 61.

IPR2020-00288—Petitioner Reply.

IPR2020-00289-00289 Petitioner Reply.

IPR2020-00292—Petition for IPR.

IPR2020-00292—Exhibit 2002—Excerpt from Exhibit 4 to Appendix B of Samsung Electronics Co., Ltd.’s Invalidity Contentions (Invalidity Contention based on U.S. Pat. No. 6,384,431 to Takahashi).

IPR2020-00288—Ex. 1020—Michael Nastasi and James W. Mayer, *Ion Implantation and Synthesis of Materials* (2006). 4 pages.

IPR2020-00288—Exhibit 2001—IPR2020-00288—Excerpt from Exhibit 1 to Appendix A of Samsung Electronics Co., Ltd.’s Invalidity Contentions regarding Morris.

IPR2020-00288—Exhibit 2002—Excerpt from Exhibit 2 to Appendix A of Samsung Electronics Co., Ltd.’s Invalidity Contentions regarding Miyamoto.

IPR2020-00288—Exhibit 2009—Complaint for Patent Infringement, *Greenthread, LLC v. Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-CV-147-JRG, Dkt. 1.

IPR2020-00288—Exhibit 2011—Exhibit A to Revised Joint Claim Construction Chart Pursuant to Patent Rule 4-5, *Greenthread, LLC v. Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-CV-147-JRG, Dkt. 60-1.

IPR2020-00288—Exhibit 2012—Samsungs Responsive Claim Construction Brief—District Court.

IPR2020-00288—Exhibit 2013—Glew Dec.

IPR2020-00288—Exhibit 2014—Excerpt from Exhibit 10 to Appendix A of Samsung Electronics Co., Ltd.’s Invalidity Contentions.

IPR2020-00288—Patent Owner Preliminary Response.

IPR2020-00288—Patent Owner Sur Reply.

IPR2020-00288—Petition.

IPR2020-00289—Exhibit 1 to Appendix C of Samsung Electronics Co., Ltd.’s Invalidity Contentions regarding Payne.

IPR2020-00289—Exhibit 1003—Smith Dec.

IPR2020-00289—Exhibit 1010—S. M. Sze et al., *Semiconductor Devices: Physics and Technology*, John Wiley & Sons, 2nd Ed., 2002 (“Sze ’02”).

IPR2020-00289—Exhibit 1012—Ben G. Streetman, *Solid State Electronic Devices*, 2nd Ed., Prentice-Hall, 1980 (“Streetman”).

IPR2020-00289—Exhibit 2001—Exhibit 1 to Appendix C of Samsung Electronics Co., Ltd.’s Invalidity Contentions regarding Payne.

IPR2020-00289—Exhibit 2002—Exhibit 3 to Appendix C of Samsung Electronics Co., Ltd.’s Invalidity Contentions regarding Wieczorek.

IPR2020-00289—Exhibit 2011—Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, 2001 (“Razavi”).

IPR2020-00289—Exhibit 2012—Excerpts from Wolf, S., *Silicon Processing for the VLSI Era*, vol. 4—Deep-Submicron Process Technology (2002) (“Wolf vol. 4”).

IPR2020-00289—Exhibit 2013—Glew Dec.

IPR2020-00289—Patent Owner Pre Resp.

IPR2020-00289—Patent Owner Sur reply.

IPR2020-00289—Petition.

IPR2020-00290—Exhibit 1003—Declaration of Dr. Bruce Smith.

IPR2020-00290—Exhibit 1013—Tango, *Mega bit Memory Technology*.

IPR2020-00290—Patent Owner Preliminary Resp.

IPR2020-00290—Patent Owner Sur Reply.

IPR2020-00290—Petition.

IPR2020-00290—Petitioners Reply to Patent Owner Preliminary Response.

IPR2020-00291—Exhibit 1003—Declaration of Dr. Bruce Smith.

IPR2020-00291—Exhibit 1011—The Insulated Gate Bipolar Transistor: IGBT Theory and Design, Vinod Kumar Khanna, IEEE Press and Wiley-Interscience, 2003.

IPR2020-00291—Exhibit 1020—S. M. Sze, *Physics of Semiconductor Devices*, Wiley-Interscience, 2nd Ed., 1981 (“Sze 81”).

IPR2020-00291—Exhibit 1021—S. M. Sze, *Semiconductor Devices: Physics and Technology*, John Wiley & Sons, 2nd Ed., 2002 (“Sze ’02”).

IPR2020-00291—Exhibit 2001—Exhibit 2 to Appendix B of Samsung Electronics Co., Ltd.’s Invalidity Contentions (Invalidity Contention based on U.S. Patent Application Publication No. 2002/0195656 (“Hattori”).

IPR2020-00291—Exhibit 2013—Declaration of Dr. Alexander D. Glew.

IPR2020-00291—Patent Owner Preliminary Resp.

IPR2020-00291—Patent Owner Sur Reply.

IPR2020-00291—Petition.

IPR2020-00291—Petitioners Reply.

IPR2020-00292—Exhibit 1003—Declaration of Dr. Bruce Smith.

IPR2020-00292—Exhibit 2001—Excerpt from Exhibit 1 to Appendix B of Samsung Electronics Co., Ltd.’s Invalidity Contentions (Invalidity Contention based on “Insulated Gate Bipolar Transistor IGBT Theory and Design” by Vinod Kumar Khanna).

IPR2020-00292—Exhibit 2012—Excerpt from Exhibit A to Joint Claim Construction Chart Pursuant to Patent Rule 4-5, *Greenthread, LLC v. Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-CV-147-JRG, Dkt. 53-1 (Mar. 18, 2020).

IPR2020-00292—Patent Owner Preliminary Response.

* cited by examiner

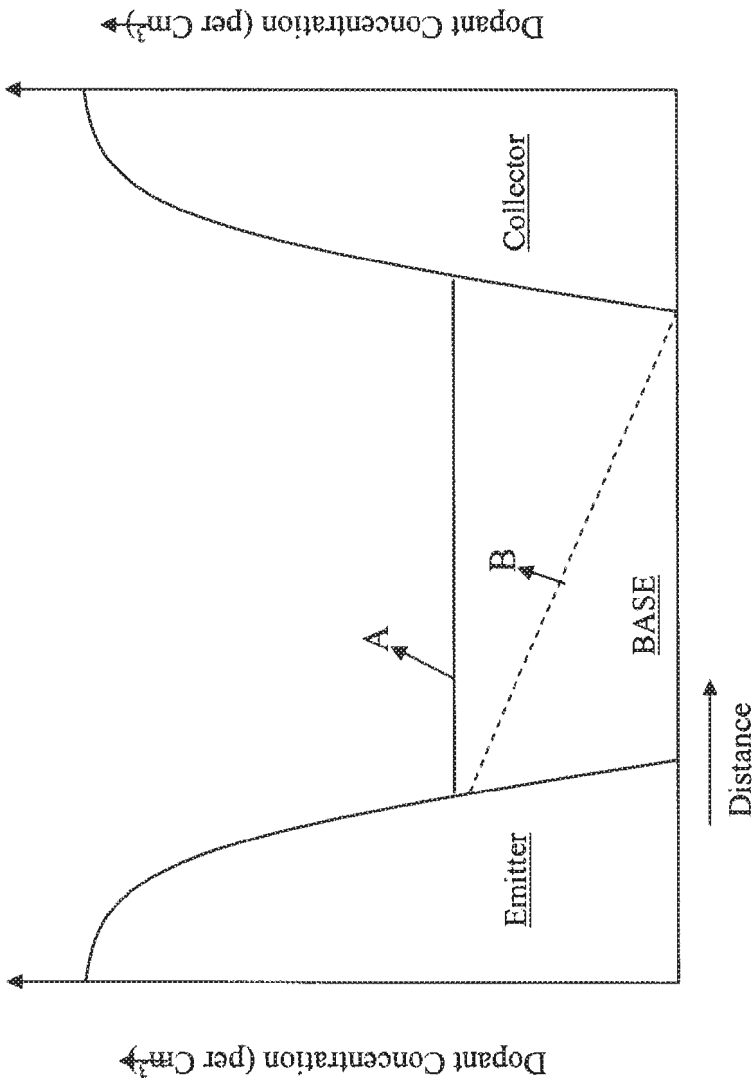


Figure 1 Prior Art

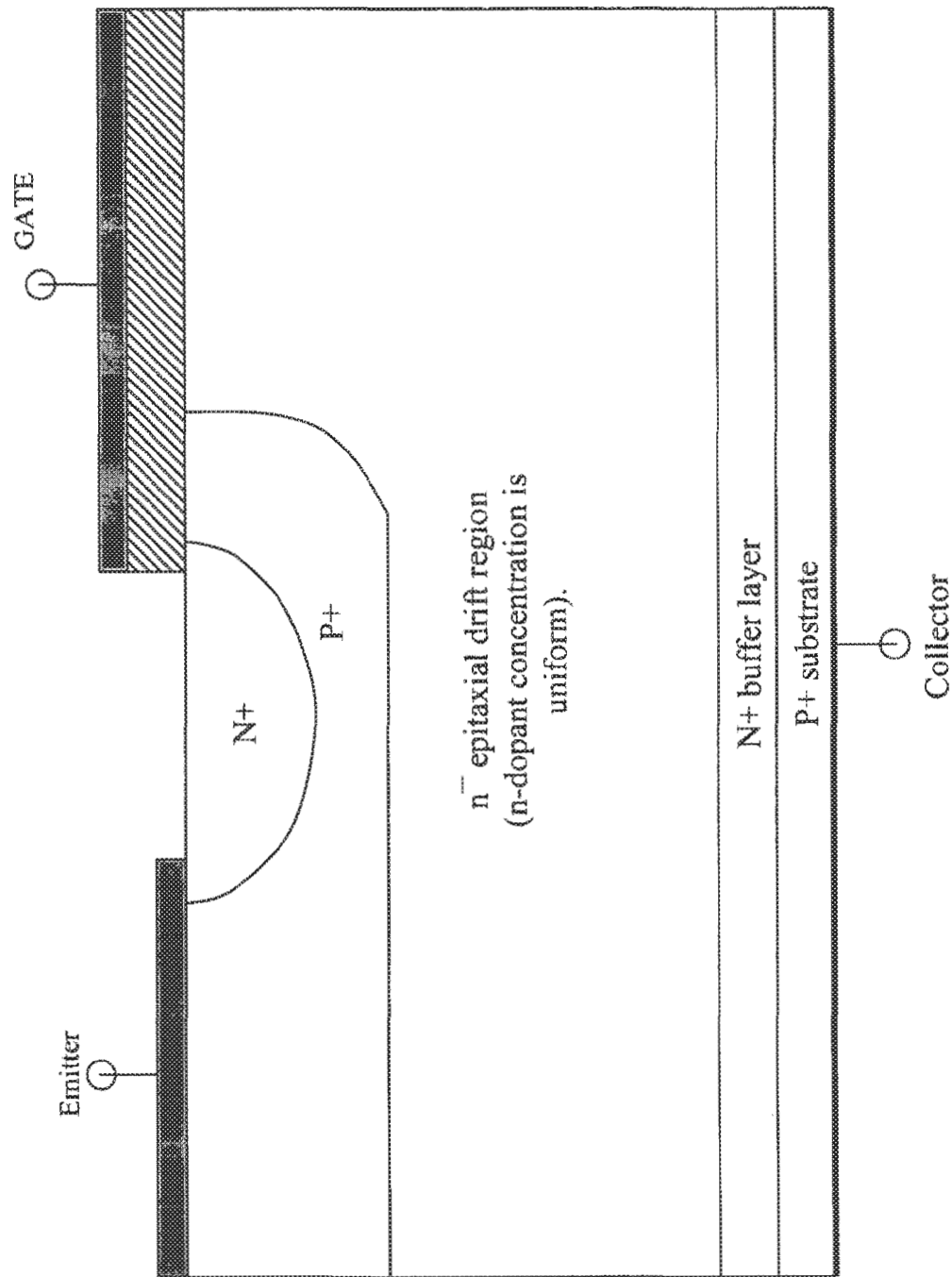


FIGURE 2 Prior art

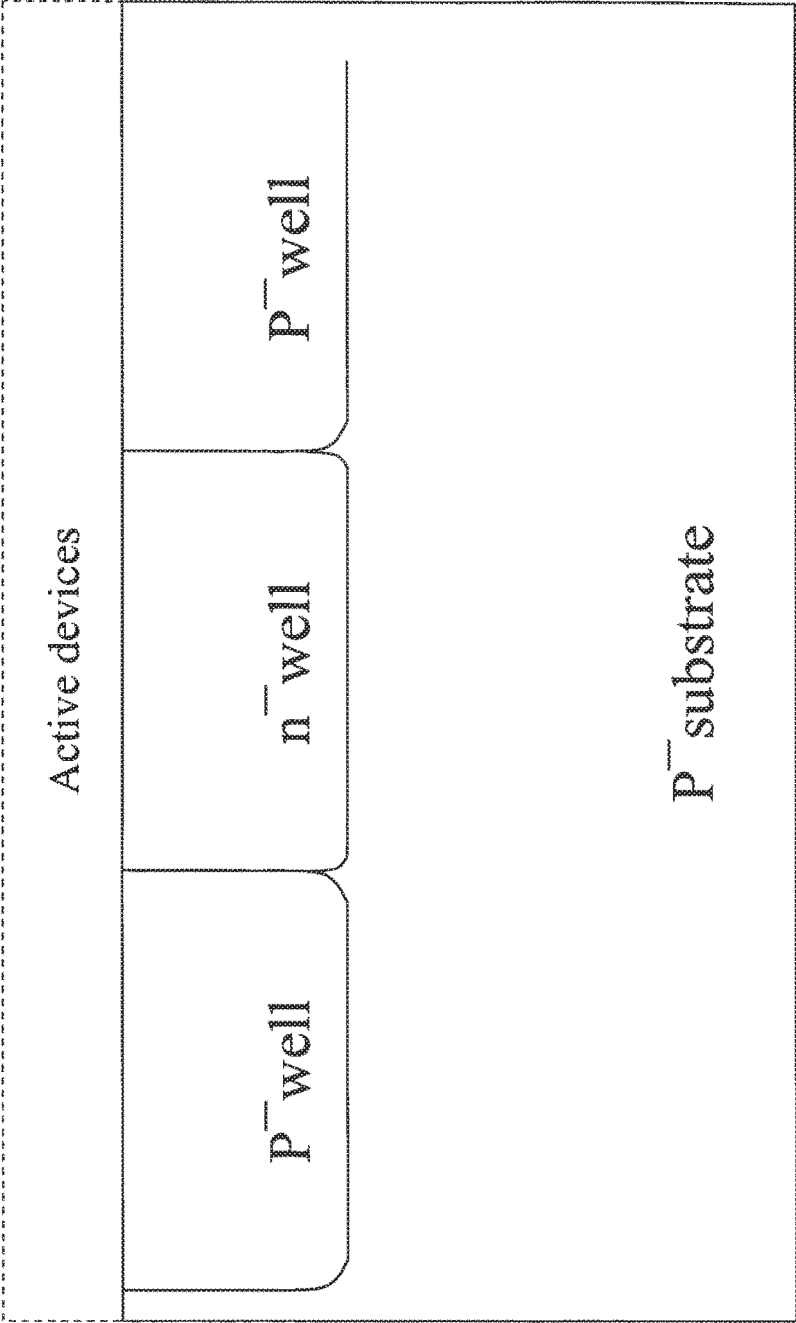


FIGURE 3A Prior art (Twin well CMOS) for a CMOS integrated circuit

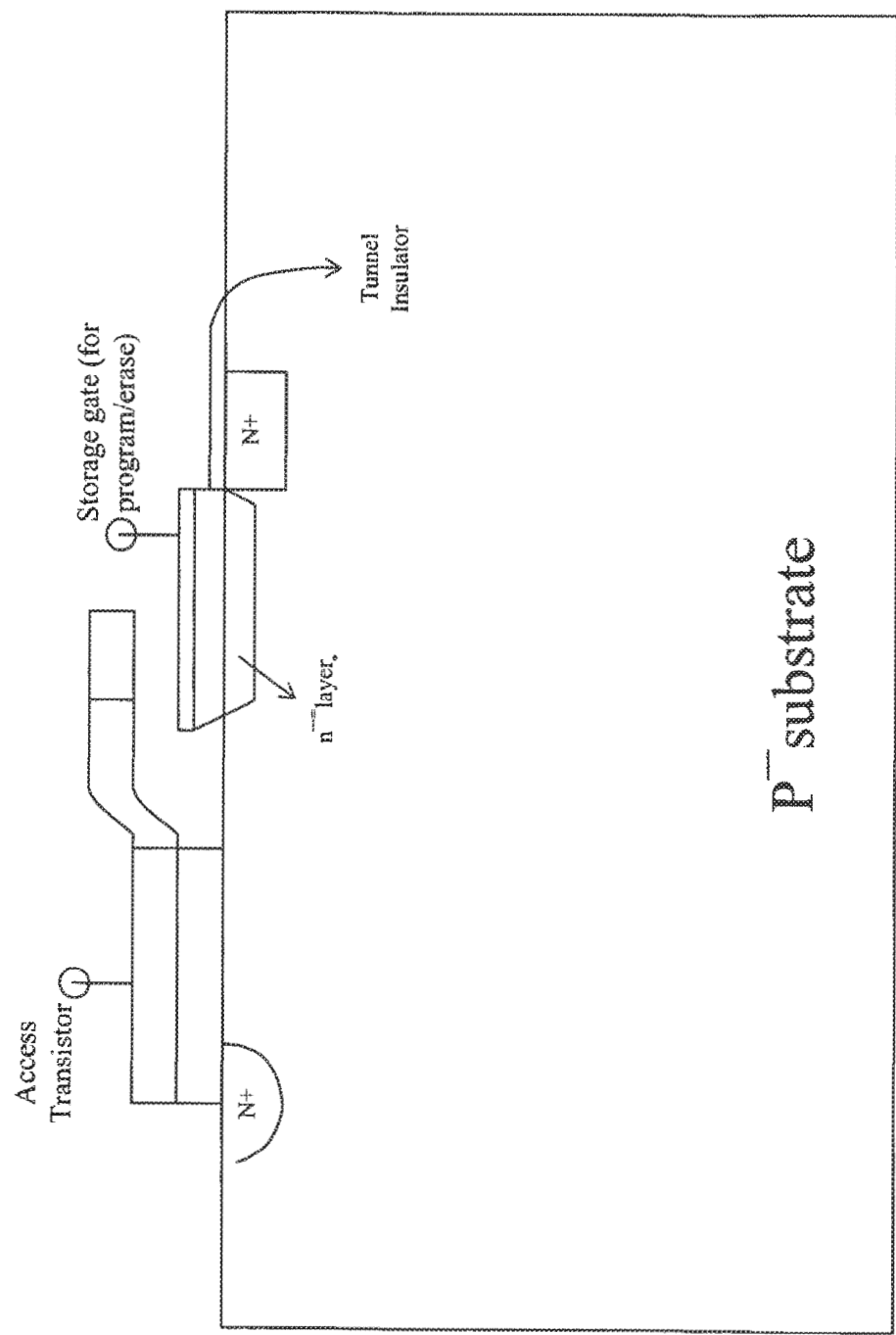


FIGURE 3B Prior art for a two-device EEPROM memory cell

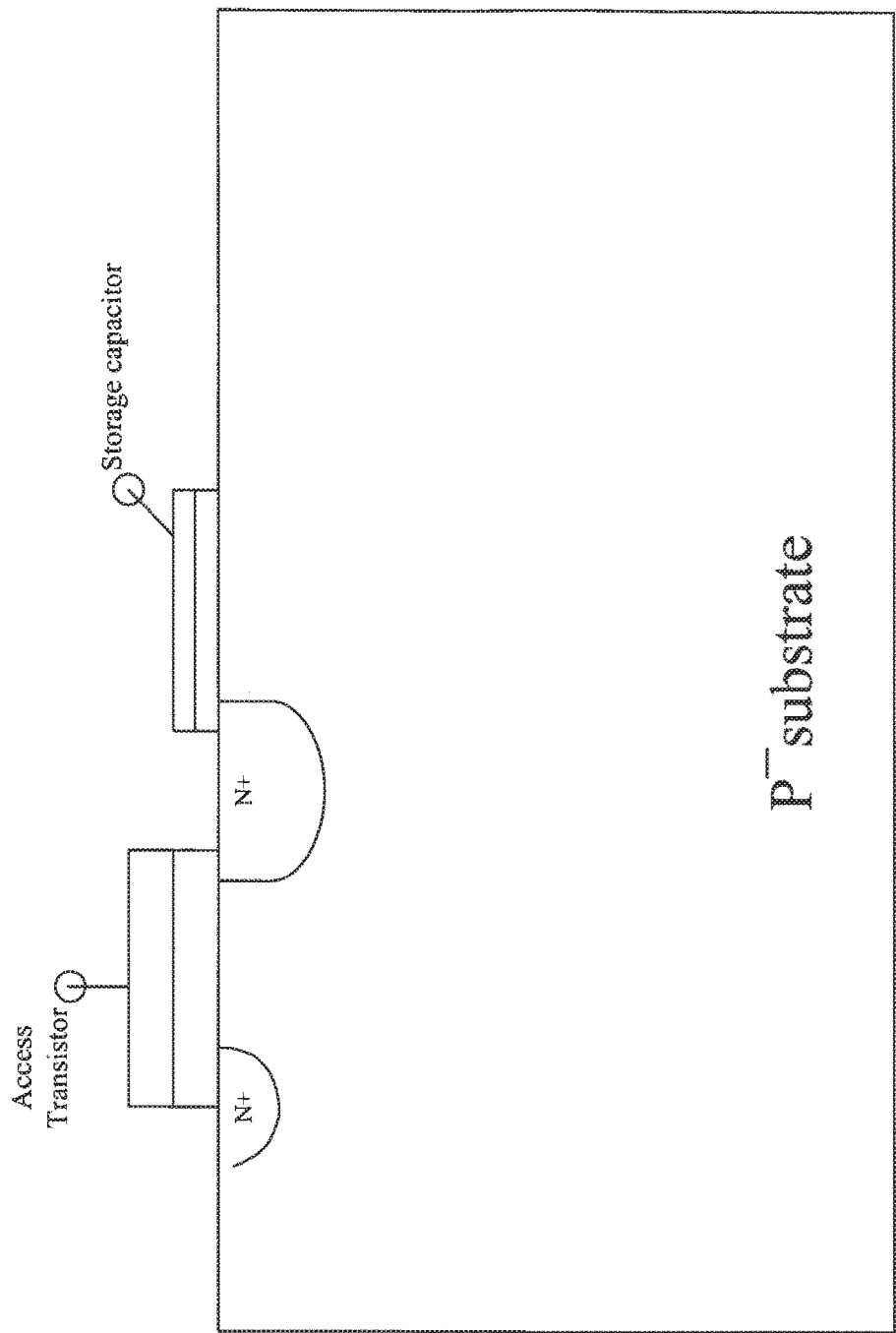


FIGURE 3C Prior art for a 1T-1C DRAM memory cell

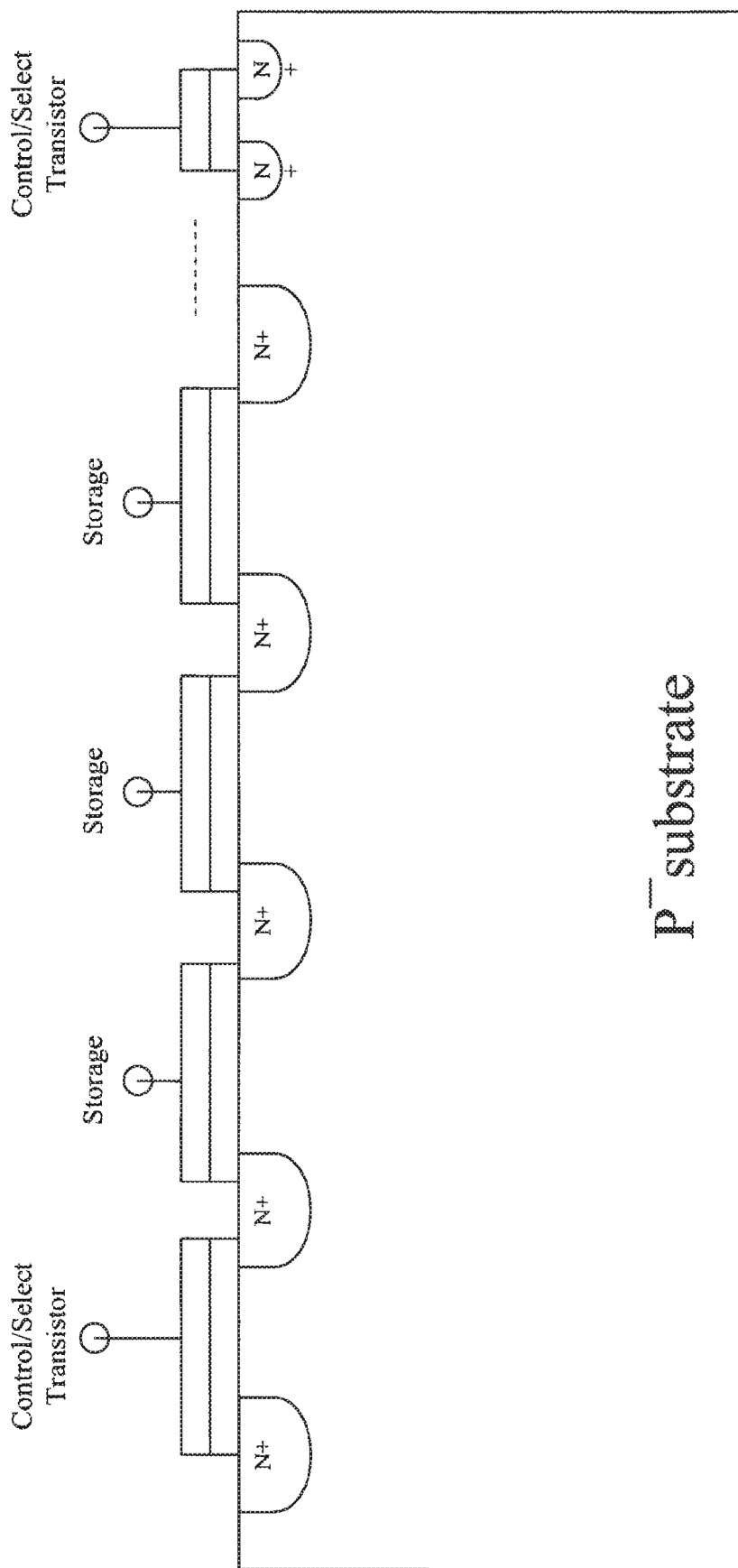


FIGURE 3D Prior art for a NAND flash memory cell

Note: Control/ Select transistors have a single insulator - traditional MOS transistor.

Storage nodes have a stacked gate structure, typically with a floating gate and control gate comprising the stack.

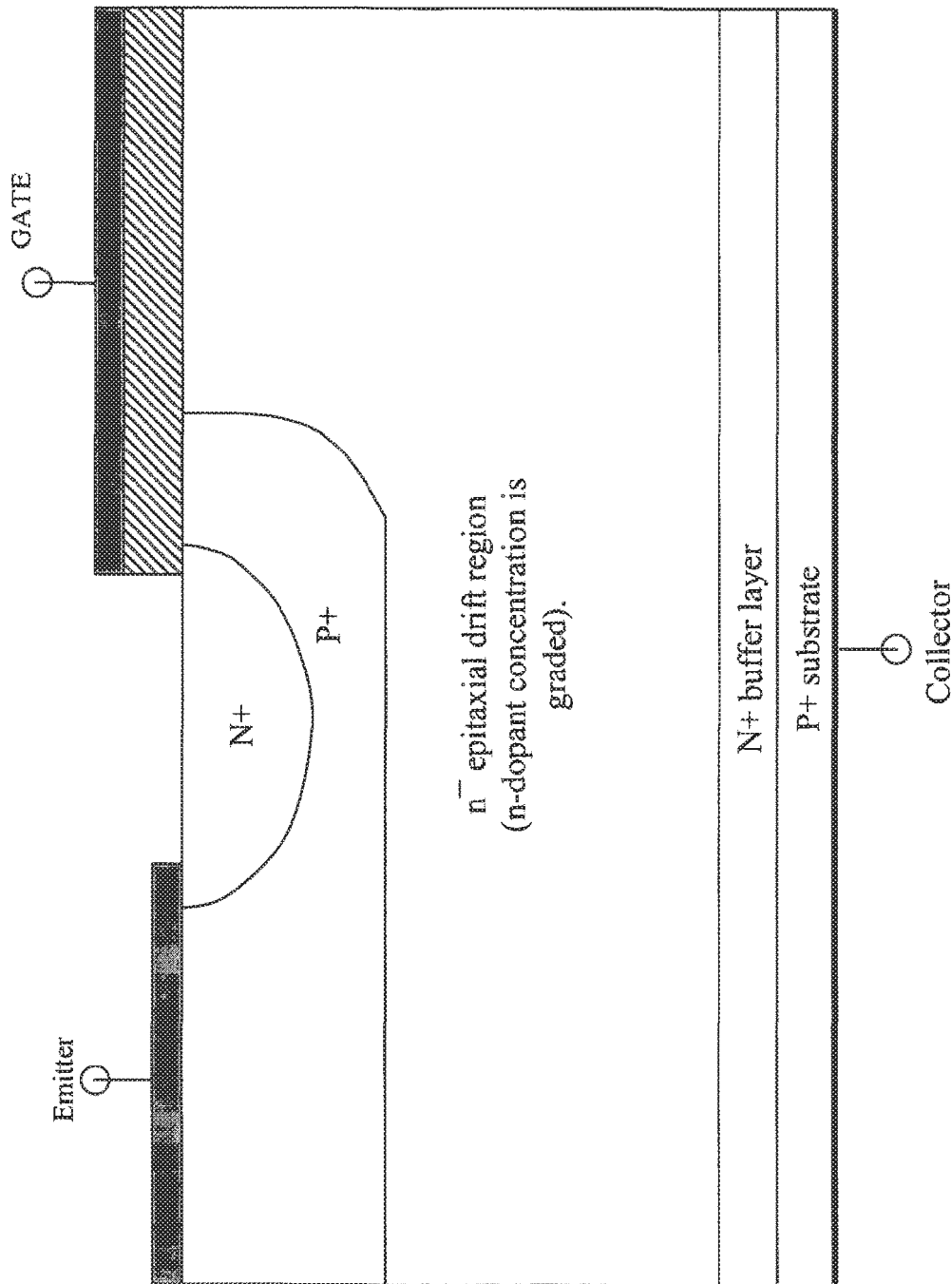


FIGURE 4 A dopant - concentration graded drift region in a IGBT

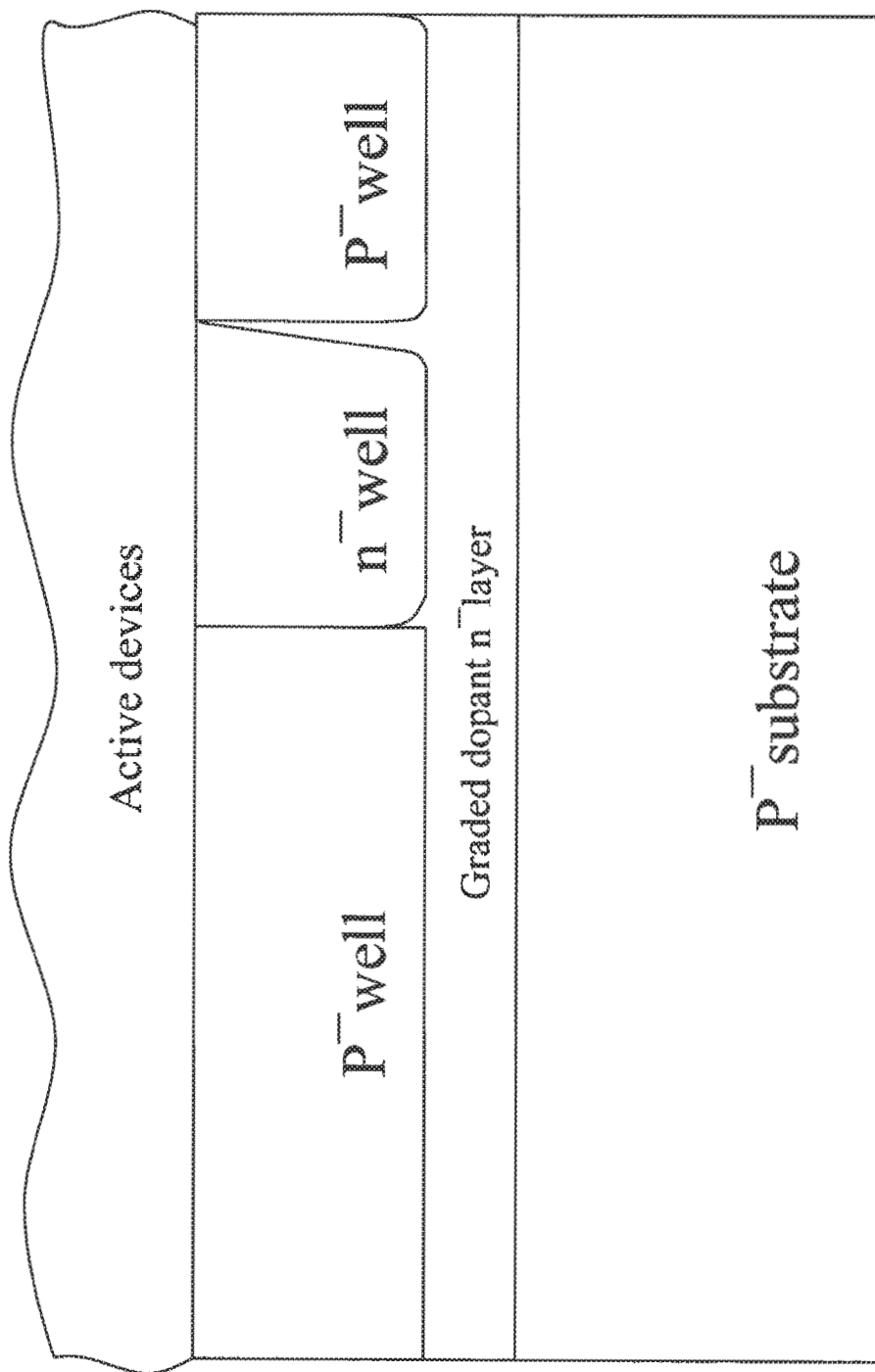


FIGURE 5A A CMOS Substrate for digital, mixed, signal, and sensors IC's

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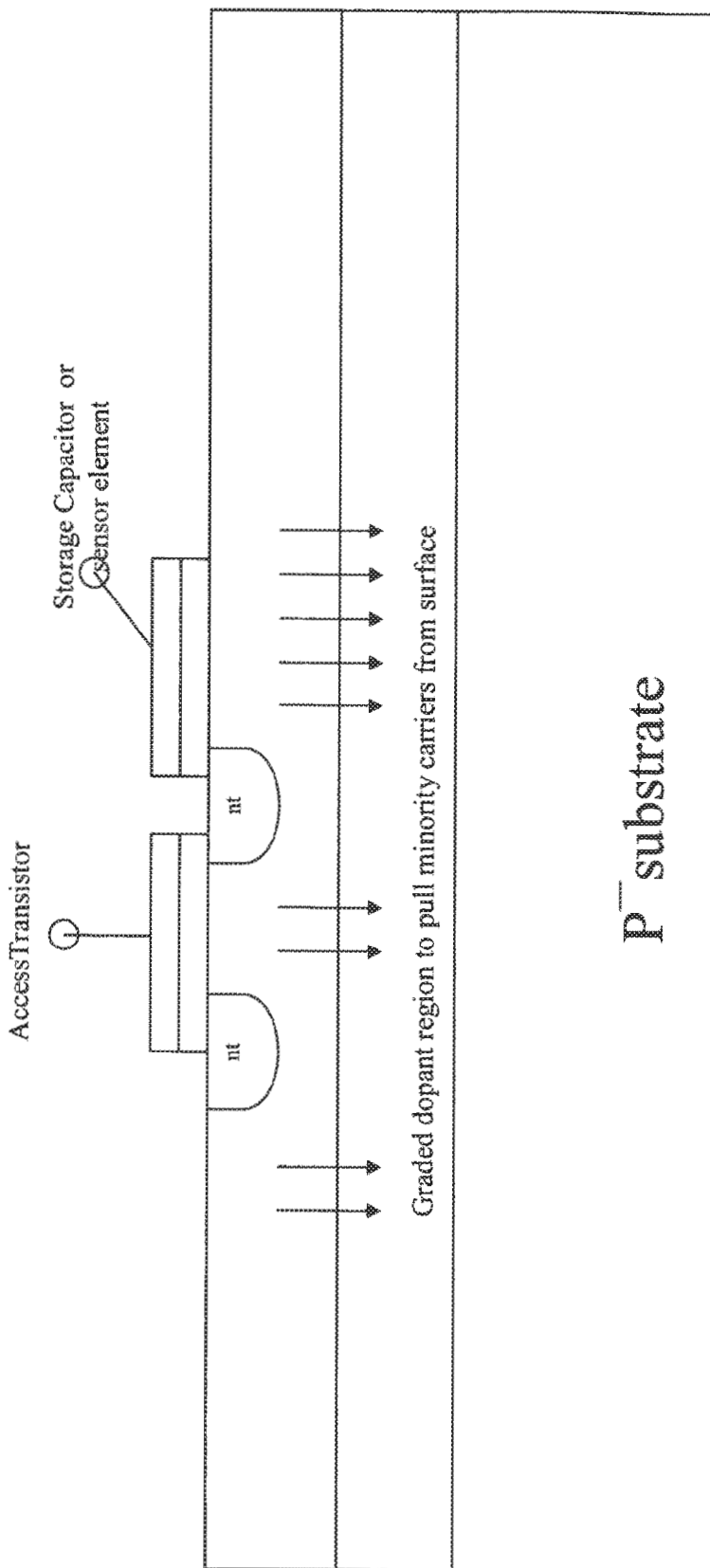


FIGURE 5B CMOS Substrate for a DRAM or image sensor, with one embodiment of the invention

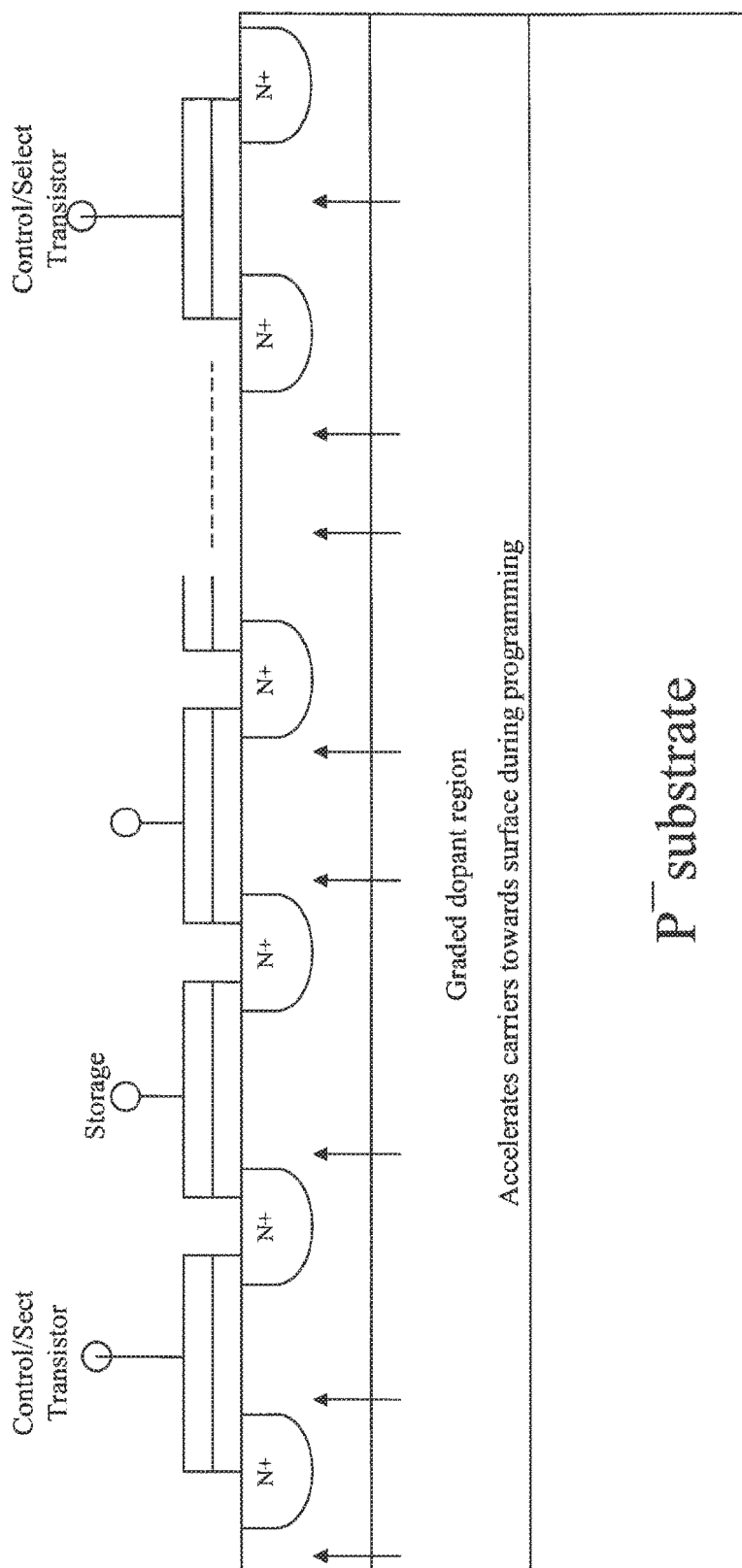


FIGURE 5C CMOS Substrate for a NAND flash device to improve programming times

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SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a Continuation of U.S. patent application Ser. No. 16/717,950, filed Dec. 17, 2019, which is a Continuation of U.S. patent application Ser. No. 15/590,282, filed May 9, 2017, which is a Continuation of U.S. patent application Ser. No. 14/931,636, filed Nov. 3, 2015, which is a Continuation of U.S. patent application Ser. No. 14/515,584, filed Oct. 16, 2014, which is a Continuation of U.S. patent application Ser. No. 13/854,319 filed Apr. 1, 2013, which is a Continuation of Ser. No. 11/622,496, filed Jan. 12, 2007, which is a Divisional of U.S. patent application Ser. No. 10/934,915, filed Sep. 3, 2004. The disclosures of which are incorporated herein by reference in their entirety.

TECHNICAL FIELD

This present invention relates to all semiconductor devices and systems. Particularly it applies to diffused diodes, avalanche diodes, Schottky devices, power MOS transistors, JFET's, RF bipolar transistors, IGBTs (Insulated Gate Bipolar Transistors), varactors, digital VLSI, mixed signal circuits and sensor devices including camera ICs employing CCD (Charge Coupled Device) as well as CMOS technologies.

BACKGROUND

Bipolar Junction Transistors (BJT) are classified as minority carrier devices because minority carriers are the principle device conduction mechanism. However, majority carriers also play a small but finite role in modulating the conductivity in BJTs. Consequently, both carriers (electrons and holes) play a role in the switching performance of BJTs. The maximum frequency of operation in BJTs is limited by the base transit time as well as the quick recombination of the majority carriers when the device is switched off (prior to beginning the next cycle). The dominant carrier mechanism in BJTs is carrier diffusion. The carrier drift current component is fairly small, especially in uniformly doped base BJTs. Efforts have been made in graded base transistors to create an aiding drift field to enhance the diffusing minority carrier's speed from emitter to collector. However, most semiconductor devices, including various power MOSFETs (traditional, DMOS, lateral, vertical and a host of other configurations), IGBT's (Insulated Gated Base Transistors), still use a uniformly doped 'drift epitaxial' region in the base. FIG. 1 shows the relative doping concentration versus distance in a BJT. FIG. 2 shows the uniformly doped epi region in an IGBT. In contrast to BJTs, MOS devices are majority carrier devices for conduction. The conduction is channel dominated. The channel can be a surface in one plane in planar devices. The surface can also be on the sidewalls in a vertical device. Other device architectures to combine planar and vertical conduction are also possible. The maximum frequency of operation is dictated primarily by source-drain separation distance. Most MOS devices use a uniformly doped substrate (or a well region). When a MOSFET is optimally integrated with a BJT in a monolithic fashion, an IGBT results. The IGBT inherits the advantages of both MOSFET and BJT. It also brings new challenges because the required characteristics (electron transit and

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hole recombination as fast as possible in n-channel IGBT) necessitate different dopant gradients either in the same layer at different positions, or at the interfaces of similar or dissimilar layers.

Retrograde wells have been attempted, with little success, to help improve soft error immunity in SRAMs and visual quality in imaging circuits. FIG. 3A shows a typical CMOS VLSI device employing a twin well substrate, on which active devices are subsequently fabricated. FIGS. 3B, 3C, and 3D illustrate device cross sections, as practiced today. Retrograde and halo wells have also been attempted to improve refresh time in DRAMs (dynamic random-access memories), as well as, reducing dark current (background noise) and enhance RGB (Red, Green, Blue) color resolution in digital camera ICs. Most of these techniques either divert the minority carriers away from the active regions of critical charge storage nodes at the surface, or, increase minority carrier density locally as the particular application requires.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. 1 illustrates the relative doping profiles of emitter, base and collector for the two most popular bipolar junction transistors: namely, uniform base ("A") and graded base ("B");

FIG. 2 illustrates the cross section of a commercial IGBT with a uniform epitaxial drift region (base);

FIGS. 3A, 3B, 3C, and 3D illustrate cross sections of commonly used prior art CMOS silicon substrates; FIG. 3A showing a typical prior art IC with two wells (one n⁺ well in which p-channel transistors are subsequently fabricated and one p⁺ well in which n-channel transistors are subsequently fabricated); FIG. 3B showing a prior art EEPROM (Electrically Erasable Programmable Read-Only Memory) memory cell having a tunnel insulator; FIG. 3C showing a prior art DRAM memory cell; and FIG. 3D showing a prior art NAND flash memory cell;

FIG. 4 illustrates the cross section of an IGBT, using one embodiment of the invention described here, where the dopant is optimally graded in the epitaxial drift region; and

FIGS. 5A, 5B, and 5C illustrate the cross sections of a CMOS silicon substrate with two wells and an underlying layer using embodiments of the invention to improve performance in each application—VLSI logic, DRAM/image IC, nonvolatile memory IC.

DETAILED DESCRIPTION

The relative doping concentrations of emitter and collector regions varies from 10^{18} to $10^{20}/\text{cm}^3$, whereas the base region is 10^{14} to $10^{16}/\text{cm}^3$ depending on the desired characteristics of the BJT. In graded base p-n-p transistors, the donor dopant concentration may be 10 to 100x at the emitter-base junction, relative to the base-collector junction ($1\times$). The gradient can be linear, quasi linear, exponential or complimentary error function. The relative slope of the donor concentration throughout the base creates a suitable aiding drift electric field, to help the holes (p-n-p transistor) transverse from emitter to collector. Since the aiding drift electric field helps hole conduction, the current gain at a given frequency is enhanced, relative to a uniformly-doped (base) BJT. The improvement in the current gain of the

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frequency at unity gain, f_T) can be as large as $2\times-5\times$. Similar performance improvements are also applicable to n-p-n transistors.

As illustrated in FIG. 4, in one embodiment according to the invention, a donor gradient is established from the emitter-drift epitaxial base region junction of the punch-through IGBT, to the drift epitaxial base region— n^+ buffer layer boundary (electrons in this case are accelerated in their transit from emitter to collector). The “average” base resistance is optimized so that conductivity modulation and lifetime (for minority carriers) in the base region are not compromised. By sweeping the carriers towards the n^+ buffer region a number of advantages are obtained. First, the frequency of operation (combination of t_{on} and t_{off} as is known in the IGBT commercial nomenclature) can be enhanced. Second, and maybe more importantly, during t_{off} , holes can be recombined much quicker at the n^+ buffer layer, compared to the uniformly doped n^- epitaxial drift region by establishing a different dopant gradient near the n^+ buffer layer. It should be noted that the drift region can also be a non-epitaxial silicon substrate. Although epitaxy enhances lifetime, it is not mandatory. Different layers of dopant regions can be transferred through wafer to wafer bonding (or other similar transfer mechanisms) for eventual device fabrication. The “reverse recovery time” for an IGBT is significantly improved due to the optimized graded dopant in the so called “drift region” as well as at the interfaces of the drift region. Graded dopants can also be implemented in the n^+ buffer layer as well as other regions adjacent to the respective layers. Two important performance enhancements are the result of dopant gradients. For example, in an n-channel IGBT, electrons can be swept from source to drain rapidly, while at the same time holes can be recombined closer to the n^+ buffer layer. This can improve t_{on} and t_{off} in the same device.

As illustrated in FIGS. 5A, 5B, and 5C, donor gradient is also of benefit to very large scale integrated circuits (VLSI)—VLSI logic, DRAM, nonvolatile memory like NAND flash. Spurious minority carriers can be generated by clock switching in digital VLSI logic and memory ICs. These unwanted carriers can discharge dynamically-held “actively held high” nodes. In most cases, statically-held nodes (with V_{cc}) cannot be affected. Degradation of refresh time in DRAMs is one of the results, because the capacitor holds charge dynamically. Similarly, degradation of CMOS digital images in digital imaging ICs is another result of the havoc caused by minority carriers. Pixel and color resolution can be significantly enhanced in imaging ICs with the embodiments described herein. Creating “subterranean” recombination centers underneath the wells (gold doping, platinum doping) as is done in some high-voltage diodes is not practical for VLSI circuits. Hence, a novel technique is described herein which creates a drift field to sweep these unwanted minority carriers from the active circuitry at the surface into the substrate in a monolithic die as quickly as possible. In a preferred embodiment, the subterranean n^- layer has a graded donor concentration to sweep the minority carriers deep into the substrate. One or more of such layers can also be implemented through wafer to wafer bonding or similar “transfer” mechanisms. This n^- layer can be a deeply-implanted layer. It can also be an epitaxial layer. As desired, the n^- well and p^- wells can also be graded or retrograded in dopants to sweep those carriers away from the surface as well. The graded dopant can also be implemented in surface channel MOS devices to accelerate majority carriers towards the drain. To decrease programming time in nonvolatile memory devices, carriers should be accelerated

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towards the surface when programming of memory cells is executed. The graded dopant can also be used to fabricate superior Junction Field-Effect transistors where the “channel pinch-off” is controlled by a graded channel instead of a uniformly doped channel (as practiced in the prior art).

One of ordinary skill and familiarity in the art will recognize that the concepts taught herein can be customized and tailored to a particular application in many advantageous ways. For instance, minority carriers can be channeled to the surface to aid programming in nonvolatile memory devices (NOR, NAND, multivalued-cell). Moreover, single-well, and triple-well CMOS fabrication techniques can also be optimized to incorporate these embodiments individually and collectively. Any modifications of such embodiments (described here) fall within the spirit and scope of the invention. Hence, they fall within the scope of the claims described below.

Although the invention has been described with reference to specific embodiments, these descriptions are not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as alternative embodiments of the invention will become apparent to persons skilled in the art upon reference to the description of the invention. It should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

It is therefore, contemplated that the claims will cover any such modifications or embodiments that fall within the true scope of the invention.

What is claimed is:

1. A VLSI semiconductor device, comprising:
 - a substrate of a first doping type at a first doping level having a surface;
 - a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
 - a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
 - transistors formed in at least one of the first active region or second active region;
 - at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
 - at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.
2. The VLSI semiconductor device of claim 1, wherein the substrate is a p-type substrate.
3. The VLSI semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

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4. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain digital logic formed by one of either p-channel and n-channel devices.

5. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.

6. The VLSI semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.

7. The VLSI semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.

8. The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.

9. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.

10. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region are both p-type and n-type.

11. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the second active region are both p-type and n-type.

12. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant region in the well region are both p-type and n-type.

13. The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.

14. The VLSI semiconductor device of claim 1, wherein the device is a dynamic random access memory (DRAM).

15. The VLSI semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.

16. The VLSI semiconductor device of claim 1, wherein the device is a flash memory.

17. The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors.

18. The VLSI semiconductor device of claim 1, wherein the device is central processing unit.

19. The VLSI semiconductor device of claim 1, wherein the device is an image sensor.

20. The VLSI semiconductor device of claim 1, wherein each of the first and second active regions are in the lateral or vertical direction.

21. A VLSI semiconductor device, comprising:

a substrate of a first doping type at a first doping level having a surface;

a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof; transistors formed in at least one of the first active region or second active region;

at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and

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at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.

22. The VLSI semiconductor device of claim 21, wherein the substrate is an n-type substrate.

23. The VLSI semiconductor device of claim 21, wherein the substrate is a p-type substrate.

24. The VLSI semiconductor device of claim 21, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

25. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.

26. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.

27. The VLSI semiconductor device of claim 21, wherein the first active region and second active region are each separated by at least one isolation region.

28. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.

29. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region are both p-type and n-type.

30. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the second active region are both p-type and n-type.

31. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant region in the well region are both p-type and n-type.

32. The VLSI semiconductor device of claim 21, wherein the graded dopant is fabricated with an ion implantation process.

33. The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.

34. The VLSI semiconductor device of claim 21, wherein the device is a flash memory.

35. The VLSI semiconductor device of claim 21, wherein the device is a logic device with capacitors in at least some of the first or second active regions.

36. The VLSI semiconductor device of claim 21, wherein the device is central processing unit.

37. The VLSI semiconductor device of claim 21, wherein the device is an image sensor.

38. The VLSI semiconductor device of claim 21, wherein each of the first and second active regions are in the lateral or vertical direction.

39. A semiconductor device, comprising:

a substrate of a first doping type at a first doping level; a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

transistors formed in at least one of the first active region or second active region; and

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at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.

40. The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.

41. A semiconductor device, comprising:

a substrate of a first doping type at a first doping level;
a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

transistors formed in at least one of the first active region or second active region; and

at least a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.

42. A semiconductor device, comprising:

a substrate of a first doping type at a first doping level;
a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

transistors formed in at least one of the first active region or second active region; and

at least a portion of at least one of the first and second active regions having at least one graded donor dopant

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concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.

43. A semiconductor device, comprising:

a substrate of a first doping type at a first doping level;
a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

transistors formed in at least one of the first active region or second active region; and

at least a portion of at least one of the first and second active regions having at least one graded acceptor dopant concentration and one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.

44. A CMOS Semiconductor device comprising:

a surface layer;

a substrate;

an active region including a source and a drain, disposed on one surface of the surface layer;

a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate, the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and

at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.

* * * * *

EXHIBIT 6



US011316014B2

(12) **United States Patent**
Rao

(10) **Patent No.:** **US 11,316,014 B2**
(45) **Date of Patent:** ***Apr. 26, 2022**

(54) **SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS**

(71) Applicant: **GREENTHREAD, LLC**, Dallas, TX (US)

(72) Inventor: **G. R. Mohan Rao**, Allen, TX (US)

(73) Assignee: **GREENTHREAD, LLC**, Dallas, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **17/371,839**

(22) Filed: **Jul. 9, 2021**

(65) **Prior Publication Data**

US 2021/0359086 A1 Nov. 18, 2021

Related U.S. Application Data

(60) Continuation of application No. 16/947,294, filed on Jul. 27, 2020, now Pat. No. 11,121,222, which is a (Continued)

(51) **Int. Cl.**

H01L 29/10 (2006.01)

H01L 27/11524 (2017.01)

(Continued)

(52) **U.S. Cl.**

CPC **H01L 29/1095** (2013.01); **H01L 27/11521** (2013.01); **H01L 27/11524** (2013.01);

(Continued)

(58) **Field of Classification Search**

CPC H01L 29/1095

(Continued)

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,160,985 A 7/1979 Kamins et al.

4,684,971 A 8/1987 Payne

(Continued)

FOREIGN PATENT DOCUMENTS

JP s6482563 A 3/1989

JP 2003051551 A 2/2003

(Continued)

OTHER PUBLICATIONS

IPR2020-00288—Exhibit 1029—Claim Construction District Court Apr. 20, 2020.

(Continued)

Primary Examiner — Ajay Arora

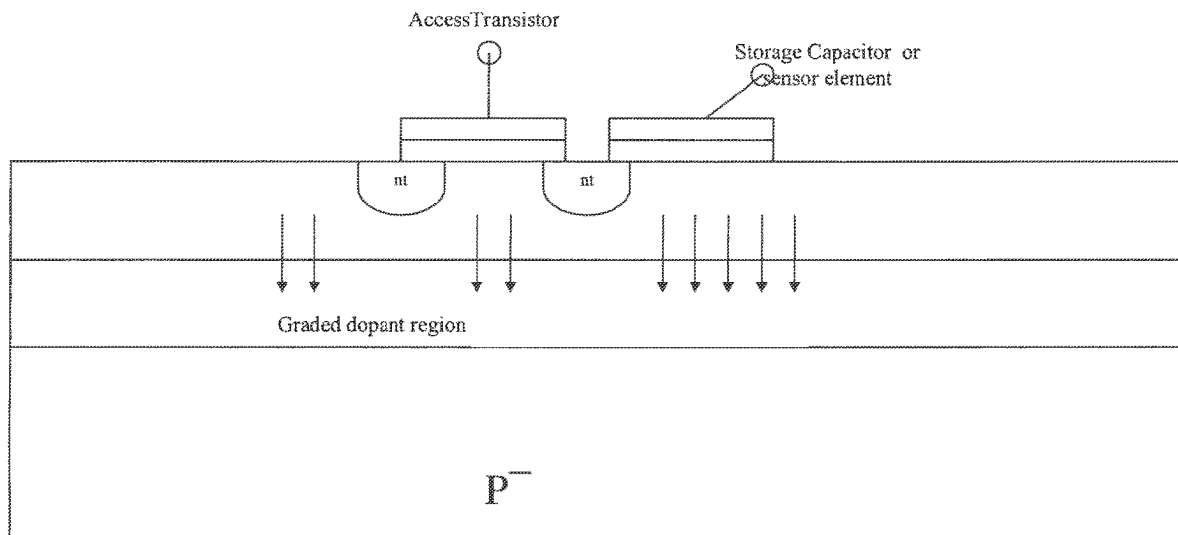
(74) *Attorney, Agent, or Firm* — Gregory M. Howison

(57)

ABSTRACT

Most semiconductor devices manufactured today, have uniform dopant concentration, either in the lateral or vertical device active (and isolation) regions. By grading the dopant concentration, the performance in various semiconductor devices can be significantly improved. Performance improvements can be obtained in application specific areas like increase in frequency of operation for digital logic, various power MOSFET and IGBT ICs, improvement in refresh time for DRAMs, decrease in programming time for nonvolatile memory, better visual quality including pixel resolution and color sensitivity for imaging ICs, better sensitivity for varactors in tunable filters, higher drive capabilities for iFETs, and a host of other applications.

30 Claims, 10 Drawing Sheets



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Related U.S. Application Data

continuation of application No. 16/717,950, filed on Dec. 17, 2019, now Pat. No. 10,734,481, which is a continuation of application No. 15/590,282, filed on May 9, 2017, now Pat. No. 10,510,842, which is a continuation of application No. 14/931,636, filed on Nov. 3, 2015, now Pat. No. 9,647,070, which is a continuation of application No. 14/515,584, filed on Oct. 16, 2014, now Pat. No. 9,190,502, which is a continuation of application No. 13/854,319, filed on Apr. 1, 2013, now abandoned, which is a continuation of application No. 11/622,496, filed on Jan. 12, 2007, now Pat. No. 8,421,195, which is a division of application No. 10/934,915, filed on Sep. 3, 2004, now abandoned.

(51) Int. Cl.

H01L 27/146 (2006.01)
H01L 27/11521 (2017.01)
H01L 29/739 (2006.01)
H01L 29/36 (2006.01)
H01L 27/02 (2006.01)
H01L 27/108 (2006.01)

(52) U.S. Cl.

CPC **H01L 27/14643** (2013.01); **H01L 29/36** (2013.01); **H01L 29/7395** (2013.01); **H01L 27/0214** (2013.01); **H01L 27/10844** (2013.01)

(58) Field of Classification Search

USPC 257/25
 See application file for complete search history.

(56)

References Cited

U.S. PATENT DOCUMENTS

4,688,063	A	8/1987	Lu et al.	
4,907,058	A	3/1990	Sakai	
4,994,887	A	2/1991	Hutter et al.	
5,835,402	A	11/1998	Rao et al.	
6,025,237	A	2/2000	Choi	
6,384,431	B1	5/2002	Takahashi et al.	
6,465,862	B1	10/2002	Harris	
2001/0028097	A1	10/2001	Matsuoka et al.	
2002/0195656	A1	12/2002	Hattori	
2003/0183856	A1	10/2003	Wieczorek et al.	
2007/0045682	A1*	3/2007	Hong	H01L 27/14689 257/292
2008/0142899	A1	6/2008	Morris et al.	
2014/0034997	A1*	2/2014	Rahimo	H01L 29/861 257/139
2017/0243876	A1	8/2017	Rao	

FOREIGN PATENT DOCUMENTS

JP	2003218356	A	7/2003
WO	2004049453	A1	6/2004

OTHER PUBLICATIONS

IPR2020-00288—Exhibit 2007—Minutes for Markman Hearing Held via Video Conference Before U.S. District Judge Rodney Gilstrap, *Greenthread, LLC v. Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-CV-147-JRG.
 IPR2020-00288—Petitioner Reply.
 IPR2020-00289-00289 Petitioner Reply.
 IPR2020-00292—Petition for IPR.
 IPR2020-00292—Exhibit 2002—Excerpt from Exhibit 4 to Appendix B of Samsung Electronics Co., Ltd.’s Invalidity Contentions (Invalidity Contention based on U.S. Pat. No. 6,384,431 to Takahashi.

IPR2020-00288—Ex. 1020—Michael Nastasi and James W. Mayer, *Ion Implantation and Synthesis of Materials* (2006). 4 pages.

IPR2020-00288—Exhibit 2001—IPR2020-00288—Excerpt from Exhibit 1 to Appendix A of Samsung Electronics Co., Ltd.’s Invalidity Contentions regarding Morris.

IPR2020-00288—Exhibit 2002—Excerpt from Exhibit 2 to Appendix A of Samsung Electronics Co., Ltd.’s Invalidity Contentions regarding Miyamoto.

IPR2020-00288—Exhibit 2009—Complaint for Patent Infringement, *Greenthread, LLC v. Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-CV-147-JRG.

IPR2020-00288—Exhibit 2011—Exhibit A to Revised Joint Claim Construction Chart Pursuant to Patent Rule 4-5, *Greenthread, LLC v. Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-CV-147-JRG.

IPR2020-00288—Exhibit 2012—Samsungs Responsive Claim Construction Brief—District Court.

IPR2020-00288—Exhibit 2013—Glew Dec.

IPR2020-00288—Exhibit 2014—Excerpt from Exhibit 10 to Appendix A of Samsung Electronics Co., Ltd.’s Invalidity Contentions.

IPR2020-00288—Patent Owner Preliminary Response.

IPR2020-00288—Patent Owner Sur Reply.

IPR2020-00288—Petition.

IPR2020-00289—Exhibit 1 to Appendix C of Samsung Electronics Co., Ltd.’s Invalidity Contentions regarding Payne.

IPR2020-00289—Exhibit 1003—Smith Dec.

IPR2020-00289—Exhibit 1010—S. M. Sze et al., *Semiconductor Devices: Physics and Technology*, John Wiley & Sons, 2nd Ed., 2002 (“Sze ’02”).

IPR2020-00289—Exhibit 1012—Ben G. Streetman, *Solid State Electronic Devices*, 2nd Ed., Prentice-Hall, 1980 (“Streetman”).

IPR2020-00289—Exhibit 2001—Exhibit 1 to Appendix C of Samsung Electronics Co., Ltd.’s Invalidity Contentions regarding Payne.

IPR2020-00289—Exhibit 2002—Exhibit 3 to Appendix C of Samsung Electronics Co., Ltd.’s Invalidity Contentions regarding Wieczorek.

IPR2020-00289—Exhibit 2011—Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, 2001 (“Razavi”).

IPR2020-00289—Exhibit 2012—Excerpts from Wolf, S., *Silicon Processing for the VLSI Era*, vol. 4—Deep-Submicron Process Technology (2002) (“Wolf vol. 4”).

IPR2020-00289—Exhibit 2013—Glew Dec.

IPR2020-00289—Patent Owner Pre Resp.

IPR2020-00289—Patent Owner Sur reply.

IPR2020-00289—Petition.

IPR2020-00290—Exhibit 1003—Declaration of Dr. Bruce Smith.

IPR2020-00290—Exhibit 1013—Tango, *Mega bit Memory Technology*.

IPR2020-00290—Patent Owner Preliminary Resp.

IPR2020-00290—Patent Owner Sur Reply.

IPR2020-00290—Petition.

IPR2020-00290—Petitioners Reply to Patent Owner Preliminary Response.

IPR2020-00291—Exhibit 1003—Declaration of Dr. Bruce Smith.

IPR2020-00291—Exhibit 1011—The Insulated Gate Bipolar Transistor: IGBT Theory and Design, Vinod Kumar Khanna, IEEE Press and Wiley-Interscience, 2003.

IPR2020-00291—Exhibit 1020—S. M. Sze, *Physics of Semiconductor Devices*, Wiley-Interscience, 2nd Ed., 1981 (“Sze ’81”).

IPR2020-00291—Exhibit 1021—S. M. Sze, *Semiconductor Devices: Physics and Technology*, John Wiley & Sons, 2nd Ed., 2002 (“Sze ’02”).

IPR2020-00291—Exhibit 2001—Exhibit 2 to Appendix B of Samsung Electronics Co., LTD’S Invalidity Contentions (Invalidity Contention based on U.S. Patent Application Publication No. 2002/0195656 (“Hattori”).

IPR2020-00291—Exhibit 2013—Declaration of Dr. Alexander D. Glew.

IPR2020-00291—Patent Owner Preliminary Resp.

IPR2020-00291—Patent Owner Sur Reply.

IPR2020-00291—Petition.

IPR2020-00291—Petitioners Reply.

IPR2020-00292—Exhibit 1003—Declaration of Dr. Bruce Smith.

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(56)

References Cited

OTHER PUBLICATIONS

IPR2020-00292—Exhibit 2001—Excerpt from Exhibit 1 to Appendix B of Samsung Electronics Co., Ltd.’s Invalidity Contentions (Invalidity Contention based on “Insulated Gate Bipolar Transistor IGBT Theory and Design” by Vinod Kumar Khanna.

IPR2020-00292—Exhibit 2012—Excerpt from Exhibit A to Joint Claim Construction Chart Pursuant to Patent Rule 4-5, *Greenthread, LLC v. Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-CV-147-JRG, (Mar. 18, 2020).

IPR2020-00292—Patent Owner Preliminary Response.

* cited by examiner

U.S. Patent

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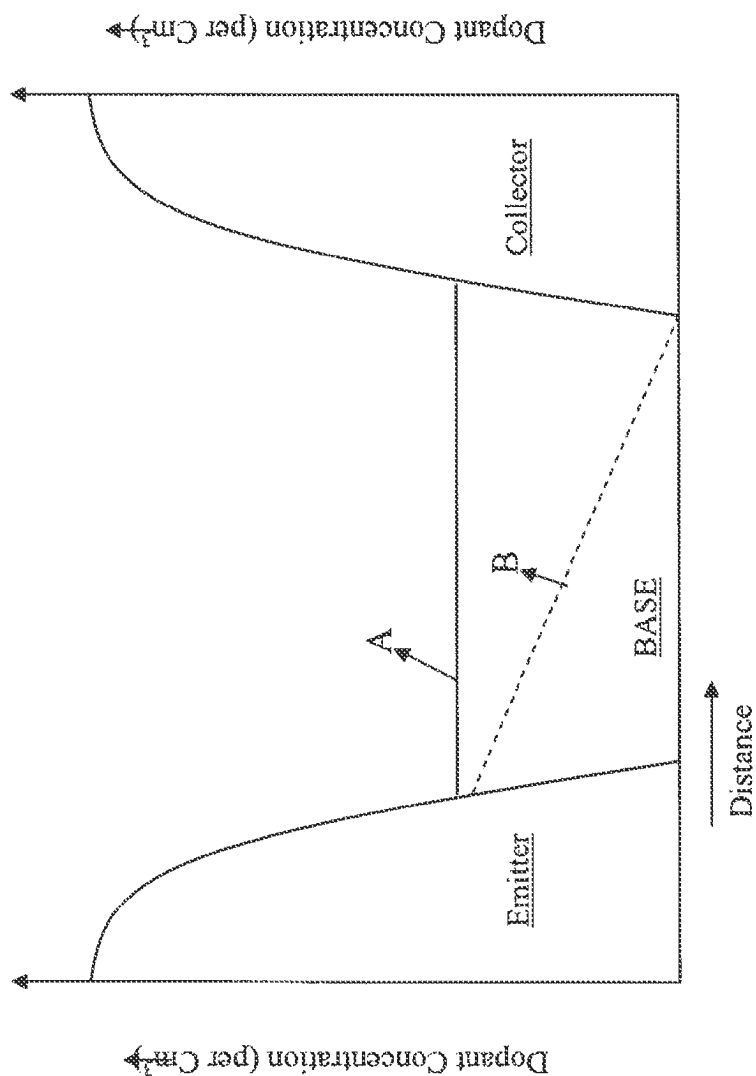


Figure 1 Prior Art

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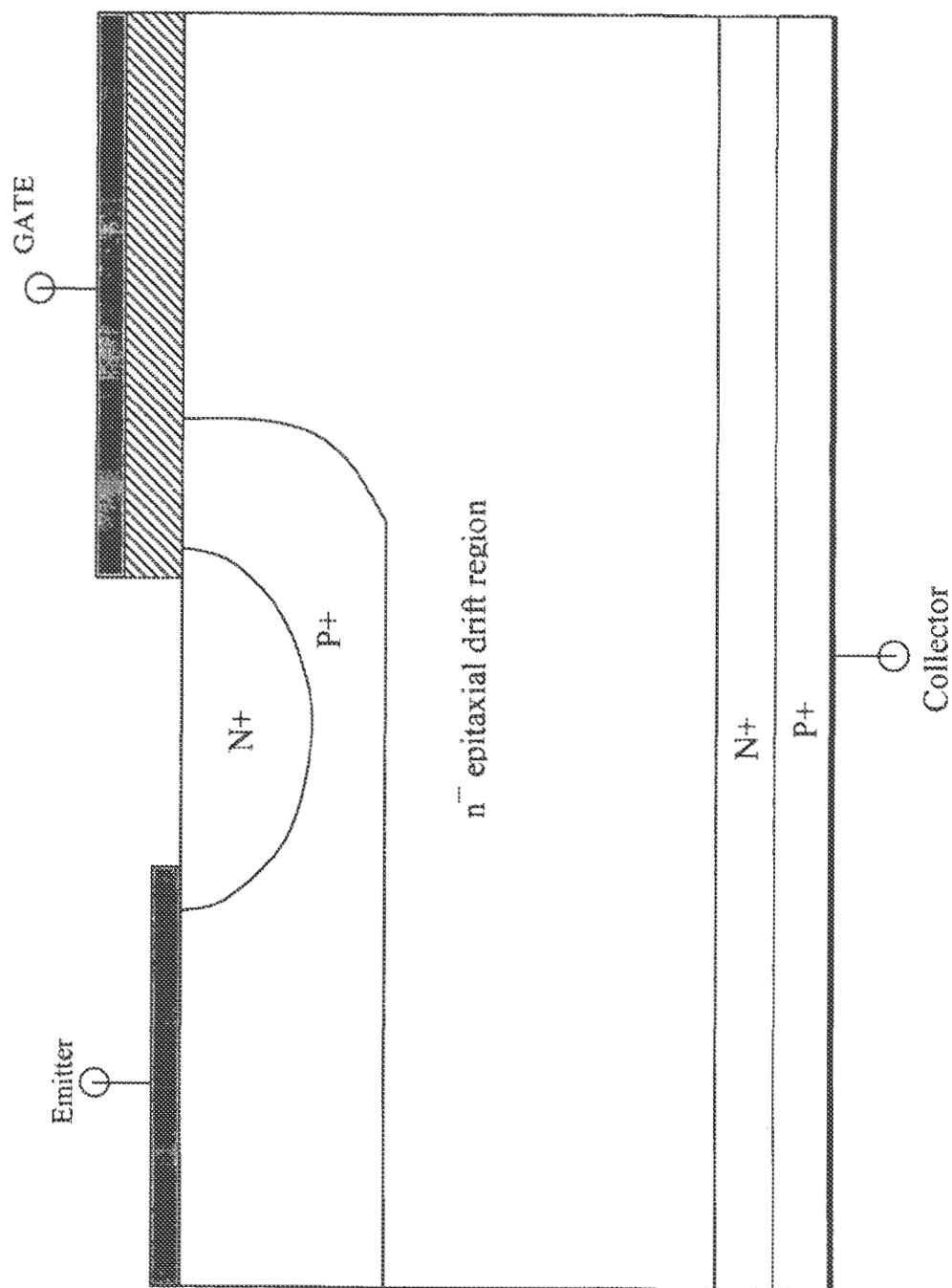


FIGURE 2 Prior art

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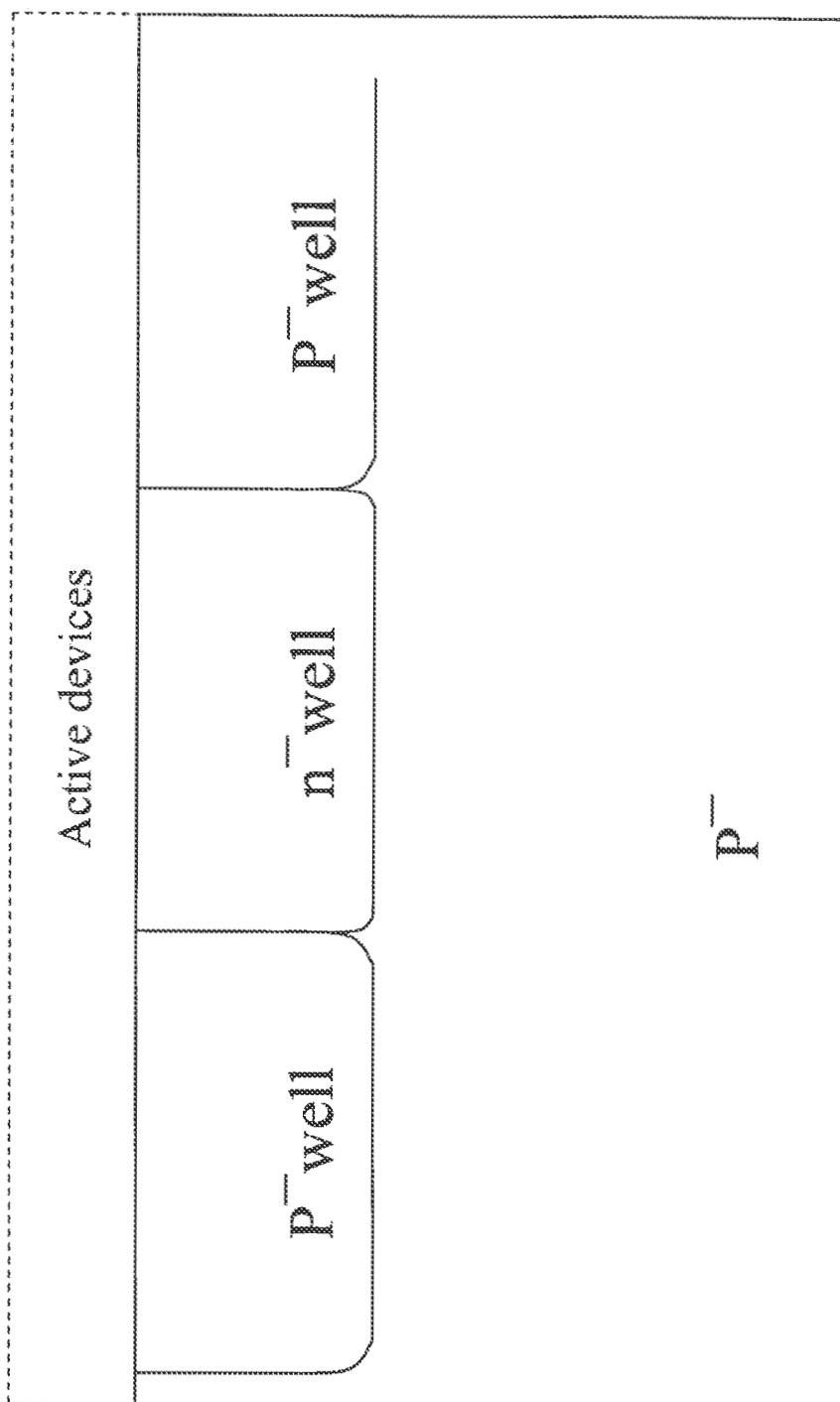


FIGURE 3A Prior art

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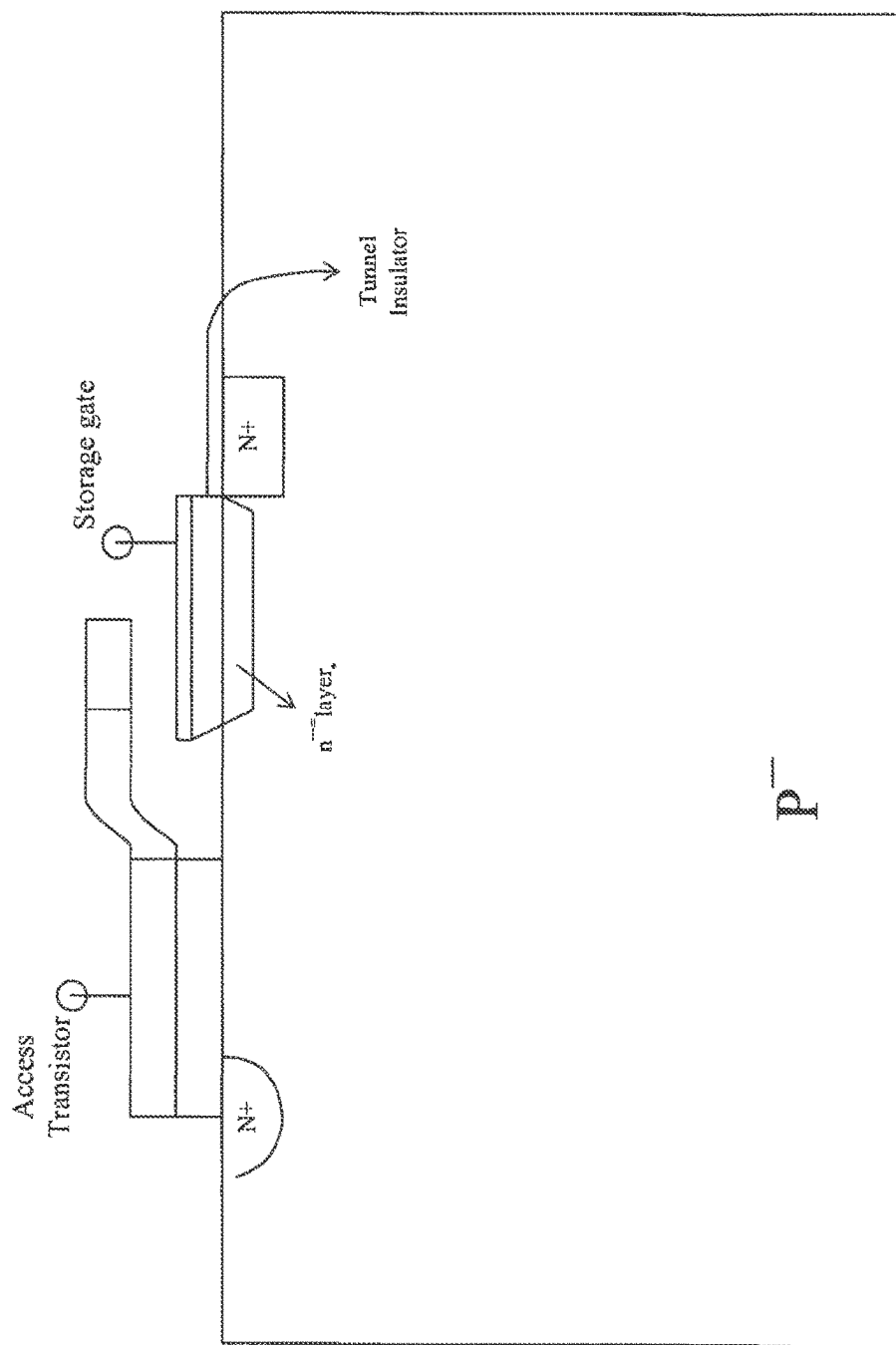


FIGURE 3B Prior art

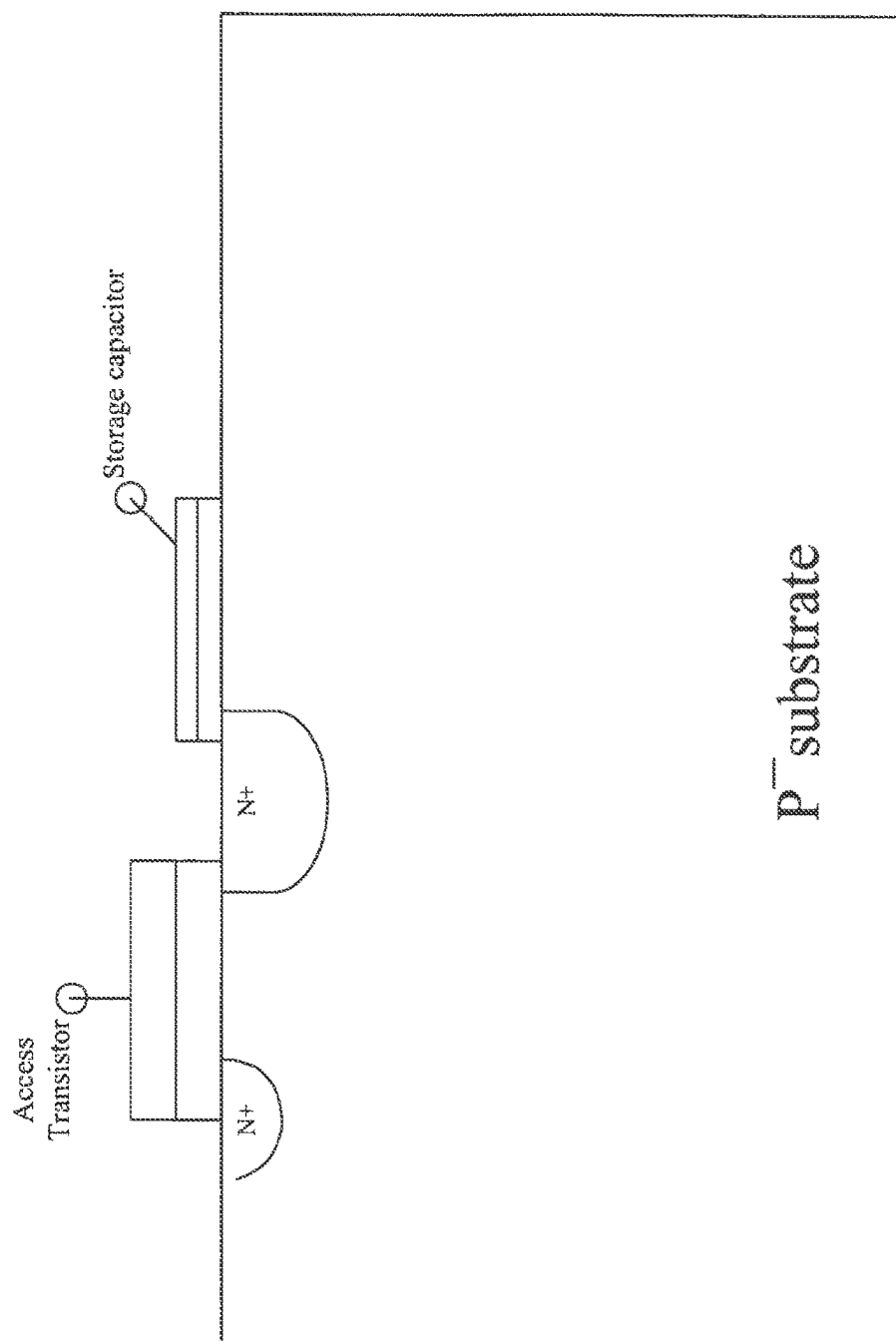


FIGURE 3C Prior art

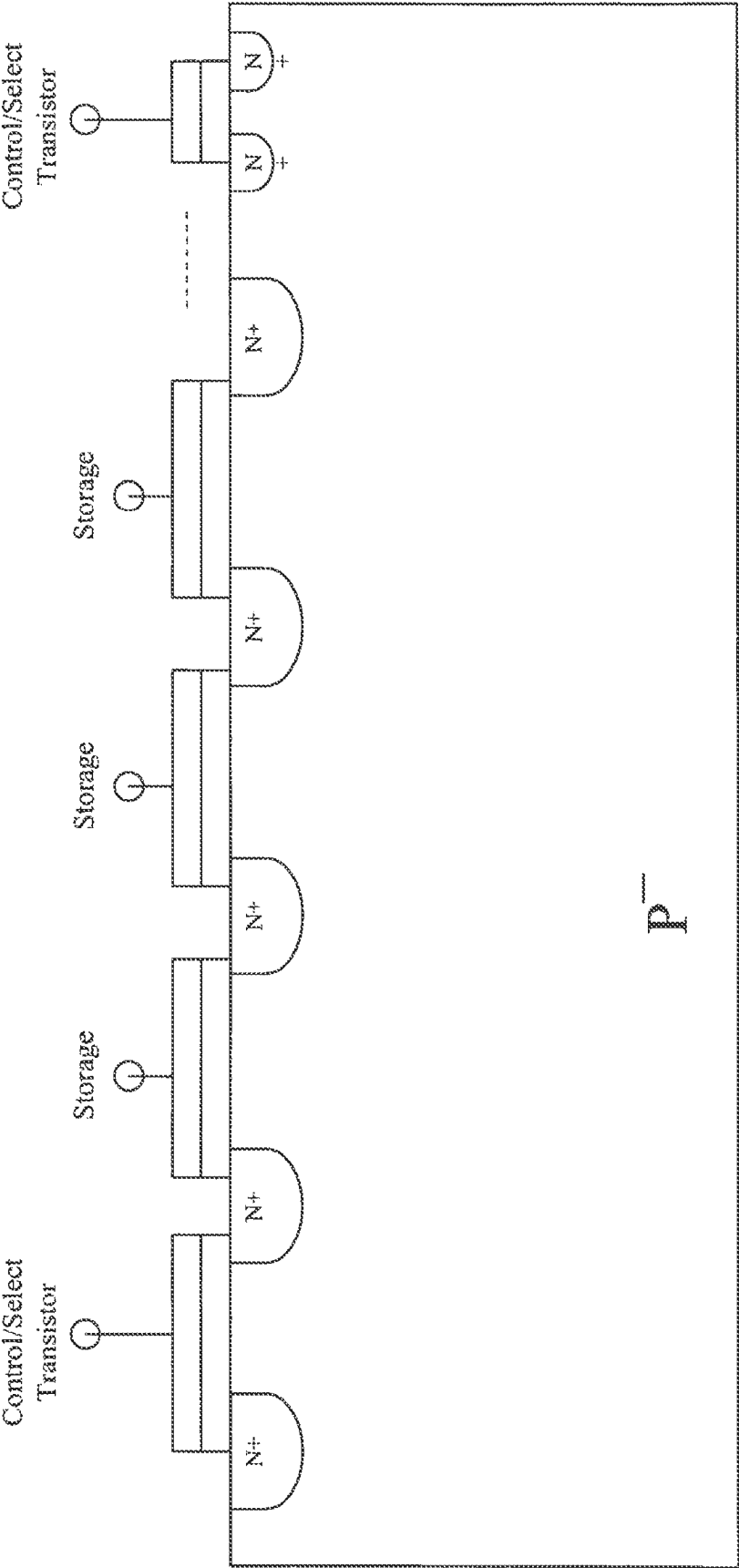


FIGURE 3D Prior art

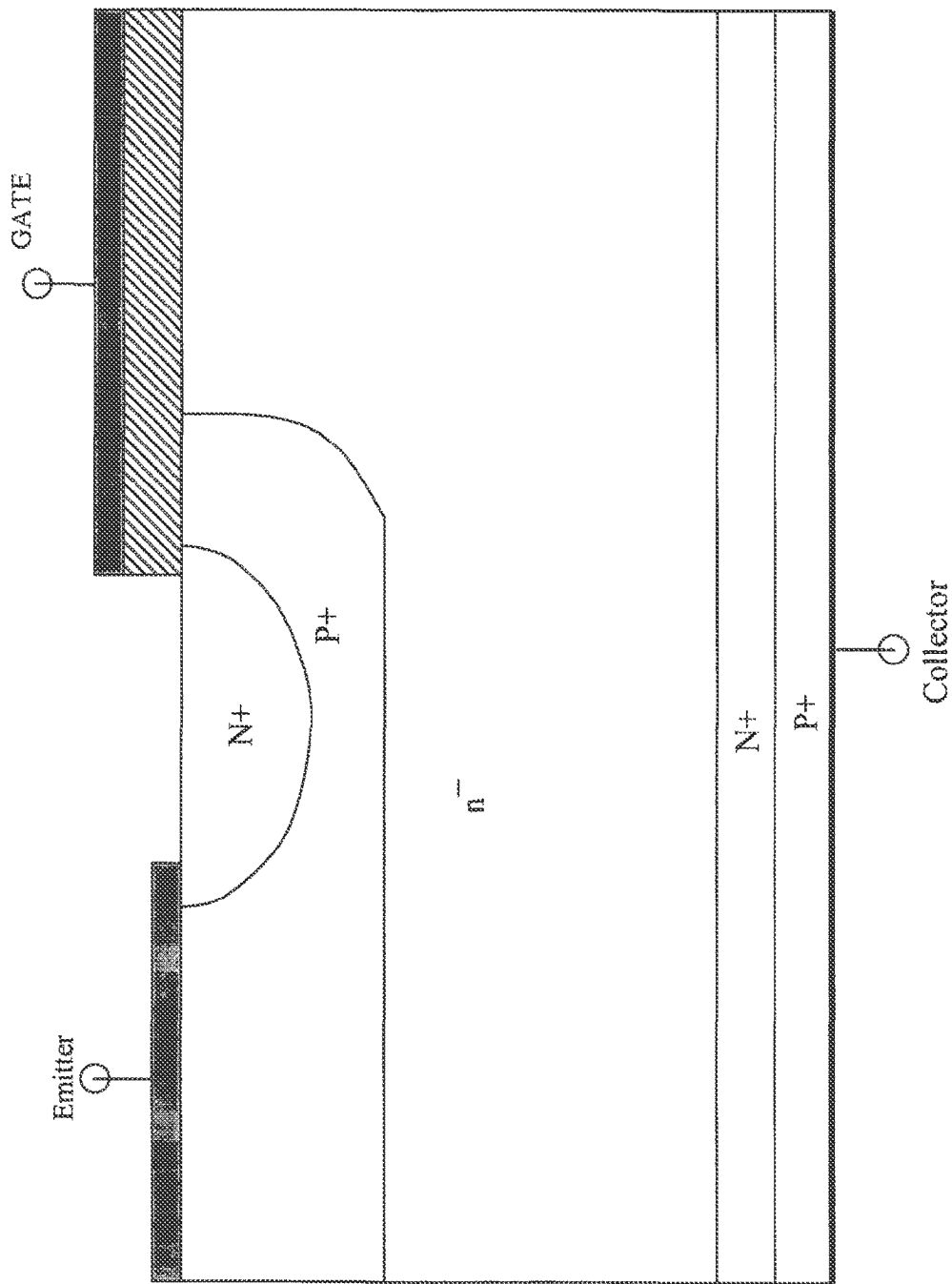


FIGURE 4

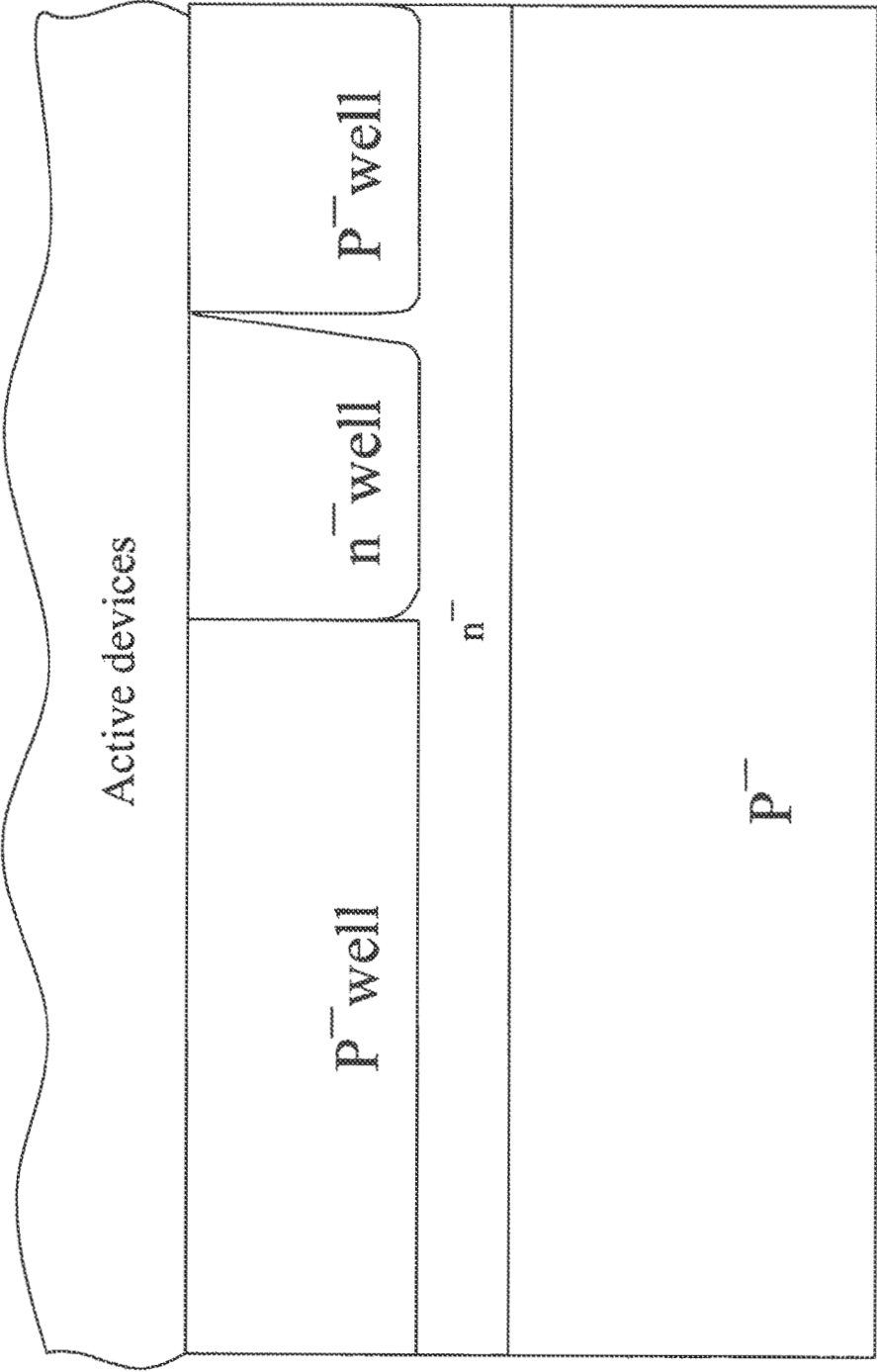


FIGURE 5A

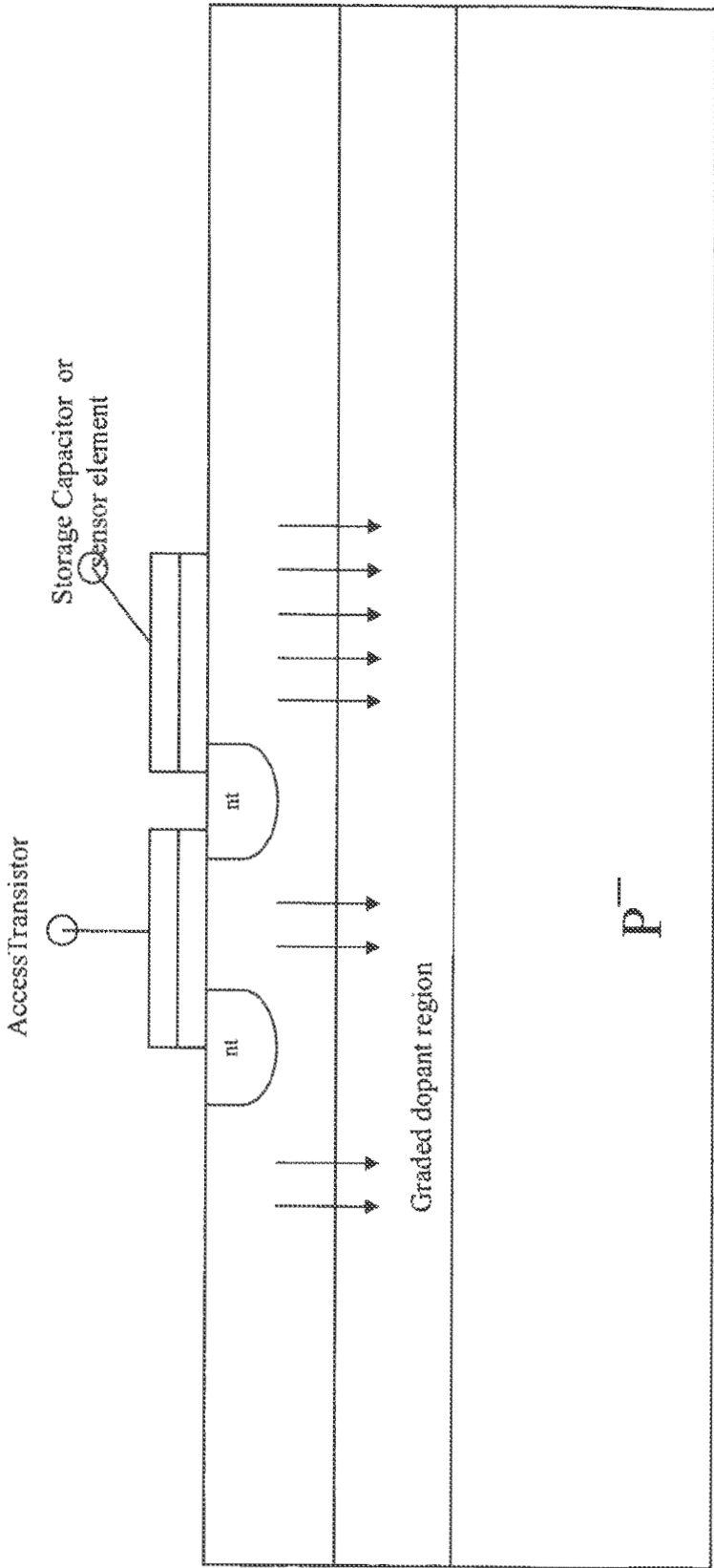


FIGURE 5B

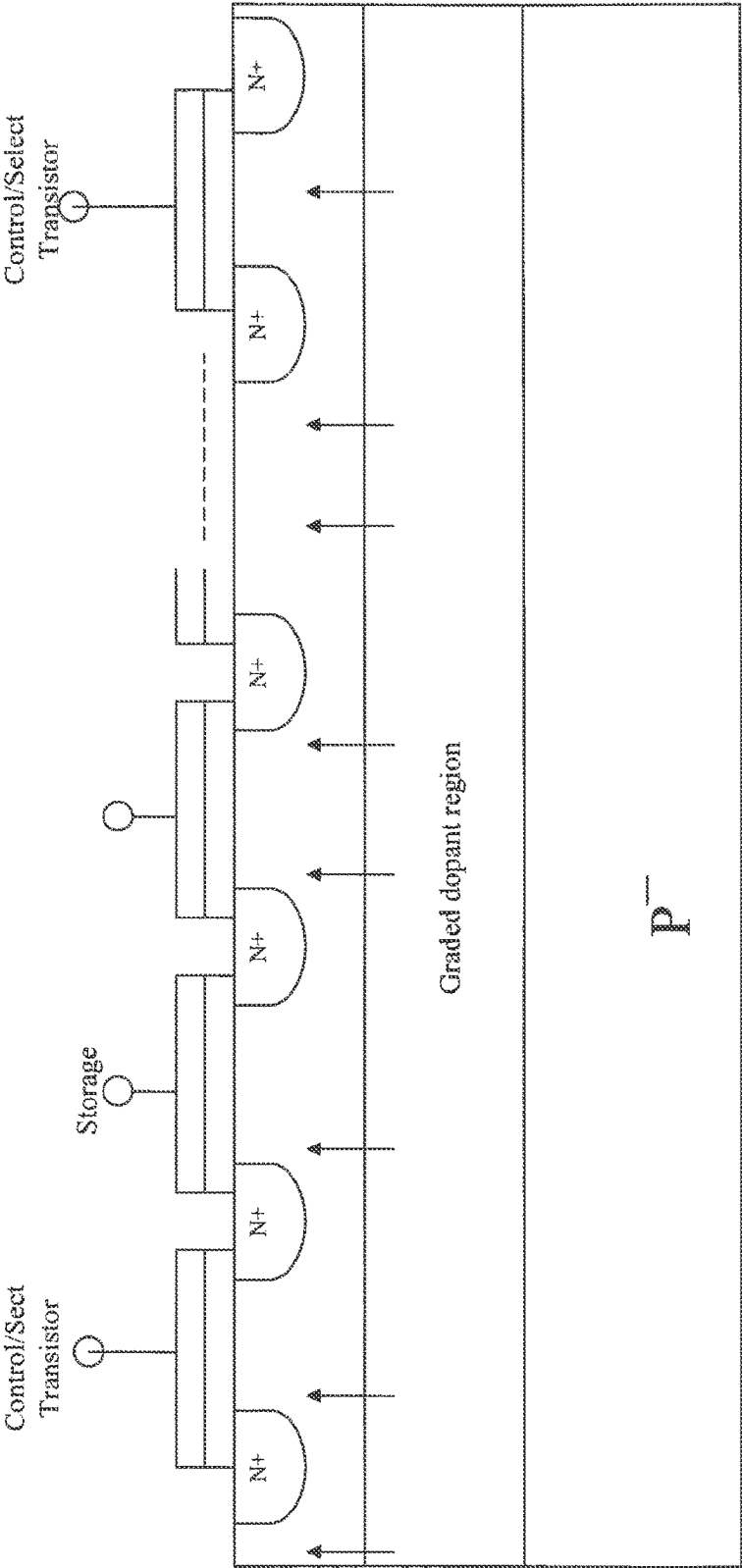


FIGURE 5C

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**SEMICONDUCTOR DEVICES WITH
GRADED DOPANT REGIONS****CROSS-REFERENCE TO RELATED
APPLICATIONS**

This application is a Continuation of U.S. patent application Ser. No. 16/947,294, filed Jul. 27, 2020, entitled SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS, which is a Continuation of U.S. patent application Ser. No. 16/717,950, filed Dec. 17, 2019, entitled SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS, issued as U.S. Pat. No. 10,734,481 on Aug. 4, 2020. U.S. patent application Ser. No. 16/717,950 is a Continuation of U.S. patent application Ser. No. 15/590,282, filed May 9, 2017, entitled SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS, issued as U.S. Pat. No. 10,510,842 on Dec. 17, 2019, which is a Continuation of U.S. patent application Ser. No. 14/931,636, filed Nov. 3, 2015, entitled SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS, issued as U.S. Pat. No. 9,647,070 on May 9, 2017, which is Continuation of U.S. patent application Ser. No. 14/515,584, filed Oct. 16, 2014, entitled SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS, issued as U.S. Pat. No. 9,190,502 on Nov. 17, 2015, which is a Continuation of U.S. patent application Ser. No. 13/854,319 filed April 1, 2013, entitled SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS, which is a Continuation of Ser. No. 11/622,496, filed Jan. 12, 2007, entitled SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS, issued as U.S. Pat. No. 8,421,195 on Apr. 16, 2013, which is a Divisional of U.S. patent application Ser. No. 10/934,915, filed Sep. 3, 2004. The disclosures of which are incorporated herein by reference in their entirety.

TECHNICAL FIELD

This present invention relates to all semiconductor devices and systems. Particularly it applies to diffused diodes, avalanche diodes, Schottky devices, power MOS transistors, JFET's, RF bipolar transistors, IGBTs (Insulated Gate Bipolar Transistors), varactors, digital VLSI, mixed signal circuits and sensor devices including camera ICs employing CCD (Charge Coupled Device) as well as CMOS technologies.

BACKGROUND

Bipolar Junction Transistors (BJT) are classified as minority carrier devices because minority carriers are the principle device conduction mechanism. However, majority carriers also play a small but finite role in modulating the conductivity in BJTs. Consequently, both carriers (electrons and holes) play a role in the switching performance of BJTs. The maximum frequency of operation in BJTs is limited by the base transit time as well as the quick recombination of the majority carriers when the device is switched off (prior to beginning the next cycle). The dominant carrier mechanism in BJTs is carrier diffusion. The carrier drift current component is fairly small, especially in uniformly doped base BJTs. Efforts have been made in graded base transistors to create an aiding drift field to enhance the diffusing minority carrier's speed from emitter to collector. However, most semiconductor devices, including various power MOSFETs (traditional, DMOS, lateral, vertical and a host of other configurations), IGBT's (Insulated Gated Base Transistors),

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still use a uniformly doped 'drift epitaxial' region in the base. FIG. 1 shows the relative doping concentration versus distance in a BJT. FIG. 2 shows the uniformly doped epi region in an IGBT. In contrast to BJTs, MOS devices are majority carrier devices for conduction. The conduction is channel dominated. The channel can be a surface in one plane in planar devices. The surface can also be on the sidewalls in a vertical device. Other device architectures to combine planar and vertical conduction are also possible. The maximum frequency of operation is dictated primarily by source-drain separation distance. Most MOS devices use a uniformly doped substrate (or a well region). When a MOSFET is optimally integrated with a BJT in a monolithic fashion, an IGBT results. The IGBT inherits the advantages of both MOSFET and BJT. It also brings new challenges because the required characteristics (electron transit and hole recombination as fast as possible in n-channel IGBT) necessitate different dopant gradients either in the same layer at different positions, or at the interfaces of similar or dissimilar layers.

Retrograde wells have been attempted, with little success, to help improve soft error immunity in SRAMs and visual quality in imaging circuits. FIG. 3A shows a typical CMOS VLSI device employing a twin well substrate, on which active devices are subsequently fabricated. FIGS. 3B, 3C, and 3D illustrate device cross sections, as practiced today. Retrograde and halo wells have also been attempted to improve refresh time in DRAMs (dynamic random-access memories), as well as, reducing dark current (background noise) and enhance RGB (Red, Green, Blue) color resolution in digital camera ICs. Most of these techniques either divert the minority carriers away from the active regions of critical charge storage nodes at the surface, or, increase minority carrier density locally as the particular application requires.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. 1 illustrates the relative doping profiles of emitter, base and collector for the two most popular bipolar junction transistors: namely, uniform base ("A") and graded base ("B");

FIG. 2 illustrates the cross section of a commercial IGBT with a uniform epitaxial drift region (base);

FIGS. 3A, 3B, 3C, and 3D illustrate cross sections of commonly used prior art CMOS silicon substrates; FIG. 3A showing a typical prior art IC with two wells (one n⁻ well in which p-channel transistors are subsequently fabricated and one p⁻ well in which n-channel transistors are subsequently fabricated); FIG. 3B showing a prior art EEPROM (Electrically Erasable Programmable Read-Only Memory) memory cell having a tunnel insulator; FIG. 3C showing a prior art DRAM memory cell; and FIG. 3D showing a prior art NAND flash memory cell;

FIG. 4 illustrates the cross section of an IGBT, using one embodiment of the invention described here, where the dopant is optimally graded in the epitaxial drift region; and

FIGS. 5A, 5B, and 5C illustrate the cross sections of a CMOS silicon substrate with two wells and an underlying layer using embodiments of the invention to improve performance in each application—VLSI logic, DRAM/image IC, nonvolatile memory IC.

DETAILED DESCRIPTION

The relative doping concentrations of emitter and collector regions varies from 10¹⁸ to 10²⁰/cm³ whereas the base

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region is 10^{14} to $10^{16}/\text{cm}^3$ depending on the desired characteristics of the BJT. In graded base p-n-p transistors, the donor dopant concentration may be 10 to 100x at the emitter-base junction, relative to the base-collector junction (1x). The gradient can be linear, quasi linear, exponential or complimentary error function. The relative slope of the donor concentration throughout the base creates a suitable aiding drift electric field, to help the holes (p-n-p transistor) transverse from emitter to collector. Since the aiding drift electric field helps hole conduction, the current gain at a given frequency is enhanced, relative to a uniformly-doped (base) BJT. The improvement in cut-off frequency (or, frequency at unity gain, f_T) can be as large as 2x-5x. Similar performance improvements are also applicable to n-p-n transistors.

As illustrated in FIG. 4, in one embodiment according to the invention, a donor gradient is established from the emitter-drift epitaxial base region junction of the punch-through IGBT, to the drift epitaxial base region— n^+ buffer layer boundary (electrons in this case are accelerated in their transit from emitter to collector). The “average” base resistance is optimized so that conductivity modulation and lifetime (for minority carriers) in the base region are not compromised. By sweeping the carriers towards the n^+ buffer region a number of advantages are obtained. First, the frequency of operation (combination of t_{on} and t_{off} as is known in the IGBT commercial nomenclature) can be enhanced. Second, and maybe more importantly, during t_{off} holes can be recombined much quicker at the n^+ buffer layer, compared to the uniformly doped n^- epitaxial drift region by establishing a different dopant gradient near the n^+ buffer layer. It should be noted that the drift region can also be a non-epitaxial silicon substrate. Although epitaxy enhances lifetime, it is not mandatory. Different layers of dopant regions can be transferred through wafer to wafer bonding (or other similar transfer mechanisms) for eventual device fabrication. The “reverse recovery time” for an IGBT is significantly improved due to the optimized graded dopant in the so called “drift region” as well as at the interfaces of the drift region. Graded dopants can also be implemented in the n^+ buffer layer as well as other regions adjacent to the respective layers. Two important performance enhancements are the result of dopant gradients. For example, in an n-channel IGBT, electrons can be swept from source to drain rapidly, while at the same time holes can be recombined closer to the n^+ buffer layer. This can improve t_{on} and t_{off} in the same device.

As illustrated in FIGS. 5A, 5B, and 5C, donor gradient is also of benefit to very large scale integrated circuits (VLSI)—VLSI logic, DRAM, nonvolatile memory like NAND flash. Spurious minority carriers can be generated by clock switching in digital VLSI logic and memory ICs. These unwanted carriers can discharge dynamically-held “actively held high” nodes. In most cases, statically-held nodes (with V_{cc}) cannot be affected. Degradation of refresh time in DRAMs is one of the results, because the capacitor holds charge dynamically. Similarly, degradation of CMOS digital images in digital imaging ICs is another result of the havoc caused by minority carriers. Pixel and color resolution can be significantly enhanced in imaging ICs with the embodiments described herein. Creating “subterranean” recombination centers underneath the wells (gold doping, platinum doping) as is done in some high-voltage diodes is not practical for VLSI circuits. Hence, a novel technique is described herein which creates a drift field to sweep these unwanted minority carriers from the active circuitry at the surface into the substrate in a monolithic die as quickly as

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possible. In a preferred embodiment, the subterranean n^- layer has a graded donor concentration to sweep the minority carriers deep into the substrate. One or more of such layers can also be implemented through wafer to wafer bonding or similar “transfer” mechanisms. This n^- layer can be a deeply-implanted layer. It can also be an epitaxial layer. As desired, the n^- well and p^- wells can also be graded or retrograded in dopants to sweep those carriers away from the surface as well. The graded dopant can also be implemented in surface channel MOS devices to accelerate majority carriers towards the drain. To decrease programming time in nonvolatile memory devices, carriers should be accelerated towards the surface when programming of memory cells is executed. The graded dopant can also be used to fabricate superior Junction Field-Effect transistors where the “channel pinch-off” is controlled by a graded channel instead of a uniformly doped channel (as practiced in the prior art).

One of ordinary skill and familiarity in the art will recognize that the concepts taught herein can be customized and tailored to a particular application in many advantageous ways. For instance, minority carriers can be channeled to the surface to aid programming in nonvolatile memory devices (NOR, NAND, multivalued-cell). Moreover, single-well, and triple-well CMOS fabrication techniques can also be optimized to incorporate these embodiments individually and collectively. Any modifications of such embodiments (described here) fall within the spirit and scope of the invention. Hence, they fall within the scope of the claims described below.

Although the invention has been described with reference to specific embodiments, these descriptions are not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as alternative embodiments of the invention will become apparent to persons skilled in the art upon reference to the description of the invention. It should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

It is therefore, contemplated that the claims will cover any such modifications or embodiments that fall within the true scope of the invention.

What is claimed is:

1. An electronic system, the system comprising:
 - at least one semiconductor device, the at least one semiconductor device including:
 - a substrate of a first doping type at a first doping level having a surface;
 - a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
 - a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
 - transistors formed in at least one of the first active region or second active region;
 - at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and

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at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the semiconductor device.

2. The system of claim 1, wherein the substrate of the at least one semiconductor device is a p-type substrate.

3. The system of claim 1, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.

4. The system of claim 1, wherein the first active region and second active region of the at least one semiconductor device contain digital logic formed by one of either p-channel and n-channel devices.

5. The system of claim 1, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.

6. The system of claim 1, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.

7. The system of claim 1, wherein the graded dopant is fabricated with an ion implantation process.

8. The system of claim 1, wherein the first and second active regions of the at least one semiconductor device are formed adjacent the first surface of the substrate of the at least one semiconductor device.

9. The system of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.

10. The system of claim 1, wherein dopants of the graded dopant concentration in the first active region of the at least one semiconductor device are both p-type and n-type.

11. The system of claim 1, wherein dopants of the graded dopant concentration in the second active region of the at least one semiconductor device are both p-type and n-type.

12. The system of claim 1, wherein dopants of the graded dopant region in the well region of the at least one semiconductor device are both p-type and n-type.

13. The system of claim 1, wherein the transistors which can be formed in the first and second active regions of the at least one semiconductor device are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.

14. The system of claim 1, wherein the at least one semiconductor device is a dynamic random access memory (DRAM).

15. The system of claim 1, wherein the at least one semiconductor device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.

16. The system of claim 1, wherein the at least one semiconductor device is a flash memory.

17. The system of claim 1, wherein the at least one semiconductor device comprises digital logic and capacitors.

18. The system of claim 1, wherein the at least one semiconductor device is a central processing unit.

19. The system of claim 1, wherein the at least one semiconductor device is an image sensor.

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20. The system of claim 1, wherein each of the first and second active regions of the at least one semiconductor device are in the lateral or vertical direction.

21. An electronic system, comprising:

at least one semiconductor device, the at least one semiconductor device including:

a substrate of a first doping type at a first doping level having a surface;

a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;

transistors formed in at least one of the first active region or second active region;

at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and

at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.

22. The system of claim 21, wherein the substrate of the at least one semiconductor device is an n-type substrate.

23. The system of claim 21, wherein the substrate of the at least one semiconductor device is a p-type substrate.

24. The system of claim 21, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.

25. The system of claim 21, wherein the first active region and second active region of the at least one semiconductor device contain at least one of either p-channel and n-channel devices.

26. The system of claim 21, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.

27. The system of claim 21, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.

28. The system of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.

29. The system of claim 21, wherein dopants of the graded dopant concentration in the first active region of the at least one semiconductor device are both p-type and n-type.

30. The system of claim 21, wherein dopants of the graded dopant concentration in the second active region of the at least one semiconductor device are both p-type and n-type.

* * * * *

EXHIBIT 7

PATENT ASSIGNMENT COVER SHEETElectronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT3351825

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT
CONVEYING PARTY DATA	
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G.R. MOHAN RAO	04/27/2015
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Name:	GREENTHREAD, LLC
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State/Country:	TEXAS
Postal Code:	75229-5400
PROPERTY NUMBERS Total: 9	
Property Type	Number
Application Number:	10934915
Patent Number:	8421195
Patent Number:	8106481
Application Number:	13854319
Application Number:	14515584
Application Number:	60982175
Application Number:	14335160
Application Number:	61509257
Application Number:	14525411
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NAME OF SUBMITTER:	GREGORY M. HOWISON

SIGNATURE:	/Gregory M. Howison, Reg. #30646/
DATE SIGNED:	05/13/2015
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ASSIGNMENT

WHEREAS, G.R. MOHAN RAO, an individual, residing at 1611 Willingham Drive, Allen, Texas 75013 ("Assignor"), has invented certain new and useful inventions set forth on the attached Exhibit A (collectively, the "Inventions"), for which certain applications for United States and foreign patents were filed as set forth on Exhibit A (collectively, the "Applications"), and from which certain United States patents have issued as set forth on Exhibit A (collectively, the "Patents"); and

WHEREAS, GREENTHREAD, LLC, a Texas Limited Liability Company, having a business address at 4544 Harrys Lane, Dallas, Texas 75229-5400 ("Assignee"), is desirous of acquiring the entire right, title, and interest in and to the Applications and Patents and any and all foreign counterparts, divisions, continuations, continuation-in-parts, improvements, reexaminations, reissues, extensions, renewals, substitutes, provisional applications, certificates, all rights under the International Convention for the Protection of Industrial Property and prolongations of the Applications and Patents.

Now, THEREFORE, for other good and valuable consideration, Assignor, by these presents does hereby irrevocably sell, assign, and transfer unto Assignee, its successors, assigns, and legal representatives the full and exclusive right in and to:

- (a) the Applications and Patents in the United States and the entire right, title, and interest in and to any and all issued patents or patent applications which may be granted therefor and/or therefrom in the United States, to all divisions, reissues, substitutions, continuations, continuations-in-part, and extensions of said Applications and Patents and any pending applications or issued patents that directly claim or are amended to claim priority to any of the Applications or Patents;
- (b) all causes of action (whether known or unknown or whether currently pending, filed or otherwise) and other enforcement rights under or on account of the Applications and Patents, including without limitation all causes of action and other enforcement rights for damages, injunctive relief, and any other remedies of any kind for past, current and future infringement; and
- (c) all rights to collect royalties or other payments under or on account of the Applications and Patents and the foregoing subcategory (b).

Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks to issue all patents for the Applications, or patents resulting therefrom, insofar as Assignor's interests are concerned, to Assignee, of the entire right, title, and interest in and to the same, for its sole use and benefit; and for the use and benefit of its legal representatives, to the full end of the term for which said patents may be granted, as fully and entirely as the same would have been held by the Assignor had this assignment not been made.

Assignor also sells and assigns to Assignee, its successors, assigns and legal representatives the full and exclusive right, title, and interest in and to the Inventions disclosed in

said Applications throughout the world, including the right to file applications and obtain patents, utility models, industrial models, and designs for the inventions in the Assignee's own name throughout the world, including all rights of priority, all rights to publish cautionary notices reserving ownership of the inventions and all rights to register the inventions in appropriate registries, all foreign rights arising from pre-grant publication of the Applications; and Assignor further agrees to execute any and all powers of attorney, applications, assignments, declarations, affidavits, and any other papers in connection therewith necessary to perfect such right, title and interest in Assignee, its successors, assigns and legal representatives.

Assignor further agrees to communicate to Assignee, its successors, assigns and/or legal representatives, any known facts respecting any improvements, and, at the expense of Assignee, to testify in any legal proceedings, sign all lawful papers, execute all divisional, continuation, continuation-in-part, reissue and substitute applications, make all lawful oaths, and generally do everything possible to vest title in Assignee and to aid Assignee, its successors, assigns and legal representatives to obtain and enforce proper protection for the Inventions in all countries.

[Signature Page to Follow]

G.R. Mohan Rao
G.R. Mohan Rao

April 27, 2015
Date

STATE OF: Texas

COUNTY OF: Dallas

BEFORE ME, a Notary Public, on this 27th day of April, 2017, personally appeared G.R. MOHAN RAO, known to me to be the person whose name is subscribed to the foregoing instrument and acknowledged to me that he/she executed same of his/her own free will for the purposes and consideration therein expressed.

[SEAL]

Kristy Lea Kyles
Notary Public
Commission Expires: 9-9-17

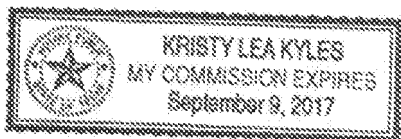


EXHIBIT A

	Atty. Ref.	Country	Serial No.	Patent No.	Title
1.	32625	US	10/934,915		Semiconductor Devices with Graded Dopant Regions
2.	32611	US	11/622,496	8,421,195	Semiconductor Devices with Graded Dopant Regions
3.	32612	US	12/549,283	8,106,481	Semiconductor Devices with Graded Dopant Regions
4.	32626	US	13/854,319		Semiconductor Devices with Graded Dopant Regions
5.	32613	US	14/515,584		Semiconductor Devices with Graded Dopant Regions
6.	32623	US	60/982,175		Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
7.	32614	US	12/256,362	7,855,916	Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
8.	32615	US	12/915,177	8,194,452	Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
9.	32616	US	13/458,173	8,531,880	Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
10.	32617	US	13/967,649	8,817,537	Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
11.	32618	US	14/335,160		Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
12.	32624	US	61/509,257		Lifetime Mixed Level Non-Volatile Memory System
13.	32619	US	13/455,267	8,891,298	Lifetime Mixed Level Non-Volatile Memory System
14.	32620	US	14/525,411		Lifetime Mixed Level Non-Volatile Memory System



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NATURE OF CONVEYANCE:	CONFIRMATORY ASSIGNMENT										
CONVEYING PARTY DATA											
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Name	Execution Date										
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RECEIVING PARTY DATA											
<table border="1"><tr><td>Name:</td><td>GREENTHREAD, LLC</td></tr><tr><td>Street Address:</td><td>4544 HARRYS LANE</td></tr><tr><td>City:</td><td>DALLAS</td></tr><tr><td>State/Country:</td><td>TEXAS</td></tr><tr><td>Postal Code:</td><td>75229-5400</td></tr></table>	Name:	GREENTHREAD, LLC	Street Address:	4544 HARRYS LANE	City:	DALLAS	State/Country:	TEXAS	Postal Code:	75229-5400	
Name:	GREENTHREAD, LLC										
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City:	DALLAS										
State/Country:	TEXAS										
Postal Code:	75229-5400										
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Property Type	Number										
Application Number:	17371839										
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Greenthread Ex. 2023, p. 124 of 208
Texas Instruments v. Greenthread

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ATTORNEY DOCKET NUMBER:	GRTD60-35314
NAME OF SUBMITTER:	GREGORY M. HOWISON
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Date:	03/07/2022
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EPAS ID: PAT6827716

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NATURE OF CONVEYANCE:	ASSIGNMENT	
CONVEYING PARTY DATA		
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	MR G.R. MOHAN RAO	09/09/2017
RECEIVING PARTY DATA		
Name:	GREENTHREAD, LLC	
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Property Type	Number	
Application Number:	17371839	
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SIGNATURE:	/Gregory Howison - Reg# 30646/	
DATE SIGNED:	07/22/2021	
Total Attachments: 4		
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source=GRT34138RaotoGreenthreadASSMTEXE#page4.tif		

ASSIGNMENT

WHEREAS, G.R. MOHAN RAO, an individual, residing at 1611 Willingham Drive, Allen, Texas 75013 ("Assignor"), has invented certain new and useful inventions set forth on the attached Exhibit A (collectively, the "Inventions"), for which certain applications for United States and foreign patents were filed as set forth on Exhibit A (collectively, the "Applications"), and from which certain United States patents have issued as set forth on Exhibit A (collectively, the "Patents"); and

WHEREAS, GREENTHREAD, LLC, a Texas Limited Liability Company, having a business address at 4544 Harrys Lane, Dallas, Texas 75229-5400 ("Assignee"), is desirous of acquiring the entire right, title, and interest in and to the Applications and Patents and any and all foreign counterparts, divisions, continuations, continuation-in-parts, improvements, reexaminations, reissues, extensions, renewals, substitutes, provisional applications, certificates, all rights under the International Convention for the Protection of Industrial Property and prolongations of the Applications and Patents.

Now, THEREFORE, for other good and valuable consideration, Assignor, by these presents does hereby irrevocably sell, assign, and transfer unto Assignee, its successors, assigns, and legal representatives the full and exclusive right in and to:

- (a) the Applications and Patents in the United States and the entire right, title, and interest in and to any and all issued patents or patent applications which may be granted therefor and/or therefrom in the United States, to all divisions, reissues, substitutions, continuations, continuations-in-part, and extensions of said Applications and Patents and any pending applications or issued patents that directly claim or are amended to claim priority to any of the Applications or Patents;
- (b) all causes of action (whether known or unknown or whether currently pending, filed or otherwise) and other enforcement rights under or on account of the Applications and Patents, including without limitation all causes of action and other enforcement rights for damages, injunctive relief, and any other remedies of any kind for past, current and future infringement; and
- (c) all rights to collect royalties or other payments under or on account of the Applications and Patents and the foregoing subcategory (b).

Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks to issue all patents for the Applications, or patents resulting therefrom, insofar as Assignor's interests are concerned, to Assignee, of the entire right, title, and interest in and to the same, for its sole use and benefit; and for the use and benefit of its legal representatives, to the full end of the term for which said patents may be granted, as fully and entirely as the same would have been held by the Assignor had this assignment not been made.

Assignor also sells and assigns to Assignee, its successors, assigns and legal representatives the full and exclusive right, title, and interest in and to the Inventions disclosed in

said Applications throughout the world, including the right to file applications and obtain patents, utility models, industrial models, and designs for the inventions in the Assignee's own name throughout the world, including all rights of priority, all rights to publish cautionary notices reserving ownership of the inventions and all rights to register the inventions in appropriate registries, all foreign rights arising from pre-grant publication of the Applications; and Assignor further agrees to execute any and all powers of attorney, applications, assignments, declarations, affidavits, and any other papers in connection therewith necessary to perfect such right, title and interest in Assignee, its successors, assigns and legal representatives.

Assignor further agrees to communicate to Assignee, its successors, assigns and/or legal representatives, any known facts respecting any improvements, and, at the expense of Assignee, to testify in any legal proceedings, sign all lawful papers, execute all divisional, continuation, continuation-in-part, reissue and substitute applications, make all lawful oaths, and generally do everything possible to vest title in Assignee and to aid Assignee, its successors, assigns and legal representatives to obtain and enforce proper protection for the Inventions in all countries.

[Signature Page to Follow]

G.R. Mohan Rao
G.R. Mohan Rao

April 27, 2015
Date

STATE OF: Texas

COUNTY OF: Dallas

BEFORE ME, a Notary Public, on this 27th day of April, 2017, personally appeared G.R. MOHAN RAO, known to me to be the person whose name is subscribed to the foregoing instrument and acknowledged to me that he/she executed same of his/her own free will for the purposes and consideration therein expressed.

[SEAL]

Kristy Lea Kyles
Notary Public
Commission Expires: 9-9-17

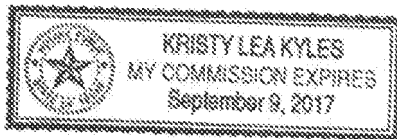


EXHIBIT A

	Atty. Ref.	Country	Serial No.	Patent No.	Title
1.	32625	US	10/934,915		Semiconductor Devices with Graded Dopant Regions
2.	32611	US	11/622,496	8,421,195	Semiconductor Devices with Graded Dopant Regions
3.	32612	US	12/549,283	8,106,481	Semiconductor Devices with Graded Dopant Regions
4.	32626	US	13/854,319		Semiconductor Devices with Graded Dopant Regions
5.	32613	US	14/515,584		Semiconductor Devices with Graded Dopant Regions
6.	32623	US	60/982,175		Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
7.	32614	US	12/256,362	7,855,916	Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
8.	32615	US	12/915,177	8,194,452	Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
9.	32616	US	13/458,173	8,531,880	Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
10.	32617	US	13/967,649	8,817,537	Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
11.	32618	US	14/335,160		Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
12.	32624	US	61/509,257		Lifetime Mixed Level Non-Volatile Memory System
13.	32619	US	13/455,267	8,891,298	Lifetime Mixed Level Non-Volatile Memory System
14.	32620	US	14/525,411		Lifetime Mixed Level Non-Volatile Memory System

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
 Stylesheet Version v1.2

EPAS ID: PAT6827495

SUBMISSION TYPE:	NEW ASSIGNMENT	
NATURE OF CONVEYANCE:	ASSIGNMENT	
CONVEYING PARTY DATA		
	Name	Execution Date
	GREENTHREAD, LLC	08/19/2019
RECEIVING PARTY DATA		
Name:	VERVAIN, LLC	
Street Address:	724 MASON DELLS DRIVE	
City:	DALLAS	
State/Country:	TEXAS	
Postal Code:	75230	
PROPERTY NUMBERS Total: 1		
Property Type	Number	
Application Number:	17371839	
CORRESPONDENCE DATA		
Fax Number:	(972)628-3616	
<i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i>		
Phone:	972-628-3624	
Email:	ipdocketing@munckwilson.com	
Correspondent Name:	GREGORY HOWISON	
Address Line 1:	12770 COIT ROAD SUITE 660	
Address Line 2:	SUITE 660	
Address Line 4:	DALLAS, TEXAS 75251	
NAME OF SUBMITTER:	GREGORY HOWISON	
SIGNATURE:	/Gregory Howison - Reg# 30646/	
DATE SIGNED:	07/22/2021	
Total Attachments: 2		
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source=20200527CorrectedAssignment#page2.tif		

ASSIGNOR Greenthread, LLC Philip W. John, Jr. Manager 6307 Bandera Ave, Apt B Dallas, Texas 75225-3617 Email: john@greenthreadllc.com	ASSIGNEE Vervain, LLC Philip W. John, Jr., Member 7424 Mason Dells Drive Dallas, Texas 75230-3244 Email: john@vervainllc.com
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ASSIGNMENT AGREEMENT

This Assignment Agreement ("Assignment") is entered into by and between Vervain, LLC, a Texas limited liability company, hereinafter referred to as "Assignee," and Greenthread, LLC, a Texas limited liability company, hereinafter referred to as "Assignor," and shall become effective upon being duly signed by the authorized representative of Assignor ("Effective Date").

RECITALS:

Assignor and Assignee are entering into a Patent Assignment Agreement (the "Agreement").

Pursuant to the Agreement, Assignor hereby desires to assign to Assignee all of its rights, title and interest in and to the following United States patents and pending application:

1. U.S. Provisional Application Number ~~61/509,256~~ ^{61/509,257}, entitled, "Lifetime Mixed Level Nand Flash System," filed on July 19, 2011;
2. U.S. Patent Number 8,891,298, entitled, "Lifetime Mixed Level Non-Volatile Memory System," filed on April 25, 2012, and issued on November 18, 2014;
3. U.S. Patent Number 9,196,385, entitled, "Lifetime Mixed Level Non-Volatile Memory System," filed on October 28, 2014, and issued on November 24, 2015;
4. U.S. Patent Number 9,997,240, entitled, "Lifetime Mixed Level Non-Volatile Memory System," filed on November 24, 2015, and issued on June 12, 2018, and
5. U.S. Patent Application Number 16/006,299, entitled, "Lifetime Mixed Level Non-Volatile Memory System," filed on June 12, 2018, and is pending (collectively referred to hereinafter referred to as the "Patent").

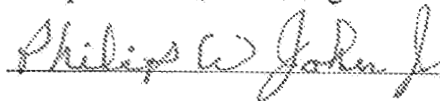
For good and valuable consideration, Assignor and Assignee hereby agree as follows:

ASSIGNMENT:

1. Assignor hereby assigns to Assignee its entire worldwide right, title and interest in and to Assignor's Patent, including the entire worldwide right, title and interest in and to any reexamination or reissue of the Patent. This includes, without limitation, Assignor's right to prosecute, and receive, all damages, royalties, awards and compensation for past, present and/or future infringement.
2. Assignor agrees to do the following without further consideration, in order to carry out the intent of this Assignment:
 - i. Execute all oaths, assignments, applications, and other papers necessary or desirable to fully secure to Assignee the rights, titles and interests herein conveyed; and
 - ii. Generally do all lawful acts for vesting in Assignee the rights, titles, and interests herein conveyed.
3. Assignor has not made and will not hereafter make any assignment, grant, mortgage, license, or other agreement affecting the rights, titles, and interests herein conveyed to Assignee.
4. Assignor hereby represents and warrants that Assignor has the authority to assign the applicable Patent pursuant to this Assignment.

The undersigned having read this Assignment and fully understanding the provisions of this Assignment, hereby executes this Assignment as of the Effective Date.

Greenthread, LLC (Assignor)
Philip W. John, Jr. Manager



Signature:

Printed Name: Philip W. John, Jr.

Date: August 9, 2019

GRTD60-35314

PATENT

CONFIRMATORY ASSIGNMENT

Whereas, **VERVAIN, LLC**, a Texas limited liability company, located at 724 Mason Dells Drive, Dallas, Texas 75230 (“Assignor”), hereby confirms that it has zero right, title and interest in and to the currently pending application entitled, SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS (the “Invention”), for which United States Patent Application was filed on July 9, 2021 (Serial No. 17/371,839) (the “Application”), and confirms the Assignment previously Assigned and recorded at reel/frame 056950/0048 on July 22, 2021 from inventor G.R. Mohan RAO to Greenthread, LLC is the only valid Assignment and the Assignment recorded on July 22, 2021 from Greenthread, LLC to Vervain, LLC at reel/frame 056949/0013 was in error as it did not list the Application; and

Whereas, **GREENTHREAD, LLC**, a Texas Limited Liability Company, located at 4544 Harrys Lane, Dallas, Texas 75229-5400 (“Assignee”), is desirous of confirming that the entire right, title, and interest in the Application is fully vested in Assignee, and desires confirmation that Assignee has never assigned any interest in and to the Application to Assignor and that Assignor has no rights to this Application, as no rights have ever been conveyed to Assignor.

Now, Therefore, for other good and valuable consideration, Assignor, by these presents does hereby sell, assign, and transfer unto Assignee, its successors, assigns, and legal representatives the full and exclusive right to the Application in the United States and the entire right, title, and interest in and to any and all Patents which may be granted therefore and/or therefrom in the United States, to all divisions, reissues, substitutions, continuations, continuations-in-part, and extensions of said application. Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks to issue all patents for the Invention, or patents resulting therefrom, insofar as Assignor's interests are concerned, to Assignee, of the entire right, title, and interest in and to the same, for his sole use and benefit; and for the use and benefit of his legal representatives, to the full end of the term for which said Patent(s) may be granted, as fully and entirely as the same would have been held by the Assignor had this assignment not been made.

Assignor also sells and assigns to Assignee, its successors, assigns and legal representatives the full and exclusive right, title, and interest to the Invention disclosed in said Application throughout the world, including the right to file applications and obtain patents, utility models, industrial models, and designs for the Invention in the Assignee's own name throughout the world, including all rights of priority, all rights to publish cautionary notices reserving ownership of the Invention and all rights to register the Invention in appropriate registries, all foreign rights arising from pre-grant publication of the Application; and Assignor further agrees to execute any and all powers of attorney, applications, assignments, declarations, affidavits, and any other papers in connection therewith necessary to perfect such right, title and interest in Assignee, its successors, assigns and legal representatives.

Assignor further agrees to communicate to Assignee, its successors, assigns and/or legal representatives, any known facts respecting any improvements, and, at the expense of Assignee, to testify in any legal proceedings, sign all lawful papers, execute all divisional, continuation, continuation-in-part, reissue and substitute applications, make all lawful oaths, and generally do everything possible to vest title in Assignee and to aid Assignee, its successors, assigns and legal representatives to obtain and enforce proper protection for the Invention in all countries.

Assignor further authorizes and directs Assignee's attorneys to insert the serial number and filing date of said application now identified by the attorney docket number and title set forth above as soon as the same shall have been made known to them by the United States Patent and Trademark Office.

VERVAIN, LLC

By: Philip W. Sohn Jr.
Name: Philip W. Sohn Jr.
Title: MANAGER
Date: 3/7/2022

Exhibit 8

Exemplar Texas Instruments Accused Products

The following list of Accused Products is exemplary, non-exhaustive, and non-limiting. Greenthread identifies the following specific products to illustrate each category or type of product that constitutes a Texas Instruments Accused Product. Greenthread further asserts claims against all product variations and part numbers of the Texas Instruments Accused Products. All of the below exemplar products were identified by Texas Instruments' website at <https://www.ti.com/product-category/new-products.html?releasePeriod=364>

Amplifiers	
1.	INA254
2.	OPA2863-QL
3.	INA310B
4.	OPA206
5.	OPA928
Microcontrollers & Processors	
1.	AM69A
2.	TMS320F2800137
3.	AM68A
4.	DRA821U
5.	TDA4VH-Q1
Digital-to-Analog Converters	
1.	DAC53001
2.	DAC63001
3.	DAC53204W
4.	DAC82001
5.	DAC82002
Analog to Digital Converters	
1.	ADS127L21
2.	ADC12DJ5200SE
3.	ADC34RF52
4.	ADS9218
5.	ADS9817
Digital Clocks	

1.	LMK6C
2.	LMK6H
3.	LMK6P
4.	LMK04832-SEP
5.	LMK5B33414
Interface ICs	
1.	DS90UB635-Q1
2.	THVD1454
3.	TCAN1462-Q1
4.	THVD2410V
5.	DS160PR1601
Audio Processors	
1.	TPA3223
2.	TAS2781
3.	PCM5120-Q1
4.	PCM3120-Q1
5.	PCM1820-Q1
Digital Light Processors	
1.	DLP4620S-Q1
2.	DLP4621-Q1
3.	DLP801XE
4.	DLP801RE
5.	DLP301S
Isolation ICs	
1.	ISOW7742-Q1
2.	ISOW7741-Q1
3.	ISOM8710
4.	SN6507-Q1
5.	AMC1400
Logic & Voltage Translation	
1.	SN74LV4T08-Q1

2.	SN74LV165B-EP
3.	SN74LV8T245
4.	SN74LV8T245-Q1
5.	SN74LV164A-Q1
Motor Drivers	
1.	DRV8962
2.	DRV831BC-Q1
3.	DRV8143-Q1
4.	DRV8411A
5.	MCT8329A
Power Management	
1.	LMR36502
2.	TPS65219
3.	LM2105
4.	TPS61033
5.	TPS61299
Radio Frequency & Microwave ICs	
1.	TRF0206-SP
2.	AFE8000
3.	AFE7952
4.	LMX1204
5.	LMX2571-EP
Sensors	
1.	AWR2944
2.	TMAG5170D-Q1
3.	OPT3005
4.	OPT4048
5.	TMP1826
Switches & Multiplexers	
1.	TMUX4053
2.	TMUX4052

3.	TMUX8211
4.	TMUX8213
5.	TMUXHS221
Wireless Connectivity ICs	
1.	CC266R-Q1
2.	CC2651R3SIPA
3.	CC2652PSIP

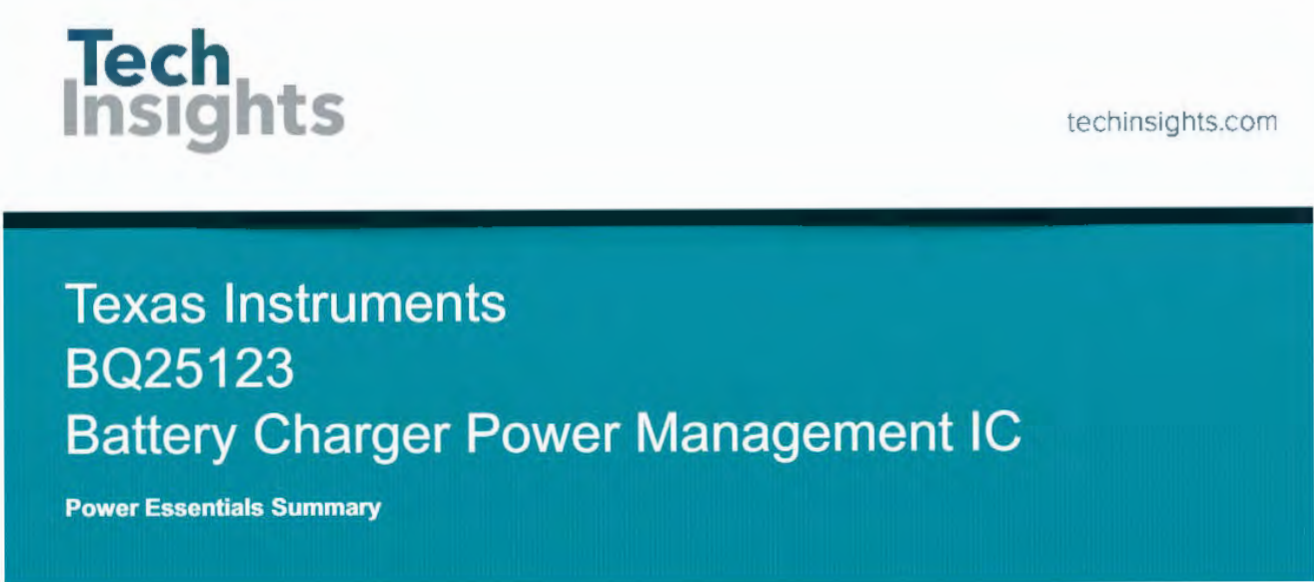
U.S. Patent No. 10,510,842	Accused Products Texas Instruments BQ25123 Battery Charger Power Management IC
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include a semiconductor device. This chart includes exemplary information regarding a representative example of the Texas Instruments Accused Products, the Texas Instruments BQ25123 Battery Charger Power Management IC ("BQ25123"). The BQ25123 was analyzed in the below-referenced report from Tech Insights. The complete report is hereby incorporated by reference into each and every claim and claim element discussed. "Texas Instruments BQ25123 Battery Charger Power Management IC Power Essentials Summary," available at https://library.techinsights.com/search/device-details?tab=reports&id=PEF-2109-802&genealogyCode=TEX-BQ25123YFPT&activeTab=Reports ("BQ25123 Report"). Selected pages are reproduced herein to aid in understanding. The image shows the Tech Insights logo in the top left and the website URL techinsights.com in the top right. Below this is a large blue rectangular area representing the report cover. The cover text reads: "Texas Instruments BQ25123 Battery Charger Power Management IC" in large white font, followed by "Power Essentials Summary" in a smaller white font. BQ25123 Report at Cover. The Texas Instruments BQ25123 is representative of the Texas Instruments Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other Texas Instruments Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '842 patent (and the other asserted patents). For example, the other Texas Instruments Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '842 patent (and the other asserted patents). The claimed invention would have application in numerous types of Texas Instruments products, including, but not limited to, amplifiers, audio processors, digital-to-analog converters, analog-to-digital converters, digital clocks, interface ICs, isolation ICS, microcontrollers and processors, digital

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

signal processors, digital light processors, motor drivers, power management, switches & multiplexers, radio frequency and microwave ICs, wireless connectivity ICs, logic & voltage translation, sensors, and other ICs, because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other Texas Instruments Accused Products contain similar features as the Texas Instruments BQ25123 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other Texas Instruments Accused Products contain similar features as the Texas Instruments BQ25123, and function in a similar way with respect to the features claimed in the asserted claims.

This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery. The Texas Instruments Accused Products, of which Texas Instruments BQ25123 is one example, are semiconductor devices.

Device Summary

- This report presents analysis of the Texas Instruments BQ25123 silicon (Si) based power management IC (PMIC). The BQ25123 is a highly-integrated battery charger PMIC geared for wearable applications and rechargeable toys. It features an integrated buck converter with a low I_{Q} of 700 nA to maximize battery life. supports charge currents from 5 mA to 300 mA, and have I²C interface programmable parameters [3].
- The BQ25123 is PMIC in a 25-ball wafer level chip scale package (WLCS), referred to die scale ball grid array (DSBGA) by Texas Instruments [3].
- The BQ25120 A5B die is about 270 μ m thick and uses bipolar-CMOS-DMOS (BCD) technology. It features two polysilicon layers for transistor and polysilicon-on-polysilicon (POP) capacitor structures, three aluminum (Al) metal layers with titanium nitride (TiN) barrier layers. tungsten (W) contacts and vias, titanium silicide (TiSi) at the source, drain, and polysilicon contact regions, a phosphosilicate glass (SiOP) pre-metal dielectric (PMD), silicon oxide (SiO) intermetal dielectric (IMD), and SiO and silicon nitride (SiN)* passivation. Local oxidation of silicon (LOCOS) is used for isolation. The redistribution layer (RDL) structure is not analyzed. The die utilizes a P-type substrate with an about 16 μ m lighter P-type likely epitaxial layer. The same die is also found in Texas Instruments' BQ25116A.
- Six switching transistor blocks are identified on this device, as shown on page 14. Transistor array Q2 was analyzed and confirmed to be N-channel DMOS with a cell (drain-to-drain) pitch of 5.8 μ m and a channel length of about 0.22 μ m.
- In the power management (PWM) controller region, the minimum observed gate length is 0.38 μ m on a 1.2 μ m pitch, and the minimum observed metal pitch is 0.53 μ m in metal 1. The results are generally consistent with TechInsights' previous analysis of the Texas Instruments' LBC7 0.25 μ m BCD processing technology [4], with a relaxed front end of line (FEOL) geometry.

*Note: The top passivation layer is not analyzed and conclusion is based on industry standard structures.

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BQ25123 Report at 5.

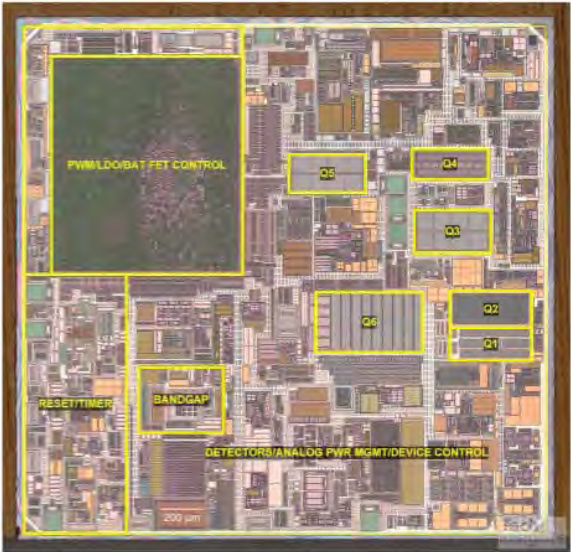
Manufacturer	Texas Instruments
Part number	BQ25123
Foundry	Texas Instruments
Type	PMIC
Date code	88 (likely 2018 August)
Package type	25-ball WLCS
Package markings	T188C6HRI BQ25123
Package dimensions	2.54 mm × 2.47 mm × 0.47 mm (including bumps)
Die markings	<Texas Instruments logo> (M) T1 2014 BQ25120 A5B
Die size (whole die)	2.54 mm × 2.47 mm
Die size (edge seal)	2.48 mm × 2.41 mm
Minimum measured transistor gate/pitch	0.38 μ m/1.2 μ m
Minimum measured metal pitch (M1)	0.53 μ m
Process generation	0.25 μ m
Feature measured to determine process generation	M1 metal pitch, use of TiSi contacts, LOCOS isolation

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Insights

BQ25120_A5B Die Photograph at the Gate Layer

- The die was deprocessed to the polysilicon gate level.
- The die utilization is characterized in the table below.

Functional Description	Length (mm)	Width (mm)	Area (mm ²)	Percentage of Die
Q1 (switching transistor connected between the DC input supply pin [IN] and the high-side bypass connection pin [PMID])	0.15	0.39	0.06	1.0
Q2 (switching transistor connected between the DC input supply pin [IN] and the high-side bypass connection pin [PMID])	0.17	0.39	0.07	1.1
Q3 (switching transistor connected between the high-side bypass connection pin [PMID] and the inductor connection pin [SW])	0.20	0.36	0.07	1.2
Q4 (switching transistor connected between the inductor connection pin [SW] and the PGND pin [PGND])	0.14	0.36	0.05	0.9
Q5 (switching transistor connected between the input to the load switch pin [VINLS] and the load switch/LDO output pin [LDO])	0.18	0.36	0.06	1.1
Q6 (switching transistor connected between the battery connection pin [BAT] and the high-side bypass connection pin [PMID])	0.28	0.50	0.14	2.4
Bandgap bias generator	0.31	0.40	0.12	2.1
Reset/timer block	1.22	0.48	0.59	9.8
Detectors/analog PWR MGMT/device control block	Irregular		3.50	58.5
PWM control/LDO/BAT FET control	1.03	0.90	0.92	15.5
Control I/O	Irregular		0.28	4.6
Others			0.12	1.8
Total die	2.41	2.48	5.98	100.0

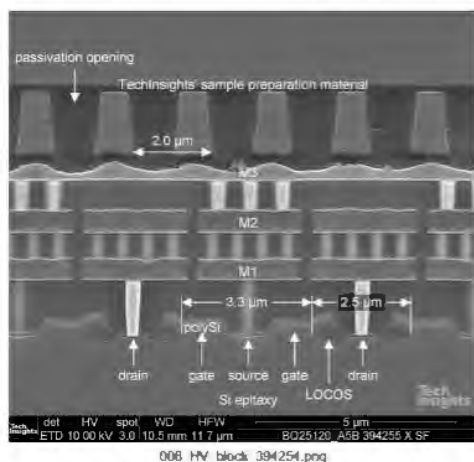


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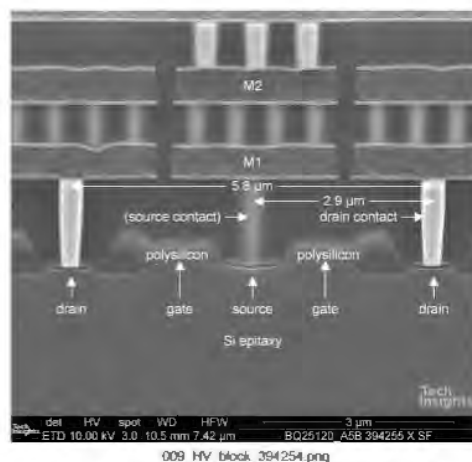
Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

BQ25120_A5B Die Q2 N-LDMOS Array

- The passivation opening pitch for the RDL is 2.0 μm . The RDL is removed in the sample preparation where partial overetch is observed in the metal 3 layer.
- The exposed Si region measures 3.3 μm and the isolation (LOCOS) region, including the central Si for drain contact, measures about 2.5 μm .
- The cell (drain-to-drain) pitch measures about 5.8 μm , and the drain-to-source pitch measures 2.9 μm .



Q2 N-LDMOS Array – SEM Cross Section A-A



Q2 N-LDMOS Array – SEM Cross Section A-A

28

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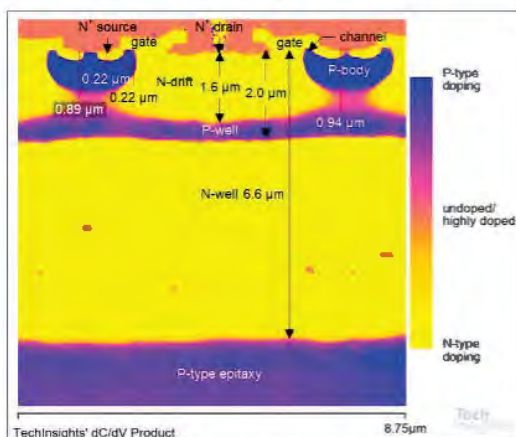
BQ25123 Report at 28.

**Tech
Insights**

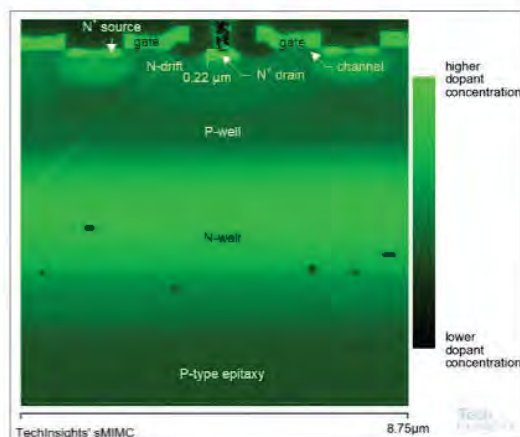
Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

BQ25120_A5B Die Q2 N-LDMOS Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the Q2 N-LDMOS show an N-channel device structure with an about 0.22 μm channel length.
- The N-well, N-drift, and N⁺ source/drain (S/D) depths are about 6.6 μm , 1.6 μm , and 0.22 μm , respectively.
- The P-body depth is nominally about 0.92 μm and the P-well depth is around 2.0 μm .



Q2 N-LDMOS – SCM Cross Section A-A



Q2 N-LDMOS – sMIM-C Cross Section A-A

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BQ25123 Report at 29.

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[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first

The Texas Instruments Accused Products include/comprise a semiconductor device comprising a substrate of a first doping type at a first doping level having first and second surfaces. For example, analysis of an exemplary Texas Instruments Accused Product (the Texas Instruments BQ25123 discussed above) reveals the presence of such a substrate.

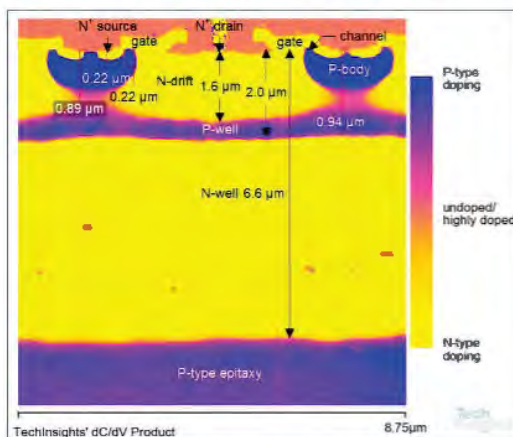
For example, the Texas Instruments BQ25123 discussed above for Claim 1, Preamble, was imaged using scanning electron microscopy (SEM) scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis. The SCM image of the LDMOS array shows a P-type substrate epitaxy having a first doping level, the substrate having a first and second surface.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

and second
surfaces;

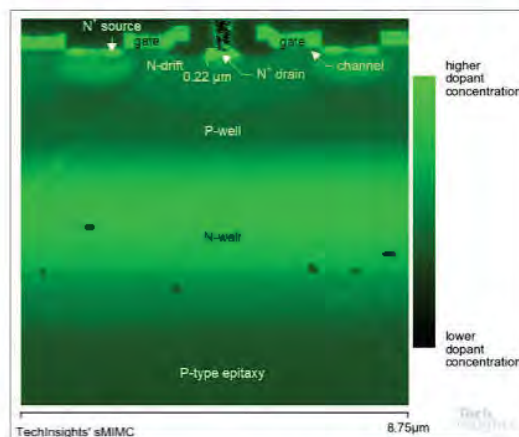
BQ25120_A5B Die Q2 N-LDMOS Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the Q2 N-LDMOS show an N-channel device structure with an about 0.22 μm channel length.
- The N-well, N-drift, and N' source/drain (S/D) depths are about 6.6 μm , 1.6 μm , and 0.22 μm , respectively.
- The P-body depth is nominally about 0.92 μm and the P-well depth is around 2.0 μm .



array_010722135721_PRODUCT_FRW_8.75u_512p_394254.png

Q2 N-LDMOS – SCM Cross Section A-A



array_010722135721_sMIM-CC_FRW_8.75u_512p_394254.png

Q2 N-LDMOS – sMIM-C Cross Section A-A

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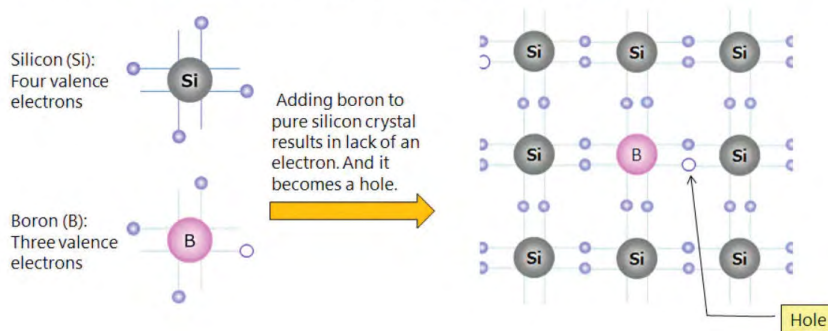
BQ25123 Report at 29.

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Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

What is a p-type Semiconductor?

A p-type semiconductor is an intrinsic semiconductor doped with boron (B) or indium (In). Silicon of Group IV has four valence electrons and boron of Group III has three valence electrons. If a small amount of boron is doped to a single crystal of silicon, valence electrons will be insufficient at one position to bond silicon and boron, resulting in holes* that lack electrons. When a voltage is applied in this state, the neighboring electrons move to the hole, so that the place where an electron is present becomes a new hole, and the holes appear to move to the "+" electrode in sequence.



* This hole is the carrier of a p-type semiconductor.

See

<https://toshiba.semicon-storage.com/us/semiconductor/knowledge/e-learning/discrete/chap1/chap1-4.html#:~:text=A%20p%2Dtype%20semiconductor%20is,III%20has%20three%20valence%20electrons.>

[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type

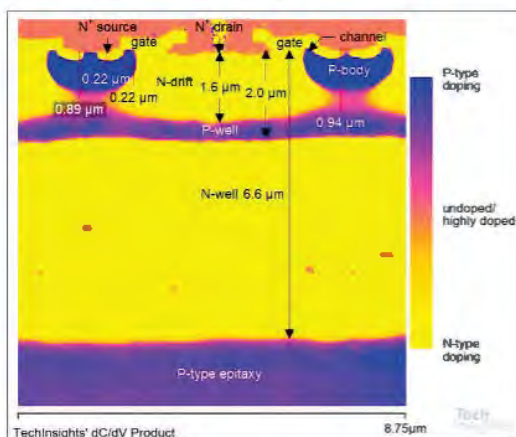
The Texas Instruments Accused Products, and products incorporating them, include/comprise a semiconductor device comprising a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed. For example, as shown in imagery from the Tech Insights Report, the exemplary Texas Instruments BQ25123 scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis includes a first active region disposed adjacent the first surface of the substrate. See below showing "P- and N-Type Regions," where N-wells and P-wells are formed, the N-wells being disposed adjacent the first surface of the substrate with a second doping type (N-type doping) opposite in conductivity to the first doping type (P-type doping) and within which transistors can be formed. Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

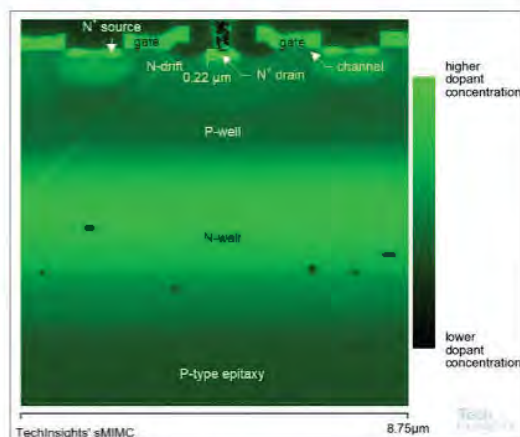
and within which transistors can be formed;

BQ25120_A5B Die Q2 N-LDMOS Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the Q2 N-LDMOS show an N-channel device structure with an about 0.22 μm channel length.
- The N-well, N-drift, and N⁺ source/drain (S/D) depths are about 6.6 μm , 1.6 μm , and 0.22 μm , respectively.
- The P-body depth is nominally about 0.92 μm and the P-well depth is around 2.0 μm .



Q2 N-LDMOS – SCM Cross Section A-A



Q2 N-LDMOS – sMIM-C Cross Section A-A

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BQ25123 Report at 29.

[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to

The Texas Instruments Accused Products include a semiconductor device comprising a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed. For example, the gate, drain, and source annotations reproduced at Claim 1, Element 2 show the active region within which transistors can be formed. Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery.

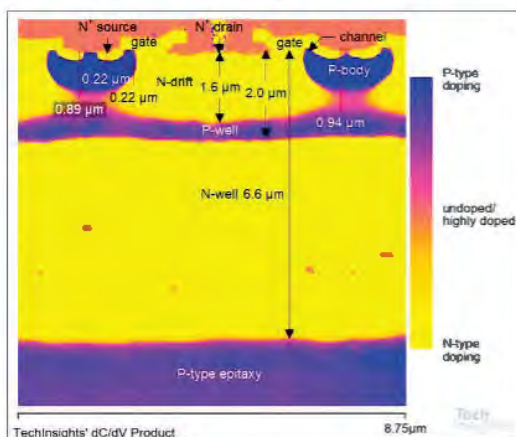
Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

the first active region and within which transistors can be formed;	
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region; and	The Texas Instruments Accused Products include a semiconductor device comprising transistors formed in at least one of the first active region or second active region. <i>See</i> above at the "P- and N-Type Regions" reproduced at Claim 1, Element 2, shows where N-wells and P-wells are formed, and annotated with source, gate, and drain.
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Element 1. For example, this is shown by the SIMS and scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis. SCM/sMIM electrically characterizes the tested device and generates maps which provide graphical representation of the dopant types and concentrations by measuring carrier movement as they are attracted to or repulsed by the probe. The SCM/sMIM maps taken from Texas Instruments Accused Products shown herein demonstrate differences in carrier concentration as a function of depth, which generate electric fields within the accused products. The contrast in the SMIM image is proportional to the capacitance of the sample under inspection, so that brighter green corresponds to higher dopant concentration, and darker green/black corresponds to lower dopant concentration. Likewise, the SCM images above show doping concentration and doping type as indicated in the legends to the right.

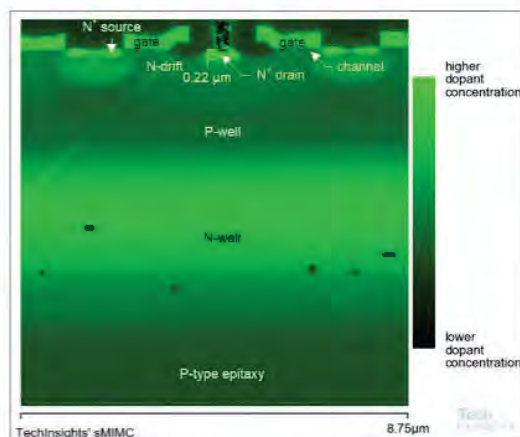
Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

BQ25120_A5B Die Q2 N-LDMOS Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the Q2 N-LDMOS show an N-channel device structure with an about 0.22 μm channel length.
- The N-well, N-drift, and N⁺ source/drain (S/D) depths are about 6.6 μm , 1.6 μm , and 0.22 μm , respectively.
- The P-body depth is nominally about 0.92 μm and the P-well depth is around 2.0 μm .



Q2 N-LDMOS – SCM Cross Section A-A



Q2 N-LDMOS – sMIM-C Cross Section A-A

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BQ25123 Report at 29.

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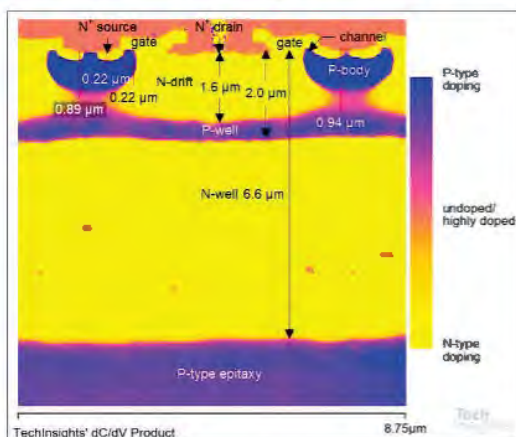
2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.

Upon information and belief, the substrate of the Texas Instruments Accused Products has epitaxial silicon on top of a non-epitaxial substrate. The SCM cross-section image below identifies a P-type epitaxy.

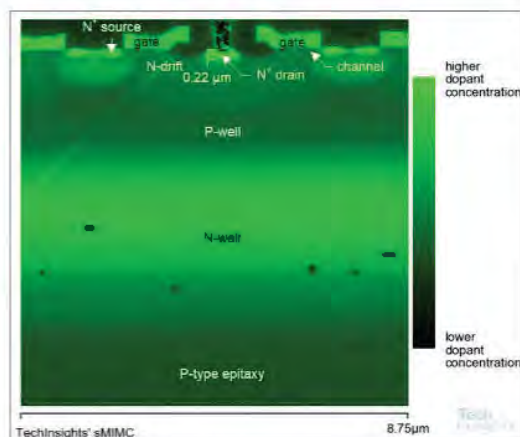
Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

BQ25120_A5B Die Q2 N-LDMOS Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the Q2 N-LDMOS show an N-channel device structure with an about 0.22 μm channel length.
- The N-well, N-drift, and N⁺ source/drain (S/D) depths are about 6.6 μm , 1.6 μm , and 0.22 μm , respectively.
- The P-body depth is nominally about 0.92 μm and the P-well depth is around 2.0 μm .



Q2 N-LDMOS – SCM Cross Section A-A



Q2 N-LDMOS – sMIM-C Cross Section A-A

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4. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a

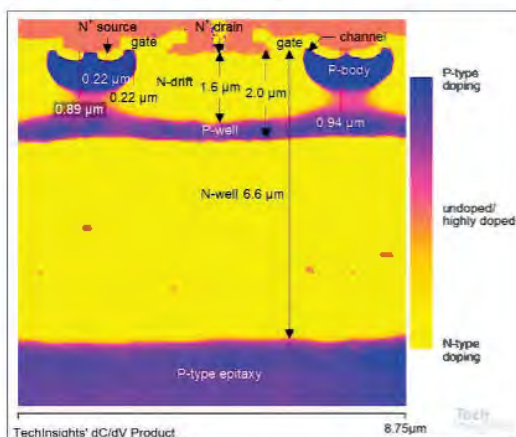
Upon information and belief, the substrate of the Texas Instruments Accused Products has epitaxial silicon on top of a nonepitaxial substrate. The SCM cross-section image below identifies a P-type epitaxy.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

nonepitaxial substrate.

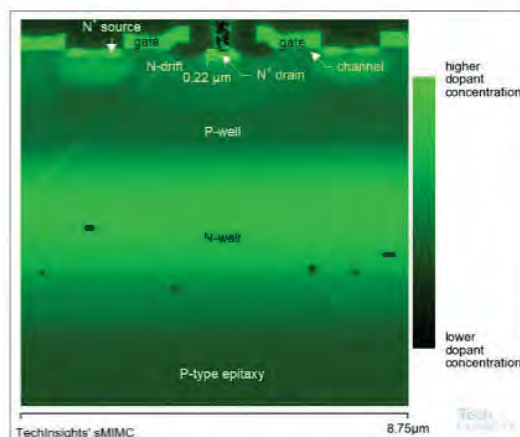
BQ25120_A5B Die Q2 N-LDMOS Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the Q2 N-LDMOS show an N-channel device structure with an about 0.22 μm channel length.
- The N-well, N-drift, and N⁺ source/drain (S/D) depths are about 6.6 μm , 1.6 μm , and 0.22 μm , respectively.
- The P-body depth is nominally about 0.92 μm and the P-well depth is around 2.0 μm .



array_010722135721_PRODUCT_FRW_8.75u_512p_394254.png

Q2 N-LDMOS – SCM Cross Section A-A



array_010722135721_sMIM-CC_FRW_8.75u_512p_394254.png

Q2 N-LDMOS – sMIM-C Cross Section A-A

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BQ25123 Report at 29.

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5. The semiconductor device of claim 1, wherein the first active region and second active region contain

The Texas Instruments Accused Products meet this limitation. As shown above, both N-well and P-wells are used in this device. The first and second active regions accordingly contain p-channel or n-channel devices. See Tech Insights Report images reproduced at Claim 1, Element 2.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

one of either p-channel and n-channel devices.	
6. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	The Texas Instruments Accused Products meet this limitation. As shown above, both N-well and P-wells are used in this device, and the wells include graded dopants. The first and second active regions accordingly contain p-channel or n-channel devices. <i>See</i> Tech Insights Report images reproduced at Claim 1, Element 2.
7. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	Upon information and belief, the substrate of the Texas Instruments Accused Products have isolation regions that separate the first and second active regions. As shown in the Device Summary below, "[l]ocal oxidation of silicon (LOCOS) is used for isolation."

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

Device Summary

- This report presents analysis of the Texas Instruments BQ25123 silicon (Si) based power management IC (PMIC). The BQ25123 is a highly-integrated battery charger PMIC geared for wearable applications and rechargeable toys. It features an integrated buck converter with a low I_{Q} of 700 nA to maximize battery life, supports charge currents from 5 mA to 300 mA, and have I²C interlace programmable parameters [3].
- The BQ25123 is PMIC in a 25-ball wafer level chip scale package (WLCSF), referred to die scale ball grid array (DSBGA) by Texas Instruments [3].
- The BQ25120 A5B die is about 270 μm thick and uses bipolar-CMOS-DMOS (BCD) technology. It features two polysilicon layers for transistor and polysilicon-on-polysilicon (POP) capacitor structures, three aluminum (Al) metal layers with titanium nitride (TiN) barrier layers, tungsten (W) contacts and vias, titanium silicide (TiSi) at the source, drain, and polysilicon contact regions, a phosphosilicate glass (SiOP) pre-metal dielectric (PMD), silicon oxide (SiO) intermetal dielectric (IMD), and SiO and silicon nitride (SiN)* passivation. Local oxidation of silicon (LOCOS) is used for isolation. The redistribution layer (RDL) structure is not analyzed. The die utilizes a P-type substrate with an about 16 μm lighter P-type likely epitaxial layer. The same die is also found in Texas Instruments' BQ25116A.
- Six switching transistor blocks are identified on this device, as shown on page 14. Transistor array Q2 was analyzed and confirmed to be N-channel DMOS with a cell (drain-to-drain) pitch of 5.8 μm and a channel length of about 0.22 μm .
- In the power management (PWM) controller region, the minimum observed gate length is 0.38 μm on a 1.2 μm pitch, and the minimum observed metal pitch is 0.53 μm in metal 1. The results are generally consistent with TechInsights' previous analysis of the Texas Instruments' LBC7 0.25 μm BCD processing technology [4], with a relaxed front end of line (FEOL) geometry.

*Note: The top passivation layer is not analyzed and conclusion is based on industry standard structures.

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BQ25123 Report at 5.

Manufacturer	Texas Instruments
Part number	BQ25123
Foundry	Texas Instruments
Type	PMIC
Date code	88 (likely 2018 August)
Package type	25-ball WLCSF
Package markings	T1 88C6HRI BQ25123
Package dimensions	2.54 mm × 2.47 mm × 0.47 mm (including bumps)
Die markings	<Texas Instruments logo> (M) T1 2014 BQ25120 A5B
Die size (whole die)	2.54 mm × 2.47 mm
Die size (edge seal)	2.48 mm × 2.41 mm
Minimum measured transistor gate/pitch	0.38 μm /1.2 μm
Minimum measured metal pitch (M1)	0.53 μm
Process generation	0.25 μm
Feature measured to determine process generation	M1 metal pitch, use of TiSi contacts, LOCOS isolation

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8. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion

Upon information and belief, the graded dopant is fabricated with an ion implantation process. For example, ion implantation is the prevalent process for implementing doping in semiconductor devices, and is believed to be used for the Texas Instruments Accused Products. Additionally Texas Instruments has multiple patents disclosing ion implantation used in semiconductor fabrication, including U.S. Patent No. 9,064,903 which states that "MOS transistors are generally constructed by way of a counter-doping ion implantation into the channel region...." Because Texas Instruments has patents disclosing this practice, and because it is well known in the art, Texas Instruments Accused Products likely meet this limitation. Information about the fabrication process for the Texas Instruments Accused Products, including usage of an ion implantation process, is in the possession of Defendant and is expected to be obtained through discovery.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

implantation process.	
[Claim 9, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include a semiconductor device. <i>See</i> above at Claim 1, Preamble.
[Claim 9, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1.
[Claim 9, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 2.
[Claim 9, Element 3] a	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 3.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	
[Claim 9, Element 4] transistors formed in at least one of the first active region or second active region; and	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 4.
[Claim 9, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate.	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 5.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

10. The semiconductor device of claim 9, wherein the substrate is a p-type substrate.	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 2.
12. The semiconductor device of claim 9, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 4.
13. The semiconductor device of claim 9, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 5.
14. The semiconductor device of claim 9, wherein the first active region and	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 6.

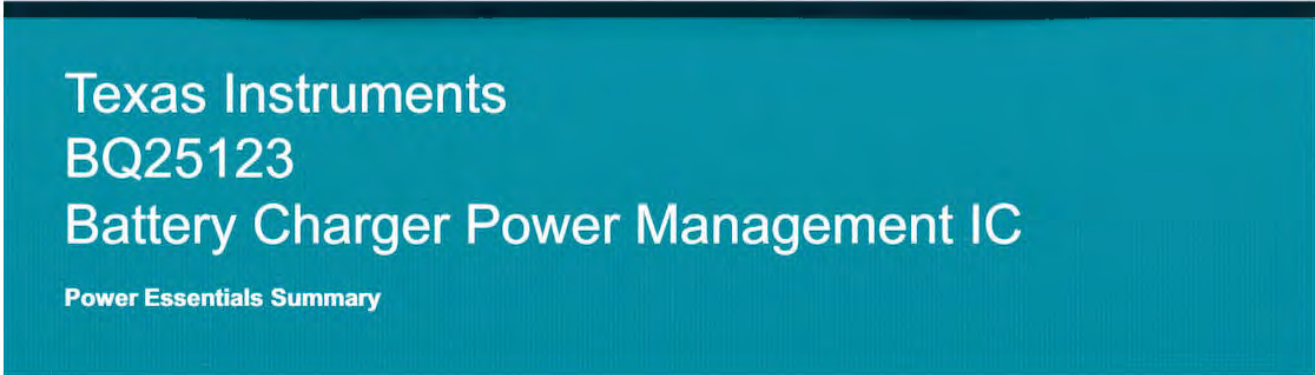
Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	
15. The semiconductor device of claim 9, wherein the first active region and second active region are each separated by at least one isolation region.	Upon information and belief, the Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 7.
16. The semiconductor device of claim 9, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, the Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 8.
17. The semiconductor device of claim 1, wherein the	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 1, Elements 2-3.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

first and second active regions are formed adjacent the first surface of the substrate.	
18. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring a source, a drain, a gate and a channel region.	The Texas Instruments Accused Products meet this limitation. As discussed above for Claim 1, the Texas Instruments Accused Products include first and second active regions. Upon information and belief, CMOS transistors formed in the first and second active regions, the CMOS transistors requiring a source, a drain, a gate, and a channel region. Details regarding transistors used are in the possession of Defendants and are expected to be obtained through discovery.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

U.S. Patent No. 10,734,481	Exemplary Accused Product Texas Instruments BQ25123 Battery Charger Power Management IC
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include a semiconductor device. This chart includes exemplary information regarding a representative example of the Texas Instruments Accused Products, the Texas Instruments BQ25123 Battery Charger Power Management IC ("BQ25123"). The BQ25123 was analyzed in the below-referenced report from Tech Insights. The complete report is hereby incorporated by reference into each and every claim and claim element discussed. "Texas Instruments BQ25123 Battery Charger Power Management IC Power Essentials Summary," available at https://library.techinsights.com/search/device-details?tab=reports&id=PEF-2109-802&genealogyCode=TEX-BQ25123YEPT&activeTab=Reports ("BQ25123 Report"). Selected pages are reproduced herein to aid in understanding.    BQ25123 Report at Cover. The Texas Instruments BQ25123 is representative of the Texas Instruments Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other Texas Instruments Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '481 patent (and the other asserted patents). For example, the other Texas Instruments Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '481 patent (and the other asserted patents). The claimed invention would have application in numerous types of Texas Instruments products, including, but not limited to, amplifiers, audio processors, digital-to-analog converters, analog-to-digital converters, digital clocks, interface ICs, isolation ICS, microcontrollers and

Page 1

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

processors, digital signal processors, digital light processors, motor drivers, power management, switches & multiplexers, radio frequency and microwave ICs, wireless connectivity ICs, logic & voltage translation, sensors, and other ICs, because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other Texas Instruments Accused Products contain similar features as the Texas Instruments BQ25123 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other Texas Instruments Accused Products contain similar features as the Texas Instruments BQ25123, and function in a similar way with respect to the features claimed in the asserted claims.

This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery. The Texas Instruments Accused Products, of which Texas Instruments BQ25123 is one example, are semiconductor devices.

Device Summary

- This report presents analysis of the Texas Instruments BQ25123 silicon (Si) based power management IC (PMIC). The BQ25123 is a highly-integrated battery charger PMIC geared for wearable applications and rechargeable toys. It features an integrated buck converter with a low I_{Q} of 700 nA to maximize battery life, supports charge currents from 5 mA to 300 mA, and have I²C interlace programmable parameters [3].
- The BQ25123 is PMIC in a 25-ball wafer level chip scale package (WLCSP), referred to die scale ball grid array (DSBGA) by Texas Instruments [3].
- The BQ25120_A5B die is about 270 μm thick and uses bipolar-CMOS-DMOS (BCD) technology. It features two polysilicon layers for transistor and polysilicon-on-polysilicon (POP) capacitor structures, three aluminum (Al) metal layers with titanium nitride (TiN) barrier layers, tungsten (W) contacts and vias, titanium silicide (TiSi) at the source, drain, and polysilicon contact regions, a phosphosilicate glass (SiOP) pre-metal dielectric (PMD), silicon oxide (SiO₂) intermetal dielectric (IMD), and SiO₂ and silicon nitride (SiN)_x passivation. Local oxidation of silicon (LOCOS) is used for isolation. The redistribution layer (RDL) structure is not analyzed. The die utilizes a P-type substrate with an about 16 μm lighter P-type likely epitaxial layer. The same die is also found in Texas Instruments' BQ25116A.
- Six switching transistor blocks are identified on this device, as shown on page 14. Transistor array Q2 was analyzed and confirmed to be N-channel DMOS with a cell (drain-to-drain) pitch of 5.8 μm and a channel length of about 0.22 μm .
- In the power management (PWM) controller region, the minimum observed gate length is 0.38 μm on a 1.2 μm pitch, and the minimum observed metal pitch is 0.53 μm in metal 1. The results are generally consistent with TechInsights' previous analysis of the Texas Instruments' LBC7 0.25 μm BCD processing technology [4], with a relaxed front end of line (FEOL) geometry.

*Note: The top passivation layer is not analyzed and conclusion is based on industry standard structures.

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BQ25123 Report at 5.

Manufacturer	Texas Instruments
Part number	BQ25123
Foundry	Texas Instruments
Type	PMIC
Date code	88 (likely 2018 August)
Package type	25-ball WLCSP
Package markings	TI 88C6HRI BQ25123
Package dimensions	2.54 mm × 2.47 mm × 0.47 mm (including bumps)
Die markings	<Texas Instruments logo> (M) TI 2014 BQ25120 A5B
Die size (whole die)	2.54 mm × 2.47 mm
Die size (edge seal)	2.48 mm × 2.41 mm
Minimum measured transistor gate/pitch	0.38 μm /1.2 μm
Minimum measured metal pitch (M1)	0.53 μm
Process generation	0.25 μm
Feature measured to determine process generation	M1 metal pitch, use of TiSi contacts, LOCOS isolation

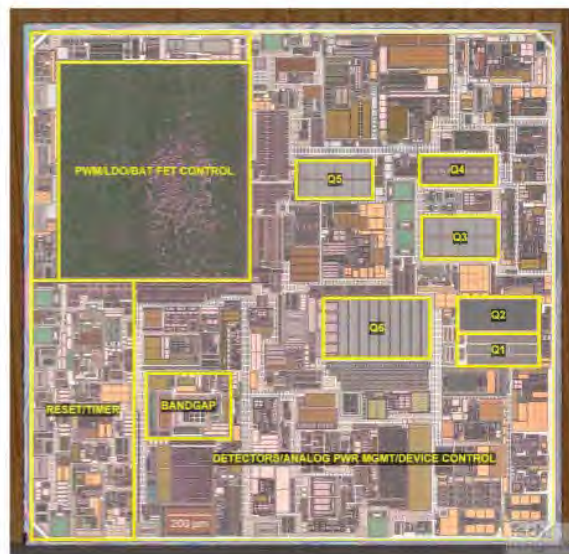
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Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

BQ25120_A5B Die Photograph at the Gate Layer

- The die was deprocessed to the polysilicon gate level.
- The die utilization is characterized in the table below.

Functional Description	Length (mm)	Width (mm)	Area (mm ²)	Percentage of Die
Q1 (switching transistor connected between the DC input supply pin [IN] and the high-side bypass connection pin [PMID])	0.15	0.39	0.06	1.0
Q2 (switching transistor connected between the DC input supply pin [IN] and the high-side bypass connection pin [PMID])	0.17	0.39	0.07	1.1
Q3 (switching transistor connected between the high-side bypass connection pin [PMID] and the inductor connection pin [SW])	0.20	0.36	0.07	1.2
Q4 (switching transistor connected between the inductor connection pin [SW] and the PGND pin [PGND])	0.14	0.36	0.05	0.9
Q5 (switching transistor connected between the input to the load switch pin [VINLS] and the load switch/LDO output pin [LDO])	0.18	0.36	0.06	1.1
Q6 (switching transistor connected between the battery connection pin [BAT] and the high-side bypass connection pin [PMID])	0.28	0.50	0.14	2.4
Bandgap bias generator	0.31	0.40	0.12	2.1
Reset/timer block	1.22	0.48	0.59	9.8
Detectors/analog PWR MGMT/device control block	Irregular		3.50	58.5
PWM control/LDO/BAT FET control	1.03	0.90	0.92	15.5
Control I/O	Irregular		0.28	4.6
Others			0.12	1.8
Total die	2.41	2.48	5.98	100.0



BQ25123YFPT_BQ25120_BPoly_blocks.png

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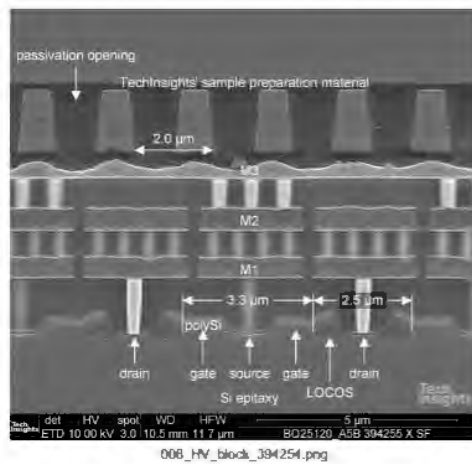
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BQ25123 Report at 14.

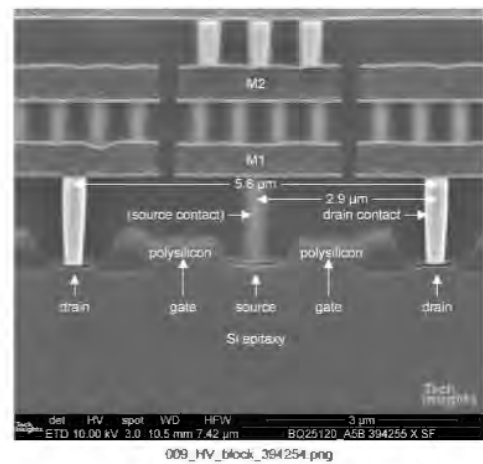
Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

BQ25120_A5B Die Q2 N-LDMOS Array

- The passivation opening pitch for the RDL is 2.0 μm . The RDL is removed in the sample preparation where partial overetch is observed in the metal 3 layer.
- The exposed Si region measures 3.3 μm and the isolation (LOCOS) region, including the central Si for drain contact, measures about 2.5 μm .
- The cell (drain-to-drain) pitch measures about 5.8 μm , and the drain-to-source pitch measures 2.9 μm .



Q2 N-LDMOS Array – SEM Cross Section A-A



Q2 N-LDMOS Array – SEM Cross Section A-A

28

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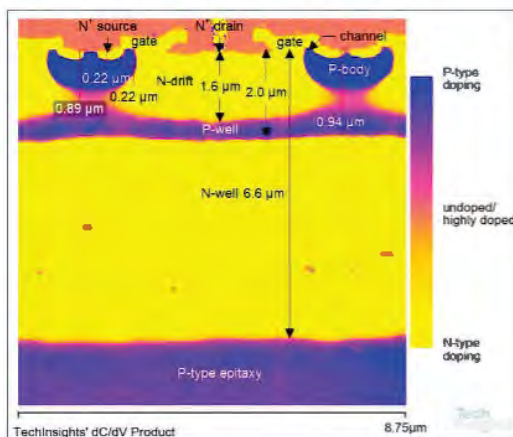
BQ25123 Report at 28.

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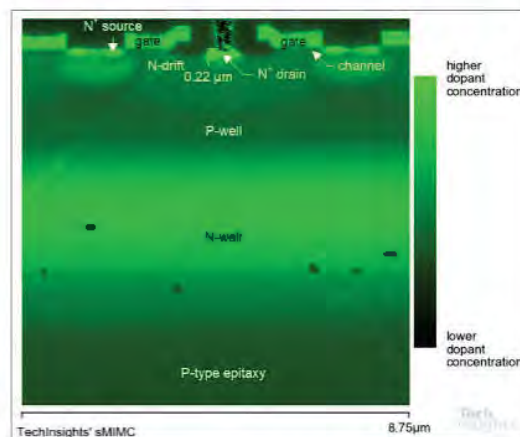
Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

BQ25120_A5B Die Q2 N-LDMOS Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the Q2 N-LDMOS show an N-channel device structure with an about 0.22 μm channel length.
- The N-well, N-drift, and N' source/drain (S/D) depths are about 6.6 μm , 1.6 μm , and 0.22 μm , respectively.
- The P-body depth is nominally about 0.92 μm and the P-well depth is around 2.0 μm .



Q2 N-LDMOS – SCM Cross Section A-A



Q2 N-LDMOS – sMIM-C Cross Section A-A

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BQ25123 Report at 29.

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[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first

The Texas Instruments Accused Products include/comprise a semiconductor device comprising a substrate of a first doping type at a first doping level having first and second surfaces. For example, analysis of an exemplary Texas Instruments Accused Product (the Texas Instruments BQ25123 discussed above) reveals the presence of such a substrate.

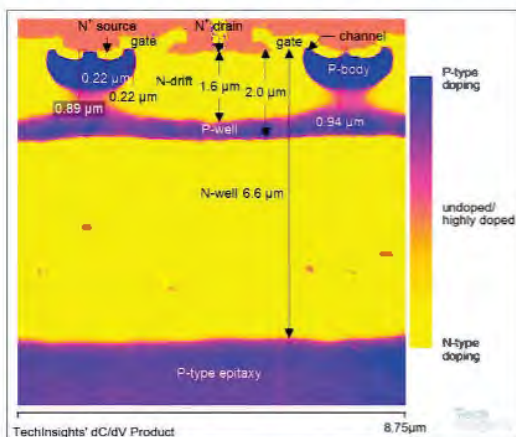
For example, the Texas Instruments BQ25123 discussed above for Claim 1, Preamble, was imaged using scanning electron microscopy (SEM) scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis. The SCM image of the LDMOS array shows a P-type substrate epitaxy having a first doping level, the substrate having a first and second surface.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

and second
surfaces;

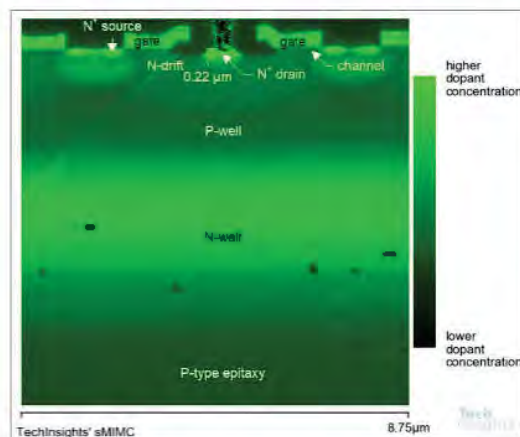
BQ25120_A5B Die Q2 N-LDMOS Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the Q2 N-LDMOS show an N-channel device structure with an about 0.22 μm channel length.
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- The P-body depth is nominally about 0.92 μm and the P-well depth is around 2.0 μm .



array_010722135721_PRODUCT_FRW_8.75u_512p_394254.png

Q2 N-LDMOS – SCM Cross Section A-A



array_010722135721_sMIM-CC_FRW_8.75u_512p_394254.png

Q2 N-LDMOS – sMIM-C Cross Section A-A

29

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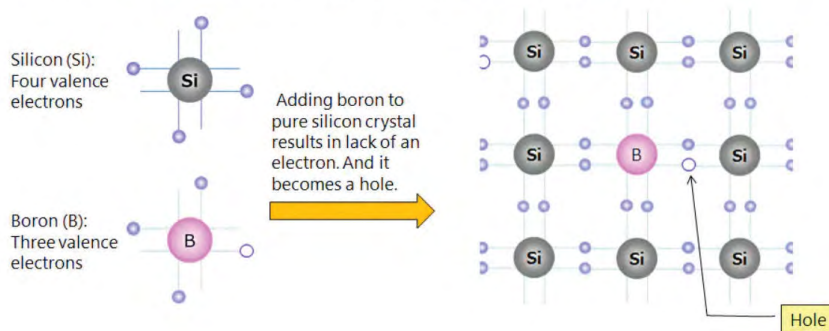
BQ25123 Report at 29.

Tech
Insights

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

What is a p-type Semiconductor?

A p-type semiconductor is an intrinsic semiconductor doped with boron (B) or indium (In). Silicon of Group IV has four valence electrons and boron of Group III has three valence electrons. If a small amount of boron is doped to a single crystal of silicon, valence electrons will be insufficient at one position to bond silicon and boron, resulting in holes* that lack electrons. When a voltage is applied in this state, the neighboring electrons move to the hole, so that the place where an electron is present becomes a new hole, and the holes appear to move to the "-" electrode in sequence.



* This hole is the carrier of a p-type semiconductor.

See

<https://toshiba.semicon-storage.com/us/semiconductor/knowledge/e-learning/discrete/chap1/chap1-4.html#:~:text=A%20p%2Dtype%20semiconductor%20is,III%20has%20three%20valence%20electrons.>

[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which

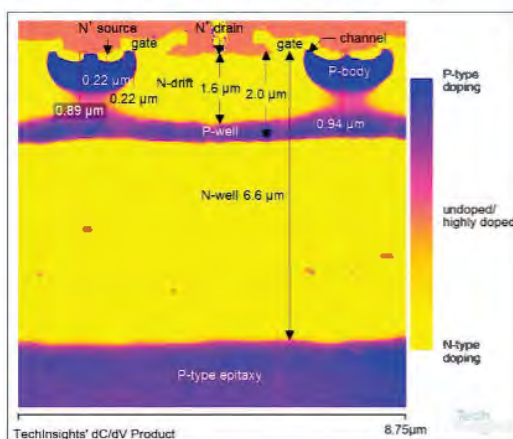
The Texas Instruments Accused Products, and products incorporating them, include/comprise a semiconductor device comprising a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed. For example, as shown in imagery from the Tech Insights Report, the exemplary Texas Instruments BQ25123 scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis includes a first active region disposed adjacent the first surface of the substrate. See below showing "P- and N-Type Regions," where N-wells and P-wells are formed, the N-wells being disposed adjacent the first surface of the substrate with a second doping type (N-type doping) opposite in conductivity to the first doping type (P-type doping) and within which transistors can be formed. Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

transistors can be formed;

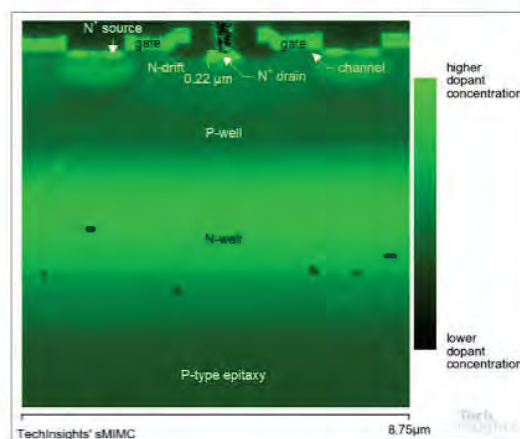
BQ25120_A5B Die Q2 N-LDMOS Array – P- and N-Type Regions

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- The P-body depth is nominally about 0.92 μm and the P-well depth is around 2.0 μm .



array_010722135721_PRODUCT_FRW_8.75u_512p_394254.png

Q2 N-LDMOS – SCM Cross Section A-A



array_010722135721_sMIM-CC_FRW_8.75u_512p_394254.png

Q2 N-LDMOS – sMIM-C Cross Section A-A

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BQ25123 Report at 29.

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[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active

The Texas Instruments Accused Products include a semiconductor device comprising a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed. For example, the gate, drain, and source annotations reproduced at Claim 1, Element 2 show the active region within which transistors can be formed. Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery.

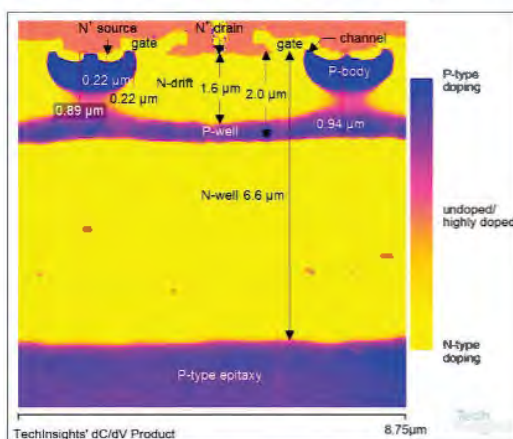
Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

region and within which transistors can be formed;	
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region;	The Texas Instruments Accused Products include a semiconductor device comprising transistors formed in at least one of the first active region or second active region. <i>See</i> above at the "P- and N-Type Regions" reproduced at Claim 1, Element 2, shows where N-wells and P-wells are formed, and annotated with source, gate, and drain.
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Element 1. For example, this is shown by the SIMS and scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis. SCM/sMIM electrically characterizes the tested device and generates maps which provide graphical representation of the dopant types and concentrations by measuring carrier movement as they are attracted to or repulsed by the probe. The SCM/sMIM maps taken from Texas Instruments Accused Products shown herein demonstrate differences in carrier concentration as a function of depth, which generate electric fields within the accused products. The contrast in the SMIM image is proportional to the capacitance of the sample under inspection, so that brighter green corresponds to higher dopant concentration, and darker green/black corresponds to lower dopant concentration. Likewise, the SCM images above show doping concentration and doping type as indicated in the legends to the right.

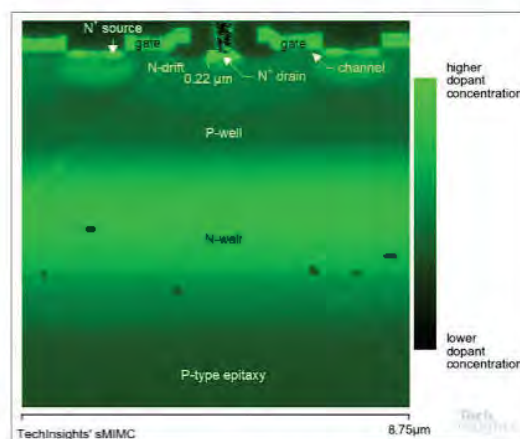
Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

BQ25120_A5B Die Q2 N-LDMOS Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the Q2 N-LDMOS show an N-channel device structure with an about 0.22 μm channel length.
- The N-well, N-drift, and N' source/drain (S/D) depths are about 6.6 μm , 1.6 μm , and 0.22 μm , respectively.
- The P-body depth is nominally about 0.92 μm and the P-well depth is around 2.0 μm .



Q2 N-LDMOS – SCM Cross Section A-A



Q2 N-LDMOS – sMIM-C Cross Section A-A

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BQ25123 Report at 29.

[Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one

The Texas Instruments Accused Products meet this limitation. *See* above at Element 1. For example, this is shown by the SIMS and scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis. SCM/sMIM electrically characterizes the tested device and generates maps which provide graphical representation of the dopant types and concentrations by measuring carrier movement as they are attracted to or repulsed by the probe. The SCM/sMIM maps taken from Texas Instruments Accused Products shown herein demonstrate differences in carrier concentration as a function of depth, which generate electric fields within the accused products. The contrast in the SMIM image is proportional to the capacitance of the sample under inspection, so that brighter green corresponds to higher dopant concentration, and darker green/black corresponds to lower dopant concentration. Likewise, the SCM images above show doping concentration and doping type as indicated in the legends to the right. The image below shows vertical dopant grading in a well

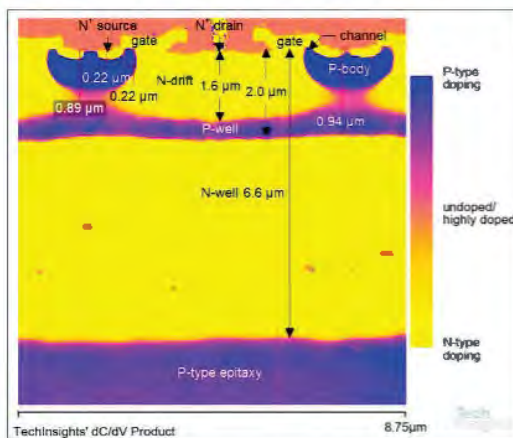
Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.

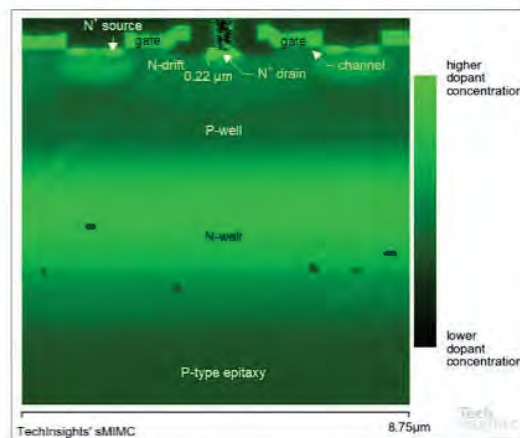
region adjacent (N-well and P-well) to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.

BQ25120_A5B Die Q2 N-LDMOS Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the Q2 N-LDMOS show an N-channel device structure with an about 0.22 μm channel length.
- The N-well, N-drift, and N⁺ source/drain (S/D) depths are about 6.6 μm , 1.6 μm , and 0.22 μm , respectively.
- The P-body depth is nominally about 0.92 μm and the P-well depth is around 2.0 μm .



Q2 N-LDMOS – SCM Cross Section A-A



Q2 N-LDMOS – sMIM-C Cross Section A-A

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BQ25123 Report at 29.

2. The semiconductor device of claim 1, wherein the substrate is a

Upon information and belief, the Texas Instruments Accused Products meet this limitation. The SCM cross-section image below identifies a P-type epitaxy.

BQ25120_A5B Die Q2 N-LDMOS Array – P- and N-Type Regions

-
- 0.22 μm 0.22 μm 0.89 μm 0.94 μm 1.6 μm 2.0 μm 6.6 μm 8.75 μm
- N⁺ source gate N⁺ drain gate channel P-body P-well N-well P-type epitaxy
- P-type doping undoped/highly doped N-type doping
- Techn Insights' d/CV Product

N⁺ source gate N-drift 0.22 μm N⁺ drain channel

P-well

N-well

P-type epitaxy

higher dopant concentration

lower dopant concentration

TechInsights' sMIMC 8.75μm

Q2 N-LDMOS – sMIM-C Cross Section A-A

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3. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a

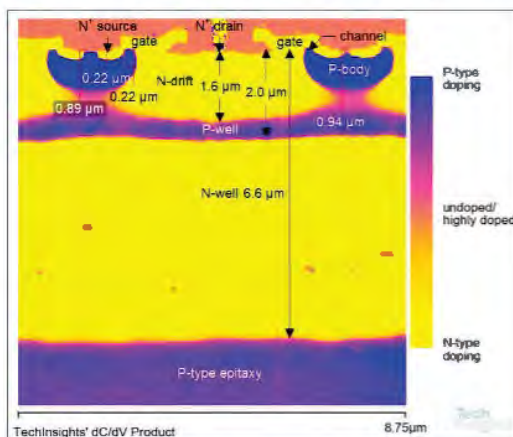
Upon information and belief, the substrate of the Texas Instruments Accused Products has epitaxial silicon on top of a nonepitaxial substrate. The SCM cross-section image below identifies a P-type epitaxy.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

nonepitaxial
substrate.

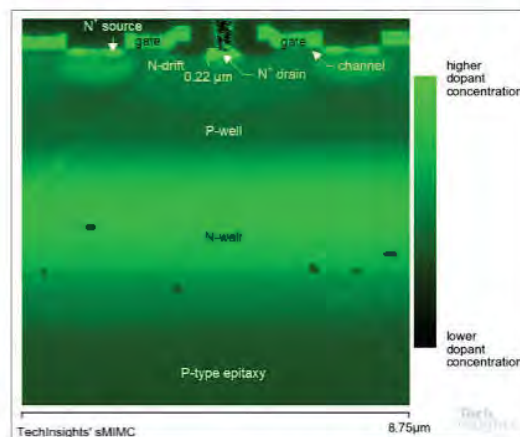
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- SCM and sMIM-C analysis of the Q2 N-LDMOS show an N-channel device structure with an about 0.22 μm channel length.
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array_010722135721_PRODUCT_FRW_8.75u_512p_394254.png

Q2 N-LDMOS – SCM Cross Section A-A



array_010722135721_sMIM-CC_FRW_8.75u_512p_394254.png

Q2 N-LDMOS – sMIM-C Cross Section A-A

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BQ25123 Report at 29.

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4. The semiconductor device of claim 1, wherein the first active region and second active region contain

The Texas Instruments Accused Products meet this limitation. As shown above, both N-well and P-wells are used in this device. The first and second active regions accordingly contain p-channel or n-channel devices. See Tech Insights Report images reproduced at Claim 1, Element 2.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

one of either p-channel and n-channel devices.	
5. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	The Texas Instruments Accused Products meet this limitation. As shown above, both N-well and P-wells are used in this device, and the wells include graded dopants. The first and second active regions accordingly contain p-channel or n-channel devices. <i>See</i> Tech Insights Report images reproduced at Claim 1, Element 2.
6. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	Upon information and belief, the substrate of the Texas Instruments Accused Products have isolation regions that separate the first and second active regions. As shown in the Device Summary below, "[l]ocal oxidation of silicon (LOCOS) is used for isolation."

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

Device Summary

- This report presents analysis of the Texas Instruments BQ25123 silicon (Si) based power management IC (PMIC). The BQ25123 is a highly-integrated battery charger PMIC geared for wearable applications and rechargeable toys. It features an integrated buck converter with a low I_{LD} of 700 nA to maximize battery life, supports charge currents from 5 mA to 300 mA, and have I²C interlace programmable parameters [3].
- The BQ25123 is PMIC in a 25-ball wafer level chip scale package (WLCSP), referred to die scale ball grid array (DSBGA) by Texas Instruments [3].
- The BQ25120_A5B die is about 270 μ m thick and uses bipolar-CMOS-DMOS (BCD) technology. It features two polysilicon layers for transistor and polysilicon-on-polysilicon (POP) capacitor structures, three aluminum (Al) metal layers with titanium nitride (TiN) barrier layers, tungsten (W) contacts and vias, titanium silicide (TiSi) at the source, drain, and polysilicon contact regions, a phosphosilicate glass (SiOP) pre-metal dielectric (PMD), silicon oxide (SiO₂) intermetal dielectric (IMD), and SiO₂ and silicon nitride (SiN_x) passivation. Local oxidation of silicon (LOCOS) is used for isolation. The redistribution layer (RDL) structure is not analyzed. The die utilizes a P-type substrate with an about 16 μ m lighter P-type likely epitaxial layer. The same die is also found in Texas Instruments' BQ25116A.
- Six switching transistor blocks are identified on this device, as shown on page 14. Transistor array Q2 was analyzed and confirmed to be N-channel DMOS with a cell (drain-to-drain) pitch of 5.8 μ m and a channel length of about 0.22 μ m.
- In the power management (PWM) controller region, the minimum observed gate length is 0.38 μ m on a 1.2 μ m pitch, and the minimum observed metal pitch is 0.53 μ m in metal 1. The results are generally consistent with TechInsights' previous analysis of the Texas Instruments' LBC7 0.25 μ m BCD processing technology [4], with a relaxed front end of line (FEOL) geometry.

*Note: The top passivation layer is not analyzed and conclusion is based on industry standard structures.

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BQ25123 Report at 5.

Manufacturer	Texas Instruments
Part number	BQ25123
Foundry	Texas Instruments
Type	PMIC
Date code	88 (likely 2018 August)
Package type	25-ball WLCSP
Package markings	TI 88C6HRI BQ25123
Package dimensions	2.54 mm × 2.47 mm × 0.47 mm (including bumps)
Die markings	<Texas Instruments logo> (M) TI 2014 BQ25120 A5B
Die size (whole die)	2.54 mm × 2.47 mm
Die size (edge seal)	2.48 mm × 2.41 mm
Minimum measured transistor gate/pitch	0.38 μ m/1.2 μ m
Minimum measured metal pitch (M1)	0.53 μ m
Process generation	0.25 μ m
Feature measured to determine process generation	M1 metal pitch, use of TiSi contacts, LOCOS isolation

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7. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion

Upon information and belief, the graded dopant is fabricated with an ion implantation process. For example, ion implantation is the prevalent process for implementing doping in semiconductor devices, and is believed to be used for the Texas Instruments Accused Products. Additionally Texas Instruments has multiple patents disclosing ion implantation used in semiconductor fabrication, including U.S. Patent No. 9,064,903 which states that "MOS transistors are generally constructed by way of a counter-doping ion implantation into the channel region...." Because Texas Instruments has patents disclosing this practice, and because it is well known in the art, Texas Instruments Accused Products likely meet this limitation. Information about the fabrication process for the Texas Instruments Accused Products, including usage of an ion implantation process, is in the possession of Defendant and is expected to be obtained through discovery.

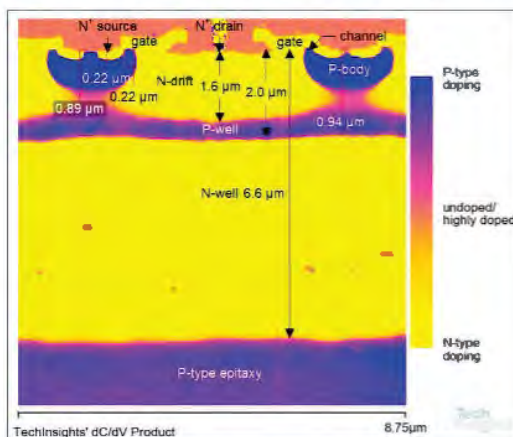
Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

implantation process.	
8. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 1, Elements 1-3.
9. The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Texas Instruments Accused Products meet this limitation. The SIMS image below indicates graded dopant regions in the first active region or the second active region that are both p-type and n-type.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

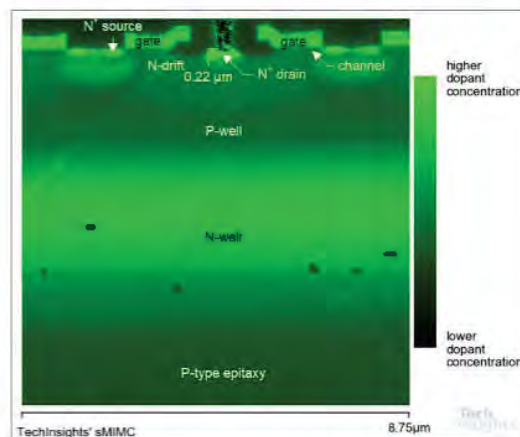
BQ25120_A5B Die Q2 N-LDMOS Array – P- and N-Type Regions

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array_010722135721_PRODUCT_FRW_8.75u_512p_394254.png

Q2 N-LDMOS – SCM Cross Section A-A



array_010722135721_sMIM-CC_FRW_8.75u_512p_394254.png

Q2 N-LDMOS – sMIM-C Cross Section A-A

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BQ25123 Report at 29.

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12. The semiconductor device of claim 1, wherein dopants of the graded dopant region in the well region are

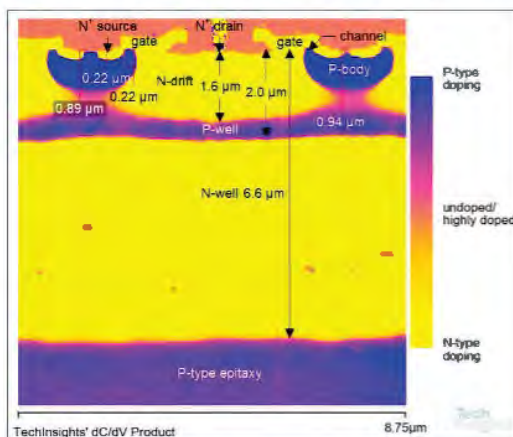
The Texas Instruments Accused Products meet this limitation. The SCM image below indicates graded dopant regions in well regions that are both p-type and n-type.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

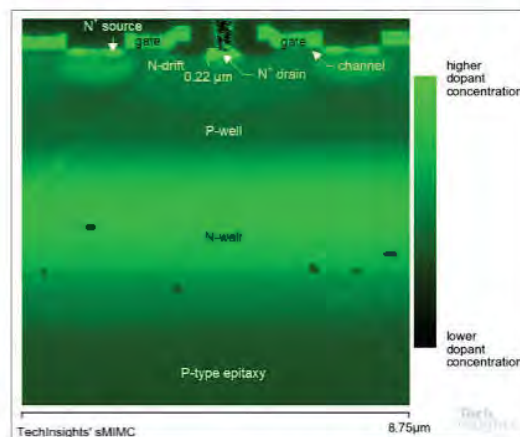
both p-type
and n-type.

BQ25120_A5B Die Q2 N-LDMOS Array – P- and N-Type Regions

- SCM and sMIM-C analysis of the Q2 N-LDMOS show an N-channel device structure with an about 0.22 μm channel length.
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Q2 N-LDMOS – SCM Cross Section A-A



Q2 N-LDMOS – sMIM-C Cross Section A-A

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BQ25123 Report at 29.

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13. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and

The Texas Instruments Accused Products meet this limitation. As discussed above for Claim 1, the Texas Instruments Accused Products include first and second active regions. Upon information and belief, CMOS transistors formed in the first and second active regions, the CMOS transistors requiring a source, a drain, a gate, and a channel region. Details regarding transistors used are in the possession of Defendants and are expected to be obtained through discovery.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

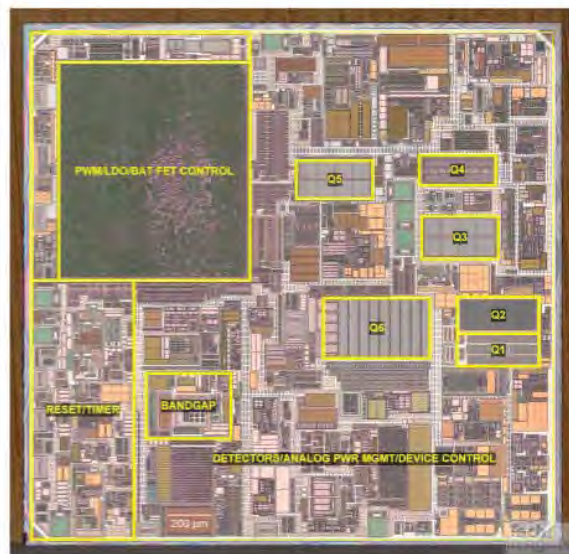
second active regions are CMOS transistors requiring at least a source, a drain, a gate and a channel.	
15. The semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Claims 3 (regarding nonepitaxial substrate), 13 (regarding CMOS).
17. The semiconductor device of claim 1, wherein the device is a logic device.	The Texas Instruments Accused Products meet this limitation. As shown in the block diagram of the figure below, the BQ25123 includes a power management and device control region which constitutes a logic device.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

BQ25120_A5B Die Photograph at the Gate Layer

- The die was deprocessed to the polysilicon gate level.
- The die utilization is characterized in the table below.

Functional Description	Length (mm)	Width (mm)	Area (mm ²)	Percentage of Die
Q1 (switching transistor connected between the DC input supply pin [IN] and the high-side bypass connection pin [PMID])	0.15	0.39	0.06	1.0
Q2 (switching transistor connected between the DC input supply pin [IN] and the high-side bypass connection pin [PMID])	0.17	0.39	0.07	1.1
Q3 (switching transistor connected between the high-side bypass connection pin [PMID] and the inductor connection pin [SW])	0.20	0.36	0.07	1.2
Q4 (switching transistor connected between the inductor connection pin [SW] and the PGND pin [PGND])	0.14	0.36	0.05	0.9
Q5 (switching transistor connected between the input to the load switch pin [VINLS] and the load switch/LDO output pin [LDO])	0.18	0.36	0.06	1.1
Q6 (switching transistor connected between the battery connection pin [BAT] and the high-side bypass connection pin [PMID])	0.28	0.50	0.14	2.4
Bandgap bias generator	0.31	0.40	0.12	2.1
Reset/timer block	1.22	0.48	0.59	9.8
Detectors/analog PWR MGMT/device control block	Irregular		3.50	58.5
PWM control/LDO/BAT FET control	1.03	0.90	0.92	15.5
Control I/O	Irregular		0.28	4.6
Others			0.12	1.8
Total die	2.41	2.48	5.98	100.0



BQ25123YFPT_BQ25120_BPoly_blocks.png

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BQ25123 Report at 14.

18. The semiconductor device of claim 17, wherein the device is central processing unit.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

[Claim 20, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include/comprise a semiconductor device. <i>See</i> above at Claim 1, Preamble.
[Claim 20, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The Texas Instruments Accused Products meet this limitation. <i>See</i> Claim 1, Element 1.
[Claim 20, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Texas Instruments Accused Products meet this limitation. <i>See</i> Claim 1, Element 2. Upon information and belief, transistors can be formed in the surface of the first active region. Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery.
[Claim 20, Element 3] a second active region separate from the first active region disposed	The Texas Instruments Accused Products meet this limitation. <i>See</i> Claim 1, Element 3. Upon information and belief, transistors can be formed in the surface of the first active region. Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

adjacent to the first active region and within which transistors can be formed in the surface thereof;	
[Claim 20, Element 4] transistors formed in at least one of the first active region or second active region;	The Texas Instruments Accused Products meet this limitation. <i>See</i> Claim 1, Element 4.
[Claim 20, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate; and	The Texas Instruments Accused Products meet this limitation. <i>See</i> Claim 1, Element 5.
[Claim 20, Element 6] at least one well region adjacent to the first or second active region containing at least one	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 6.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.	
22. The semiconductor device of claim 20, wherein the substrate is a p-type substrate.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Claim 2.
23. The semiconductor device of claim 20, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Claim 3.
24. The semiconductor device of claim 20, wherein the first active region and second active region contain at least one of either p-	The Texas Instruments Accused Products meet this limitation. <i>See</i> Claim 4.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

channel and n-channel devices.	
25. The semiconductor device of claim 20, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Claim 5.
26. The semiconductor device of claim 20, wherein the first active region and second active region are each separated by at least one isolation region.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Claim 6.
27. The semiconductor device of claim 20, wherein dopants of the	The Texas Instruments Accused Products meet this limitation. <i>See</i> Claim 9.

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

graded dopant concentration in the first active region or the second active region are either p-type or n-type.	
31. The semiconductor device of claim 20, wherein the graded dopant is fabricated with an ion implantation process.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Claim 7.
32. The semiconductor device of claim 20, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Claim 13.
34. The semiconductor device of claim 20, wherein the device is a logic device.	The Texas Instruments Accused Products meet this limitation. <i>See</i> above, Claim 17.
~~35. The semiconductor device of~~	

Exhibit A-2 to Greenthread's Complaint (U.S. Patent No. 10,734,481)

claim 34, wherein the device is central processing unit.	
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Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
[Claim 1, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include a VLSI semiconductor device. The Texas Instruments BQ25123 Battery Charger Power Management IC ("BQ25123") discussed for claim 1 of Exhibit A-1 is a semiconductor device (<i>see</i> Exhibit A-1, Claim 1, Preamble) with transistors, and is a VLSI semiconductor device upon information and belief. Details regarding transistor count are in the possession of the Defendants and are expected to be obtained through discovery. The Texas Instruments BQ25123 is representative of the Texas Instruments Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other Texas Instruments Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '222 patent (and the other asserted patents). For example, the other Texas Instruments Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '222 patent (and the other asserted patents). The claimed invention would have application in numerous types of Texas Instruments products, including, but not limited to, amplifiers, audio processors, digital-to-analog converters, analog-to-digital converters, digital clocks, interface ICs, isolation ICS, microcontrollers and processors, digital signal processors, digital light processors, motor drivers, power management, switches & multiplexers, radio frequency and microwave ICs, wireless connectivity ICs, logic & voltage translation, sensors, and other ICs, because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other Texas Instruments Accused Products contain similar features as the Texas Instruments BQ25123 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other Texas Instruments Accused Products contain similar features as the Texas Instruments BQ25123, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having a surface;	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 1.
[Claim 1, Element 2] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 2.
[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 3.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region;	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4.
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 5. <i>See</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 1, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 1, Element 6. Upon information and belief, at least some of the transistors form digital logic of the VLSI semiconductor device. For example, transistors are commonly used to implement digital logic, e.g., for controlling access to memory components/functionality. Details regarding transistors in the Texas Instruments Accused Products are in the possession of the Defendants and are expected to be obtained through discovery. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
2. The VLSI semiconductor device of claim 1, wherein the substrate is a p-type substrate.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 2.
3. The VLSI semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 4.
4. The VLSI semiconductor device of claim 1, wherein the first active region and second	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 5; Exhibit A-2, Claim 4. Upon information and belief, the first and second active regions contain digital logic as claimed. <i>See</i> above at Claim 1, Element 6.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
active region contain digital logic formed by one of either p-channel and n-channel devices.	
5. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 6.
6. The VLSI semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 7.
7. The VLSI semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 8.
8. The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Elements 1-3.
9. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 9.
13. The VLSI semiconductor device of claim 1, wherein the	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 13. Upon information and belief, the transistors which can be formed in the first and second active regions are CMOS digital logic transistors as claimed. <i>See</i> above at Claim 1, Element 6.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	
15. The VLSI semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 15.
16. The VLSI semiconductor device of claim 1, wherein the device is a flash memory.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 16.
17. The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors.	The Texas Instruments Accused Products meet this limitation. Upon information and belief, the semiconductor device comprises digital logic and capacitors. <i>See</i> above at Claim 1, Element 6 (discussion regarding digital logic). Details regarding digital logic and capacitors in the Texas Instruments Accused Products are in the possession of the Defendants and are expected to be obtained through discovery.
20. The VLSI semiconductor device of claim 1, wherein each of the first and second active regions are in the lateral or vertical direction.	The Texas Instruments Accused Products meet this limitation. As shown by SEM imaging (<i>see</i> Exhibit A-1, Claim 1, Elements 1-3), each of the first and second active regions are in the lateral or vertical direction.
[Claim 21, Preamble] A VLSI semiconductor device, comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include a semiconductor device. <i>See</i> above at Claim 1, Preamble.
[Claim 21, Element 1] a substrate of a first doping type at a first doping level having a surface;	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1.
[Claim 21, Element 2] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 9, Element 2.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
conductivity to the first doping type and within which transistors can be formed in the surface thereof;	
[Claim 21, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 9, Element 3.
[Claim 21, Element 4] transistors formed in at least one of the first active region or second active region;	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4.
[Claim 21, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 5. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 21, Element 6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 1, Element 6. As shown by SCM/sMIM analysis (<i>see</i> Exhibit A-1, Claim 1, Element 1), the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof. For example, the quasilinear nature of the concentration is shown in the SCM/sMIM graph discussed at Exhibit A-1, Claim 1, Element 5. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
23. The VLSI semiconductor device of claim 21, wherein the substrate is a p-type substrate.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 2.
24. The VLSI semiconductor device of claim 21, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 4.
25. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 5.
26. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 6.
27. The VLSI semiconductor device of claim 21, wherein the first active region and second active region are each separated by at least one isolation region.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 7.
28. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 9.
32. The VLSI semiconductor device of claim 21, wherein the	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 8.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
graded dopant is fabricated with an ion implantation process.	
33. The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 15.
34. The VLSI semiconductor device of claim 21, wherein the device is a flash memory.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 16.
38. The VLSI semiconductor device of claim 21, wherein each of the first and second active regions are in the lateral or vertical direction.	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 20.
[Claim 39, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include a semiconductor device. <i>See</i> Exhibit A-1, Claim 1, Preamble.
[Claim 39, Element 1] a substrate of a first doping type at a first doping level;	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 1.
[Claim 39, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 2.
[Claim 39, Element 3] a second active region separate from the first active region disposed adjacent to the first active region	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 3.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
and within which transistors can be formed;	
[Claim 39, Element 4] transistors formed in at least one of the first active region or second active region; and	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4.
[Claim 39, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 5; <i>see</i> above at Claim 21, Element 5. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
40. The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-2, Claim 1, Element 6. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 41, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include a semiconductor device. <i>See</i> above at Claim 39, Preamble.
[Claim 41, Element 1] a substrate of a first doping type at a first doping level;	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 1.
[Claim 41, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 39, Element 2.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
conductivity to the first doping type and within which transistors can be formed;	
[Claim 41, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 39, Element 3.
[Claim 41, Element 4] transistors formed in at least one of the first active region or second active region; and	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4.
[Claim 41, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 5. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 42, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include a semiconductor device. <i>See</i> above at Claim 39, Preamble.
[Claim 42, Element 1] a substrate of a first doping type at a first doping level;	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 1.
[Claim 42, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 39, Element 2.

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
[Claim 42, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 39, Element 3.
[Claim 42, Element 4] transistors formed in at least one of the first active region or second active region; and	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4.
[Claim 42, Element 5] at least a portion of at least one of the first and second active regions having at least one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The Texas Instruments Accused Products meet this limitation. SCM/sMIM analysis (<i>see</i> Exhibit A-1, Claim 1, Element 5) reveals at least one graded dopant acceptor concentration (e.g., concentration in n-well) as claimed. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 44, Preamble] A CMOS Semiconductor device comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include a CMOS Semiconductor device. <i>See</i> Exhibit A-1, Claim 1, Preamble; Exhibit A-1, Claim 18.
[Claim 44, Element 1]: a surface layer;	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 21, Element 1.
[Claim 44, Element 2] a substrate;	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 44, Element 1.
[Claim 44, Element 3] an active region including a source and a drain, disposed on one surface of the surface layer;	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 2 (discussion of active region); Exhibit A-1, Claim 18 (discussion of source and drain).

Exhibit A-3 to Greenthread's Complaint

U.S. Patent No. 11,121,222	Accused Products
[Claim 44, Element 4] a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate, the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 21, Element 5. Upon information and belief, the drift layer has a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions as claimed, as a result of the above-discussed graded concentration of dopants. Details regarding electric field characteristics are in the possession of the Defendants and are expected to be obtained through discovery. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 44, Element 5] at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 21, Element 6. The well region (discussed above for Claim 21, Element 6) has a graded concentration of dopants. Upon information and belief, the well region is disposed in the single drift layer, and it has a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions as claimed, as a result of the well region's graded concentration of dopants. Details regarding electric field characteristics are in the possession of the Defendants and are expected to be obtained through discovery. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-4 to Greenthread's Complaint

U.S. Patent No. 8,421,195	Accused Products
[Claim 1, Preamble] A CMOS Semiconductor device comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include a CMOS semiconductor device. The Texas Instruments BQ25123 Battery Charger Power Management IC ("BQ25123") discussed for claim 1 of Exhibit A-3 is a semiconductor device (<i>see</i> Exhibit A-1, Claim 1, Preamble and Exhibit A-3, Claim 44, Preamble) with transistors, and is a CMOS semiconductor device upon information and belief. The Texas Instruments BQ25123 is representative of the Texas Instruments Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other Texas Instruments Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '195 patent (and the other asserted patents). For example, the other Texas Instruments Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '195 patent (and the other asserted patents). The claimed invention would have application in numerous types of Texas Instruments products, including, but not limited to, amplifiers, audio processors, digital-to-analog converters, analog-to-digital converters, digital clocks, interface ICs, isolation ICS, microcontrollers and processors, digital signal processors, digital light processors, motor drivers, power management, switches & multiplexers, radio frequency and microwave ICs, wireless connectivity ICs, logic & voltage translation, sensors, and other ICs, because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other Texas Instruments Accused Products contain similar features as the Texas Instruments BQ25123 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other Texas Instruments Accused Products contain similar features as the Texas Instruments BQ25123, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1] a surface layer;	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 44, Element 1.
[Claim 1, Element 2] a substrate;	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 44, Element 2.
[Claim 1, Element 3] an active region including a source and a drain, disposed on one surface of said surface layer;	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 44, Element 3.
[Claim 1, Element 4] a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 44, Element 4. Upon information and belief, the drift layer (<i>see</i> Exhibit A-3, Claim 44, Element 4) has a first static unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate, as claimed. Details regarding electric field characteristics are in the possession of the Defendants and are expected to be obtained through discovery. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SPM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-4 to Greenthread's Complaint

U.S. Patent No. 8,421,195	Accused Products
unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and	
[Claim 1, Element 5] at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 44, Element 5. Upon information and belief, the well region has a second static unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate, as claimed. Details regarding electric field characteristics are in the possession of the Defendants and are expected to be obtained through discovery. <i>See also</i> SPM/SMIM analysis reproduced at Exhibit A-1 Claim 1 Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SPM/SMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
2. The CMOS Semiconductor device of claim 1, wherein the said drift layer is a deeply-implanted layer.	The Texas Instruments Accused Products meet this limitation. Upon information and belief, the drift layer is a deeply-implanted layer.
3. The CMOS Semiconductor device of claim 1, wherein said drift layer is an epitaxial layer.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 4; Exhibit A-3, Claim 44, Element 4. Upon information and belief, the drift layer is grown above the substrate and is an epitaxial layer.
5. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a quasi-linear gradient.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Elements 1, 5.
6. The CMOS Semiconductor device of claim 1, wherein said graded concentration follows an exponential gradient.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Elements 1, 5.

Exhibit A-5 to Greenthread's Complaint

U.S. Patent No. 9,190,502	Accused Products
[Claim 7, Preamble] A semiconductor device comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include a semiconductor device. The Texas Instruments BQ25123 Battery Charger Power Management IC ("BQ25123") discussed for claim 1 of Exhibit A-1 is a semiconductor device (<i>see</i> Exhibit A-1, Claim 1, Preamble) with transistors, and is a semiconductor device upon information and belief. Details regarding transistor count are in the possession of the Defendants and are expected to be obtained through discovery. The Texas Instruments BQ25123 is representative of the Texas Instruments Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other Texas Instruments Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '502 patent (and the other asserted patents). For example, the other Texas Instruments Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '502 patent (and the other asserted patents). The claimed invention would have application in numerous types of Texas Instruments products, including, but not limited to, amplifiers, audio processors, digital-to-analog converters, analog-to-digital converters, digital clocks, interface ICs, isolation ICs, microcontrollers and processors, digital signal processors, digital light processors, motor drivers, power management, switches & multiplexers, radio frequency and microwave ICs, wireless connectivity ICs, logic & voltage translation, sensors, and other ICs, because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other Texas Instruments Accused Products contain similar features as the Texas Instruments BQ25123 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other Texas Instruments Accused Products contain similar features as the Texas Instruments BQ25123, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 7, Element 1] a surface layer;	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-4, Claim 1, Element 1.
[Claim 7, Element 2] a substrate;	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-4, Claim 1, Element 2.
[Claim 7, Element 3] an active region including a source and a drain, disposed on one surface of said surface layer;	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-4, Claim 1, Element 3.
[Claim 7, Element 4] a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-4, Claim 1, Element 4. The graded concentration of dopants observed via SCM/sMIM analysis (<i>see</i> Exhibit A-1, Claim 1, Elements 1, 5) generates a first static unidirectional electric drift field to aid the movement of minority carriers, as claimed. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-5 to Greenthread's Complaint

U.S. Patent No. 9,190,502	Accused Products
aid the movement of minority carriers from said surface layer to said substrate;	
[Claim 7, Element 5] and at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-4, Claim 1, Element 5. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
8. The semiconductor device of claim 7 wherein said first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions.	The Texas Instruments Accused Products meet this limitation. Upon information and belief, the first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions. Details regarding the electric fields and active regions are in the possession of the Defendants and are expected to be obtained through discovery. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
[Claim 1, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include an electronic system. <i>See</i> Exhibit A-1, Claim 1, Preamble; Exhibit A-4, Claim 1, Preamble. Each Texas Instruments Accused Product is an electronic system, because a computer is an electronic system. The Texas Instruments BQ25123 is representative of the Texas Instruments Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other Texas Instruments Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '014 patent (and the other asserted patents). For example, the other Texas Instruments Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '014 patent (and the other asserted patents). The claimed invention would have application in numerous types of Texas Instruments products, including, but not limited to, amplifiers, audio processors, digital-to-analog converters, analog-to-digital converters, digital clocks, interface ICs, isolation ICS, microcontrollers and processors, digital signal processors, digital light processors, motor drivers, power management, switches & multiplexers, radio frequency and microwave ICs, wireless connectivity ICs, logic & voltage translation, sensors, and other ICs, because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other Texas Instruments Accused Products contain similar features as the Texas Instruments BQ25123 transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other Texas Instruments Accused Products contain similar features as the Texas Instruments BQ25123, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 1, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Preamble.
[Claim 1, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 1, Element 1.
[Claim 1, Element 1c] a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 1, Element 2; Exhibit A-1, Claim 9, Element 2.
[Claim 1, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 1, Element 3; Exhibit A-1, Claim 9, Element 3.
[Claim 1, Element 1e] transistors formed in at least one of the first	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 1, Element 4.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
active region or second active region;	
[Claim 1, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 1, Element 5. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 1, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the semiconductor device.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 1, Element 6; Exhibit A-3, Claim 21, Element 5. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.6.
2. The system of Claim 1, wherein the substrate of the at least one semiconductor device is a p-type substrate.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 2.
3. The system of Claim 1, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 3.
4. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device contain digital logic formed by one of either p-channel and n-channel devices.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 4.
5. The system of Claim 1, wherein the first active region and second	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 5.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
active region of the at least one semiconductor device contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	
6. The system of Claim 1, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 6.
7. The system of Claim 1, wherein the graded dopant is fabricated with an ion implantation process.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 7.
8. The system of Claim 1, wherein the first and second active regions of the at least one semiconductor device are formed adjacent the first surface of the substrate of the at least one semiconductor device.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 8.
9. The system of Claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 9.
13. The system of claim 1, wherein the transistors which can be formed in the first and second active regions of the at least one semiconductor device are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 13.
15. The system of Claim 1, wherein the at least one semiconductor device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 15.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
16. The system of Claim 1, wherein the at least one semiconductor device is a flash memory.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 16.
17. The system of Claim 1, wherein the at least one semiconductor device comprises digital logic and capacitors.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 17.
20. The system of Claim 1, wherein each of the first and second active regions of the at least one semiconductor device are in the lateral or vertical direction.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 20.
[Claim 21, Preamble] An electronic system, the system comprising:	To the extent the preamble is a limitation, the Texas Instruments Accused Products include an electronic system. <i>See</i> above at Claim 1, Preamble.
[Claim 21, Element 1a] at least one semiconductor device, the at least one semiconductor device including:	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1a.
[Claim 21, Element 1b] a substrate of a first doping type at a first doping level having a surface;	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1b.
[Claim 21, Element 1c] a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1c; Exhibit A-1, Claim 9, Element 2.
[Claim 21, Element 1d] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1d; Exhibit A-1, Claim 9, Element 3.
[Claim 21, Element 1e] transistors formed in at least one of the first active region or second active region;	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1e.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
[Claim 21, Element 1f] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1f; Exhibit A-1, Claim 9, Element 5. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 21, Element 1g] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier thereof movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.	The Texas Instruments Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 1g; Exhibit A-3, Claim 21, Element 6. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
23. The system of Claim 21, wherein the substrate of the at least one semiconductor device is a p-type substrate.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 23.
24. The system of Claim 21, wherein the substrate of the at least one semiconductor device has epitaxial silicon on top of a nonepitaxial substrate.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 24.
25. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain at least one of either p-channel and n-channel devices.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 25.
26. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device contain either p-channel or n-channel	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 26.

Exhibit A-6 to Greenthread's Complaint

U.S. Patent No. 11,316,014	Accused Products
devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.	
27. The system of Claim 21, wherein the first active region and second active region of the at least one semiconductor device are each separated by at least one isolation region.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 27.
28. The system of Claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region of the at least one semiconductor device are either p-type or n-type.	The Texas Instruments Accused Products meet this limitation. <i>See</i> Exhibit A-3, Claim 28.

CIVIL COVER SHEET

The JS 44 civil cover sheet and the information contained herein neither replace nor supplement the filing and service of pleadings or other papers as required by law, except as provided by local rules of court. This form, approved by the Judicial Conference of the United States in September 1974, is required for the use of the Clerk of Court for the purpose of initiating the civil docket sheet. (SEE INSTRUCTIONS ON NEXT PAGE OF THIS FORM.)

I. (a) PLAINTIFFS GREENTHREAD, LLC (b) County of Residence of First Listed Plaintiff <u>Dallas County, TX</u> (EXCEPT IN U.S. PLAINTIFF CASES) (c) Attorneys (Firm Name, Address, and Telephone Number) Alan L. Whitehurst, McKool Smith, P.C. 1999 K St.,NW Suite 600, Washington, DC 20006, Tel: 202.370.8300	DEFENDANTS TEXAS INSTRUMENTS INCORPORATED County of Residence of First Listed Defendant _____ (IN U.S. PLAINTIFF CASES ONLY) NOTE: IN LAND CONDEMNATION CASES, USE THE LOCATION OF THE TRACT OF LAND INVOLVED. Attorneys (If Known) _____
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II. BASIS OF JURISDICTION (Place an "X" in One Box Only) ☐ 1 U.S. Government Plaintiff ☒ 3 Federal Question (U.S. Government Not a Party) ☐ 2 U.S. Government Defendant ☐ 4 Diversity (Indicate Citizenship of Parties in Item III)	III. CITIZENSHIP OF PRINCIPAL PARTIES (Place an "X" in One Box for Plaintiff and One Box for Defendant) (For Diversity Cases Only) <table> <tr> <td></td> <td>PTF</td> <td>DEF</td> <td></td> <td>PTF</td> <td>DEF</td> </tr> <tr> <td>Citizen of This State</td> <td>☐ 1</td> <td>☐ 1</td> <td>Incorporated or Principal Place of Business In This State</td> <td>☐ 4</td> <td>☐ 4</td> </tr> <tr> <td>Citizen of Another State</td> <td>☐ 2</td> <td>☐ 2</td> <td>Incorporated and Principal Place of Business In Another State</td> <td>☐ 5</td> <td>☐ 5</td> </tr> <tr> <td>Citizen or Subject of a Foreign Country</td> <td>☐ 3</td> <td>☐ 3</td> <td>Foreign Nation</td> <td>☐ 6</td> <td>☐ 6</td> </tr> </table>		PTF	DEF		PTF	DEF	Citizen of This State	☐ 1	☐ 1	Incorporated or Principal Place of Business In This State	☐ 4	☐ 4	Citizen of Another State	☐ 2	☐ 2	Incorporated and Principal Place of Business In Another State	☐ 5	☐ 5	Citizen or Subject of a Foreign Country	☐ 3	☐ 3	Foreign Nation	☐ 6	☐ 6
	PTF	DEF		PTF	DEF																				
Citizen of This State	☐ 1	☐ 1	Incorporated or Principal Place of Business In This State	☐ 4	☐ 4																				
Citizen of Another State	☐ 2	☐ 2	Incorporated and Principal Place of Business In Another State	☐ 5	☐ 5																				
Citizen or Subject of a Foreign Country	☐ 3	☐ 3	Foreign Nation	☐ 6	☐ 6																				

IV. NATURE OF SUIT (Place an "X" in One Box Only) Click here for: Nature of Suit Code Descriptions.			
CONTRACT ☐ 110 Insurance ☐ 120 Marine ☐ 130 Miller Act ☐ 140 Negotiable Instrument ☐ 150 Recovery of Overpayment & Enforcement of Judgment ☐ 151 Medicare Act ☐ 152 Recovery of Defaulted Student Loans (Excludes Veterans) ☐ 153 Recovery of Overpayment of Veteran's Benefits ☐ 160 Stockholders' Suits ☐ 190 Other Contract ☐ 195 Contract Product Liability ☐ 196 Franchise	TORTS PERSONAL INJURY ☐ 310 Airplane ☐ 315 Airplane Product Liability ☐ 320 Assault, Libel & Slander ☐ 330 Federal Employers' Liability ☐ 340 Marine ☐ 345 Marine Product Liability ☐ 350 Motor Vehicle ☐ 355 Motor Vehicle Product Liability ☐ 360 Other Personal Injury ☐ 362 Personal Injury - Medical Malpractice	PERSONAL INJURY ☐ 365 Personal Injury - Product Liability ☐ 367 Health Care/Pharmaceutical Personal Injury Product Liability ☐ 368 Asbestos Personal Injury Product Liability PERSONAL PROPERTY ☐ 370 Other Fraud ☐ 371 Truth in Lending ☐ 380 Other Personal Property Damage ☐ 385 Property Damage Product Liability	FORFEITURE/PENALTY ☐ 625 Drug Related Seizure of Property 21 USC 881 ☐ 690 Other LABOR ☐ 710 Fair Labor Standards Act ☐ 720 Labor/Management Relations ☐ 740 Railway Labor Act ☐ 751 Family and Medical Leave Act ☐ 790 Other Labor Litigation ☐ 791 Employee Retirement Income Security Act IMMIGRATION ☐ 462 Naturalization Application ☐ 465 Other Immigration Actions
REAL PROPERTY ☐ 210 Land Condemnation ☐ 220 Foreclosure ☐ 230 Rent Lease & Ejectment ☐ 240 Torts to Land ☐ 245 Tort Product Liability ☐ 290 All Other Real Property	CIVIL RIGHTS ☐ 440 Other Civil Rights ☐ 441 Voting ☐ 442 Employment ☐ 443 Housing/Accommodations ☐ 445 Amer. w/Disabilities - Employment ☐ 446 Amer. w/Disabilities - Other ☐ 448 Education	PRISONER PETITIONS Habeas Corpus: ☐ 463 Alien Detainee ☐ 510 Motions to Vacate Sentence ☐ 530 General ☐ 535 Death Penalty Other: ☐ 540 Mandamus & Other ☐ 550 Civil Rights ☐ 555 Prison Condition ☐ 560 Civil Detainee - Conditions of Confinement	BANKRUPTCY ☐ 422 Appeal 28 USC 158 ☐ 423 Withdrawal 28 USC 157 INTELLECTUAL PROPERTY RIGHTS ☐ 820 Copyrights ☒ 830 Patent ☐ 835 Patent - Abbreviated New Drug Application ☐ 840 Trademark ☐ 880 Defend Trade Secrets Act of 2016 SOCIAL SECURITY ☐ 861 HIA (1395ff) ☐ 862 Black Lung (923) ☐ 863 DIWC/DIWW (405(g)) ☐ 864 SSID Title XVI ☐ 865 RSI (405(g)) FEDERAL TAX SUITS ☐ 870 Taxes (U.S. Plaintiff or Defendant) ☐ 871 IRS—Third Party 26 USC 7609
OTHER STATUTES ☐ 375 False Claims Act ☐ 376 Qui Tam (31 USC 3729(a)) ☐ 400 State Reapportionment ☐ 410 Antitrust ☐ 430 Banks and Banking ☐ 450 Commerce ☐ 460 Deportation ☐ 470 Racketeer Influenced and Corrupt Organizations ☐ 480 Consumer Credit (15 USC 1681 or 1692) ☐ 485 Telephone Consumer Protection Act ☐ 490 Cable/Sat TV ☐ 850 Securities/Commodities/Exchange ☐ 890 Other Statutory Actions ☐ 891 Agricultural Acts ☐ 893 Environmental Matters ☐ 895 Freedom of Information Act ☐ 896 Arbitration ☐ 899 Administrative Procedure Act/Review or Appeal of Agency Decision ☐ 950 Constitutionality of State Statutes			

V. ORIGIN (Place an "X" in One Box Only) ☒ 1 Original Proceeding ☐ 2 Removed from State Court ☐ 3 Remanded from Appellate Court ☐ 4 Reinstated or Reopened ☐ 5 Transferred from Another District (specify) _____ ☐ 6 Multidistrict Litigation - Transfer ☐ 8 Multidistrict Litigation - Direct File

VI. CAUSE OF ACTION	Cite the U.S. Civil Statute under which you are filing (Do not cite jurisdictional statutes unless diversity): 35 U.S.C. § 271
	Brief description of cause: Patent Infringement

VII. REQUESTED IN COMPLAINT:	☐ CHECK IF THIS IS A CLASS ACTION UNDER RULE 23, F.R.Cv.P.	DEMAND \$ _____	CHECK YES only if demanded in complaint: JURY DEMAND: ☒ Yes ☐ No
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VIII. RELATED CASE(S) IF ANY (See instructions):	JUDGE _____	DOCKET NUMBER _____
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DATE Apr 6, 2023	SIGNATURE OF ATTORNEY OF RECORD /s/ Alan L. Whitehurst
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FOR OFFICE USE ONLY			
RECEIPT # _____	AMOUNT _____	APPLYING IFP _____	JUDGE _____

INSTRUCTIONS FOR ATTORNEYS COMPLETING CIVIL COVER SHEET FORM JS 44

Authority For Civil Cover Sheet

The JS 44 civil cover sheet and the information contained herein neither replaces nor supplements the filings and service of pleading or other papers as required by law, except as provided by local rules of court. This form, approved by the Judicial Conference of the United States in September 1974, is required for the use of the Clerk of Court for the purpose of initiating the civil docket sheet. Consequently, a civil cover sheet is submitted to the Clerk of Court for each civil complaint filed. The attorney filing a case should complete the form as follows:

- I.(a) Plaintiffs-Defendants.** Enter names (last, first, middle initial) of plaintiff and defendant. If the plaintiff or defendant is a government agency, use only the full name or standard abbreviations. If the plaintiff or defendant is an official within a government agency, identify first the agency and then the official, giving both name and title.
 - (b) County of Residence.** For each civil case filed, except U.S. plaintiff cases, enter the name of the county where the first listed plaintiff resides at the time of filing. In U.S. plaintiff cases, enter the name of the county in which the first listed defendant resides at the time of filing. (NOTE: In land condemnation cases, the county of residence of the "defendant" is the location of the tract of land involved.)
 - (c) Attorneys.** Enter the firm name, address, telephone number, and attorney of record. If there are several attorneys, list them on an attachment, noting in this section "(see attachment)".
- II. Jurisdiction.** The basis of jurisdiction is set forth under Rule 8(a), F.R.Cv.P., which requires that jurisdictions be shown in pleadings. Place an "X" in one of the boxes. If there is more than one basis of jurisdiction, precedence is given in the order shown below.
- United States plaintiff. (1) Jurisdiction based on 28 U.S.C. 1345 and 1348. Suits by agencies and officers of the United States are included here. United States defendant. (2) When the plaintiff is suing the United States, its officers or agencies, place an "X" in this box.
- Federal question. (3) This refers to suits under 28 U.S.C. 1331, where jurisdiction arises under the Constitution of the United States, an amendment to the Constitution, an act of Congress or a treaty of the United States. In cases where the U.S. is a party, the U.S. plaintiff or defendant code takes precedence, and box 1 or 2 should be marked.
- Diversity of citizenship. (4) This refers to suits under 28 U.S.C. 1332, where parties are citizens of different states. When Box 4 is checked, the citizenship of the different parties must be checked. (See Section III below; **NOTE: federal question actions take precedence over diversity cases.**)
- III. Residence (citizenship) of Principal Parties.** This section of the JS 44 is to be completed if diversity of citizenship was indicated above. Mark this section for each principal party.
- IV. Nature of Suit.** Place an "X" in the appropriate box. If there are multiple nature of suit codes associated with the case, pick the nature of suit code that is most applicable. Click here for: [Nature of Suit Code Descriptions](#).
- V. Origin.** Place an "X" in one of the seven boxes.
- Original Proceedings. (1) Cases which originate in the United States district courts.
- Removed from State Court. (2) Proceedings initiated in state courts may be removed to the district courts under Title 28 U.S.C., Section 1441.
- Remanded from Appellate Court. (3) Check this box for cases remanded to the district court for further action. Use the date of remand as the filing date.
- Reinstated or Reopened. (4) Check this box for cases reinstated or reopened in the district court. Use the reopening date as the filing date.
- Transferred from Another District. (5) For cases transferred under Title 28 U.S.C. Section 1404(a). Do not use this for within district transfers or multidistrict litigation transfers.
- Multidistrict Litigation – Transfer. (6) Check this box when a multidistrict case is transferred into the district under authority of Title 28 U.S.C. Section 1407.
- Multidistrict Litigation – Direct File. (8) Check this box when a multidistrict case is filed in the same district as the Master MDL docket.
- PLEASE NOTE THAT THERE IS NOT AN ORIGIN CODE 7.** Origin Code 7 was used for historical records and is no longer relevant due to changes in statute.
- VI. Cause of Action.** Report the civil statute directly related to the cause of action and give a brief description of the cause. **Do not cite jurisdictional statutes unless diversity.** Example: U.S. Civil Statute: 47 USC 553 Brief Description: Unauthorized reception of cable service.
- VII. Requested in Complaint.** Class Action. Place an "X" in this box if you are filing a class action under Rule 23, F.R.Cv.P.
- Demand. In this space enter the actual dollar amount being demanded or indicate other demand, such as a preliminary injunction.
- Jury Demand. Check the appropriate box to indicate whether or not a jury is being demanded.
- VIII. Related Cases.** This section of the JS 44 is used to reference related pending cases, if any. If there are related pending cases, insert the docket numbers and the corresponding judge names for such cases.

Date and Attorney Signature. Date and sign the civil cover sheet.