

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TEXAS INSTRUMENTS INCORPORATED,
Petitioner,

v.

GREENTHREAD, LLC,
Patent Owner.

IPR2024-00672
Patent 10,510,842 B2

Before JON B. TORNQUIST, MONICA S. ULLAGADDI, and
JULIA HEANEY, *Administrative Patent Judges*.

HEANEY, *Administrative Patent Judge*.

DECISION

Granting Institution of *Inter Partes* Review

35 U.S.C. § 314

Granting Motion for Joinder

35 U.S.C. § 315(c); 37 C.F.R. § 42.122(b)

I. INTRODUCTION

A. Background

On March 12, 2024, Texas Instruments Incorporated (“Petitioner”) filed a Petition (Paper 3, “Pet.”) requesting *inter partes* review of claims 1–18 (“the challenged claims”) of U.S. Patent No. 10,510,842 B2 (Ex. 1001, “the ’842 patent”). Concurrently with the Petition, Petitioner filed a Motion for Joinder (Paper 2, “Mot.”), requesting that we join it with *Semiconductor Components Industries, LLC v. Greenthread, LLC*, IPR2023-01243 (“1243 IPR”), in which we instituted trial on February 12, 2024. Mot. 1. Greenthread, LLC (“Patent Owner”) filed a Preliminary Response (Paper 13, “Prelim. Resp.”) and an Opposition to Petitioner’s Motion for Joinder (Paper 7, “Opp. Mot. Join.”). With our authorization, Petitioner filed a Reply to Patent Owner’s Preliminary Response (Paper 16). Patent Owner did not reply.

B. Related Proceedings

The parties indicate that the ’842 patent is at issue in the following district court proceedings:

Greenthread, LLC v. Western Digital Corp., No. 1:23-cv-00326 (D. Del. filed March 24, 2023);

Greenthread, LLC v. Cirrus Logic, Inc., No. 1:23-cv-00369 (W.D. Tex. filed March 31, 2023);

Greenthread, LLC v. Texas Instruments Inc., No. 2:23-cv-00157 (E.D. Tex. filed April 6, 2023);

Greenthread, LLC v. OSRAM GmbH, No. 2:23-cv-00179 (E.D. Tex. filed April 19, 2023);

Greenthread, LLC v. ON Semiconductor Corp., No. 1:23-cv-00443
(D. Del. filed April 21, 2023);

Greenthread, LLC v. OmniVision Technologies, Inc., No. 2:23-cv-00212 (E.D. Tex. filed May 10, 2023); and

Greenthread, LLC v. Monolithic Power Systems, Inc., No. 1:23-cv-00579 (D. Del. filed May 26, 2023).

Pet. 1–2; Paper 5, 1–2.

The parties further note that the '842 patent is at issue in the following *inter partes* review proceedings:

Semiconductor Components Industries LLC v. Greenthread, LLC,
IPR2023-01243 (“1243 IPR”);

Cirrus Logic, Inc. et al. v. Greenthread, LLC, IPR2024-00016;

Monolithic Power Systems, Inc. v. Greenthread, LLC, IPR2024-00550.

Pet. 2; Paper 5, 2.

The parties also note that the '842 patent was at issue in a number of district court and *inter partes* review proceedings that are no longer pending.
Pet. 2–3; Paper 5, 3–4.

C. The '842 Patent

The '842 patent issued December 17, 2019, and claims the benefit of a series of continuation applications, the earliest of which was filed September 3, 2004. Ex. 1001, codes (45), (60). The '842 patent is titled “Semiconductor Devices with Graded Dopant Regions” and “relates to all semiconductor devices and systems.” *Id.* at code (54), 1:32–33.

The '842 patent explains that, in bipolar junction transistors, minority carriers are the principal device conduction mechanism, but notes that

majority carriers also play a small but finite role in modulating the conductivity in such devices. *Id.* at 1:43–47. The '842 patent further explains that “[e]fforts have been made in graded base transistors to create an aiding drift field to enhance the diffusing minority carrier’s speed from emitter to collector.” *Id.* at 1:55–57. According to the '842 patent, this improvement has not been implemented in most semiconductor devices, including various power MOSFETs and IGBTs, which “still use a uniformly doped ‘drift epitaxial’ region in the base.” *Id.* at 1:57–62. The invention of the '842 patent implements a graded dopant concentration in these devices, which the '842 patent contends results in two important performance enhancements: “electrons can be swept from source to drain rapidly, while at the same time holes can be recombined closer to the n+ buffer layer,” thereby improving “ t_{on} and t_{off} in the same device.” *Id.* at 3:38–43.

Figure 1 of the '842 patent is reproduced below.

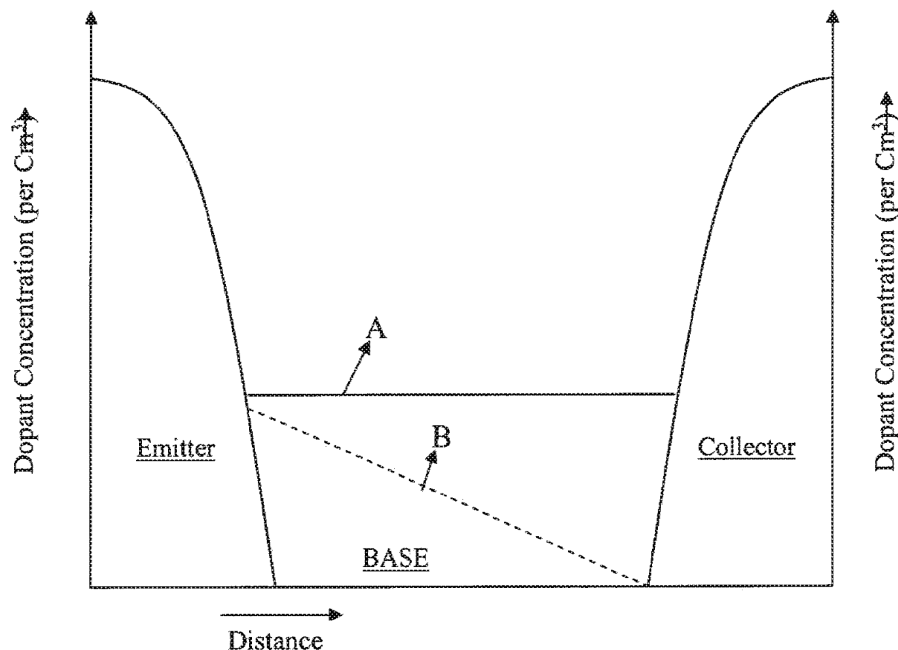


Figure 1 is labeled “Prior Art” and shows a plot of dopant concentration versus distance. Ex. 1001, Fig. 1. According to the ’842 patent, Figure 1 “illustrates the relative doping profiles of emitter, base and collector for the two most popular bipolar junction transistors: namely, uniform base (‘A’) and graded base (‘B’).” *Id.* at 2:35–38.

Figure 3A of the ’842 patent is reproduced below.

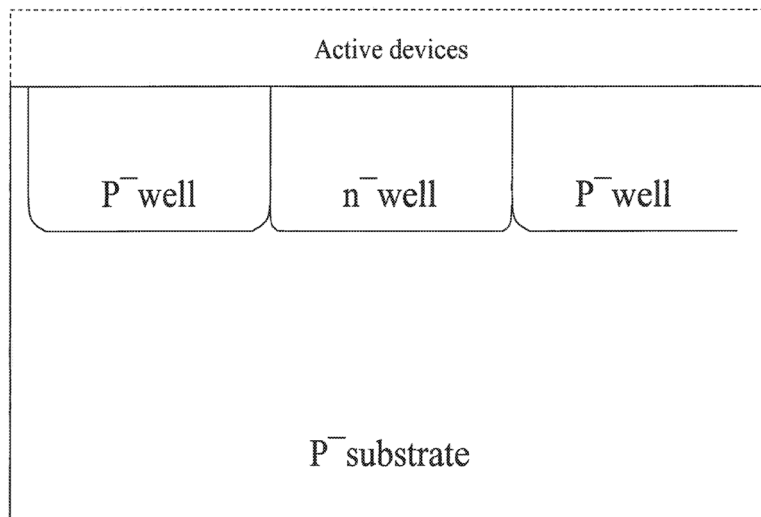


Figure 3A is labeled “Prior art (Twin well CMOS) for a CMOS integrated circuit” (“IC”), and shows a “typical” complementary metal-oxide-semiconductor (“CMOS”) very large-scale integrated circuit (“VLSI”) device that employs “a twin well substrate, on which active devices are subsequently fabricated.” *Id.* at 2:16–18, Fig. 3A; *see also id.* at 2:41–46 (explaining that Figure 3A shows a “commonly used prior art CMOS silicon substrate[]” having “a typical prior art IC with two wells (one n⁻ well in which p-channel transistors are subsequently fabricated and one p⁻ well in which n-channel transistors are subsequently fabricated)”).

Figure 5A of the '842 patent is reproduced below.

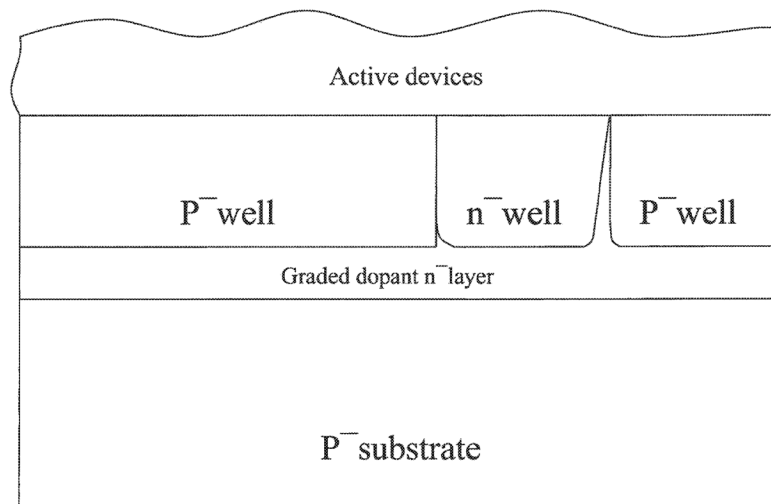


Figure 5A illustrates a cross section of a CMOS silicon substrate with two wells and an underlying layer using embodiments of the invention. *Id.* at 2:54–56. Figure 5A is labeled “[a] CMOS Substrate for digital, mixed[] signal, and sen[s]or[] IC’s.” Ex. 1001, Fig. 5A. The figure illustrates “a CMOS silicon substrate with two wells and an underlying layer,” which is labeled “Graded dopant n⁻ layer.” *Id.* at 2:54–58, Fig. 5A.

According to the '842 patent, “[s]purious minority carriers can be generated by clock switching in digital VSLI logic and memory ICs.” Ex. 1001, 3:47–48. The '842 patent states that these “unwanted carriers” degrade performance of various types of devices, including digital imaging ICs, and describes “a novel technique” in which “a drift field [is used] to sweep these unwanted minority carriers from the active circuitry at the surface into the substrate in a monolithic die as quickly as possible.” *Id.* at 3:49–55, 3:60–64. For example, “[i]n a preferred embodiment, the subterranean n⁻ layer has a graded donor concentration to sweep the minority carriers deep into the substrate.” *Id.* at 3:64–66.

D. Illustrative Claim

Petitioner challenges claims 1–18 (all claims) of the '842 patent. Claims 1 and 9 are independent, and claim 1 is illustrative of the claimed subject matter.

1. A semiconductor device, comprising:

[1.1] a substrate of a first doping type at a first doping level having first and second surfaces;

[1.2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

[1.3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

[1.4] transistors formed in at least one of the first active region or second active region; and

[1.5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.

Ex. 1001, 4:45–60 (bracketed numbering added by Petitioner).

E. The Asserted Grounds of Unpatentability

The Petition in this proceeding challenges the same claims of the '842 patent on identical grounds of unpatentability, and relies on the same evidence, including the same declarant testimony, as presented in the 1243 IPR. Pet. 5; Mot. 1, 4–6; 1243 IPR, Paper 31, 7–8; Ex. 1003 (Declaration of Travis Blalock Ph.D.). Petitioner asserts the following grounds of unpatentability:

Claims Challenged	35 U.S.C. § ¹	Reference(s)/Basis
1, 2, 4–10, 12–18	103(a)	Kawagoe ²
1, 2, 4–10, 12–18	103(a)	Kawagoe, Gupta ³
1–3, 5–11, 13–18	103(a)	Wieczorek, ⁴ Wolf ⁵
1–3, 5–11, 13–18	103(a)	Wieczorek, Wolf, Gupta

Pet. 5.

II. TIMELINESS OF PETITION UNDER 35 U.S.C. § 315(B)

Pursuant to 35 U.S.C. § 315(b), “[a]n *inter partes* review may not be instituted if the petition requesting the proceeding is filed more than 1 year after the date on which the petitioner, real party in interest, or privy of the petitioner is served with a complaint alleging infringement of the patent.”

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), included revisions to 35 U.S.C. §§ 102 and 103 that became effective in 2013, after the effective filing date of the challenged claims. *See* Ex. 1001, codes (22), (60). Therefore, we apply the pre-AIA versions of 35 U.S.C. §§ 102 and 103(a).

² US 6,043,114, issued March 28, 2000 (Ex. 1007, “Kawagoe”). Petitioner asserts that Kawagoe is prior art under 35 U.S.C. § 102(b). Pet. 4.

³ US 6,163,877, issued December 19, 2000 (Ex. 1014, “Gupta”). Petitioner asserts that Gupta is prior art under 35 U.S.C. § 102(b). Pet. 5.

⁴ US 2003/0183856 A1, published October 2, 2003 (Ex. 1006, “Wieczorek”). Petitioner asserts that Wieczorek is prior art under 35 U.S.C. §§ 102(a),(e). Pet. 4.

⁵ Stanley Wolf and Richard N. Tauber, *Silicon Processing for the VLSI Era*, Vols. 1–4, Lattice Press (2000) (Ex. 1008, “Wolf”). Petitioner asserts that Wolf was published and publicly available no later than 2002, and is prior art under 35 U.S.C. § 102(b). Pet. 5 (citing Exs. 1012, 1013, 1036). Exhibit 1008 was submitted in four parts (A–D) and includes selected portions of Wolf. We cite to Wolf using its original page numbers and omit the exhibit part designations.

Patent Owner argues that the Petition is untimely under 35 U.S.C. § 315(b) because Petitioner is in privity with time-barred entities. Prelim. Resp. 18–39. However, 35 U.S.C. § 315(b) also provides that the one-year time bar “shall not apply to a request for joinder under subsection (c).” *See also* 37 C.F.R. § 42.122(b). Because the Petition is accompanied by a timely request for joinder (Paper 2) to the instituted proceeding (IPR2023-01243), which we grant as further discussed below, Patent Owner’s argument that the Petition is time-barred under 35 U.S.C. § 315(b) is moot, irrespective of whether Petitioner is in privity with time-barred entities.

III. MOTION FOR JOINDER

A party in an *inter partes* review may be joined as a party in another *inter partes* review, subject to certain statutory provisions:

(c) JOINDER.—If the Director institutes an *inter partes* review, the Director, in his or her discretion, may join as a party to that *inter partes* review any person who properly files a petition under section 311 that the Director, after receiving a preliminary response under section 313 or the expiration of the time for filing such a response, determines warrants the institution of an *inter partes* review under section 314.

35 U.S.C. § 315(c); *see also* 37 C.F.R. § 42.122 (“Any request for joinder must be filed, as a motion under § 42.22, no later than one month after the institution date of any *inter partes* review for which joinder is requested.”). “To join a party to an instituted [*inter partes* review (IPR)], the plain language of § 315(c) requires two different decisions.” *Facebook, Inc. v. Windy City Innovations, LLC*, 973 F.3d 1321, 1332 (Fed. Cir. 2020). “First, the statute requires that the Director (or the Board acting through a delegation of authority) . . . determine whether the joinder applicant’s petition for IPR ‘warrants’ institution under § 314.” *Id.* “Second, to effect

joinder, § 315(c) requires the Director to exercise [] discretion to decide whether to ‘join as a party’ the joinder applicant.” *Id.*

A. Whether the Petition Warrants Institution

Petitioner argues its Petition “is substantively the same as the [1243 IPR] petition. It challenges the same claims, on the same grounds, relies on the same prior art, and includes the exact same substantive arguments” Mot. 1. Patent Owner argues the Petition fails to establish obviousness of the “aid carrier movement” limitation [1.5]. Prelim. Resp. 3–16. This is the same substantive argument Patent Owner raises in its Patent Owner Response to the 1243 IPR petition. *Compare* IPR2023-01243 Paper 46, 13–26 *with* Prelim. Resp. 3–16. As we discuss further below (section III.A.3), the trial in the 1243 IPR is the better proceeding in which to resolve the parties’ arguments as to patentability of the challenged claims, and we determine institution is warranted here for the same reasons stated in the Decision on Institution in the 1243 IPR. Because Patent Owner includes patentability arguments in its Preliminary Response, however, we briefly address patentability of the challenged claims below.

1. Challenges Based on Kawagoe

Petitioner challenges claims 1, 2, 4–10, and 12–18 as obvious based on Kawagoe, alone or in combination with Gupta. Pet. 5, 12–38, 60–65.

2. Kawagoe (Ex. 1007)

Kawagoe discloses a process for manufacturing a semiconductor integrated circuit device using an epitaxial wafer, i.e., a semiconductor wafer having a semiconductor single crystal epitaxial layer grown over a polished semiconductor substrate. Ex. 1007, 1:13–27, 2:31–35. According to Kawagoe, “[t]he epitaxial wafer is advantageous in that it is excellent in

suppressing the soft errors and resisting to the latchup,”⁶ and also has “excellent breakdown characteristics” that “drastically reduce the defect density of the gate insulating film” of a semiconductor integrated device. *Id.* at 1:33–40.

Kawagoe discloses various “representative” processes, including processes in which the single crystal (epitaxial) layer contains an impurity of the same type and in the same concentration as the substrate body. Ex. 1007, 2:55–3:9. According to Kawagoe, the impurity concentration of the substrate body can be made higher than that of the epitaxial layer “so that the resistance of the semiconductor substrate body can be relatively lowered to improve the resistance to the latchup.” *Id.* at 4:1–8. Kawagoe discloses a process for manufacturing a semiconductor integrated circuit device including a step of forming a semiconductor region (well) extending below the epitaxial layer and having an impurity concentration that decreases with increasing depth below the epitaxial layer. *Id.* at 3:10–25. According to Kawagoe, the well can be used for forming a complementary Metal-Oxide-Semiconductor. Field-Effect-Transistor (“MOS.FET”) circuit. *Id.* at 3:32–38.

⁶ Petitioner submits Exhibit 1009 (Wang and Agrawal, Single Event Upset: An Embedded Tutorial, 21st Int’l Conf on VLSI Design, 429–434, IEEE 2008), which explains that “soft errors” are “random and not related to permanent hardware faults” and “[t]heir causes may be internal (e.g., interconnect coupling) or external (e.g., cosmic radiation),” including “alpha particles [that] are emitted when the nucleus of an unstable isotope decays to a lower energy state.” Ex. 1009, Abstract, 430. Dr. Blalock characterizes “latchup” as “a ‘short-circuit’ failure condition in poorly designed circuits.” Ex. 1003 ¶ 77.

Kawagoe describes seven embodiments, including Embodiment 1 (Ex. 1007, 6:41–12:40, Figs. 1–8) and Embodiment 4 (*id.* at 14:46–19:63, Figs. 16–25). Figure 1, reproduced below, depicts the device of Embodiment 1.

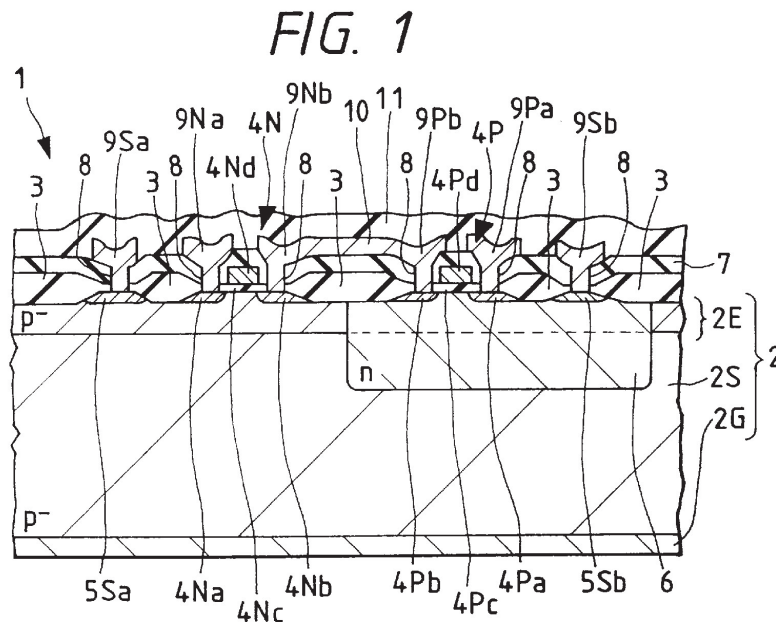


Figure 1 depicts “an essential portion of a semiconductor integrated circuit device” that includes semiconductor substrate body 2S, epitaxial layer 2E, and gettering layer 2G. *Id.* at 6:51–56, Fig. 1. Substrate body 2S and epitaxial layer 2E are doped with a p-type impurity in equal concentrations. *Id.* at 6:60–7:3, 10:51–55, 11:12–16. Embodiment 1 includes n-channel MOS.FET (“nMOS”) 4N and p-channel MOS.FET (“pMOS”) 4P, the latter being formed in n-well 6, which is doped with n-type impurity and extends below the epitaxial layer. *Id.* at 8:46–52, 9:32–40, 11:18–24, 11:43–50, Figs. 1, 5, 7.

Figure 23, reproduced below, depicts a semiconductor device of Embodiment 4 in the process of manufacture. *Id.* at 17:11–13.

FIG. 23

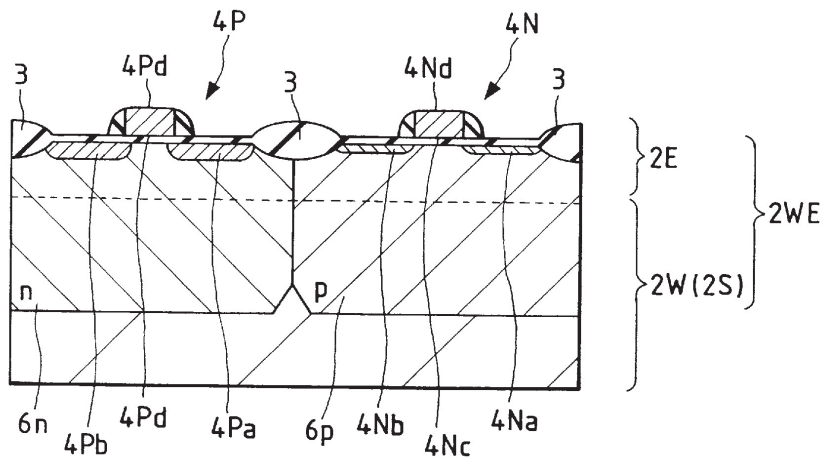


Figure 23 shows a step in a process for manufacturing the semiconductor integrated circuit device of Embodiment 4, including p-well 6p formed with nMOS 4N and n-well 6n formed with pMOS 4P. *Id.* at 6:1–4, 15:26–32, 18:3–35. Substrate body 2S and epitaxial layer 2E are doped with p-type impurity, and the impurity concentration of substrate body 2S is higher than that of epitaxial layer 2E “to improve the resistance to the latchup.” *Id.* at 14:64–15:6, 15:13–17, 16:16–21, 19:59–63, Fig. 17. In Embodiment 4, the impurity concentration in p-well 6p and n-well 6n decreases with increasing depth below the epitaxial layer. *Id.* at 15:62–16:15, 17:55–61, Fig. 17. Kawagoe discloses that the concentration gradient reduces soft errors by attracting carriers (electrons) to the substrate and preventing them from entering the p-well. *Id.* at 16:2–11.

Petitioner relies on Kawagoe Figure 17, which is reproduced below and illustrates properties of the semiconductor device of Embodiment 4.

FIG. 17

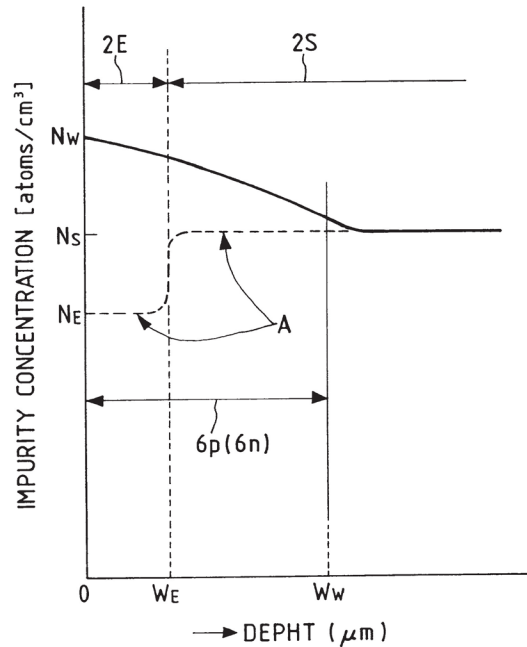


Figure 17 is a plot of impurity concentration as a function of depth in a semiconductor integrated circuit device, which shows “the p-well 6p and n-well 6n have their impurity concentrations gradually lowered in the depthwise direction from the principal surface (having an impurity concentration NW) of the epitaxial layer 2E.” Ex. 1007, 5:41–45, 15:62–16:40.

3. Analysis of Claim 1

Petitioner contends that Kawagoe discloses a semiconductor device as recited in each limitation of claim 1; Petitioner relies on Kawagoe’s Embodiments 1 and 4, both alone and in combination. Pet. 13–30 (citing Ex. 1007, 1:13–23, 1:33–40, 2:57–3:9, 8:40–52, 8:66–67, 9:47–48, 12:8–40, 6:50–7:3, 14:46–15:40, 15:62–16:40, 17:10–18:38, 19:49–63, Figs. 16, 17, 20, 23; Ex. 1003 ¶¶ 72–78, 80, 85, 94; Ex. 1008, 381, 387–89, 406, 419,

523, 530; Ex. 1014, 1:52–54, 2:17–21; Ex. 1026, 1).). In particular, Petitioner contends that Kawagoe Figure 17 discloses dopant concentration in the channel region is “gradually lowered in the depthwise direction from the principal surface (having an impurity concentration NW) of the epitaxial layer 2E” (Pet. 24 (citing Ex. 1007, 15:62–16:40)) and teaches a “graded dopant concentration” that “aid[s] carrier movement from the first surface to the second surface of the substrate,” as recited in claim element 1.5. *Id.* at 25–27. Petitioner relies on Kawagoe’s disclosure that the concentration gradient attracts electrons to substrate body 2S and further contends the downward-sloping dopant concentration in Kawagoe Figure 17 “aids carrier movement from the first surface to the second surface of the substrate to the same extent to which Applicant relied on the prior art and admitted to the Patent Office that such carrier movement would occur under the same scenario.” *Id.* at 27–28 (citing Ex. 1007, 16:2–11; Ex. 1003 ¶ 94). As support for that contention, Petitioner relies on the file history for U.S. Patent No. 8,421,195 (“the parent ’195 patent”) and references cited during examination. *Id.* at 28–30 (citing Ex. 1003 ¶ 94; Exs. 1010, 1016, 1031).

We find that Petitioner’s challenge to claim 1 based on Kawagoe is sufficiently supported for purposes of institution.

Patent Owner argues Petitioner’s Kawagoe-based challenge is deficient because Kawagoe’s disclosure of graded dopant concentration teaches impeding carrier movement rather than aiding it, as required by claim element 1.5. Prelim. Resp. 13–14. Patent Owner relies on Kawagoe’s disclosure that the concentration gradient prevents electrons from entering the p-well. *Id.* at 14 (citing Ex. 1007, 16:7–11). Patent Owner further

argues Kawagoe's carriers are not in the active regions, as required by claim element 1.5. *Id.* at 14–16 (citing Ex. 1003 ¶ 91, n.5).

At this stage of the proceeding, we determine that the arguments and evidence of record favor Petitioner. Both parties agree that a downward-sloping gradient, as disclosed in Kawagoe, will create an electrical field with a force in a direction toward the substrate. *See generally* Prelim. Resp.; Ex. 1007, 16:7–9. Patent Owner does not meaningfully dispute that Kawagoe has a graded dopant concentration in an active region. *See generally* Prelim. Resp. Further, Patent Owner contradictorily stated during prosecution of the '195 patent that a graded dopant concentration itself creates “a built-in electrical field that forces the movement of carriers in a particular direction” (Ex. 1016, 289–290) and is “the additional parameter for ensuring that all minority carriers are being moved in one direction” (*id.* at 290). In light of this evidentiary record, which at most presents a material issue of fact for resolution at trial, we determine Petitioner establishes a reasonable likelihood of prevailing in its challenge of claim 1.

We decline to further discuss the parties' arguments or resolve any disputed issues as to challenges based on Kawagoe on this preliminary record, because the trial in the 1243 IPR is the better proceeding in which to do so. Specifically, as compared to the preliminary phase of this case, the instituted trial in the 1243 IPR affords the parties better opportunity to brief, argue, and develop evidence in support of their positions. Thus, for the same reasons stated in our Decision on Institution in the 1243 IPR, we determine the Petition here warrants institution.

4. *Remaining Claims*

In view of our determination as to claim 1, and because Petitioner's arguments and evidence for claims 2, 4–10, and 12–18 (Pet. 30–38) are similar to Petitioner's arguments and evidence for claim 1 (*id.* at 13–30) and are unopposed at this stage by Patent Owner, we determine that it is unnecessary to provide an explicit analysis of Petitioner's challenges to the remaining claims in order to provide guidance to the parties for the upcoming trial. Consolidated Trial Practice Guide November 2019 ("CTPG")⁷ at 64; *see* 37 C.F.R. § 42.108(a) ("When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim."); *see also SAS Institute Inc. v. Iancu*, 138 S. Ct. at 1359–60 (holding that 35 U.S.C. § 314 forbids the Board's prior "partial institution" practice).

B. *Whether to Join Petitioner as a Party to the 1243 IPR*

Joinder may be authorized when warranted, but the decision to grant joinder is discretionary. *See* 35 U.S.C. § 315(c); 37 C.F.R. § 42.122. A motion for joinder should (1) set forth reasons why joinder is appropriate; (2) identify any new grounds of unpatentability asserted in the petition; (3) explain what impact (if any) joinder would have on the trial schedule for the existing review; and (4) address specifically how briefing and discovery may be simplified. *See, e.g., Kyocera Corp. v. Softview LLC*, IPR2013-00004, Paper 15 (PTAB April 24, 2013). As the moving party, Petitioner bears the burden of proving that it is entitled to the requested relief. 37 C.F.R. § 42.20(c).

⁷ Available at <https://www.uspto.gov/TralPracticeGuideConsolidated>.

As an initial matter, the Motion for Joinder meets the requirements of 37 C.F.R. § 42.122(b) because Petitioner filed it within one month after the 1243 IPR was instituted on February 12, 2024. Mot. 3–4.

Petitioner asserts that the four *Kyocera* factors favor joinder here because Petitioner seeks to join the 1243 IPR in an understudy role. Mot. 4, 6–8. Petitioner explains that the joinder will have no impact on the pending schedule for the 1243 IPR. *Id.* at 6. Petitioner further provides the following conditions it would abide by as long as Semiconductor Components Industries, LLC (“the 1243 Petitioner”) remains an active party to the 1243 IPR:

- (a) [Petitioner] shall not make any substantive filing and shall be bound by the filings of the [1243] Petitioner, unless a filing concerns termination and settlement, or issues solely involving [Petitioner];
- (b) [Petitioner] shall not present any argument or make any presentation at oral hearing unless an issue solely involves [Petitioner], or when addressing Board-approved motions that do not affect the [1243] Petitioner, or its respective position;
- (c) [Petitioner] shall not seek to cross-examine or defend the cross-examination of any witness, unless the topic of cross-examination concerns issues solely involving [Petitioner];
- (d) [Petitioner] shall not seek discovery from Patent Owner on issues not solely involving [Petitioner];
- (e) [Petitioner] will not rely on expert testimony beyond that submitted by the [1243] Petitioner unless the [1243] Petitioner is terminated from the case. If the [1243] Petitioner is not terminated from the case, [Petitioner] agrees to rely entirely on, and be bound by, the expert declarations and depositions in the [1243] IPR. Unless and until the current petitioner in IPR2023-01243 ceases to participate in the instituted [1243] IPR, [Petitioner] will not assume an active role.

Id. at 7–8. Petitioner contends that “due to [Petitioner] taking only an ‘understudy’ role, Patent Owner and the [1243] Petitioner will only need to respond to one principal set of papers, will not require additional time to address additional arguments raised by [Petitioner], and can thus proceed with the existing trial schedule,” and “[t]hese steps will minimize or eliminate any potential complications or delay that could potentially result from joinder.” *Id.* at 8.

Patent Owner argues that Petitioner’s Motion for Joinder should be denied because joinder would be prejudicial to Patent Owner and contrary to public policy favoring settlement. Opp. Mot. Join. 3–5. Patent Owner also argues that joinder is unavailable if Patent Owner prevails on Director Review in the 1243 IPR. *Id.* at 5–8.

Patent Owner’s first argument is not persuasive because it is based on speculation that Petitioner “is trying to block settlement with *any* of these defendants unless [Patent Owner] *also* settles with” Petitioner. Opp. Mot. Join. 5. As discussed below, we determine that Patent Owner will not be prejudiced unduly by the joinder. Moreover, we note that even in a situation where the petitioner and patent owner in the proceeding to be joined had settled (*Code200 v. Bright Data Ltd.*, IPR2022-00861, Paper 17 at 5 (PTAB July 25, 2022) (vacated)), the Director nevertheless vacated a decision to deny a motion for joinder. *Code200 v. Bright Data Ltd.*, IPR2022-00861, Paper 18 at 7 (Office of the Director of the USPTO Aug. 23, 2022) (precedential); *see also eBay, Inc. v. Lexos Media IP, LLC*, IPR2024-00336, Paper 11 at 13–15 (PTAB Feb. 23, 2024).

Patent Owner's second argument is moot because Patent Owner's Request for Director Review has been denied. 1243 IPR, Paper 43 (PTAB Apr. 24, 2024).

Based on the facts and circumstances discussed above, we determine Petitioner has established good cause for joining the 1243 IPR. Specifically, we find that joining Petitioner to the 1243 IPR is unlikely to require any delay or modification to the scheduling order already in place for the 1243 IPR. We also determine that Patent Owner will not be prejudiced unduly by the joinder of this proceeding. Thus, we determine that granting the Motion for Joinder would help "secure the just, speedy, and inexpensive resolution" of these proceedings. *See* 37 C.F.R. § 42.1(b). For the above reasons, we grant Petitioner's Motion for Joinder and join Petitioner as a party to the 1243 IPR.

IV. CONCLUSION

For the reasons given above, we determine that there is a reasonable likelihood that Petitioner would prevail with respect to at least one of the claims challenged in the Petition. Accordingly, we institute an *inter partes* review of all challenged claims based on the grounds asserted in the Petition. In addition, we grant Petitioner's Motion for Joinder. Patent Owner's argument that the Petition is time-barred under 35 U.S.C. § 315(b) is moot because it is accompanied by a request for joinder to an instituted proceeding, which we grant.

V. ORDER

For the reasons given, it is

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review is hereby instituted as to claims 1–18 of the ’842 patent on the grounds set forth in the Petition;

FURTHER ORDERED that Petitioner’s Motion for Joinder is *granted*, and Petitioner is joined as a petitioner in IPR2023-01243;

FURTHER ORDERED that Petitioner shall have an “understudy” role in the IPR2023-01243 under the conditions reproduced above (*see* Mot. 7–8);

FURTHER ORDERED that all further filings in the joined proceeding shall be made in IPR2023-01243, and that no further filings shall be made in IPR2024-00672;

FURTHER ORDERED that the Scheduling Order in IPR2023-01243 remains unchanged, and shall govern the joined proceeding;

FURTHER ORDERED that a copy of this Decision shall be entered in IPR2023-01243; and

FURTHER ORDERED that the case caption in IPR2023-01243 shall be modified to reflect Petitioner’s joinder in accordance with the attached example;

FURTHER ORDERED that after conferring with Petitioner, Patent Owner shall, within one week of this Decision, submit to the Board via email to Trials@uspto.gov, a version of this Decision to be filed on the public record, with any redactions proposed by either party.

IPR2024-00672
Patent 10,510,842 B2

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Example Caption for Joined Proceeding

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC and
TEXAS INSTRUMENTS INCORPORATED,
Petitioner,

v.

GREENTHREAD, LLC,
Patent Owner.

IPR2023-01243¹
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¹ Texas Instruments Incorporated, which filed a petition in IPR2024-00672, has been joined as a petitioner in this proceeding.