

WHAT IS CLAIMED IS:

1. A semiconductor device with graded dopant concentration in the active region, to aid carrier movement from emitter to collector.
2. A semiconductor device with graded dopant concentration in the active region, to aid carrier movement from source to drain.
3. A semiconductor device with graded dopant concentration in the well regions, to aid carrier movement away from the active surface regions, towards the substrate.
4. A semiconductor device with graded dopant concentration in the substrate region to aid carrier movement away from the active surface regions, deeper towards the substrate.
5. A semiconductor device with at least one each of dopant concentration of both donor and acceptor, to optimize the operating performance of the device.
6. A semiconductor device with at least one graded dopant concentration fabricated with ion implantation, to provide an aiding or retarding electric field locally in a monolithic integrated circuit.
7. A semiconductor device with at least one graded dopant concentration in an epitaxial layer.
8. A semiconductor device where one layer of dopant from one wafer, is transferred to another wafer having either same polarity or different polarity dopant through wafer bonding or similar processes.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Inventor : G. R. Mohan Rao
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Title : SEMICONDUCTOR DEVICES WITH GRADED
DOPANT REGIONS
Docket No. : 0299-0001.04

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Sir:

Please amend the above-identified application as follows:

Amendments to the Specification begin on page 2 of this amendment;

Amendments to the Drawings begin on page 11 of this amendment and include attached replacement sheets;

Amendments to the Claims are reflected in the listing of claims which begins on page 12 of this amendment; and

Remarks begin on page 17 of this amendment.

Amendments to the Specification:

Please replace paragraph [0001] with the following amended paragraph:

[0001] This application is a continuation of U.S. Application Serial No. 11/622,496, filed January 12, 2007, which application is incorporated herein by reference.

Please replace paragraph [0003] with the following amended paragraph:

[0003] Bipolar Junction transistors Transistors (BJT) are classified as minority carrier devices [[as]] because minority carriers are the principle device conduction mechanism. However, majority carriers also play a small [[yet]] but finite role in modulating the conductivity in BJTs. Consequently, both carriers (electrons and holes) play a role in the switching performance of BJTs. The maximum frequency of operation in BJTs is limited by the base transit time as well as the quick recombination of the majority carriers when the device is switched off (prior to beginning the next cycle). The dominant carrier mechanism in BJTs is carrier diffusion. The ~~Carrier carrier~~ drift current component is fairly small, especially in uniformly doped base BJTs. Efforts have been made in graded base transistors to create an [[']] aiding drift field [[']] [[,]] to enhance the diffusing minority carrier's speed from emitter to collector. However, most semiconductor devices, including various power MOSFETs (traditional, DMOS, lateral, vertical and a host of other configurations), IGBTs (Insulated Gated Base Transistors), still use a uniformly doped drift epitaxial region in the base. FIG. 1 shows the relative doping concentration versus distance in a BJT. FIG. 2 shows the [[']] uniformly doped epi region [[']] in [[a]] an IGBT. In contrast to BJTs, MOS devices are majority carrier devices for conduction. The conduction is channel dominated. The channel can be a surface in one plane in planar devices. The surface can also be on the sidewalls in a vertical device. Other device architectures to combine planar and vertical conductions are also possible. The maximum frequency of

operation is dictated primarily by source-drain separation distance. Most MOS devices use a uniformly doped substrate (or a well region). When a MOSFET is optimally integrated with a BJT in a monolithic fashion, an IGBT results. The IGBT inherits the advantages of both MOSFET and BJT. It also brings new challenges because the required characteristics (electron transit and hole recombination as fast as possible in the case of an n-channel IGBT) require necessitate different dopant gradients either in the same layer at different positions, or at the interfaces of similar or dissimilar layers.

Please replace paragraph [0004] with the following amended paragraph:

[0004] Retrograde wells have been attempted, with little success, to help improve soft error immunity in SRAMs and visual quality in imaging circuits. FIG. 3(a) shows a typical CMOS VLSI device employing a twin well substrate, on which active devices are subsequently fabricated. FIGS. 3(b), 3(c), and 3(d) illustrate device cross sections, as practiced today. Retrograde and halo wells have also been attempted to improve refresh time in DRAMs (dynamic random-access random-access memories), as well as, reducing dark current (background noise) and enhance RGB (Red, Green, Blue) color resolution in digital camera ICs. Most of these techniques either divert the minority carriers away from the active regions of critical charge storage nodes at the surface, or, increase minority carrier density locally as the particular application requires.

Please replace paragraph [0006] with the following amended paragraph:

[0006] ~~FIGURE 1~~ FIG. 1 illustrates the relative doping profiles of emitter, base, and collector for the two most popular bipolar junction transistors: namely, uniform base ("A") and graded base ("B");

Please replace paragraph [0008] with the following amended paragraph:

[0008] FIGURES ~~FIGS.~~ 3(a), 3(b), 3(c), and 3(d) illustrate cross sections of commonly used prior art CMOS silicon substrate substrates; FIG. 3(a) showing a typical prior art IC with two wells (one ~~n-well~~ n⁻well in which p-channel transistors are subsequently fabricated ~~[[,]]~~ and ~~[[,]]~~ one ~~p-well~~ p⁻well in which n-channel transistors are subsequently fabricated); ~~—typical IC, EEPROM using tunnel insulator, DRAM and NAND flash;~~ FIG. 3(b) showing a prior art EEPROM (Electrically Erasable Programmable Read-Only Memory) memory cell having a tunnel insulator; FIG. 3(c) showing a prior art DRAM memory cell; and FIG. 3(d) showing a prior art NAND flash memory cell;

Please replace paragraph [0009] with the following amended paragraph:

[0009] ~~FIGURE~~ FIG. 4 illustrates the cross section of ~~[[a]]~~ an IGBT, using one embodiment of the invention described here, where the dopant is optimally graded in the ~~epitaxial~~ epitaxial drift region; ~~[[and]]~~

Please replace paragraph [0010] with the following amended paragraph:

[0010] FIGURES ~~FIGS.~~ 5(a), 5(b), and 5(c) illustrate the cross sections of a ~~[[MOS]]~~ CMOS silicon substrate with two wells~~[[,]]~~ and ~~[[,]]~~ an underlying layer using embodiments of the invention to improve performance in each application – VLSI logic, DRAM/image IC, nonvolatile memory IC ~~[[.]]~~;

Please replace paragraph [0011] with the following amended paragraph:

[0011] ~~FIGURE~~ FIG. 6 shows a typical CMOS integrated circuit. The p-channel transistor is situated (fabricated) in an n-well n⁻well, while the n-channel transistor is situated in a ~~p-well~~

p⁻well. The wells are separated by a STI (~~Shallow Trench~~ Trench Isolation Isolation) for isolation. This is a typical structure for a CMOS VLSI IC fabricated on a uniformly doped ~~p⁻ or n⁻~~ substrate p⁻ or n⁻ substrate. As one embodiment of the invention, each of the n-well n⁻well and p-well p⁻well have has their respective graded dopants in the well regions. The ~~n-well~~ n⁻well has a graded dopant to 'sweep' "sweep" away the holes from the surface towards the ~~interface~~ interfaces of the n-well n⁻well and the uniformly doped substrate. As an exemplary performance improvement of the switching time of the p-channel transistor, its 'off' "off" time will be significantly improved. With an analogous graded dopant in the ~~p-well~~ p⁻well, the n-channel transistor's switching performance can also be improved. A DRAM memory cell ~~which~~ dynamically holds ~~change~~ an electrical charge, for example in a ~~p-well~~ p⁻well with graded dopant, can have an improved refresh time characteristic.

Please replace paragraph [0012] with the following amended paragraph:

[0012] ~~FIGURE~~ FIG. 7 shows another embodiment using graded dopants to improve the performance characteristics of transistors in a CMOS integrated circuit. Whereas the embodiment in FIG 6, is fabricated on a uniformly doped ~~'bulk'~~ "bulk" silicon substrate (as is commonly known in the semiconductor industry), the embodiment of FIG 7, has an '~~epitaxial substrate~~' "epitaxial substrate". This epitaxial substrate is approximately 1-3 microns thick ~~[[,]]~~ and ~~[[,]]~~ is the top layer for a 50-300 microns thick bulk substrate. ~~Some of~~ ~~[[The]]~~ the ~~advantage~~ advantages of graded dopant epitaxial silicon is its superior minority carrier lifetime and ~~the creating creation of~~ an electric field for minority carrier sweep. Superior minority carrier life time can enhance refresh time in a DRAM, or reduce programming time in a flash memory. Whereas the wells (both ~~p-well~~ p⁻well and ~~n-well~~ n⁻well) in FIG 6, are fabricated with graded

dopants, the wells in FIG 7. are fabricated with commonly known practices in the industry. Such commonly known practices may include ~~'hollow ion implantations'~~ "halo ion implantations" that are localized in the well regions[[,]] but [[,]] they do not constitute 'graded dopants' "graded dopants" as described in the present disclosure ~~invention here with.~~

Please replace paragraph [0013] with the following amended paragraph:

[0013] ~~FIGURE~~ FIG. 8 shows another embodiment practicing the graded dopant invention for a CMOS IC. The wells contain 2-way graded dopant: namely, an ~~'aiding electric field'~~ "aiding electric field" on the top of the well, and a ~~'retarding electric field'~~ "retarding electric field" at the bottom of the well. The aiding and retarding electric fields are for the respective minority carriers (holes and electrons).

Please replace paragraph [0014] with the following amended paragraph:

[0014] ~~FIGURE~~ FIG. 9 shows another embodiment practicing the 2-way graded dopant for the ~~epitaxial~~ epitaxial substrate. The aiding and retarding electric fields can also help sweep minority carriers into the substrate and thus increase immunity to ~~'soft errors'~~ "soft errors". Soft errors due to ~~(transient)~~ radiation ~~(transient)~~ is well known in CMOS ~~[[IC's]]~~ ICs.

Please replace paragraph [0016] with the following amended paragraph:

[0016] ~~FIGURE~~ FIG. 14 shows another embodiment where the CMOS IC is a microcontroller mounted on a photovoltaic panel. Both the CMOS controller and the photovoltaic panel are fabricated employing graded dopant concepts described ~~herewith~~ herein. The microcontroller can be used for optimizing power management for the PV panel. The CMOS microcontroller can be entirely powered by the PV ~~[[-]]~~ panel, which could be operated on solar energy.

Please replace paragraph [0017] with the following amended paragraph:

[0017] ~~FIGURE FIG.~~ FIG. 15 shows another embodiment where a power device is mounted on the ~~PV-panel~~ PV panel. The power device can be a ~~'boosting device'~~ "boosting device" (for voltage and/or current) or a ~~'switching device'~~ "switching device" (like IGBT-insulated gate bipolar transistor) providing dynamic clocked power. This module – ~~PV-panel~~ PV panel mounted with power device – could be a ~~'solar'~~ "solar" to ~~[['ac']]~~ "ac" (alternating current) provider/converter. Both of them employ graded dopants.

Please replace paragraph [0018] with the following amended paragraph:

[0018] ~~FIGURE FIG.~~ FIG. 16 shows an embodiment where a ~~PV-panel~~ PV panel, a microcontroller, and a power device – all employing ~~grade~~ graded dopants – to provide an integrated power conversion module from ~~'solar'~~ "solar" to ~~[['ac']]~~ "ac".

Please replace paragraph [0019] with the following amended paragraph:

[0019] The relative doping concentrations of emitter and collector regions varies from 10^{18} to $10^{20}/\text{cm}^3$, ~~where as~~ whereas the base region is 10^{14} to $10^{16}/\text{cm}^3$ depending on the desired characteristics of the BJT. In graded base p-n-p transistors, the donor dopant concentration may be 10 to 100 x at the emitter-base junction, relative to the base-collector junction (1x). The gradient can be linear, quasi linear, exponential or complimentary error function. The relative slope of the donor concentration throughout the base ~~[[,]]~~ creates a suitable aiding drift electric field, to help the holes (p-n-p transistor) transverse from emitter to collector. Since the aiding drift electric field helps hole conduction, the current gain at a given frequency is enhanced, relative to a uniformly-doped ~~[[-]]~~ (base) BJT. The improvement in cut-off frequency (or,

frequency at unity gain, f_T) can be as large as 2x-5x. Similar performance improvements are also applicable to n-p-n transistors.

Please replace paragraph [0020] with the following amended paragraph:

[0020] As illustrated in FIG. 4, in one embodiment according to the invention, a donor gradient is established from the emitter-drift epitaxial base region junction of the punch-through IGBT, to the drift epitaxial base region – $[[n^+]]$ n^+ buffer layer boundary (electrons in this case are accelerated in their transit from emitter to collector). The 'average' "average" base resistance is optimized $[[,]]$ so that conductivity modulation and lifetime (for minority carriers) in the base region are not compromised. By sweeping the carriers towards the $[[n^+]]$ n^+ buffer region $[[two]]$ a number of advantages are obtained. $[[-]]$ First, the frequency of operation (combination of t_{on} and t_{off} as is known in the IGBT commercial nomenclature) can be enhanced. Second, and maybe More more importantly, during t_{off} holes can be recombined much quicker at the $[[n^+]]$ n^+ buffer layer, compared to $[[a]]$ the uniformly doped n^{++} epitaxial drift region by establishing a different dopant gradient near the n^+ buffer layer. It should be noted that the drift region can also be a non-epitaxial silicon substrate. Although Epitaxy epitaxy enhances lifetime, but, epitaxy it is not mandatory. Different layers of ~~dopan~~ dopant regions can be transferred through wafer to wafer bonding (or other similar transfer mechanisms) for eventual device fabrication. The "reverse recovery time" for an IGBT is significantly improved due to the optimized graded dopant in the so called "drift region" as well as at the interfaces of the drift region. Graded dopants can also be implemented in the n^+ buffer layer as well as other regions adjacent to the respective layers. Two important performance enhancements are the result of dopant gradients. For example, in an n-channel IGBT, electrons can be swept from source to drain rapidly, while at

the same time holes can be recombined closer to the n^+ buffer layer. This can improve t_{on} and t_{off} in the same device.

Please replace paragraph [0021] with the following amended paragraph:

[0021] As illustrated in FIGS. 5(a), 5(b), and 5(c), donor gradient is also of benefit to very large scale integrated circuits (VLSI) – VLSI logic, DRAM, nonvolatile memory like NAND flash. Spurious minority carriers can be generated by clock switching in digital VLSI logic and memory ~~[[IC'S]] ICs~~. These unwanted carriers can discharge dynamically-held 'actively-held high' "actively held high" nodes. In most cases, Statically statically held nodes (with V_{CC}) ~~can~~ not ~~cannot~~ be affected, ~~in most cases~~. Degradation of refresh time in ~~DRAM's~~ DRAMs is one of the results, because the capacitor holds charge dynamically. Similarly, degradation of CMOS digital images ~~[[,]]~~ in digital imaging ~~[[IC's]] ICs~~ is another result of the havoc caused by minority carriers. Pixel and color resolution can be significantly enhanced in imaging ~~[[IC's]]~~ ICs with the embodiments described ~~here~~ herein. Creating 'Sub-Terrain' "subterranean" recombination centers underneath the wells (gold doping, platinum doping) as is done in some high-voltage diodes is not practical for VLSI circuits. Hence, a novel technique ~~has been~~ is described ~~here~~ herein ~~by creating which creates~~ a drift field to sweep these unwanted minority carriers ~~from the active circuitry at the surface~~ into the substrate as quickly as possible, ~~from the active circuitry at the surface~~. In a preferred embodiment, the ~~subterrain~~ subterranean n-layer has a graded donor concentration to sweep the minority carriers deep into the substrate. One or more of such layers can also be implemented through wafer to wafer bonding or similar "transfer" mechanisms. This n-layer can be a deeply-implemented layer. It can also be an epitaxial layer. As desired, ~~[[The]] the~~ n-well and p-well also can be graded or retrograded in dopants, ~~as desired,~~ to sweep those carriers away from the surface as well. The graded dopant can also be

implemented in surface channel MOS devices to accelerate majority carriers towards the drain. ~~To decrease programming time~~ [[In]] in nonvolatile memory devices, ~~to decrease programming time,~~ carriers should be accelerated towards the surface when programming of memory cells is executed. The graded dopant can also be used to fabricate superior Junction ~~field-effect~~ Field-Effect transistors where the “channel ~~pinchoff~~ pinch-off” is controlled by a graded channel instead of a uniformly doped channel (as practiced in the prior art).

Please replace paragraph [0022] with the following amended paragraph:

[0022] One of ordinary skill and familiarity in the art will recognize that the concepts taught herein can be customized and tailored to a particular application in many advantageous ways. For instance, minority carriers can be channeled to the surface [[,]] to aid programming in nonvolatile memory devices (NOR, NAND, multivalued-cell). Moreover, ~~single-well~~ single-well, ~~as-well and~~ triple-well CMOS fabrication techniques can also be optimized to incorporate these embodiments [[,]] individually and collectively. Any modifications of such embodiments (described here) fall within the spirit and scope of the invention. Hence, they fall within the scope of the claims described below.

Amendments to the Drawings:

The attached sheets of drawings include changes to Figs. 1-16 (all Figures). The sheets replace all of the original drawing sheets, including Figs. 1-16. The amendments made to the drawings are limited to improving readability and to correcting editorial problems, such as typos. No substantive changes have been made and no new matter has been added.

Attachment: Replacement Sheets for Figures 1-16 (one figure per sheet)

Amendments to the Claims:

The listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-8 (Cancelled)

9. (Newly Added) A semiconductor device comprising:

a surface layer;

a substrate;

an active region including at least one emitter, at least one base and at least one collector disposed in the above said device;

at least one drift layer positioned between said emitter and said collector, said drift layer having at least one graded concentration of dopants, said drift layer further having a first static unidirectional electric field to aid movement of carriers from said emitter to said collector; and

at least one isolation region disposed in the semiconductor device, said isolation region having a graded concentration of dopants and a second static unidirectional electric field to aid isolation between active regions.

10. (Newly Added) The semiconductor device of claim 9 wherein said static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions.

11. (Newly Added) A semiconductor device comprising:

- at least one active region with a channel conduction surface;
- at least one active device with a vertical conduction;
- a first static unidirectional electric field in said channel conducting region; said first unidirectional electric field having a graded dopant concentration;
- a second static unidirectional electric field in said vertical conduction; said second static unidirectional electric field having a graded dopant concentration; and
- a third static unidirectional electric field; said third static unidirectional electric field having a graded dopant concentration.

12. (Newly Added) The semiconductor device of claim 9 wherein the semiconductor device is a silicon substrate.

13. (Newly Added) The semiconductor device of claim 9 wherein the semiconductor device is an III-V compound substrate.

14. (Newly Added) The semiconductor device of claim 9 wherein the semiconductor device is an II-VI compound substrate.

15. (Newly Added) The semiconductor device of claim 9 wherein the semiconductor device is an organic material substrate.

16. (Newly Added) The semiconductor device of claim 9 wherein the semiconductor device is a silicon carbide substrate.

17. (Newly Added) The semiconductor device of claim 9 wherein the semiconductor device has at least one bipolar transistor.

18. (Newly Added) The semiconductor device of claim 9 wherein the semiconductor device has at least one vertical bipolar transistor.

19. (Newly Added) The semiconductor device of claim 9 wherein the semiconductor device has at least one planar bipolar transistor with a conducting surface layer.

20. (Newly Added) The semiconductor device of claim 9 wherein the semiconductor device has at least one MOS transistor.

21. (Newly Added) The semiconductor device of claim 9 wherein the semiconductor device has at least one IGBT.

22. (Newly Added) A semiconductor device comprising:

a substrate;

a surface layer;

an active region including at least one emitter and one collector disposed in the device;

a single drift layer disposed between said emitter and said collector, said drift layer having at least one graded concentration of dopants, said drift layer further having a first static unidirectional electric field to aid movement of carriers from said emitter to said collector; and

at least one isolation region disposed in the semiconductor device, said isolation region having a graded concentration of dopants and a second static unidirectional electric field to aid movement of carriers.

23. (Newly Added) The semiconductor device of claim 22 wherein the semiconductor device is a varactor.

24. (Newly Added) The semiconductor device of claim 22 wherein the semiconductor device is a varistor.

25. (Newly Added) The semiconductor device of claim 22 wherein the semiconductor device is an avalanche transistor.

26. (Newly Added) The semiconductor device of claim 22 wherein the semiconductor device is a Zener diode.

27. (Newly Added) The semiconductor device of claim 22 wherein the semiconductor device is a Schottky diode.

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28. (Newly Added) The semiconductor device of claim 22 wherein the semiconductor device is a tunneling diode.

29. (Newly Added) The semiconductor device of claim 22 wherein the semiconductor device is an Esaki diode.

REMARKS

In the specification, the paragraphs [0001], [0003], [0004], [0006], [0008] - [0014], and [0016] - [0022] have been amended to correct editorial problems. The amendments do not contain any new matter.

In amended Figs. 1-16 (all figures) amendments have been made to improve the readability and to correct editorial problems, such as typos. No substantive changes have been made and no new matter has been added.

Applicant has cancelled claims 1-8 and added new claims 9-29.

The Commissioner is authorized to charge any additional fees or deficiencies or credit any overpayments to Eugene M. Cummings, P.C., Deposit Account No. **50-4199**, with reference to attorney docket number (0299-0001.04).

Respectfully submitted,

Law Offices of Eugene M. Cummings P.C.

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By: /David M. Mundt/
David M. Mundt, Reg. No. 41,207
Law Offices of Eugene M. Cummings, P.C.
1 North Wacker Drive, Suite 4130
Chicago, Illinois 60606
Telephone: (312) 984-0144
Facsimile: (312) 984-0146