

Microelectronic Circuit Design



WCB/McGraw-Hill

A Division of The McGraw-Hill Companies

MICROELECTRONIC CIRCUIT DESIGN

Copyright © 1997 by The McGraw-Hill Companies, Inc. All rights reserved. Printed in the United States of America. Except as permitted under the United States Copyright Act of 1976, no part of this publication may be reproduced or distributed in any form or by any means, or stored in a data base or retrieval system, without the prior written permission of the Publisher.

This book is printed on acid-free paper.

3 4 5 6 7 8 9 DOW DOW 9 0 3 2 1 0 9 8 7

ISBN 0-07-032482-4

This book was set in Times Roman by Publication Services.
The editor was Lynn B. Cox; the editing supervisor was Eva Marie Strock;
the interior designer was Mel Haber;
the cover designer was Francis Owens;
the production supervisor was Natalie Durbin.
R. R. Donnelley & Sons, Wilard, was the printer and binder.

Library of Congress Cataloging-in-Publication Data

Jaeger, Richard C.

Microelectronic circuit design / Richard C. Jaeger.

p. cm. — (McGraw-Hill series in electrical and computer engineering)

Includes bibliographical references and index.

ISBN 0-07-032482-4

1. Integrated circuits—Design and construction.

2. Semiconductors—Design and construction. 3. Electronic circuit design. I. Title. II. Series.

TK7874.J333 1996

621.3815—dc20

96-26208

CIP

INTERNATIONAL EDITION

Copyright 1997. Exclusive rights by The McGraw-Hill Companies, Inc. for manufacture and export. This book cannot be re-exported from the country to which it is consigned by McGraw-Hill. The International Edition is not available in North America.

When ordering this title, use ISBN 0-07-114386-6

<http://www.mhhe.com>

Chapter 4 explores the characteristics of **field-effect transistors (FETs)**. The **metal-oxide-semiconductor field-effect transistor (MOSFET)** is without doubt the most commercially successful solid-state device. It is the primary component in high-density VLSI chips, including microprocessors and memories. A second type of FET, the **junction field-effect transistor (JFET)**, is based on a *pn* junction structure.

P-channel MOS (PMOS) transistors were the first MOS devices to be successfully fabricated in large-scale integrated circuits (LSI). The first microprocessor chips used PMOS technology. Greater performance was later obtained with the commercial introduction of **n-channel MOS (NMOS) technology** in both enhancement-mode and depletion-mode devices.

This chapter discusses the qualitative and quantitative *i-v* behavior of MOSFETs and JFETs and investigates the differences between the various types of transistors. Techniques for biasing the transistors in various regions of operation are also presented.

4.1 CHARACTERISTICS OF THE MOS CAPACITOR

At the heart of the MOSFET is the **MOS capacitor** structure depicted in Fig. 4.1. The top electrode of the MOS capacitor is formed of a metal, typically aluminum or heavily doped polysilicon (polycrystalline silicon). We refer to this electrode as the **gate (*G*)** for reasons that will become apparent shortly. A thin insulating layer, typically silicon dioxide, isolates the metal gate from the substrate or body—the semiconductor region that acts as the second electrode of the capacitor. Silicon dioxide is a stable, high-quality electrical insulator readily formed by thermal oxidation of the silicon substrate. The ability to form this high-quality insulator is one of the basic reasons that silicon is the dominant semiconductor material today. The semiconductor region may be *n*-type or *p*-type, as in Fig. 4.1.

The qualitative behavior of the MOS capacitor is the basis for operation of the MOSFET. The semiconductor forming the bottom electrode of the capacitor has a substantial resistivity and a limited supply of holes and electrons. Because the semiconductor therefore can be depleted of carriers, as discussed in Chapter 2, the capacitance of this structure is a nonlinear function of voltage v_G . Figure 4.2 shows the conditions in the region of the substrate immediately below the gate electrode for three different bias voltages.

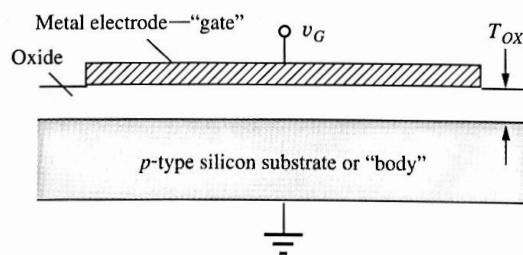


Figure 4.1 MOS capacitor structure on *p*-type silicon.

Accumulation Region

The situation for a large negative bias on the gate with respect to the substrate is depicted in Fig. 4.2(a). The large negative charge on the metal plate is balanced by holes attracted to the silicon-silicon dioxide interface directly below the gate. For the bias condition shown, the hole density at the surface exceeds that which is present in the original *p*-type substrate, and the surface is said to be operating in the **accumulation region** or just in **accumulation**.

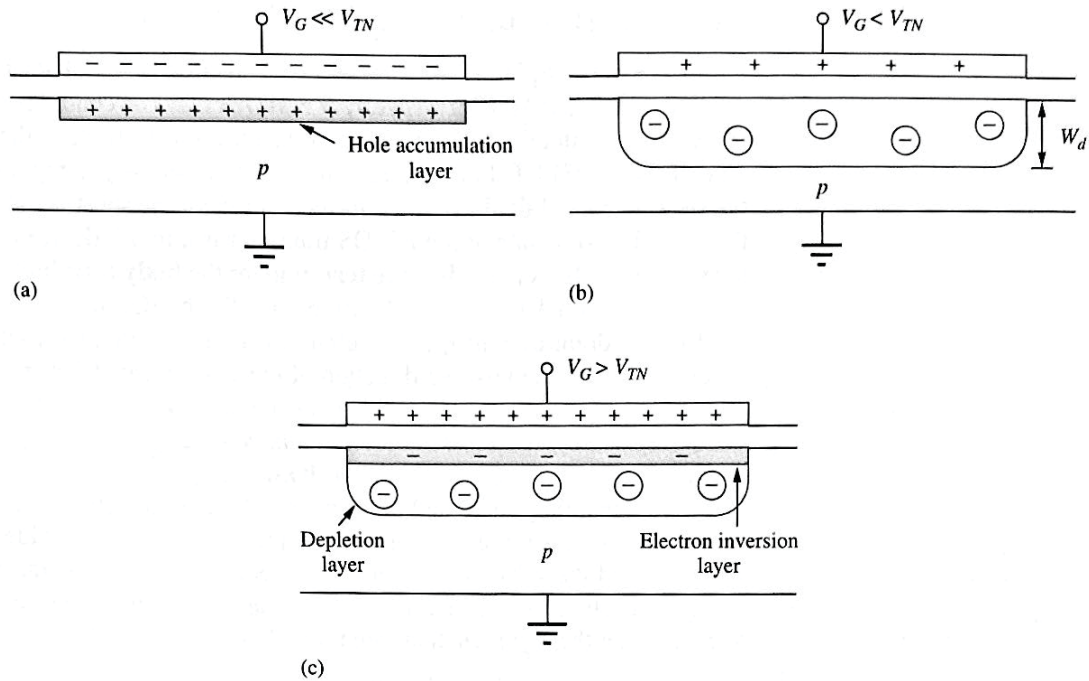


Figure 4.2 MOS capacitor operating in (a) accumulation, (b) depletion, (c) inversion.

This accumulation layer is extremely shallow, existing primarily as a charge sheet directly below the gate.

Depletion Region

Now consider the situation as the gate voltage is slowly increased. First, holes are repelled from the surface. Eventually, the hole density near the surface is reduced below the majority-carrier level set by the substrate doping level, as depicted in Fig. 4.2(b). This condition is called **depletion** and the region, the **depletion region**. The region beneath the metal electrode is depleted of free carriers in much the same way as the depletion region that exists near the metallurgical junction of the *pn* junction diode. In Fig. 4.2(b), positive charge on the gate electrode is balanced by the negative charge of the ionized acceptor atoms in the depletion layer. The depletion-region width w_d can range from a fraction of a micron to many tens of microns depending on the applied voltage and substrate doping levels.

Inversion Region

As the voltage on the top electrode increases further, electrons are attracted to the surface. At some voltage level, the electron density at the surface will exceed the hole density. At this voltage, the surface has inverted polarity from the *p*-type of the original substrate to an *n*-type **inversion layer**, or **inversion region**, directly underneath the top plate. This inversion region is an extremely shallow layer, existing primarily as a charge sheet directly below the gate. The high density of electrons in the inversion layer is supplied by the electron-hole generation process within the depletion layer.

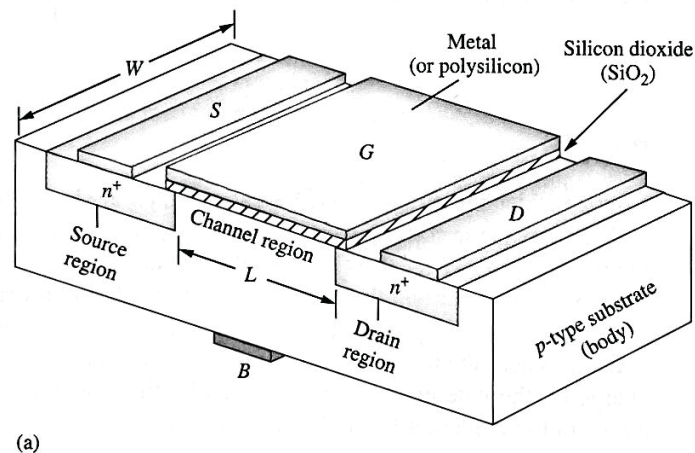
The positive charge on the gate is balanced by the combination of negative charge in the inversion layer plus negative ionic acceptor charge in the depletion layer. The voltage at which the surface inversion layer forms plays an extremely important role in field-effect transistors and is called the **threshold voltage** V_{TN} .

4.2 STRUCTURE OF THE NMOS TRANSISTOR

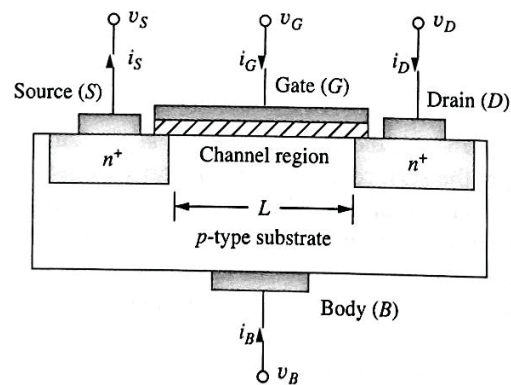
Figure 4.3 shows a plan view, cross section, and circuit symbol of an *n*-channel MOSFET, usually called an **NMOS transistor**, or **NMOSFET**. The central region of the MOSFET is the MOS capacitor discussed in Sec. 4.1, and the top electrode of the capacitor is called the **gate** of the MOSFET. In addition, two heavily doped *n*-type regions (n^+ regions), called the **source** (*S*) and **drain** (*D*), are formed in the *p*-type substrate aligned with the edge of the gate. The substrate of the NMOS transistor is a fourth device terminal and is referred to synonymously as the **substrate terminal**, or the **body terminal** (*B*).

The terminal voltages and currents for the NMOS device are also defined in Fig. 4.3(b). The drain current i_D , source current i_S , gate current i_G , and body current i_B are all defined, with the positive direction of current indicated for an NMOS transistor. The important terminal voltages are the gate-source voltage $v_{GS} = v_G - v_S$, the drain-source voltage $v_{DS} = v_D - v_S$, and the source-bulk voltage $v_{SB} = v_S - v_B$. These voltages are all ≥ 0 during normal operation of the NMOSFET.

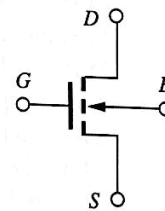
Note that the source and drain regions form *pn* junctions with the substrate. These two junctions are kept reverse-biased at all times in order to provide isolation between the junctions and the substrate as well as between adjacent MOS transistors. Thus, the bulk voltage must be less than or equal to the voltages applied to the source and drain terminals to ensure that these *pn* junctions are properly reverse-biased.



(a)



(b)



(c)

Figure 4.3 (a) NMOS transistor structure; (b) cross section; and (c) circuit symbol.