

CMOS Active Pixel Image Sensors Fabricated Using a 1.8-V, 0.25- μm CMOS Technology

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Abstract—This paper reports the experimental results of the first CMOS active pixel image sensors (APS) fabricated using a high-performance 1.8-V, 0.25- μm CMOS logic technology. No process modifications were made to the CMOS logic technology so that the impact of device scaling on the image sensing performance can be studied. This paper highlights the device and process design considerations required to enable CMOS as an image sensor technology.

I. INTRODUCTION

CMOS active pixel image sensors (APS) have attracted much attention in the past few years [1]–[5]. The advantages of CMOS imagers are

- 1) low-voltage operation and low-power consumption,
- 2) compatibility with on-chip electronics integration (control logic and timing, image processing, signal-conditioning such as CDS and A/D conversion)
- 3) random access of the image data, and
- 4) potentially lower cost as compared to the conventional CCD.

Most of the experimental work on CMOS imagers to date (Fig. 1, [2]) employed relatively mature foundry CMOS technologies (groundrules $\geq 0.5 \mu\text{m}$, power supply $\geq 5 \text{ V}$) without process modifications. The success of earlier CMOS image sensor work was based partly on the similarity of older CMOS technologies and CCD technologies in key areas such as contact and isolation technologies, junction depths, and gate oxide thickness. The expectation has been that the imaging performances would be preserved with device down-scaling. However, CMOS device designs for fully-scaled sub-0.25- μm technologies [6] differ substantially from older generations. Recent analyses [7] also indicated that it is important to examine the impact of CMOS device and technology scaling on CMOS image sensor performances. This paper reports the experimental results of the first CMOS active pixel image sensors fabricated using a high-performance 1.8-V, 0.25- μm CMOS logic technology. The pixels are $7 \mu\text{m} \times 7 \mu\text{m}$, with a 33% fill factor.

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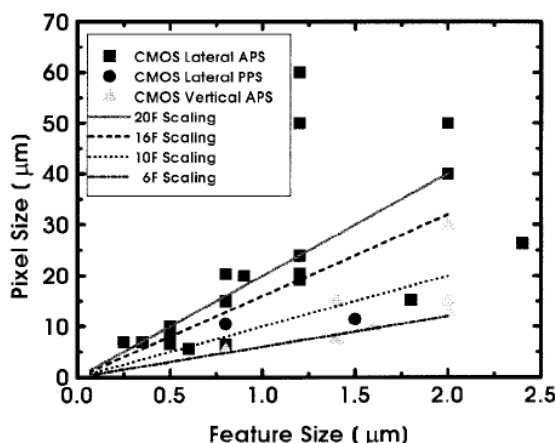


Fig. 1. Historical scaling trend of CMOS active pixel image sensor pixel sizes. APS = active pixel sensor. PPS = passive pixel sensor. Vertical APS refers to pixels that use vertical device structures to perform active functions (e.g., CMD, BCMD). The upper solid line shows pixel size scaling as $20F$ (typical of 4-transistor photogate and photodiode designs), and the lower dotted line shows pixel size scaling as $10F$ (typical of 3-transistor photodiode designs). F is the minimum lithographic feature size.

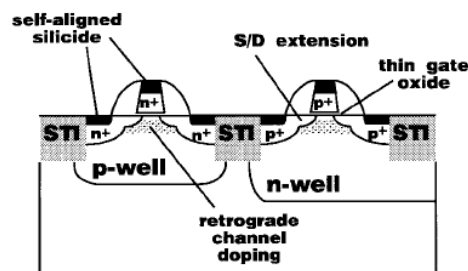


Fig. 2. Schematic device cross section which illustrates key device and technology features (adapted from [5]).

II. TECHNOLOGY

The technology is typical of high-performance CMOS logic [6], [8] scaled from earlier CMOS generations [9]. Design groundrules employed in the pixel design were $0.35 \mu\text{m}$. Device design [8] (Fig. 2) features 1.8-V power supply, 4-nm gate oxide, $0.12\text{-}\mu\text{m}$ nFET effective channel length, retrograde channel doping by high-energy implants, ultra-shallow source/drain extensions to control short-channel effects, self-aligned silicide gate and source/drain to reduce resistances, shallow trench isolation (STI), tungsten-filled-trench (damascene) local interconnect, and tight-pitched borderless contacts. All the technology features described above depart

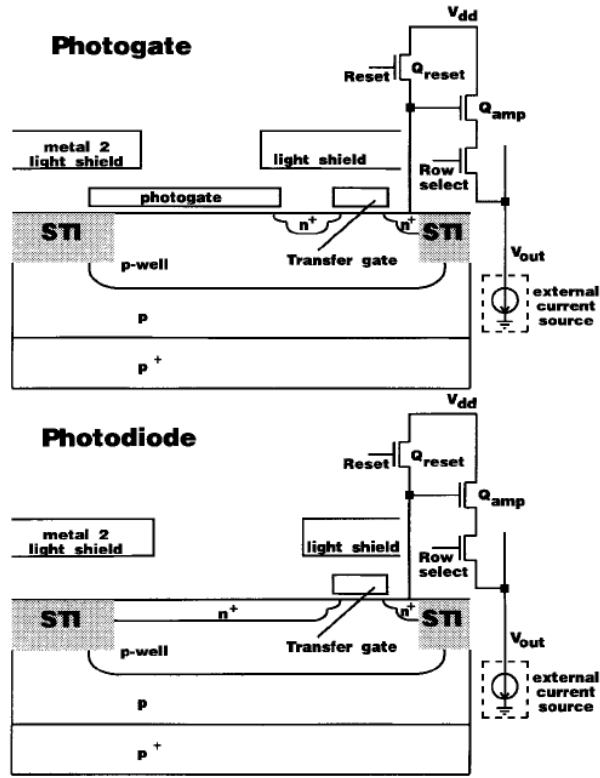


Fig. 3. Pixel circuit and device schematic.

substantially from earlier 5-V CMOS generations, and are totally different from CCD technologies (typical power supply of 8–15 V).

III. EXPERIMENTAL RESULTS

Conventional four-transistor photogate and photodiode type pixels with in-pixel reset switch, transfer gate, select switch, and source follower amplifier were fabricated (Figs. 3 and 4). Notice that $0.35\text{-}\mu\text{m}$ groundrules were used in the layout although the technology is capable of $0.25\text{-}\mu\text{m}$ groundrules. The pixel size was $7\text{ }\mu\text{m} \times 7\text{ }\mu\text{m}$, with a 33% fill factor. This was scaled from the $10\text{ }\mu\text{m} \times 10\text{ }\mu\text{m}$ pixel (with the same fill factor) of the earlier $0.5\text{-}\mu\text{m}$ technology [10]. An external current source ($10\text{ }\mu\text{A}$) was used to bias the source follower. The threshold voltage (V_{TH}) was 0.5 V .

Clocks and measured output waveforms for both types of pixels are shown in Figs. 5 and 6. In Figs. 5 and 6, the output voltage drop between reset switch-off and transfer gate turn-on ($t_1 < t < t_2$) was due to reset clock coupling. Although the rise and fall transition times of the output signal was long (the in-pixel source follower directly drives the large pad and probe capacitances), the basic operations of the pixels were not affected.

A. Output Swing

The charge to voltage conversion gain was $45.6\text{ }\mu\text{V/e}$ as measured by the mean-variance method [11], [12]. This agreed

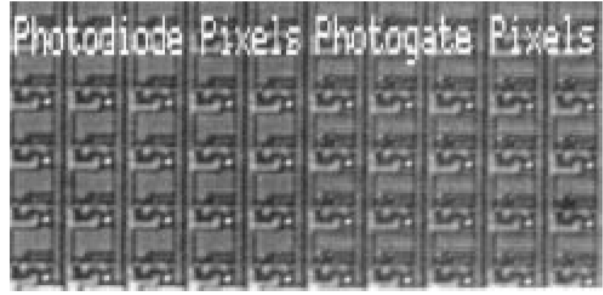


Fig. 4. Photomicrograph of the fabricated pixels. Pixel size was $7\text{ }\mu\text{m} \times 7\text{ }\mu\text{m}$, with a 33% fill factor. The light shield (2nd level metal) was omitted to reveal the pixel details.

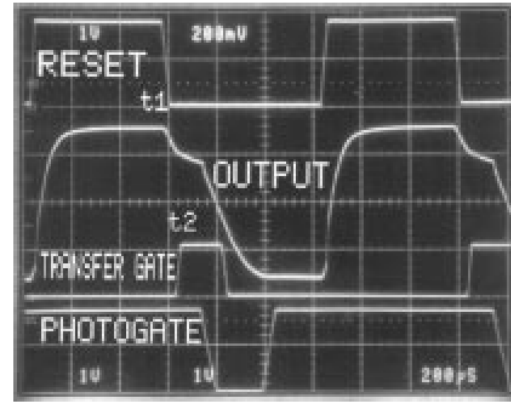


Fig. 5. Measured waveforms of the reset clock, output (V_{out}), transfer gate clock, and photogate clock for the photogate pixel. Medium light level. Clocks = 1 V/div , output = 200 mV/div .

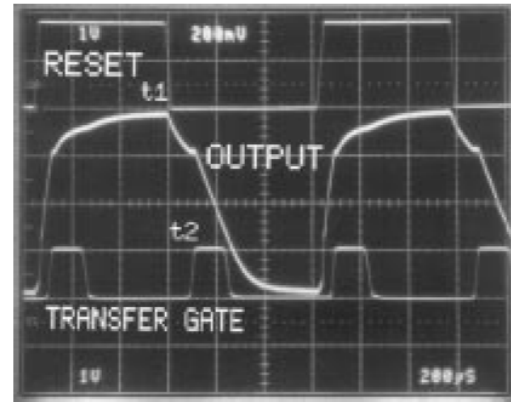


Fig. 6. Measured waveforms of the reset clock, output (V_{out}), and transfer gate clock for the photodiode pixel. Medium light level. Clocks = 1 V/div , output = 200 mV/div .

with the capacitance of the floating diffusion node ($\approx 3.5\text{ fF}$) calculated from the pixel layout. The analog output swing (at the V_{out} node) decreased drastically with the voltage-scaled power supply since the threshold voltage cannot be scaled. Due to the effect of the body potential on the threshold voltage, the threshold voltage of the source follower input transistor (Q_{amp}) and the reset switch (Q_{reset}) are high, and the output

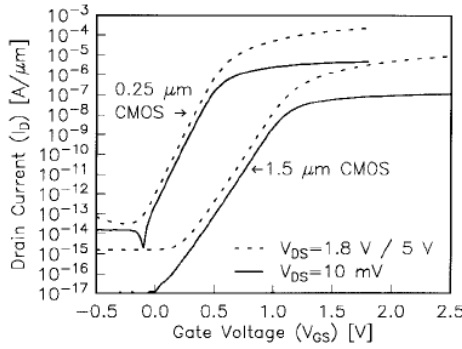


Fig. 7. Comparison of measured drain current for the 0.25- μm CMOS technology in this paper and a 1.5- μm CMOS technology that is also applicable for CCD's [10]–[11]. $V_{SB} = 0$ V.

swing is at most 500 mV if an enhancement nFET load was used for the source follower. Use of a depletion source follower load and/or boosting the reset clock above the power supply will enhance the analog swing (to 1.2 V) at the output. The full signal charge was therefore 11 000 electrons for a 500 mV output swing, and 26 000 electrons for a 1.2 V output swing.

B. Off Current

A significant consequence of device scaling is the increase of the FET off-current. Most pixel architectures convert the photo-charge to either a voltage or a current by placing the photo-charge onto a high impedance node such as the gate of a MOSFET. This high impedance node needs to be isolated from the rest of the pixel circuit and this is usually done by a MOSFET switch. Off-current from that MOSFET switch will appear as “dark current.” Fig. 7 compares the measured drain current as a function of the gate voltage for the 0.25- μm CMOS technology ($V_{DD} = 1.8$ V, $V_{TH} = 0.42$ V, $t_{ox} = 4$ nm) in this paper and a 1.5- μm CMOS technology ($V_{DD} = 10$ V, $V_{TH} = 1.0$ V, $t_{ox} = 45$ nm) that is also applicable for CCD's [13], [14]. The off-current is about 2.8 decades ($V_{SB} = 0$ V) to 20 times ($V_{SB} = V_{DD} - V_{TH}$) larger for the 0.25- μm technology because of the subthreshold slope and the lower threshold voltage.

In this pixel architecture (Fig. 3), the transistors that need to hold a small off-current were the reset gate and the transfer gate. Since both transistors had a source to substrate back bias of about $V_{DD} - V_{TH}$, the off-current was too small to introduce any noise to the high-impedance readout node. This may not be true for other pixel architectures.

C. Threshold Voltage Tracking

One of the major issues for CMOS imagers is the fixed-pattern noise caused by transistor mismatch. Fig. 8 shows the measured threshold voltage tracking ($\sigma_{\Delta V_{TH}}$). Short range V_{TH} tracking was good (≈ 6.5 mV), and could be significantly improved by using gate lengths slightly larger than the minimum gate length (this has some impact on pixel size and/or fill factor).

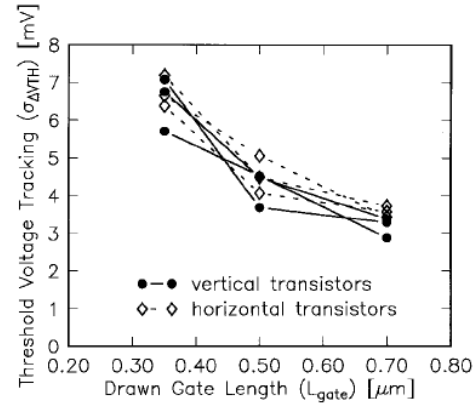


Fig. 8. Measured tracking of threshold voltage (one standard deviation) as a function of the drawn gate length. The various curves are for different matching pairs of transistors.

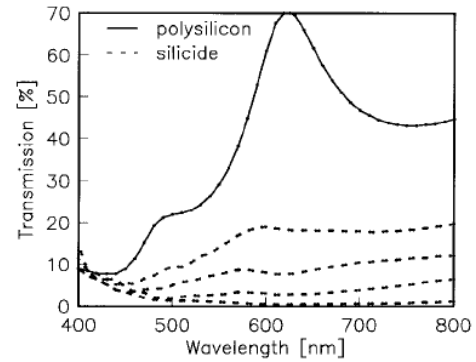


Fig. 9. Measured spectral transmission of polysilicon (150 nm) and various silicides commonly employed in CMOS technologies. Films were deposited on quartz wafers in this measurement. Multilayer interference effects were not removed from these data.

D. Optical Sensitivity

Salicided gates and junctions have limited optical transmission (Fig. 9). We also fabricated pixels that used the shallow-trench oxide isolation (STI) as an optical window (Fig. 10). This layout allows light to go into the silicon through the shallow trench isolation regions. Photo-generated carriers are collected by the photogate/photodiode via carrier diffusion. With a 36% STI to photosensitive area ratio, the photodiode showed roughly 50% improvement in optical sensitivity compared to the layout where the photosensitive area was completely covered by the photodiode. The improvement for photogate pixels was insignificant because of the limited amount of open STI region (8%) allowable by design groundrules.

E. Dark Current

Dark current is a major consideration for imagers. The measured dark current for the photogate pixel is shown in Fig. 11. Fig. 12 shows the schematic energy diagram for the dark current measurement. The dark current was measured

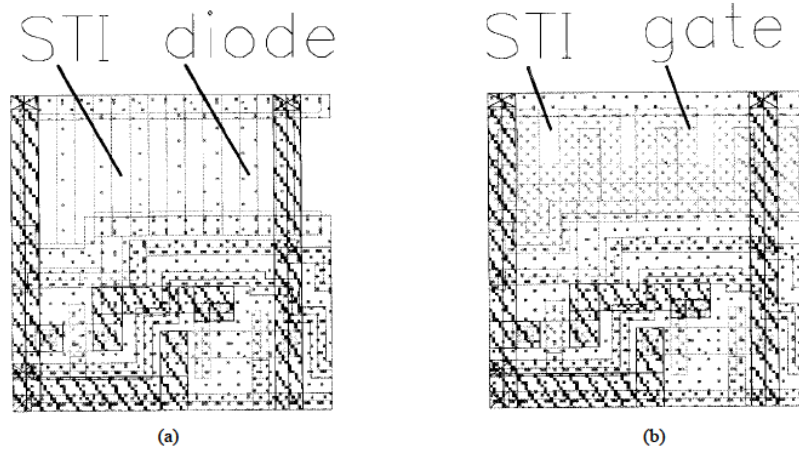


Fig. 10. Layout of four-transistor CMOS active pixel image sensor cells with oxide isolation (STI) optical windows. (a) Photodiode. (b) Photogate.

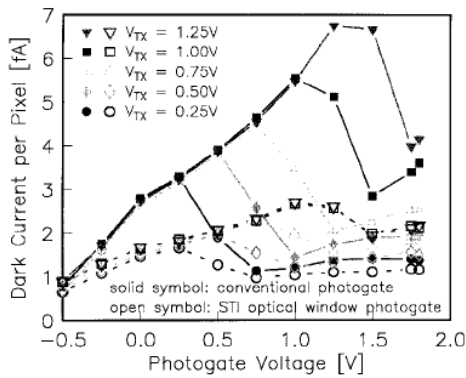


Fig. 11. Measured dark currents of photogate pixels at room temperature.

by first resetting the floating diffusion readout diode (pulsing V_{reset} to V_{DD}) and then monitoring the drop of the potential at the floating diffusion node within a fixed time window. When the photogate voltage (V_{PG}) was lower than the transfer gate voltage (V_{TX}) (solid line in the energy diagram of Fig. 12), any dark current generated under the photogate was immediately collected at the floating diffusion readout diode because of the favorable potential distribution (there was no charge under the potential well of the photogate at this bias condition). Dark current increased with increasing voltage on the photogate because the depletion width under the photogate increased with gate voltage. As the photogate voltage (V_{PG}) increased beyond the transfer gate voltage (V_{TX}) (dashed line in the energy diagram of Fig. 12), dark charge was first collected under the photogate for some period of time without being collected at the floating diffusion diode. As the potential under the photogate dropped below that of the transfer gate voltage, the dark charges generated under the photogate were again collected at the floating diffusion diode, causing the potential at the floating diffusion diode to drop again [the dark charge under the potential well of the photogate had an energy determined by the bias of the transfer gate (V_{TX})]. Therefore, the measured dark current in Fig. 11 increased with V_{PG} when $V_{\text{PG}} < V_{\text{TX}}$ and then decreased with V_{PG} when $V_{\text{PG}} > V_{\text{TX}}$.

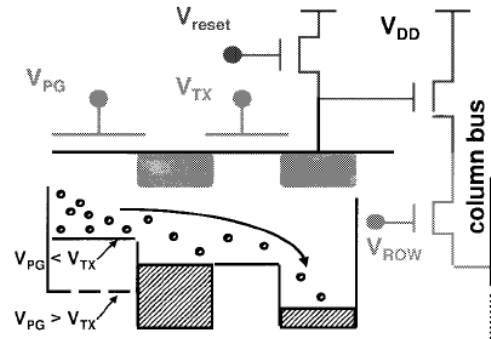


Fig. 12. Schematic energy diagram and circuit of the dark current measurement for photogate pixels.

For the photogate, the dark current was about 3–7 fA per pixel, corresponding to 25 to 38 electrons (rms) of dark noise for a 33 ms integration time. With the photogate biased in accumulation (pinning) mode, the dark current reduced to about 1 fA per pixel.

The measured dark current for the photodiode pixel is shown in Fig. 13. Fig. 14 shows the schematic energy diagram for the dark current measurement. The dark current was measured by first resetting the floating diffusion readout diode (pulsing V_{reset} to V_{DD}) and then monitoring the drop of the potential at the floating diffusion node within a fixed time window. For the photodiode, the dark current was about 1–2 fA per pixel, corresponding to 14 to 20 electrons (rms) of dark noise for a 33 ms integration time.

These dark current values are somewhat higher (≈ 2 –20 times) than the best quality CCD's but is quite respectable since the technology has not yet been optimized for low dark current and the junctions were salicided and bounded by shallow trench isolation instead of LOCOS.

Comparing the area and perimeter of the pixels with an STI optical window and a standard layout, the relative contribution of the area and edge components of the dark current were calculated. For the photogate, the gate area completely dominated the leakage, indicating that dark current generation via

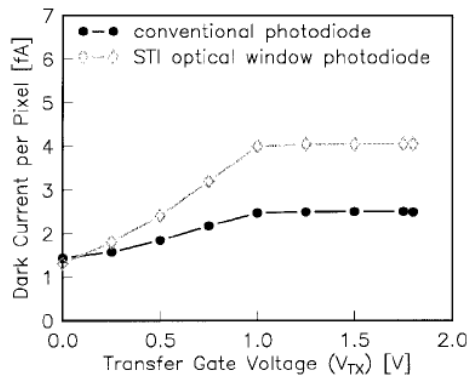


Fig. 13. Measured dark currents of photodiode pixels at room temperature.

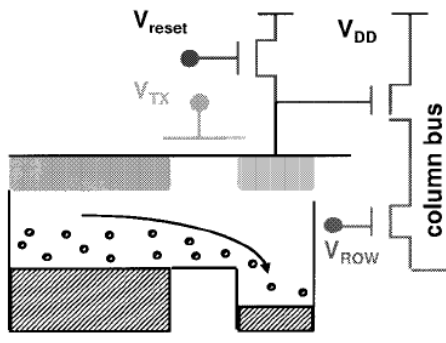


Fig. 14. Schematic energy diagram and circuit of the dark current measurement for photodiode pixels.

Si/SiO₂ interface states was responsible for most of the dark current for the surface channel photogate. For the photodiode, the area and perimeter component each contributed to about half of the dark current measured for the layout shown in Fig. 10. In order to minimize the dark current and maximize the optical transmission, the preferred layout of the open STI optical window pixel is one where the active junction region is a donut-ring shape instead of the strips in the present design. For the donut-ring shaped active junction design, the dark current is calculated to be the same as the conventional layout and yet have a 90% improvement in optical sensitivity over the conventional layout.

IV. CONCLUSIONS

This paper reports the first experimental results of CMOS imagers fabricated using a high-performance 1.8 V, 0.25- μ m CMOS logic technology. No process modifications were made to the CMOS logic technology so that the impact of device scaling on the image sensing performance (e.g. leakage current, analog swing, etc.) can be studied. This paper highlights the device and process design considerations required to enable CMOS as an image sensor technology.

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Emmanuel Crabbé, photograph and biography not available at the time of publication.