

Petition for *Inter Partes* Review of U.S. Patent No. 11,121,222

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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TEXAS INSTRUMENTS INCORPORATED,

Petitioner

v.

GREENTHREAD LLC,

Patent Owner

U.S. PATENT NO. 11,121,222

Case IPR2024-00674

PETITION FOR *INTER PARTES* REVIEW

UNDER 35 U.S.C. §312 AND 37 C.F.R. §42.104

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## TABLE OF EXHIBITS

| Exhibit No. | Description                                                                                                                       |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------|
| 1001        | U.S. Patent No. 11,121,222 to Rao (the “222 Patent”)                                                                              |
| 1002        | Prosecution History of the ‘222 Patent (“the Prosecution History”)                                                                |
| 1003        | Declaration of Travis Blalock, PhD                                                                                                |
| 1004        | Curriculum Vitae of Travis Blalock, PhD                                                                                           |
| 1005        | U.S. Patent No. 4,684,971 (“Payne”)                                                                                               |
| 1006        | U.S. Patent No. 4,907,058 to Sakai (“Sakai”)                                                                                      |
| 1007        | U.S. Patent No. 6,043,114 to Kawagoe, et al., (“Kawagoe”)                                                                         |
| 1008A       | Stanley Wolf and Richard N. Tauber, <i>Silicon Processing For The VLSI Era</i> , Vol 1, Lattice Press (2000) (“Wolf.1”)           |
| 1008B       | Stanley Wolf and Richard N. Tauber, <i>Silicon Processing For The VLSI Era</i> , Vol. 2, Lattice Press (2000) (“Wolf.2”)          |
| 1008C       | Stanley Wolf and Richard N. Tauber, <i>Silicon Processing For The VLSI Era</i> , Vol. 3, Lattice Press (2000) (“Wolf.3”)          |
| 1008D       | Stanley Wolf and Richard N. Tauber, <i>Silicon Processing For The VLSI Era</i> , Vol. 4, Lattice Press (2000) (“Wolf.4”)          |
| 1009        | U.S. Patent No. 4,160,985 (“Kamins”)                                                                                              |
| 1010        | U.S. Patent No. 4,481,522 (“Jastrzebski”)                                                                                         |
| 1011        | U.S. Patent Application Publication No. 2003/0042511 (“Rhodes”)                                                                   |
| 1012        | U.S. Patent Application Publication No. 2002/0102783 (“Fujimoto”)                                                                 |
| 1013        | Wang and Agrawal, <i>Single Event Upset: An Embedded Tutorial</i> , 21 <sup>st</sup> Intl Conf on VLSI Design, IEEE 2008 (“Wang”) |
| 1014        | Publication Declaration of Alyssa G. Resnick for Wolf.1 and Wolf.2 (“Resnick Decl.”)                                              |
| 1015        | Publication Declaration of Rachel J. Watters for Wolf.3 and Wolf.4 (“Watters Decl.”)                                              |
| 1016        | IPR2020-289, Patent Owner Preliminary Response                                                                                    |
| 1017        | U.S. Pat. No. 8,421,195 (the “195 Patent”)                                                                                        |
| 1018        | U.S. Pat. No. 11,316,014 (the “014 Patent”)                                                                                       |
| 1019        | Civil Action No. 2:19-cv-00147-JRG, Dkt. 67 (E.D. Tex. Apr. 20, 2020)                                                             |
| 1020        | Prosecution History of U.S. Pat. No. 8,421,195                                                                                    |
| 1021        | Prosecution History of U.S. Pat. No. 11,316,014                                                                                   |
| 1022        | U.S. Patent Application Publication No. 2004/0063288 (“Kenney”)                                                                   |

| Exhibit No. | Description                                                                                                                                                                                                                                                                              |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1023        | Jaeger, <i>Introduction to Microelectronic Fabrication</i> , Vol. V, Addison-Wesley Modular Series on Solid State Devices (1988) (“Jaeger”)                                                                                                                                              |
| 1024        | U.S. District Courts – Case Statistics, obtained at <a href="https://www.uscourts.gov/statistics-reports/analysisreports/federal-court-management-statistics">https://www.uscourts.gov/statistics-reports/analysisreports/federal-court-management-statistics</a> , dated March 31, 2023 |
| 1025        | U.S. Patent No. 4,435,896 (“Parrillo”)                                                                                                                                                                                                                                                   |
| 1026        | L.C. Parrillo, R.S. Payne et al., <i>Twin-Tub CMOS - A Technology for VLSI Circuits</i> , IEEE 1980 (“Parrillo2”)                                                                                                                                                                        |
| 1027        | U.S. Patent Application Publication No. 2007/0045682 to Hong <i>et al.</i> (“Hong”)                                                                                                                                                                                                      |
| 1028        | The Oxford American Dictionary and Language Guide, Oxford University Press (1996)                                                                                                                                                                                                        |
| 1029        | Defendants’ Opening Claim Construction Brief                                                                                                                                                                                                                                             |
| 1030        | Patent Owner’s Response Claim Construction Brief                                                                                                                                                                                                                                         |
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| 1033        | Proposed Claim Constructions in the District Court Case                                                                                                                                                                                                                                  |
| 1034        | Redacted District Court Case Transfer Order                                                                                                                                                                                                                                              |
| 1035        | Civil Action No. 2:19-cv-00147-JRG, Dkt. 105 (E.D. Tex. Jul. 9, 2020)                                                                                                                                                                                                                    |
| 1036        | IPR2020-289, Termination Order                                                                                                                                                                                                                                                           |
| 1037        | District Court’s Tentative Claim Construction Ruling                                                                                                                                                                                                                                     |
| 1038        | U.S. Patent Application Publication No. 2003/0183856 to Wieczorek (“Wieczorek”)                                                                                                                                                                                                          |
| 1039        | Publication Declaration of Sylvia Hall-Ellis for Wolf                                                                                                                                                                                                                                    |
| 1040        | Law360 Article “Stays Pending IPR In Del. District Courts Are Here To Stay,” Kraning and Del Dotto, March 11, 2022.                                                                                                                                                                      |
| 1041-1100   | RESERVED                                                                                                                                                                                                                                                                                 |
| 1101        | Complaint for Patent Infringement, <i>Greenthread, LLC v. Texas Instruments Inc.</i> , Case No. 2:23-cv-00157 (E.D. Tex. April 6, 2023)                                                                                                                                                  |
| 1102        | Docket Control Order, <i>Greenthread, LLC v. Texas Instruments Inc.</i> , Case No. 2:23-cv-00157 (E.D. Tex. Aug. 8, 2023)                                                                                                                                                                |

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|      |                                                                                                                                                                                                                                                                                                                                           |
|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1103 | Combined Civil and Criminal Federal Court Management Statistics (Dec. 31, 2023)   United States Courts (uscourts.gov), available at:<br><a href="https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distprofile1231.2023.pdf">https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distprofile1231.2023.pdf</a> |
|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

Texas Instruments Incorporated (“Petitioner” or “TI”), requests *inter partes* review of claim 44 (the “Challenged Claim”) of U.S. Patent No. 11,121,222 (EX1001). This Petition is accompanied by a Motion for Joinder to join instituted IPR proceeding *Semiconductor Components Industries, LLC v. Greenthread, LLC*, IPR2023-01244.

## **I. INTRODUCTION**

The ‘222 Patent is directed to a Complementary Metal-Oxide Semiconductor (CMOS) device having graded dopant concentrations. EX1001, 4:13-29. This Petition demonstrates that the Challenged Claim is unpatentable as obvious.

## **II. MANDATORY NOTICES**

### **A. Real Party-In-Interest**

Petitioner Texas Instruments Incorporated is the real party-in-interest.

### **B. Related Matters**

The ‘222 Patent is the subject of the following active proceedings:

- *Greenthread, LLC v. ON Semiconductor Corporation and Semiconductor Components Industries, LLC*, Civil Action No. 1:23-cv-00443 in the District of Delaware, filed April 21, 2023 (“District Court Case”);
- *Greenthread, LLC v. Western Digital Corporation et al*, Civil Action No. 1:23-cv-00326 in the District of Delaware, filed March 24, 2023;
- *Greenthread, LLC v. Cirrus Logic, Inc.*, Civil Action No. 1:23-cv-

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00369 in the Western District of Texas, filed March 31, 2023;

- *Greenthread, LLC v Texas Instruments Incorporated*, Civil Action No. 2:23-cv-00157 in the Eastern District of Texas, filed April 6, 2023;
- *Greenthread, LLC v. OSRAM GmbH et al*, Civil Action No. 2:23-cv-00179 in the Eastern District of Texas, filed April 19, 2023;
- *Greenthread, LLC v. OmniVision Technologies, Inc.*, Civil Action No. 2:23-cv-00212 in the Eastern District of Texas, filed May 10, 2023;
- *Greenthread, LLC v. Monolithic Power Systems, Inc.*, Civil Action No. 1:23-cv-00579 in the District of Delaware, filed May 26, 2023;
- *Monolithic Power Systems, Inc. v. Greenthread, LLC*, IPR2024-00470, before the Patent Trial and Appeal Board, filed February 3, 2024;
- *Cirrus Logic, Inc. et al v. Greenthread, LLC*, IPR2024-00020, before the Patent Trial and Appeal Board, filed October 27, 2023;
- *Cirrus Logic, Inc. et al v. Greenthread, LLC*, IPR2024-00021, before the Patent Trial and Appeal Board, filed October 27, 2023;
- *Semiconductor Components Industries, LLC d/b/a ON Semiconductor v. Greenthread, LLC*, IPR2023-01242, before the Patent Trial and Appeal Board, filed July 27, 2023; and
- *Semiconductor Components Industries, LLC d/b/a ON Semiconductor v.*

*Greenthread, LLC*, IPR2023-01244, before the Patent Trial and Appeal Board, filed July 27, 2023.

The '222 Patent was previously subject to the following proceedings, which are no longer pending:

- *Greenthread, LLC v. Intel Corporation, Dell Inc., and Dell Technologies Inc.*, Civil Action No. 6:22-cv-105 in the Western District of Texas (“Intel Litigation”), filed January 27, 2022;
- *Greenthread, LLC v. Intel Corporation*, Civil Action No. 6:22-cv-01293 in the Western District of Texas, severed December 21, 2022, and transferred to District of Oregon as 3:22-cv-02001;
- *Greenthread, LLC v. Micron Technology, Inc. et al.*, Civil Action No. 1:23-cv-00333 in the District of Delaware, filed March 24, 2023;
- *Intel Corporation v. Greenthread, LLC*, IPR2023-00420, before the Patent Trial and Appeal Board, filed December 28, 2022;
- *Intel Corporation v. Greenthread, LLC*, IPR2023-00552, before the Patent Trial and Appeal Board, filed February 1, 2023;
- *Dell Technologies Inc. et al v. Greenthread, LLC*, IPR2023-00509, before the Patent Trial and Appeal Board, filed January 27, 2023; and
- *Sony Group Corporation v. Greenthread, LLC*, IPR2023-00324, before the Patent Trial and Appeal Board, filed December 12, 2022.

**C. Counsel Service Information Lead**

| Lead Counsel                                                                                                                                                                                                                                         | Backup counsel                                                                                                                                                                                                                              |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
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**D. 37 C.F.R. §42.8(b)(4): Service Information**

Please address all correspondence and service to the address listed above. Petitioner consents to electronic service by email at [IPR12189-0088IP2@fr.com](mailto:IPR12189-0088IP2@fr.com) (referencing No. 12189-0088IP2 and cc'ing [PTABInbound@fr.com](mailto:PTABInbound@fr.com), [griswold@fr.com](mailto:griswold@fr.com) and [bisenius@fr.com](mailto:bisenius@fr.com)).

**III. PAYMENT OF FEES UNDER 37 C.F.R. §42.103**

The undersigned authorizes the Office to charge the fee set forth in 37 C.F.R. §42.15(a)(1) for this Petition to Deposit Account No. 02-0384. Review of 1 claim is requested. The undersigned further authorizes payment for any additional fees that may be due in connection with this Petition.

**IV. CERTIFICATION OF GROUNDS FOR STANDING**

Petitioner certifies under Rule 42.104(a) that the '222 Patent is available for IPR and Petitioner is not barred or estopped from requesting IPR of the Challenged Claim on the grounds identified in this Petition.

## V. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED

### A. Prior Art Printed Publications

The ‘222 Patent claims priority to September 3, 2004. Petitioner’s challenge is based on the following prior-art references:

- **Payne** - U.S. Patent No. 4,684,971 to Payne (EX1005) issued on August 4, 1987 and is prior art under 35 U.S.C. §102(b).<sup>1</sup>
- **Sakai** – U.S. Patent No. 4,907,058 to Sakai (EX1006) issued on March 6, 1990 and is prior art under 35 U.S.C. §102(b).
- **Kawagoe** – U.S. Patent No. 6,043,114 to Kawagoe et al. (EX1007) issued on March 28, 2000 and is prior art under 35 U.S.C. §102(b).

### B. Relief Requested

Petitioner requests cancellation of the Challenged Claim as unpatentable under 35 U.S.C. §103. The specific grounds of the challenge are set forth below and are supported by the declaration of Dr. Blalock (EX1003).

| Ground | Basis | Challenged Claim | Reference(s)   |
|--------|-------|------------------|----------------|
| I      | § 103 | 44               | Payne          |
| II     | § 103 | 44               | Sakai, Kawagoe |

## VI. THE ‘222 PATENT

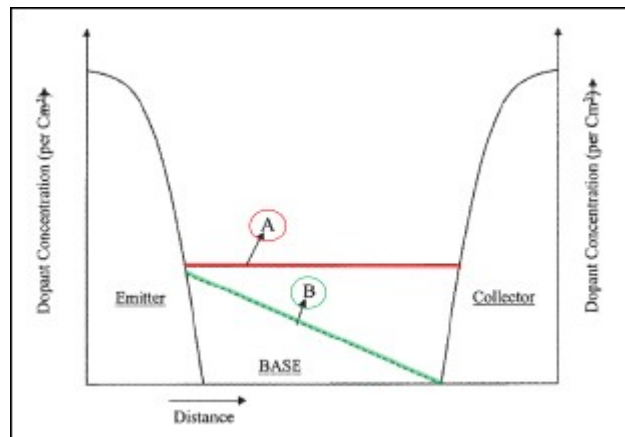
The ‘222 Patent is directed to “grading the dopant concentration” in certain

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<sup>1</sup> Cites to 35 U.S.C. §§102 and 103 are to the pre-America Invents Act (pre-AIA).

regions of a semiconductor device. EX1001, Abstract. The Challenged Claim claims that the semiconductor device comprises a single drift layer and a well region disposed in the single drift layer that have graded dopant concentrations and first/second static unidirectional electric drift fields “to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions.” *Id.*, Cl. 44.

The ‘222 Patent admits that graded dopant concentrations were known. For example, the graded dopant concentration “B” (green) in Figure 1 below is described as one of “the two most popular” doping profiles used in prior art bipolar transistors, in contrast to the uniform doping profile “A” (red). EX1001, 2:27-30; EX1003, ¶44.



EX1001, FIG. 1 (“Prior Art”).<sup>2</sup> The ‘222 Patent further admits that it was known to grade the dopant concentration in well regions of CMOS devices to affect the movement of carriers, but alleges, without support, that prior attempts were met with “little success.” *Id.*, 2:5-19; EX1003, ¶¶47-50.

<sup>2</sup> All colors and colored annotations to figures added.

The 44 claims of the ‘222 Patent, including the Challenged Claim, issued without prior art-based rejection. EX1002. In the Notice of Allowance, the Examiner noted that “the closest reference” for each claim is Hong (EX1027). EX1002, 226-229. With regard to the Challenged Claim, the Examiner stated: “Similarly, claim 44 is allowed because the prior art of record does not teach or suggest, singularly or in combination, at least the limitations of ‘a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions’ (see last 3 lines). ***Again, the closest reference is Hong.***” *Id.*, 228-229. But Hong, the only reference mentioned during prosecution, is not prior art because it was filed on August 31, 2005, long after the claimed priority date of the ‘222 Patent. EX1027; EX1003, ¶51.

## **VII. PERSON OF ORDINARY SKILL IN THE ART**

A person of ordinary skill in the art (“POSITA”) of the subject matter of the ‘222 Patent would have had a Bachelor’s degree in electrical engineering, material science, applied physics, or a related field, and four years of experience in semiconductor design and manufacturing or equivalent work experience. EX1003, ¶¶52-55. Additional education might compensate for a deficiency in experience, and vice-versa. *Id.*

## **VIII. CLAIM CONSTRUCTION**

Claims in an IPR are construed under *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). 37 C.F.R. §42.100(b). Petitioner does not believe any

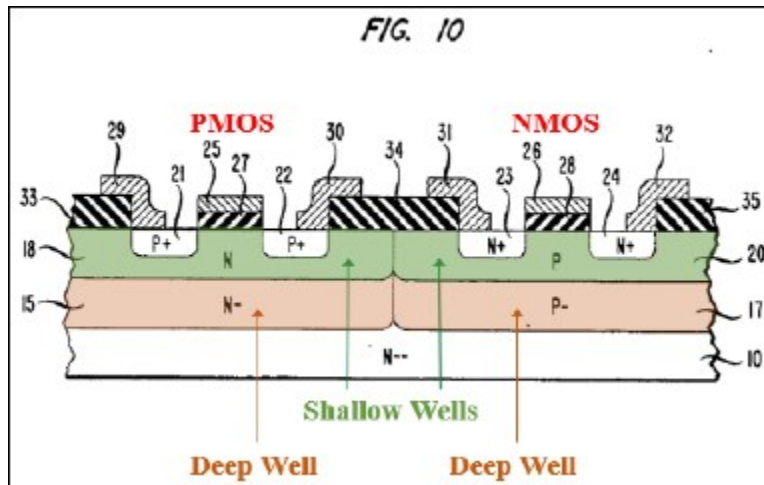
terms need be construed to resolve the issues presented in this Petition. However, Petitioner is aware that Patent Owner and Intel Corporation took positions on the meaning of certain claims. *See* EX1033 (listing constructions in IPR2023-00552); EX1037 (same). Petitioner takes no position on whether Intel’s or Patent Owner’s proposals are correct, but the Challenged Claim is unpatentable under either proposal. EX1003, ¶¶56-59.

## **IX. OVERVIEW OF THE PRIOR ART**

### **A. Payne**

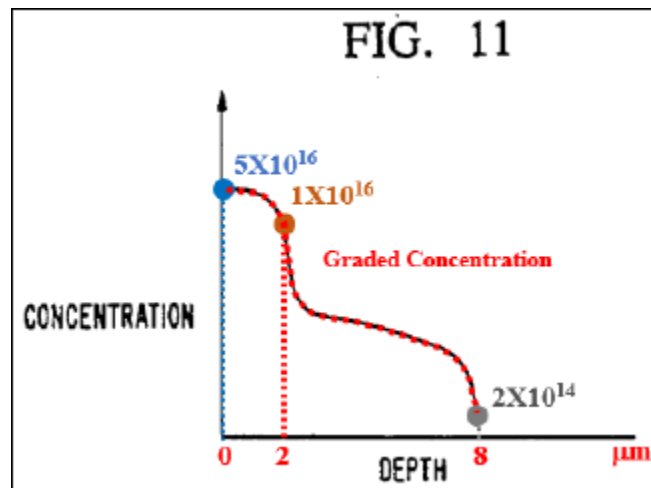
Payne discloses a “CMOS structure and method of manufacture ... for achieving a high packing density in integrated circuits.” EX1005, Abstract. CMOS devices comprise “n-channel” (NMOS) and “p-channel” (PMOS) transistors. EX1005, 1:1-14, 5:18-27. According to Payne, the traditional CMOS fabrication processes using “single tub or twin tub approach[es]” (single-well or twin-well architecture) require source/drain regions of NMOS and PMOS transistors to be sufficiently spaced apart (*e.g.*, at least 12μm), which hinders high packing density. *Id.*, 1:10-50; EX1003, ¶¶60-62.

Payne teaches forming a nested well structure, whereby shallow wells (18 and 20) of “greater impurity concentration” are formed in deep twin-wells (15 and 17), as shown below. EX1005, 1:5-15, 1:51-2:2, 5:18-55, Cl. 1.



*Id.*, FIG. 10; see also 2:3-28, 2:56-5:21, 5:44-50, FIGS. 2-9.

Payne further teaches that the nested well structure has a graded dopant concentration (“high-low implant profile”) that decreases with depth, as shown below in Figure 11. *Id.*, 2:38-41, 5:14-17, 5:51-57 6:7-17, FIG. 11.

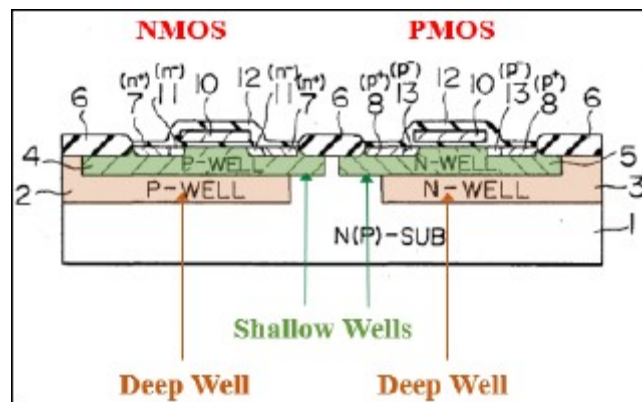


*Id.*, FIG. 11 (annotated with exemplary maximum dopant concentrations at different depths disclosed in Payne); *id.*, 2:56-59, 5:48-55; see also *infra* Section X.A.1.e. Payne’s nested well structure having the “high-low implant profile of FIG. 11” advantageously allows source and drain regions to be placed closer (*e.g.*, less than

5 $\mu$ m separation) resulting in “a high packing density.” *Id.*, Abstract, 1:43-54, 5:56-6:20.

### B. Sakai

Like Payne, Sakai discloses the use of a nested well structure (“twin double well structure”) in CMOS devices to achieve high-packing density. EX1006, 1:6-13, 1:55-2:5, 2:51-3:7, 7:19-37, 8:9-24. Figure 10 below illustrates Sakai’s “twin double well structure,” and shows “shallow P-well” 4 and “shallow N-well” 5 (green) formed in a surface portion of “deep P-well” 2 and “deep N-well” 3 (tan), respectively. EX1006, 1:53-2:39, 5:53-6:19; EX1003, ¶¶63-64.

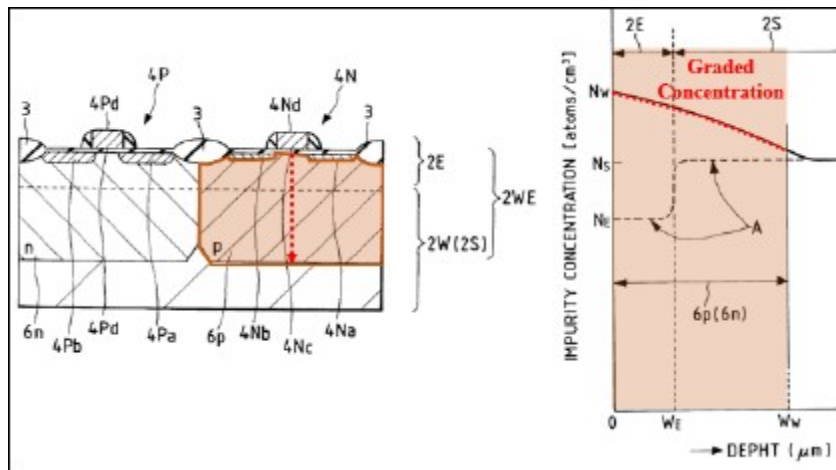


*Id.*, FIG. 10D.

Sakai further discloses that the dopant concentration in the shallow wells is greater than the dopant concentration in the deep wells. *Id.*, 5:56-6:4.

### C. Kawagoe

Kawagoe discloses a CMOS device in which wells have graded dopant concentrations that decrease with depth, as illustrated below right. EX1007, 14:46-55, 15:26-40, 15:62-16:40 (“p-well 6p and n-well 6n have their impurity concentrations gradually lowered in the depthwise direction ...”).<sup>3</sup>



*Id.*, FIGS. 17, 23 The graded dopant concentrations reduce soft errors by sweeping unwanted carriers into the substrate body. *Id.*, 16:2-11 (“electrons produced by the  $\alpha$ -ray are *attracted to the substrate body 2S* by that concentration gradient ... so that the soft errors can be reduced ...”); EX1003, ¶65.

## X. SPECIFIC GROUNDS FOR PETITION

### A. Ground I:

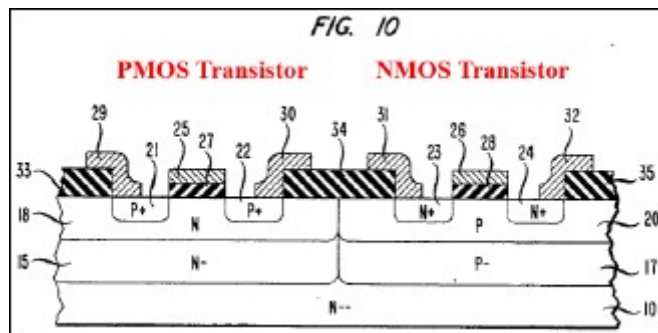
Payne renders claim 44 obvious. EX1003, ¶¶66-121.

#### 1. Independent Claim 44

<sup>3</sup> All emphases added unless otherwise noted.

**a Preamble: “A CMOS Semiconductor device comprising:”**

Payne is directed to a CMOS semiconductor device. EX1003, ¶67; EX1005, Title, Abstract, 1:51-54 (“it is a primary object of the invention to provide a CMOS structure and method of manufacture which requires little semiconductor space and therefore permits a high packing density.”), 1:5-15 (“Complementary field effect transistors (hereinafter designated CMOS) [] comprise n-channel and p-channel devices ...”). Payne Figure 10 illustrates a “p-channel” (PMOS) transistor (with “P+” source/drain regions 21/22) adjacent to an “n-channel” (NMOS) transistor (with “N+” source/drain regions 23/24) of a CMOS semiconductor device. *Id.*, 2:50- 60, 5:18-34, 6:57-59.



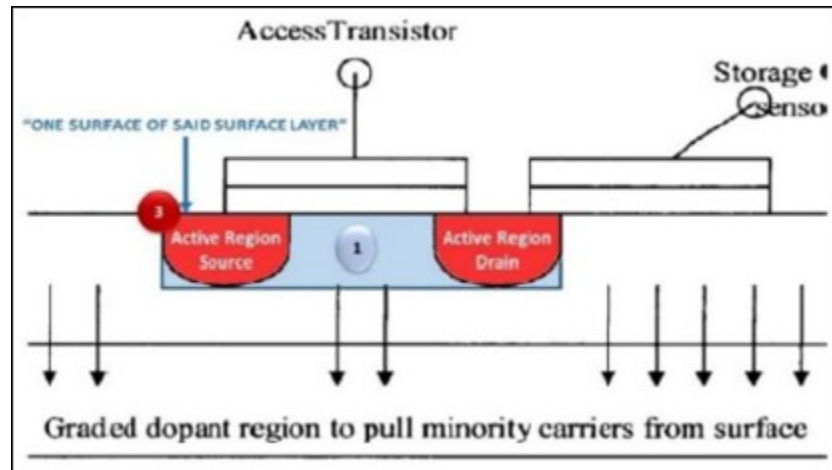
EX1005, FIG. 10.

**b Element [44.1]: “a surface layer;”**

Payne discloses or, at a minimum, renders obvious this element. EX1003, ¶¶68-70. According to Patent Owner, a “surface layer” is “a layer at the surface of the silicon” (or “a layer at the surface of the semiconductor device”)—which Patent

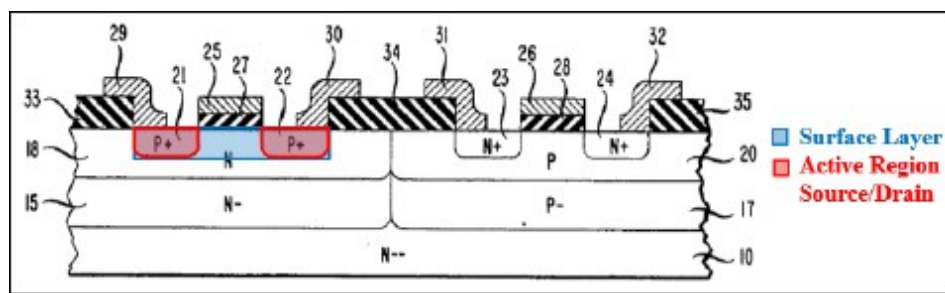
Owner annotated in blue below—“where the active region [(red)] is located.”

EX1030, 6, 9, 12, 13; EX1033.

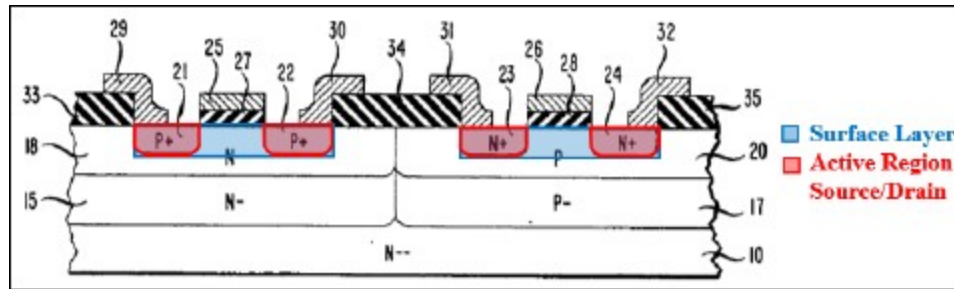


EX1001, FIG. 5(b); EX1030, 7, 12.

Payne satisfies element [44.1] to the same extent that Figure 5(b) meets it. EX1003, ¶¶68-70. Payne’s Figure 10 discloses a surface layer (blue) that matches the surface layer Patent Owner identified in Figure 5(b). Payne’s surface layer is at the surface of Payne’s silicon substrate 10, and the “source and drain regions, 21 and 22 [(red)] of P+ conductivity” of Payne’s p-channel transistor (left) are located in it. EX1005, 2:50-60; 5:21-27, 6:57-59, FIG. 1.



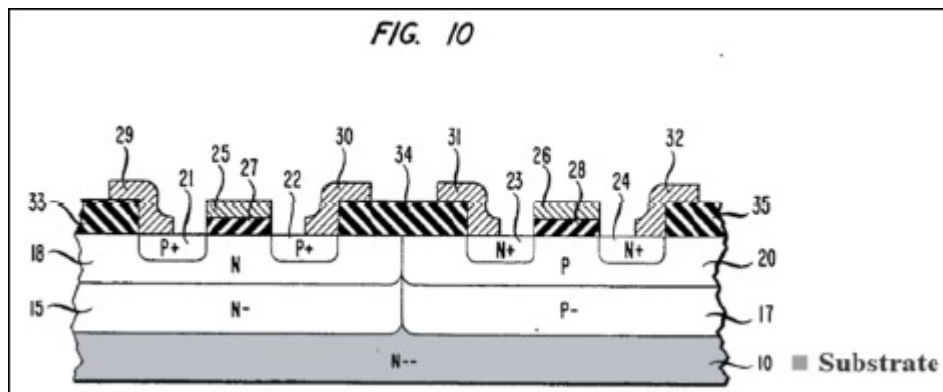
EX1005, FIG. 10. Payne likewise discloses a surface layer containing the “source and drain regions, 23 and 24, of N<sup>+</sup> conductivity” of Payne’s n-channel transistor (right). *Id.*, 5:24-27, 6:57-59; EX1003, ¶70.



EX1005, FIG. 10.

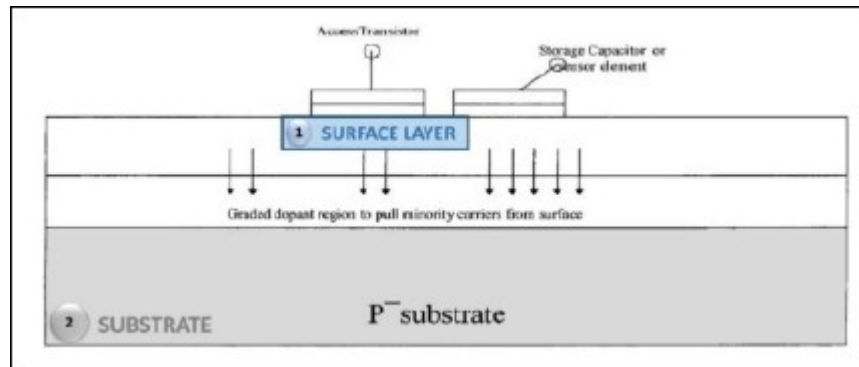
**c Element [44.2]: “a substrate;”**

Payne discloses this element. EX1003, ¶¶71-73. Payne’s Figure 10 illustrates a CMOS device “fabricated in a silicon semiconductor *substrate* [(grey)], 10 of ‘N-’ conductivity type which typically has a doping concentration of approximately  $1-2 \times 10^{14}$  ions/cm<sup>3</sup>[.]” EX1005, 1:60-65, 2:50-60.



EX1005, FIG. 10.

Payne satisfies element [44.2] under Patent Owner’s proposed construction of “plain and ordinary meaning [*i.e.*] ‘an underlying layer.’” EX1033. Payne’s substrate also matches Patent Owner’s identification of the substrate (grey) in Figure 5(b) of the ‘222 Patent.



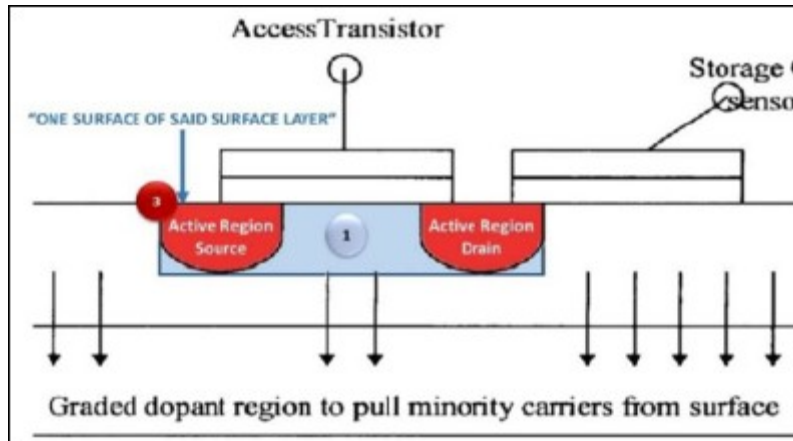
EX1030, 6-7, 16-17 (well region and drift layer can be part of substrate); EX1001, FIG. 5(b).

Payne also satisfies this element under Intel’s proposed construction that a substrate is “the initial material within which or on which the semiconductor device is fabricated.” *See* EX1033; EX1003, ¶73. Payne’s substrate is the initial material within which or on which Payne’s semiconductor device is later fabricated. EX1005, 1:60-65, 2:50-60 (“the [CMOS] device is fabricated in a silicon semiconductor substrate, 10”), FIGS. 1, 10.

**d Element [44.3]: “an active region including a source and a drain, disposed on one surface of the surface layer;”**

Payne discloses or, at a minimum, renders obvious this element. EX1003, ¶¶74-79. According to Patent Owner, Figure 5(b) of the ‘222 Patent depicts an

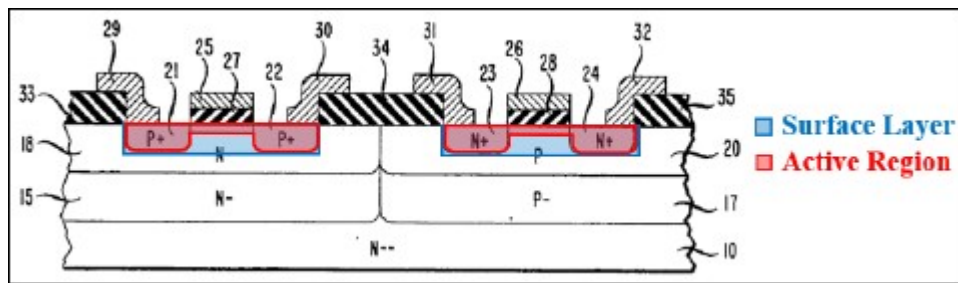
active region (red) “disposed on one surface [(top surface)] of said surface layer,” as shown below:



EX1001, FIG. 5(b); EX1030, 6-7, 11 (“[T]he ‘active region’ is part of the ‘surface layer’ ... When the claim says the active region is ‘disposed on one surface of the surface layer,’ it means the active region is located on the ‘ceiling’ of the silicon *inside* the silicon.”) (emphasis in original), 12.

Payne satisfies element [44.3] under Patent Owner’s interpretation. EX1003, ¶¶75-77. Payne’s Figure 10 below illustrates a “p-channel” transistor with source/drain regions 21/22 (left), and an “n-channel” transistor with source/drain regions 23/24 (right). EX1005, 5:18-29, 1:5-19, 6:57-59. These source/drain regions are formed with “a surface impurity concentration of approximately  $10^{19}$ -  $10^{20}$  ions/cm<sup>3</sup>.” EX1005, 5:21-29, 1:43-45. The channel region between these source

and drain regions is part of the surface region, which has an impurity concentration of “typically  $0.5\text{-}5 \times 10^{16}$  ions/cm<sup>3</sup>.” EX1005, 5:51-52, 4:31-39, 4:63-5:5. The source/drain regions of a transistor, together with the channel region in between them, form an active region. EX1003 ¶¶75-77; EX1008B, 299 (“The top surface of the [silicon substrate] body consists of active or transistor regions as well as passive or (field) regions. The **active regions** are those in which transistor action occurs; i.e., the **channel** and the heavily doped **source** and **drain** regions.”), 300, FIG. 5-2, 382, FIG. 6-8(c), 387, FIG. 6-10; EX1008C, 525, FIG. 8-1(e). The active region (red) of each of Payne’s transistors is disposed on one surface (top surface) of a corresponding surface layer (blue), exactly as depicted in Patent Owner’s annotated Figure 5(b) above. EX1003, ¶¶75-77; *supra* Section X.A.1.b.

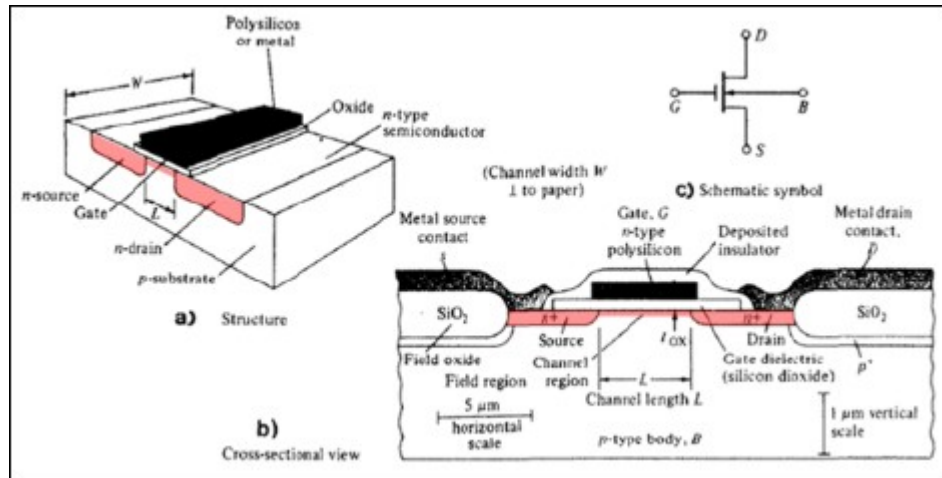


EX1005, FIG. 10.

Payne satisfies element [44.3] under Patent Owner’s position that the term “active region” means “a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed” (EX1033) because the active region of a MOS transistor is “[its] channel

and [its] **heavily doped** source and drain regions,” highlighted in red below.

EX1008B, 299; EX1003, ¶78.

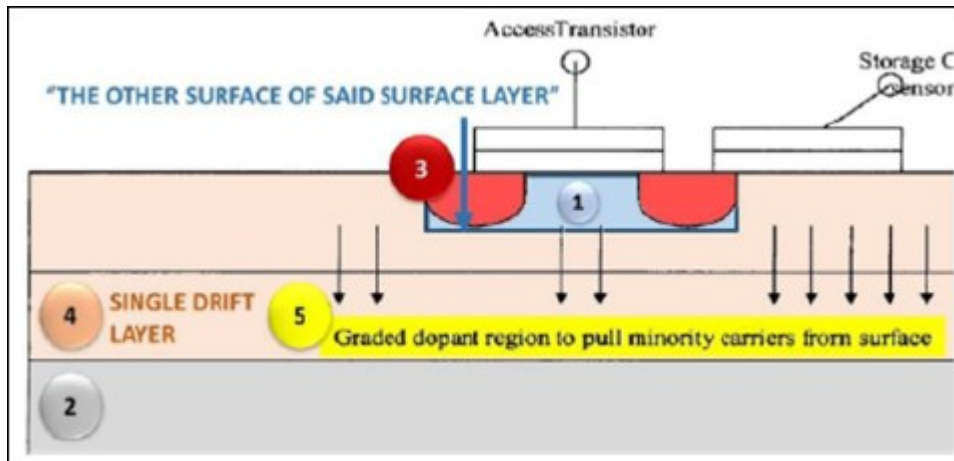


EX1008B, FIG. 5-1; *id.*, 298-301, 374, FIGS. 5-2, 6-4. Payne also satisfies this claim element under Intel’s proposed construction that an “active region” is the “region that forms the current path of a device” or “the source, drain and channel region of a device” because current flows through the channel region that connects the source and drain regions of a transistor when the transistor is active (when an appropriate voltage is applied to its gate). EX1033; EX1008B, 299-301, FIGS. 5-1, 5-2; EX1008D, 197, FIG. 5-13; EX1003 ¶79. Patent Owner does not dispute this. EX1030, 3-4 (“[w]hen a positive voltage is applied to the gate ... a conductive **channel** [is formed] between the **source** and the **drain**, and **current** can begin to flow through the transistor”).

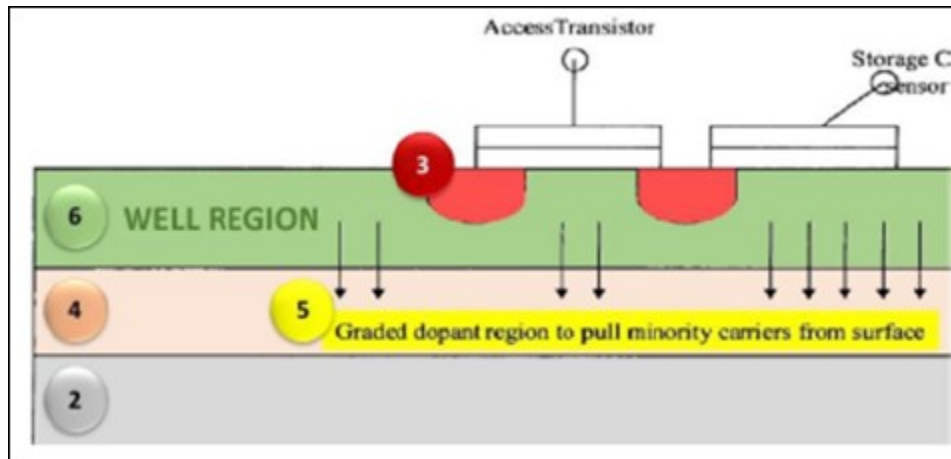
- e     **Element [44.4]: “a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate,”**

Payne discloses or, at a minimum, renders obvious this element. EX1003, ¶¶80-89.

**Single drift layer** – In its claim construction brief, Patent Owner identified the single drift layer in tan in Figure 5(b). EX1030, 7. According to Patent Owner, the single drift layer (tan) is “disposed between ‘the other surface [(bottom surface)] of said surface layer [(blue)]’ and [said] substrate [(grey)]”:

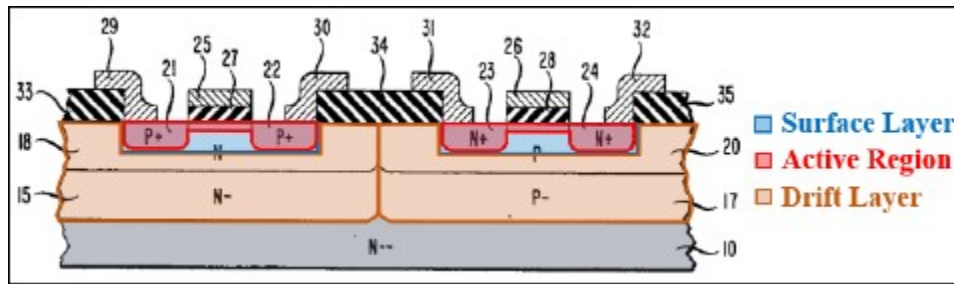


EX1001, FIG. 5(b); EX1030, 7. The single drift layer in Figure 5(b) has a well region (green) disposed in it, forming a nested structure, as required by the claim (*see* element [44.6]), and as shown below:



EX1001, FIG. 5(b); EX1030 at 7; *id.*, 11 (“the ‘well region’ is part of the ‘single drift layer.’”).

Payne discloses a single drift layer to the same extent the ‘222 Patent’s Figure 5(b) does. EX1003, ¶¶81-84. In Payne’s Figure 10, the “**first tub region**” 15 (tan) of Payne’s nested well structure—with shallow well (“surface region”) 18 disposed in it—is an example of the claimed single drift layer. *Id.* ¶ 82; EX1005, 3:28-43 (ion implantation for tub 15), 4:19-30 (thermal drive-in to achieve the desired depth for tub 15), 4:31-39, 5:7-17, 5:44-48, 5:48-50 (“In a typical device, the final depth of surface regions 18 and 20 would be approximately 1-2 $\mu$  and the depth of the **tub regions 15 and 17** would be typically 3-8 $\mu$ .”). This single drift layer (tan) is “disposed between ‘the other surface [(bottom surface)] of said surface layer [(blue)]’ and [said] substrate [(grey)]” under Patent Owner’s interpretation, and in exactly the same way as depicted in Patent Owner’s annotated Figure 5(b) above.

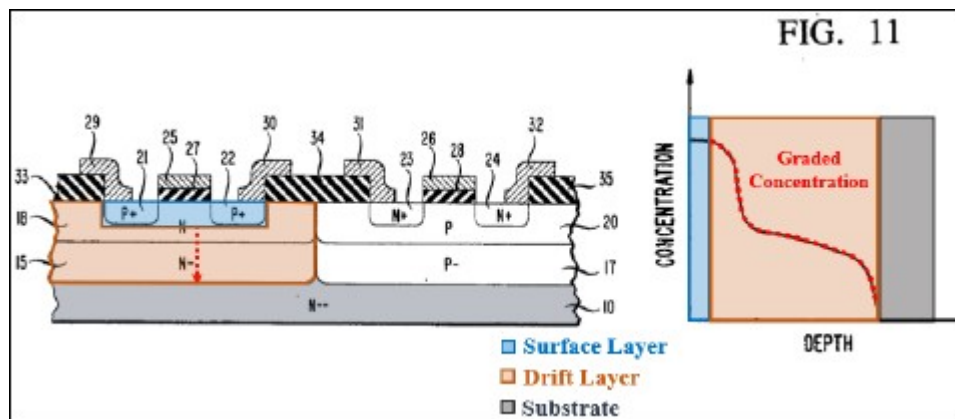


EX1005, FIG. 10. Payne’s tub 17 (right), in which shallow well 20 is disposed, is likewise a single drift layer (tan) disposed between a surface layer (blue) and the substrate (grey). EX1005, 4:3-30, 4:63-5:17, 5:44-50; EX1003, ¶84; *see supra* Section X.A.1.b.

Payne meets all other claim requirements associated with the single drift layer to the same extent Figure 5(b) meets them. *See* below and elements [44.5]-[44.6]; EX1003, ¶84. Notably, as detailed in element [44.5], each of Payne’s tubs 15/17 is a ***single*** drift layer because it has a graded-dopant concentration that, according to Patent Owner, creates a unidirectional electric drift field that aids the movement of minority carriers in a ***single*** direction—from the surface layer to the substrate. EX1030, 7: EX1020, 253-54, 289-290; *infra* Section X.A.1.f.

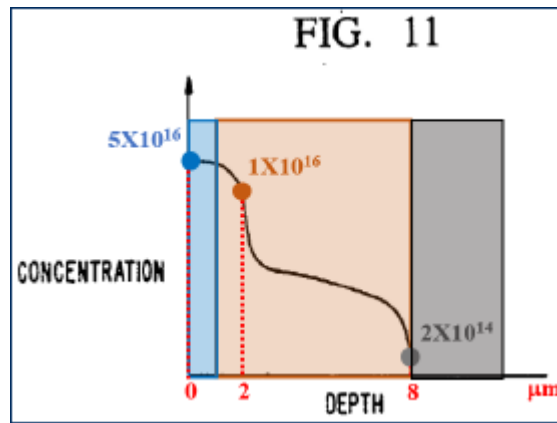
**Graded-dopant concentration** – The ‘222 Patent admits that graded-dopant concentrations were known, EX1001, 2:13-15, FIG. 1 (“Prior Art”), and that it was known to grade the dopant concentration in CMOS devices to affect the movement of minority carriers. *Id.*, 1:34-2:5, FIGS. 3(a)-3(d) (all “Prior art”). Payne’s single drift layer has a graded-dopant concentration extending between the surface layer

and the substrate. EX1003 ¶¶85-88. Payne explains that the “impurity profile in both tubs [15/17] thereby has the general shape illustrated in FIG. 11” which exhibits “[t]he major advantage” of a “**high-low implant profile.**” EX1005, 2:38-41, 5:14-17, 5:56-57. Payne’s Figure 11 (below right) illustrates the dopant concentration measured along the red dotted line in Figure 10 (below left), which starts at the bottom of the surface layer (blue) and extends to the substrate (grey). As shown below, Payne discloses a downward-sloping graded-dopant concentration in the single drift layer (tan) associated with Payne’s PMOS transistor (left).<sup>4</sup>



<sup>4</sup> See *Kingsford Prod. Co., LLC v. Creative Spark, LLC*, IPR2016-01831, Paper 32 at 32 (P.T.A.B. Mar. 9, 2018) (“Figures that are not drawn to scale may be relied upon to disclose qualitative relationships between measured quantities, even though they may not be relied upon to disclose precise quantitative relationships between those same quantities ...”).

EX1005, FIGS. 10-11. Dr. Blalock has annotated Figure 11 to reflect exemplary (maximum) dopant concentrations at various depths disclosed in Payne: (1)  $5 \times 10^{16}$  ions/cm<sup>3</sup> at the surface of the shallow wells (depth  $0 \mu\text{m}$ ), (2)  $10^{16}$  ions/cm<sup>3</sup> at a depth of  $\sim 2 \mu\text{m}$  (boundary of deep and shallow wells), and (3)  $2 \times 10^{14}$  ions/cm<sup>3</sup> at a depth of  $\sim 8 \mu\text{m}$  (boundary of substrate and deep wells). EX1003, ¶¶85-88.



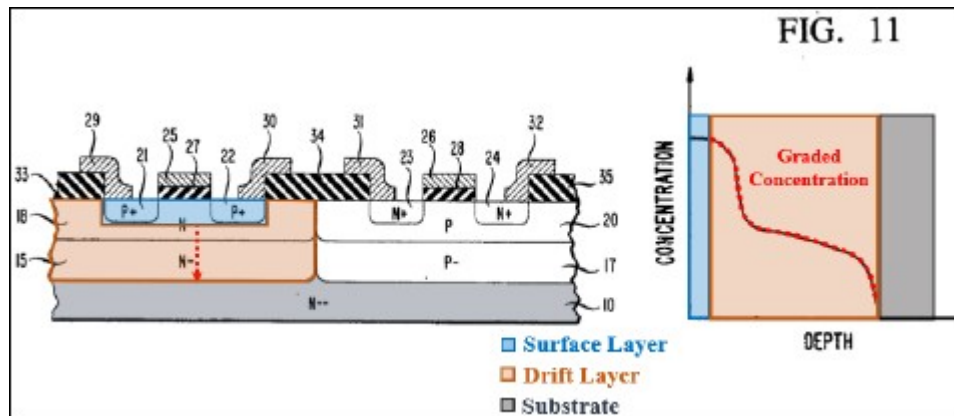
EX1005, FIG. 11. Indeed, Payne explains that “[t]he surface impurity concentration of the surface regions [18/20] is typically  $0.5\text{-}5 \times 10^{16}$  ions/cm<sup>3</sup> and that [the surface impurity concentration] of the tub regions [15/17] is typically  $10^{15}\text{-}10^{16}$  ions/cm<sup>3</sup>, with the former concentration being *at least twice as much* as the latter over these ranges.” *Id.*, 5:51-55. The concentration is lowest at the substrate, where it is “ $1\text{-}2 \times 10^{14}$  ions/cm<sup>3</sup>.” *Id.*, 2:56-59. Payne also explains that “the final depth of surface regions 18 and 20 would be approximately  $1\text{-}2 \mu$  and the depth of tub regions 15 and 17 would be typically  $3\text{-}8 \mu$ .” *Id.*, 5:48-50. EX1003, ¶88.

While the above discusses the single drift layer associated with Payne’s PMOS transistor (left in Figure 10), Payne teaches that the single drift layer

associated with Payne's NMOS transistor (right) also has a downward-sloping graded-dopant concentration. EX1005, 5:14-17; EX1003, ¶89.

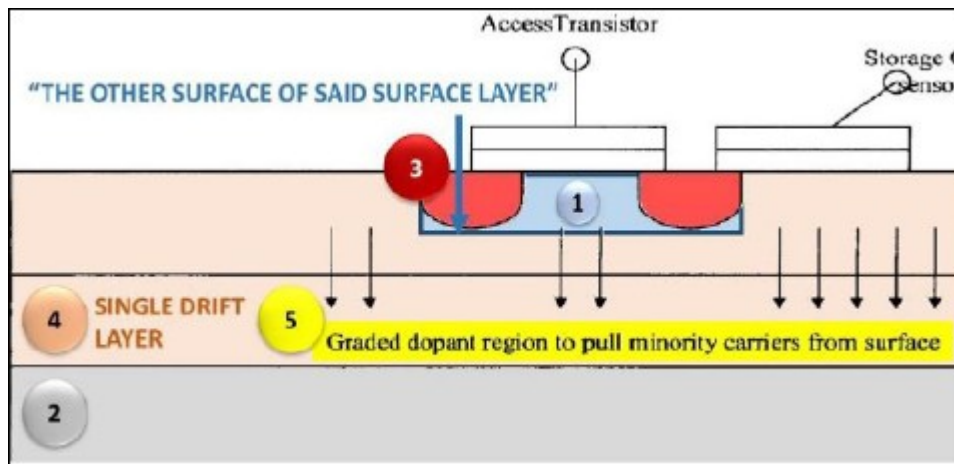
- f **Element [44.5]: “the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and”**

Payne discloses or, at a minimum, renders obvious this element. EX1003, ¶¶90-108. As shown in the figures below, Payne's single drift layer (tan) has a downward-sloping graded-dopant concentration extending between the surface layer (blue) and the substrate (grey). *See supra* Section X.A.1.e.



EX1005, FIGS. 10-11. And, as is clear from Figure 10, there are no active regions in the area of the substrate below the wells (grey) because the active regions in Payne are at the surface of the silicon substrate, as in any CMOS device. *See supra* Section X.A.1.d; EX1008B, 299 (“The *top surface* of the [silicon substrate] body *consists*

of **active or transistor regions** as well as passive or (field) regions. The **active regions** are those in which transistor action occurs; i.e., the **channel** and the heavily doped **source** and **drain** regions.”), 300-301, FIG. 5-2, 382, FIG. 6-8(c), 387, FIG. 6-10; EX1008C, 525, FIG. 8-1(e). EX1003, ¶¶90-94. Payne in fact satisfies element [44.5] to the same extent shown in Figure 5(b) of the ’222 Patent, where the active regions (red) are at the surface of the silicon substrate, and the substrate below the single drift layer is blank, just as in Payne. *Id.*



EX1001, FIG. 5(b); EX1030, 7. Indeed, Patent Owner admits that active regions would be understood as being at the surface of the silicon substrate and therefore they are not located in Payne’s substrate area below the wells (grey). EX1030, 19 (“A POSITA ... would understand that an **active region** [(red)] is a doped silicon region **at the surface** of a semiconductor device where a transistor can be formed.”), 11, 12 (“[T]he surface layer at the surface of the semiconductor device [is] where the active region is located.”), 14 (“The claims make clear that the active region is

part of the surface layer ...”); EX1033; EX1003, ¶¶90-94. Payne’s device fabrication steps illustrated in Figures 1-10 confirm this. *Id.* As Payne explains, the starting material used to fabricate its CMOS device is the silicon semiconductor substrate 10, shown in Figure 1, which is devoid of any active regions or active devices. EX1005, 2:50-60; *see also id.*, 1:5-15, 1:51-54. Deep wells (tubs 15/17) are formed in the substrate through ion implantation and drive-in annealing steps as illustrated in Figures 2-6. *Id.*; 3:28-4:25. Shallow wells (surface regions 18/20) are subsequently formed through additional ion implantation and drive-in annealing steps as illustrated in Figures 7-9. *Id.*, 4:31-5:12. Only then are active regions (source and drain regions 21/22 and 23/24) formed “in accordance with standard techniques” in the shallow wells, as shown in Figure 10. *Id.*, 5:18-29.

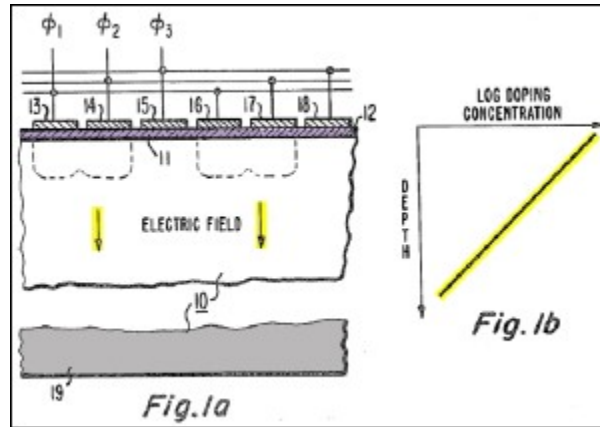
Payne’s downward-sloping graded-dopant concentration aids the movement of minority carriers from the surface layer to the substrate—more precisely, to an area of the substrate where there are no active regions, as discussed above—to the same extent to which Applicant relied on the prior art and admitted to the Patent Office that such carrier movement would occur under the same scenario. EX1003, ¶¶95-99. During prosecution of the parent ‘195 Patent, Applicant represented to the Patent Office that a downward-sloping graded-dopant concentration was known in the prior art to create an “inherent ‘built-in’ unidirectional electric field” that moves

carriers deep into the substrate (while an upward-sloping concentration, not at issue in Payne, would move those carriers in the opposite direction towards the surface):

[T]he graded dopant concentration itself creates a ***‘built-in’ electrical field*** that forces the movement of carriers into a particular direction, whereby ***the ‘direction’ of the electrical field and the resulting direction of the carrier movement depends solely on the slope of the graded concentration of dopant.***

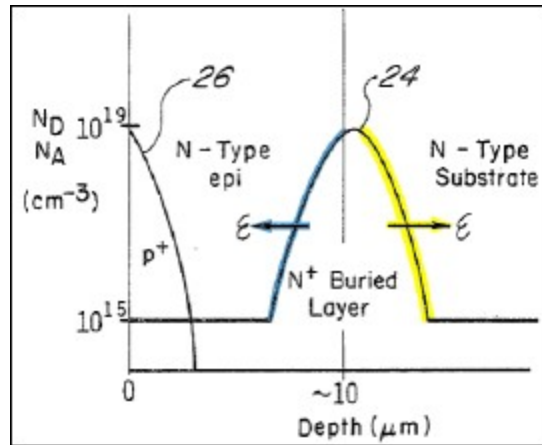
EX1020, 289-290 (underlining in original); EX1003, ¶¶95-99. Applicant further represented that “a unidirectional drift (electric) field necessarily affects ***all*** the present ***minority*** carriers in the same way.... Depending on the particular slope of the graded concentration of dopant, ***all minority*** carriers are either ***swept*** ‘down’ ... or ‘up...’” EX1020, 289. Applicant cited Jastrzebski in support. *Id.*, 290. In Jastrzebski, the graded-dopant concentration is “decreasing with depth” from the top surface 11 (purple) of the substrate 10, as shown in Figure 1b below. EX1010, 5:14-

22. Jastrzebski teaches that this downward-sloping graded-dopant concentration creates an electric drift field that “force[s] most of the charge carriers ... ***deep into the substrate***[.]” *Id.*, 5:14-22; *id.*, 2:27-32 (“This is done by creating a field, such as a drift field, in the semiconductor substrate to ***sweep minority charge carriers...into the bulk [substrate], away from the electrode-bearing surface of the substrate.***”).



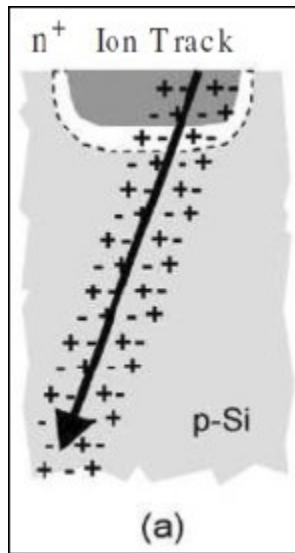
EX1010, FIGS. 1a-1b. Applicant made the same representation to the Patent Office regarding Kamins. EX1020, 237-238, 253-254. According to Applicant, Kamins' Figure 3 shows "two electrical fields with opposing directions" (highlighted in blue and yellow) that correspond to increasing and decreasing graded-dopant concentrations, respectively. *Id.*, 237 (citing EX1009, 3:6-13), 253. Applicant explained that Kamins "show[s] **minority carrier[s] accelerated into the substrate.**" *Id.*, (citing EX1009, FIG. 2 and quoting EX1009, 3:6-13 ("carriers... accelerated... **away from the surface... into the substrate**")). According to Applicant, the electric field associated with the downward-sloping graded concentration at depth beyond ~10µm (red) causes "[minority] carriers created [in that region to be] ...**accelerated into the substrate**" *Id.* (citing EX1009, 3:6-13, FIGS. 2-3); *see also* EX1030 at 24 (Kamin's "bottom electric field [(yellow)] draws a **minority carrier** from the substrate to a **deeper** part of the substrate."); EX1009, 2:67-3:18 ("The non-uniform dopant concentration in the substrate creates electric fields in the substrate indicated

by arrows labeled ‘ $\epsilon$ ’ in FIGS. 2 and 3” such that “carriers created below the maximum dopant concentration are accelerated into the substrate.”), FIG. 2 (referring to these carriers as “photogenerated minority carriers”), 2:11-16 (same).



EX1009, FIG. 3.

Dr. Blalock explains that during a so-called single event upset (SEU), an  $\alpha$ -ray generates millions of carriers, some of which are produced in or near the active regions at the surface of the substrate. EX1003, ¶100; EX1013, 431 (“A[n] [ $\alpha$ -] particle can induce SEU when it strikes at the *channel region* of an off NMOS transistor or the *drain region* of an off PMOS transistor.”), FIG. 2. As shown in Figure 2, such event generates both types of carriers (holes, denoted “+” and electrons, denoted “-”), one of which will be the minority carrier in any given surface layer. EX1003, ¶100.

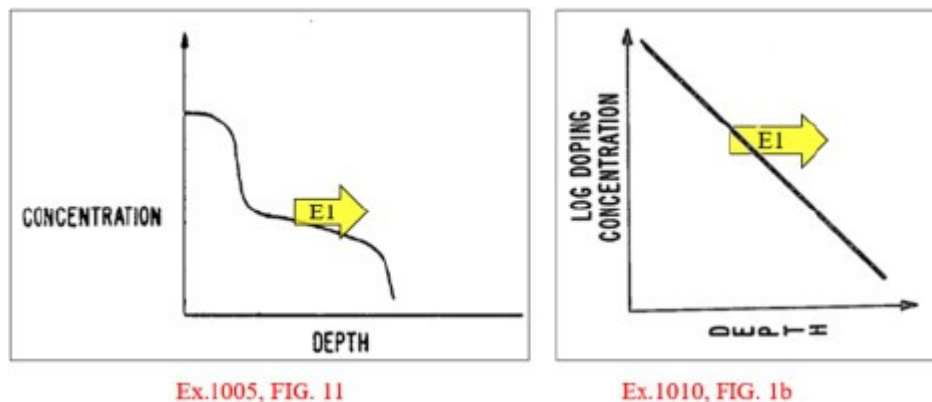


EX1013, FIG. 2(a).

Like Jastrzebski and the right-hand side of Kamins Figure 3 (yellow), Payne's graded-dopant concentration is downward-sloping, as shown in Figure 11. Moreover, this graded-dopant profile is determined by the ion-implantation and drive-in steps of the chip fabrication processes (those steps are described in Payne in relation to Figures 2 and 5-9 in particular) and thus the profile (and any resulting electric field) is static—it is set once the device has been fabricated and does not change afterwards. EX1003, ¶¶101-102; EX1005, 5:7-17, 5:44-55 (describing “the *final* depth” of tubs and surface regions and their typical ranges of impurity concentrations). During prosecution of the parent ‘195 Patent, Applicant described “static” similarly, conceding that “Kamins (US 4,160,985), just like Applicant, discloses the presence of a ‘static’ drift field, ‘because the drift field is created by graded concentration of dopants which does not change over time.’” EX1020, 318

(citing EX1009, 2:15-16, 2:64-3:2, 1:38-46, 3:8-11 and EX1020, 302-03), 333 (same).

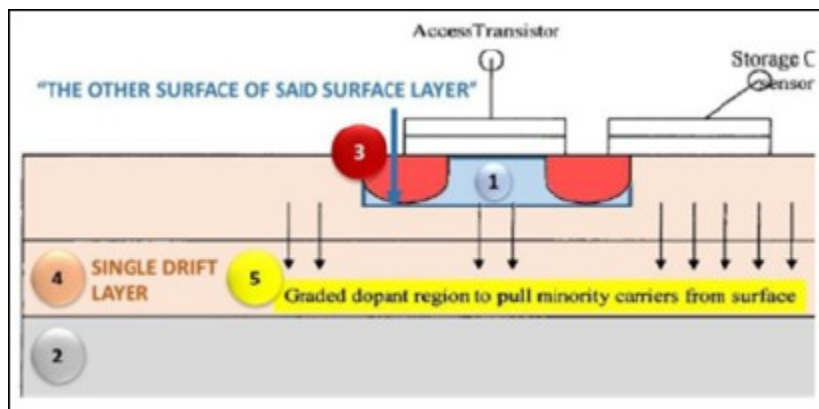
Thus, according to Jastrzebski, Kamins, Applicant, and Patent Owner, Payne's profile generates a (first) "built-in" static unidirectional electric drift field (illustrated by the yellow arrow labelled "E1" below left) that aids the movement of minority carriers from the surface layer to the substrate (specifically, to an area of the substrate where there are no active regions).<sup>5</sup> EX1003, ¶¶95-103.



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<sup>5</sup> The figures of this Petition depict electric fields in N-wells, e.g., Payne's nested N-wells 15/18 or Sakai's nested N-wells 3/5. Sections X.A.1.f-g, X.B.1.f-g. The electric fields would be pointing in the opposite direction in Payne's and Sakai's nested P-wells. In both cases, these electric fields result from the downward- sloping graded concentrations in Payne's and Sakai's N-wells and P-wells and aid the movement of minority carriers (holes in N-wells, electrons in P-wells) downward to the substrate. Id.; EX1003, ¶¶104-105.

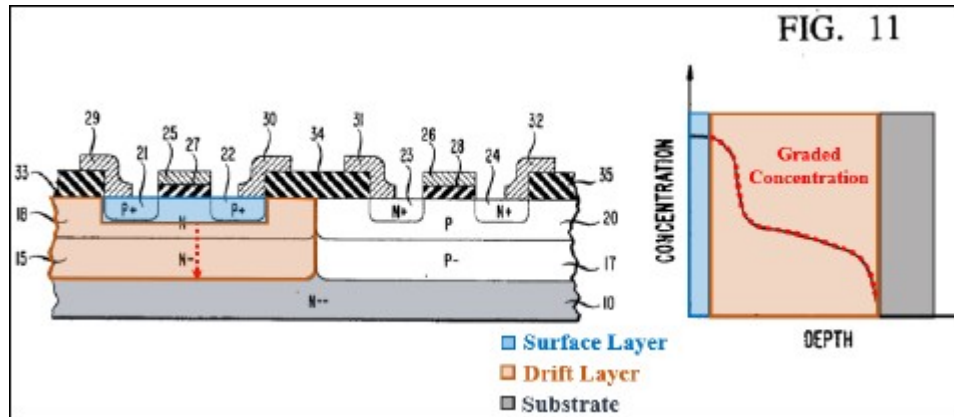
Notably, Payne satisfies element [44.5] to the same extent the ‘222 Patent’s Figure 5(b) meets it. EX1003, ¶¶105-106. While the ‘222 Patent does not disclose any single drift layer’s dopant profile, Patent Owner contends that annotated Figure 5(b) below shows that “[t]he single drift layer has a graded concentration of dopants ... [that] create[s] an electric field that aids the movement of minority carriers [] from the surface layer to the substrate.” EX1030, 7.



EX1001, FIG. 5(b); EX1030, 7.

In light of the above, Payne satisfies element [44.5] under Patent Owner’s plain-meaning constructions. EX1033; EX1003, ¶¶105-108. Payne’s Figure 11 shows a graded-dopant concentration that is downward-sloping over the entire single drift layer (tan)—in fact, from the top of the silicon/surface layer (blue) to the bottom of the single drift layer—and thus, according to Patent Owner (and also in light of Applicant’s representations to the Patent Office discussed above), this graded-dopant concentration creates a static unidirectional electric drift field that aids the movement of minority carriers from the surface layer to the substrate (specifically,

to an area of the substrate where there are no active regions). EX1005, FIG. 11;  
EX1003, ¶¶105-108.



EX1005, FIGS. 10-11.

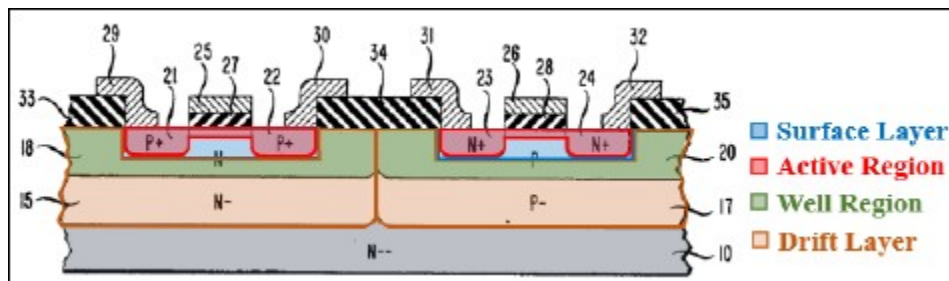
For the same reasons, Payne satisfies Intel’s construction that the first static unidirectional electric drift field must be “unidirectional *over* the drift layer,” and also satisfies Intel’s alternative proposed construction of the sub-phrase “to aid the movement of minority carriers from the surface layer to an area of the substrate where there are no active regions” to mean “to sweep the [] carriers from [the surface layer] to [an area of the substrate where there are no active regions].” *Id.*, EX1033; EX1020, 289-290; EX1003, ¶¶105-108.

- g Element [44.6]: “at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.”**

Payne discloses or, at a minimum, renders obvious this element. EX1003,

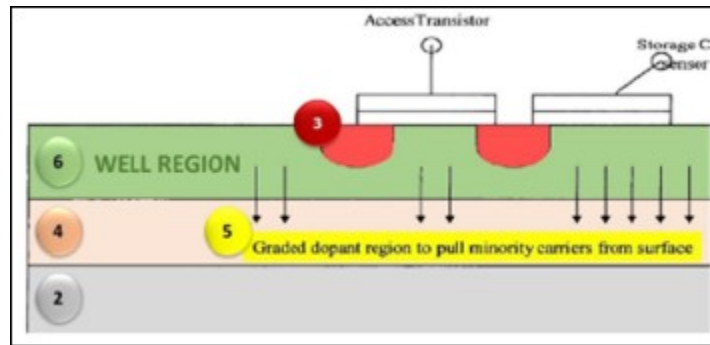
¶¶109-121.

**Well region disposed in the single drift layer...having a graded concentration of dopants** – As detailed above in Sections X.A.1.e-f regarding elements [44.4] and [44.5], Payne’s “tub region” 15 is an example of the claimed single drift layer. As shown below, Payne’s “surface region” 18 (green) disposed in tub region 15 (tan) is an example of a well region (a shallow well) disposed in Payne’s single drift layer (tub). EX1005, 1:65-68, 4:31-39, 5:7-14, 5:44-55; EX1003, ¶¶110-116. Payne’s surface region 20 (green) is another well region disposed in a single drift layer (tub 17). EX1005, 1:65-68, 4:63-5:14, 5:44-55; EX1003, ¶110; see supra Section X.B.1.e.



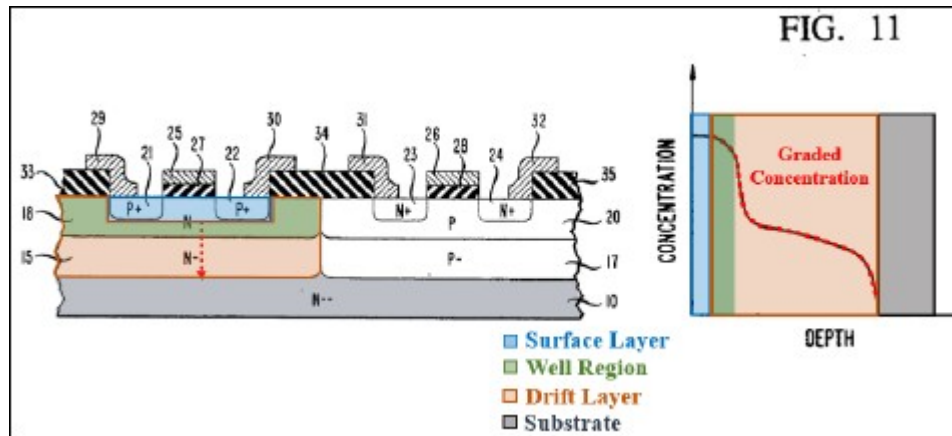
EX1005, FIG. 10.

Notably, Payne satisfies element [44.6] to the same extent that Figure 5(b) of the ‘222 Patent, annotated by Patent Owner (as shown below), meets it:



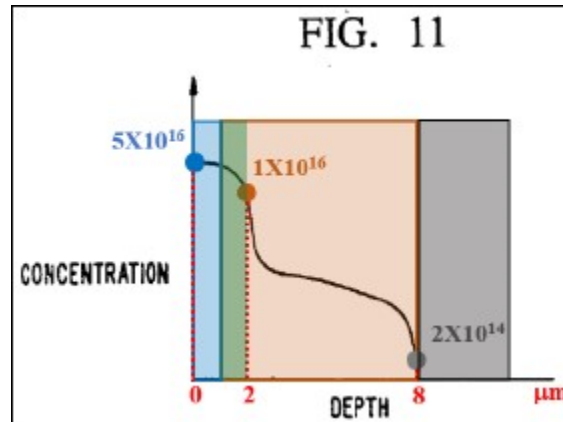
EX1001, FIG. 5(b); EX1030, 7.

As detailed above with respect to element [44.4], Payne’s Figure 11 (below right) illustrates the dopant concentration measured along the red dotted line in Figure 10 (below left). As shown, Payne’s well region (“surface region 18”) (green)—disposed in the single drift layer (tub 15) (tan border)—has a graded-dopant concentration that is downward-sloping with increasing depth. EX1003, ¶¶110-116; *supra* Section X.A.1.e.



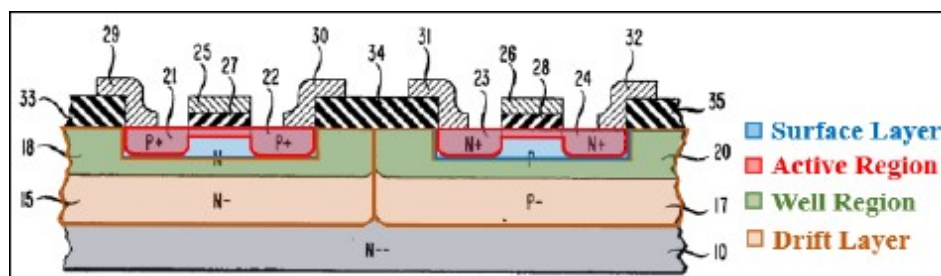
EX1005, FIGS. 10-11. As discussed in Section X.A.1.e, Payne discloses that Figure 11 illustrates a “*high-low implant profile*” that is downward-sloping with depth, such as from  $5 \times 10^{16}$  ions/cm<sup>3</sup> (near the top surface of the silicon/surface layer (blue))

to  $1 \times 10^{16}$  ions/cm<sup>3</sup> near the bottom of well 18 (green), to  $2 \times 10^{14}$  ions/cm<sup>3</sup> near the bottom of the single drift layer (tub 15) (tan). *Id.*, 2:56-59, 5:48-57; EX1003, ¶¶110-116.



EX1005, FIG. 11.

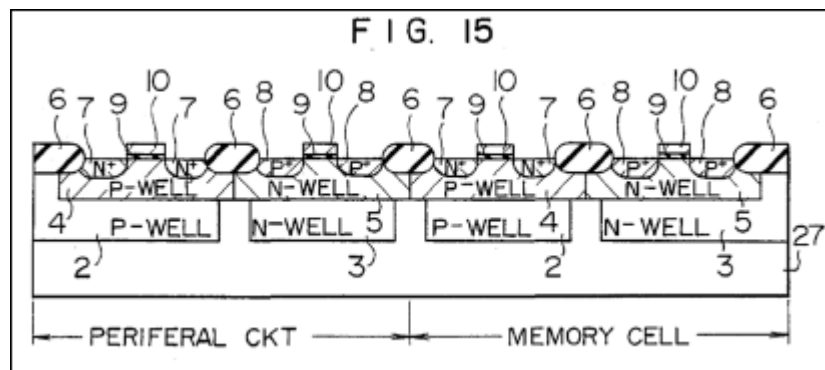
In light of the above, Payne satisfies element [44.6] under Patent Owner’s construction that the term “well region” should be accorded plain meaning and is “a doped region that surrounds the active region of a semiconductor device.” EX1033. As shown in Figure 10 below, the well region (green) is a doped region that surrounds the surface layer (blue) and the active region (red) therein. EX1003, ¶¶110-116.



EX1005, FIG. 10.

Payne also satisfies Intel’s proposed construction of “well region” to mean “[a] well, whether formed by single or multiple implants. Portions of a well are not well regions.” EX1033. Each surface region 18/20 is a well (and not a portion of a well) formed with an ion implant of phosphorous or boron. EX1003 ¶¶110-116; EX1005, 4:31-39, 4:63-5:5, FIGS. 7, 9.

In addition, as discussed in Section X.B, Sakai teaches a nested structure similar to Payne, which Sakai refers to as “twin double well.” *See, e.g.*, EX1006, 7:19-37 (“The memory of FIG. 15 has a ***twin double well*** structure ...made up of the ***deep*** P-well region 2, the ***deep*** N-well region 3, the ***shallow*** P-well region 4 and the ***shallow*** N-well region 5”).

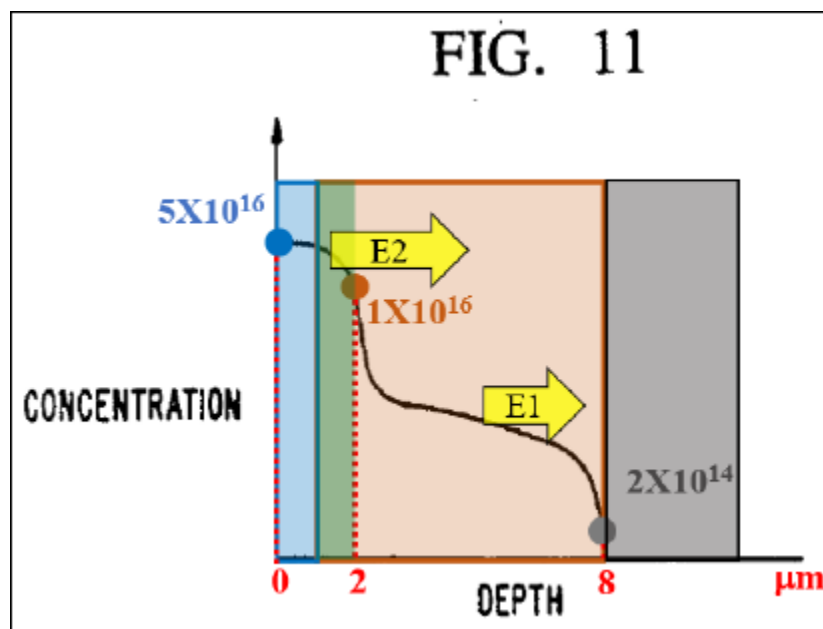


EX1006, FIG. 15; 1:57-67, 5:56-6:4, FIG. 10B, FIGS. 3, 8-9, 11E. Sakai confirms that Payne’s “surface region” is a shallow well region. EX1003, ¶¶110-116.

**Second static unidirectional electric drift field to aid the movement of Carriers** – According to Section X.A.1.f—including Applicant’s repeated representations during prosecution of the parent ‘195 Patent, the Jastrzebski and Kamins prior art relied on by Applicant during its prosecution, and Patent Owner’s

statements in its claim construction brief—the downward-sloping graded-dopant concentration in the well region generates a (second) static unidirectional electric drift field that aids the movement of minority carriers from the surface layer to the area of the substrate where there are no active regions. EX1003, ¶¶117-121; *supra* Section X.A.1.f. Further, Payne’s graded-dopant profile, including the profile in the well region, is set once the device has been fabricated and does not change, making the profile (and any resulting electric field) static, as described in Section X.A.1.f.

Payne’s Figure 11 is further annotated below to show the exemplary first static unidirectional electric drift field (“E1”) present in a deep portion of the single drift layer (discussed in Section X.A.1.f), and a different, exemplary second static unidirectional electric drift field (“E2”) present in the well region disposed in the single drift layer. EX1003, ¶¶117-121; *see also* fn.6.



EX1005, FIG. 11. Moreover, E1 and E2 are illustrated as electric fields having

different magnitudes, to reflect the different local slopes (gradients) of the graded-dopant profile. EX1003, ¶¶117-121; EX1022, [0071] (“the vertical  $\epsilon$ -field ... is established by the rate of change in the graded dopant concentration, i.e., the greater the rate of change ... the greater the intensity of the  $\epsilon$ -field.”).

In light of the above, Payne satisfies element [44.6] under Patent Owner’s plain-meaning construction of “to aid the movement of [] carriers”. EX1033; EX1003, ¶¶117-121. Payne’s Figure 11 shows that the dopant concentration is downward-sloping with increasing depth over the entire well region, and thus, according to Patent Owner (and also in light of Applicant’s representations to the Patent Office, discussed in Section X.A.1.f), creates a static unidirectional electric drift field that aids the movement of minority carriers downward from the surface layer to the substrate (specifically, to the area of the substrate where there are no active regions). EX1030, 2, 29; EX1003 ¶¶117-121. For the same reasons, Payne also satisfies this claim element under Intel’s construction that the second static unidirectional electric drift field must be “unidirectional over the well region,” and also satisfies Intel’s alternative proposed construction that “to aid the movement of [] carriers” means “to sweep the [] carriers from [the surface layer] to [the area of the substrate where there are no active regions.]” EX1033; *supra* Section X.A.1.f; EX1020, 289-290; EX1003, ¶¶117-121.

## **B. Ground II**

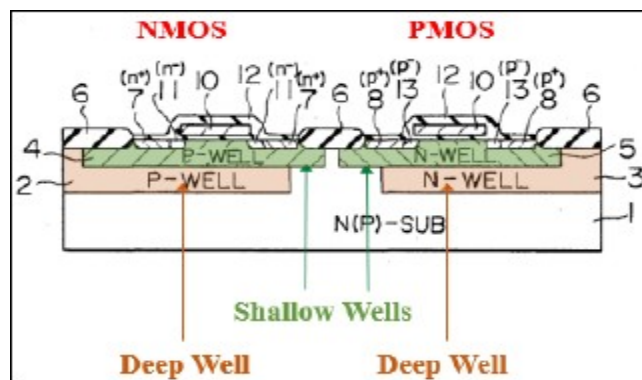
Sakai in combination with Kawagoe (hereinafter, “Sakai-Kawagoe”) renders

claim 44 obvious. EX1003, ¶¶122-178.

**1. Independent Claim 44**

**a Preamble: “A CMOS Semiconductor device comprising:”**

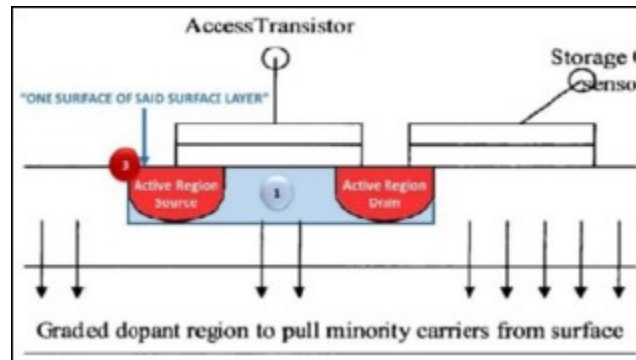
Sakai is directed to CMOS semiconductor devices. EX1003, ¶¶123-126; EX1006, Title, 1:6-13 (“The present invention relates to a complementary semiconductor device (hereinafter referred to as ‘CMOS’)”), 1:55-2:5. A CMOS device has “N-channel MOS [(NMOS)] transistor[s]” and “P-channel MOS [(PMOS)] transistor[s].” *Id.*, 4:15-29; EX1008A, 807-09. “[T]win-well” CMOS technology is a conventional structure that uses separate, side-by-side wells for the p- and n-type transistors, and is the technology focus of both Sakai and Kawagoe. EX1008B, 387-88; EX1006, 1:6-13, 7:19-23; EX1007, 14:46-55, 15:26-40, FIGS. 16, 21-24, 26-28. Sakai teaches a “twin *double* well” structure, whereby shallow wells (p-well 4 and n-well 5) (green) are formed in the wells (p-well 2 and n-well 3) (tan) of a conventional twin-well CMOS device, as shown in Figure 10D below. EX1006, 1:55-2:5, 5:53-6:4, 7:19-23, 7:32-37, 8:6-8; *compare* EX1006, FIG. 1 with FIGS. 2A, 3.



EX1006, FIG. 10D; *see also id.*, FIGS. 2A, 3, 8-9, 10A-10E, 11A-11E, 15-17, 3:18-43. While this Ground relies primarily on Sakai's Embodiment V (FIGS. 10A-E and accompanying discussion), which itself is based on Embodiment I (FIGS. 2A-B) (*see* EX1006, 5:53-55), Sakai discloses similar “twin double well” structures in the other embodiments and those embodiments are applicable for the same reasons as explained throughout this Ground. *Id.*, FIGS. 3, 8-9, 11A-11E, 15-17 (and accompanying discussion); EX1003, ¶¶123-126.

**b Element [44.1]: “a surface layer;”**

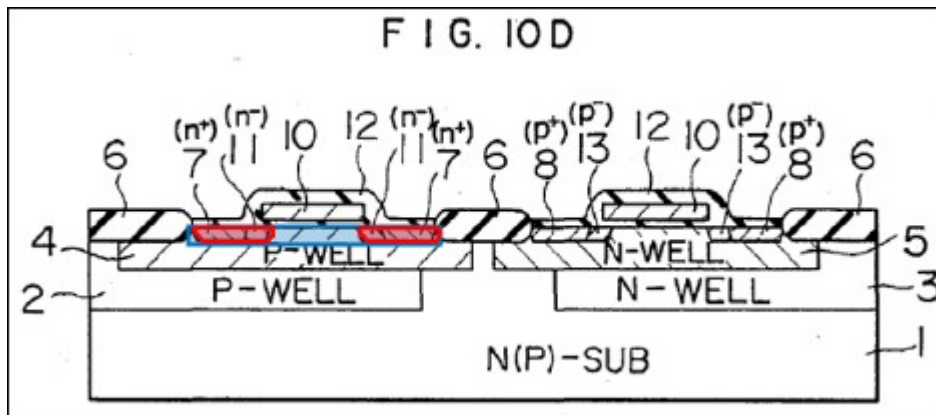
Sakai discloses or, at a minimum, renders obvious this element. EX1003, ¶¶127-129. According to Patent Owner, a “surface layer” is “a layer at the surface of the silicon” (or “a layer at the surface of the semiconductor device”)—which Patent Owner annotated in blue in Figure 5(b) below—“where the active region [(red)] is located.” EX1030, 6, 9, 12, 13; EX1033; *see supra* Section X.A.1.b.



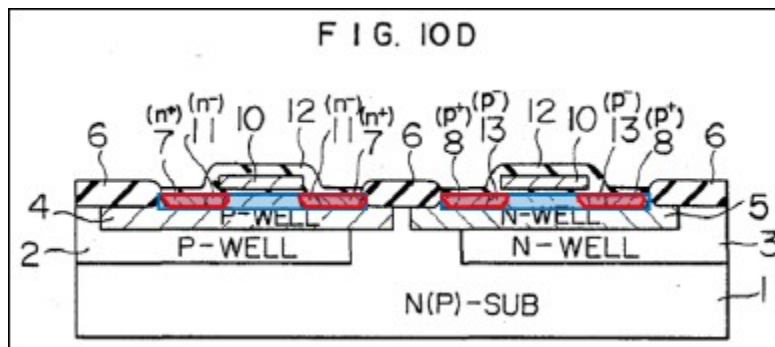
EX1001, FIG. 5(b); EX1030, 7, 12.

Sakai satisfies element [44.1] to the same extent that Figure 5(b) meets it. EX1003, ¶¶127-129. Sakai's Figure 10D discloses a surface layer (blue) that

matches the surface layer Patent Owner identified in Figure 5(b). Sakai's surface layer is at the surface of Sakai's silicon substrate 1, and the source and drain regions ("highly-doped N-diffusion layer 7") [(red)] of Sakai's N-channel MOS transistor (left) are located in it. EX1006, 1:28-30, 1:68-2:5, 4:25-29, 5:53-55, 5:59, 6:16-17; *see also* 2:51-58, 3:52-4:14, 5:24-32, 6:54-55.



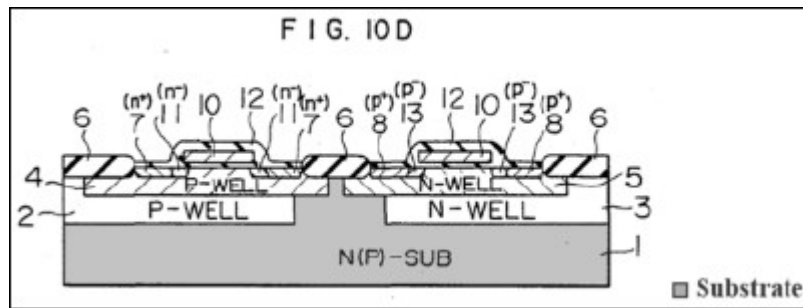
EX1006, FIG. 10D; *see also id.*, FIGS. 2A, 3, 8-9, 11A-11E, 15-17. Sakai likewise discloses a surface layer containing "highly-doped P-diffusion layer 8," which serves as the source/drain regions in the "P-channel MOS transistor" (below right). *Id.*, 1:68-2:5, 4:25-29, 5:53-55, 6:16-17; *see also id.*, 2:51-58, 3:52-4:14, 5:24-32, 6:54-55.



EX1006, FIG. 10D; *id.*, FIGS. 2A, 3, 8-9, 11A-11E, 15-17.

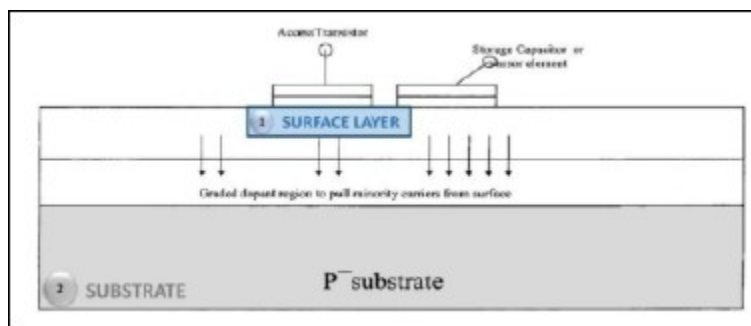
**c Element [44.2]: “a substrate;”**

Sakai discloses “a silicon substrate 1 [(grey below)] [] made of N-silicon or P- silicon.” EX1003, ¶¶130-132; EX1006, 4:13-14, 5:59; *id.*, 1:61, 6:26-27.



EX1006, FIG. 10D; *see also id.*, FIGS. 2A, 3, 8-9, 11A-11E, 15-17.

Sakai satisfies element [44.2] under Patent Owner’s proposed construction of “[p]lain [and ordinary] meaning”, where the plain and ordinary meaning is “an underlying layer.” EX1033. Sakai’s substrate also matches Patent Owner’s identification of substrate (grey) in Figure 5(b) of the ‘222 Patent.



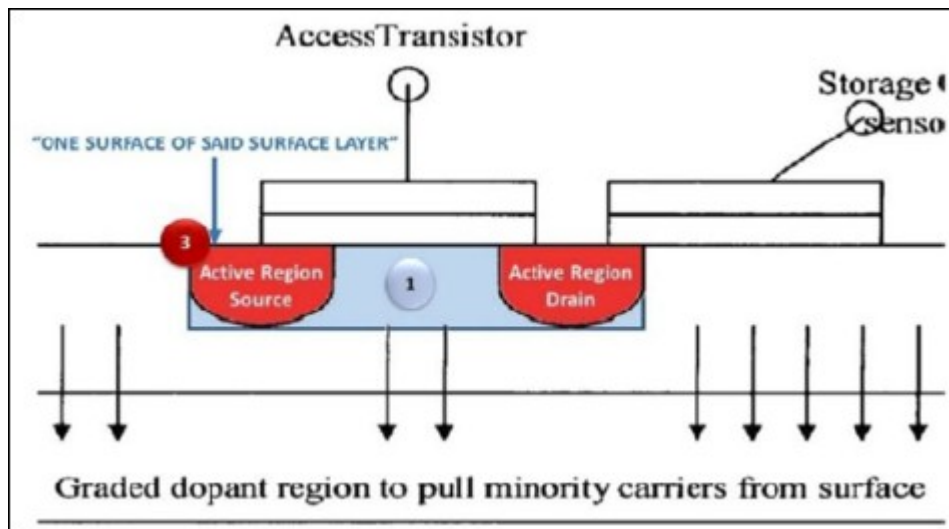
EX1030, 6-7, 16-17 (well region and drift layer can be part of substrate); EX1001, FIG. 5(b).

Sakai also satisfies this element under Intel’s proposed construction of

“substrate” because Sakai’s substrate is the initial material within which or on which Sakai’s semiconductor device is fabricated. EX1033; EX1003, ¶¶130-132; EX1006, 1:6-8, 5:53-61; *see also id.*, 1:57-2:5, 3:18-43, FIGS. 2A, 3, 8-9, 10A-10E, 11A-11E, 15-17.

**d Element [44.3]: “an active region including a source and a drain, disposed on one surface of the surface layer;”**

Sakai discloses or, at a minimum, renders obvious this element. EX1003, ¶¶133-138. As described in Section X.A.1.d, according to Patent Owner, Figure 5(b) of the ‘222 Patent depicts an active region (red) “disposed on one surface [(top surface)] of said surface layer.”

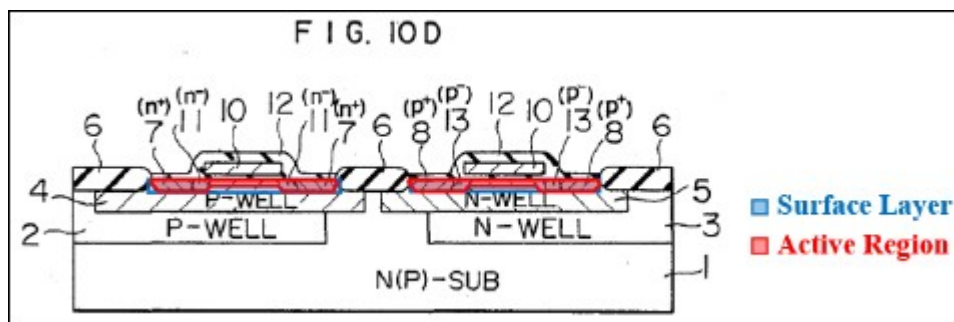


EX1001, FIG. 5(b); EX1030, 6-7, 10-12; *see supra* Section X.A.1.d.

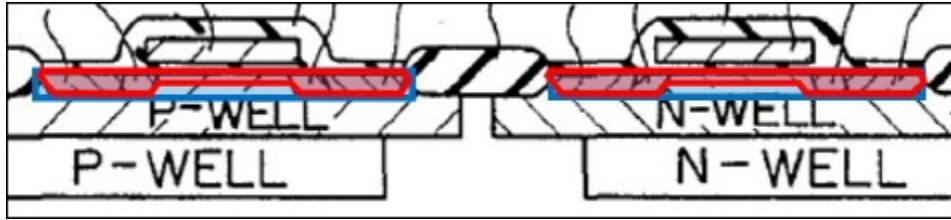
Sakai satisfies element [44.3] under Patent Owner’s interpretation. EX1003, ¶¶133-138. Sakai Figure 10D below illustrates an “N-channel” MOS transistor with source/drain regions (“highly-doped N...diffusion layers” 7) (left) in a doped shallow

P-well 4, and a “P-channel” MOS transistor with source/drain regions (“highly-doped ... P-diffusion layers” 8) (right) in a doped shallow N-well 5. EX1006, 1:27-32, 1:57-2:5, 4:25-29, 5:53-55, 5:64-6:4, 6:16-17; *id.*, 2:51-58, 3:524:14, 5:24-32, 6:52-58; *see supra* Section X.B.1.b. The source/drain regions of a p-channel or n-channel transistor, together with the channel region between them, form an active region. EX1003, ¶¶133-138; EX1008B, 299 (“The top surface of the [silicon substrate] body consists of active or transistor regions as well as passive or (field) regions. The **active regions** are those in which transistor action occurs; i.e., the **channel** and the heavily doped **source** and **drain** regions.”), 300, FIG. 5-2, 382, FIG. 6-8(c), 387, FIG. 6-10; EX1008C, 525, FIG. 8-1(e).

The active region (red) of each of Sakai’s transistors is disposed on one surface (top surface) of a corresponding surface layer (blue), exactly as depicted in Patent Owner’s annotated Figure 5(b) above. EX1003, ¶135; *supra* Section X.B.1.b.

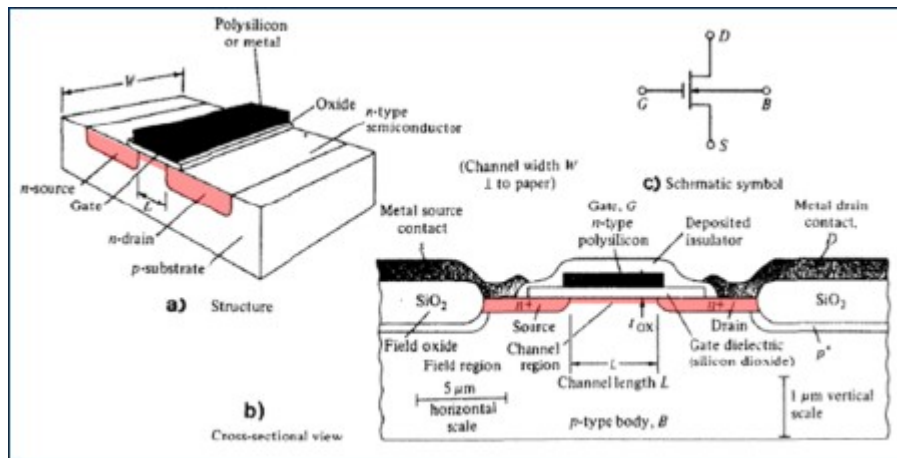


EX1006, FIG. 10D; *see also id.*, FIGS. 2A, 3, 8-9, 11A-11E, 15-17. For clarity, an enlarged version of Sakai’s active regions and surface layers is below.



EX1006, FIG. 10D (excerpted).

Sakai satisfies element [44.3] under Patent Owner’s position that the term “active region” means “a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed” (EX1033) because the active region of a MOS transistor is “[its] channel and [its] heavily doped source and drain regions,” highlighted in red below. EX1008B, 299; EX1003, ¶¶133-138.



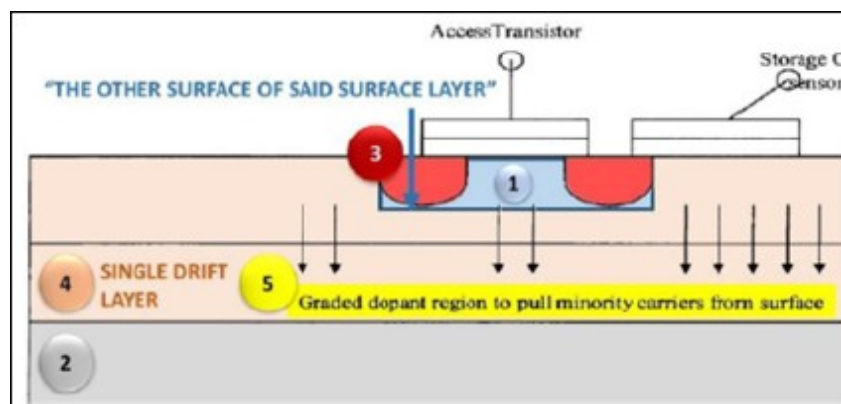
EX1008B, FIG. 5-1; *id.*, 298-301, 374, FIGS. 5-2, 6-4. Sakai also satisfies this element under Intel’s proposed construction that an active region is the “region that forms the current path of a device” or “the source, drain and channel region of a device” because current flows through the channel region that connects the source

and drain regions of a transistor when the transistor is active (when an appropriate voltage is applied to its gate). EX1033; EX1008B, 299-301, FIGS. 5-1, 5-2; EX1008D, 197, FIG. 5-13; EX1003, ¶¶133-138. Patent Owner does not dispute this. EX1030, 3-4 (“[w]hen a positive voltage is applied to the gate ... a conductive channel [is formed] between the source and the drain, and current can begin to flow through the transistor”).

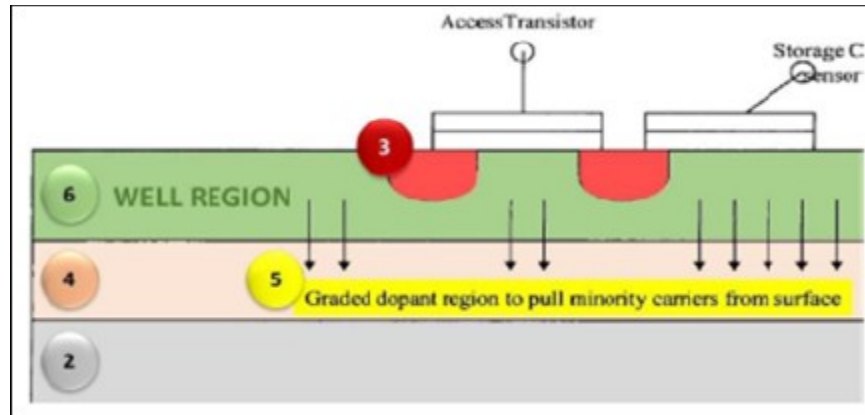
- e **Element [44.4]: “a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate,”**

Sakai-Kawagoe renders obvious this element. EX1003, ¶¶139-159.

**Single drift layer** – As described in Section X.A.1.e, according to Patent Owner, Figure 5(b) of the ‘222 Patent depicts a single drift layer (tan) “disposed between ‘the other surface [(bottom surface)] of said surface layer [(blue)]’ and [said] substrate [(grey)]”:

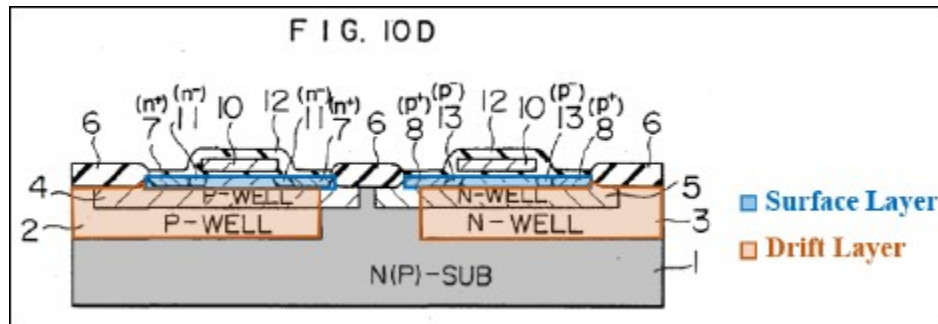


EX1001, FIG. 5(b); EX1030 at 7. The single drift layer in Figure 5(b) has a well region (green) disposed in it, forming a nested structure, as required by the claim (*see* element [44.6]):



EX1001, FIG. 5(b); EX1030, 7; *id.*, 11 (“the ‘well region’ is part of the ‘single drift layer.’”).

Sakai-Kawagoe meets a single drift layer to the same extent Figure 5(b) of the ‘222 Patent does. EX1003, ¶¶140-143. In Sakai’s Figure 10D, the “deep P-well region 2” (left) of Sakai’s nested well structure—with shallow P-well region 4 disposed in it—is an example of the claimed drift layer. *Id.*; EX1006, 5:56-6:4, 1:57-67, 7:32-37; *see also id.*, 6:24-28, 6:52-58. This single drift layer (tan) is “disposed between ‘the other surface [(bottom surface)] of said surface layer [(blue)]’ and said substrate [(grey)]” under Patent Owner’s interpretation, and in exactly the same way as depicted in Patent Owner’s annotated Figure 5(b) above. EX1030, 16.

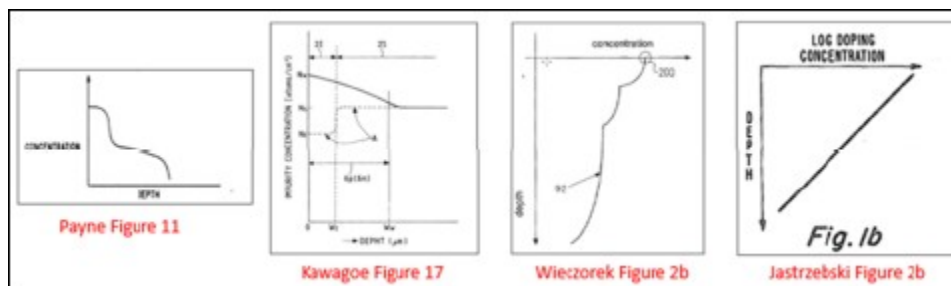


EX1006, FIG. 10D; *see also id.*, FIGS. 2A, 3, 8-9, 11A-11E, 15-17. Sakai’s “deep N-well region 3” (right), in which “shallow N-well region 5” is disposed, is likewise a single drift layer (tan) disposed between a surface layer (blue) and the substrate (grey). *Id.*, 5:56-6:4, 1:57-67, 7:32-37; *see also id.*, 6:24-28, 6:52-58; EX1003, ¶¶140-143; *see supra* Section X.B.1.b.

Sakai-Kawagoe meets all other claim requirements associated with the single drift layer to the same extent Figure 5(b) meets them, as explained below. *See* elements [44.5]-[44.6]; EX1003, ¶¶143-151. Notably, as detailed in element [44.5], each of the deep wells 2/3 in Sakai-Kawagoe is a *single* drift layer because it has a graded-dopant concentration that, according to Patent Owner, creates a unidirectional electric drift field that aids the movement of minority carriers in a *single* direction—from the surface layer to the substrate. EX1030, 7: EX1020, 253-54, 289-290; *infra* Section X.B.1.f.

**Graded concentration of dopants extending between the surface layer and the substrate** – Sakai-Kawagoe renders obvious a single drift layer having a graded concentration of dopants extending between the surface layer and the

substrate. EX1003, ¶¶144-151. For example, the single drift layer (e.g., deep P- well 2 (above left) with shallow P-well 4 disposed in it) has a **high-to-low** dopant concentration, whereby the “shallow P-well region 4” has “an impurity concentration of  $5 \times 10^{16}$  to  $10^{18}$  atoms per  $\text{cm}^3$ ,” which is up to **two orders of magnitude higher** than the dopant concentration in the deep “P-well region 2,” which is in the range of “ $10^{15}$  to  $10^{16}$  atoms per  $\text{cm}^3$ .” EX1006, 5:56-6:4; EX1003, ¶¶144-151. The same applies to the single drift layer formed by deep N-well 3 (above right) with shallow N-well 5 disposed in it. *Id.* A POSITA would have understood that Sakai’s **high-to-low** concentration is **gradually decreasing** across Sakai’s single drift layer because it is formed “through ion implantation techniques and thermal diffusion techniques.” EX1006, 5:56-6:4, 6:24-28, 6:52-58, 8:35-38; EX1003, ¶¶144-151. Indeed, a downward-sloping graded-dopant concentration formed through ion implantation and thermal diffusion was well-known in the art. And such gradients were disclosed in many prior art references, such as Payne, Kawagoe, Wiczorek and Jastrzebski, as shown below.

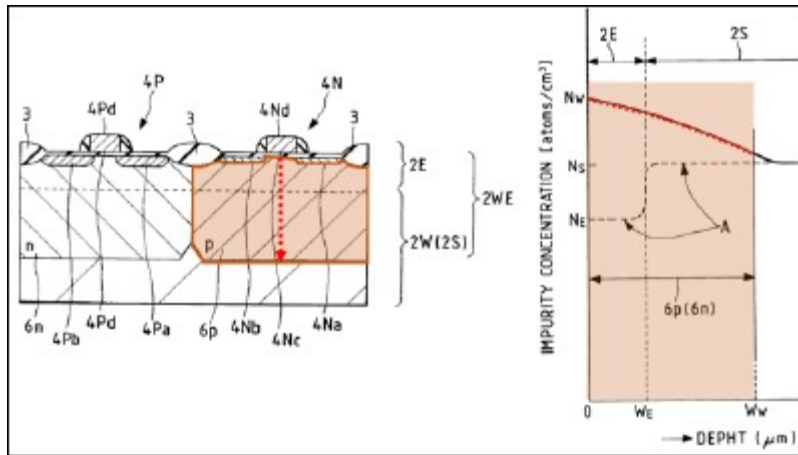


EX1005, FIG. 11, 3:28-42, 4:19-39, 5:7-17; EX1007, FIG. 17, 15:62-16:2, 17:3161;

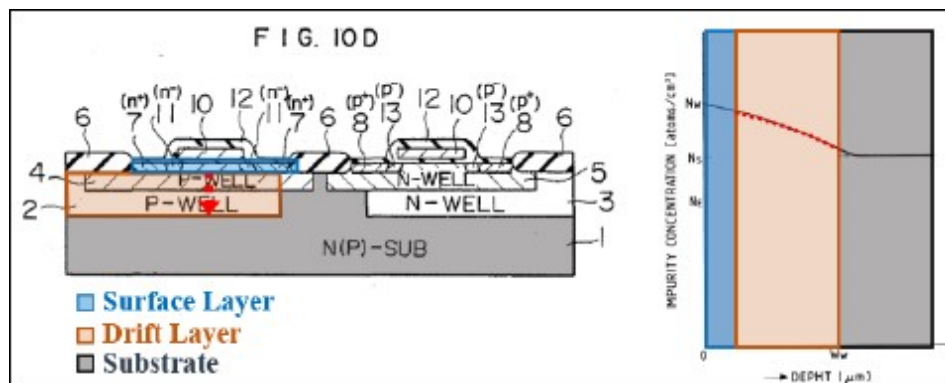
EX1038, FIG. 2b, [0008], [0010]-[0011]; EX1010, FIG. 1b, 5:5-27; 9:2-8. Significantly, Payne’s Figure 11 illustrates a graded-dopant profile that is downward-sloping over a *nested well structure* similar to Sakai’s “*twin double well*” structure, as detailed in Sections X.A.1.e-f. EX1003, ¶¶144-151. Additionally, the ‘222 Patent mentions dopant gradients (“linear, quasi linear, exponential or complimentary error function”) only once and does not describe how to make them, confirming implementing them in CMOS devices was well-known. EX1001, 2:60-61. *Ex Parte Nico Hawley-Weld, Dan Volpe, & Ben Silverman*, No. APPEAL 2023- 000345, 2022 WL 17495059, at \*7 (P.T.A.B. Dec. 6, 2022) (“in the absence of specific description [in the specification], it is appropriate to assume that anyone desiring to perform the claimed function would know how to do so.”); *In re Epstein*, 32 F.3d 1559, 1568 (Fed. Cir. 1994). The ‘222 Patent also lists linear/quasi-linear among the other well-known gradients without giving any reason to use one over another. EX1001, 2:60-61. And, as further detailed below, a POSITA would have been motivated to combine Sakai with Kawagoe to ensure that the high-to-low dopant concentration taught by Sakai is implemented as a graded, downward-sloping concentration to protect Sakai’s devices against soft errors. EX1003, ¶¶144-151.

Kawagoe teaches that wells of a CMOS device such as “p-well 6p and n-well 6n” in Figure 23 (below left) “have their impurity concentrations *gradually lowered* in the depthwise direction” from the top surface of the silicon substrate (“principal surface”) to the bottom of the wells, as illustrated in Figure 17 (below right).

EX1007, 5:41-45, 8:46-52, 14:46-15:6, 15:26-40, 15:62-16:40, FIG. 16.



EX1007, FIGS. 23, 17. A side-by-side association of Sakai’s “twin double well” structure Figure 10D with Kawagoe’s dopant profile Figure 17 illustrates an example of Sakai’s high-to-low dopant concentration implemented in accordance with Kawagoe’s teaching that the overall dopant profile should be “gradually lowered in the depthwise direction.” EX1007, 15:62-16:7; EX1003, ¶¶149-151.



EX1006, FIG. 10D; EX1007, FIG. 17 (excerpted); *see also* EX1006, FIGS. 2A, 3, 8-9, 11A-11E, 15-17. Sakai’s high-to-low dopant concentration across deep N-well 3 (right side of Figure 10D) implemented in accordance with the same teachings of

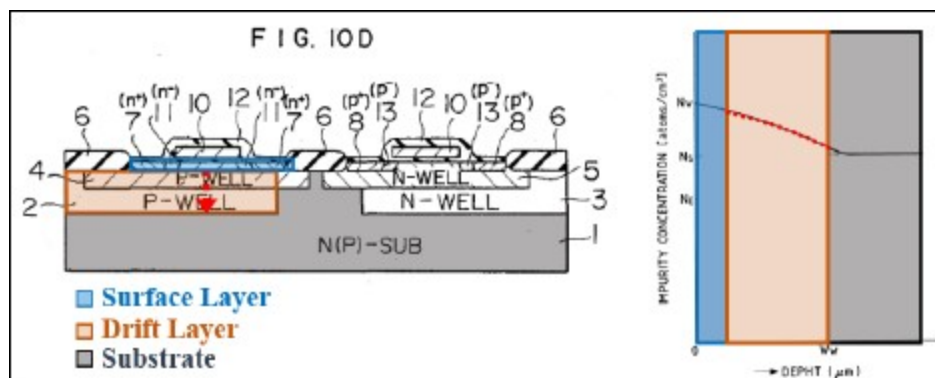
Kawagoe would similarly result in a gradual downward-sloping profile. EX1003, ¶¶149-151. Accordingly, Sakai-Kawagoe meets a single drift layer having a downward-sloping graded concentration of dopants extending between the surface layer and the substrate. *Id.*

**Motivation to combine Sakai and Kawagoe** - A POSITA would have been motivated to combine Sakai and Kawagoe for numerous reasons. EX1003, ¶¶152-159. Both are Hitachi patents. EX1006, cover; EX1007, cover. Both are directed to CMOS devices that were (and still are) “widely used” to form memories and microcomputers because of their “low [] power dissipation” and because CMOS devices “can operate at high speed.” EX1006, 1:7-17, EX1007, 3:32-38, 19:15-16, 20:1-8, 21:5-12, 22:14-21, 24:28-31.

Sakai teaches improving the circuit density (packing density) of CMOS chips by disposing shallow wells into deep wells of a “twin-well” CMOS device to form a “twin double well” structure (nested well structure). EX1006, 1:55-2:5, 7:19-37, 8:9-24, FIGS. 2A, 10D, 15. Sakai’s “twin double well” structure is used to form high-packing-density memory devices, including SRAM memory devices illustrated in Figure 15 and discussed in Kawagoe. *Id.*, 7:24-37 (“[CMOS] static memory of...6 MOS transistors”); EX1008B, 572-573 (“SRAMS... are... static memories), FIG. 8-2 (CMOS SRAM cell); EX1007, 21:5-12, FIG. 27(B). High-packing-density SRAMs are susceptible to soft errors. EX1008B, 583 (“SRAMs offer better resistance than DRAMs to [soft-errors] ... However, as geometries have been scaled

down to produce circuits of greater density, alpha-particle-induced soft-error rates have also become a concern in SRAMs.”); EX1003, ¶¶152-159.

A POSITA would thus have been motivated to apply Kawagoe’s teachings directed to protecting memories against alpha-particle-induced soft errors to Sakai’s twin double well structure (including for SRAM memory). EX1003, ¶¶152-159. A POSITA would have engineered the dopant profile across each of Sakai’s single drift layers (tan) so that it is downward-sloping from the top surface of the silicon substrate to the bottom of the deep well—as illustrated in the dopant profile at right—because Kawagoe teaches that such a profile causes alpha-particle-generated minority carriers to move to the substrate. EX1007, 16:2-11 (the “gradient [in the p-well] [] is **gradually lowered** in the depthwise direction” and, as a result, “electrons produced by the  $\alpha$ -ray are attracted to the substrate body 2S by that concentration gradient ... so that the soft errors can be reduced ”), 21:20-23; EX1003, ¶¶152-159.

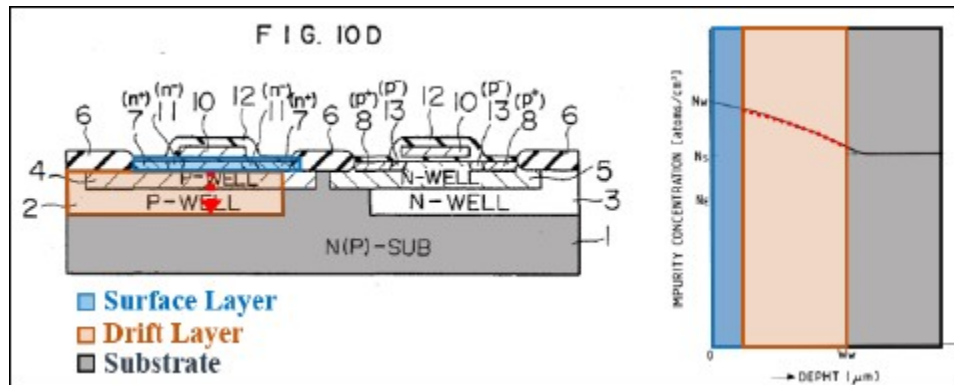


EX1006, FIG. 10D; EX1007, FIG. 17 (excerpted); *see also* EX1006, FIGS. 2A, 3, 8-9, 11A-11E, 15-17. Such a downward-sloping dopant profile is consistent with Sakai’s teachings of (1) higher dopant concentration in the shallow wells compared

to the deep wells, and (2) the use of ion implantation followed by thermal drive-in, which naturally results in a non-uniform, graded-dopant concentration, discussed above. EX1006, 5:56-6:4; EX1003, ¶¶152-159. There is a reasonable expectation of success because it was well-known that various ion-implantation and thermal drive-in processes enable different dopant profiles to be readily engineered and fabricated as needed, EX1008A, 371, 373 (“Complex-doping profiles can be produced” using ion implantation), and because the prior art is replete with teachings on how to form downward-sloping dopant concentrations, as in Kawagoe, Payne, Jastrzebski and Wieczorek. EX1003, ¶¶152-159. Further, the ‘222 Patent specification mentions various dopant gradients (including ones with a one-way slope, *e.g.*, quasi-linear) and does not illustrate or otherwise describe how to make them, confirming that such gradients were well-known and a POSITA would have known how to manufacture a CMOS device having them. EX1001, 2:60-61; *Ex Parte Hawley-Weld* at \*7; *In re Epstein*, 32 F.3d at 1568. Accordingly, a POSITA would have equally known how to implement a single drift layer in Sakai to result in a known downward-sloping graded-dopant concentration profile. This combination also merely amounts to (1) combining prior art elements (Sakai’s CMOS device and Kawagoe’s dopant profile) according to known methods (well-known ion implantation and thermal drive in techniques) to yield predictable results and (2) use of a known technique (creating Kawagoe’s profile) to improve similar devices (Sakai’s CMOS devices) in the same way (to reduce soft errors).

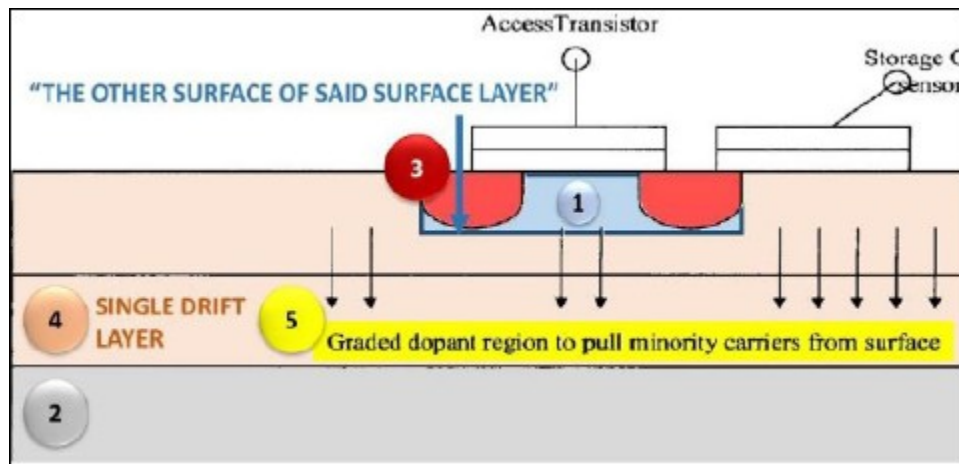
- f **Element [44.5]: “the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and”**

Sakai-Kawagoe renders obvious this element. EX1003, ¶¶160-167. As discussed above with regard to element [44.4], Sakai-Kawagoe renders obvious a single drift layer (tan) having a downward-sloping dopant concentration extending between the surface layer (blue) and the substrate (grey), similar to Kawagoe Figure 17 below. *See supra* Section X.B.1.e.



EX1006, FIG. 10D; EX1007, FIG. 17 (excerpted); *see also* EX1006, FIGS. 2A, 3, 8-9, 11A-11E, 15-17. And, as is clear from Figure 10D, there are no active regions in the area of the substrate below the wells (grey) because the active regions in Sakai are at the surface of the silicon substrate, as in any CMOS device. *See* Section X.B.1.d; EX1008B, 299 (“The **top surface** of the [silicon substrate] body **consists of active or transistor regions** as well as passive or (field) regions. The **active regions** are those in which transistor action occurs; i.e., the **channel** and the heavily doped **source** and **drain** regions.”), 300-301, FIG. 5-2, 382, FIG. 6-8(c), 387, FIG. 6-10;

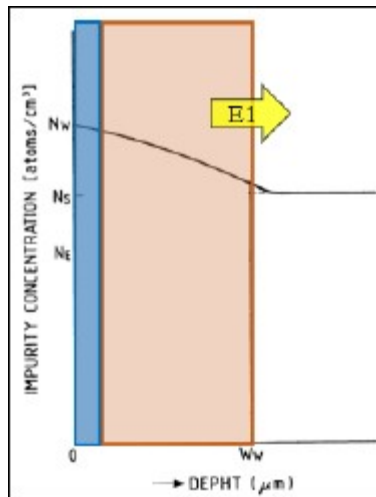
EX1008C, 525, FIG. 8-1(e). EX1003, ¶¶160-165. Sakai in fact satisfies element [44.5] to the same extent shown in Figure 5(b) of the '222 Patent, where the active regions (red) are at the surface of the silicon substrate, and the substrate below the single drift layer is blank, just as in Sakai. *Id.*



EX1001, FIG. 5(b); EX1030, 7. Indeed, Patent Owner admits that active regions would be understood as being at the surface of the silicon substrate and therefore they are not located in Sakai's substrate area below the wells (grey). EX1030, 19 ("A POSITA ... would understand that an **active region** [(red)] is a doped silicon region **at the surface** of a semiconductor device where a transistor can be formed."), 11, 12 ("[T]he surface layer at the surface of the semiconductor device [is] where the active region is located."), 14 ("The claims make clear that the active region is part of the surface layer ..."); EX1033; EX1003, ¶¶160-165.

Thus, according to Section X.A.1.f—including Applicant's repeated representations to the Patent Office and the Jastrzebski and Kamins cited art relied on by Applicant—Sakai-Kawagoe's downward-sloping graded-dopant

concentration extending between the surface layer (blue) and the substrate (grey) in Sakai's Figure 10D creates a "built-in" unidirectional electric drift field (illustrated "E1" below) to aid the movement of minority carriers from the surface layer to an area of the substrate where there are no active regions. EX1003, ¶¶160-165; *supra* Section X.A.1.f; *see also* fn.6.



EX1007, FIG. 17 (excerpted). Such a profile is created "through ion implantation techniques and thermal diffusion techniques" and thus the profile (and any resulting electric drift field) is static—it is set once the CMOS device has been fabricated and does not change afterwards. EX1003, ¶¶160-165; EX1006, 5:56-6:4, 6:24-28, 6:52-58, 8:35-38; *supra* Section X.A.1.f. As discussed in Section X.A.1.f, Applicant described "static" similarly during prosecution of the parent '195 Patent. EX1020, 318 (citing EX1009), 333 (same).

In light of the above, Sakai-Kawagoe satisfies element [44.5] under Patent Owner's plain-meaning constructions. EX1033; EX1003, ¶¶160-166. Sakai-

Kawagoe’s graded-dopant concentration is downward-sloping over the entire single drift layer (tan)—in fact, from the top of the silicon/surface layer (blue) to the bottom of the single drift layer—and thus, according to Patent Owner (and also in light of Applicant’s representations to the Patent Office discussed above), creates a static unidirectional electric drift field that aids the movement of minority carriers from the surface layer to the substrate (specifically to an area of the substrate where there are no active regions). EX1007, FIG. 17; EX1003, ¶¶160-166.

For the same reasons, Sakai-Kawagoe satisfies Intel’s construction that the first static unidirectional electric drift field must be “unidirectional *over* the drift layer,” and also satisfies Intel’s alternative proposed construction of the sub-phrase “to aid the movement of [] carriers from the surface layer to an area of the substrate where there are no active regions” to mean “to sweep the [] carriers from [the surface layer] to [an area of the substrate where there are no active regions].” *Id.*, EX1033; *supra* Section X.A.1.f; EX1020, 289-290; EX1003, ¶¶160-167.

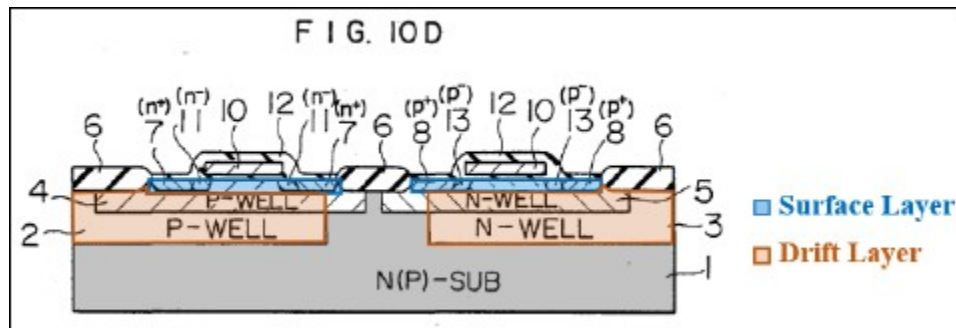
- g Element [44.6]: “at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.”**

Sakai-Kawagoe renders obvious this element. EX1003, ¶¶168-178.

Well region disposed in the single drift layer...having a graded **concentration of dopants** – As detailed above, Sakai-Kawagoe renders obvious a single drift

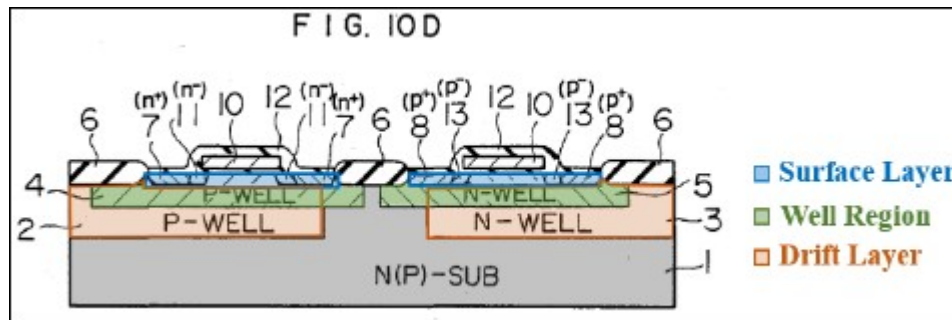
layer (deep P-well 2 or deep N-well 3) (tan), as shown below. EX1006, 5:56-6:4.

Sections X.B.1.e-f; EX1003, ¶¶169-174.



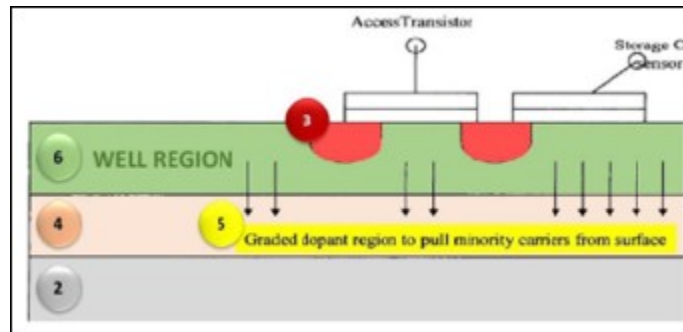
EX1006, FIG. 10D; *id.*, FIGS. 2A, 3, 8-9, 11A-11E, 15-17.

Each shallow well in Sakai’s nested well structures (“twin double wells”)—*e.g.*, the “**shallow P-well region 4**” (left) or “**shallow N-well region 5**” (right)—is an example of a well region (green) disposed in a single drift layer (tan). EX1006, 1:57-67, 5:56-6:4, 7:32-37.

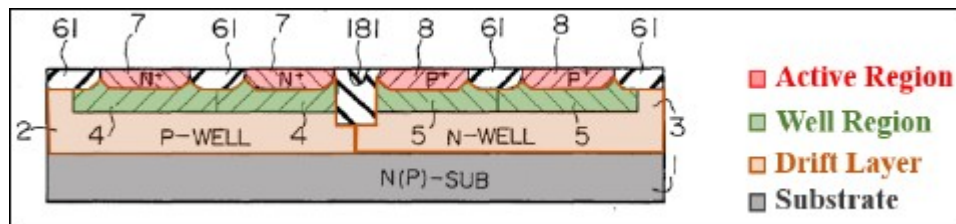


EX1006, FIG. 10D; *id.*, FIGS. 2A, 3, 8-9, 11A-11E, 15-17.

Notably, Sakai-Kawagoe satisfies element [44.6] to the same extent that Figure 5(b) of the ‘222 Patent, annotated by Patent Owner in its claim construction brief, meets it:

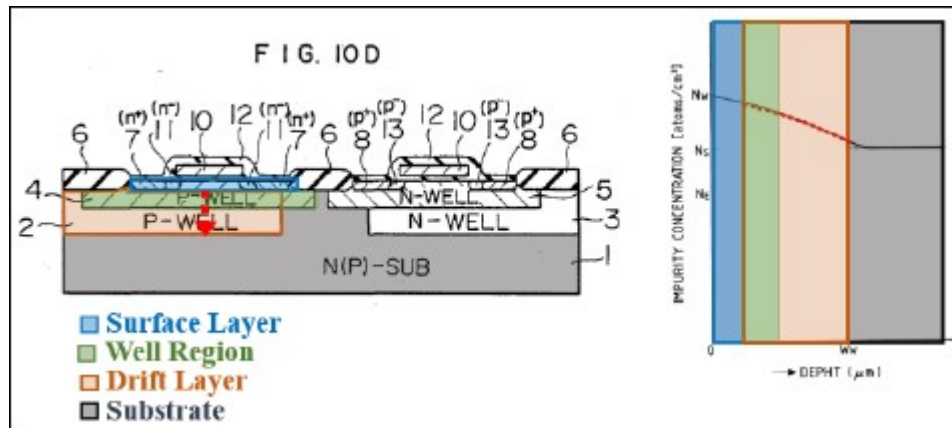


EX1001, FIG. 5(b); EX1030, 7. To the extent Patent Owner argues that the well region must be entirely contained within the single drift layer, Sakai discloses that too. *See, e.g.*, EX1006, FIGS. 11E (below), 3, 8-9, 16.



EX1006, FIG. 11E; *id.*, 1:29-30, 2:60-61, 6:22-31, 6:52-58.

Further, as also detailed above with respect to element [44.4], Sakai-Kawagoe's structure has a downward-sloping graded-dopant concentration extending between the surface layer and the substrate, such that each well region (e.g., shallow well 4) (green) also has such downward-sloping graded-dopant concentration. EX1007, 15:62-16:7 (dopant "concentrations gradually lowered in the depthwise direction from the principal surface"); EX1003, ¶¶169-174; *supra* Section X.B.1.e.



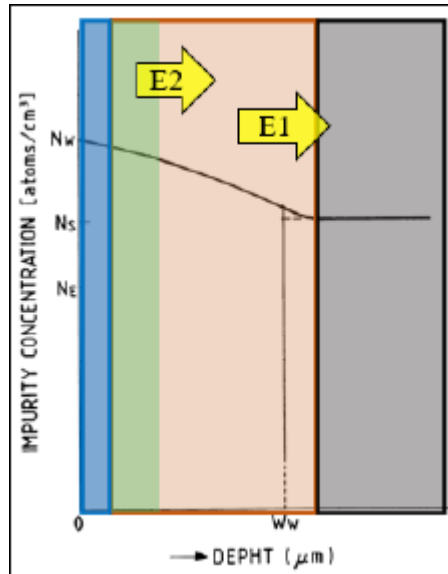
EX1006, FIG. 10D; EX1007, FIG. 17 (excerpted); *see also* EX1006, FIGS. 2A, 3, 8-9, 11A-11E, 15-17.

In light of the above, Sakai-Kawagoe satisfies element [44.6] under Patent Owner’s construction that the term “well region” means “a doped region that surrounds the active region of a semiconductor device.” EX1033; EX1003, ¶¶169-174. As shown in Sakai’s Figure 10D (with graded-dopant concentration shown in Kawagoe’s Figure 17) above, the exemplary shallow well region (green) is a doped region that surrounds both the surface layer (blue) and the active region therein. EX1003, ¶¶169-174; *supra* Section X.B.1.d. Sakai-Kawagoe also satisfies Intel’s proposed construction of this term. EX1033; EX1003 ¶¶169-174. The mapping of “well region” to each shallow well 4/5 satisfies Intel’s construction because they are formed with an ion implant of P-type or N-type impurities. EX1006, 5:64-6:4, 6:52-58; EX1033; EX1003 ¶¶169-174.

**Second static unidirectional electric drift field to aid the movement of carriers**—According to Section X.A.1.f—including Applicant’s repeated

representations during prosecution of the parent ‘195 Patent, the Jastrzebski and Kamins prior art relied on by Applicant during its prosecution, and Patent Owner’s statements in its claim construction brief—the downward-sloping graded-dopant concentration in the well region generates a (second) static unidirectional electric drift field that aids the movement of minority carriers from the surface layer to the area of the substrate where there are no active regions. EX1003, ¶¶175-178; *supra* Section X.A.1.f. Further, Sakai-Kawagoe’s graded-dopant profile, including the profile in the well region, is set once the device has been fabricated and does not change, making the profile (and any resulting electric field) static, as described in Section X.B.1.f.

Kawagoe’s Figure 17 is further annotated below to show the exemplary first static unidirectional electric drift field (“E1”) described in Section X.B.1.f, at a depth corresponding to Sakai’s deep well (tan), and an exemplary second static unidirectional electric drift field (“E2”), at a depth corresponding to Sakai’s shallow well (green) (exemplary well region disposed in the single drift layer). EX1003, ¶¶175-178; *see also* fn.6.



EX1007, FIG. 17 (excerpted); Ex. 1003, ¶¶176. Moreover, E1 and E2 are illustrated as electric fields having different magnitudes, to reflect the different local slopes (gradients) of the dopant profile. EX1003, ¶¶175-178; EX1022, [0071] (“the vertical  $\epsilon$ -field ... is established by the rate of change in the graded dopant concentration, i.e., the greater the rate of change ... the greater the intensity of the  $\epsilon$ - field.”).

In light of the above, Sakai-Kawagoe satisfies element [44.6] under Patent Owner’s plain-meaning construction of “to aid the movement of [] carriers.” EX1033; EX1003, ¶¶175-178. As shown in Kawagoe Figure 17 above, Sakai-Kawagoe’s graded-dopant concentration is downward-sloping over the entire well region, and thus, according to Patent Owner (and also in light of Applicant’s representations to the Patent Office, discussed in Section X.A.1.f), creates a static unidirectional electric drift field that aids the movement of minority carriers downward from the surface layer to the substrate (specifically, to the area of the

substrate where there are no active regions). EX1003, ¶¶175-178.

For the same reasons, Sakai-Kawagoe also satisfies this element under Intel’s construction that the second static unidirectional electric drift field must be “unidirectional over the well region,” and also satisfies Intel’s alternative proposed construction that the term “to aid the movement of [] carriers” means “to sweep the [] carriers from [the surface layer] to [the area of the substrate where there are no active regions].” EX1033; *supra* Section X.A.1.f; EX1020, 289-290; EX1003, ¶¶175-178.

## **XI. THE BOARD SHOULD INSTITUTE IPR**

### **A. 35 U.S.C. § 314(a)**

The merits of this Petition are strong, which alone warrants institution. On June 21, 2022, Director Vidal issued an interim procedure regarding application of the *Fintiv* factors clarifying that “the PTAB will not deny institution [] under *Fintiv* (i) when a petition presents compelling evidence of unpatentability.” Director Vidal, Memorandum, “Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation,” 9 (June 21, 2022). As just one example of compelling evidence here, Ground I is a single-reference obviousness ground explaining how Payne discloses or, at a minimum, renders obvious the Challenged Claim. This evidence, “if unrebutted in trial, would plainly lead to a

conclusion that one or more claims are unpatentable” (*id.*, 4), thus the Board should decline to exercise its discretion under §314(a). *Id.*; *PopSockets LLC v. Flygrip, Inc.*, IPR2022-00938, Paper 8 (P.T.A.B. Nov. 1, 2022).

The *Fintiv* factors also weigh in favor of institution.

**Factor 1 (Stay)**—This factor is neutral as neither party has requested a stay.

**Factor 2 (Trial Date)**—Patent Owner’s complaint was filed on April 6, 2023 in the Eastern District of Texas (E.D. Tex.). EX1101. In the Docket Control Order for the related district court proceeding, the Court has set jury selection date of March 3, 2025. EX1102, 2. A final written decision (“FWD”) for the IPR proceeding that this petition seeks to join is anticipated on February 12, 2025.

*Semiconductor Components Industries LLC v. Greenthread, LLC*, IPR2023-01244, Paper 33. There is therefore “a reasonable likelihood that the Board will address the overlapping validity issues prior to the district court reaching them at trial..., thereby providing the possibility of simplifying issues for trial.” *Juniper Networks, Inc. v. Packet Intelligence LLC*, IPR2020-00339, Paper 21 at 18 (P.T.A.B Sept. 10, 2020).

The Board should therefore not deny institution as the Final Written Decision of the joined proceeding will occur prior to the beginning of the District Court trial. Even if the average time to trial is considered, this still disfavors discretionary denial.

Based on a median time from filing to trial in E.D. Tex. of 21.4 months, the disposition date is mid-January, 2025. EX1103, 35. Even in the unlikely event that the court accelerates the scheduled deadlines in the case to meet a mid-January 2025

trial date, with a gap of less than a month between the expected FWD and start of trial (based on median time to trial), the “efficiency and system integrity concerns that animate the *Fintiv* analysis are not as strong all other things being equal.”

*Google LLC v. Parus Holdings, Inc.*, IPR2020-00846, Paper 9 at 14 (PTAB Oct. 21, 2020).

**Factor 3 (Investment)**—The bulk of investment in the Related Litigation by the parties and court has yet to occur. By the time of institution in this proceeding, the Related Litigation will be at a similar posture where “much of the district court’s investment relates to ancillary matters untethered to the validity issue itself.” *Sand Revolution*, IPR2019-01393, Paper 24 at 10-11.

**Factor 4 (Overlap)**—Invalidity contentions for the Related Litigation have not yet been submitted, so there are currently no overlapping issues between the two proceedings. Furthermore, as discussed above, the scheduled jury selection date of March 3, 2025 indicates that issues of validity will be settled by the PTAB prior to the beginning of the related District Court trial.

**Factor 6 (Merits and Other Circumstances)**—The strength of the merits alone is enough to justify institution in the public interest, and outweighs any inefficiencies born of parallel litigation. *See Fintiv* at 15; Memorandum on Interim Procedure for Discretionary Denials (June 21, 2022). Petitioner has been diligent in filing this Petition and has actively sought to reduce the burden on the office by filing a copycat petition with a motion for joinder rather than a petition based on

separate merits arguments not already before the Board.

**B. 35 U.S.C. § 325(d)**

The Board should likewise not deny institution under §325(d) because all six *Becton Dickinson* factors weigh in favor of institution. *Becton, Dickinson, & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (P.T.A.B. Dec. 15, 2017); *see also Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (P.T.A.B. Feb. 13, 2020) (precedential).

The Board has consistently “held that a reference that ‘was neither applied against the claims nor discussed by the Examiner’ does not weigh in favor of exercising ... discretion under §325(d).” *Fasteners for Retail, Inc. v. RTC Indus., Inc.*, IPR2019-00994, Paper 9 at 7-11 (P.T.A.B. Nov. 5, 2019). Here, Kawagoe was not cited, and thus the Examiner did not consider the Sakai-Kawagoe ground (Ground II) set forth in this Petition. *Advanced Bionics*, Paper 6 at 8. And although Payne and Sakai were cited, they were not discussed by the Examiner or Applicant during prosecution of the ‘222 Patent. EX1002. Indeed, there was no prior art-based rejection and the Examiner stated that a single reference, Hong (EX1027), is “the closest reference” to every claim, including the Challenged Claim. EX1002, 226-229. Specifically, with regard to the Challenged Claim, the Examiner stated: “Similarly, claim 44 is allowed because the prior art of record does not teach or suggest, singularly or in combination, at least the limitations of ‘a second static unidirectional electric drift field to aid the movement of carriers from the surface

layer to the area of the substrate where there are no active regions’ (see last 3 lines). ***Again, the closest reference is Hong.***” *Id.*, 228-229. But, as noted above, Hong is not prior art because it was filed on August 31, 2005, long after the claimed priority date of the ‘222 Patent. EX1027.

In sum, the prosecution history makes clear that the Examiner erred in a manner material to the patentability of the Challenged Claim. *Advanced Bionics*, Paper 6 at 8; *Peloton Interactive, Inc. v. iFit, Inc.*, IPR2022-00030, Paper 12 at 16 ((P.T.A.B. Apr. 22, 2022)). In particular, the Examiner overlooked teachings of Payne and Sakai that are pertinent to the Challenged Claim, as this Petition demonstrates.

Further, Payne, Sakai, and Kawagoe are not cumulative to any art cited or discussed during prosecution of the ‘222 Patent’s parents, such as Rhodes, Jastrzebski, Kamins, or Hueting. Indeed, other than during prosecution of the parent ‘195 and ‘502 Patents, prosecution of the other parent applications involved claims that are wholly different from the Challenged Claim. *Fasteners for Retail*, IPR2019-00994, Paper 9 at 10 (refusing to deny institution because, despite allegation that the petition art was considered during prosecution, “enough differences exist [between the two sets of claims] to convince us that the challenges presented in this petition are not cumulative to those already considered by the examiner.”). Most significantly, none of the claims prosecuted in the parent applications (other than claims of the ‘195 and ‘502 Patents) claim a “surface layer,” a “single drift layer,”

Petition for *Inter Partes* Review of U.S. Patent No. 11,121,222

and “at least one well region disposed in the single drift layer.” EX1001, Claim 44; EX1003, ¶¶179-181. And because none of the ground references (Payne, Sakai, Kawagoe) were cited in the ‘195 and ‘502 Patents, they were not considered during prosecution of the ‘195 and ‘502 Patents. *Id.* “Here, the Examiner did not consider [] the grounds asserted in the Petition, and certainly not with respect to the challenged claims” and therefore “there [is] no overlap between arguments made during examination and in the Petition.” *Bowtech Inc. v. MCP IP, LLC*, IPR2019-00383, Paper 14 at 5-6 (P.T.A.B. Aug. 6, 2019).

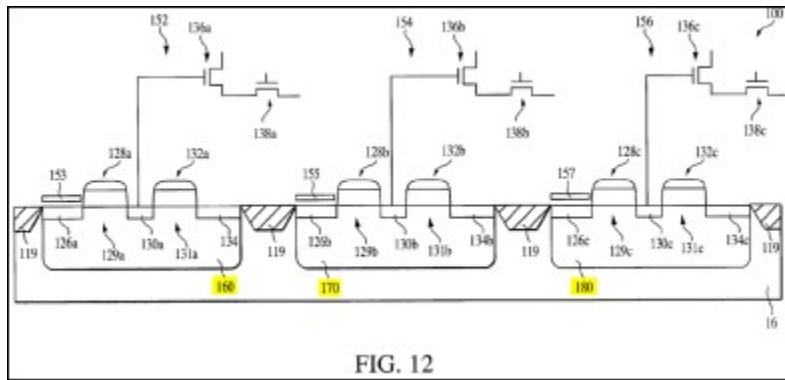
**Payne and Sakai are not cumulative with the Rhodes cited art** – The Challenged Claim is similar to claim 1 of the ‘195 Patent, which was the subject of *Samsung Electronics Co., Ltd. v. Greenthread LLC*, IPR2020-00289, before the Patent Trial and Appeal Board, filed December 23, 2019. In its POPR to the terminated IPR2020-00289 challenging claims of the ‘195 Patent, Patent Owner argued that Payne is cumulative with Rhodes on the alleged ground that the nested well structure of Payne is nothing more than a single well formed with multiple implants. *See* EX1016, 25-41. This is incorrect. EX1003, ¶¶179-191.

***First***, Sakai expressly discloses having a twin ***double well*** structure with a shallow ***well*** region disposed in a deep ***well*** region. EX1006, 1:57-67, 7:32-37, FIGS. 10D, 11E, 15. These well regions are all labeled as “P-WELL” or “N-WELL” in Sakai’s figures. *Id.* Sakai’s nested wells clearly do not form one single well. They are expressly disclosed and labeled as distinct wells. EX1003, ¶183.

**Second,** Payne's nested well structure, in which shallow wells are formed in deeper wells with *separate* implants *and* annealing steps, differentiates Payne from Rhodes which does not teach a nested well structure. EX1003, ¶¶184-185. As Payne describes and illustrates in Figures 2 and 5-9, the deep wells ("tub regions") of Payne's nested well structure are formed first, using their own specific masks, ion implantation and thermal drive-in process steps. EX1005, 3:17-4:30. The shallow wells ("surface regions") are then separately formed, using different masks, ion implantation and thermal drive-in process steps. EX1005, 4:31-5:17, 5:44-55. Payne's separately formed deep and shallow wells, such as wells 15 and 18, are not a single well formed using multiple implants. *Id.*

**Third,** Sakai likewise uses separate implants and annealing steps to form each well of its nested well structure. EX1006, 5:56-6:4, 6:24-28, 6:52-58, FIGS. 10A, 10B. A POSITA would have therefore understood Payne's tub and surface regions to constitute distinct wells just as Sakai used that term. EX1003, ¶186.

In contrast to Payne and Sakai's structures, Rhodes teaches a twin well architecture with side-by-side wells 160/170/180 (shown below) that Payne and Sakai seek to improve upon with their nested well structure. EX1011, [0064]; EX1005, 1:24-68; EX1006, 1:6-2:39.



EX1011, FIG. 12, [0064]. Rhodes does not mention or suggest (in paragraph [0064] or otherwise) forming a nested well structure, and thus does not teach a “well region disposed in [a] single drift layer.” EX1003, ¶¶187-188. And none of its figures shows a deep well and a shallow well. *Id.* This was the reason the Examiner allowed the claims of the ‘195 Patent to issue over Rhodes (and other art, including Kamins and Jastrzebski). EX1020, 346. Nowhere in the prosecution did the Applicant or Examiner discuss nested well structures, as Payne and Sakai disclose. Thus, there is no support for Patent Owner’s argument in the POPR that “it is reasonable to infer that the Examiner agreed with the argument Patent Owner makes explicitly herein that a multiple-implant well does not disclose a well region disposed in a single drift layer.” EX1016, 27.

Patent Owner also implied in its POPR that the Applicant overcame Rhodes-based rejections during prosecution by adding the “drift layer” limitation to the pending claims. EX1016, 22-24. This is incorrect. EX1003, ¶¶190-191. Applicant overcame Rhodes-based rejections on the basis that Rhodes is a “CMOS imaging device,” and by amending the claims to include a “graded dopant concentration in

the...active channel regions,” (a limitation that was later removed). EX1020, 94-96. The “drift layer” limitation was added much later in the process after several intervening rejections. There is no indication the Examiner specifically considered Rhodes in relation to the “drift layer” limitation, let alone the “well region disposed in the single drift layer” limitation.

**C. Neither Petitioner’s Concurrently Filed Petition nor Prior Terminated Petitions Warrant Denying Institution**

**Petitioner’s Concurrently Filed Petition (“Petition I”) -** Petitioner’s Concurrently Filed Petition (IPR2024-00673) (“Petition I”) challenges thirty-six other claims of the ’222 Patent that are significantly different in scope compared to Challenged Claim 44 of the instant Petition (“Petition II”), and relies on materially different prior art and grounds than those of the instant Petition II. For those reasons, *General Plastic* factors weigh strongly against discretionary denial. *Bumble Trading Inc. v. Match Grp., LLC*, IPR2019-01537, Paper 14, at 67 (P.T.A.B. Mar. 11, 2020) (“The Petitions in IPR2019-01538 and IPR2019-01537 are distinct in that no claim is addressed in both petitions. Accordingly, exercising our discretion not to institute one of the petitions would leave one set of claims unaddressed, despite our determination that Petitioner has more than established than a reasonable likelihood that Petitioner would prevail with respect to the challenged claims.”); *Peloton Interactive, Inc. v. iFit, Inc.*, IPR2022-00030, Paper 12, at 34 (P.T.A.B. Apr. 22, 2022) (granting institution where “claims 29 and 49 differ in at least four ways [from

claims challenged in a separate petition]. In our view, these significant differences tend to justify Petitioner's filing of multiple petition[s] to challenge different claims of the '062 patent.").

In *General Plastic*, the Board articulated seven non-exclusive factors to be considered in determining whether to exercise discretion to deny a petition when multiple petitions are filed to challenge the same patent:

- 1) "whether the same petitioner previously filed a petition directed to the same claims of the same patent";
- 2) "whether at the time of filing of the first petition the petitioner knew of the prior art asserted in the second petition or should have known of it";
- 3) "whether at the time of filing of the second petition the petitioner already received the patent owner's preliminary response to the first petition or received the Board's decision on whether to institute review in the first petition";
- 4) "the length of time that elapsed between the time the petitioner learned of the prior art asserted in the second petition and the filing of the second petition";
- 5) "whether the petitioner provides adequate explanation for the time elapsed between the filings of multiple petitions directed to the same claims of the same patent";
- 6) "the finite resources of the Board"; and

- 7) the statutory requirement “to issue a final determination not later than 1 year after institution of review.”

*See General Plastic Industrial Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 at 15–19 (PTAB Sept. 6, 2017) (precedential).

*General Plastic* Factor 1 weighs heavily in favor of institution. There is no overlap between the claims challenged in Petition I and Petition II because the instant Petition II challenges claim 44 of the ‘222 Patent, whereas the concurrent Petition I challenges 36 different claims (1-9, 13-28, and 32-42). Moreover, claim 44 is materially different from all other claims of the ‘222 Patent, including claims challenged in Petition I. Notably, claim 44 claims a “surface layer,” a “single drift layer,” and “at least one well region disposed in the single drift layer” that are not claimed in any other claim of the ‘222 Patent. EX1001, claims 1-44. Two petitions are therefore required to properly address those major differences in claim scope by using different, appropriately targeted, prior art. In particular, the primary references used in this Petition II (Payne and Sakai) disclose CMOS devices with nested well structures, whereby shallow wells are disposed in deep wells. *Supra* Sections X.A.1.e, X.A.1.g, X.B.1.e, X.B.1.g. Payne’s and Sakai’s nested well structures are needed to properly address the claimed “single drift layer” and “well region disposed in the single drift layer” unique to the Challenged Claim 44 of the instant Petition II. In fact, Payne and Sakai disclose those claimed structures. *Id.* Payne and Sakai are

not used in Petition I because the claims challenged in Petition I are materially different in claim scope; they do not claim the nested structures claimed in claim 44 but, on the other hand, claim a variety of structures and devices such as a p-type substrate, a non-epitaxial substrate, an isolation region, DRAM, flash memory, digital logic and capacitors, and a central processing unit (*see, e.g.*, claims 2, 3, 6, 14, 16-18) that are better addressed using the different prior art and grounds of Petition I.

*General Plastic* Factors 2 and 4 are neutral because, as explained above, the Payne and Sakai prior art relied on in the instant Petition II are much better suited to address the “single drift layer” and “at least one well region disposed in the single drift layer” requirements of Challenged Claim 44 than the primary ground references relied on in Petition I (Kawagoe, Wieczorek). Thus, timing considerations are immaterial. *Peloton*, at 30 (“Petitioner’s explanation for not previously presenting the grounds set forth in the present Petition [] outweighs the passage of time between Petitioner’s learning of [the prior art] and the filing of the present Petition.”).

*General Plastic* Factor 3 weighs in favor of institution as well. As of the filing date of the instant Petition II, Patent Owner has not filed its Preliminary Response (POPR) to Petition I, and the Board has not issued an institution decision addressing Petition I either.

*General Plastic* Factor 5 is not applicable because there is no overlap between the claims challenged in Petition I and Petition II.

*General Plastic* Factors 6 and 7 also weigh in favor of institution. Granting Petition II would allow for an efficient use of the Board's finite resources because the sole Challenged Claim is distinct from the claims challenged in Petition I. Additionally, as with the present petition, Petitioner's Concurrently Filed Petition is filed with a motion for joinder to join an already instituted proceeding (IPR2023-01242).

**Prior Terminated Petitions Do Not Warrant Denying Institution -**

Petitioner is not a related company to those who have previously challenged the '222 Patent. In addition, Petitioner is a defendant in the District Court Case, and Petitioner therefore would potentially be severely prejudiced if the instant Petition II is not instituted. *Apple Inc. v. Uniloc 2017 LLC*, IPR2019-01667, Paper 7, 11-12 (P.T.A.B. Apr. 21, 2020).

Respectfully submitted,

Dated: March 12, 2024

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**CERTIFICATION UNDER 37 CFR § 42.24**

Under the provisions of 37 CFR §42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter partes* Review totals 12,846 words, which is less than the 14,000 allowed under 37 CFR §42.24.

Dated: March 12, 2024

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**CERTIFICATE OF SERVICE**

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on March 12, 2024, a complete and entire copy of this Petition for *Inter partes* Review and all supporting exhibits were provided by Express Mail, to the Patent Owner by serving the correspondence address of record as follows:

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